

Average Current Mode Controlled Power Factor Correction Converter using TMS320LF2407A

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ABSTRACT

Low cost, high performance DSP controllers with integrated peripherals such as, analog-to-digital (A/D) converters and pulse width modulator (PWM), have enabled the power supply designers with a new tool for implementing control for their power conversion functions. However, the power designers with mostly analog control experience are faced with new challenges as they start to adopt this new technology and make transition from the existing analog space to its new digital environment.

This application report identifies some of the basic differences between the two approaches and shows a step-by-step implementation of a DSP controlled average current mode power factor correction (PFC) converter. Different control loop parameters in the analog control space are redefined prior to their digital implementation. The loop is analyzed and the required voltage and current loop compensators are derived. Finally, the discretization of these compensators and their implementation in software are also presented.

Contents

1	Introduction	2
2	PFC Stage Hardware Interface to TMS320LF2407A	3
3	PFC Stage Digital Controller Design	4
4	PFC Stage Digital Controller Design Example	10
5	Experimental Results	13
6	References	14

List of Figures

1	TMS320LF2407A Controlled Power Factor Correction (PFC) Stage	3
2	Control Loop Block Diagram of the DSP Controlled PFC Stage	4
3	Frequency and Average Component Calculation	6
4	Bode Plot For Current Loop Compensation.....	9
5	Input Current and Voltage Waveforms (224Vrms).....	13
6	Input Current and Voltage Waveforms (100Vrms).....	14

1 Introduction

Digital Signal Processors (DSPs) designed for closed loop control implementations are extensively used in areas of motor control, uninterruptible power supplies (UPS), and motion control applications.

With the availability of low cost, high performance DSP controllers featuring high CPU bandwidth and integrated power electronics peripherals such as, analog-to-digital (A/D) converters, pulse width modulator (PWM) with built-in dead-time and asynchronous power stage protection, power supply designers have started to consider this technology as a suitable option for their real-time power conversion and control applications.

Compared to traditional analog control, DSP controllers provide many distinctive advantages:

- standard control hardware design for multiple platforms
- less susceptibility to aging and environmental variations
- better noise immunity
- ease of implementations of sophisticated control algorithms
- flexible design modifications to meet a specific customer need
- single chip solution for both control and communication functions

The use of DSPs in power supply applications brings new challenges to many analog designers in their effort to change the design from the existing analog space to its new digital environment.

For a DSP controlled power supply, many pertinent factors in the design and implementation of its digital control loop need to be addressed. Redefinition of the analog control blocks and the associated parameters in digital domain are essential for the analog designers to change the control design from the analog hardware to its digital software counterpart. This application report discusses the different implementation aspects of a DSP based average current mode control of a power factor correction (PFC) stage with input voltage feed-forward. Different control loop parameters in analog domain are redefined prior to their digital implementation. The modifications in the analog feed-forward circuits and its implementation in software are discussed in detail. For the 16-bit fixed-point DSP(TMS320LF2407A) based implementation, the scaling and normalization needed to implement the universal input operating range (85Vac-265Vac, 47Hz-63Hz) is explained. The loop is analyzed in s-domain and the required voltage and current loop compensators are derived. The discretization of these compensators and their implementation in software are also presented.

An example design is explained to illustrate the DSP implementation of the PFC converter. Finally, test results from a laboratory prototype are presented to validate the performance of the digital implementation.

2 PFC Stage Hardware Interface to TMS320LF2407A

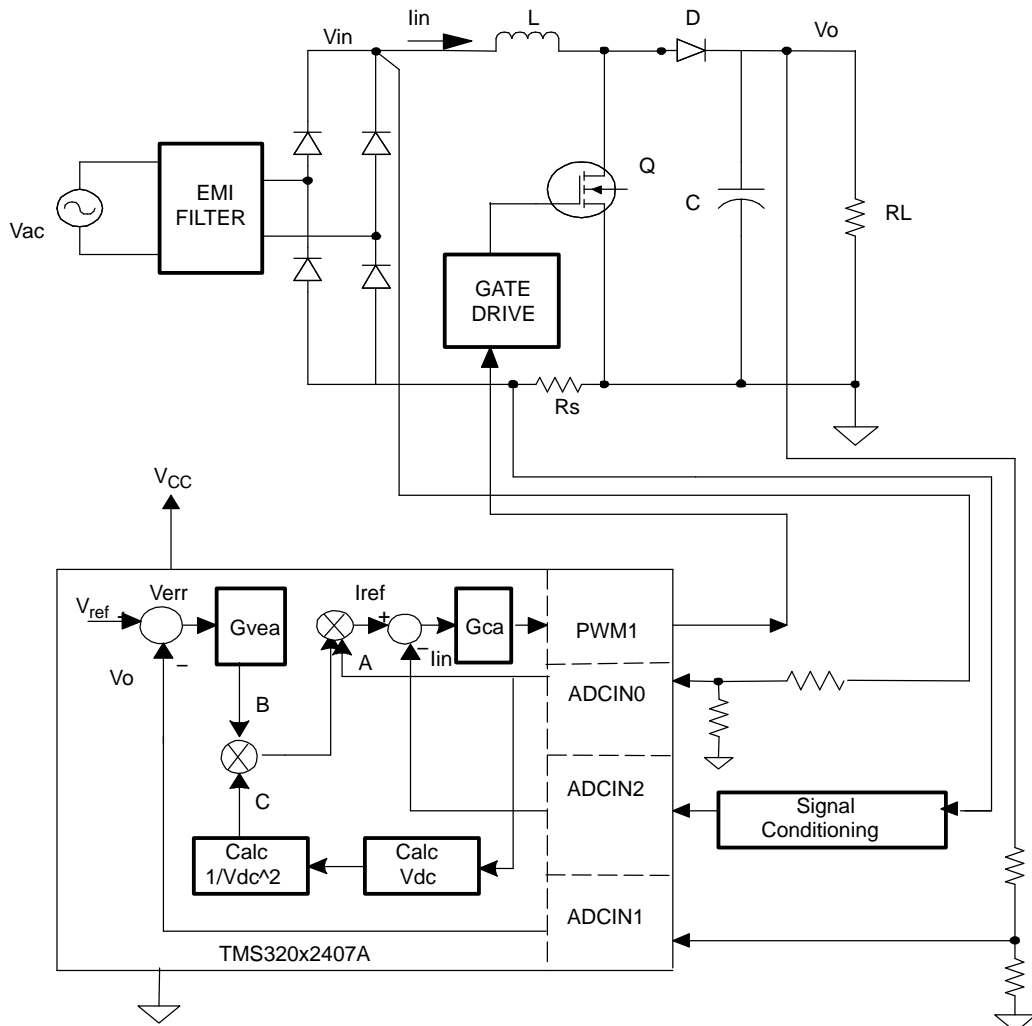


Figure 1. TMS320LF2407A Controlled Power Factor Correction (PFC) Stage

Figure 1 shows a power factor correction (PFC) stage interfaced to a TMS320LF2407A DSP. This is an ac-dc boost converter stage, which converts the ac input voltage to a high voltage dc bus and maintains sinusoidal input current at high input power factor. As indicated in Figure 1, three signals are required to implement the control algorithm. These are, the rectified input voltage V_{in} , the inductor current i_{lin} , and the dc bus capacitor voltage V_o . The converter is controlled by two feedback loops. The average output dc voltage is regulated by a slow response 'outer loop'; whereas, the inner loop that shapes the input current is a much faster loop.

The instantaneous signals V_{in} , V_o and i_{lin} , are all sensed and conditioned by the respective voltage and current sense circuits. The sensed signals are then fed back to the DSP via three ADC channels ADCIN0, ADCIN1, and ADCIN2 respectively. The rate at which these signals are sensed and converted by the ADC is called the control loop sampling frequency f_s . The digitalized sensed bus voltage V_o is compared to the desired reference bus voltage V_{ref} . The difference signal ($V_{ref} - V_o$) is then fed into the voltage loop controller G_{vea} . The digitized output of the controller G_{vea} , indicated as 'B', is multiplied by two other components, 'A' and 'C', to generate the reference current command for the inner current loop. In [Figure 1](#), the component 'A' represents the digitized instantaneous sensed signal V_{in} . The component 'C' is calculated as,

$$C = \frac{1}{V_{dc} * V_{dc}}$$

where, V_{dc} is the calculated average component of the sensed digitized signal

V_{in} . In [Figure 1](#), I_{ref} is the reference current command for the inner current loop. I_{ref} has the shape of a rectified sinewave and it's amplitude is such that it maintains the output dc voltage at a reference level V_{ref} , against variation in load and fluctuation in line voltage. The sensed digitized inductor current i_{lin} is compared with the reference current I_{ref} . The difference between I_{ref} and i_{lin} is passed into the current controller G_{ca} . The output of this controller is finally used to generate the PWM duty ratio command for the PFC switch.

3 PFC Stage Digital Controller Design

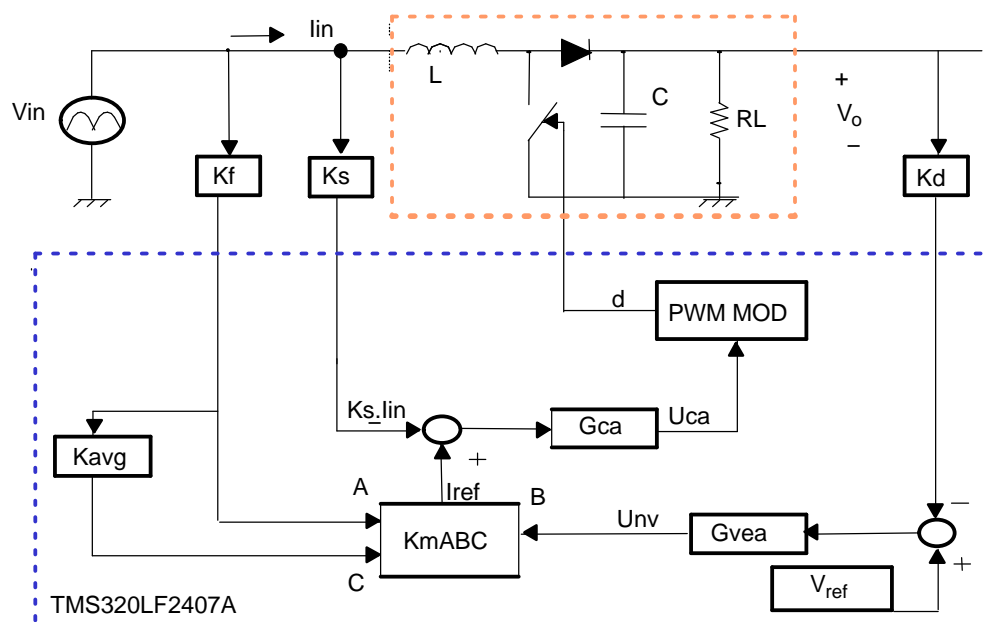


Figure 2. Control Loop Block Diagram of the DSP Controlled PFC Stage

[Figure 2](#) shows the control loop block diagram of the DSP controlled PFC converter shown in [Figure 1](#). In this figure, the voltage and current sense/conditioning circuits are replaced by their respective gain blocks. These blocks are indicated as K_f , K_s , and K_d . The multiplier gain K_m is also added to the control block. K_m allows adjustments of the reference signal I_{ref} based on the converter input operating voltage. The inner loop is the current loop, which is programmed by the reference current signal I_{ref} . The input to the current loop power stage is the duty ratio command d and it's output is the inductor current i_{lin} . The current controller G_{ca} is designed to generate the appropriate control output U_{ca} such that the inductor current i_{lin} follows the reference current I_{ref} . The outer voltage loop is programmed by the reference voltage command V_{ref} . The input to the voltage loop power stage is U_{nv} (voltage controller output) and its output is the dc bus voltage V_o . The voltage controller G_{vea} is designed to generate the appropriate U_{nv} to

control the amplitude of the reference current I_{ref} such that for the applied load current and line voltage, the bus voltage V_o is maintained at the reference level. For this control implementation it is necessary to calculate these voltage and current controllers. This in turn requires the identification of some of the blocks in [Figure 1](#), especially, when this control is implemented in software using a fixed point DSP controller such as TMS320LF2407A.

3.1 Voltage and Current Sensing Gain

For the PFC stage shown in [Figure 1](#), the instantaneous rectified input voltage V_{in} and the power factor corrected rectified input current i_{in} are given by,

$$V_{in} = V_m \sin 2\omega t, 0 \leq V_m \leq V_{max}, \text{ and, } i_{in} = I_m \sin 2\omega t, 0 \leq I_m \leq I_{max}$$

Where, V_{max} and I_{max} are the absolute maximum values of the peak amplitudes V_m and I_m respectively. For a DSP based PFC implementation these signals are sensed by the on-chip A/D converter, with appropriate external conditioning circuits added to each channel, in order to bring these signals within the range of the A/D converter. The user software reads the converted signals i.e., the digitized signals, from the A/D converter result registers and saves them in temporary memory locations in a suitable fixed-point format. For a fixed point DSP like TMS320LF2407A, these digitized signals are represented as numbers with finite word length. Of the 16 available data bits of TMS320LF2407A, 15 least significant bits(LSB) are used to represent the magnitude of the signal and the most significant bit(MSB) is used to represent its sign. It is, therefore, necessary to select the range of the signal to be converted and then map the full range of the converted results within the full range of the fixed-point representation. For TMS320LF2407A, this range is 0 to 32767 for the positive going signals. Once this mapping is done correctly, the next step is to choose a suitable fixed-point arithmetic notation for these digitized signals. For a 16-bit DSP, it is advantageous to use Q15 notation as the fixed-point representation for these signals. With this representation, the numbers within the range 0 to 32767, represents an absolute value between 0 to 1. This means, with Q15 representation, the voltage and current signals are automatically saved as per-unit (pu) numbers normalized with respect to their own maximum values.

Using this approach, the feed-forward voltage sensing circuit in [Figure 2](#) yields,

$$A = V_{in} K_f \Rightarrow A|_{max} = V_{max} K_f \Rightarrow 1 = V_{max} K_f$$

where, V_{max} is the absolute maximum amplitude of the rectified input voltage V_{in} . Therefore, the feed-forward voltage sensing gain K_f is defined as,

$$K_f = 1/V_{max}$$

In a similar manner the current sensing gain is calculated as,

$$K_S = 1/I_{max}$$

where, I_{max} is the absolute maximum amplitude of the rectified input current i_{in} . The dc bus voltage sensing gain is calculated as,

$$K_d = 1/V_{o,max}$$

where, $V_{o,max}$ is the absolute maximum value of the dc bus voltage. Note that, these definitions for the gain blocks are applicable only if Q15 notation is used for the converted signals and their full range is mapped over the full fixed-point range as explained earlier.

3.2 Software Implementation of Input Voltage Feed-forward

Input voltage feed-forward causes power input to remain constant at a specified level (determined by the load) regardless of line voltage changes. To implement this, a voltage V_{dc} proportional to rms input voltage is squared and divided into the control level. So we define the signal needed for feed-forward implementation as,

$$C = \frac{1}{V_{dc} * V_{dc}}$$

This is the same signal mentioned before in Section 2. This is computed in software from the measurement of the rectified input voltage signal V_{in} . To calculate the average component V_{dc} of the rectified input V_{in} , it is necessary to calculate the frequency $f (=1/T)$ of the signal and then integrate the signal over one period. This is depicted in Figure 3.

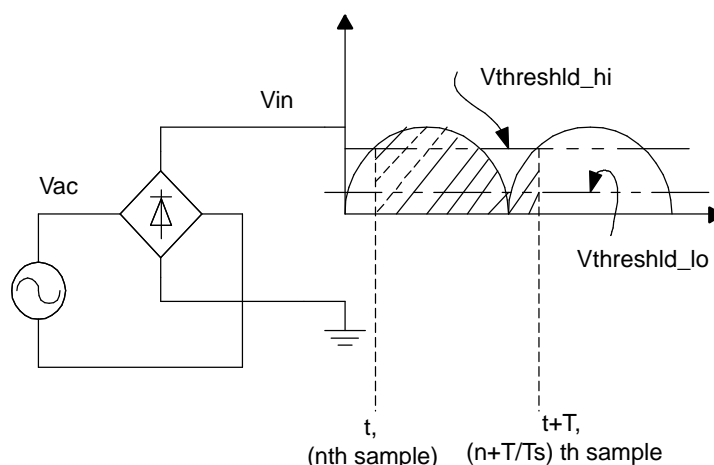


Figure 3. Frequency and Average Component Calculation

3.2.1 Frequency Calculation

During the software implementation of the frequency and the subsequent average V_{in} calculation, the number of samples (N) of V_{in} is counted and saved every time the signal crosses over a threshold level. In Figure 3 this level is indicated as “ $V_{threshld_hi}$ ”. The lower threshold level “ $V_{threshld_lo}$ ” is used to achieve noise immunity. This means $N=T/T_s$, is the number of times the signal V_{in} is sampled over its one period(T) when the sampling loop frequency is $f_s=1/T_s$. Once N is known, the per unit frequency f_{pu} is calculated as,

$$f_{PU} = \frac{f}{f_{max}} = \frac{\frac{1}{T}}{\frac{1}{T_{MIN}}} = \frac{\frac{1}{NT_s}}{\frac{1}{N_{MIN} T_s}} = \frac{N_{MIN}}{N}$$

Where, f_{max} is the maximum frequency of V_{in} and N_{min} is the minimum number of samples of V_{in} over one period(corresponding to it's max frequency). The user software that calculates the frequency, uses the value of N and first calculates an intermediate value $1/N$. Then, this is multiplied by N_{min} to find the pu frequency. Now, in order to save the intermediate value $1/N$ with maximum accuracy without causing an accumulator overflow, it is essential to know the value of N_{min} , see *Motor Speed Measurement Considerations Using TMS320C24x DSPs* (SPRA771). This means that the user should select the maximum frequency of the signal to be measured, and based on that and the value of T_s , also determine N_{min} . Once N_{min} is known, the quantity $1/N$ can be saved with maximum accuracy with the appropriate fixed-point representation. For example, for a PFC converter with input operating frequency range of 47Hz ~ 63Hz, the maximum input frequency can be chosen as 70Hz. Then with $f_{max}=140$ Hz (twice the input frequency) and the value of T_s known from the sampling loop implementation, N_{min} can be easily calculated.

3.2.2 Feed-forward Component Calculation

Once the frequency of the signal V_{in} is known, its average component is calculated using,

$$V_{dc} = \frac{1}{T} \int_t^{t+T} V_{in} \cdot dt$$

where, T is the time period corresponding to the frequency f of the rectified input voltage V_{in} . In discrete form the average component is expressed as,

$$V_{dc} = \frac{1}{T} \sum_{i=n}^{i=n+T/Ts} V_{in}(i) \times Ts = \sum_{i=n}^{i=n+T/Ts} V_{in}(i) \times \frac{1}{T/Ts} = \sum V_{in}(i) \times \frac{1}{N}$$

where, $V_{in}(i)$ represents the digitized i -th sample of V_{in} .

Again when N is known, the integral under the V_{in} curve is computed by calculating the sum of the products

$$\sum V_{in}(i) \times \frac{1}{N}$$

over one period. This gives the average component V_{dc} of the input rectified voltage V_{in} . Since V_{in} is measured as a per unit value normalized with respect to its maximum value V_{max} , this calculated value of V_{dc} is also a pu quantity with a base value of normalization of V_{max} . However, for a sine-wave input voltage the maximum value of the average component V_{dc} is only $2V_{max}/\pi$. Therefore, to achieve better accuracy in the fixed-point representation of V_{dc} , the previously calculated value is converted to a pu quantity normalized with respect to its own maximum value. This value is given by:

$$V_{dc1} = \sum V_{in}(i) \times \frac{1}{N} \times \frac{V_{max}}{(2V_{max}/\pi)}, = V_{dc} \times \frac{\pi}{2}$$

Now, in calculating the inverse, V_{inv} , of V_{dc1} , i.e., $V_{inv}=1/V_{dc1}$, it is clear that V_{inv} is maximum when V_{dc1} is minimum and vice versa. Therefore, to achieve better accuracy in the fixed-point representation of V_{inv} , it is necessary to represent this with a pu value normalized with respect to its own maximum value. For a sine-wave input voltage, the minimum value of V_{dc} is $2V_{min}/\pi$, where, the minimum amplitude, V_{min} , of the rectified input voltage is selected based on the input operating voltage range of the PFC converter. For example, to operate the PFC converter with a low line voltage of 90Vrms, the chosen value of V_{min} should be less than or equal to 127V. With the selected value of V_{min} , the maximum value of V_{inv} is $(\pi/2V_{min})$ and the corresponding pu value of V_{inv} with respect to its own maximum value is:

$$V_{inv} = \frac{1}{V_{dc1} \times V_{dc_MAX}} \times \frac{1}{V_{inv_MAX}} = \frac{1}{V_{dc1}} \times \frac{V_{dc_MIN}}{V_{dc_MAX}} = \frac{1}{V_{dc1}} \times \frac{V_{min}}{V_{max}}$$

Once V_{inv} is calculated with the maximum accuracy, the feed-forward component C can be calculated with the same accuracy as,

$$C = V_{inv}^2$$

3.3 The Multiplier Gain K_m

The multiplier gain K_m is adjusted such that at the minimum input voltage, the reference current I_{ref} is at its maximum when the PFC converter delivers the maximum load. From the block diagram in [Figure 2](#),

$$I_{ref} = K_m ABC = K_m (V_{in} K_f) (U_{nv}) V_{inv}^2$$

With the current loop closed,

$$I_{ref} = I_{in} K_S \Rightarrow I_{ref_MAX} = I_{MAX} K_S = 1$$

As explained in [Section 3.2.2](#), at the minimum operating voltage $V_{inv} = 1$. Again, for full load power the voltage controller output will be at its maximum, i.e., $U_{nv} = 1$. Therefore, at minimum operating voltage, to generate maximum reference current the required value of K_m is,

$$K_m = I_{ref\ MAX} \left[\frac{1}{V_{min} K_f U_{nv} V_{inv}^2} \right] = \frac{V_{max}}{V_{min}}$$

3.4 Voltage and Current Loop Compensators

High frequency approximation of the current loop power stage ($1/sC = 0$) is,

$$G_{id} = \frac{\hat{I}_{in}}{\hat{d}} = \frac{V_O}{sL}$$

From the PFC control block diagram in [Figure 2](#), the loop gain equation for the current loop is,

$$T_i = G_{id} K_S G_{CA} F_m$$

Where the modulator gain is,

$$F_m = \frac{\hat{d}}{\hat{U}_{CA}}$$

This modulator is implemented partly in software and partly using the DSP PWM hardware. The software uses the modulator input, i.e., the current controller output U_{ca} , and calculates a duty ratio value for the PWM hardware module in TMS320LF2407A. The PWM hardware uses the duty ratio value and generates the appropriate PWM signal for the PFC switch. The software is implemented such that, when the modulator input, U_{ca} , is 1, the modulator output, i.e., the PWM duty ratio d , is 100%. This means, the modulator gain in this case is $F_m = 1$. Therefore, for a current loop crossover frequency of f_{ci} , the required current error amplifier compensator is,

$$G_{CA} = \frac{2\pi f_{ci} L}{K_S V_O}$$

Once the current loop is closed, the voltage loop power stage transfer function can be calculated as,

$$G_{VC} = \hat{V}_O / \hat{U}_{nv} = \frac{K_m}{2K_f K_S} \left[\frac{V_{min}}{V_{max}} \right]^2 \frac{Z_f}{V_O}$$

where, Z_f represents the equivalent impedance of the parallel branch consisting of the bus capacitor C , the PFC stage output impedance r_o and the load impedance Z_L , and is given by,

$$Z_f = \frac{1}{\frac{1}{r_o} + \frac{1}{Z_L} + sC}$$

For a constant power load P_o , the load impedance Z_L and the output impedance r_o are related by,

$$Z_L = \frac{-V_O^2}{P_o} = -r_o$$

For resistive load R_L , the load impedance Z_L and the output impedance r_o are related by,

$$Z_L = R_L = \frac{V_O}{I_O} = r_o$$

From the block diagram in Figure 2, the loop gain equation for the voltage loop is,

$$T_V = K_d G_{VEA} G_{VC}$$

Using this loop gain equation, for a voltage loop crossover frequency of f_{cv} , the required voltage error amplifier compensator is,

$$G_{VEA} = \frac{2K_f K_S \left[\frac{V_{\max}}{V_{\min}} \right]^2}{K_d K_m} \frac{V_O}{Z_f} \Big|_{f=f_{cv}}$$

3.5 Software Implementation of the Voltage and Current Loop Compensators

The voltage and current loop controllers, given in previous section, are transformed to an equivalent digital form as explained below, before they are implemented in software using TMS320LF2407A. For example, the current controller can be written as,

$$G_{CA}(s) = K_P \times \frac{1 + T_I s}{T_I s} = K_P + \frac{K_I}{s} = \frac{U_{CA}(s)}{E(s)}$$

Where, K_p is the magnitude of the current compensator calculated in Section 3.4 and E is the current error signal.

The location of the compensator zero, $\omega_z = 2\pi f_z = 1/T_I$, is usually chosen somewhere below the crossover frequency f_{ci} to maintain adequate phase margin. The current loop compensator design is illustrated graphically by the current loop bode plot shown in Figure 4. The top trace in Figure 4 represents the gain plot for all the control blocks in the current loop, i.e. G_d , F_m and K_s , except the current compensator G_{ca} . The gain plot for the compensator G_{ca} , shown in the middle trace in Figure 4, is derived to achieve the desired loop gain T_i shown in the bottom trace. In Figure 4 the power stage has a -1 slope. Therefore, placing the compensator zero f_z , at the desired crossover frequency of f_{ci} , results in a phase margin of 45 deg. However, in a digital implementation some of this phase margin can be lost because of the control loop sampling and computation delay. To compensate for this loss, it might be necessary to place the compensator zero somewhere below the crossover frequency as indicated in Figure 4.

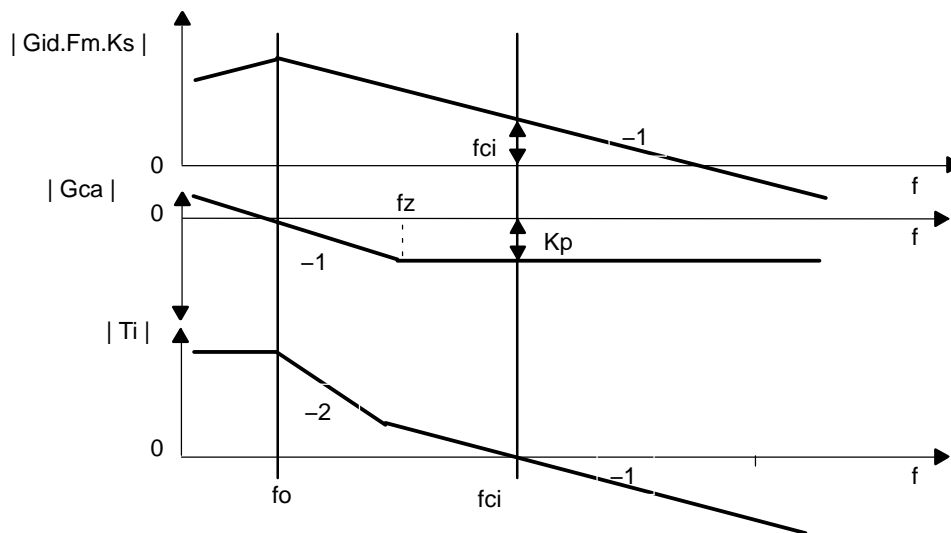


Figure 4. Bode Plot For Current Loop Compensation

In discrete form, the current controller mentioned before, can be expressed as,

$$U_{CA}(n) = K_P E(n) + K_I T_S \sum_{j=0}^n E(j)$$

where, T_s is loop sampling time. This is implemented with output saturation and integral component correction using the following three equations:

PFC Stage Digital Controller Design Example

$$\begin{aligned}
 U_{CA}(n) &= K0 * E(n) + I(n - 1), \\
 I(n) &= I(n - 1) + K1 * E(n) + Kcorr * Epi \\
 Epi &= Us - U_{CA}(n)
 \end{aligned}$$

where,

$$Us = U_{CAmax} \text{ when } U_{CA}(n) \geq U_{CAmax}$$

$$Us = U_{CAmin} \text{ when } U_{CA}(n) \leq U_{CAmin}$$

otherwise,

$$Us = U_{CA}(n)$$

Here, Us represents the final output of the current controller with saturation and integral component correction. The coefficients in the last three equations, representing the discrete form of the analog current compensator, are defined as,

$$K0 = K_P, K1 = K_I T_S, K_{CORR} = K1/K0$$

These equations can be easily implemented in software using TMS320LF2407A.

4 PFC Stage Digital Controller Design Example

The system parameters used in this design are:

Output power $P_o=825$ W,
DC bus voltage $V_o =380$ V,
Switching frequency $f_{sw}=120$ kHz;
Digital loop sampling frequency $f_s = 60$ kHz
 $L=100$ uH, $C=390$ uF,
Volt loop bandwidth $f_{cv}=10$ Hz, Current loop bandwidth $f_{ci}=8$ kHz,
Maximum frequency of rectified input voltage $f_{max}=200$ Hz
 $V_{max}=410$ V, $V_{min}=109.95$ V, $V_{omax}=410$ V

To deliver the maximum output power at the minimum input voltage, the maximum value of the input current (neglecting the losses in the PFC converter) is, $I_{max}=2P_o/V_{min} = 15$ A Different gain parameters are calculated as,

$$K_f = 1/410, K_d = 1/410, K_s = 1/15, K_m = 410/109.95 = 3.7286$$

4.1 Current Controller Implementation Example

For $f_{ci} = 8$ kHz, the magnitude of the current controller is, $G_{CA} = 0.1985$ Set current loop PI compensator zero at 800Hz. So, the integral time constant for the current compensator is, $T_{IC} = 1/(2\pi \cdot 800) = 198.94 \times 10^{-6}$ Therefore, the complete current loop controller is,

$$G_{CA}(s) = 0.1985 \times \frac{1 + 198.94 \times 10^{-6}s}{198.94 \times 10^{-6}s}$$

$$\Rightarrow G_{CA}(s) = K_{Pi} + \frac{K_{Ii}}{s} = \frac{U_i(s)}{E_i(s)}$$

where, $K_{Pi} = 0.1985$ and $K_{Ii} = 997.77$

The discrete controller is implemented using the following equations,

$$U_i(n) = K0i * E_i(n) + I_i(n - 1),$$

$$I_i(n) = I_i(n - 1) + K1i * E_i(n) + Kcorri * Epii$$

$$Epii = Usi - U_i(n)$$

where,

$$U_{si} = U_{i_{\max}} \text{ when } U_i(n) \geq U_{i_{\max}}$$

$$U_{si} = U_{i_{\min}} \text{ when } U_i(n) \leq U_{i_{\min}}$$

otherwise,

$$U_{si} = U_i(n)$$

The coefficients for the discrete current controller are,

$$K_{0i} = K_{P_i} = 0.1985 = 6504(Q15)$$

$$K_{1i} = K_{I_i} T_S = 0.016629 = 545(Q15)$$

$$K_{corri} = \frac{K_{1i}}{K_{0i}} = 0.08376 = 2745(Q15)$$

where, $T_S = 16.667 \times 10^{-6}$ sec.

The code segment that implements the above controller is given below:

```

PFC_I_CONTROL_INIT:
;PFC current control loop initialization
    LDP    # K0i
    SPLK  #6504,K0i          ;Q15
    SPLK  #545,K1i          ;Q15
    SPLK  #2745,Kcorri      ;Q15
    RET
PFC_I_CONTROL:
;PFC current control loop using feed-forward technique
    SETC  SXM
    SETC  OVM
    spm  #0
    LDP  #Iref
LACC  Iref          ;Q15
SUB   Ipfc         ;Q15
SACL  En0i         ;Q15
LACC  Uni,15       ;Q30,32-bit
LT    En0i         ;Q15
MPY   K0i          ;Q15*Q15
APAC  #Q30
SACH  GPR0_pfc    ;Q31
ADDH  GPR0_pfc    ;Q31
SACH  Upii        ;Q15
SACH  Usi         ;Q15
UiMAX .set 7ffeh
UiMIN .set 0
    LACC  Upii
    BCND  SAT_UiMIN, LT ;
    LACC  Upii
    SUB   #UiMAX
    BCND  SAT_UiMAX, GEQ ;
    B     FWD_i
SAT_UiMIN SPLK #UiMIN,Usi
B         FWD_i
SAT_UiMAX SPLK #UiMAX,Usi
FWD_i:   LACC  Usi          ;Q15
SUB   Upii          ;Q15
SACL  EpII          ;Q15
LT    EpII          ;Q15
MPY   Kcorri        ;Q15
LTP   En0i          ;Q15
MPY   Kli           ;Q15
APAC  #Q30
ADD   Uni,15
SACH  GPR0_pfc     ; Q31
ADDH  GPR0_pfc     ; Q31
  
```

```
SACH    Uni                ;Q15, Controller final output
RET
```

4.2 Voltage Controller Implementation Example

For constant power load, $ZL = -175.03$. For $f_{cv} = 10\text{Hz}$, the magnitude of the voltage controller is, $G_{VEA} = 4.63$. Set the volt loop PI compensator zero at 10Hz . Then the integral time constant is, $T_{IV} = 1/(2\pi \cdot 10) = 15.9155 \times 10^{-3}$. Therefore, the complete voltage loop controller is,

$$G_{vea}(s) = 4.7517 \times \frac{1 + 15.9155 \times 10^{-3}s}{15.9155 \times 10^{-3}s}$$

$$\Rightarrow G_{vea}(s) = K_{Pv} + \frac{K_{Iv}}{s} = \frac{Uv(s)}{Ev(s)}$$

where, $K_{Pv} = 4.63$ and $K_{Iv} = 290.91$

The discrete controller is implemented using the following equations,

$$Uv(n) = K0v * Ev(n) + Iv(n - 1),$$

$$Iv(n) = Iv(n - 1) + K1v * Ev(n) + Kcorr * Epiv$$

$$Epiv = Usv - Uv(n)$$

where,

$$Usv = Uv_{max} \text{ when } Uv(n) \geq Uv_{max}$$

$$Usv = Uv_{min} \text{ when } Uv(n) \leq Uv_{min}$$

otherwise,

$$Usv = Uv(n)$$

The coefficients for the discrete voltage controller are,

$$K0v = K_{Pv} = 4.7517 = 19463(Q12)$$

$$K1v = K_{Iv} T_S = 0.004976 = 163(Q15)$$

$$Kcorr = \frac{K1v}{K0v} = 0.001047 = 34(Q15)$$

where, $T_S = 16.667 \times 10^{-6}$ sec.

The code segment that implements the above controller can be written in the same way as shown in [Section 4.1](#).

5 Experimental Results

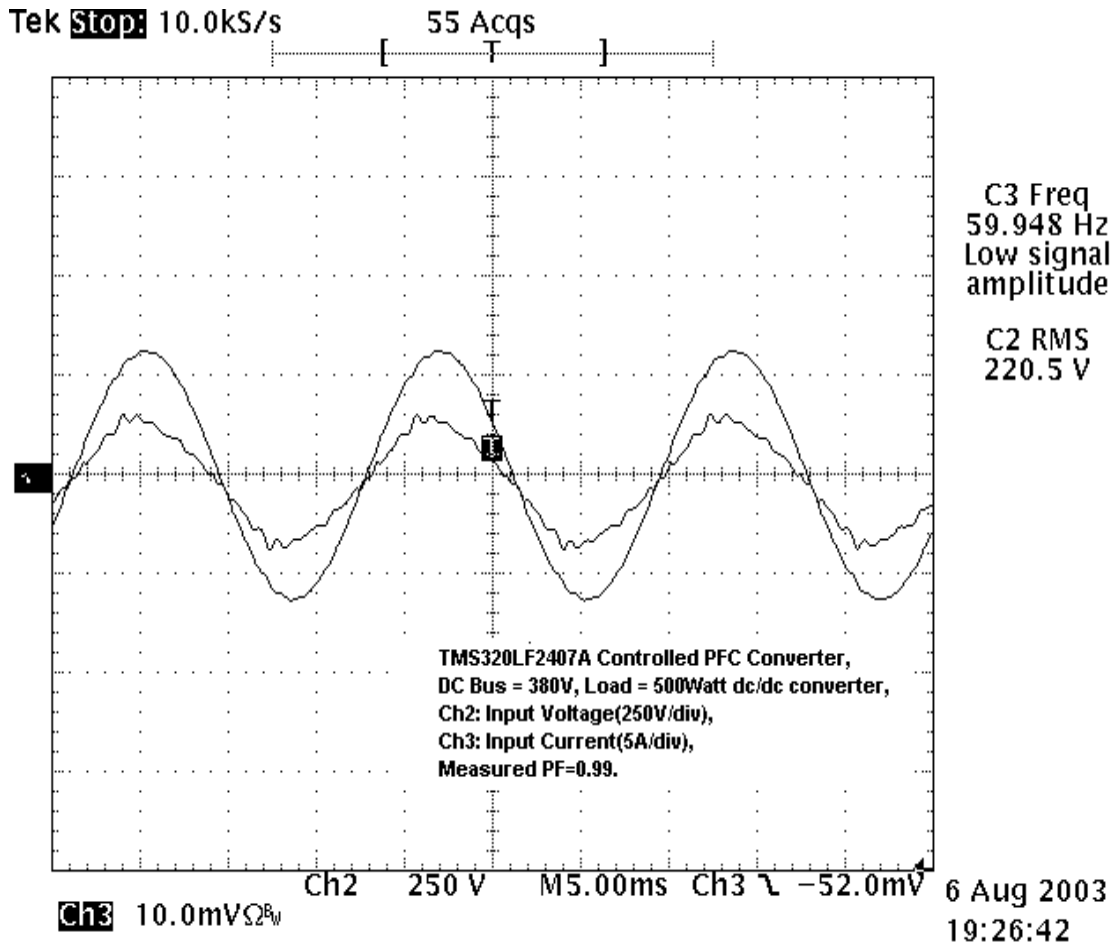


Figure 5. Input Current and Voltage Waveforms (224Vrms)

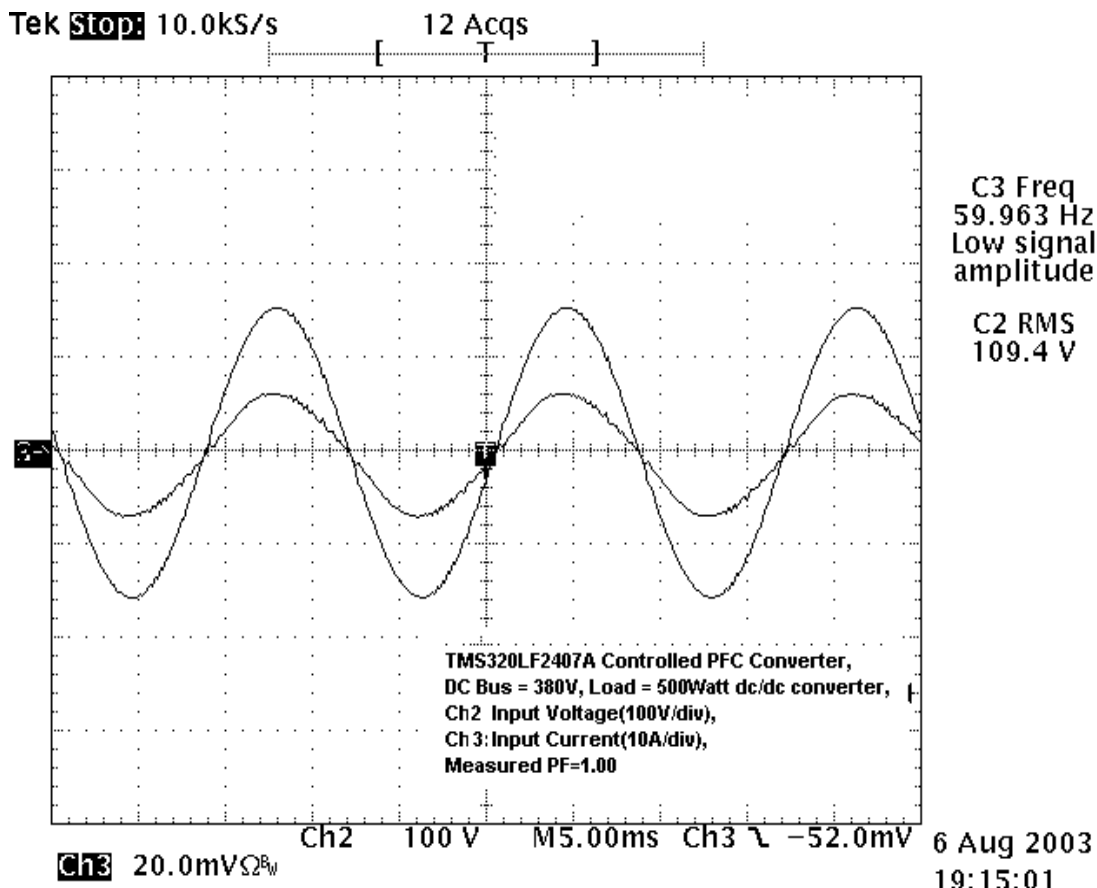


Figure 6. Input Current and Voltage Waveforms (100Vrms)

Figure 5 shows the input current (5A/div) and input voltage (224Vrms) waveforms of the PFC converter. Figure 6 shows the same waveforms for the same output load, but at a different input voltage (100Vrms). In this case, the PFC stage is used to drive a dc/dc stage, which delivers 48V output at 10A of load current.

6 References

1. L.H. Dixon, "Average Current Mode Control of Switching Power Supplies", Unitrode Power Supply Design Seminar Manual SEM700, 1990
2. R.B. Ridley, "Average small-signal analysis of the boost power factor correction circuit", Proceedings of the Virginia Power Electronics Center Seminar (VPEC), Blacksburg, VA, Sept., 1989.
3. *Motor Speed Measurement Considerations when Using TMS320C24x/24xx* (SPRA771).

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