Connecting an 802.11b WLAN Card to the OMAP5910

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ABSTRACT

There are numerous applications that require the addition of an 802.11B WLAN to the OMAP5910. While the OMAP5910 does not easily support a PCARD or compact flash interface, the TI based WLAN card does have a mode that works very well for interconnection to the OMAP5910. This application note describes how, by using this mode, the TI-based 802.11 WLAN card can be connected to the OMAP5910 processor with a minimum of external logic.

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1   WLAN Basics

Before we discuss the details of how to add WLAN to the OMAP5910, we should mention some wireless basics. Some of the wireless technologies in use today are:

- Wireless personal area networks (WPAN) for the interconnection of devices separated less than 50 meters away (PCs, PDAs, printers).

  Bluetooth: 1 Mbps over 10 to 30 meters

- Wireless LAN (WLAN) for interconnection of devices in a larger area (about 100 meters), configuring a local network like an "Ethernet without wires."

  - HomeRF : 11 Mbps for domestic use; not very well supported by the industry anymore.

  - Wi-Fi:11 Mbps known as IEEE 802.11b and supported by the WECA. Existing extensions a/g/i…

  - HiperLAN: two types (1 and 2) supporting 20Mbps and 54Mbps. Developed by the ETSI.

  - MMAC: Japanese organization for standardization of WLAN for the 5-GHz band.

This application note will deal with the Wi-FI standard, IEEE802.11B.

2   TI 802.11 WLAN Card

This section provides a high-level description of the device that supports this application, the 802.11 WLAN cards that can be used, and the interface used on these cards.

2.1   TI TNET1100B WLAN Chip

The following sections define the TNET1100B device that is used in the80211 WLAN cards.

2.1.1   *Features*

The features listed below are provided by the Texas Instruments TNET1100B 802.11b WLAN chipset. WLAN cards that are implemented using this device can be used to interface to the OMAP5910.

Features of the TNET1100B device include:

- Host Interface

  - Supports 33-MHz, 32-bit PCI 2.2, Mini PCI, and CardBus 7.0 specifications

  - Provides 16-bit generic slave-mode operation on host interface

  - Supports PCMCIA/CF+ Applications through 16-bit generic slave mode

  - Provides enhanced generic slave mode, enabling glueless interface with TI OMAP

- Processor EMIFS Port

  - Supports USB 1.1 slave applications for on-chip and off-chip transceiver modes

  - Hardware direct memory access (DMA) and bus mastering

- Medium-Access Controller (MAC)
    - 44-MHz embedded ARM 7TDMI central processing unit (CPU)
    - 64K-byte embedded random access memory (RAM)
    - Hardware-based MAC access protocol management
    - Hardware-generated positive acknowledgment (ACK), request to send (RTS), clear to send (CTS), probe response, and beacons
    - Hardware-based encryption/decryption using 64-bit, 128-bit, and 256-bit wired-equivalent privacy (WEP) keys
    - Hardware-based receive (RX) frame parsing
    - Dynamic allocation of transmit (TX) and RX memory blocks
- Baseband Processor
    - Data rates of 22 Mbit/s, 11 Mbit/s, 5.5 Mbit/s, 2 Mbit/s, and 1 Mbit/s
    - Supports IEEE Std 802.11b modulations
    - Supports short physical-layer convergence protocol (PLCP) preambles
    - Multipath delay spread tolerance > 500 ns RMS
- Radio Interface
    - Supports multiple radio topologies
    - On-chip, 8-bit, 22-MHz analog-to-digital converters (ADCs) for in-phase and quadrature (I/Q) RX inputs
    - On-chip, 10-bit, 44-MHz digital-to-analog converters (DACs) for I/Q TX outputs
    - Analog and digital RX automatic gain control (AGC) outputs
    - Analog TX power control
    - Implements antenna diversity
    - Programmable radio reference clock: 5.5 MHz, 11 MHz, or 22 MHz system level
    - Single-chip MAC and baseband processor
    - Two-wire serial electrically erasable programmable read-only memory (EEPROM) interface
    - 16 general-purpose I/O (GPIO) signals with interrupt capability
    - Processing gain up to 15 dB
    - Supports JTAG boundary scan
    - 1.8-V low-power core supply voltage
    - 3.3-V I/O supply voltage

2.1.2 TNET1100B Block Diagram

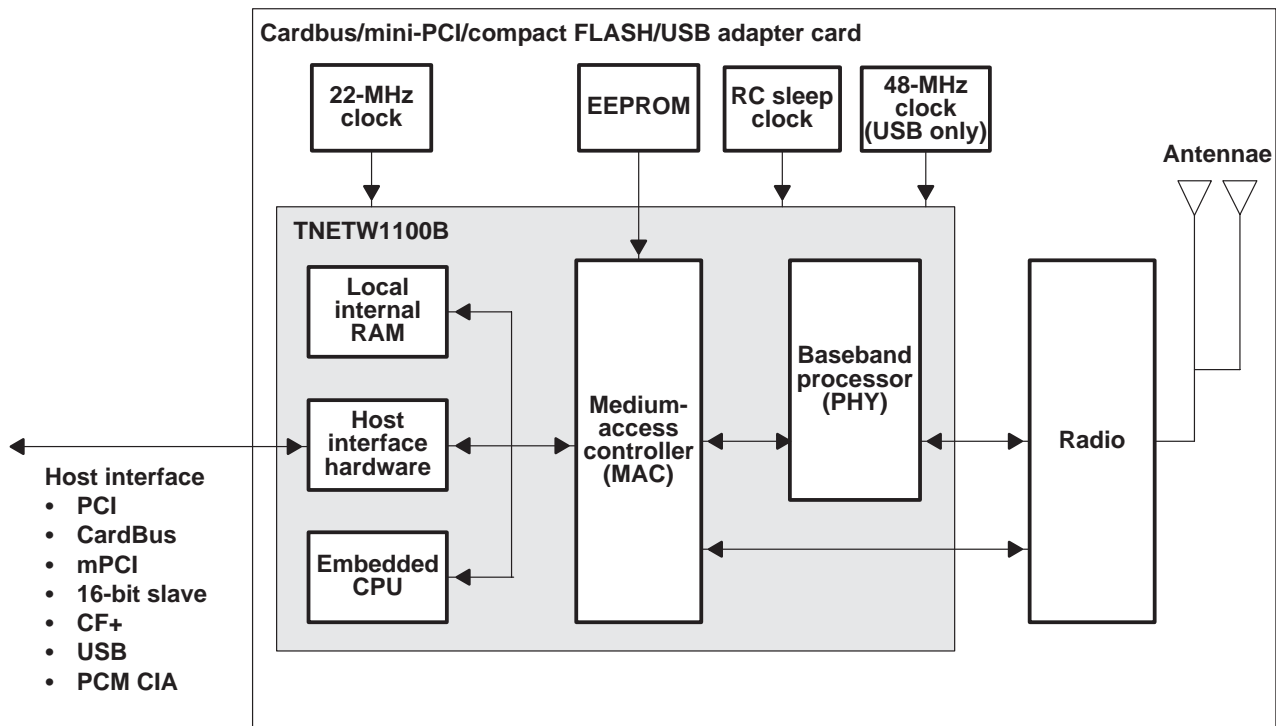Figure 1 is the block diagram of the TNETW1100B WLAN device.

Figure 1. TNET1100B Block Diagram

2.2 16-Bit Slave Interface

The TNET1100B features a 16-bit slave interface which will be used in this application. In generic slave mode, A15–A0 provide the lower 16 bits of the 24-bit input address bus on CAD31–CAD16. Signals D15–D0 provide a 16-bit bidirectional data bus on CAD15–CAD0. The remaining generic slave address lines (A23–A16) are distributed among other CardBus signals. For more detailed information on the slave mode and its operation, refer to the *TNETW1100B Medium-Access Controller (MAC) and Baseband Processor for Spread-Spectrum Wireless-LAN (WLAN)* datasheet (SPAS047).

2.3 PCCARD Connector

We will use the PCCARD form factor for the WLAN Card. Table 1 defines the pinout for the PCCARD connector.

Table 1. PCCard Connector Pinouts

Pin	Name	Pin	Name	Pin	Name
1	GND	24	CAD21	47	RSVRD
2	CAD0	25	CAD22	48	CBLOCK#
3	CAD1	26	CAD23	49	CSTOP#
4	CAD3	27	CAD24	50	CDEVSEL#
5	CAD5	28	CAD25	51	VCC
6	CAD7	29	CAD26	52	VPP2
7	CCBE0#	30	CAD27	53	CTRDY#
8	CAD9	31	CAD29	54	A23CFRAME#
9	CAD11	32	RSVRD	55	CAD17
10	CAD12	33	WP	56	PC_CARD_PD1
11	CAD14	34	GND	57	CVS2
12	CCBE1#	35	GND	58	CRST#
13	CPAR	36	CCD1#	59	CSERR#
14	CPERR#	37	D11	60	CREQ#
15	CGNT	38	CAD2	61	CCBE3#
16	CINT#	39	CAD4	62	CAUDIO
17	VCC	40	RSVRD	63	CSTSCHG
18	VPP1	41	CAD8	64	CAD28
19	CCCLK	42	CAD10	65	CAD30
20	CIRDY#	43	CVS1	66	CAD31
21	CCBE2#	44	CAD13	67	CCD2#
22	CAD18	45	CAD15	68	GND
23	CAD20	46	CAD16		

Table 2 defines the pins used on the PCCARD connector for control of the PCCARD interface on the WLAN card by the OMAP5910. The WLAN card is used in the slave interface mode.

Table 2. WLAN Card Interface Signals

Signal	Description
VCC	Main Power. Tied to 3.3V
VPP	Programming voltage. Tied to 3.3V.
PC_WAIT#	Wait signal. Holds off processor for long accesses.
CINT	Interrupt lead from the WLAN card
CRST#	Resets the WLAN card
CAD[0..15]	Data bus in slave mode.
CAD[16]	PC_CARD_PD1 Power down pin
CAD[17..31]	Address bus in slave mode.
CCBE0	CSBE_0
CCBE1	CSBE_1
CCBE2	OE (Read)
CCBE3	WE (Write)

2.4 WLAN Cards

Any WLAN card that is designed using the TNET1100B should work in this design.

3 OMAP5910 Interface

This section describes how to connect the WLAN card to the OMAP5910 processor. Appendix A has a full schematic of the design.

The sections that follow offer an explanation of what is being done.

3.1 Block Diagram

Figure 2 is the block diagram of the interconnection between the OMAP5910 and the 802.11 PCCARD.
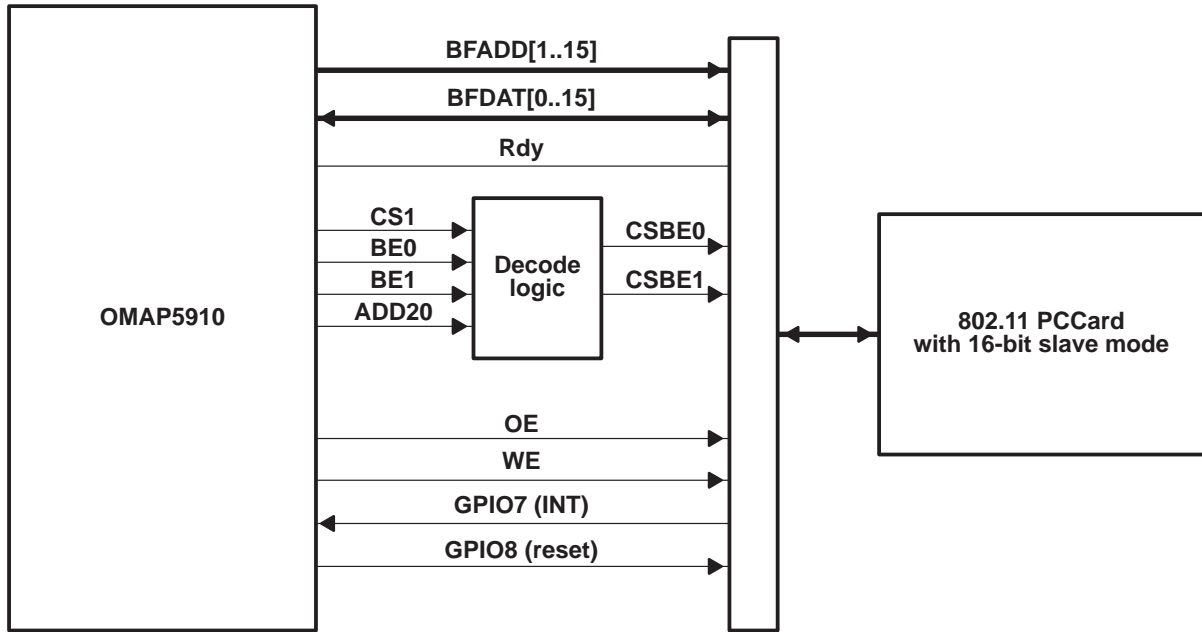
Figure 2. OMAP5910 and TNET1100B Block Diagram

Table 3 defines each of the signals used on the OMAP5910 and the functions they perform in the interface to the WLAN card.

Table 3. OMAP5910 WLAN Card Interface Signals

Name	Type	Description
BFADD(1:15)	O	16 address lines from the EMIFF bus to control the WLAN card.
BFDATA[0..15]	I/O	16 bi-directional data lines.
RDY	I	Rdy/Wait signal from the WLAN card to the OMAP5910.
CS1	O	Chip Select 1 from the OMAP5910 processor.
BE0	O	Byte enable 0.
BE1	O	Byte Enable 1.
ADD20	O	Address line 20 from the OMAP5910 processor.
OE	O	Output enable signal.
WE	O	Write enable signal.
GPIO7	I	Used as an interrupt line from the WLAN card to the OMAP5910.
GPIO8	O	Used as a reset line form the OMAP5910 to the WLAN card.

3.2 Address Decode Logic

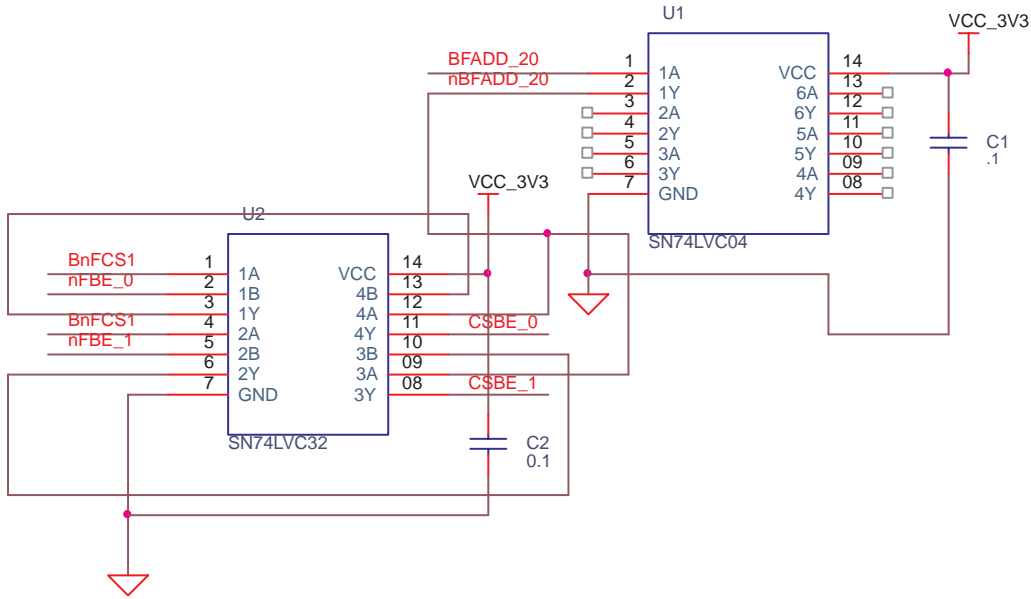Figure 3 shows the decode circuitry from the application schematic in Appendix A.

Figure 3. Address Decode

The OMAP5910 CS 1 is used for the WLAN card. Table 4 describes the signals used in the decode logic.

Table 4. OAMP5910 Interface Signals

Name	Description
BnFCS1	This is the main address chip select
nFBE0	This is the byte enable 0 signal.
nFBE1	This is the byte enable 1 signal.
nBFADD_20	This is address line 20.

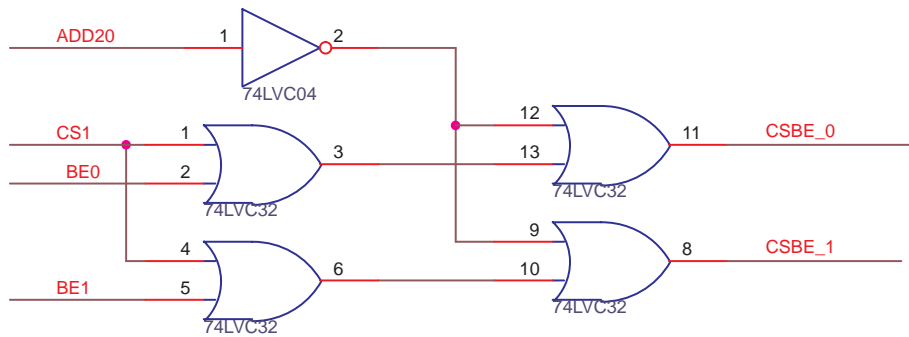A simpler view is provided in Figure 4 of the decode logic.

Figure 4. Address Decode

Chip selects other than CS1 may be used, depending on the overall system design. ADD20 may also be substituted for other address pins to lower the overall block size as needed.

3.3 Power

Power for the WLAN card and the support logic is provided by a 3.3V supply. The actual design of the power circuitry itself has been left up to the designer. Make sure that the total power of the WLAN card is understood to insure that sufficient power is provided.

3.4 Reset

The reset signal from the OMAP5910, connected to GPIO7, is used to insure that the WLAN card starts from a known state once the system is powered up. You will find a reset button on the schematic as well. While not required, this button is a convenient way to manually reset the WLAN card during the software development phase.

3.5 RDY/Wait Signal

The RDY signal provides a way that the WLAN card can extend the bus cycles of the OMAP5910 during long accesses. It should be noted, however, that the FRDY signal on the OMAP5910 has been known to exhibit some metastability issues. A resistor is provided in the design to allow for the removal of this connection if such issues occur. There is no known fix for this issue at this time. The timing of the chip select used can be adjusted to minimize the dependency on the RDY signal in the design.

4 Integrated Designs

While this application note has focused on using a PCCARD connector to add a PCCARD WLAN device onto the OMAP5910, other options are also available. These include:

- Taking the design of the WLAN card and embedding it into the design of the board
- Purchasing ready-made modules with the WLAN components already mounted

National Datacomm Corporation (NDC), http://www.ndclan.com/ , provides modules based on the TNET1100B design as well as integrated PCCARD devices.

5 Summary

The design in this application note has been tested under WinCE. A prototype board was designed that matches the included schematic for the Innovator platform. Depending on the operating system of the design, additional work will be required in the creation of a driver.

6 References

1. *OMAP5910 Dual-Core Processor Data Manual* (SPRS197)
2. *OMAP5910 Dual-Core Processor Functional and Peripheral Overview Reference Guide* (SPRU602)
3. *TNETW1100B Medium-Access Controller (MAC) and Baseband Processor for Spread Spectrum Wireless LAN (WLAN)* data sheet (SPAS047)

Appendix A   Schematic
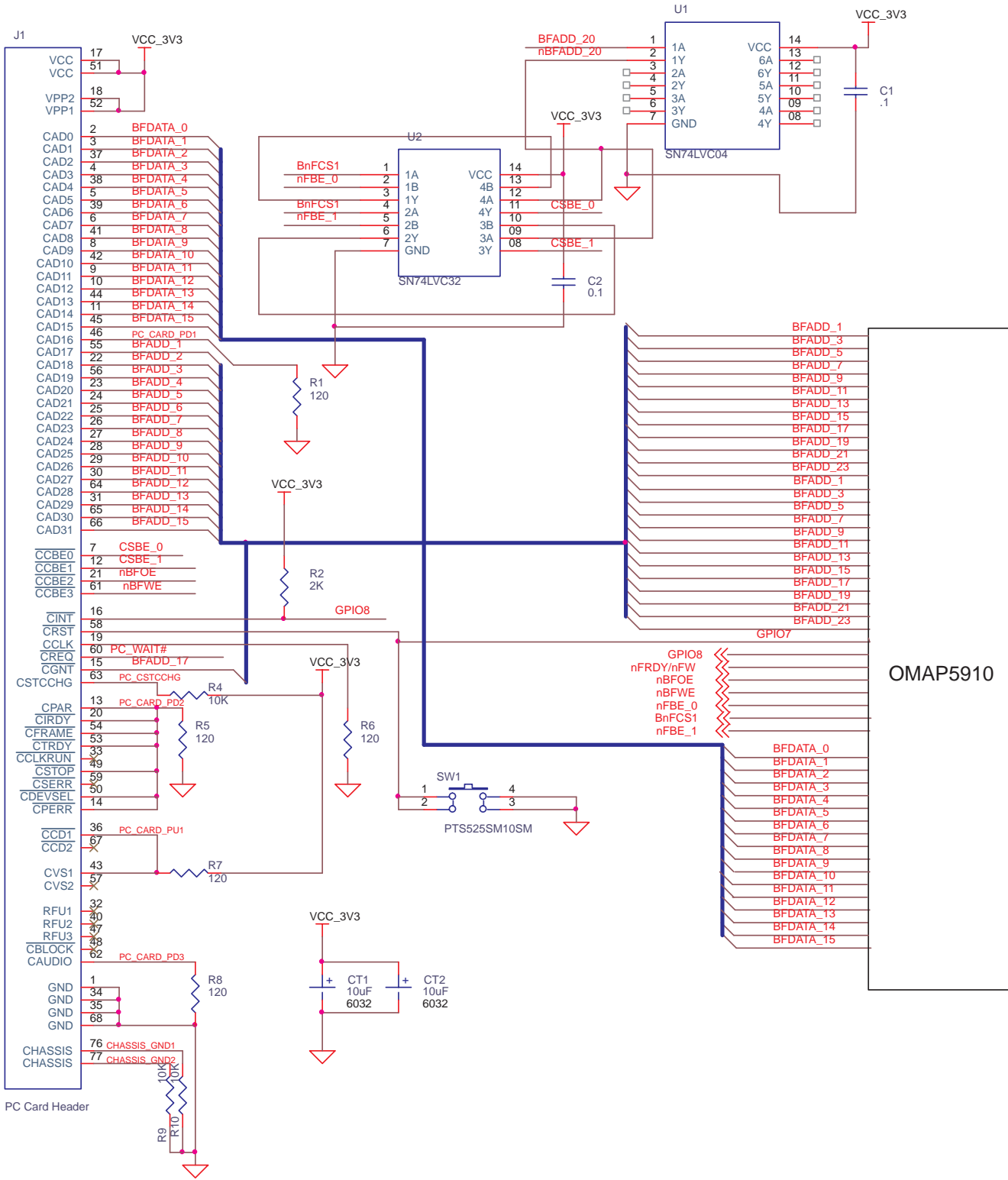
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