Application Note

Hardware-Based Synchronous Rectification Control with CLB

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ABSTRACT

This application note provides detailed guidance on leveraging the configurable logic block (CLB) module of the real-time C2000™ MCU. Leveraging this CLB module creates robust and simple synchronous rectification (SR) pulse width modulation (PWM) signals for the desired SR control of LLC resonant converters. The proposed method implements SR control without any software effort during runtime.

This application note provides insight with realistic examples showcasing how to interact with CLB and EPWM modules.

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1 Introduction

LLC resonant converters are becoming increasingly popular in industrial power applications. To achieve higher efficiency, the rectification diodes are replaced with MOSFETs to reduce conduction losses. A common practice is to use digital control for LLC converters for flexibility and scalability, especially in high-power applications. Application users must currently compare the switching and resonant frequencies in real-time, as discussed in *Intelligent LLC SR Control Using C2000™ and UCD7138*. For example, clamping the SR PWM on-time is required if the present switching frequency is below the resonant frequency. Otherwise, turning off the SR PWM following the primary-side PWM is required. Since the SR control requires fast response for reliability considerations, the software comparison can be placed in high frequency ISR, which takes up part of the CPU bandwidth.

Current-mode LLC is increasingly popular for solving the load-transient challenge using traditional voltage-mode control. However, defining the on time for SR PWM as preceding the comparator event using normal EPWM configuration is impossible because the comparator sets the turn-off timing of the primary-side PWM for current-mode LLCs using digital control. This document introduces a new way of implementing the SR control by leveraging the CLB module in the latest generation of C2000™ microcontrollers. This document also provides examples of implementing CLB in actual applications. These detailed configurations and example codes are based on the F28003x series, which applies to any C2000™ devices with the CLB module.

The desired SR driving signal under different switching frequencies (f_S) is given in Figure 1-1. To achieve adequate SR control, the below control targets normally achieve correct SR control:

- Hardware-based SR control without the software switch between the SR clamp mode (f_S < fo) and resonant mode (f_S > fo)
- Adjustable SR PWM turn-on delay
- Adjustable SR PWM clamping time
- Add the turn-off delay for SR PWM during resonant mode (optional)

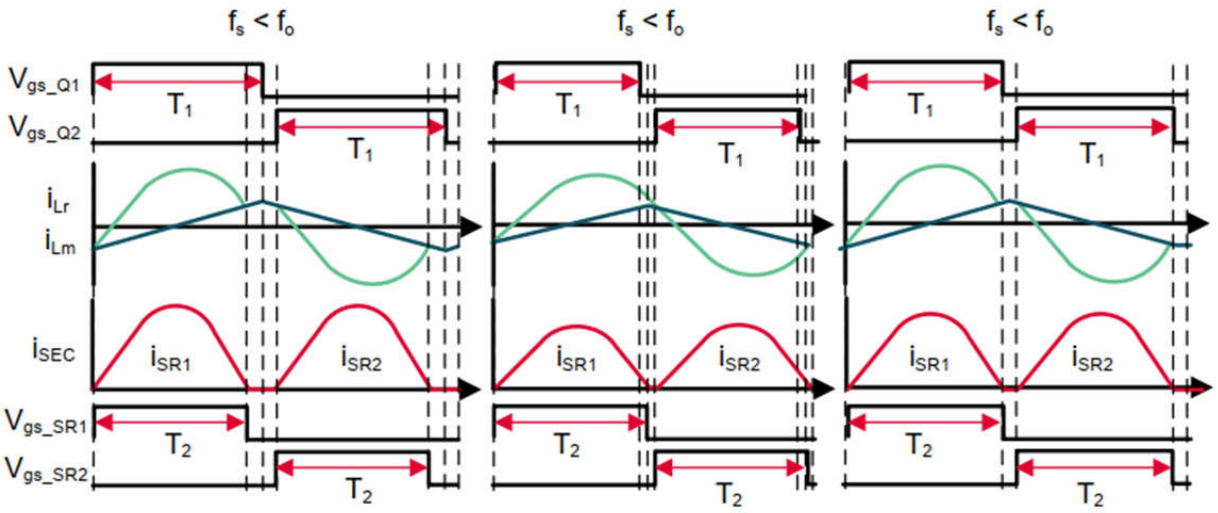

Figure 1-1. Desired SR Driving Signal Under Different f_S

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2 Basic CLB Implementation

The document, *Implement Three-Phase Interleaved LLC on C2000™ Type-4 PWM*, showcases using CLB for SR control. This application note discusses making the CLB logic more feasible for actual applications.

Figure 2-1 shows EPWM1 is selected as the primary-side PWM, EPWM2 is selected for SR PWM as the example, and the expected SR PWM configurations for resonant and SR clamp modes are included.

To achieve adjustable turn-on delay for SR PWM, the CLB module is not used to create the final SR PWM signals but the intermediate signal overriding the action qualifier (AQ) submodule output is used, meaning the addition of turn-on delay by the dead band (DB) submodule of the EPWM module is possible.

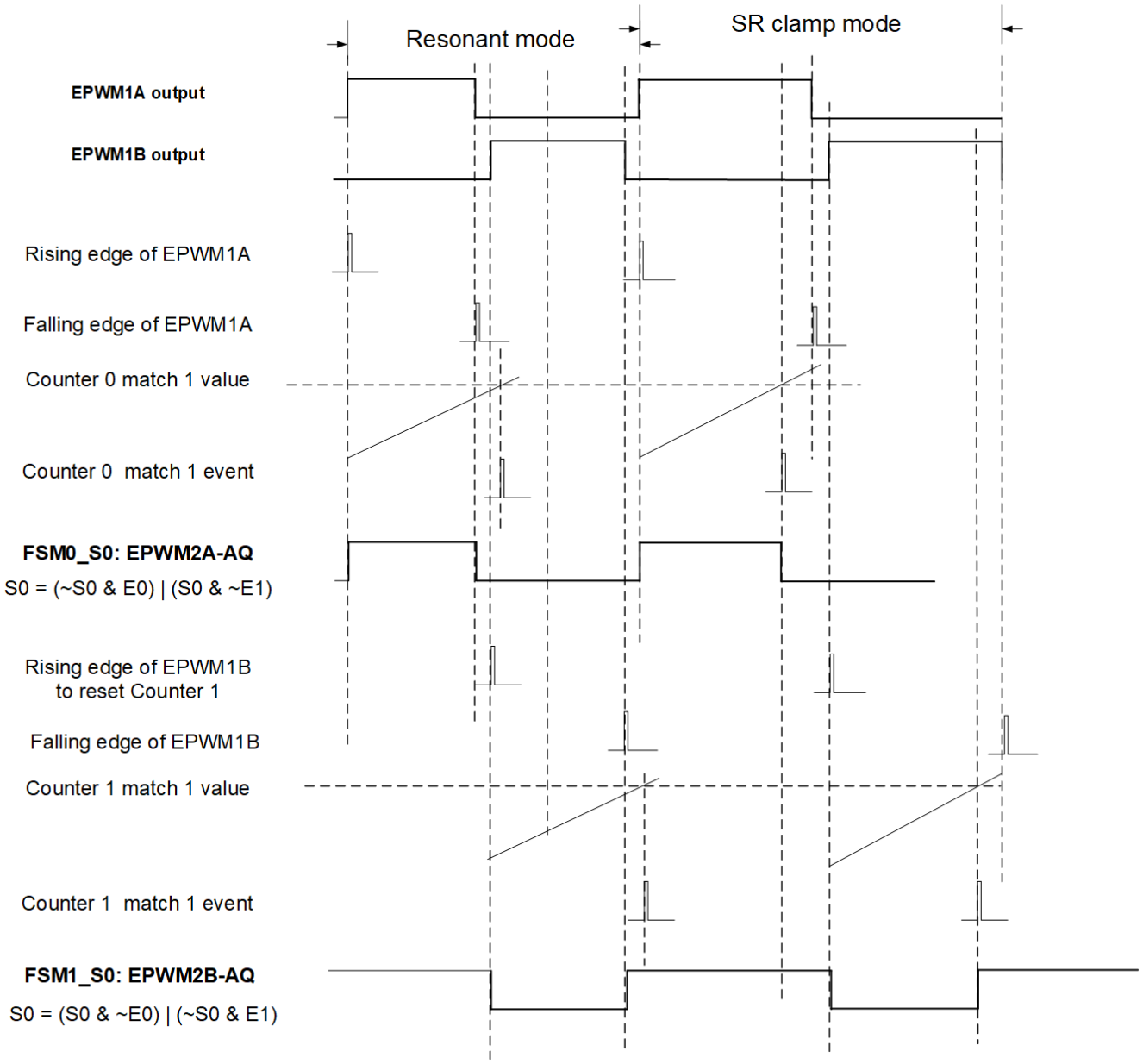

Figure 2-1. CLB Configurations and SR Control Logic

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The turn-on event is aligned with the rising edge of EPWM1A in example SR EPWM2A. The turn-off event follows the falling edge of EPWM1A during resonant mode or is limited by max on-time during SR clamp mode. Counter 0 is defined to start counting at the rising edge in the CLB and provide the match 1 event when the counter value reaches the predefined one (the predefined period corresponds to half of the resonant period). Users can utilize a look-up table (LUT) for ORing the falling edge and the match 1 event of Counter 0.

The finite state machine (FSM) is required for creating the expected logic for EPWM2A. In Figure 2-2, S0 is set to turn high at E0 and low at E1, with the rising edge of EPWM1A as an E0 event and LUT output as an E1 event. In Table 2-1, the Karnaugh map is created for S0 state.

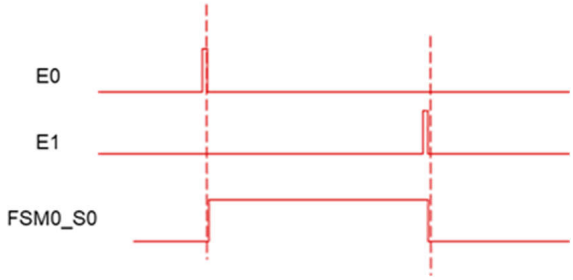

Figure 2-2. State Machine in the FSM Block

Table 2-1. FSM0 S0 Karnaugh Map

FSM0 S0				
S0 E0E1	00	01	11	10
0	0	0	1	1
1	1	0	0	1

Based on the Karnaugh map, Equation 1 for FSM0_S0 is deducible as:

$$S0 = (\sim S0 \,\&\, E0) \mid (S0 \,\&\, \sim E1) \tag{1}$$

In Table 2-2, using FSM0_S0 to override the module output of EPWM2A is possible by assigning FSM0_S0 to output 4 of the CLB2 module directly with the CLB multiplexer output enable register CLB_OUT_EN. In the Table 2-2 example, the CLB2 module is selected for EPWM2 for the reasons explained in this section.

Table 2-2. Peripheral Signal Multiplexer Table for CLB2

CLB2			
CLB2	CLB2_OUT0_0	PWMA	EPWM2
CLB2	CLB2_OUT1_0	PWMA_OE	EPWM2
CLB2	CLB2_OUT2_0	PWMB	EPWM2
CLB2	CLB2_OUT3_0	PWMB_OE	EPWM2
CLB2	CLB2_OUT4_0	**AQ_PWMA**	**EPWM2**
CLB2	CLB2_OUT5_0	AQ_PWMB	EPWM2
CLB2	CLB2_OUT6_0	AQ_PWMA	EPWM2
CLB2	CLB2_OUT7_0	AQ_PWMB	EPWM2

EPWM2B differs regarding FSM configurations because EPWM2B creates the AQ module output with the reverse polarity of EPWM1B (explained further in Section 3). Similarly, CLB2_OUT5 is activated to select FSM1_S0 as the AQ module output for EPWM2B.

Using the same method, the Equation 2 for FSM1_S0 is:

$$S0 = (S0 \,\&\, \sim E0) \mid (\sim S0 \,\&\, E1) \tag{2}$$

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Alternatively, the CLB configuration diagram in Figure 2-3 is configurable to where *IN0~IN4* refers to the falling edges of EPWM1A and EPWM1B and the rising edges of EPWM1B and EPWM1A. Additionally, IN5 turns the SR on and off (explained further in Section 5).

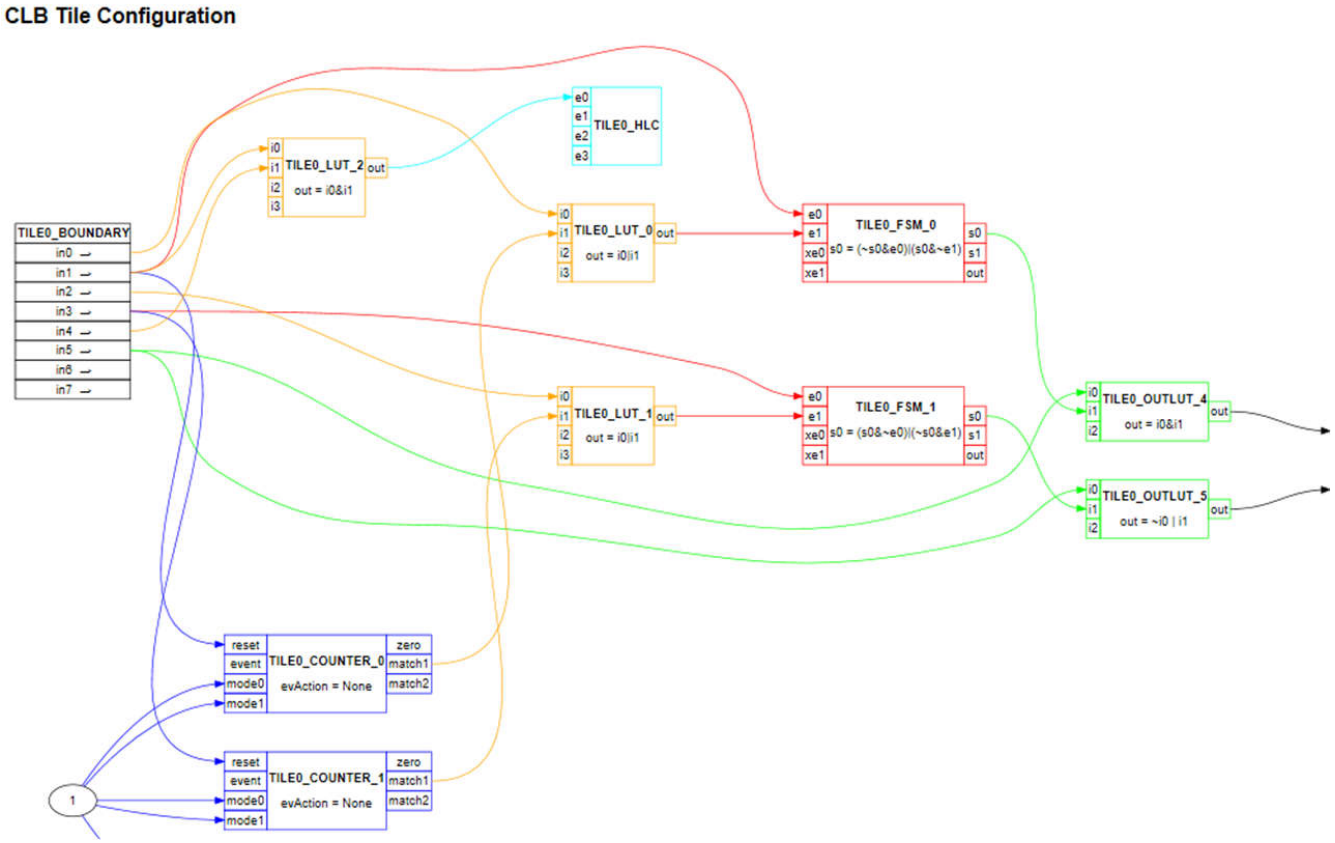

Figure 2-3. CLB Configuration Diagram

3 Turn-On Delay Configurations

For most applications, users add the turn-on delay for the SR PWM with respect to the primary side PWM, and the DB submodule can be used. However, only the rising edge delay can be directly enabled for the AQ signal (EPWM2A) with the DB submodule. Thus, to further leverage the falling edge delay block for EPWM2B AQ signal, create the reversed polarity signal for the original AQ output, and reverse the signal back after adding the falling edge delay with the DB submodule. The detailed configurations are shown in Figure 3-1 with the added red arrows. These configurations allow users to add a turn-on delay with the existing rising and falling edge delay of the DB submodule for SR PWMs, EPWM2A, and EPWM2B, respectively.

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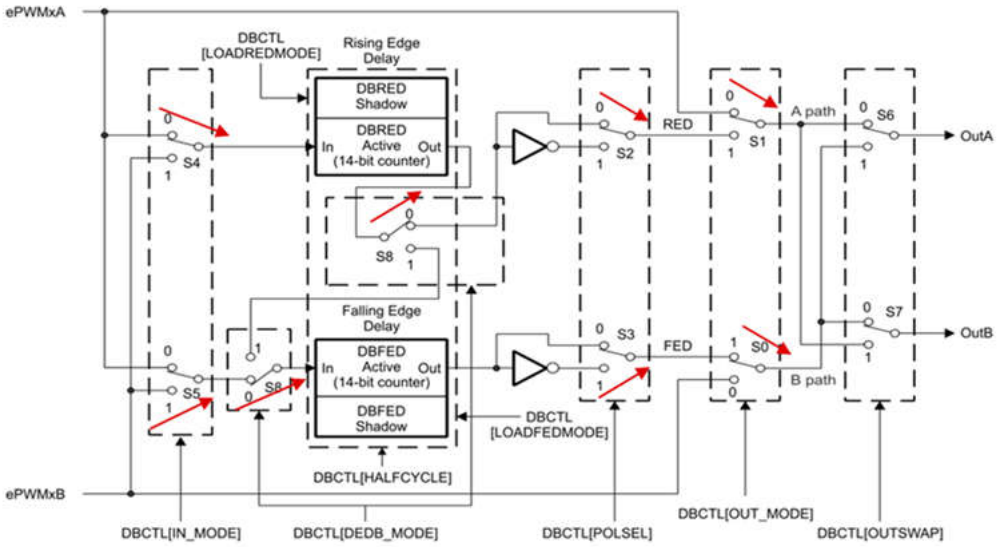

Figure 3-1. Dead Band Submodule Configurations

4 Turn-Off Delay Configurations

The switching frequency is larger than the resonant frequency during resonant mode, and the current on the SR MOSFETs still exist after the primary side PWM turns off, as shown in Figure 1-1. Extending the on time for the SR PWM by adding the turn-off delay (normally within 200 ns) helps improve system efficiency. To add the turn-off delay, this report provides two configurations.

The first configuration option is to leverage an extra Counter 2 from another CLB tile (like CLB3).

The first step in this configuration is to set the CLB input IN0 and IN1 to use the falling edges of EPWM1A and EPWM1B to reset the related counter to 0 (Figure 4-1) and set the match 1 values to represent the required turn-off delay for SR PWM. The next step is to select the match 1 event of the Counter 2 as the output, which replaces the original CLB2 IN0 (falling edge of EPWM1A) and IN2 (falling edge of EPWM1B), respectively.

Note

Although only eight output signals are provided in each CLB tile, the tiles are replicable to create up to 32 output signals, and signals *OUT16~OUT31* are the same as signals *OUT0~OUT15*. Therefore, CLB3 uses OUT0 and OUT1 in Figure 4-1, while CLB2 uses IN0 to select CLB3_OUT16 and IN2 to select CLB3_OUT17.

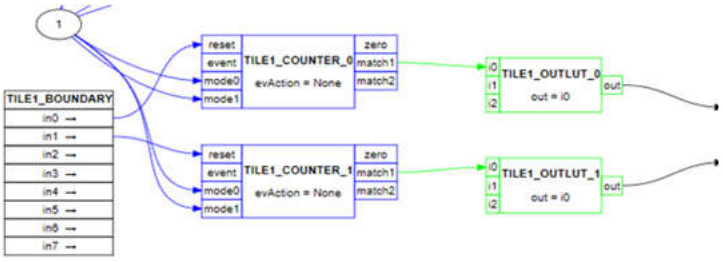

Figure 4-1. First CLB Configuration Option with Additional 2 Counters

For three-phase, interleaved LLC, there are not enough CLB tiles to provide the extra counters for the turn-off-delay design (Figure 4-1); however, using a second option that utilizes a single counter within the same CLB tile for the specific SR PWM is possible. In this second option (Figure 4-2), the falling edges of EPWM1A and EPWM1B (OR logic with LUT) are selected to reset the Counter 2 while the match 1 value is set with the expected delay timing. The important change for the CLB block diagram is replacing the IN0 inputs of LUT0 and LUT1 with the match 1 event of counter 2. With this option, the remaining FSM 2 works as the LUT function since all three LUT functions are occupied.

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Note

The second option works well if the required turn-off delay is less than the dead time of the primary-side PWM.

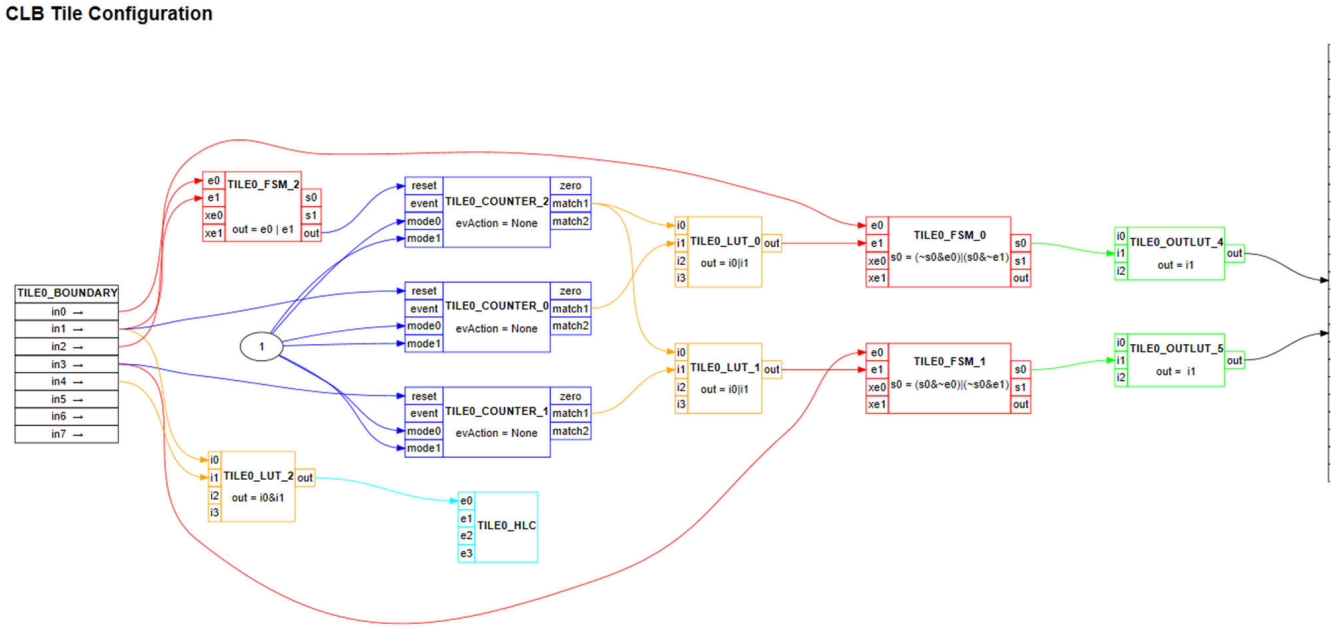

Figure 4-2. Second CLB Configuration Option with Single Counter

5 Different Options to Turn On or Turn Off SR PWM

The SR PWM is generated without extra software with the above CLB configurations. However, turning off the SR PWM to meet system requirements is sometimes required in the actual application. For example, turning off the SR PWM during the light load condition is a common practice for reducing switching loss, and some applications only turn on the SR PWM once the LLC completes the soft start process. Two methods for turning off the SR PWM are discussed in this section: software control and a purely hardware-based scheme with CLB.

5.1 Software Control Method

Turning off the SR PWM using the DB or Trip Zone (TZ) submodule is easy since the final SR PWM is created through both the CLB and DB submodule of EPWM. For example, the codes below leverage the large dead time to turn off the PWM outputs, with PERIOD_MAX representing the max period of the primary side PWM across all conditions. The benefit of this software control method is that DB edge-delay values provide the shadow mode, so the SR PWM output is completely activated or deactivated without any glitches when compared to the method using a software-forced trip event with TZ submodule. This method can be used together with load condition judgment in the software.

```
EPWM_setRisingEdgeDelayCount(EPWM2_BASE, PERIOD_MAX);
EPWM_setFallingEdgeDelayCount(EPWM2_BASE, PERIOD_MAX);
```

5.2 Hardware-Based Scheme

The following suggested hardware-based scheme achieves faster control response for SR PWM. The digital compare (DC) events created by the DC submodule of EPWM are included to help create a link between the CMPSS and the CLB module among multiple input signals for CLB. Figure 4-2 shows that the output current signal is fed into the CMPSS and that V_{light_load} refers to the load current threshold for turning SR PWM on or off. Figure 2-3 shows the DCAH event selected as the input signal IN5 for CLB2. The DCAH event changes to *logic 1* when the load increase is larger than the load threshold set by V_{light_load}, with the active-high logic from the CMPSS output. The SR PWM is turned on as long as the load changes from light load to heavy load. Figure 4-2 shows example codes for the CMPSS used for the SR on and off control.

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Note

Activate the digital filter so the transient around the threshold load condition is clear with adequate hysteresis.

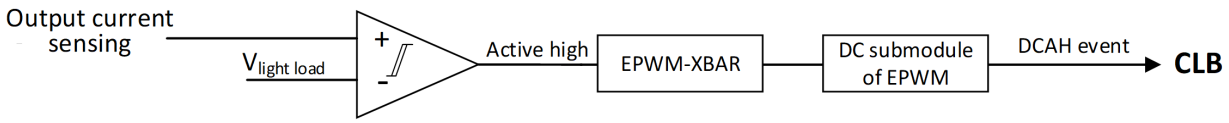

Figure 5-1. Hardware-Based SR Control with Load Current Sensing

```
XBAR_setEPWMMuxConfig(XBAR_TRIP10,XBAR_EPWM_MUX02_CMPSS2_CTRIPH);
 XBAR_enableEPWMMux(XBAR_TRIP10, XBAR_MUX02);
 // Enable CMPSS2 and configure the negative input signal to come from the DAC
 //
 CMPSS_enableModule(CMPSS2_BASE);
 CMPSS_configHighComparator(CMPSS2_BASE, CMPSS_INSRC_DAC);
 // Set DAC reference level, refers to 6A
 //
 CMPSS_setDACValueHigh(CMPSS2_BASE, 112);
CMPSS_configDAC(CMPSS2_BASE, CMPSS_DACREF_VDDA);
// Enable the digital filter
 CMPSS_configFilterHigh(CMPSS2_BASE,1,150,149);
 CMPSS_initFilterHigh(CMPSS2_BASE);
 CMPSS_configOutputsHigh(CMPSS2_BASE, CMPSS_TRIP_FILTER);
 CMPSS_setHysteresis(CMPSS2_BASE,4);
 EPWM_selectDigitalCompareTripInput(EPWM2_BASE,
EPWM_DC_TRIP_TRIPIN10,
EPWM_DC_TYPE_DCAH);
```

6 How to Adjust the SR PWM Clamping Time

Some applications adjust the max on time for the SR PWM during resonant mode to improve efficiency or compensate for component variations of the resonant tank, as discussed in *Implement Three-Phase Interleaved LLC on C2000™ Type-4 PWM*. Indicating the match 1 REF value of both Counter 0 and Counter 1 requires adjusting during run time. This adjustment is done with the high-level controller (HLC). The HLC provides communication and data exchange between the CPU and CLB. The CPU can write to a general purpose HLC register R0, to further move the R0 value to the match 1 REF value of counters.

The match 1 REF value does not inherently provide the shadow load mode option, unlike most EPWM registers. However, achieving a similar shadow mode with HLC is possible. Figure 2-3 showcases the zero event of Counter 0 as the Event 0 for HLC since HLC is an event-based system that aligns with the rising edge of EPWM1A. The update of the match 1 REF value for the counters and the EPWM1 module takes effect simultaneously.

Note

To avoid unpredictable behaviors by copying the R0 contents to another CLB register when R0 is being written, add another CLB input with GPREG bit (IN4 in Figure 2-3), and use the lookup tables to take the AND logic of GPREG bit and the zero event of Counter 0 as the HLC trigger event.

The following example codes can be used to update and adjust the SR PWM clamping time.

```
//before update R0 register, set in4=0
 CLB_setGPREG(CLB_SR_BASE, 0x00);
 //update the clamp duty cycle for EPWM2A and EPWM2B
 CLB_writeInterface(CLB_SR_BASE, CLB_ADDR_HLC_R0, clamp_duty);
 //set input4 to 1 allow copy of R0 to counter match1 register
 CLB_setGPREG(CLB_SR_BASE, 0x10);
```


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7 Summary

This application note detailed guidance on using CLB for achieving robust and simple SR control for LLC resonant converters. This document discussed turn-on and turn-off delay configuration features and flexible activation and deactivation options that can be applied to feasible and actual applications.

8 References

- IEEE Transactions on Power Electronics, *Digital Implementation of Adaptive Synchronous Rectifier (SR) Driving Scheme for High-frequency LLC Converters with Microcontroller*
- Texas Instruments, *Intelligent LLC SR Control Using C2000™ and UCD7138* application note
- Texas Instruments, *Implement Three-Phase Interleaved LLC on C2000™ Type-4 PWM* application note

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