Application Report
SWPA222A – November 2012

Power Delivery Network Analysis

Erwan Petillon *HW Systems Solutions*

ABSTRACT

The purpose of the Application Note (APN) is to present the flow, the environment settings and TI requirements used to perform the analysis of critical power nets of a platform using an application processor. In complement to the APN, a package including all necessary data to perform a PDN analysis of the OMAP4430 Blaze processor board are attached (layout, stack-up, schematic….)

The Power Delivery Network (PDN) performance is measured by extracting of the Printed Circuit Board (PCB) 3 parameters, DC resistivity, capacitor loop inductance and target impedance decoupling.

The application note explained each parameter theoretically and detailed the environment, set-up for the parameters extraction and comparisons to TI recommendations. To conclude each parameter sections, PDN extraction results of the OMAP4430 Blaze processor board with some general layout recommendations are presented.

Document History

Version	Date	Author	Notes
1.0	August 2012	E. Petillon	First release
A	November 2012	E. Petillon	Numerous typo corrections.

WARNING: EXPORT NOTICE

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from Disclosing party under this Agreement, or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws. This provision shall survive termination or expiration of this Agreement.
According to our best knowledge of the state and end-use of this product or technology, and in compliance with the export control regulations of dual-use goods in force in the origin and exporting countries, this technology is classified as follows:

US ECCN: 3E991
EU ECCN: EAR99

And may require export or re-export license for shipping it in compliance with the applicable regulations of certain countries.

Contents

Figures

Tables

1 Generals

PDN performances were not considered as major criteria in the early of the PCB designs. In today's platform with lower voltage, higher current, smaller voltage noise margin, PDN performances should be estimated early in the PCB design and optimized to meet the device specification.

The objective of a PDN is to supply a clean and stable voltage to the device. However the PDN is not ideal due to the parasitic added by the elements constituting the power network. Figure 1 presents a break-down model of a complete PDN network from Voltage Resource Manager (VRM) to the Application Processor (AP).

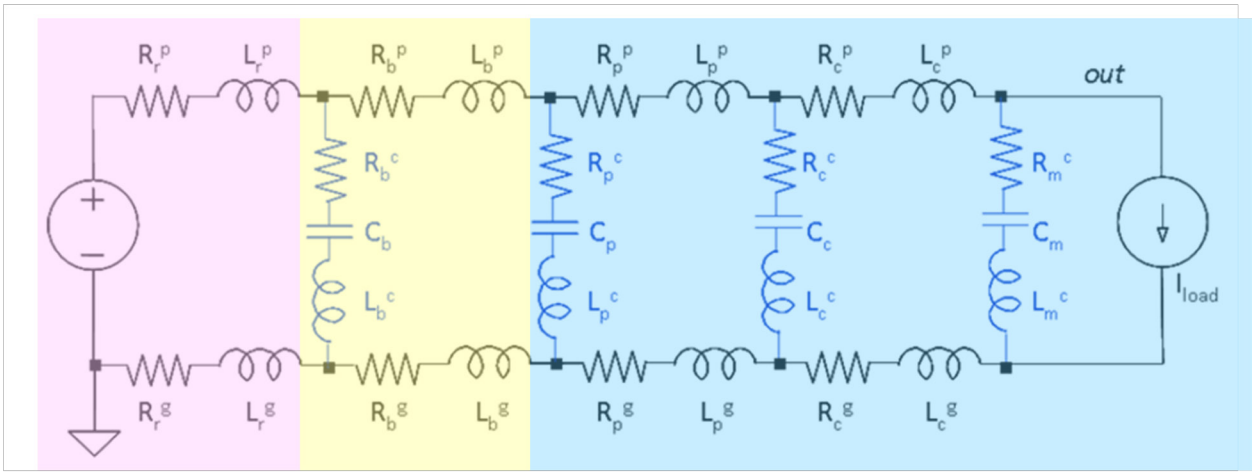

Figure 1: Power Delivery Network model

This APN focuses on the analysis of the PCB and the decoupling capacitors strategy used.

To extract the PDN performances of the PCB layout, you will need:

- Platform Schematic.
- PCB Layout out.
- PCB Stack-up with dielectric properties (Dk and Df), refer to Table 1.
- S-parameters capacitors models from manufacturer.
- Power Integrity (PI) tool.

PDN results for the OMAP4430 blaze processor board were extracted using nVolt from Nimbic.

	Thickness		Dielectric properties	
	In um	In mils	Dk	Df
L1	5	0.197		
prepreg	50	1.969	4.5	0.035
L2	35	1.378		

prepreg	50	1.969	4.5	0.035
L3	35	1.378		
prepreg	60	2.362	4.5	0.035
L4	35	1.378		
prepreg	140	5.512	4.5	0.035
L5	17	0.669		
prepreg	304	11.969	4.5	0.035
L6	17	0.669		
prepreg	140	5.512	4.5	0.035
L7	35	1.378		
prepreg	60	2.362	4.5	0.035
L8	35	1.378		
prepreg	50	1.969	4.5	0.035
L9	35	1.378		
prepreg	50	1.969	4.5	0.035
L10	5	0.197		
Total	1158	45.5905512		

Table 1: OMAP4430 Blaze processor board stack-up

2 DC resistance

DC resistance is determined by the geometry of the net, its material conductivity, refer to Figure 2.

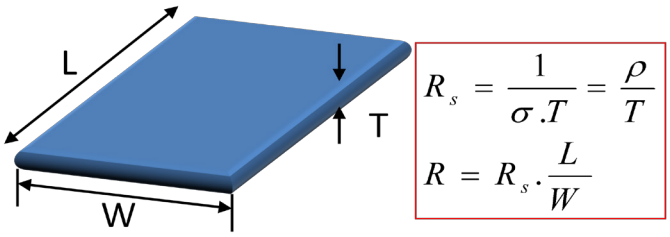

Figure 2: DC resistance

Once DC resistance is determined, IR drop can be calculated with Ohm's law.

$$DC\ IR\ drop = R_{dc} . I$$

An IR drop of 0.5%-2.5% of the nominal voltage is tolerated depending on the total system-level margin allowed for proper device functionality and sense line position.

TI specifies in the Data Manual (DM) a board DC resistance budget, from VRM to OMAP balls for critical power nets.

Due to the shape geometry complexity, vias and multilayer's used during the net routing, it is difficult to calculate manually the DC resistance. Numerous Signal Integrity (SI) or Layout EDA tools extract the DC resistance.

To extract DC resistance, you will need:

- Platform Schematic.
- PCB Layout out.
- PCB Stack-up.
- DC resistance extracting tool.

Figure 3 describe the flow used by most of the tool to extract DC resistance. In TI PDN analysis, the lumped methodology is preferred; each power and GND pins of VRM and AP are grouped.

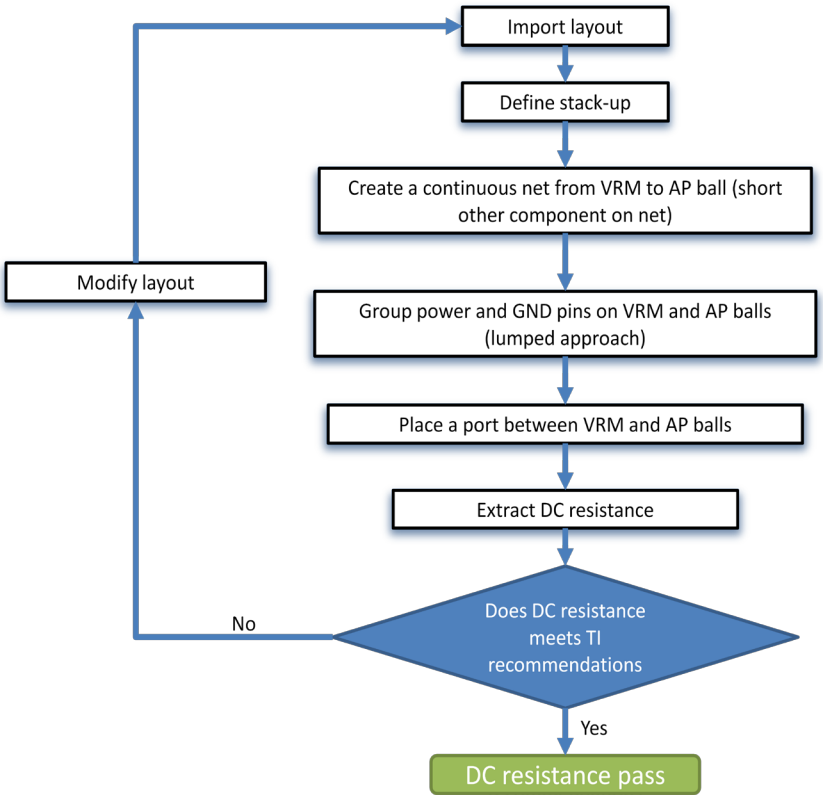

Figure 3: DC resistance extraction flow

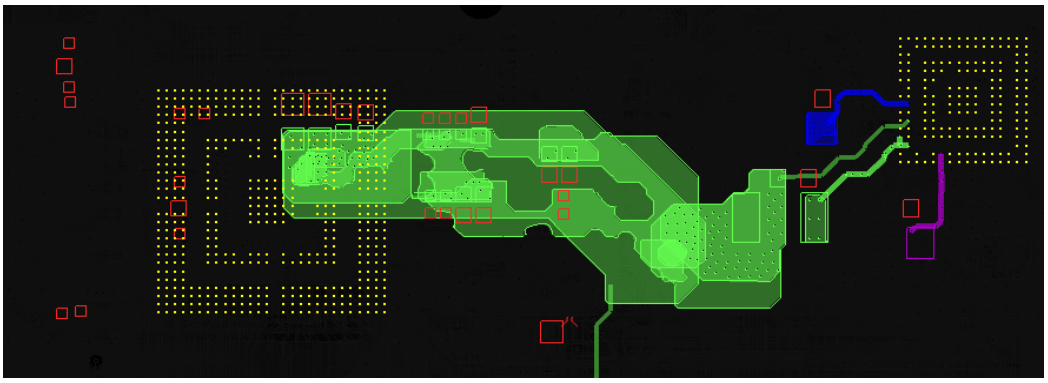

Figure 4: VCORE1_OMAP_MPU OMAP4430 Blaze OMAP4430 processor board.

Table 2 presents the DC resistivity analysis of VCORE1_OMAP_MPU, VCORE2_OMAP_IVAUD and VCORE2_OMAP_CORE nets.

Net Name	Volt (v)	Max Current (A)	TI recommendations (mOhm)	Extracted resistance (mOhm)	Max Irdrop (mV)
VCORE1_OMAP_MPU	1.38	1.45	14	8.45	12.25
VCORE2_OMAP_IVAUD	1.26	0.7	29	13.80	9.66
VCORE3_OMAP_CORE	1.1	0.85	13.75	18.34	15.58

Table 2: DC resistance OMAP4430 blaze processor board

In this configuration, DC resistivity is measured between VRM and OMAP balls. GND return path (GND plane) is not included as its effect is minor as it is shown in Table 3.

	Current (Amps)	Loop Resistance (Ohms)	OMAP balls Voltage(Volts)	V+ (Volts)	V- (Volts)
VCORE1_OMAP_MPU	1.45	0.00860495	1.36729	1.36775	0.000459935
VCORE2_OMAP_IVAUD	0.7	0.0139813	1.24986	1.25032	0.000459935
VCORE3_OMAP_CORE	0.85	0.0185016	1.08394	1.0844	0.000459935

Table 3: DC resistance OMAP4430 blaze processor board with GND return path included

Other tool offers the possibility to map current and voltage distribution over the power nets and GND return path, refer to Figure 5.

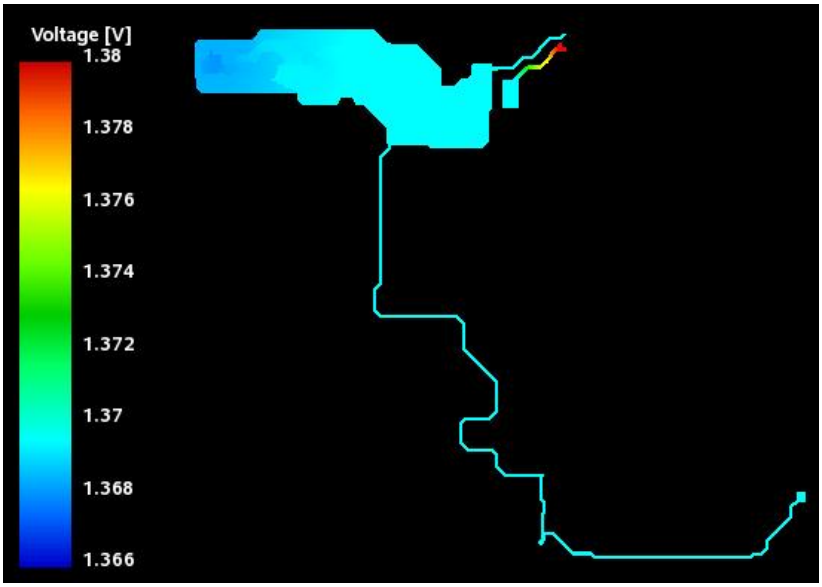

Figure 5: VCORE1_OMAP_MPU voltage mapping

Table 4 presents maximum DC resistivity of OMAP4430 for 1GHz and 1.2GHz operation.

PARAMETERS		PDN IMPEDANCE CHARACTERISTICS		PCB RESISTANCE BETWEEN SPMS and OMAP	MAXIMUM LOOP INDUCTANCE PER CAPACITOR (WITHOUT ESL) (nH)
		IMPEDANCE TARGET (mΩ)	FREQUENCY OF INTEREST (MHz)		
VCORE3_OMAP_CORE		122	48	13.75	1
VCORE1_OMAP_MPU	1GHz	93	40	14	0.7
	1.2GHz	71	28	10	0.7
VCORE2_OMAP_IVAUD		194	46	29	1

Table 4: DC resistivity OMAP4430 PDN requirements

General recommendations for minimizing DC resistivity:

- Shorten the length of the power nets trace by optimizing VRM and AP placement but also their balls positioning.
- Widen the power nets trace.
- Avoid discontinuity in power nets trace by inserting other signal nets or matrix of vias with their associated anti-pads (Swiss cheese effect) within the power nets.
- Avoid via starvation by determining maximum current carrying capacity and numbers of transitional via.

3 Capacitor Loop inductance

The loop inductance is a parameter quantifying the effectiveness of a decoupling capacitor. Figure 6 represents the different loop inductances added to the capacitor ESL.

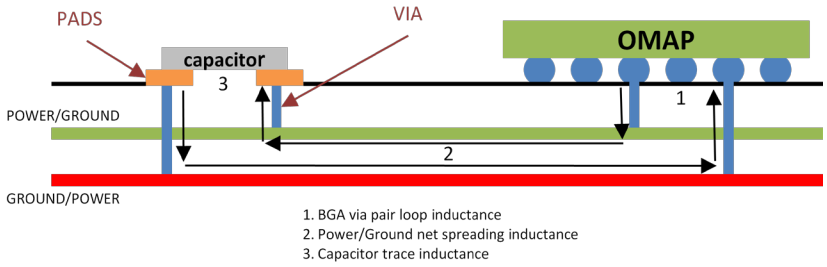

Figure 6: Loop inductance principle

Figure 7 shows a typical flow for capacitors Z-parameters extraction. Once Z-parameters is extracted, the loop inductance of a capacitor is determined by

$$L_{eff} = \frac{Imaginary\ Z_{power,gnd\ pads\ of\ caps}}{2\pi * Freq}$$

Where L_{eff} is the effective loop inductance,

$Z_{power\ ,\ gnd\ pads\ of\ caps}$ represents the Z-response of the port defined across the power and ground pads of the corresponding capacitors,

Typically, capacitors loop inductance is determined at a frequency of 50 MHz.

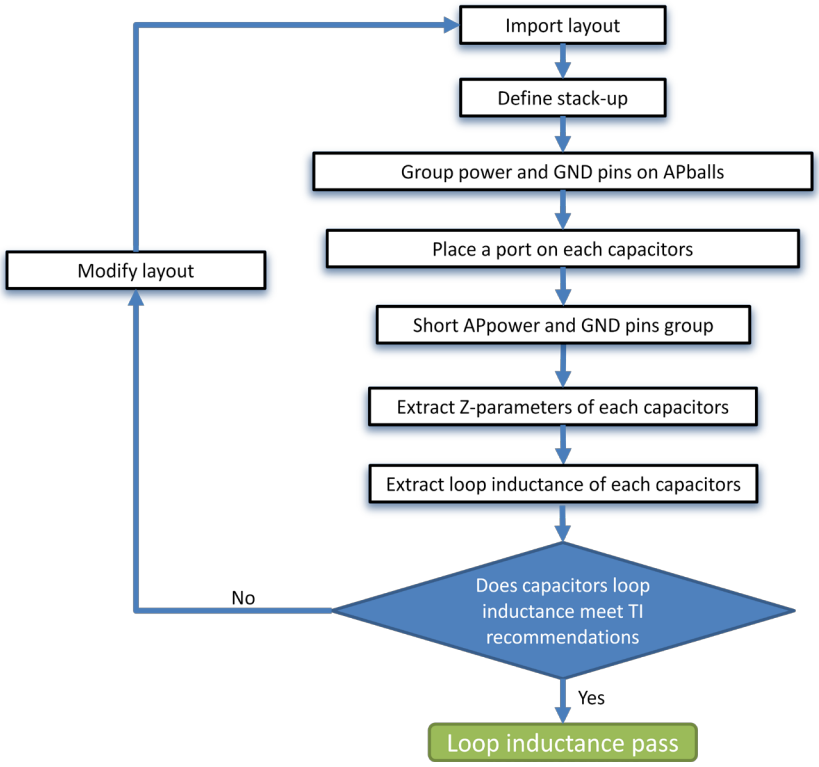

Figure 7: Capacitors loop inductance extraction flow

TI specifies in the Data Manual (DM) a maximum capacitor loop inductance, for example Table 5 refers to OMAP4430 PDN requirements. Following this requirement will help significantly to meet TI target impedance decoupling requirement, refer to section 4 for more details.

PARAMETERS		PDN IMPEDANCE CHARACTERISTICS		PCB RESISTANCE BETWEEN SPMS and OMAP	MAXIMUM LOOP INDUCTANCE PER CAPACITOR (WITHOUT ESL) (nH)
		IMPEDANCE TARGET (mΩ)	FREQUENCY OF INTEREST (MHz)		
VCORE3_OMAP_CORE		122	48	13.75	1
VCORE1_OMAP_MPU	1GHz	93	40	14	0.7
	1.2GHz	71	28	10	0.7
VCORE2_OMAP_IVAUD		194	46	29	1

Table 5: Loop Inductance OMAP4430 PDN requirements

To extract capacitors loop inductance, you will need:

- Platform Schematic.
- PCB Layout out.
- PCB Stack-up.
- Loop inductance extracting tool.

Figure 8 presents the loop inductance results of all decoupling capacitors on VCORE1_OMAP_MPU at 50 MHz. All capacitors loop inductances are below recommendations.

Capacitor instances VCORE1_OMAP_MPU	Loop inductance at 50MHz (in H)
C187	4.76E-10
C188	4.70E-10
C189	5.15E-10
C194	6.61E-10
C195	5.71E-10
C196	5.72E-10
C204	6.80E-10
C205	6.88E-10
C206	6.64E-10
C207	6.98E-10
C208	6.55E-10
C209	5.11E-10
C79	6.31E-10
C84	6.63E-10
Avg (excluding bulk caps)	6.04E-10
PMIC loop inductance	3.39E-09
TI Loop Inductance	7.00E-10

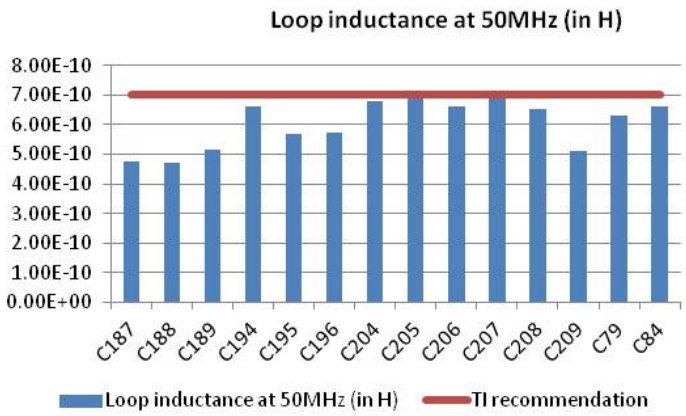

Figure 8: Capacitors Loop inductance on VCORE1_OMAP_MPU

It is also interesting to extract VRM loop inductance and compare it to DM specification.

General recommendations for minimizing capacitors loop inductance:

- Keep the power and ground plane pair as close to the TOP and BOTTOM surfaces.
- Placing power and ground plane pairs closer to the surface where the capacitor is mounted.
- Avoid discontinuity in power or GND planes to provide continuous return path for return current.

- Use via-in-pads for capacitors.
- Place vias as close to AP balls.
- Place decoupling capacitors closed to AP.
- Select capacitors with small footprint to minimize ESL.

4 Target impedance

To complete the PDN analysis, it is necessary to determine the target impedance of the overall power net. Target impedance extraction is achieved using the Frequency Domain Target Impedance Method (FDTIM).and the objective is to maintain the target spectrum below the Z target value (Z_{target}) from DC to F_{max}.

The Z_{target} value is determined by:

$$Z_{target} = \frac{Voltage\ Rail * \%\ Ripple}{0.5 * I_{max\ transient}}$$

F_{MAX} is the point in frequency after which adding a reasonable number of decoupling capacitors does not bring down the power rail impedance $|Z_{EFF}|$ below the target impedance (Z_{TARGET}) due to the dominance of the parasitic planar spreading inductance and package inductances.

Figure 9 presents a typical flow for a Target impedance extraction.

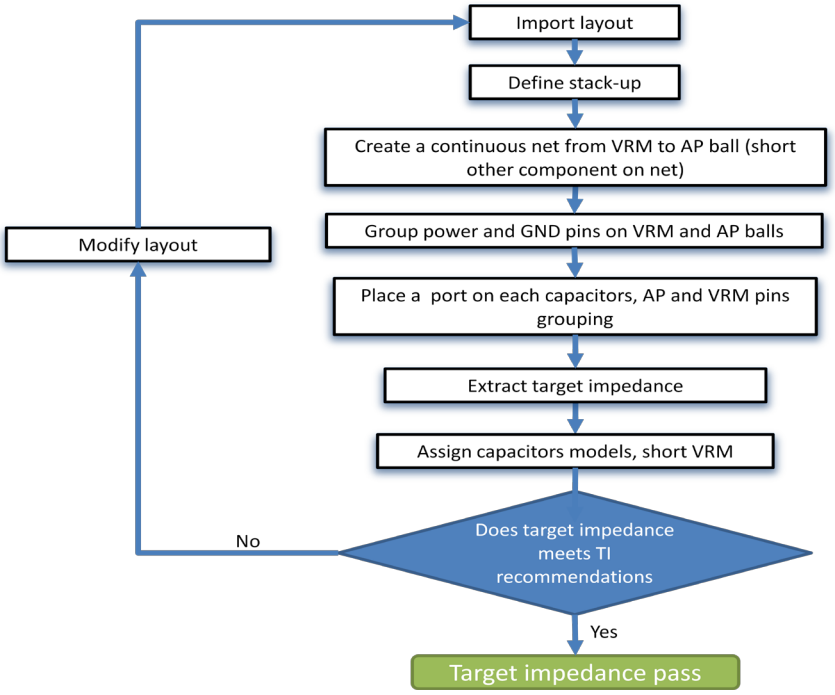

Figure 9: Target impedance extraction flow

TI specifies, in the DM, an impedance target (Z_{TARGET}) and a frequency range (F_{MAX}). Table 6 refers to OMAP4430 PDN requirements.

PARAMETERS		PDN IMPEDANCE CHARACTERISTICS		PCB RESISTANCE BETWEEN SPMS and OMAP	MAXIMUM LOOP INDUCTANCE PER CAPACITOR (WITHOUT ESL) (nH)
		IMPEDANCE TARGET (mΩ)	FREQUENCY OF INTEREST (MHz)		
VCORE3_OMAP_CORE		122	48	13.75	1
VCORE1_OMAP_MPU	1GHz	93	40	14	0.7
	1.2GHz	71	28	10	0.7
VCORE2_OMAP_IVAUD		194	46	29	1

Table 6: Target Impedance OMAP4430 PDN requirements

To determine target impedance response, you will need:

- Platform Schematic.
- PCB Layout out.
- PCB Stack-up.
- S-parameters capacitors models from manufacturer.
- Target impedance (S-parameters) extracting tool.

During the PDN analysis it is important to capture the decoupling frequency achieved for the required target impedance but also the target impedance achieved at the required decoupling frequency.

Table 7 resumes the target impedance results achieved on OMAP4430 Blaze processor board.

Figure 10 represents the complete target impedance response of the VCORE1_OMAP_MPU net on OMAP4430 blaze processor board.

Net Name	TI recommendations		OMAP4430 Blaze processor board results			
	Value (mΩ)	Frequency (MHz)	At TI recommended value (mΩ)	Reached frequency (MHz)	At TI recommended frequency (MHz)	Reached value (mΩ)
VCORE1_OMAP_MPU	93	40	93	49.2	40	75
VCORE2_OMAP_IVAUD	194	46	194	86	46	98
VCORE3_OMAP_CORE	122	48	122	48.4	48	122

Table 7: OMAP4430 Blaze processor board Z_{TARGET} results

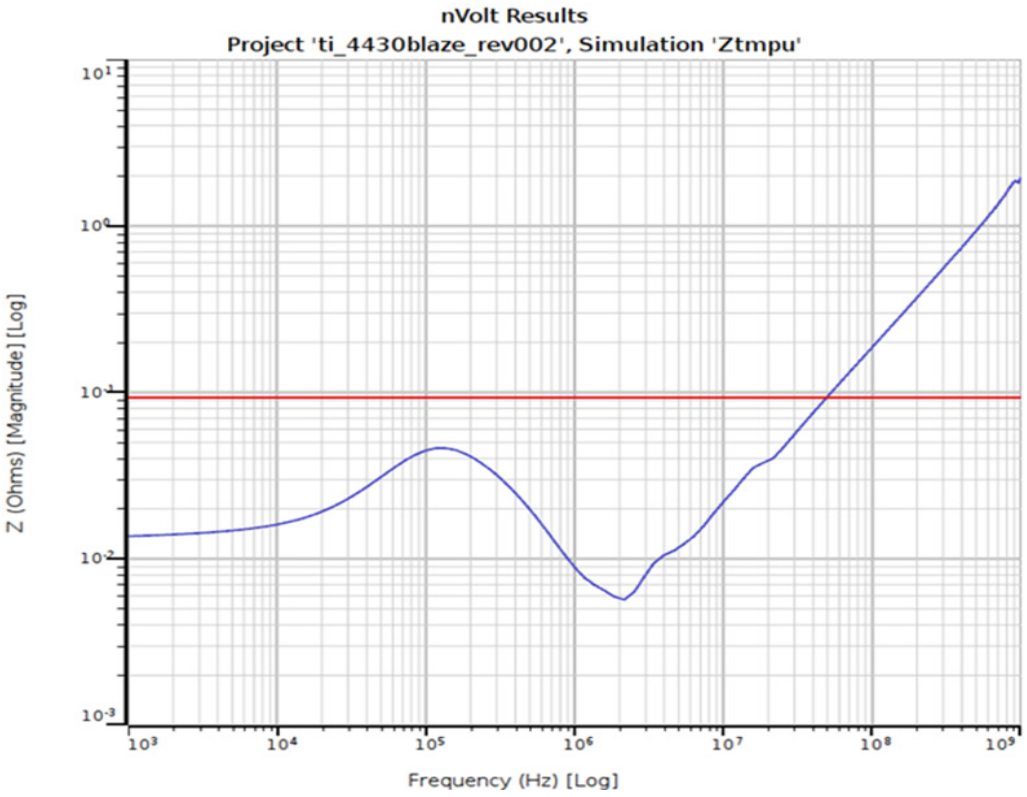

Figure 10: VCORE1_OMAP_MPU OMAP4430 Blaze processor board Z_{TARGET} response

Recommendations for improving target impedance response are similar to the recommendations to reduce the capacitors loop inductances. It is clear that reducing or removing capacitors with high loop inductance could help improving the Z_{TARGET} response.

If resonant peak appears before the required decoupling frequency then the decoupling strategy should be modified, add or replace a capacitor by the appropriate value to remove or decrease the resonant peak.

Figure 11 represents various target impendence responses with different decoupling strategy, only bulks capacitors, only 100nF capacitors, no capacitors.

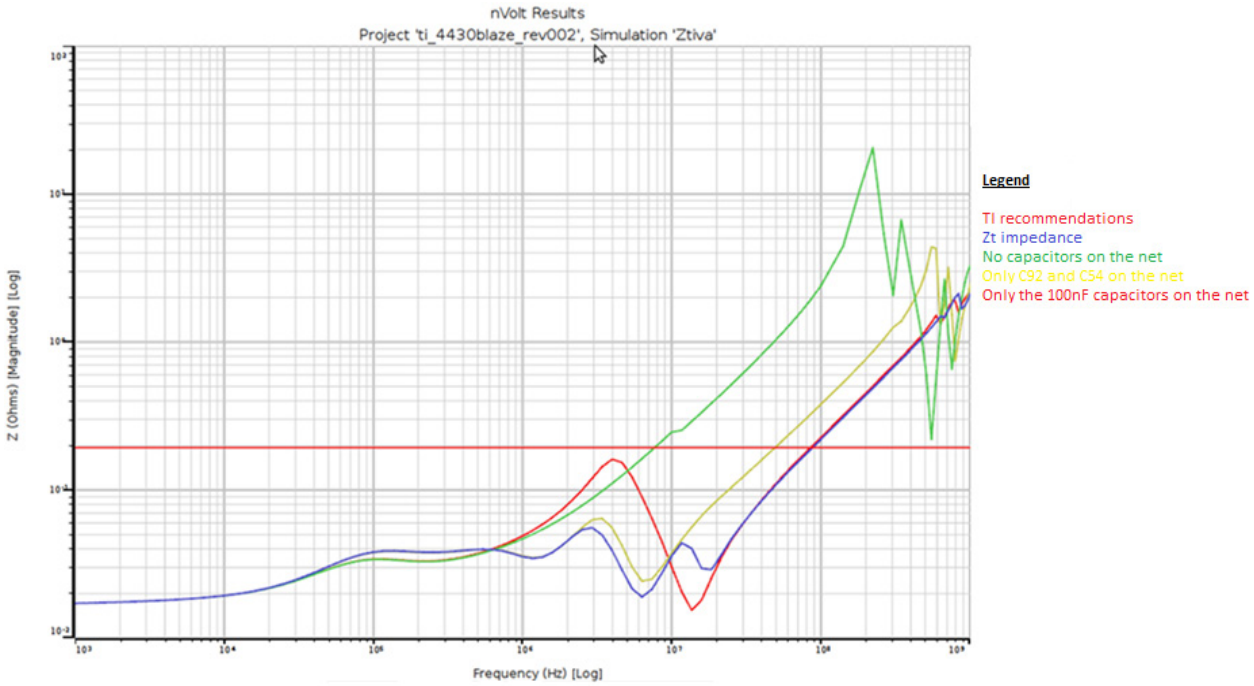

Figure 11: Different ZTARGET responses of VCORE2_OMAP_IVAUD net

5 OMAP4430 Blaze processor board PDN analysis.

A complete package to perform the PDN analysis of OMAP4430 Blaze processor board is attached to the application note. Use the Adobe paperclip icon to access the files below:

- OMAP4430 processor board Schematic (750-2165-001-SCH_REVB_PDN_only.pdf).
- PCB Layout out (720-2165-002_RevA_PDN_only.brd)
- PCB Stack-up with dielectric properties (Dk and Df) attached in the excel sheet.
- S-parameters capacitors models used for target impedance extraction.
- Excel sheet (TI-blaze4430_rev720-2165-002_results.xlsx) resuming the PDN results of VCORE1_OMAP_MPU, VCORE2_OMAP_IVAUD and VCORE3_OMAP_CORE extracted using nVolt tool.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265