Application Note

xWR6843 Power Optimization

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ABSTRACT

This application report is meant to assist designs with varying power constraints using the TI AWR6843 or IWR6843 mmWave Sensor. Varying degrees of power optimization are possible on the sensor depending on the application and use-case. Power optimization can be implemented in many different forms depending on what is appropriate for the use case. This document describes the implementation of different optimization techniques along with both their degree of power savings and their associated design tradeoffs.

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Trademarks

1 Introduction

TI mmWave Sensors enable high performance measurement and object detection over a variety of applications but some designs require minimal power consumption. This Application Note will showcase various power-saving techniques on the mmWave sensor where power consumption concerns are critical. Using this guide will enable one to implement various optimizations for evaluation. Moreover this guide discusses the tradeoffs involved as well.

The power saving techniques discussed in this guide can be implemented exclusively through software. Using the AWR6843 Evaluation Module (EVM), mmWave-SDK, and Code Composer Studio IDE one can replicate the results shown here with the use of standard laboratory equipment for power measurement.

2 Radar System Overview

2.1 Architecture Overview

The highly integrated nature of the AWR/IWR6843 Sensor allows for varying schemes of power optimization. For example an application that makes use of only 1Tx/1Rx will see less power consumed during active chirp time than a multi-Tx/Rx application where more angular resolution is required. As such one should be aware of the various performance compromises that result from optimizing for power. However the benefit of integration allows the optimizations to be implemented through software that can even be configured at runtime.

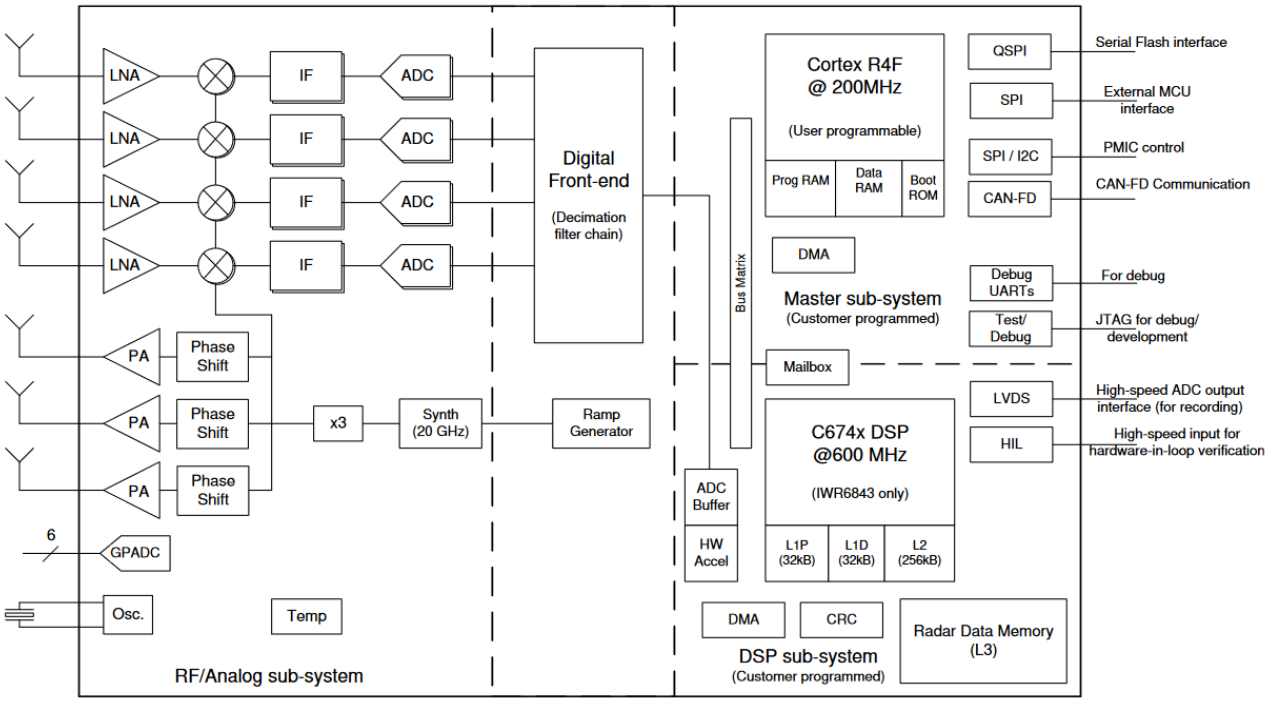


Figure 2-1. AWR6843 Block Diagram

2.2 Equipment for Evaluation

2.2.1 Hardware

All of the power saving techniques discussed in this document can be performed using the **AWR6843ISK EVM** and **MMWAVEICBOOST**boards (Note: the MMWAVEICBOOST board is not required for evaluation, but is required for debug and is highly recommended). Also the **mmWave-SDK 3.5** is leveraged using the **68xx Low Power Demo** available on the TI Resource Explorer.

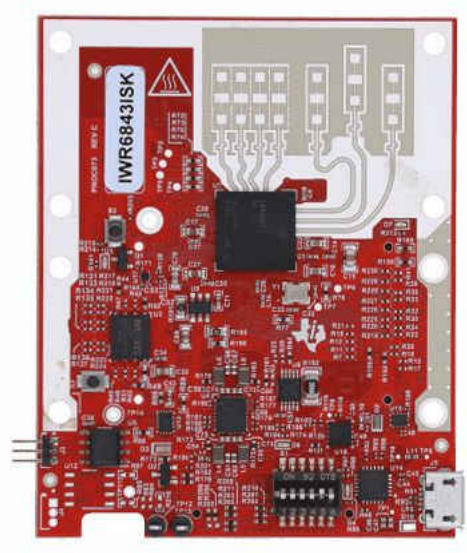


Figure 2-2. AWR6843ISK EVM

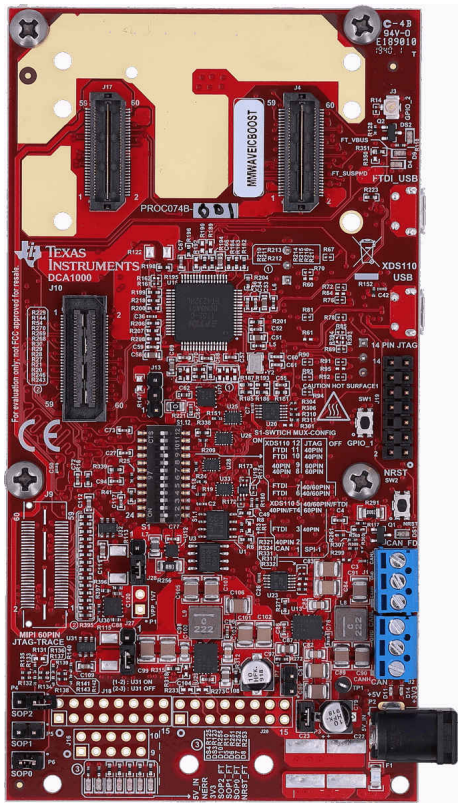


Figure 2-3. MMWAVEICBOOST Carrier Card Platform

2.2.2 Software

The **68xx Low Power Demo** is a modified version of the **mmWave-SDK 68xx Out-of-Box Demo – HWA Version** with the addition of software libraries and code level changes for power optimization. You should first run the **68xx Low Power Demo** using the steps from User Guide before proceeding with power measurement.

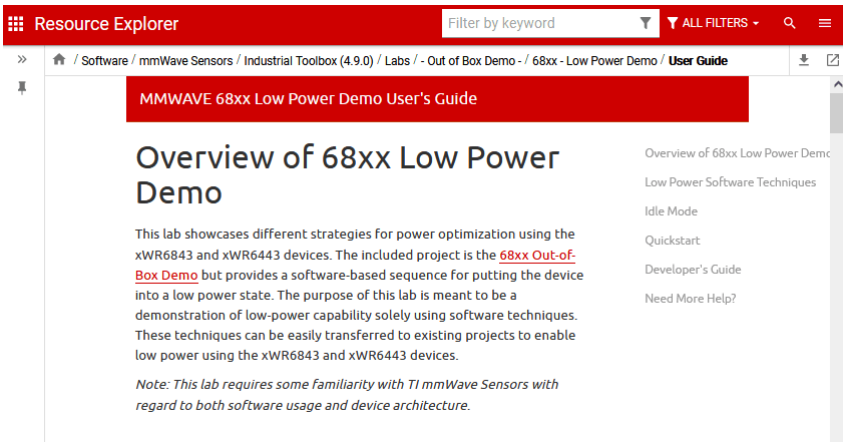


Figure 2-4. 68xx Low Power Demo User Guide on TI Resource Explorer

2.3 Radar Measurement Cycle

By default, the device boots once at power on, chirps based on end configuration provided by user, and leaves all subsystems running (even if they are not used). In many cases, this default behavior is fine. However, for power-sensitive applications, action can be taken to reduce the power consumption in both the Acquisition and Inter-frame Periods

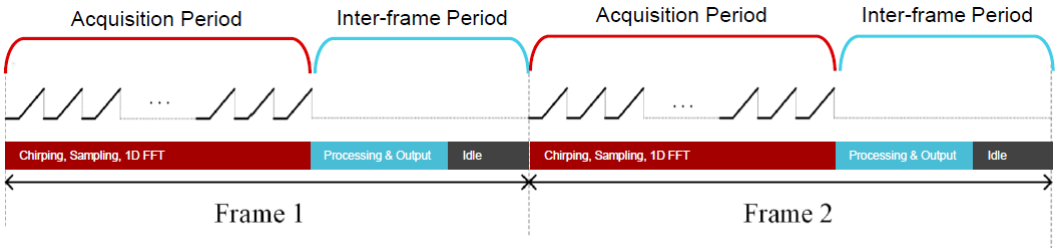


Figure 2-5. Radar Cycle – Acquisition and Interframe Periods

3 Active Mode Optimizations

3.1 Acquisition Period Overview

Active Mode optimization is achieved through minimizing the acquisition period (see Figure 3-1).

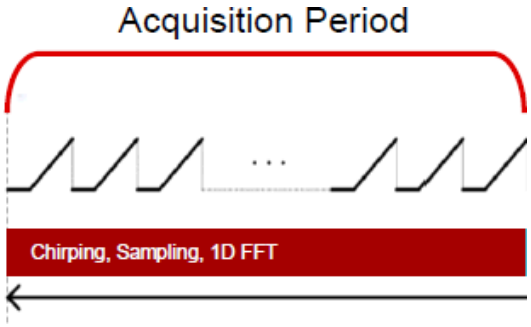


Figure 3-1. Acquisition Period

During the acquisition period the following occurs:

- Chirping
- ADC Sampling
- 1D FFT processing for range

3.2 Acquisition Period Optimization Parameters

Acquisition period can be simplified to Equation 1.

$$T_A = T_c \times N_c \times N_{Tx} \quad (1)$$

Where,

T_A : Represents the total **acquisition period**

T_c : Represents the duration of a **single chirp**

N_c : Represents the total **number of chirps** per Tx

N_{Tx} : Represents the number of Tx antenna

Reducing any of these parameters will result in a reduction of power consumption seen during the acquisition period, while reducing more than one parameter will have a multiplicative effect overall. Moreover reduction of power in active mode is the most effective way to reduce average power consumption.

3.3 Acquisition Period Optimization Tradeoffs

Reductions should be made with consideration for tradeoffs as described in Table 3-1.

Table 3-1. Acquisition Period Optimization Tradeoffs

Parameter	Parameter Type	Tradeoff
T_c	Single chirp duration	Reduces range resolution (assuming all other parameters held constant).
N_c	Number of chirps	Reduces velocity resolution
N_{Tx}	Number of Tx antennas	Reduces angular resolution

3.4 Acquisition Period Optimization Implementation

The following parameters can be configured at runtime via chirp profile, however, not all chirp configurations are supported at demo-level. For further guidance on chirp design one should consult the *Programming Chirp Parameters in TI Radar Devices* and the mmWave Sensing Estimator.

3.4.1 Single Chirp Duration

```
profileCfg 0 60 7 3 24 0 0 166 1 256 12500 0 0 158
```

Chirp Duration corresponds to the parameter **rampEndTime**, which is configured 5th in the **profileCfg** parameter set.

3.4.2 Number of Chirps

```
frameCfg 0 1 32 0 100 1 0
```

Number of Chirps corresponds to the parameter **number of loops** which is configured third in the **frameCfg** parameter set.

3.4.3 Number of Tx Antennas

```
channelCfg 15 5 0
```

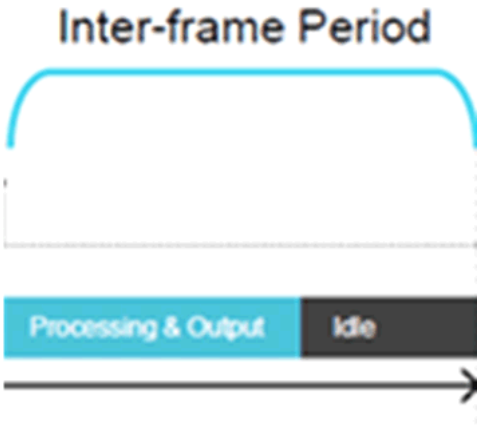
```
chirpCfg 0 0 0 0 0 0 0 1
chirpCfg 1 1 0 0 0 0 0 4
```

Number of Tx Antenna is first enabled by parameter **txChannelEn**, which is the 2nd parameter of **channelCfg**. The value is configured as a bitmask, thus the value **5** corresponds to enabling of **Tx 1** and **Tx3**.

Furthermore, the antennae are configured with the parameter **Tx Antenna Enable Mask**, which is the 8th parameter of the **chirpCfg** parameter set.

4 Idle Mode Optimizations

4.1 Inter-Frame Period Overview



During the above **Inter-frame Period** the following occurs:

- Continuation of FFT processing
- Other processing
- Data output to host or PC
- Idle state for remaining duration

The power saving techniques described here revolve entirely around the **Idle State** where different device components and peripherals are powered off to limit consumption. In this state, there are varying degrees of functionality for the sensor, which are discussed in Section 4.2.4.

4.2 Idle Mode Techniques

The components discussed below demonstrate low power capability by powering down various peripherals which leaves the device in a state resembling idle mode. At code level, idle mode is invoked by powering down a sequence of different device peripherals.

4.2.1 Power Domain Components

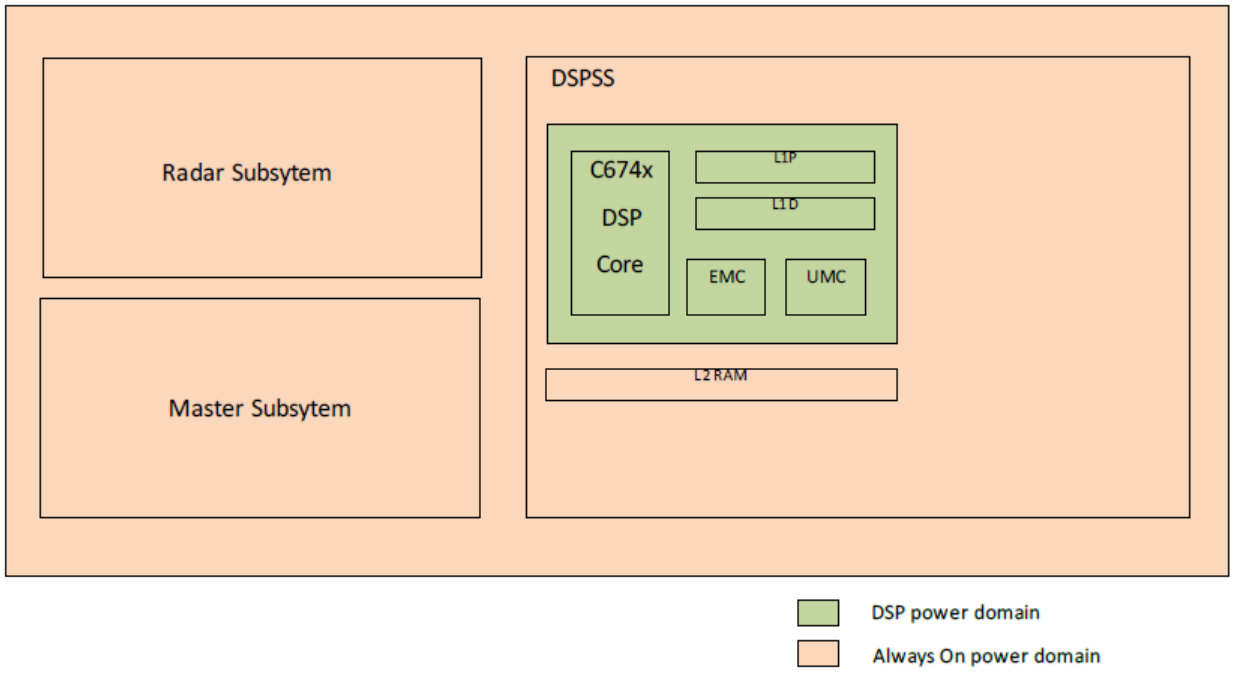


Figure 4-1. Power Domain Components

4.2.1.1 DSP Power Domain Shutdown

Condition: For systems not requiring DSP functionality (ie xWR6443)

Action: DSP can be shut down and clock gated achieving lowest power from this module. There is no function to revert back to functional DSP without a hard reset of the device. Both the LVDS and CBUFF functions (part of DSS) are also clock-gated as part of the DSS power-down function.

4.2.2 Digital Domain Components

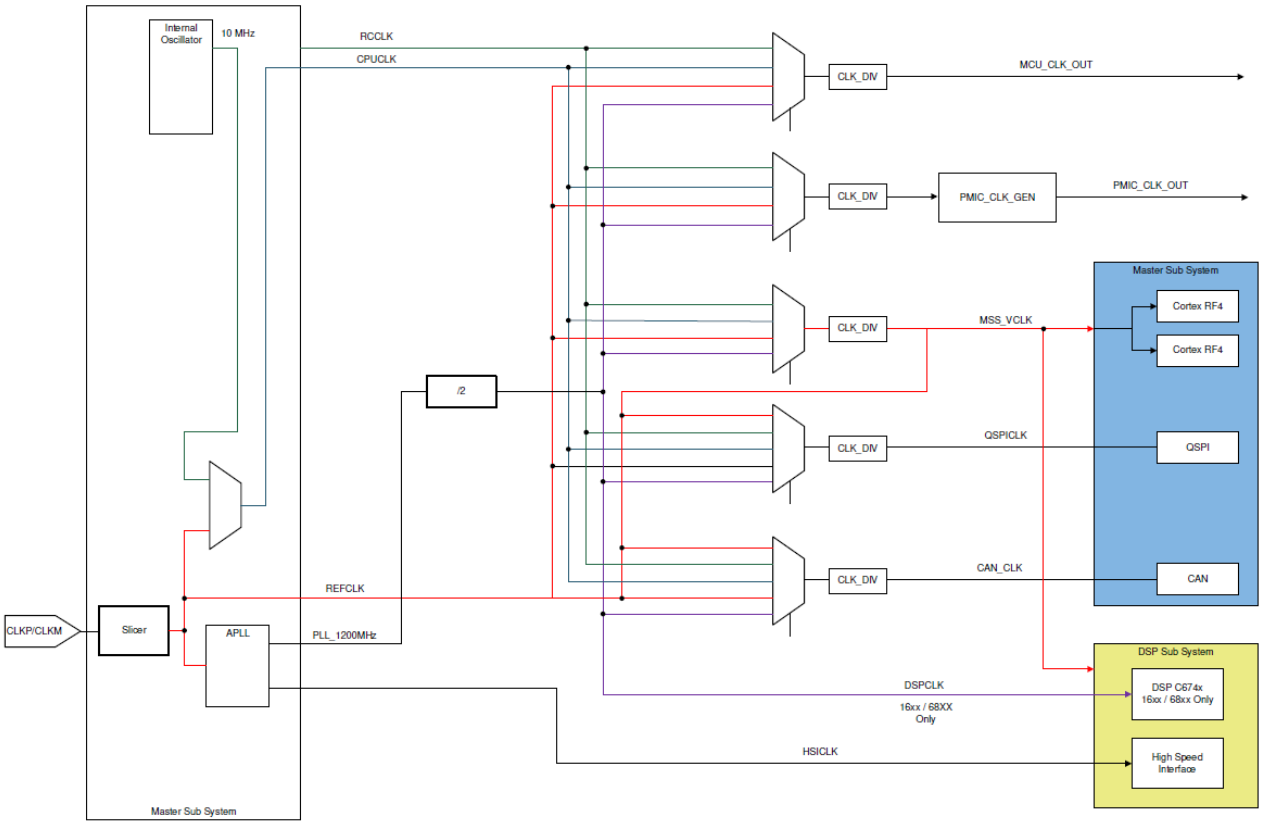


Figure 4-2. Digital Domain Components

4.2.2.1 DSS Clock Gating (DSP Subsystem)

Condition: For systems requiring some DSP functionality

Action: Perform DSS clock gating only while maintaining power to the DSP domain. This option is a “graceful” alternative that allows L1 memory to be retained but saves less power. NOTE:

Note

The LVDS and CBUFF clock gating that are integrated with option 1 **have not** been implemented in option 2. But, if implementation is desired, use the mmWave SDK Functions **SOC_gateClock/ SOC_ungateClock** with either **SOC_MODULE_CBUFF** or **SOC_MODULE_LVDS** as the input for ModuleId.

4.2.2.2 MSS VCLK to 40 MHz (Master Subsystem)

Condition: When in idle time either in-frame when active time and processing has completed, or in between frames.

Action: MCU VCLK can be reduced from 200 MHz to 40 MHz. Other peripherals dependent on the MCU clock and needing to be run in this time period will need to be checked for timing as well as any OS dependent timer.

4.2.2.3 BSS Clock Gating (Radar Subsystem - BIST)

Condition: When the active chirping is not required. However, BSS needs to be active (or unhalted) whenever there is a modification or peripheral read (GPADC) made to the analogue front-end.

Action: BSS can be halted (clkgated) with one SDK API command – and unhalted in the same way. BSS execution will be frozen and unfrozen accordingly maintaining context and execution location.

4.2.3 Analog Domain Components

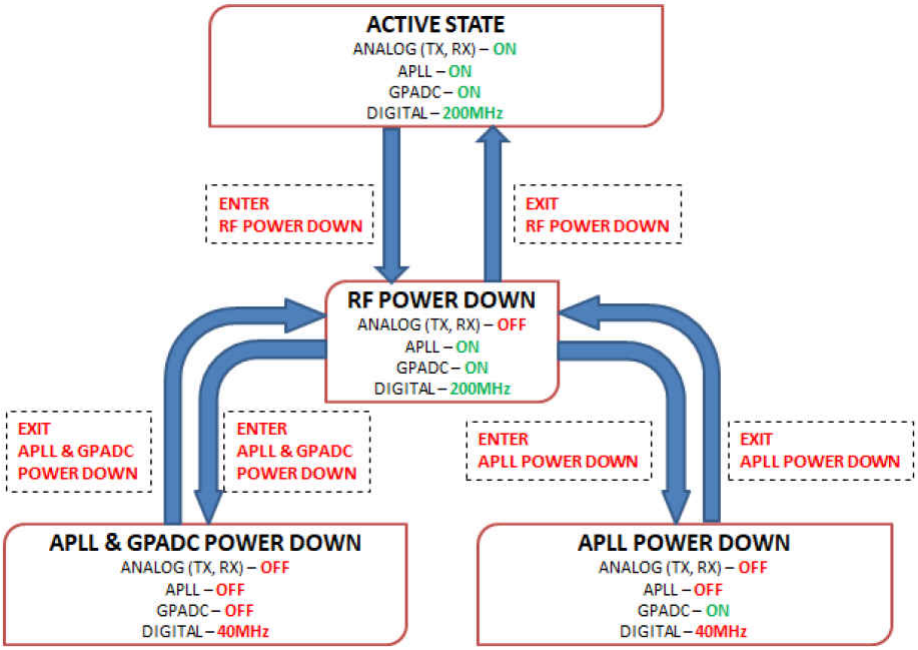


Figure 4-3. Analog Domain Components

4.2.3.1 RF Power Down (Radar Subsystem - Analog Front End)

Condition: When the active chirping is not required, and BSS is unhalted.

Action: The analogue componentry is initialised to pre-RFInit settings (and subsequently restored to post-RFInit).

4.2.3.2 APLL Power Down (Radar Subsystem - APLL)

Condition: When the active chirping is not required, BSS is unhalted, MSS is in ROSC mode @ 40Mhz.

Action: APLL is disabled / re-enabled accordingly. Need to ensure that all system clocks that are needed (ie PMIC_CLKOUT) are treated before PLL is turned off. The included DFP functions to perform this function include options to either enable or disable GPADC functionality.

4.2.4 Component Summary

The functional differences between analog and digital domain components can be mostly attributed to switching time. The digital clocking peripherals can be gated and ungated on the order of a few microseconds and can be implemented for use in a runtime scheme, whereas the analog peripherals require on the order of a few milliseconds in order to realize complete power switching. This makes the analog domain components most suitable for when device operation is not needed for a longer time.

The compromises in device functionality from using each of the power components are described below.

Component	Domain	Software Library	Functionality
DSP shutdown	Digital	Low Pow Lib	No DSP functionality due to shutdown of DSP Specific Power Domain. Full device reset is required for to enable DSP power domain.
DSS_CLK gate	Digital	Low Pow Lib	No DSP functionality for duration of clock gating. Functionality can be resumed by ungating DSP_CLK to 600 MHz.
MSS_VCLK gate	Digital	Low Pow Lib	No Cortex CR4F functionality. Functionality can be resumed by ungating MSS_VCLK to 200 MHz. Exception is for CAN_FD and QSPI peripherals which run on lower clock frequency.
BSS_CLK gate	Digital	SDK	No active chirping functionality of any kind. Functionality can be resumed by ungating BSS_CLK to 200 MHz.

Component	Domain	Software Library	Functionality
RF power down	Analog	DFP	No active chirping functionality of any kind. Functionality can be restored with DFP API.
APLL power down	Analog	DFP	No active chirping functionality of any kind. Functionality can be restored with DFP API.
APLL/GPADC power down	Analog	DFP	No active chirping functionality of any kind. Functionality can be restored with DFP API.

4.3 Idle Mode Implementation

4.3.1 Idle Power CLI Configuration in 68xx Low-Power Demo

The CLI commands **idlePowerDown** and **idlePowerCycle** are implemented to invoke any combination of the Idle Mode components as specified by the user.

- **idlePowerDown** – Will invoke each of the specified Idle Mode functions as specified by the user and leaves the device in an idle state indefinitely. A full device reset is required to return to a functional state.
- **idlePowerCycle** -- Will invoke each of the specified Idle Mode functions as specified by the user and then return to a functional state after a user specified delay.

Both of the commands use the following parameter structure **<subframeidx> <enDSPpowerdown> <enDSSclkgate> <enMSSvclkgate> <enBSSclkgate> <enRFpowerdown> <enAPLLpowerdown> <enAPLLGPADCpowerdown> <componentMicroDelay> <idleModeMicroDelay>,** where:

- <**subframeidx**>: always set to -1
- <**enDSPpowerdown**>: 1 enables **DSP Power Domain Off**, 0 disables
- <**enDSSclkgate**>: 1 enables **DSS Clock Gating**, 0 disables
- <**enMSSvclkgate**>: 1 enables **MSS Clock Gating**, 0 disables
- <**enBSSclkgate**>: 1 enables **BSS Clock Gating**, 0 disables (Note: Performed last at code level as discussed above)
- <**enRFpowerdown**>: 1 enables **RF Power Down**, 0 disables
- <**enAPLLpowerdown**>: 1 enables **APLL Power Down**, 0 disables
- <**enAPLLGPADCpowerdown**>: 1 enables **APLL/GPADC Power Down**, 0 disables
- <**componentMicroDelay**>: specifies a delay duration, in microseconds, between each successive power function
- <**idleModeMicroDelay**>: specifies a delay duration, in microseconds, after Idle Mode has been acheived but before device is powered up (if using **idlePowerCycle**)

4.3.2 Example Invoking Idle Mode

Idle Mode should be invoked at CLI using a PC UART Terminal (e.g. PuTTY or Tera Term). First a standard chirp config should be sent to start chirping from the sensor (e.g. profile_2d.cfg). Then to invoke Idle Mode one should send either of the idlePowerDown or idlePowerCycle commands. A few example schemes are discussed below.

4.3.2.1 Nominal Power Down Scheme

idlePowerCycle -1 1 0 1 1 1 0 0 0 1000000

This scheme first performs the below power down functions, waits 1 ms, and then performs power up in reverse order:

- DSP Power Down
- MSS VCLK to 40 MHz
- RF Power Down
- BSS Clock Gate

This scheme is deemed nominal because it leverages the most effective power down functions while keeping the device in a state that can quickly resume operational mode. An example use case where this scheme could be used is when the device should be kept in Idle Mode indefinitely but resume normal operation on receipt of a CAN signal.

NOTE: This scheme powers down the entire DSP Power Domain. For a use-case where DSP would be needed when operating, one should leverage the **DSS Clock Gating** function instead.

4.3.2.2 Full Power Down Scheme

idlePowerCycle -1 1 0 1 0 1 0 1 0 1000000

This scheme first performs the below power down functions, waits 1 ms, and then performs power up in reverse order:

- DSP Power Down
- MSS VCLK to 40 MHz
- RF Power Down
- APLL Power Down

This scheme is designed to showcase the lowest consumption possible while still retaining power to the device. An example use case where this scheme could be used is when the device should be kept in Idle Mode indefinitely but resume normal operation on receipt of a CAN signal.

NOTE: This scheme powers down the entire DSP Power Domain. For a use-case where DSP would be needed when operating, one should leverage the **DSS Clock Gating** function instead.

4.3.2.3 Fast Power Down Scheme (Clock Gates Only)

idlePowerCycle -1 0 1 1 1 0 0 0 0 1

This scheme first performs the below power down functions, waits 1 µs, and then performs power up in reverse order:

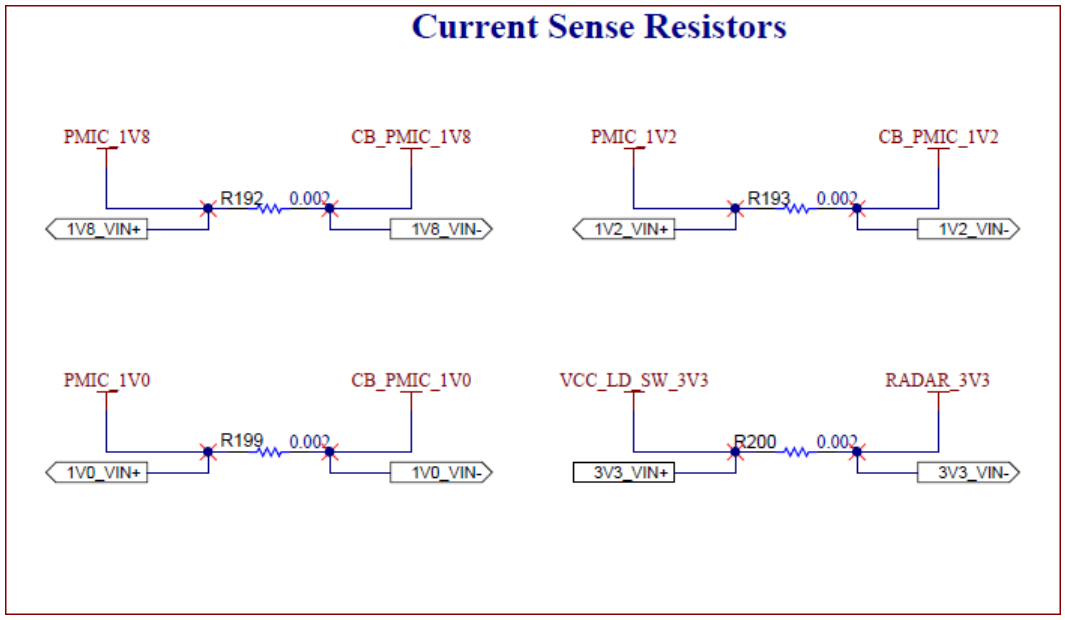
- DSS Clock Gate
- MSS VCLK to 40 MHz
- BSS Clock Gate

This scheme is designed to showcase an Idle State where very fast switching is needed. Because of this none of the Analog Domain components are leveraged. An example use case where this scheme could be used is between frames in operational mode where a fast framing time is used.

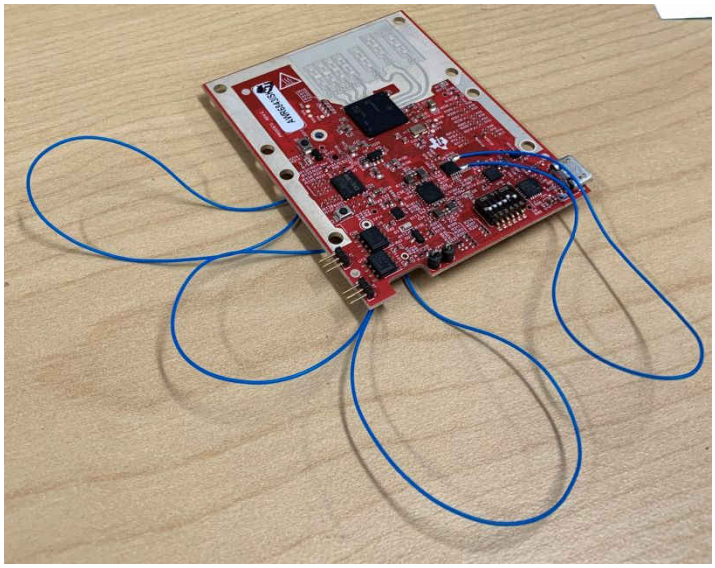
5 Power Measurement Methods and Results

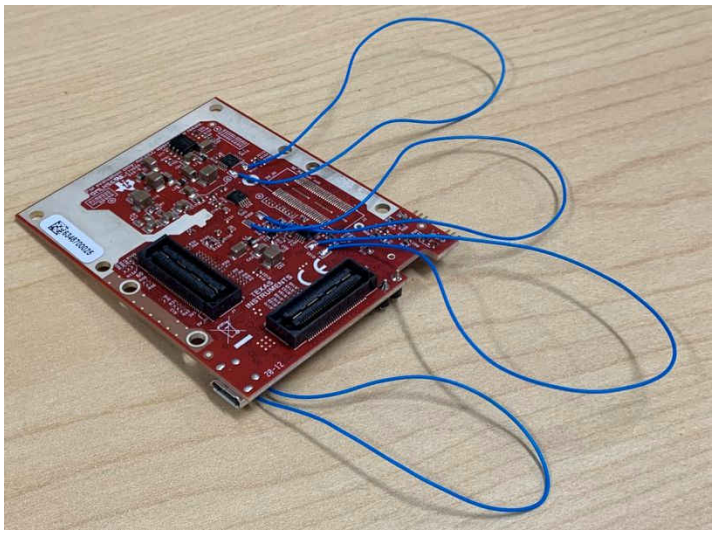
5.1 Power Measurement Method

AWR6843 EVM Board features current sense resistors for following PMIC rails 1.2 V, 1.8 V, 1.0 V, 3.3 V. Resistors were replaced with wire loops and probed with use of a current probe.



For more information, see page 3 in the *Current Sensor Resistors* section of the AWR6843ISK Schematic and Assembly Files.





The wire loops allow the four PMIC rails at device boundary to be probed individually. Using these measurements one can easily determine power consumed by the device.

5.2 Idle Mode Power Measurements

Measurements are shown below for each of the schemes described in section 5. Using the wire loop method and standard current probe one can replicate these measurements with very little deviation. The measurements below were performed at room temperature after the device had been chirping for a certain amount of time and then stopped. Moreover these measurements have been verified to be within 10% across several AWR6843ISK board revisions and device types.

5.2.1 Nominal Power Down Scheme Measurements

Power measurements for the Nominal Power Down Scheme described in Section 5 are shown below.

Nominal Scheme Functions	Device Power Consumption (mW)	Power Saved by Function (mW)	Total Power Saved by Scheme (mW)
Startup	895	0	0
DSP Power Off	738	157.2	157.2
MSS_VCLK to 40 MHz	576	162	319.2
RF Power Down	371.4	204.6	523.8
BSS Clock Gate	**292.2**	79.2	**603**

5.2.2 Full Power Down Scheme Measurements

Power measurements for the Full Power Down Scheme described in Section 5 are shown below.

Full Power Scheme Functions	Device Power Consumption (mW)	Power Saved by Function (mW)	Total Power Saved by Scheme (mW)
Startup	895	0	0
DSP power down	738	157.2	157.2
MSS VCLK 40	576	162	319.2
RF power down	372.6	203.4	522.6
APLL and GPADC power down	**217.8**	154.8	**677.4**

5.2.3 Fast Power Down Scheme Measurements

Power measurements for the Fast Power Down Scheme described in Section 5 are shown below.

Fast Power Scheme Functions	Device Power Consumption (mW)	Power Saved by Function (mW)	Total Power Saved by Scheme (mW)
Startup	895	0	0
DSS clock gate	750	145.2	145.2
MSS VCLK 40	588	162	307.2
BSS clock gate	**510**	78	**385.2**

6 References

- 68xx Low Power Demo on TI Resource Explorer
- *Programming Chirp Parameters in TI Radar Devices*

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