User's Guide

DLP® LightCrafter™ DLPC910 Evaluation Module (EVM)

ABSTRACT

The DLP® LightCrafter™ DLPC910 evaluation module (EVM) offers a reference design to enable faster development cycles for users of the DLPC910 Controller architecture in support of DMDs that use the DLPC910 controller. This platform targets applications needing high speed pattern management along with high resolution patterns.

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1 Overview

This guide explains the hardware features of the DLP LightCrafter DLPC910 EVM (DLPLCRC910EVM) system and operation of the DLPC910 Graphical User Interface (GUI). The EVM architecture and connectors are described along with a quick start guide on how to connect a supported DMD EVM and an AMD Xilinx VC-707 Evaluation Board (or equivalent) to the DLPLCRC910EVM to run patterns. A separate Virtex® 7 field programmable gate array (FPGA) Code User Guide [Link here] can be used to display patterns. Specific details for each DLP component can be found in related component documentation.

Note

DMD EVMs, the AMD Xilinx VC-707 evaluation board, power supply, optics, illumination source, and FPGA Mezzanine Card (FMC) cables are sold separately.

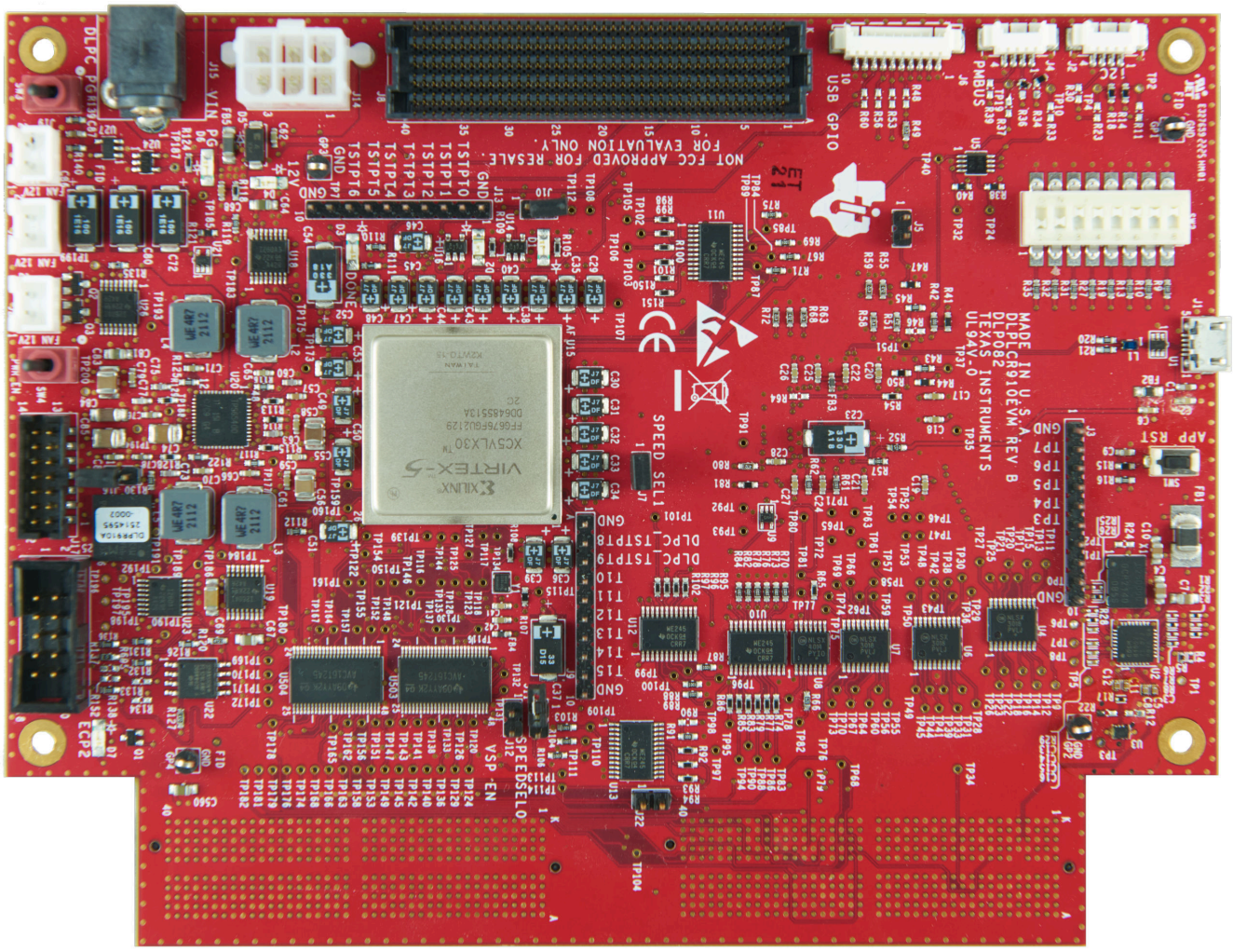

Figure 1-1. DLP LightCrafter DLPC910 Evaluation Module

2 If You Need Assistance

Refer to the TI E2E DLP products forum.

3 DLP LightCrafter DLPC910 EVM (DLPLCRC910EVM) Overview

3.1 Welcome

The DLPLCRC910EVM, coupled to a supported DMD EVM allows for easy evaluation of the DLP LightCrafter subsystem in bringing together high speed and high resolution display with advanced pattern control which is an excellent choice for:

- Lithography applications
  - Direct imaging
  - Flat panel display
  - Printed circuit board manufacturing
- Industrial
  - 3D printing
  - 3D scanners for machine vision
  - Quality control
- High speed imaging and display
  - 3D imaging
  - Augmented reality and information overlay

3.2 DLP LightCrafter DLPC910 Evaluation Module (DLPLCRC910EVM) Hardware

The DLPLCRC910EVM is one third of a complete DMD imaging electronics subsystem. The DLP LightCrafter DLPC910 EVM (DLPLCRC910EVM) consists of the DLPC910 board which includes a DLPC910 Digital Controller, a USB interface, power management circuits, and supporting digital logic.

Also needed to complete the imaging subsystem is a compatible DLP LightCrafter DMD EVM which is compatible with the DLPLCRC910EVM and an Apps FPGA board or other front end to send patterns to the DLPC910 controller. A DMD EVM consists of a DMD, a DMD board (PCB) containing on-board DMD power circuits, DMD mounting hardware when necessary, and a high pin count (HPC) FPGA mezzanine connector (FMC) cable for connections to the DLPC910 board.

Figure 3-1- block diagram outlining the major components of the DLPLCRC910EVM System Hardware.

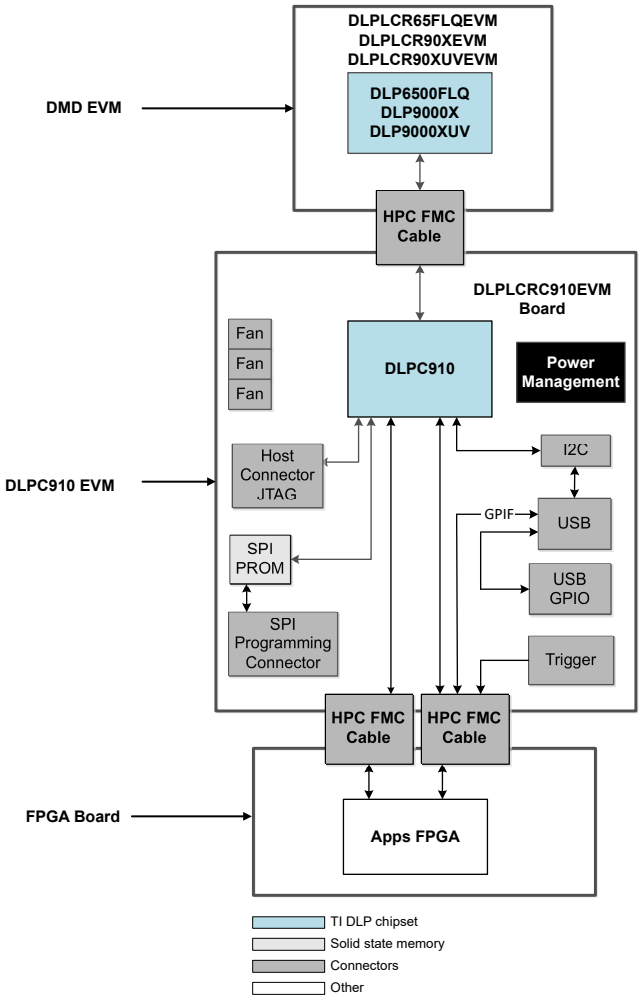

Figure 3-1. DLPLCRC910EVM Hardware Components

3.3 DLPLCRC910EVM Board

The DLPLCRC910EVM contains the electronics capable of controlling supported DMDs. The EVMs offer several interface options, USB, I^{2}C, a trigger input, and HPC FMC connectors to connect a supported DMD EVM board and an input board. Figure 3-2 shows the EVM block diagram of the DLPLCRC910EVM.

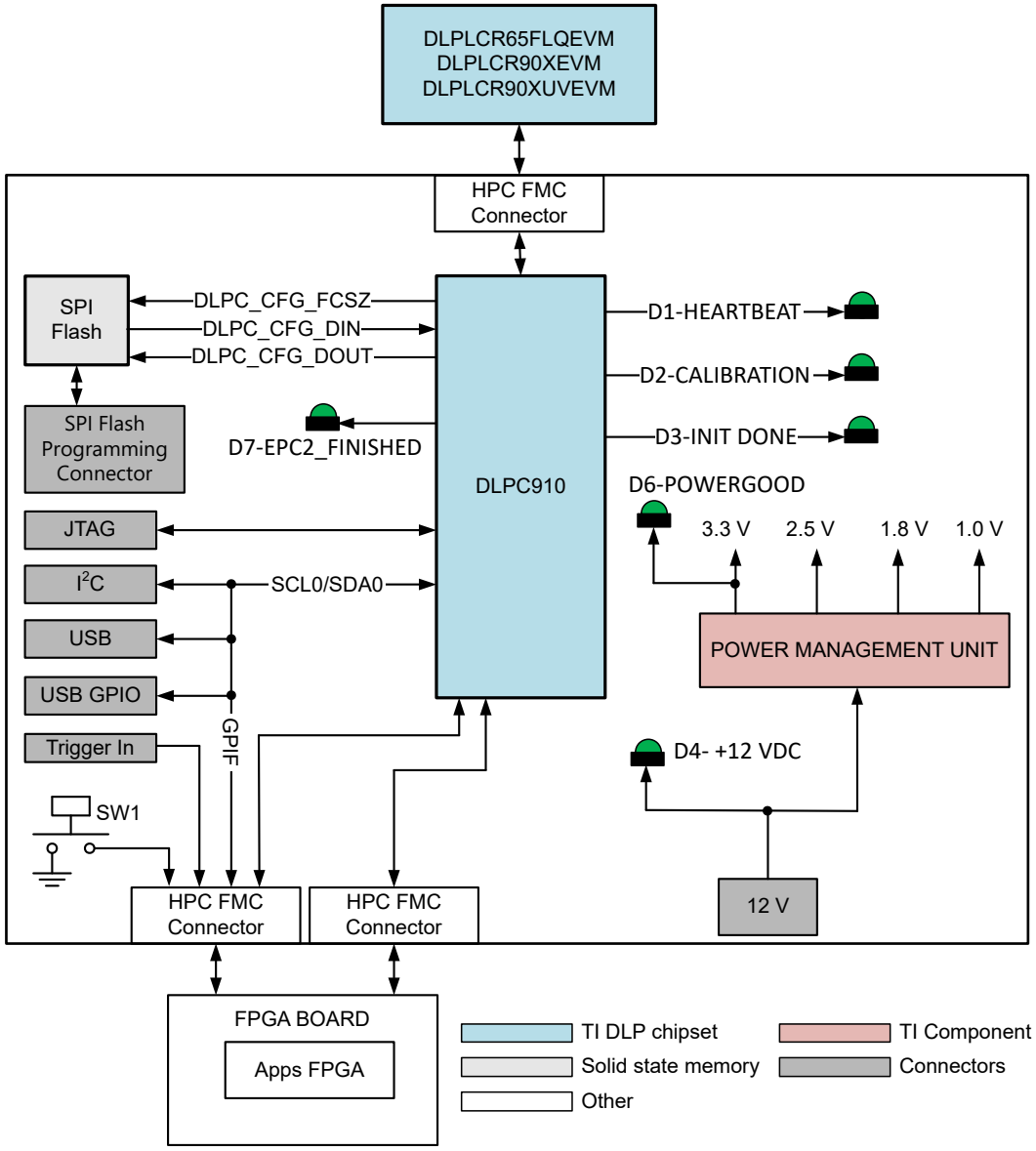

Figure 3-2. DLP LightCrafter DLPC910 EVM Block Diagram

The DLPLCRC910EVM major components are:

- DLPC910 Digital DMD Controller
- USB 2.0 interface
- Power Management Unit to supply power supplies to support the DLPC910 subsystem
- HPC FMC Connectors - one for a supported DMD EVM board and two for an attached FPGA or other front end board
- DLPC910 configuration SPI Flash memory

3.4 Other Items Needed for Operation

The DLPLCRC910EVM is a flexible evaluation module which, when coupled to one of the supported DLP DMD EVMs and an APPS FPGA board enables the sending of customer created patterns to the DLPC910 Controller, and then to the attached DMD for display. The DLP LightCrafter DLPC910 EVM and the supported DMD EVMs are offered for purchase separately so that customers can determine which elements customers wish to piece together for an application evaluation system.

The following items are not included with the EVM and need to be purchased separately if needed for customer evaluation:

- Supported DMD EVM board [DLPLCR65FLQEVM, DLPLCR90XEVM, or DLPLCR90XUVEVM]
- APPS FPGA board - example: AMD Xilinx VC-707 Evaluation Board (with separate power supply).
- Power supply - see Section 7.1 *External Power Supply Requirements* for details
- USB cable: A to Micro-B USB cable
- Illumination module or source
- Illumination and projection optics

3.5 DLPLCRC910EVM Connections

Figure 3-3 depicts the switches and connectors with their respective locations. Note: DMD EVM board, APPS FPGA board, power supply (and cable), and USB cable are NOT included with the module.

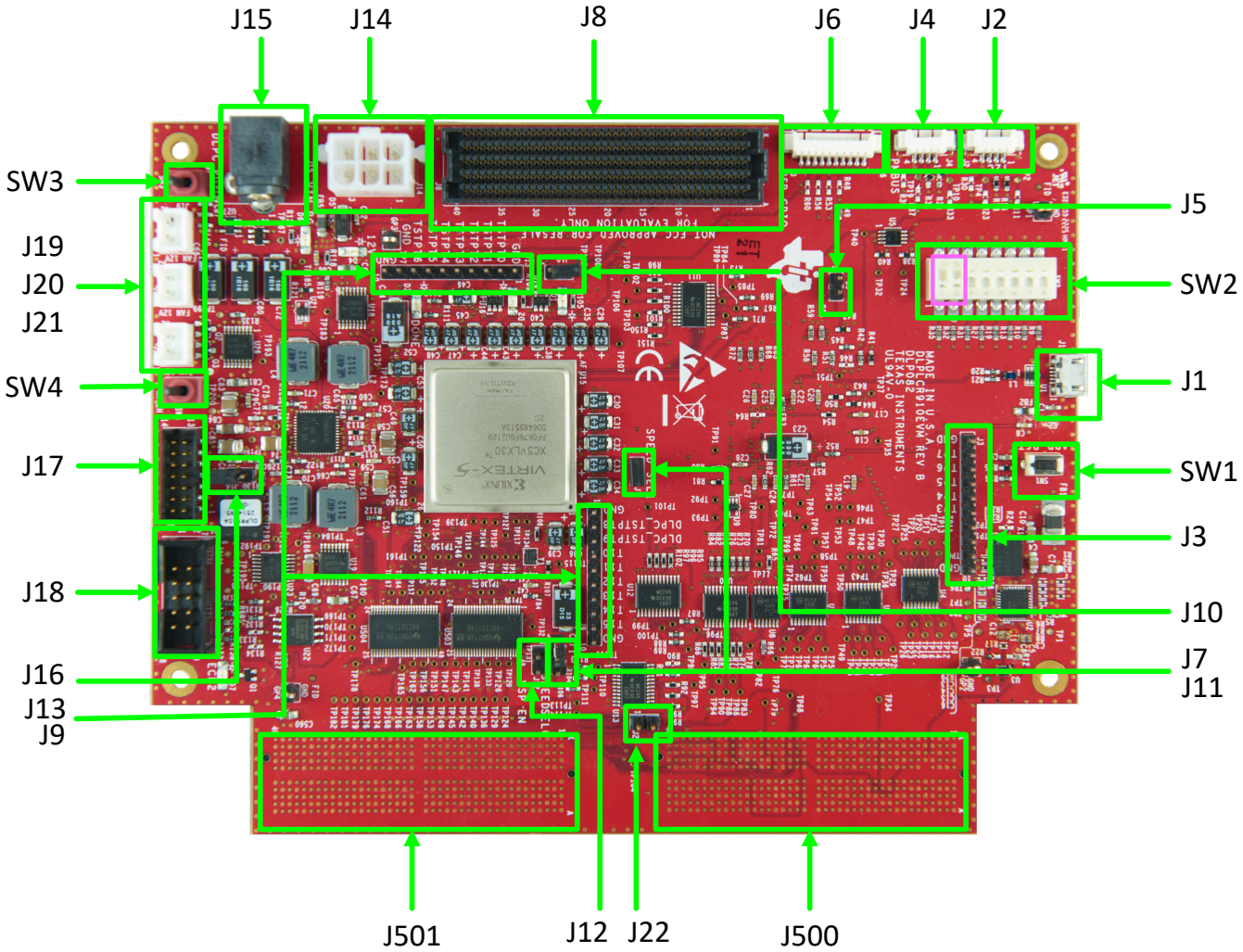

Figure 3-3. DLPLCRC910EVM Connectors (Top View)

Table 3-1. DLPLCRC910EVM Connector Reference

Connector Reference	EVM Function	Description or Use
SW1	Apps FPGA Reset Switch	Momentary contact switch to reset the Apps FPGA GUI code running on the attached AMD Xilinx VC-707 EVM. When released, the Apps FPGA boots from reset.
SW2	8 Position Apps FPGA Options dip switch	Used for selecting Apps FPGA options: • SW2_0: MIRROR FLOAT - Mirror Float Enable (Default not enabled = switch OFF) • SW2_1: LOAD4_ENZ - Load 4 enable switch. (Default not enabled = switch OFF) • SW2_2: COMP_DATA - Compliment Data (Default not enabled = switch ON) • SW2_3: NS_FLIP - Top to bottom flip (Default = not enabled switch ON) • SW2_4: Not Used (Default = switch ON) • SW2_5: Not Used (Default = switch ON) • SW2_6: Not Used (Default = switch ON) • SW2_7: WDT_ENZ - Watchdog timer enable (Default not enabled = switch ON) By default, positions 1 and 2 are in the switch "OFF" position [logic 1]. **Note** The inputs connected to SW2 are pulled high through a pullup resistor when in the "OFF" position [logic 1] and pulled low when in the "ON" position [logic 0]. Positions 0 and 1 are not enabled when the switch is "OFF" [logic 1] and positions 2, 3, and 7 are not enabled when "ON" [logic 0].
SW3	DMD Park	Turning this switch off issues PWR_FLOAT and parks the DMD and stops the DLPC910 logic. **Note** Turn this switch off before disabling power with SW4 and turn this switch on before enabling power with SW4. Once SW3 is turned off a full power cycle using SW4 is required to restore operation.
SW4	Power Enable Switch	Enables Power on the DLPLCRC910EVM. **Note** Turn on SW3 (PWR_FLOAT - DMD Park) before enabling power and turn off SW3 before disabling power.
J1	Micro USB B Connector	Connect USB cable from PC running DLPC910 GUI.
J2	External I^2C PMBUS	I^2C connector.
J3	Apps FPGA Test Points 0 - 7	Apps FPGA connected test points: • GND: Pin 1 • APPS_TSTPT7: Pin 2 -Apps FPGA DLPC910 Trigger (input) • APPS_TSTPT6: Pin 3 - debounced SW5 push button (output) • APPS_TSTPT5: Pin 4 - data enable from apps loader (output) • APPS_TSTPT4: Pin 5 - load busy from apps loader (output) • APPS_TSTPT3: Pin 6 - mirror settling busy from apps loader (output) • APPS_TSTPT2: Pin 7 - trigger from the apps loader (output) • APPS_TSTPT1: Pin 8 - mirror reset busy from apps loader (output) • APPS_TSTPT0: Pin 9 - mirror reset active signal (output) • GND: Pin 10
J4	External PMBUS	PMBUS connector for TI development and test only.
J5	Prom address select	Prom address select for USB firmware load [default address 001 - not populated; address 011 - populated].

Table 3-1. DLPLCRC910EVM Connector Reference (continued)

Connector Reference	EVM Function	Description or Use
J6	USB GPIO B0 - B7	USB GPIO Header: • GND: Pin 1 • USB GPIO B7: Pin 2 • USB GPIO B6: Pin 3 • USB GPIO B5: Pin 4 • USB GPIO B4: Pin 5 • USB GPIO B3: Pin 6 • USB GPIO B2: Pin 7 • USB GPIO B1: Pin 8 • USB GPIO B0: Pin 9 • GND: Pin 10 These pins are available for customer definition or future use.
J7	DCLKIN Speed Selection Pin 1	SPEED_SEL_1 used in conjunction with J11 (SPEED_SEL_0) to select 400 or 480 MHz operation. Routed to Apps FPGA. Configurations: • 400 MHz: J7 and J11 jumpered - DLP6500FLQ, DLP9000X, or DLP9000XUV (default) • 480 MHz: J7 jumpered and J11 not jumpered - DLP9000X and DLP9000XUV only **Note** The DLPLCR65FLQEVM does NOT run at 480 MHz.
J8	DMD EVM Board HPC FMC Connector	Used to connect a DLPLCR65FLQEVM, DLPLCR90XEVM, or DLPLCR90XUVEVM.
J9	DLPC910 Test Points 8 - 15	DLPC910 connected test points: • GND: Pin 1 • DLPC_TSTPT8: Pin 2 • DLPC_TSTPT9: Pin 3 • DLPC_TSTPT10: Pin 4 • DLPC_TSTPT11: Pin 5 • DLPC_TSTPT12: Pin 6 • DLPC_TSTPT13: Pin 7 • DLPC_TSTPT14: Pin 8 • DLPC_TSTPT15: Pin 9 • GND: Pin 10 Reserved for TI internal testing and debug.
J10	DLPC910 I^2C Address Selector Jumper	Selects the DLPC910 I^2C Address: • 0x36: Not jumpered (default) • 0x34: Jumpered **Note** If installed, then use the DLPC910 Status/Control Registers Settings page to change the I^2C address to operate correctly.

Table 3-1. DLPLCRC910EVM Connector Reference (continued)

Connector Reference	EVM Function	Description or Use
J11	DCLKIN Speed Selection Pin 0	SPEED_SEL_0 used in conjunction with J7 (SPEED_SEL_1) to select 400 or 480 MHz operation. Routed to Apps FPGA. Configurations: • 400 MHz: J7 and J11 jumpered - DLP6500FLQ, DLP9000X, or DLP9000XUV (default) • 480 MHz: J7 jumpered and J11 not jumpered - DLP9000X and DLP9000XUV only **Note** The DLPLCR65FLQEVM does **not** run at 480 MHz. Although the DLP9000X and DLP9000XUV run at 400 MHz, only 480 MHz operation has been fully validated.
J12	VSP Enable (no longer used)	This jumper is no longer used.
J13	DLPC910 Test Points 0 - 7	DLPC910 connected test points: • GND: Pin 1 • DLPC_TSTPT0: Pin 2 • DLPC_TSTPT1: Pin 3 • DLPC_TSTPT2: Pin 4 • DLPC_TSTPT3: Pin 5 • DLPC_TSTPT4: Pin 6 • DLPC_TSTPT5: Pin 7 • DLPC_TSTPT6: Pin 8 • DLPC_TSTPT7: Pin 9 • GND: Pin 10 Reserved for TI internal testing and debug.
J14	+12 VDC 6-Pin Power Connector (Alternate)	EVM power alternate input. [Pin 1,2,3 = GND, Pin 4,5,6 = +12 VDC,] See Section 7.1.
J15	+12 VDC Power input	EVM power input. [Pin 1 = +12 VDC, Pin 2,3 = GND] See Section 7.1.
J16	REV_SEL_0	DLPR910 Configuration Prom Revision Selection Jumper. REV_SEL_1 is held low. • Not jumpered = 0 (default) • Jumpered = 1 - Not Used
J17	JTAG Connector	JTAG header for connecting a JTAG programmer to the DLPR910.
J18	Flash Configuration Connector	SPI Flash programming connector.
J19, J20, J21	+12 VDC external Fan Connectors	2-pin +12 VDC fan connectors [Pin 1 = GND, Pin 2 = +12 VDC]
J22	Apps FPGA Reset Jumper	Jumper 22 prevents SW1 from pulling the Apps FPGA on the attached AMD Xilinx VC-707 EVM into reset. • Not jumpered = Allows SW1 to pull the Apps FPGA into reset (default) • Jumpered = Prevent SW1 from pulling Apps FPGA into reset
J500	Apps FPGA FMC connector 1	DLPC910 to Apps FPGA and USB parallel interface to the Apps FPGA 400 pin FMC connector.
J501	Apps FPGA FMC connector 2	DLPC910 to the Apps FPGA 400 pin FMC connector.

3.6 DLP LightCrafter DLPC910 LEDs

DLP LightCrafter DLPC910 EVM LEDs (Top View - Upper Left) and DLP LightCrafter DLPC910 EVM LEDs (Top View - Lower Left) depicts the LEDs with their respective locations:

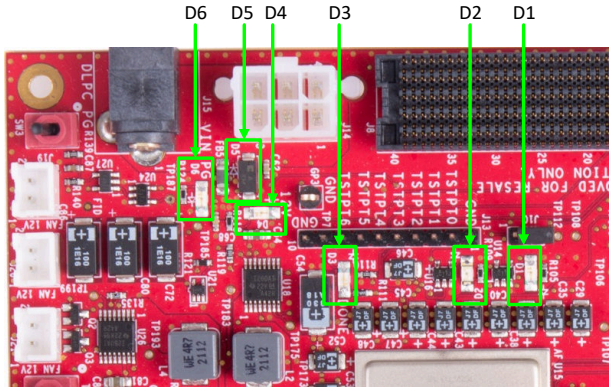

Figure 3-4. DLP LightCrafter DLPC910 EVM LEDs (Top View - Upper Left)

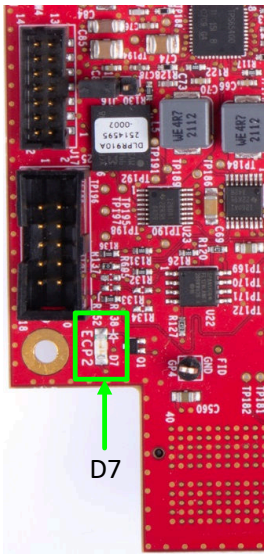

Figure 3-5. DLP LightCrafter DLPC910 EVM LEDs (Top View - Lower Left)

Table 3-2. DLP LightCrafter DLPC910 EVM LED Reference

Connector Reference	EVM Function	Description or Use
D1	Heartbeat LED [Flashing]	Flashes when DLPC910 controller is running
D2	Calibration Active	Illuminates while calibration is active
D3	DLPC910 Done	DLPC910 Initialization complete
D4	12 V Power	+12 VDC is present on the input connector
D6	Power Good	All voltages are present and stable
D7	ECP2 Finished	DLPC910 configuration via SPI Flash complete

Note

D5 is a protection Zener diode for the +12 VDC input and is not an LED.

3.7 Apps FPGA Trigger Input

On the DLPLCRC910EVM the trigger input for the DLPC910 is mediated through the Apps FPGA.

Connecting header J3 APPS_TSTPT7 (Pin 2) to J3 APPS_TSTPT6 (Pin 3) allows the use of SW5 on the AMD Xilinx VC-707 board (lower right corner) to advance patterns when pressed.

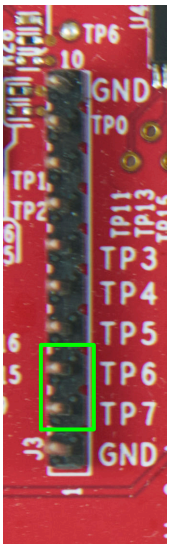

Figure 3-6. J3 Apps FPGA Test Point Header

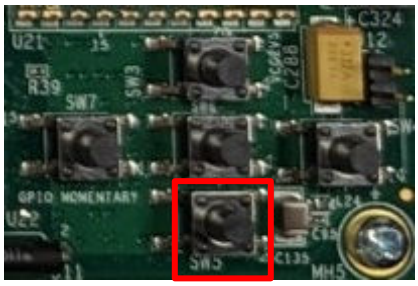

Figure 3-7. VC-707 SW5

3.8 DLPLCRC910EVM HPC FMC Cables

DMD EVMs supported by the DLPLCRC910EVM come supplied with a 300 mm Samtec™ 400-pin HPC FMC cable [SAMTEC HDR-169468-01]. HPC FMC Cable (Front and Back) shows the front and back of the cable. The cable is keyed and can only be installed one way on the DLPLCRC910EVM and on the DMD EVM. As shows the left end is the DLPLCRC910EVM end and the right end is the DMD EVM end.

Use of the cable is optional. The EVM can be connected directly to the DLP LightCrafter DLPC910 EVM J8 HPC FMC connector.

Figure 3-8. HPC FMC Cable (Front and Back)

Use caution when bending the flex cable to not exceed bending guidelines provided by the cable manufacturer.

3.9 DLPLCRC910EVM and DMD EVM Assembly

The DLPC910 EVM requires a compatible DMD EVM such as the DLPLCR65FLQEVM, DLPLCR90XEVM, or DLPLCR90XUVEVM.

- The DMD EVM male HPC FMC connector can be connected directly to the DLPLCRC910EVM female HPC FMC connector
- The 300 mm Samtec HPC FMC ribbon cable provided with the DMD EVMs can be used to provide more flexibility in the positioning of the DMD board relative to the DLPLCRC910EVM board. Attach the HPC FMC male connector end of the cable to the female HPC FMC connector on the DLPLCRC910EVM board and the HPC FMC female end of the cable to the male HPC FMC connector on the DMD EVM board.

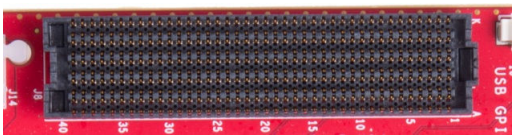

Figure 3-9. DLPLCRC910EVM Female HPC FMC Connector

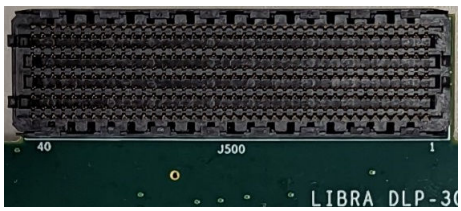

Figure 3-10. DLPLCR65FLQEVM Male HPC FMC Connector

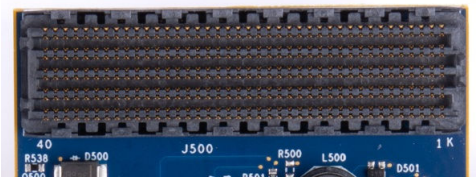

Figure 3-11. DLPLCR90XEVM Male HPC FMC Connector

Figure 3-12. Samtec 300 mm HPC FMC Extension cable (Front and Back)

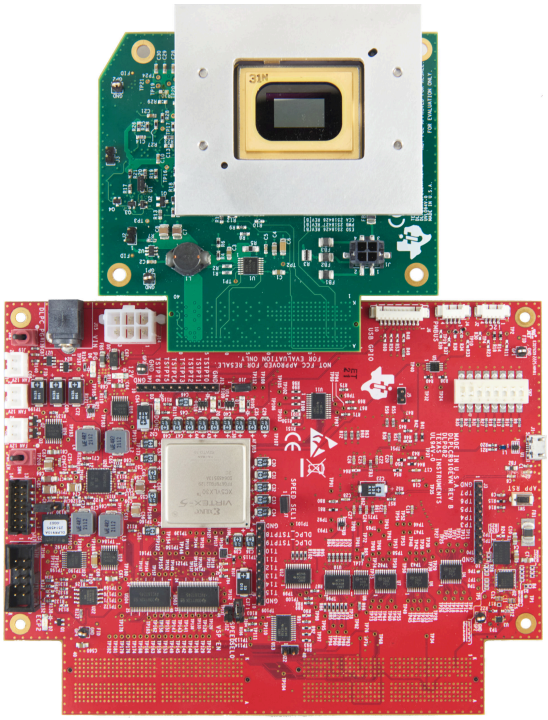

Figure 3-13. Assembled DLPLCRC910EVM with DLPLCR65FLQEVM (without cable)

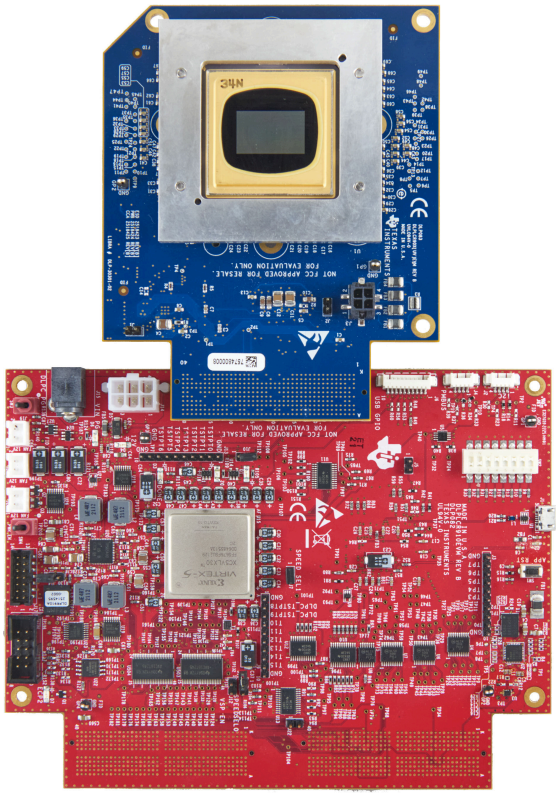

Figure 3-14. Assembled DLPLCRC910EVM with DLPLCR90XEVM or DLPLCR90XUVEVM (without cable)

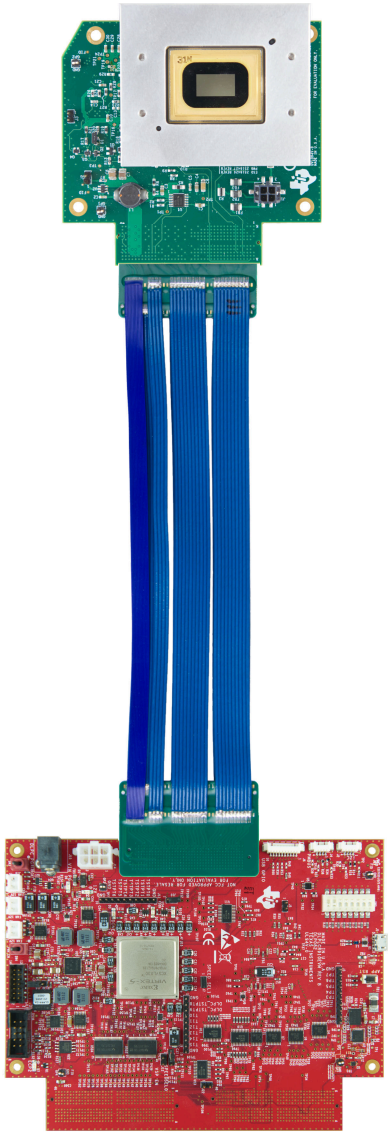

Figure 3-15. Assembled DLPLCRC910EVM with DLPLCR65FLQEVM (with cable)

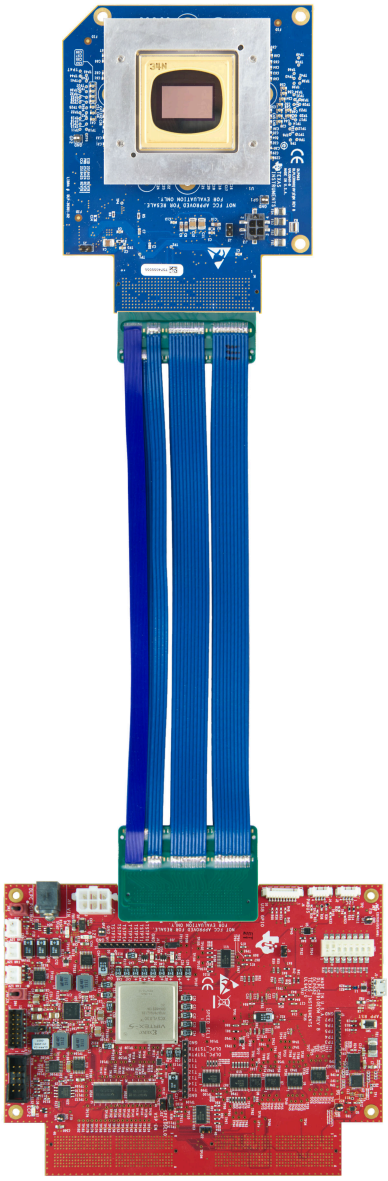

Figure 3-16. Assembled DLPLCRC910EVM with DLPLCR90XEVM or DLPLCR90XUVEVM (with cable)

3.10 Connecting an Apps FPGA Board to the DLPLCRC910EVM

The DLPLCRC910EVM requires a compatible Apps board, such as the AMD Xilinx VC-707 board or similar to send control and pixel data to the DLPLCRC910EVM.

If using the AMD VC-707 board, set SW2- 1 ON and SW11-4 ON as shown in AMD VC-707 Board Dip Switch Settings.

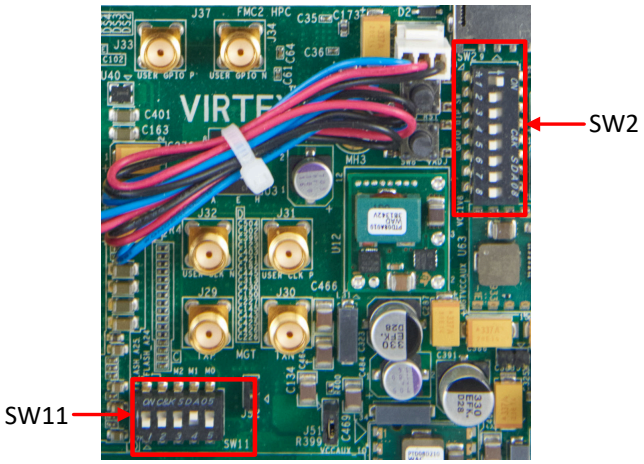

Figure 3-17. AMD VC-707 Board Dip Switch Settings

- The APPS female HPC FMC connectors connect directly to the DLPLCRC910EVM male HPC FMC connectors
  - Line up the HPC FMC male connectors on the DLPLCRC910EVM with the HPC FMC female connectors on the Apps FPGA board.

Note

Verify that the connectors are lined up correctly before applying pressure to connect the boards.

  - Firmly apply pressure to the boards to allow the connectors to fully mate. After the initial application of pressure, apply pressure at one end and then the other until the connectors are fully seated.

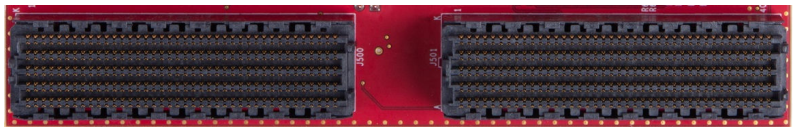

Figure 3-18. DLPLCRC910EVM Male HPC FMC Connectors (for Apps FPGA Board)

Figure 3-19. AMD Xilinx VC-707 Female HPC FMC Cable Connectors

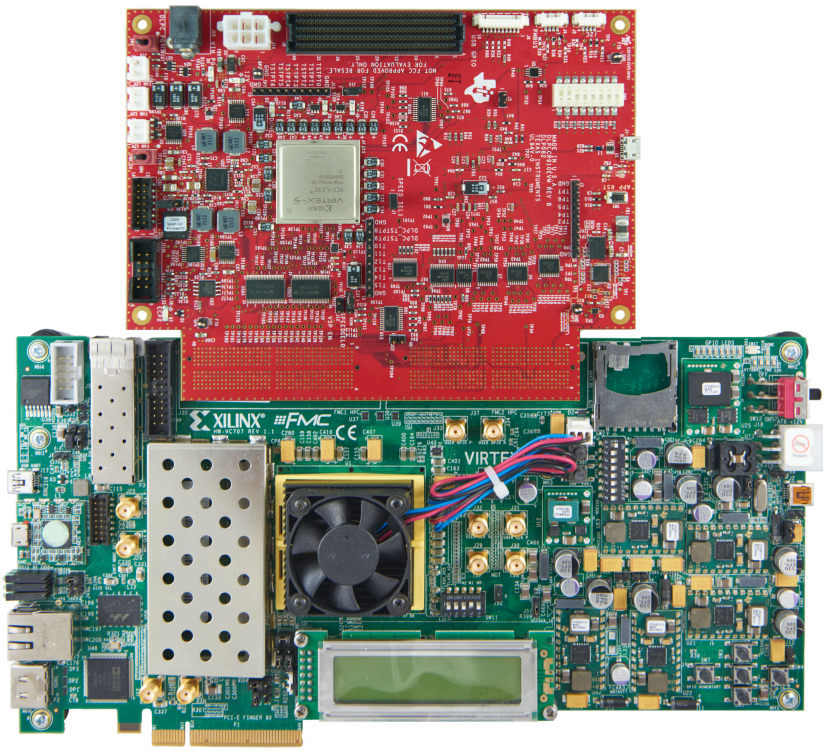

Figure 3-20. Assembled DLPLCRC910EVM with AMD Xilinx VC-707 board (without cables)

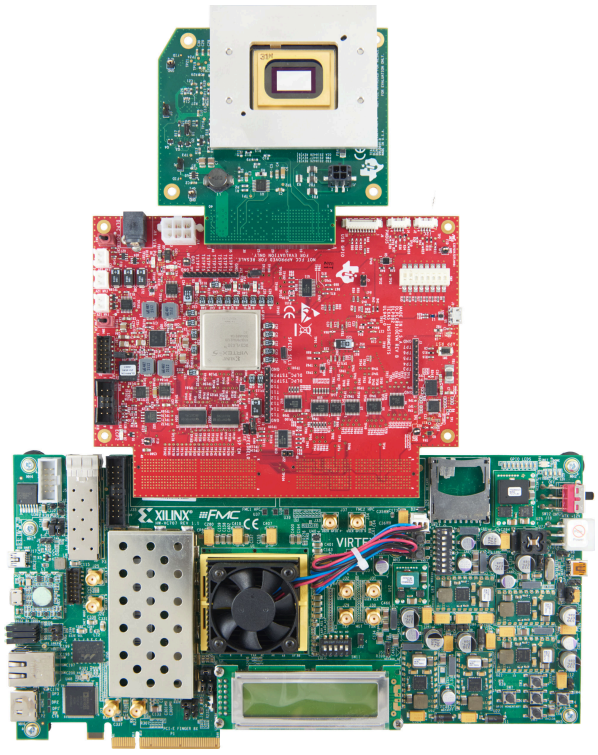

Figure 3-21. Fully Assembled DLPLCRC910EVM - AMD Xilinx VC-707 - DLPLCR65FLQEVM (without cables)

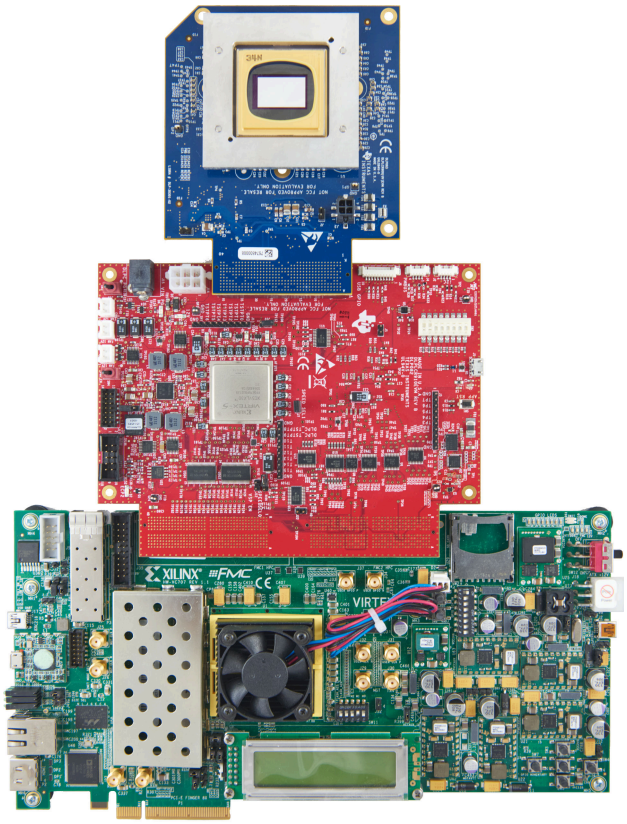

Figure 3-22. Fully Assembled DLPLCRC910EVM - AMD Xilinx VC-707 - DLPLCR90XEVM or DLPLCR90XUVEVM (without cables)

The 300 mm Samtec HPC FMC ribbon cables are an alternative for these connections. Two cables are needed. The board and cable connectors are keyed.

- Attach the HPC FMC female connector end of the cables to the male HPC FMC connectors on the DLPLCRC910EVM board.
- Attach the HPC FMC male connector end of the cables to the female HPC FMC connectors on the Apps FPGA board .

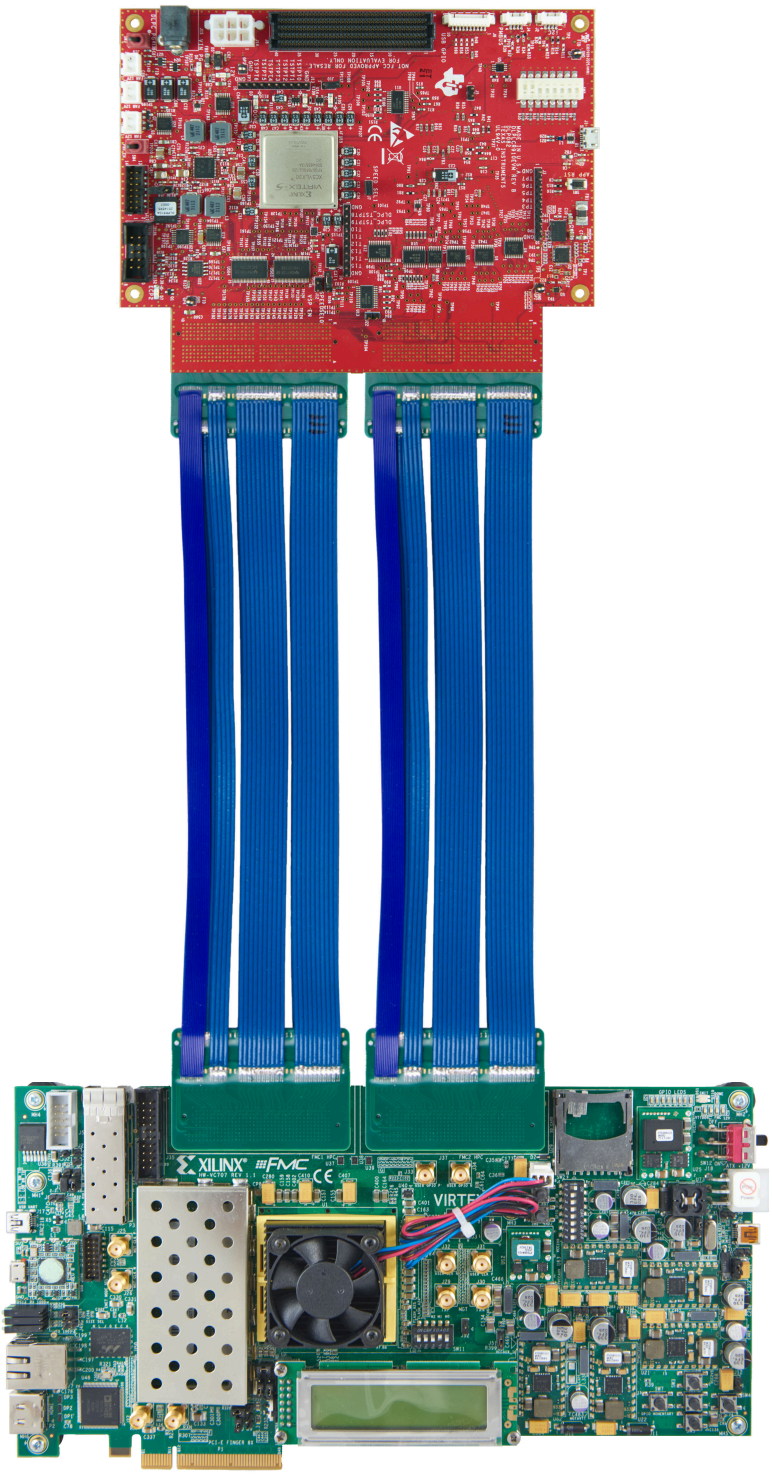

Figure 3-23. Assembled DLPLCRC910EVM with AMD Xilinx VC-707 board (with cables)

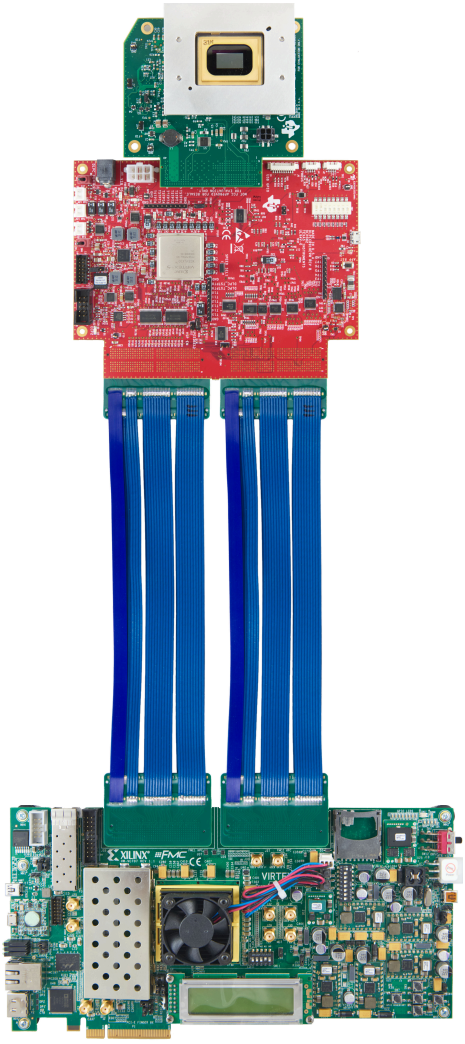

Figure 3-24. Fully Assembled DLPLCRC910EVM - AMD Xilinx VC-707 - DLPLCR65FLQEVM (with cables)

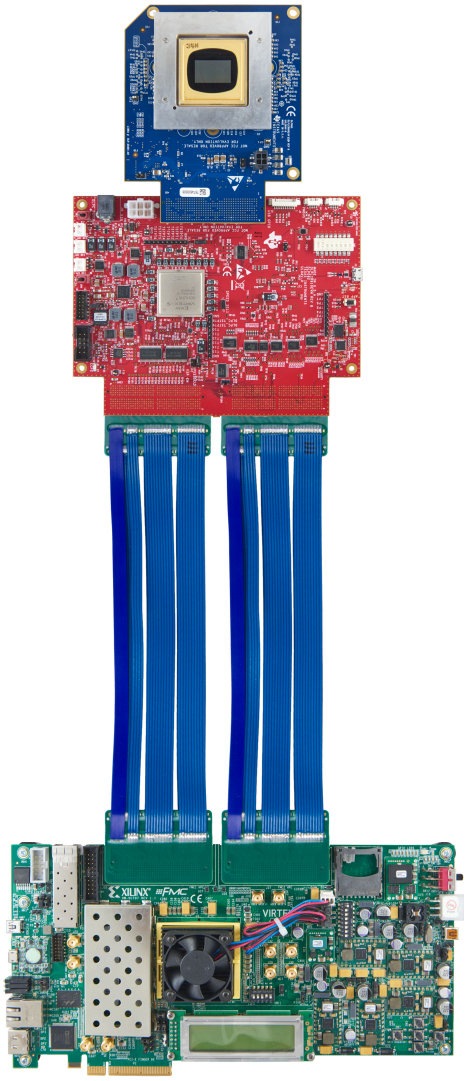

Figure 3-25. Fully Assembled DLPLCRC910EVM - AMD Xilinx VC-707 - DLPLCR90XEVM or DLPLCR90XUVEVM (with cables)

4 Quick Start

This chapter offers a quick start guide to power-up the DLPLCRC910EVM and run the GUI control software.

4.1 Power-up the DLPLCRC910EVM

The DLPLCRC910EVM is ready to use after assembling with a supported DMD EVM and a front end board such as the AMD Xilinx VC-707 EVM. Steps 1 through 6 show how to power, display an image, and connect the EVM to a PC.

1. Before connecting the AMD Xilinx VC-707 board program the configuration PROM per the instructions in AMD Xilinx VC-707 Configuration PROM Programming.
2. Connect a 12-V DC power supply to the power supply connector J15 in Figure 3-3.
3. LED — D4 illuminates if power is present at J15.
4. Power on the AMD Xilinx VC-707 board.

Note

Allow sufficient time for the VC-707 board to configure (10 seconds is suggested).

5. Turn on SW3 [DMD Park (PWR_FLOAT)].
6. Turn on SW4 [Power Enable].
7. LED — D7 illuminates indicating that the PROM has configured the DLPC910.
8. LED — D2 briefly illuminates indicating calibration is in progress and goes out when complete.
9. LED — D1 flashes (heartbeat) to indicating that the DLPC910 is running.

Note

A DMD EVM board and a properly configured AMD Xilinx VC-707 board must be present for the DLPC910 to initialize.

10. Connect a USB cable from a PC to connector J1 on the DLPLCRC910EVM, as seen in Figure 3-3. The first time the cable is connected on a PC, the DLPLCRC910EVM enumerates. The required drivers are installed as part of the DLPLCRC910EVM GUI installation.
11. The DLPLCRC910EVM can be controlled with the GUI software available for download from the DLPLCRC910EVM Tool Folder.

4.2 Power-down the DLPLCRC910EVM

To shut down the DLPLCRC910EVM follow steps 1 through 4:

1. Recommended: In the DLPC910 GUI issue a DMD Park (PWR_FLOAT) command

Note

Issuing a **DMD Park** (PWR_FLOAT) via software is not required but is good practice.

2. Turn off SW3 [DMD Park]
3. Turn off SW4 [Power Enable]
4. Power off the AMD Xilinx VC-707 board

5 Operating the DLPLCRC910EVM

This chapter introduces the Windows GUI software provided with the DLPLCRC910EVM.

5.1 DLPLCRC910EVM GUI and Apps FPGA Software

The DLPC910REF-SW includes a GUI application to control the Apps FPGA, GUI source code, a prom file for the AMD Xilinx VC-707 board, and Apps FPGA VHDL source code.

For details on the Apps FPGA VHDL source code please see DLPC910 Apps FPGA Guide

5.2 PC Software

Upon execution of the DLPC910 GUI application, the panel shown in Figure 5-1 is displayed. The GUI panel contains the following:

- Menu bar (top)
- Icon ribbon bar (top)
- Main window with:
  - Script Command sub-window
  - Script sub-window
  - Status sub-window
- Hardware Connected - information bar (bottom):
  - *Apps Com Ok* - Apps FPGA communication
  - *910 Com Ok* - DLPC910 communication
  - Connected DMD:
    - *DLP6500* -
    - *DLP9000X* - reported for both DLP9000X and DLP9000XUV

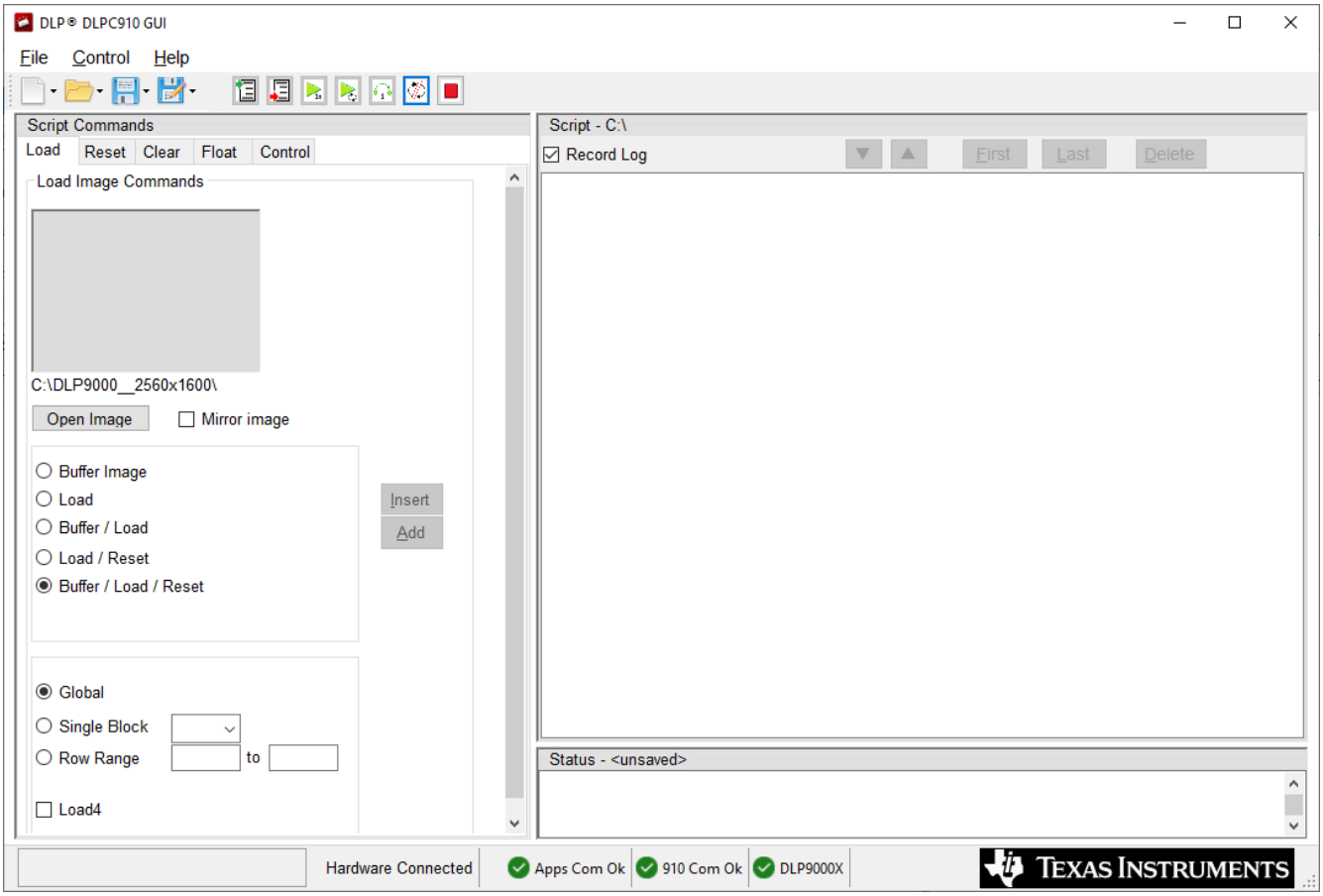

Figure 5-1. DLPLCRC910EVM GUI

Note

If the connection status shows **910 Com Err** check J10 I^2C address selection. See DLPLCRC910EVM Connections.

Note

If the text in the GUI does not display correctly please change the DPI settings. Right click on the executable and select *Properties*. On the *Compatibility* tab select the "Change high DPI settings" button. Change your settings as shown in Figure 5-2.

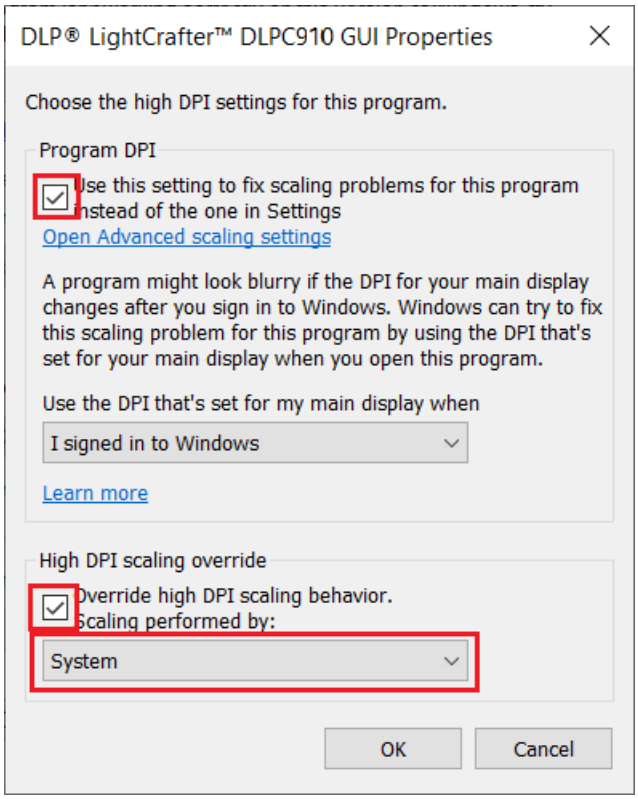

Figure 5-2. High DPI Settings

5.2.1 Menu Bar

The DLPLCRC910EVM Menu bar consists of three items:

1. **File Menu**

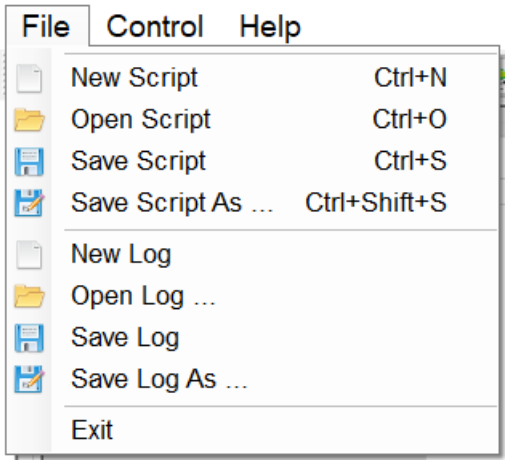

Figure 5-3. File Menu

Script items

- ***New Script*** empties the Script sub-window to record a new script.
- ***Open Script*** opens a dialogue box to select an existing script from the disk.
- ***Save Script*** saves the current contents of the Script sub-window to the current script file. If the file is not yet saved the save as dialogue opens.
- ***Save Script As*** opens a dialogue box to save the current script with a new name.

Log items

- ***New Log*** empties the Status sub-window to record a new command log sequence.
- ***Open Log*** opens a dialogue box to select an existing command log sequence file from the disk.
- ***Save Log*** saves the current contents of the Status sub-window to the current script file. If the file is not yet saved the save as dialogue opens.
- ***Save Log As*** opens a dialogue box to save the current command log sequence with a new name.

2. **Control Menu**

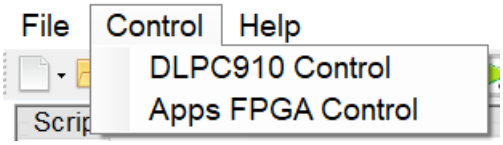

Figure 5-4. Control Menu

- ***DLPC910 Control*** displays the DLPC910 Register Control page.
- ***Apps FPGA Control*** displays the Apps FPGA Registers page.

3. **Help Menu**

Figure 5-5. Help Menu

About DLP® LightCrafter DLPC910 GUI displays the Software Version, USB DLL Version, and USB FW Version information box:

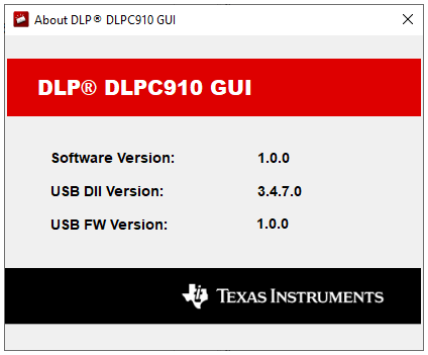

Figure 5-6. About Box

5.2.2 Icon Bar

The ***Icon*** bar has four File Controls and seven Script Controls as shown in Figure 5-7.

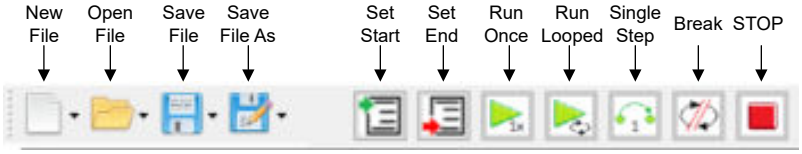

Figure 5-7. Icon Bar

File Controls:

- ***New File*** dropdown:
  - ***Script*** - empties the Script sub-window to record a new script.
  - ***Status*** - empties the Status sub-window to record a new command log sequence.
- ***Open File*** dropdown:
  - ***Script*** - opens a dialogue box to select an existing script from the disk.
  - ***Status*** - opens a dialogue box to select an existing command log sequence file from the disk.
- ***Save File*** dropdown:
  - ***Script*** - saves the current contents of the Script sub-window to the current script file. If the file is not yet saved the save as dialogue opens.
  - ***Status*** - saves the current contents of the Status sub-window to the current script file. If the file is not yet saved the save as dialogue opens.
- ***Save File As*** dropdown:
  - ***Script*** - opens a dialogue box to save the current script with a new name.
  - ***Status*** - opens a dialogue box to save the current command log sequence with a new name.

Script Controls:

- ***Set Start*** - sets the starting line in the script
- ***Set End*** - sets the ending line in the script
- ***Run Once*** - runs the current script in the Script window one time. If the start and end point are set executes only the lines from *start* to *end* one time.
- ***Run Looped*** - runs the script repeatedly until *Break* or *STOP* are pressed. If the start and end point are set executes only the lines from *start* to *end* repeatedly.
- ***Single Step*** - executes the highlighted line and moves to the next script line.
- ***Break*** - stops execution until pressed again or until *Run Once* or *Run Looped* is pressed
- ***STOP*** - halts script execution and resets the script.

5.2.3 Main Window

The **Main Window** consists of three sub-windows:

5.2.3.1 Script Commands sub-window

Script Commands are divided into five tabs:

5.2.3.1.1 Load Tab

Load Image Commands

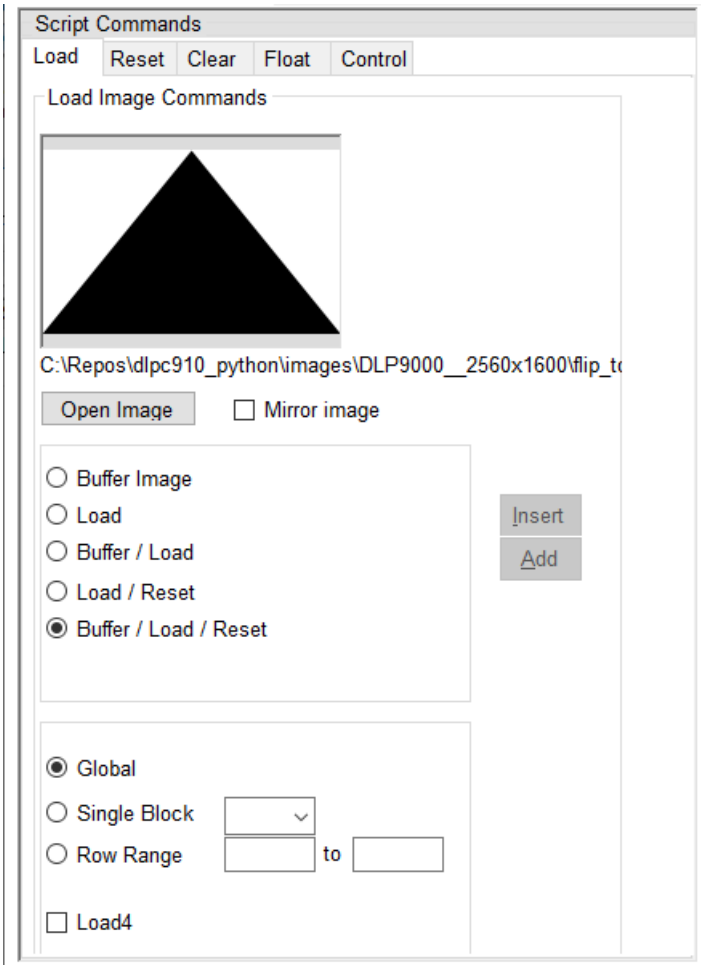

Figure 5-8. Load Tab

- ***Open Image*** button - opens a dialogue box to select an image to use for loading the Apps FPGA user pattern buffer.

  Note

  Images the size of the native DMD resolution are required. Images larger than the DMD resolution are truncated to the native resolution of the attached DMD.

- ***Mirror Image*** check box - when checked the image data is reversed left to right when buffering to the Apps FPGA user buffer resulting in a *mirror image*.

The Apps FPGA contains a user image buffer which is populated independent of:

- sending the pixel data to the attached DMD via the DLPC910 controller.
- requesting a DMD mirror reset [mirror clocking pulse (MCP)] to update the pixel data sent to the mirror array.

There are three commands:

- **Buffer** - loads pixel data into a user pattern buffer inside the Apps FPGA.

- **Load** - sends the data currently in the Apps FPGA buffer via the DLPC910 controller to the attached DMD.
- **Reset** - requests a DMD MCP of the specified blocks on the DMD (Global, Single, Dual, or Quad block reset).

Buffer, Load, and Reset commands are able to be entered separately (Reset only commands are entered from the ***Reset Tab*** or grouped together in a single script entry:

- ***Buffer Image*** - sends the image data from the selected image to the Apps FPGA user buffer. The selection of Global, Single Block, or Row Range determines the data buffered.
- ***Load*** - sends the image data in the Apps FPGA user buffer to the attached DMD via the DLPC910 controller. The selection of Global, Single Block, or Row Range determines the data sent.
- ***Buffer / Load*** - sends the image data from the selected image to the Apps FPGA user buffer based on the selection of Global, Single Block, or Row Range and sends the selected image data in the Apps FPGA user buffer to the attached DMD via the DLPC910 controller.
- ***Load / Reset -*** sends image data stored in the Apps FPGA user buffer to the attached DMD via the DLPC910 controller and resets the DMD mirrors based on the selection of Global, Single Block, or Row Range.

Note

For a row range the required blocks are reset to display the rows loaded.

- ***Buffer / Load / Reset*** - sends the image data from the selected image to the Apps FPGA user buffer, then sends the selected image data in the Apps FPGA user buffer to the attached DMD via the DLPC910 controller and resets the DMD based on the selection of Global, Single Block, or Row Range.

Note

For a row range the required blocks are reset to display the rows loaded.

- ***Global*** - directs the ***Load*** command to load all of the data from the Apps FPGA user buffer and directs the ***Reset*** command to reset all DMD blocks at the same time.
- ***Single Block*** - directs the ***Load*** command to load the data from the Apps FPGA user buffer to the specified block and directs the ***Reset*** command to reset the specified DMD block.
- ***Row Range*** - directs the ***Load*** command to load the data from the Apps FPGA user buffer to the specified row range and directs the ***Reset*** command to reset the DMD blocks that encompass the specified rows.
- ***Load4*** check box - is intended for Global mode only and directs the ***Load*** command to load only the first ¼ of the Apps FPGA user buffer to the attached DMD via the DLPC910 controller.

Note

Using ***Load4*** with other modes besides ***Global*** resets results in unpredictable behavior.

Once an image is selected, the desired operation (Buffer - Load - Reset) or combination is selected, and the Load - Reset mode is selected press one of the following options:

- ***Insert*** button - inserts the command between the highlighted command and the prior command in the ***Script*** sub-window. If there are no commands in the ***Script*** **sub-window**, then no entry is made.

Note

Take care that the command is valid in the position inserted.

- ***Add*** button - adds the command as the last line in the ***Script*** **sub-window**.

5.2.3.1.2 Reset Tab

Separate DMD reset commands:

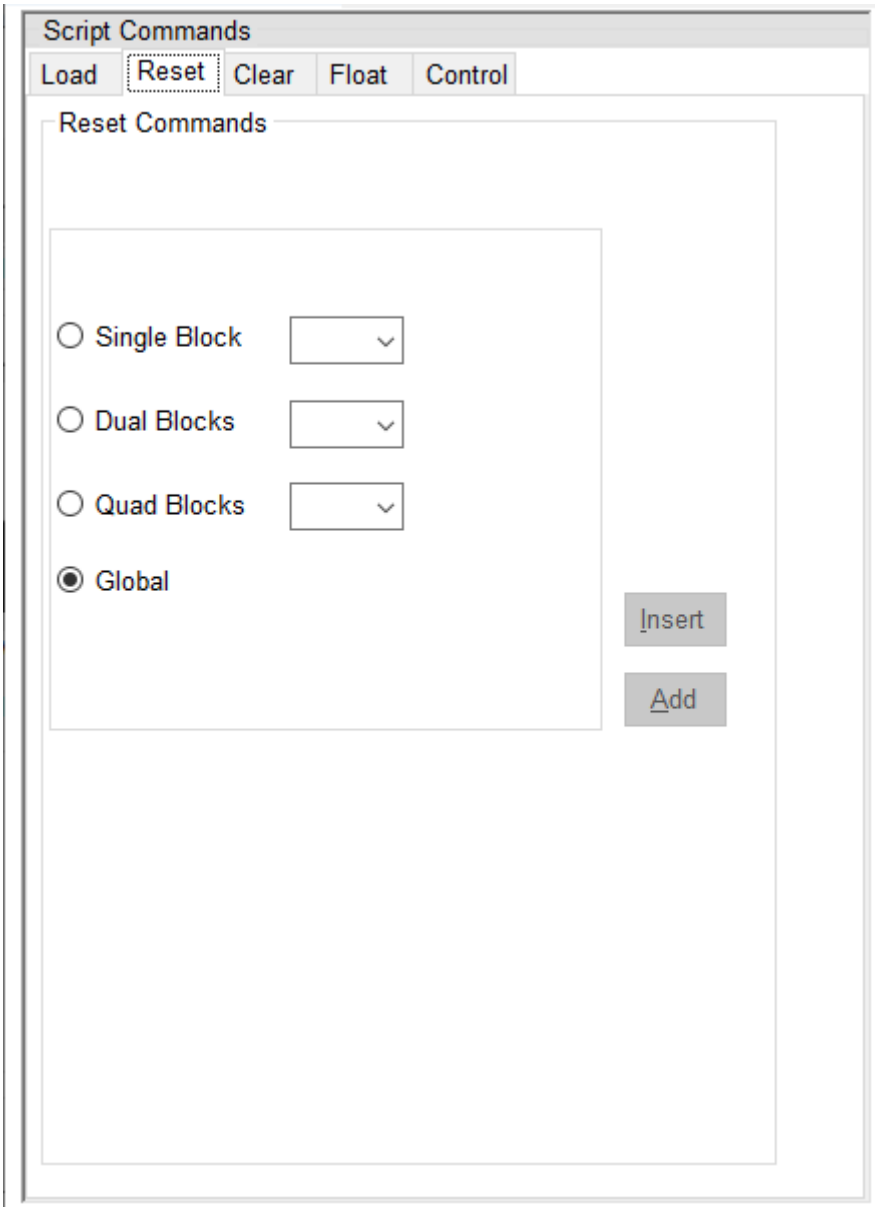

Figure 5-9. Reset Tab

- ***Single Block*** radio button - selects a single block from the drop-down list to reset on the DMD:
  - The DLP9000X DMD and DLP9000XUV have 16 selectable blocks
  - The DLP6500 DMD has 15 selectable blocks
- ***Dual Block*** radio button - selects group of two blocks from drop-down list to reset on the DMD:
  - The DLP9000X DMD and DLP9000XUV have the following selectable dual block groups - (1,2), (3,4), (5,6), (7,8), (9,10), (11,12), (13,14), and (15,16).
  - The DLP6500 DMD has the following selectable dual block groups - (1,2), (3,4), (5,6), (7,8), (9,10), (11,12), (13,14), and (15).
- ***Quad Block*** radio button - selects group of two blocks from drop-down list to reset on the DMD.
  - The DLP9000X DMD and DLP9000XUV have the following selectable quad block groups - (1-4), (5-8), (9-12), and (13-16)
  - The DLP6500 DMD has the following selectable quad block groups - (1-4), (5-8), (9-12), and (13-15)
- ***Global*** radio button - sends a reset to all blocks on the DMD at the same time.

Once a Reset type and group is selected press one of the following options:

- ***Insert*** button - inserts the command between the highlighted command and the prior command in the ***Script*** **sub-window**. If there are no commands in the ***Script*** **sub-window**, then no entry is made.
- *Add* button - adds the command as the last line in the ***Script*** **sub-window**.

5.2.3.1.3 Clear Tab

Clear DMD data commands:

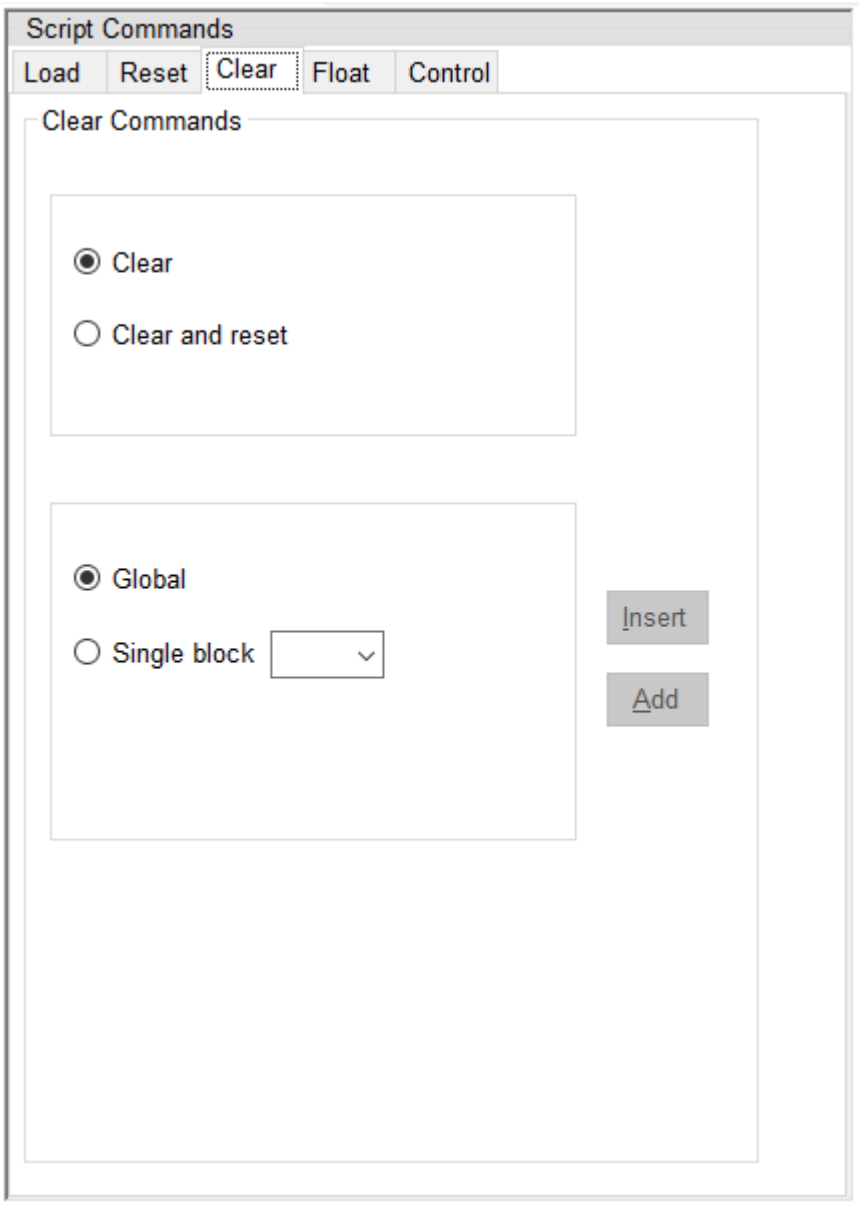

Figure 5-10. Clear Tab

Note

Clear commands can only be applied to individual blocks. If Global is selected the GUI sends the command one at a time to each available block on the DMD.

Operation Mode:

- ***Clear*** radio button - selects a clear only operation on the block scope selected.
- ***Clear and Reset*** radio button - selects a clear and reset operation on the block scope selected.

Block Scope:

- ***Global*** radio button - performs the selected operation mode on all DMD blocks.
- ***Block*** radio button - performs the selected operation mode on the specified DMD block:
  - The DLP9000X DMD and DLP9000XUV DMD have 16 selectable blocks
  - The DLP6500 DMD has 15 selectable blocks

Once an Operation Mode and Block Scope is selected press one of the following options:

- ***Insert*** button - inserts the command between the highlighted command and the prior command in the ***Script*** **sub-window**. If there are no commands in the ***Script*** **sub-window**, then no entry is made.
- *Add* button - adds the command as the last line in the ***Script*** **sub-window**.

5.2.3.1.4 Float Tab

Mirror Float Commands

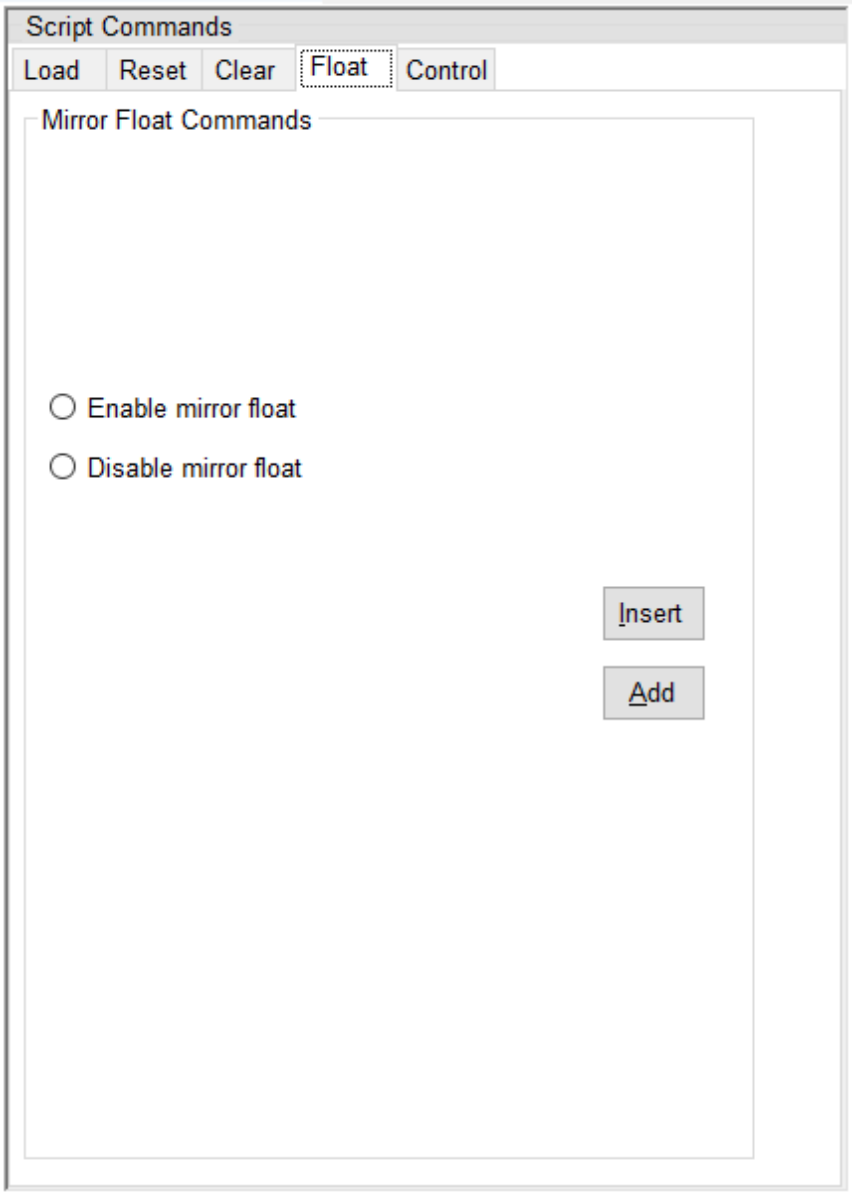

Figure 5-11. Float Tab

Note

A ***Mirror Float*** command sends a specialized reset waveform to the DMD mirrors to release the mirrors and leave them nominally flat. ***Mirror Float*** is NOT a substitute for a DMD Park (PWR_FLOAT) when preparing to shut down the system.

- ***Enable Float*** radio button - selects a float enable command to temporarily disable the DMD mirrors.
- ***Disable Float*** radio button - selects a float disable command to return to normal DMD operation.

Once the desired Float operation is selected press one of the following options:

- ***Insert*** button - inserts the command between the highlighted command and the prior command in the ***Script* sub-window**. If there are no commands in the ***Script* sub-window**, then no entry is made.
- ***Add*** button - adds the command as the last line in the ***Script* sub-window**.

5.2.3.1.5 Control Tab

Script Control Commands

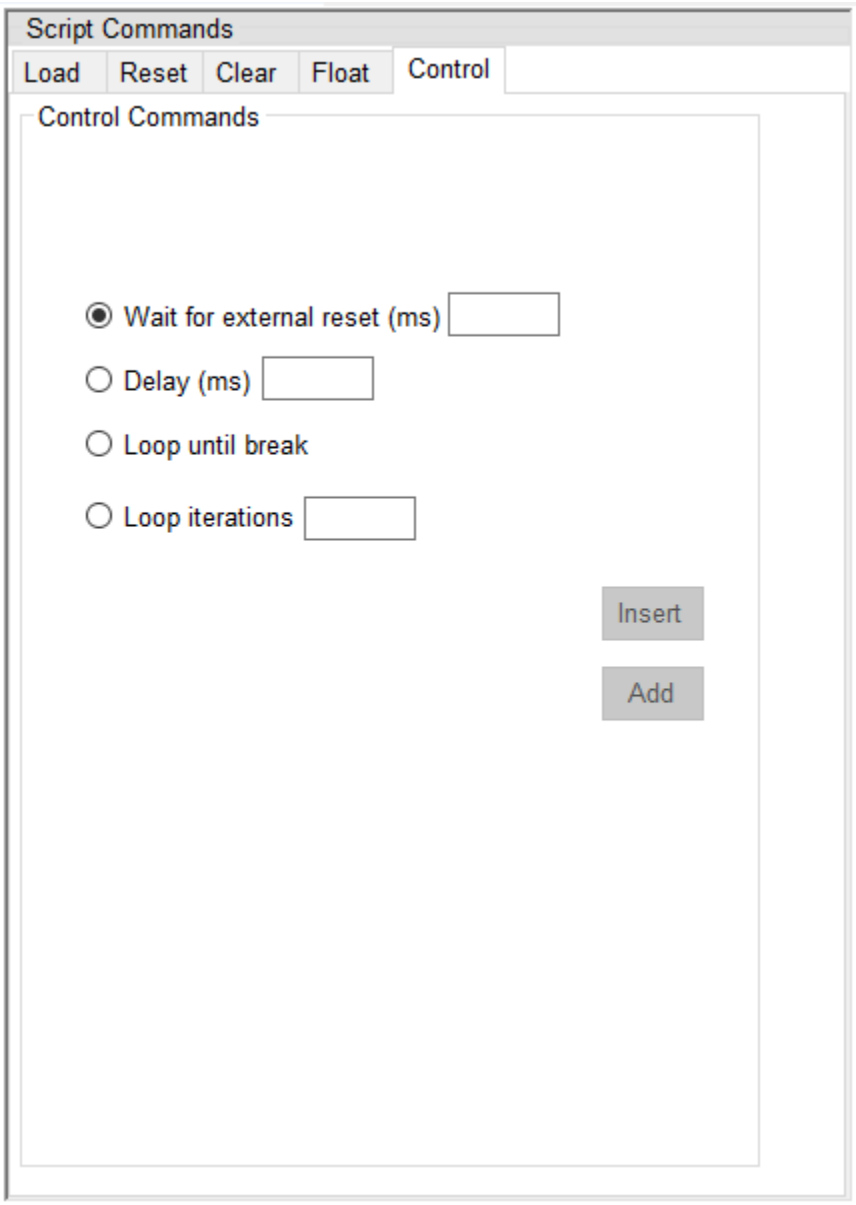

Figure 5-12. Control Tab

The following commands insert script control commands into the script:

- ***Wait for external reset (ms)*** radio button - inserts a wait in milliseconds specified time in the entry box has transpired. to wait for an external trigger input. A trigger received in the period issues a global DMD mirror clocking pulse and resume the script execution. When the specified time expires with no received trigger, the script execution resumes without issuing the reset.

Note

When a script is running this command overrides any settings in the Apps FPGA Control window.

- ***Delay (ms)*** radio button - stops execution of commands in the script until the specified time in the entry box has transpired.
- ***Loop until break*** radio button - sets a beginning label (number) and an end label (number) to repeat until the ***Break*** button (or ***STOP*** button) on the Icon Bar is pressed. Any commands between the beginning and ending label repeats indefinitely until the ***Break*** button or ***STOP*** button is pressed.
- ***Loop iterations*** radio button - sets a beginning label (number) and an end label (number) to repeat until the specified number of iterations have finished, or the ***Break*** button or ***STOP*** button on the Icon Bar is pressed.

Note

Nesting of loops is allowed regardless of type, however placing the end label of a loop inside another loop results in unpredictable behavior.

Once the desired Script Control Command is selected press one of the following options:

- ***Insert*** button - inserts the command between the highlighted command and the prior command in the ***Script*** **sub-window**. If there are no commands in the ***Script*** **sub-window**, then no entry is made.
- *Add* button - adds the command as the last line in the ***Script*** **sub-window**.

Note

Control commands must be added to the script one at a time.

5.2.3.2 Script Sub-Window

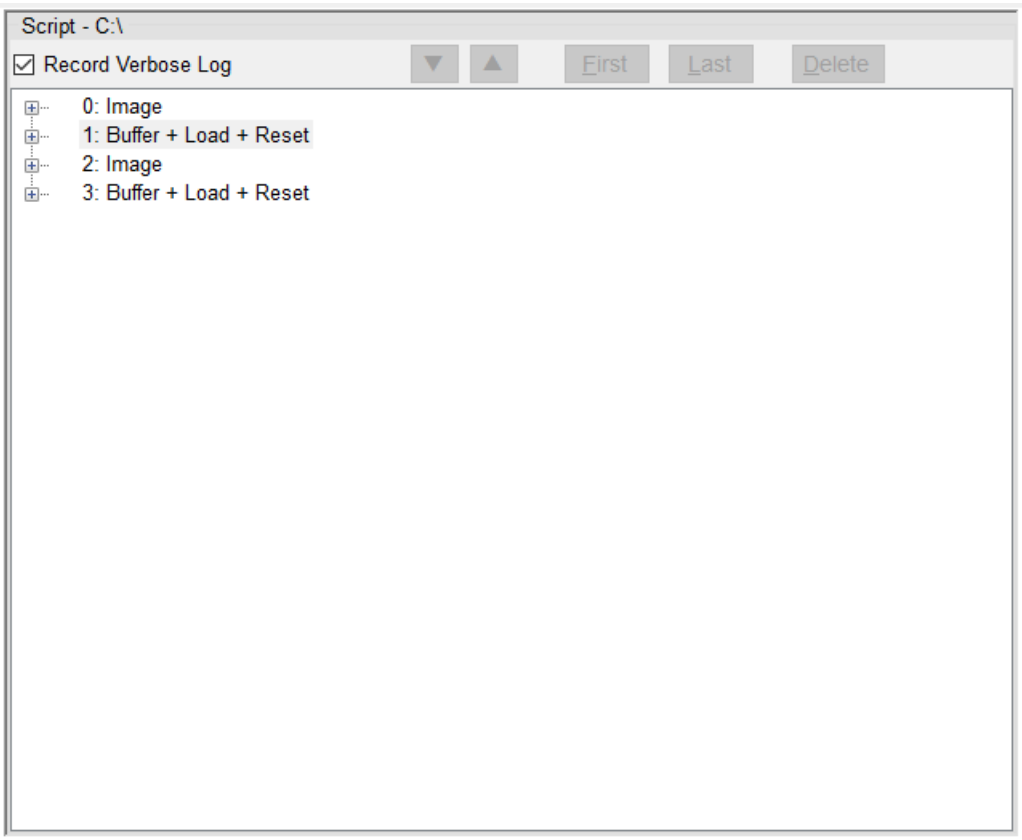

Figure 5-13. Script Sub-Window

Script sub-window - shows the Script Commands entered from the ***Script Commands*** **sub-window** tabs.

The control bar consists of:

- ***Record Verbose Log*** check box - controls the logging level of command data sent over USB and echoed in the ***Status*** **sub-window**. Verbose records all USB transactions and data. When unchecked only start, stop, break and buffering commands are echoed to improve script execution speed.
- ***Down*** button - moves the currently selected script line down one line.
- ***Up*** button - moves the currently selected script line up one line.
- ***First*** button - moves highlight to the first line of the script.
- ***Last*** button - moves highlight to the last line of the script.
- ***Delete*** button - deletes the currently highlighted script line.

Note

Save a script to a file to edit the script manually. Care must be taken to verify that the syntax and command structure are followed. Blank lines are ignored in the script.

Note

A saved script file has the version of the GUI used recorded in the first line of the script as a comment.

Note

As compiled for release, a script can contain only 64 **unique** images to prevent long command buffering time when running a script. The GUI checks for unique images when the ***Run Once*** or ***Run Continuously*** button is pressed. Images above 64 are ignored when the script is executed. This limit can be changed in the GUI source code and then recompile the GUI.

5.2.3.3 Status Sub-Window

Figure 5-14. Status sub-window

When the ***Record Verbose Log*** box is checked in the ***Script* sub-window**, the ***Status* sub-window** echoes the data being sent over USB while a script is running. When not checked only Stop, Start, Break, and Buffering commands are echoed to speed up script execution.

Note

If an image file is not found when a script is played, then the log windows shows that the file is not found, but displays the valid images found.

The current logged data can be copied and pasted into another application by selecting lines and selecting copy from the right click context menu. Use *select all* followed by *delete* to clear the log.

5.2.4 DLPC910 Registers

Selecting ***DLPC910 Control*** from the ***Control*** item on the main menu opens the ***DLPC910 Registers* window** which consist of three tabs:

5.2.4.1 Status/Control Tab

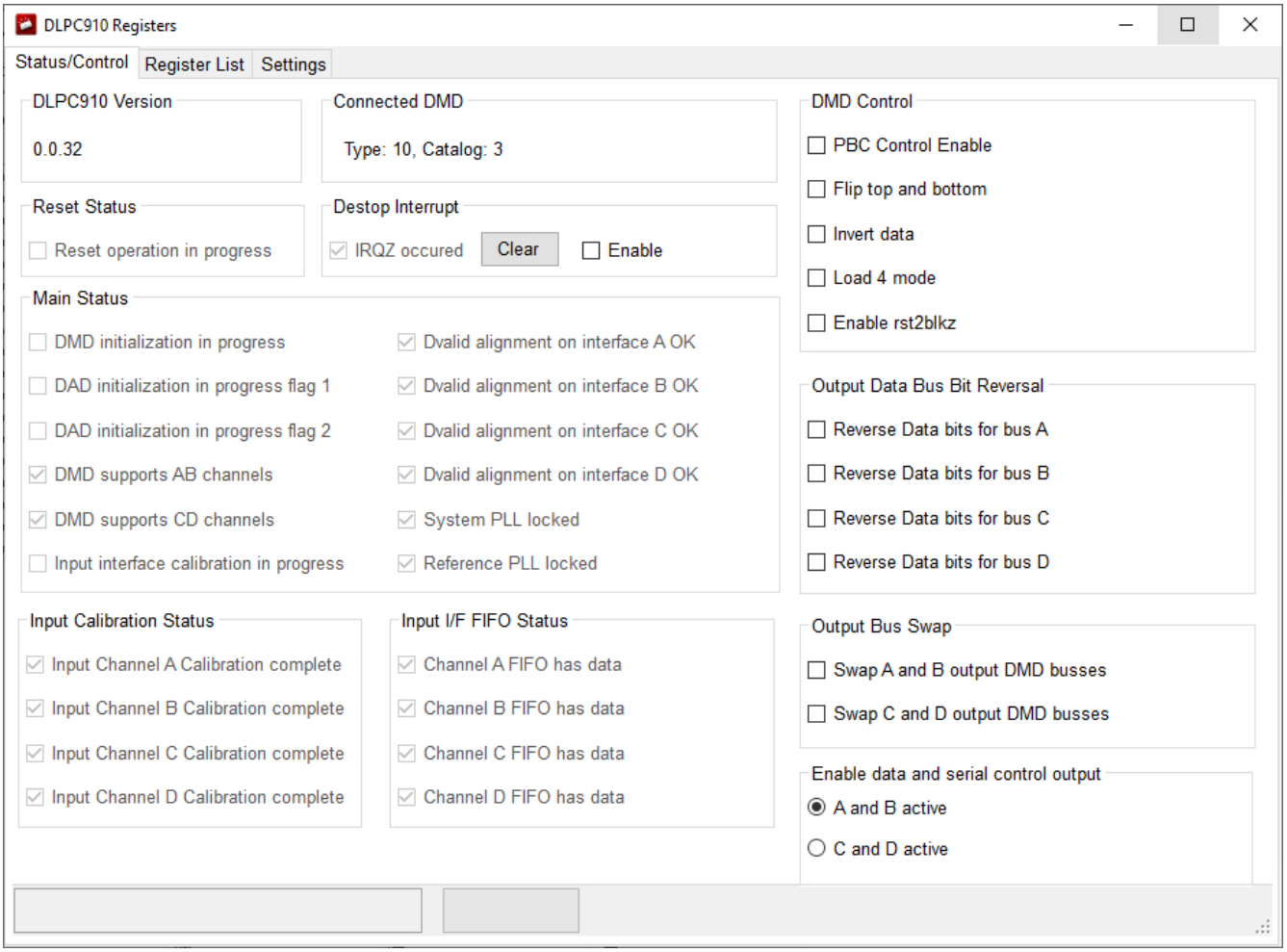

Figure 5-15. Status/Control Tab

5.2.4.1.1 *Status* Items

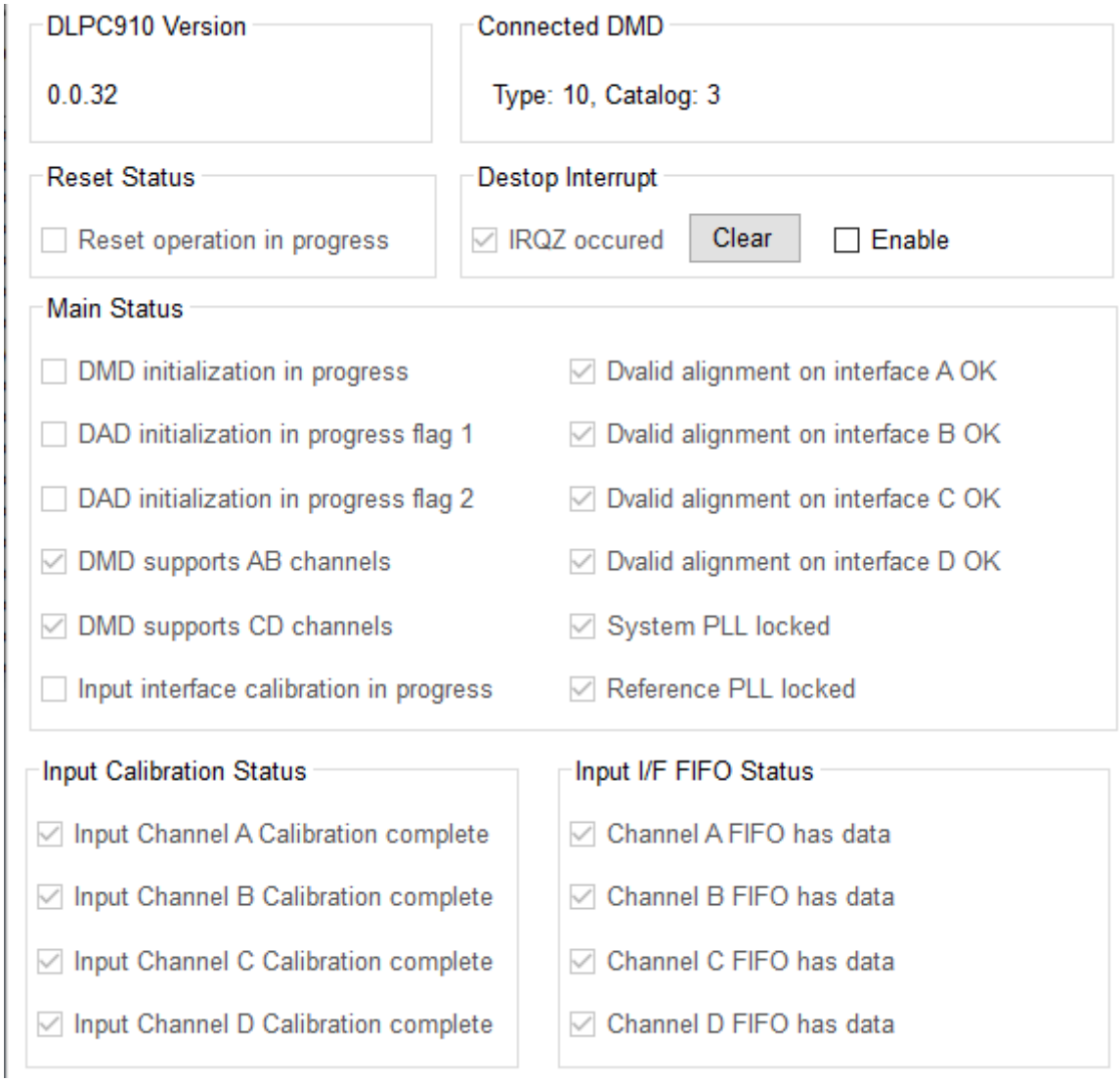

Figure 5-16. Status items

- **DLPC910 Version** - controller version (major.minor.revision).
- **Connected DMD** - connected DMD information:
  - **Type:** - DMD type number: [DLP6500 DMD = 5 ; DLP9000X DMD or DLP9000XUV DMD = 10].
  - **Catalog:** value = 3 (any other value is not a supported DMD).
- **Reset Status** - a DMD reset is in progress.
- **Destop Interrupt.**

  When checked indicates that a DMD IRQZ event occurred. The only existing source for this event is a DMD power fault indicating bias, offset, or reset power supplies have become inactive. The cause of the fault must be determined and resolved prior to a system reset to continue operation.

  This bit must be cleared after a power cycle or a reset to the DLPC910.

  - ***IRQZ*** occurred - when checked a DMD power fault occurred.
  - ***Clear*** button - clear DMD power fault.
  - ***Enable*** checkbox - enables the interrupt.
- **Main Status**
  - **DMD initialization in progress** - reading DMD information (unchecked when complete).
  - **DAD initialization in progress flag 1** - stage one reset driver initialization (unchecked when complete).

  - **DAD initialization in progress flag 2** - stage two reset driver initialization (unchecked when complete).
  - **DMD supports AB channels** - valid for DLP6500 DMD, DLP9000X DMD, and DLP9000XUV DMD.
  - **DMD supports CD channels** - valid only for DLP9000X DMD and DLP9000XUV DMD.
  - **Input interface calibration in progress** - active while the input channels are undergoing calibration (unchecked when complete).
  - **Dvalid alignment on interface A OK** - calibration and clock edge alignment of DVALID complete for channel A (checked when complete).
  - **Dvalid alignment on interface B OK** - calibration and clock edge alignment of DVALID complete for channel B (checked when complete).
  - **Dvalid alignment on interface C OK** - calibration and clock edge alignment of DVALID complete for channel C (checked when complete).
  - **Dvalid alignment on interface D OK** - calibration and clock edge alignment of DVALID complete for channel D (checked when complete).
  - **System PLL locked.**
  - **Reference PLL locked.**
- **Input Calibration Status** - these boxes are checked when each channel completes the SERDES calibration process from the training patterns from the Apps FPGA during initialization.
  - **Input Channel A calibration complete.**
  - **Input Channel B calibration complete.**
  - **Input Channel C calibration complete.**
  - **Input Channel D calibration complete.**
- **Input I/F FIFO Status** - checked when valid row data is received on the respective channel first-in first-out (FIFO) buffer.

  The **DESTOP_INFIFO_STATUS** register is used for validating there is data in the input bus FIFO buffers. When data is sent an empty FIFO buffer indicates that potentially DVALID is not properly aligned for the respective bus.

  - **Channel A FIFO has data.**
  - **Channel B FIFO has data.**
  - **Channel C FIFO has data.**
  - **Channel D FIFO has data.**

5.2.4.1.2 *DMD Control* Items

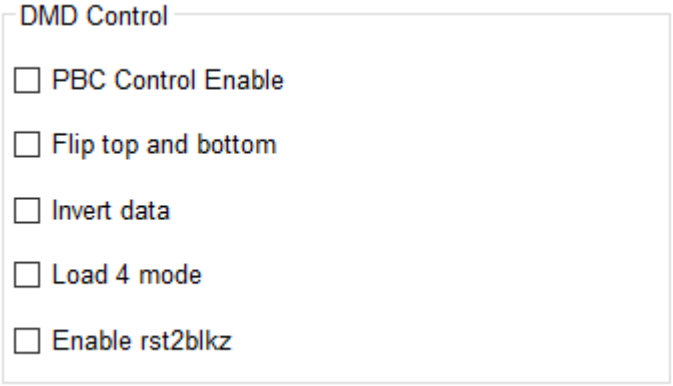

Figure 5-17. DMD Control section

- ***PBC Control Enable*** checkbox - enable software control of DMD parameters through I^2C.

> **Note**
> When not checked the software DMD Control flags are ignored and are controlled by DLPC910 input pins (default = not checked - external pin control)

  - ***Flip top and bottom*** checkbox - swaps the top of the DMD and the bottom (default = not flipped):
    - ***Zero row*** - go to beginning row becomes go to end

- ***Increment*** row mode becomes "decrement" row mode

Note

Set row addressing is not affected by this flag.

– ***Invert data*** checkbox - complements the input data [1 → 0 and 0 → 1] (default = not inverted)
– ***Load 4 mode*** checkbox - loads 4 DMD rows for each row input (default = normal load mode)
– ***Enable rst2blkz*** checkbox - sets the DMD flag to receive quad block reset requests (default = not enabled)

5.2.4.1.3 *Design* Items

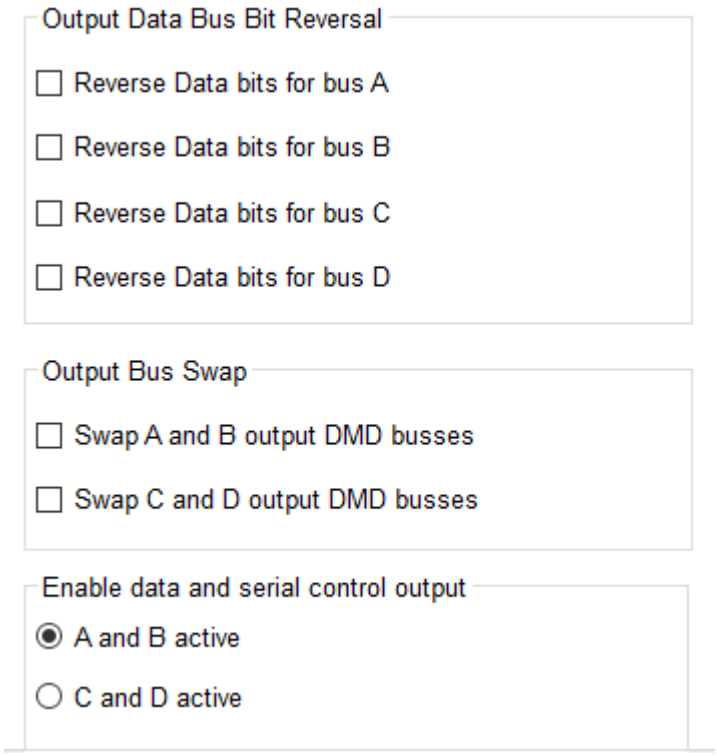

Figure 5-18. Design Items

Note

Design options are available when designing a board to assist with layout. Using the design options on the TI EVM results in unpredictable behavior.

Output Data Bus Bit reversal - reverses the data bits for the selected bus (bits [15:0] → bits [0:15]):

- ***Reverse Data bits for bus A*** checkbox - (default = not reversed)
- ***Reverse Data bits for bus B*** checkbox - (default = not reversed)
- ***Reverse Data bits for bus C*** checkbox - (default = not reversed)
- ***Reverse Data bits for bus D*** checkbox - (default = not reversed)

Output Bus Swap:

- ***Swap A and B output DMD buses*** checkbox - swaps the outputs of A with B including serial control output (default = un-swapped)
- ***Swap C and D output DMD buses*** checkbox - swaps the outputs of C with D including serial control output (default = un-swapped)

Enable data and serial control output - only available for the DLP6500FLQ DMD. Enables using the CD bus to drive a DLP6500FLQ DMD rather than the AB bus. The DLP9000X DMD and DLP9000XUV DMD ignore this setting:

- ***A and B active*** - radio button (default)
- ***C and D active*** - radio button

5.2.4.2 Register List Tab

The DLPC910 ***Register List*** **tab** shows the DLPC910 controller register list and settings for each register:

Note

Use the **USB I²C Interface** to communicate with the DLPC910 controller registers.

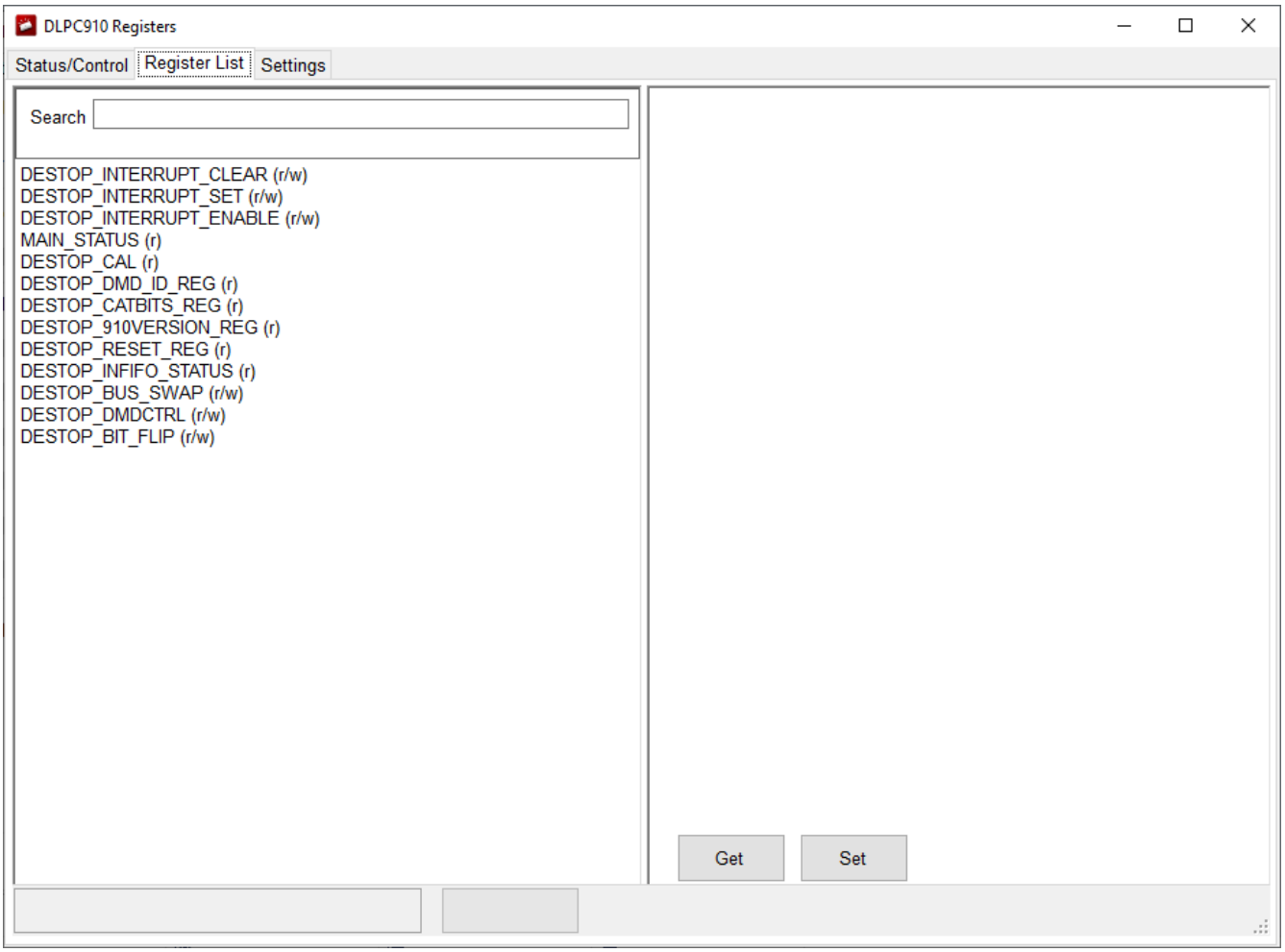

Figure 5-19. DLPC910 Register List Tab

Note

For more information see the Register Map section of the DLPC910 data sheet.

Register Definitions

The following designations are used throughout this section of the document:

- R – designates read only
- R/W – designates readable and writable

5.2.4.2.1 DESTOP_INTERRUPT_CLEAR - 0x0000

Clear DMD IRQZ

Table 5-1. DESTOP_INTERRUPT_CLEAR Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0000	2	**reset_int** 0 = no DMD IRQZ event occurred 1 = DMD IRQZ event occurred Reading provides the current interrupt status: The only existing source for this event is a DMD power fault indicating bias, offset, or reset power supplies have become inactive. The cause of the fault must be determined and resolved prior to a system reset to continue operation. **Note** The bit must be cleared after a power cycle or a reset to the DLPC910. Writing a 1 clears the interrupt bit via software.	R/W	read from firmware

5.2.4.2.2 DESTOP_INTERRUPT_SET - 0x0004

Set DMD IRQZ

Table 5-2. DESTOP_INTERRUPT_SET Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0004	2	**reset_int** 0 = no DMD IRQZ event occurred 1 = DMD IRQZ event occurred Reading provides the current interrupt status Writing a 1 asserts the interrupt bit via software	R/W	read from firmware

5.2.4.2.3 DESTOP_INTERRUPT_ENABLE - 0x0008

Enable DMD IRQZ

Table 5-3. DESTOP_INTERRUPT_ENABLE Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0008	2	**reset_int** 0 = DMD IRQ not enabled 1 = DMD IRQ enabled Writing a 1 enables the interrupt	R/W	read from firmware

5.2.4.2.4 MAIN_STATUS (DLPC910) - 0x000C

Read DLPC910 Status

Table 5-4. MAIN_STATUS Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x000C	0	**dmd_init_act_top** - DMD initialization in progress (reading DMD information) 0 = not active 1 = active	R	read from firmware
	1	**dad_init_act1** - DAD initialization stage one reset driver initialization 0 = not active 1 = active	R	read from firmware
	2	**dad_init_act2** - DAD initialization stage two reset driver initialization 0 = not active 1 = active	R	read from firmware
	3	**dmd_dev_ok_ab** - DMD supports AB channels (valid for DLP6500 DMD, DLP9000X DMD, and DLP9000XUV DMD) 0 = channels not active 1 = channels active	R	read from firmware
	4	**dmd_dev_ok_cd** - DMD supports CD channels (active only for DLP9000X DMD and DLP9000XUV DMD) 0 = channels not active 1 = channels active	R	read from firmware
	5	**calibrat_active** - input interface channel calibrations in progress 0 = not active 1 = active	R	read from firmware
	6	**dval_check_a_ok** - Dvalid calibration and alignment complete and OK on interface A 0 = not complete 1 = complete	R	read from firmware
	7	**dval_check_b_ok** - Dvalid calibration and alignment complete and OK on interface B 0 = not complete 1 = complete	R	read from firmware
	8	**dval_check_c_ok** - Dvalid calibration and alignment complete and OK on interface C 0 = not complete 1 = complete	R	read from firmware
	9	**dval_check_d_ok** - Dvalid calibration and alignment complete and OK on interface D 0 = not complete 1 = complete	R	read from firmware
	10	**sys_pll_locked** - System PLL locked 0 = not locked 1 = locked	R	read from firmware
	11	**ref_pll_locked** - Reference PLL locked 0 = not locked 1 = locked	R	read from firmware

5.2.4.2.5 DESTOP_CAL - 0x0010

Input Channel Calibration Status

Table 5-5. DESTOP_CAL Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0010	0	**cal_a_done_reg** - Input Channel A calibration complete 0 = not complete 1 = complete	R	read from firmware
	1	**cal_b_done_reg** - Input Channel B calibration complete 0 = not complete 1 = complete	R	read from firmware
	2	**cal_c_done_reg** - Input Channel C calibration complete 0 = not complete 1 = complete	R	read from firmware
	3	**cal_d_done_reg** - Input Channel D calibration complete 0 = not complete 1 = complete	R	read from firmware

5.2.4.2.6 DESTOP_DMD_ID_REG - 0x0014

Read DMD ID information

Table 5-6. DESTOP_DMD_ID_REG Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0014	3:0	**destop_dmd_id** 5 = DLP6500FLQ DMD 10 = DLP9000X DMD or DLP9000XUV DMD	R	read from firmware

5.2.4.2.7 DESTOP_CATBITS_REG - 0x0018

Verify Catalog Bits

Table 5-7. DESTOP_CATBITS_REG Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0018	3:0	**destop_dmd_catbits** 3 = Catalog DMD **Note** Any other value is not a supported DMD	R	read from firmware

5.2.4.2.8 DESTOP_910VERSION_REG - 0x001C

DLPC910 Firmware Version Information

Table 5-8. DESTOP_910VERSION_REG Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x001C	3:0	**destop_version_major** - DLPC910 FW major version number	R	read from firmware
	7:4	**destop_version_minor** - DLPC910 FW minor version number	R	read from firmware
	15:8	**destop_version_revision** - DLPC910 FW revision number	R	read from firmware

5.2.4.2.9 DESTOP_RESET_REG - 0x0020

DMD Reset in Progress Status

Table 5-9. DESTOP_RESET_REG Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0020	0	**reset_active** 0 = DMD reset not active 1 = DMD reset active Writing a 1 enables the interrupt	R	read from firmware

5.2.4.2.10 DESTOP_INFIFO_STATUS - 0x0024

FIFO Channel Data Status

Table 5-10. DESTOP_INFIFO_STATUS Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0024	0	**infifo_a_empty** - FIFO A Status 0 = FIFO has data 1 = FIFO empty	R	read from firmware
	1	**infifo_b_empty** - FIFO B Status 0 = FIFO has data 1 = FIFO empty	R	read from firmware
	2	**infifo_c_empty** - FIFO C Status 0 = FIFO has data 1 = FIFO empty	R	read from firmware
	3	**infifo_d_empty** - FIFO D Status 0 = FIFO has data 1 = FIFO empty	R	read from firmware

5.2.4.2.11 DESTOP_BUS_SWAP - 0x0028

Bus Swap and Serial Control Output Settings

Table 5-11. DESTOP_BUS_SWAP Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0028	0	**ab_busswap** - swaps the outputs of A with B including serial control output 0 = un-swapped (default) 1 = swapped	R/W	0
	1	**cd_busswap** - swaps the outputs of C with D including serial control output 0 = un-swapped (default) 1 = swapped	R/W	0
	8	**en_data_ser_out** - enable data and serial control output [0 = A and B active (default); 1= C and D active] 0 = A and B active (default) 1= C and D active **Note** Only available for the DLP6500FLQ DMD. Enables using the CD bus to drive a DLP6500FLQ DMD rather than the AB bus. The DLP9000X DMD and DLP9000XUV DMD ignore this setting.	R/W	0

5.2.4.2.12 DESTOP_DMDCTRL - 0x002C

PBC DMD Control Settings

Table 5-12. DESTOP_DMDCTRL Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x002C	0	**pbc_ctrl_en** - enable software control of DMD parameters (PBC) via DLPC910 I^2C. 0 = controlled from external pins [SW2] (default) 1 = controlled from PBC via DLPC910 I^2C	R/W	0
	1	**ns_flip** - swaps the top of the DMD and the bottom: 0 = not flipped (default) 1 = flipped **Note** This flag changes the following definitions: • ***Zero row*** - go to "beginning" row becomes go to "end" • "***Increment***" row mode becomes "decrement" row mode	R/W	0
	2	**data_comp** - complements (inverts) the input pixel data (1 → 0 and 0 → 1) 0 = not inverted (default) 1 = inverted	R/W	0
	3	**load_four** - loads 4 DMD rows for each row input 0 = active 1 = not active (default)	R/W	1
	4	**rst2blkz** - sets the DMD flag to receive quad block reset requests 0 = active 1 = not active (default)	R/W	1

5.2.4.2.13 DESTOP_BIT_FLIP - 0x0030

Reverse Input Channel Bus Bit Order Settings

Table 5-13. DESTOP_BIT_FLIP Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0030	0	**a_bitflip** - Reverses the data bits for channel A (bits [15:0] → bits [0:15]): 0 = not reversed (default); 1 = reversed	R/W	0
	1	**b_bitflip** - Reverses the data bits for channel B (bits [15:0] → bits [0:15]): 0 = not reversed (default); 1 = reversed	R/W	0
	2	**c_bitflip** - Reverses the data bits for channel D (bits [15:0] → bits [0:15]): 0 = not reversed (default); 1 = reversed	R/W	0
	3	**d_bitflip** - Reverses the data bits for channel D (bits [15:0] → bits [0:15]): 0 = not reversed (default); 1 = reversed	R/W	0

5.2.4.3 Settings Tab

The ***Settings*** tab allows an alternate I²C address to be set:

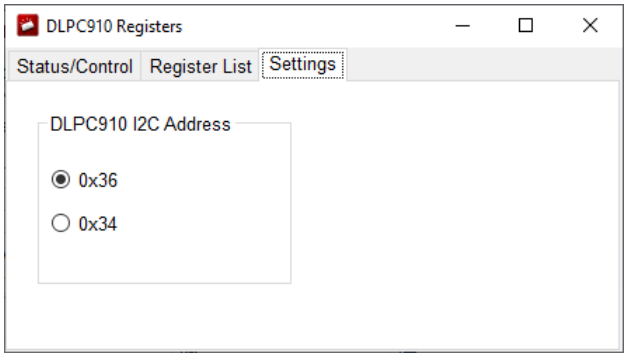

Figure 5-20. DLPC910 I²C Address Settings Tab

- The I²C available addresses:
  - ***0x36*** radio button - (default)
  - ***0x34*** radio button - alternate I²C address

Note

To communicate with the alternate I²C address jumper J10 must be populated.

5.2.5 Apps FPGA Registers

Selecting ***Apps FPGA Control*** from the ***Control*** item on the main menu opens the Apps FPGA Registers window which consist of two tabs:

5.2.5.1 Status/Control Tab

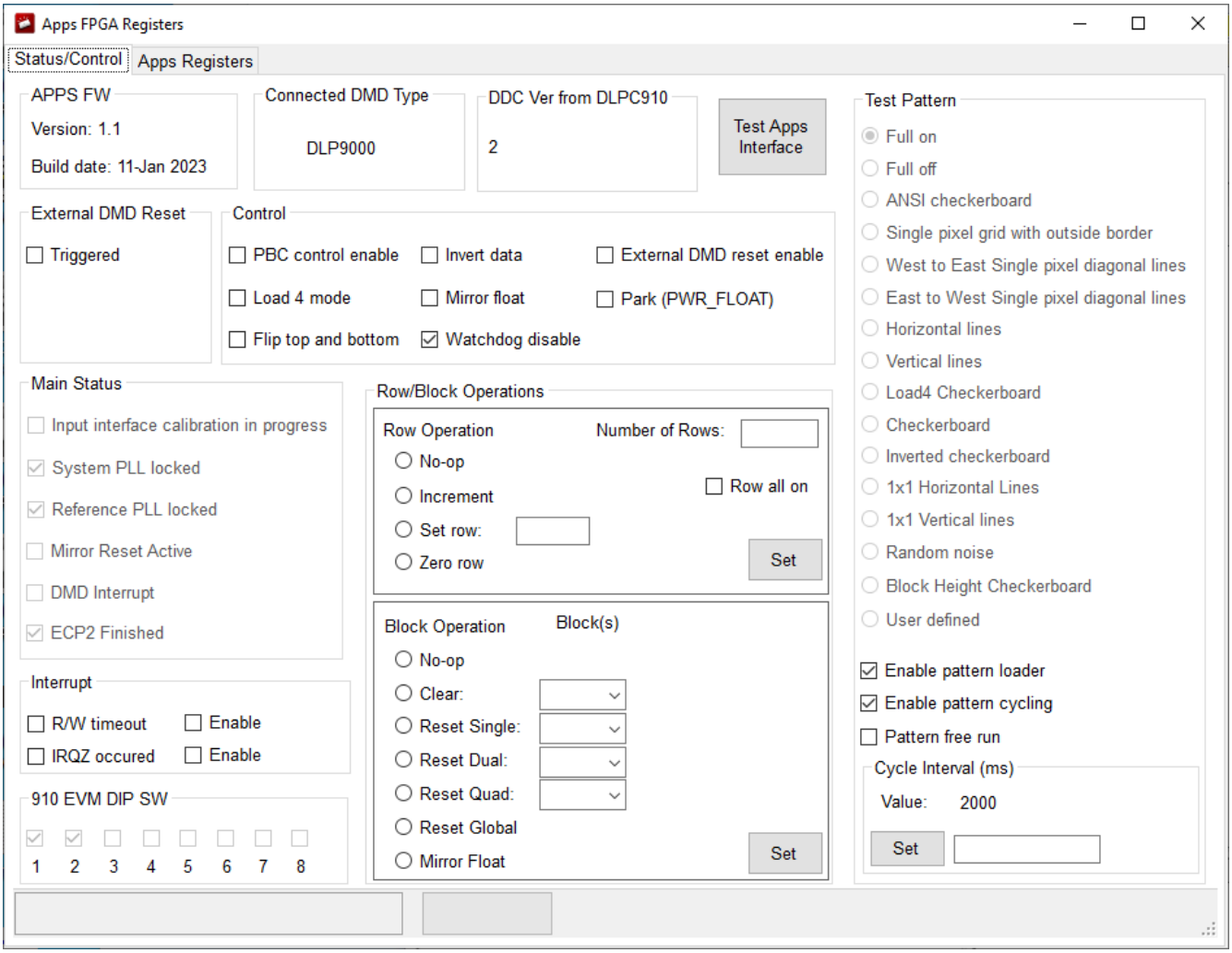

Figure 5-21. Status/Control Tab

The ***Status/Control*** **tab** is divided into the following sections:

5.2.5.1.1 *Status Items*

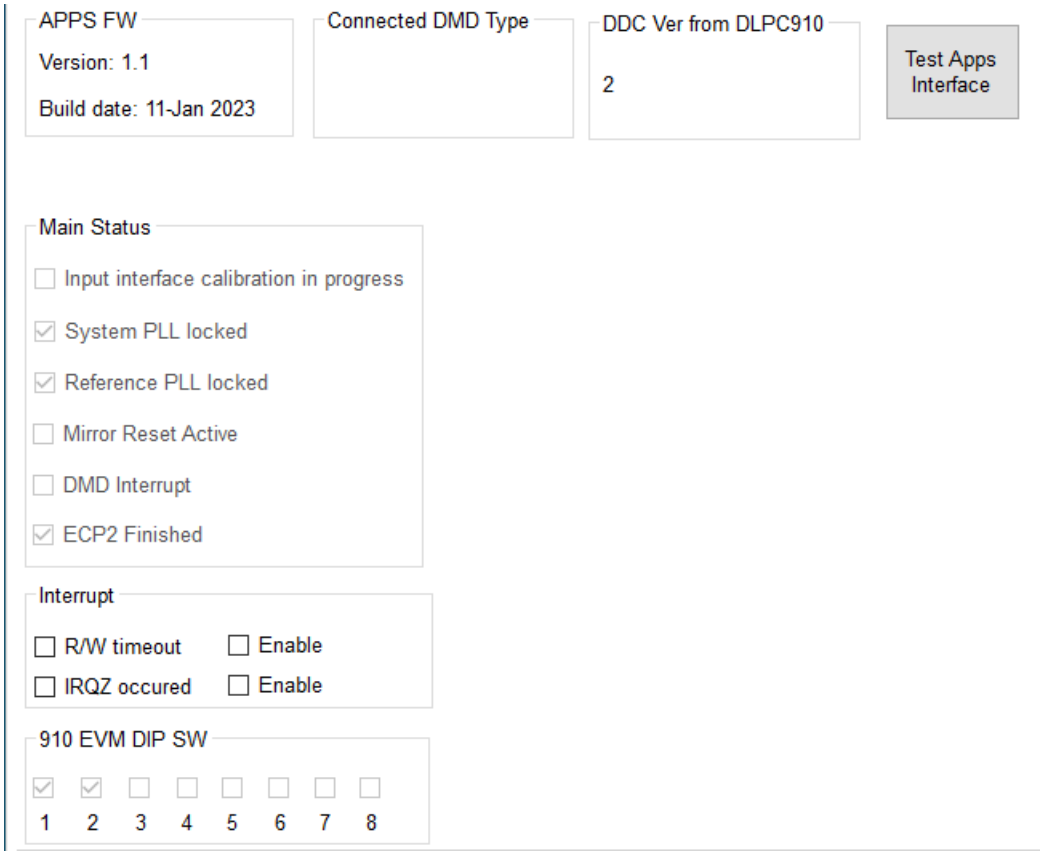

Figure 5-22. Status Items

- – **APPS FW**- Apps FPGA firmware information:
  - **Version:** *(major revision).(minor revision)* format.
  - **Build Date:** *DD-mmm-YYYY* format.
  - – **Connected DMD Type** - reports DLP6500FLQ or DLP9000X.

Note

Both the DLP9000X and DLP9000XUV report the same value.

  - – **DDC Ver from DLPC910** - reports the DLPC910 configuration firmware version.
  - – ***Test Apps Interface*** button - runs a test of the USB interface to the Apps FPGA. Opens a popup window to show the progress and pass or fail status.
  - – **Main Status**
    - ***Input interface calibration in progress*** - active while the input channels are undergoing calibration.
    - ***System PLL locked.***
    - ***Reference PLL locked.***
    - ***Mirror Reset Active*** - a DMD reset is in progress.
    - ***DMD Interrupt*** (DMD IRQZ).
    - ***ECP2 Finished*** - DLPC910 configuration complete.
  - – ***Interrupt***
    - ***R/W timeout*** - when checked the Apps FPGA timed out attempting to read write the DMD IRQZ status.
    - ***(R/W) Enable***
    - ***IRQZ occurred*** - When checked indicates that a DMD IRQZ event occurred.

Note

The only existing source for this event is a DMD power fault indicating bias, offset, or reset power supplies have become inactive. The cause of the fault must be determined and resolved prior to a system reset to continue operation.

- ***(IRQZ) Enable***

– ***910 EVM DIP SW*** - shows the logic values of the 8 positions on the DLPLCRC910EVM dip switch SW2.

Note

Positions 0 and 1 are not enabled when at logic 1 and positions 2, 3, and 7 are not enabled when at logic 0.

5.2.5.1.2 *PBC Control* Items

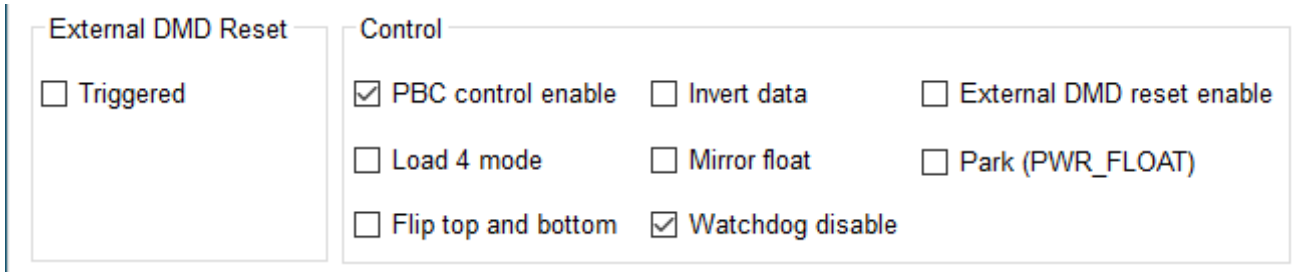

Figure 5-23. PBC Control section

- ***External DMD Reset*** checkbox - when ***PBC control enable*** and ***External DMD reset enable*** are set the *Triggered* checkbox is populated when a trigger is received. Clear to receive another trigger event.

Note

External reset does not affect the Pattern Loader when running. The status box is provided to verify that the External trigger input is working.

- ***PBC control enable*** checkbox - enable software control of DMD parameters (PBC) via Apps FPGA [not enabled (default); enabled]:

Note

When not enabled software DMD Control flags are ignored and are controlled by dip switch SW2

  – ***Load 4 mode*** checkbox - loads 4 DMD rows for each row input [active; not active (default)]
  – ***Flip top and bottom*** checkbox - swaps the top of the DMD and the bottom [not flipped (default); flipped]:
    - ***Zero row*** go to beginning row becomes go to end row
    - ***Increment*** row mode becomes decrement row mode

Note

Set row addressing is not affected by this flag.

  – ***Invert data*** checkbox - complements the input data (1 → 0 and 0 → 1), sets DMD via SPI [not inverted (default); inverted]
  – ***Float*** checkbox - sends a mirror Float to the attached DMD mirrors to release the mirrors and leave them nominally flat. ***Float*** is NOT a substitute for a DMD ***Park*** (PWR_FLOAT) when preparing to shut down the system. Return to normal operation by unchecking. [don't float (default); float mirrors]
  – ***Watchdog disable*** checkbox - Enables DMD reset watchdog in the DLPC910 controller (generates a reset request every 10 seconds when enabled) [enabled (default); not enabled]
  – ***External DMD reset enable*** checkbox - enable external trigger for DMD global reset. See Wait for external trigger [not enabled (default); enabled]

Note

The external DMD reset does not affect the Pattern Loader when running. This setting is provided to verify in the ***External DMD Reset*** status checkbox that the external trigger input is working.

- ***Park*** checkbox - parks the DMD (PWR_FLOAT) and halts the DLPC910.

Note

A power cycle is required to resume operations on the DLPLCRC910EVM after ***Park***.

5.2.5.1.3 *Row/Block Operations* Items

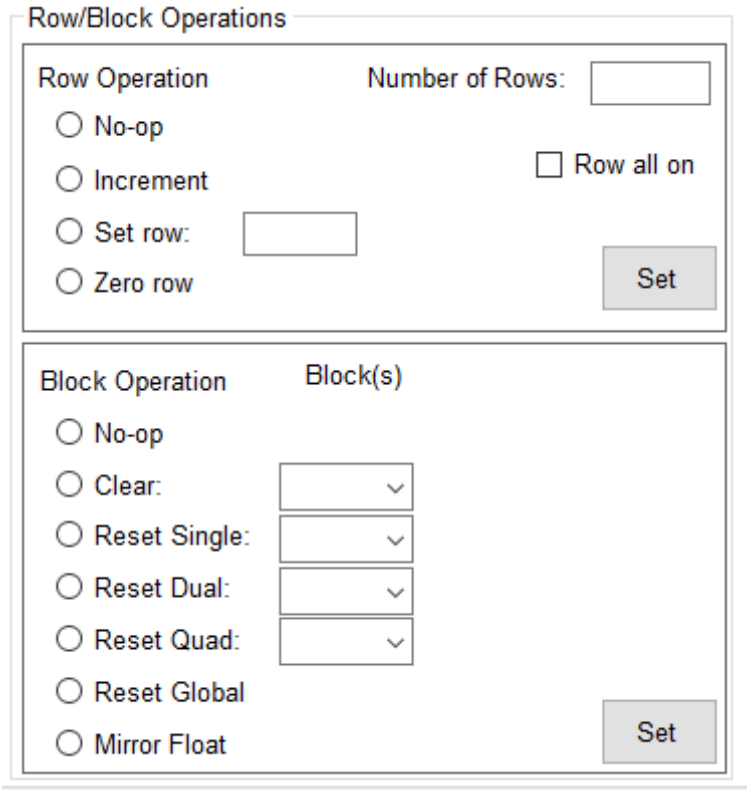

Figure 5-24. Row/Block Operations

- **Row Operation**

  Note

  – The DLP6500FLQ has 1080 addressable rows (0 - 1079)
  – The DLP9000X and DLP9000XUV have 1600 addressable rows (0 - 1599)

  Addressing any row beyond these limits is ignored.

  – ***No-op*** radio button - sends a row command with no row operation
  – ***Increment*** radio button - starting at the current row pointer address, increments the DMD row pointer and loads the data to that row. If ***Number of Rows*** is specified loads the number of rows specified.
  – ***Set row:*** radio button - Sets the row address pointer specified by the ***Row address* entry box** and loads the data to the row. If ***Number of Rows*** is specified loads the number of rows specified starting at the row specified by *Set row*.
    - ***Row address* entry box** - specifies the starting row address for ***Set row***
  – ***Zero row*** radio button - sends the row address pointer to the beginning row of the DMD. If Flip top and bottom is active, sends the row address pointer to the bottom row of the DMD.
  – ***Number of Rows:* entry box** - specifies the number of rows to load for ***Increment***, and ***Set row***.
  – ***Rows all on*** checkbox - When checked all "ones" are sent to the rows operated on by the commands in the Row operation group.

  Once the desired parameters are set press the ***Set*** button to send the operation to the Apps FPGA for execution.

- **Block Operation**
  – ***No-op*** radio button - sends a row command with no block operation

- ***Clear*** radio button
  - Dropdown selection box - selects the DMD block to clear (load "zeros"):
    - The DLP9000X DMD and DLP9000XUV DMD have 16 selectable blocks
    - The DLP6500 DMD has 15 selectable blocks
- ***Reset Single:*** radio button
  - Dropdown selection box - selects the DMD block to perform a single block reset on:
    - The DLP9000X DMD and DLP9000XUV have 16 selectable blocks
    - The DLP6500 DMD has 15 selectable blocks
- ***Reset Dual:*** radio button
  - Dropdown selection box - selects the DMD block group to perform a dual block reset on:
    - The DLP9000X DMD and DLP9000XUV have the following selectable dual block groups - (1,2), (3,4), (5,6), (7,8), (9,10), (11,12), (13,14), and (15,16).
    - The DLP6500 DMD has the following selectable dual block groups - (1,2), (3,4), (5,6), (7,8), (9,10), (11,12), (13,14), and (15).
- ***Reset Quad:*** radio button
  - Dropdown selection box - selects the DMD block group to perform a quad block reset on:
    - The DLP9000X DMD and DLP9000XUV have the following selectable quad block groups - (1-4), (5-8), (9-12), and (13-16)
    - The DLP6500 DMD has the following selectable quad block groups - (1-4), (5-8), (9-12), and (13-15)
- ***Reset Global*** radio button - sends a reset to all blocks on the DMD at the same time.
- ***Mirror Float*** radio button - sends a specialized reset waveform to the DMD mirrors to release the mirrors and leave them nominally flat.

Note

Mirror Float is NOT a substitute for a DMD ***Park*** (PWR_FLOAT) when preparing to shut down the system.

Once the desired parameters are set press the ***Set*** button to send the operation to the Apps FPGA for execution.

5.2.5.1.4 *Test Pattern* Items

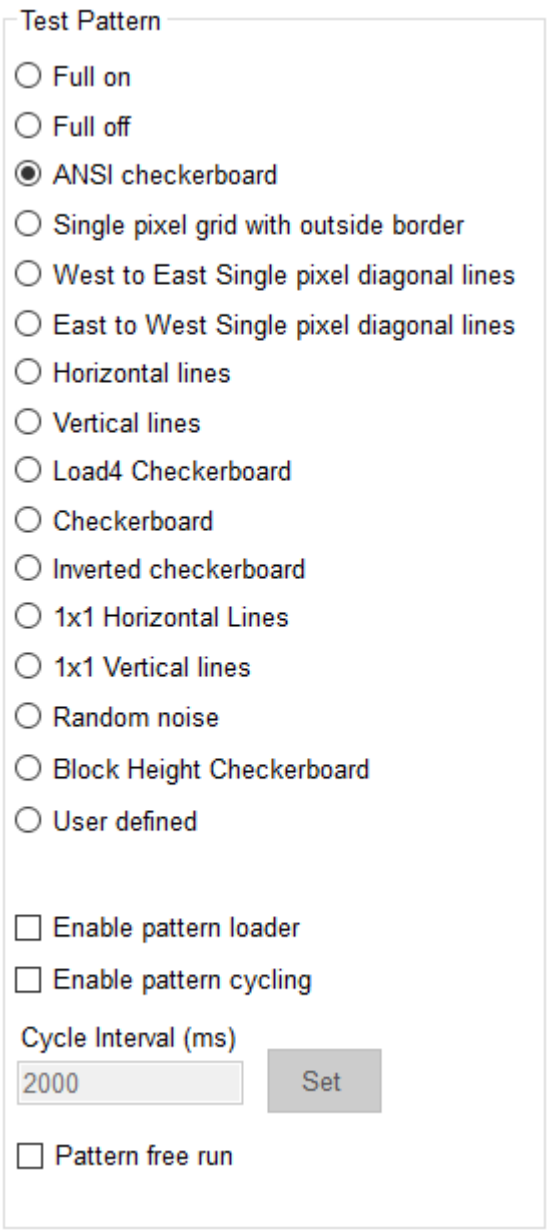

Figure 5-25. Test Pattern Items

- **Test Pattern** section:

  Test Pattern Generator (TPG) pattern list (created by Apps FPGA):

  1. **Full on** - Turns all pixels on; can be used to check for pixels stuck off.
  2. **Full off** - Turns all pixels off; can be used to check for pixels stuck on.
  3. **ANSI checkerboard pattern** - black and white checkerboard four blocks wide and four blocks tall (easy to see on DMD).
  4. **Single pixel line grid pattern with single pixel outside border** - border is on to help visualize the extent of the DMD array.
  5. **West to East Single pixel diagonal lines** - can be used to check for row data issues.
  6. **East to West Single pixel diagonal lines** - can be used to check for row data issues.
  7. **Horizontal lines** - can be used to check for issues with row loads.
  8. **Vertical lines** - can be used to check for issues with data bus lines.

9. **Load4 checkerboard** - when in normal mode the checks are normal width but ¼ height; when in load 4 mode appears the same as the small checkerboard pattern.
10. **Checkerboard** - small checkerboard (64 x 64 pixels)
11. **Inverted checkerboard** - inverted version of small checkerboard pattern.
12. **1x1 Horizontal Lines** (every row alternating black/white) - can be used to check for issues with row loads.
13. **1x1 Vertical lines** (every column alternating black/white) - can be used to check for issues with data bus lines.
14. **Random noise pattern**

Note

The random noise pattern is an active pattern that changes every load interval (APPS_LOAD_TRIG_INTERVAL Definition).

15. **Block Height Checkerboard** - checks are the height of each reset block for the attached DMD and the width of an input bus [16 bits].
16. **User defined** pattern - (loaded through the GUI Load tab).

– ***Enable pattern loader*** checkbox - loads patterns from the test pattern list.

Note

When pattern cycling is not enabled the loader shows the pattern selected from the list.

– ***Enable pattern cycling*** checkbox - cycles through the patterns from the test pattern list:
  - ***Cycle interval (ms)*** entry box - defines the time between pattern changes when pattern cycling is enabled (current GUI default is 2000 ms).

Note

Toggling the pattern loader enable while the loader is running typically results in random noise temporarily displayed on the DMD during the transition which is expected behavior.

– ***Pattern free run*** checkbox - enables the free run mode for TPG patterns. This mode loads TPG patterns back to back with no time between patterns after a pattern reset is complete.

Note

All desired parameters (PBC Control and Row and Block operations) must be set before starting free run mode. Disable free run mode before doing any other operations.

Not applicable to patterns run over USB from the Script page.

5.2.5.2 Apps Registers Tab

The ***Apps Registers*** **tab** shows the Apps FPGA register list and settings for each register:

Note

Use the **USB GPIF Interface** to communicate with the Apps FPGA registers.

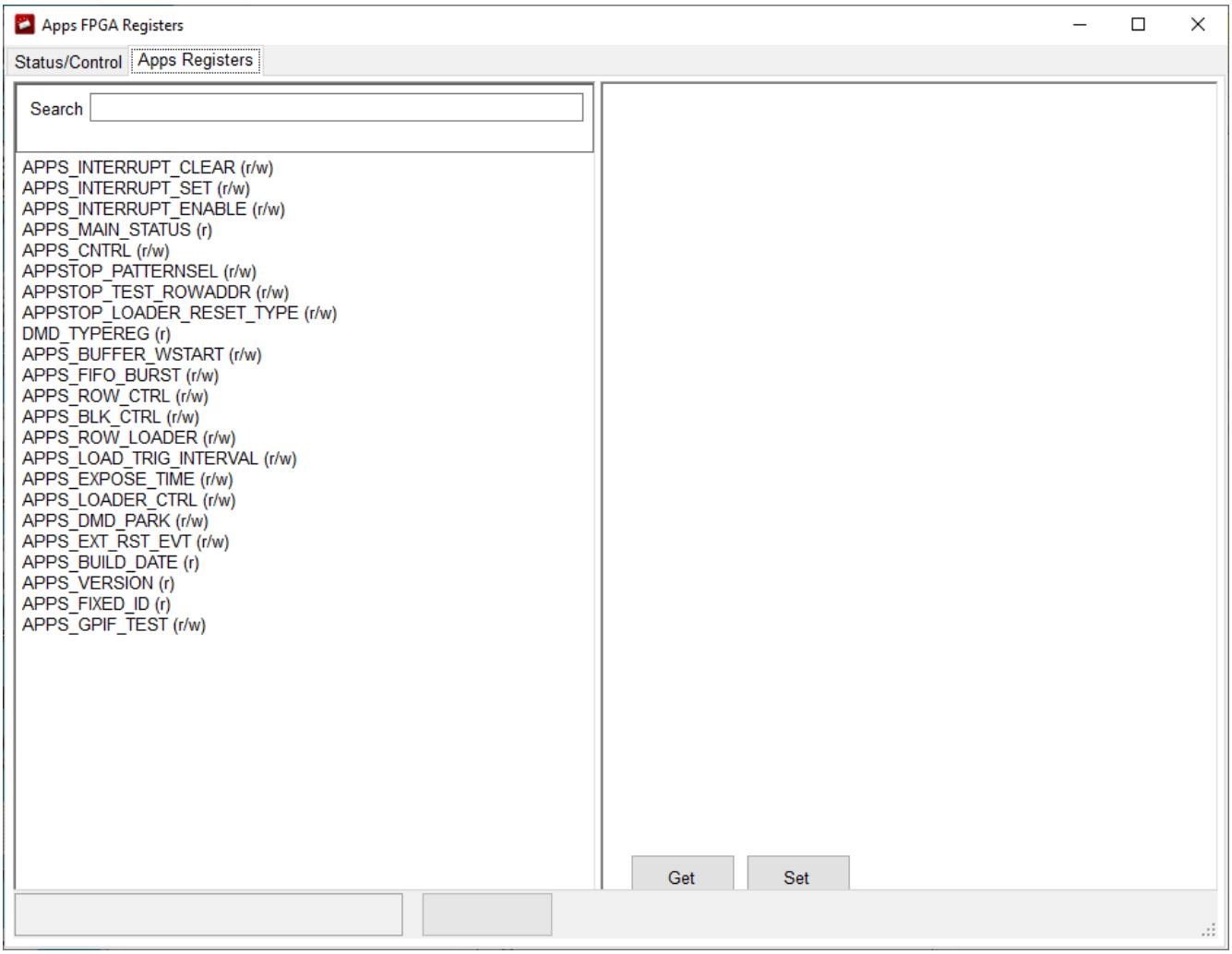

Figure 5-26. Apps Registers Tab

Register Definitions

The following designations are used throughout this section of the document:

- R – designates read only
- R/W – designates readable and writable

5.2.5.2.1 APPS_INTERRUPT_CLEAR - 0x0000

Clear DMD IRQZ

Table 5-14. APPS_INTERRUPT_CLEAR Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0000	0	**apps_vbus_fsm_timeout_a** - swaps the outputs of A with B including serial control output 0 = no timeout occurred 1 = asserted when a R/W access fails to complete in the allocated timeout duration	R/W	0
	2	**reset_int** 0 = no DMD IRQZ event occurred 1 = DMD IRQZ event occurred Reading provides the current interrupt status: The only existing source for this event is a DMD power fault indicating bias, offset, or reset power supplies have become inactive. The cause of the fault must be determined and resolved prior to a system reset to continue operation. **Note** The bit must be cleared after a power cycle or a reset to the DLPC910. Writing a 1 clears the interrupt bit via software.	R/W	read from firmware

5.2.5.2.2 APPS_INTERRUPT_SET - 0x0004

Set DMD IRQZ

Table 5-15. APPS_INTERRUPT_SET Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0004	0	**apps_vbus_fsm_timeout_a** - swaps the outputs of A with B including serial control output 0 = no timeout occurred 1 = asserted when a R/W access fails to complete in the allocated timeout duration	R/W	0
	2	**reset_int** 0 = no DMD IRQZ event occurred 1 = DMD IRQZ event occurred Reading provides the current interrupt status Writing a 1 asserts the interrupt bit via software	R/W	read from firmware

5.2.5.2.3 APPS_INTERRUPT_ENABLE - 0x0008

Enable DMD IRQZ

Table 5-16. APPS_INTERRUPT_ENABLE Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0008	0	**apps_vbus_fsm_timeout_a** - swaps the outputs of A with B including serial control output 0 = no timeout occurred 1 = asserted when a R/W access fails to complete in the allocated timeout duration	R/W	0
	2	**reset_int** 0 = DMD IRQZ not enabled 1 = DMD IRQZ enabled Reading provides the current interrupt status Writing a 1 enables the interrupt	R/W	read from firmware

5.2.5.2.4 MAIN_STATUS (Apps) - 0x000C

Apps FPGA Status

Table 5-17. MAIN_STATUS Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x000C	0	**calibrat_active** - input interfaces calibration in progress 0 = complete 1 = in progress	R	read from firmware
	1	**ecp** - ECP2 finished signal from DLPC910 0 = not complete 1 = complete	R	read from firmware
	2	**irq** - DMD IRQZ signal from DLPC910 = interrupt not active 1 = interrupt active	R	read from firmware
	3	**ract** - DMD reset active [0 = reset not active; 1 = reset active] 0 = reset not active 1 = reset active	R	read from firmware
	4	**sys_pll_lockd** - system PLL locked flag 0 = not locked 1 = locked	R	read from firmware
	5	**ref_pll_lockd** - reference PLL locked flag 0 = not locked 1 = locked	R	read from firmware

5.2.5.2.5 APPS_CNTRL - 0x0010

Apps PBC Control Settings

Table 5-18. APPS_CNTRL Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0010	0	**pbc_ctlen** - enable software control of DMD parameters (PBC) via Apps FPGA. 0 = controlled from SW2 (default) **Note** When not enabled software DMD Control flags are ignored and are controlled by dip switch SW2 1 = controlled from PBC via Apps FPGA PBC registers	R/W	0
	1	**load4** - loads 4 DMD rows for each row input [0 = active; 1 = not active (default)] 0 = not active 1 = active	R/W	1
	2	**ns_flip_en** - swaps the top of the DMD and the bottom 0 = not flipped (default) 1 = flipped **Note** This flag changes the following definitions: • ***Zero row*** - go to "beginning" row becomes go to "end" • "***Increment***" row mode becomes "decrement" row mode	R/W	0
	3	**watchdog_en** - Enables DMD reset generator timer in the DLPC910 controller 0 = enabled 1 = not enabled (default)	R/W	1
	4	**comp_data_en** - complements (inverts) the input pixel data (1 → 0 and 0 → 1), sets DMD via SPI 0 = not inverted (default) 1 = inverted	R/W	0
	7	**float** - sends a specialized reset waveform to the DMD mirrors to release the mirrors and leaves them nominally flat. 0 = do not float (default) 1 = float mirrors **Note** **float** is NOT a substitute for a DMD ***Park*** when preparing to shut down the system. Return to normal operation by setting to 0.	R/W	0
	8	**etrg** - enable external trigger for DMD global reset. See Wait for external trigger 0 = not active (default) 1 = active	R/W	0

5.2.5.2.6 APPSTOP_PATTERNSEL - 0x0014

Apps Loader Pattern Selection and Pattern Cycle Interval

Table 5-19. APPSTOP_PATTERNSEL Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0014	7:0	**pattern_sel** - selects the test pattern to display in test pattern generator mode: • **0000** - full on pattern • **0001** - full off pattern • **0010** - ANSI checkerboard • **0011** - single pixel line grid pattern with single pixel outside border • **0100** - West to East Single pixel diagonal lines • **0101** - East to West Single pixel diagonal lines • **0110** - horizontal lines • **0111** - vertical lines • **1000** - load4 checkerboard (when in normal mode the checks are normal width (64 pixels) but ¼ height; when in load 4 mode appears the same as the checkerboard pattern) • **1001** - 64 x 64 pixel checkerboard • **1010** - inverted checkerboard (inverted version of checkerboard pattern) • **1011** - 1x1 horizontal lines (every row alternating black/white) • **1100** - 1x1 vertical lines (every column alternating black/white) • **1101** - random noise pattern **Note** The random noise pattern is an active pattern that changes every load interval (APPS_LOAD_TRIG_INTERVAL Definition). • **1110** - block height and bus width checkerboard (checks are the height of each reset block for the attached DMD and the width of an input bus [16 bits]) • **1111** - user defined pattern (loaded through the GUI Load tab)	R/W	0 (full on)
	8	**cen** - enables cycling through all patterns when in test pattern generator mode and the pattern loader is enabled	R/W	1 (at startup)
	31:12	**tpg_cycle_interval** - defines the pattern cycle display interval in ms when in pattern cycling mode	R/W	[currently 2000]

5.2.5.2.7 APPSTOP_TEST_ROWADDR - 0x0018

Set Test Row Address

Table 5-20. APPSTOP_TEST_ROWADDR Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0018	10:0	**test_rowaddr** - sets the row address to be loaded with ones: DLP6500FLQ (0 - 1079) DLP9000X and DLP9000XUV (0 - 1599) **Note** Requires that row address mode be active.	R/W	0 read from firmware at startup

5.2.5.2.8 APPSTOP_LOADER_RESET_TYPE - 0x001C

Set TPG Reset Type

CAUTION
The loader must be disabled using APPS_LOADER_CTRL Definition **enable loader** before changing from one reset type to another and re-enable afterward.

Table 5-21. APPSTOP_LOADER_RESET_TYPE Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x001C	3:0	**rst_type** - sets the type of reset operation for the TPG: • 0000b - Single block phased • 0001b - Dual block phased • 0010b - Global • 0011b - Quad block phased	R/W	0010b - Global

5.2.5.2.9 DMD_TYPEREG - 0x0020

DMD Type, DLPC910 FW Version, and SW2 Information

Table 5-22. DMD_TYPEREG Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x00020	3:0	**appstop_dmd_typereg** - DMD type: 0000b = Unsupported DMD or DMD not connected 1110b = DLP6500FLQ 1111b = DLP9000X or DLP9000XUV **Note** Any other value is invalid	R	read from firmware
	6:4	**ddc_ver** - DLPC910 controller firmware version	R	read from firmware
	31:24	**evm_dlpsw (bits 31:24)** - dip switch SW2 logic values	R	read from firmware [default production setting is 3]

5.2.5.2.10 APPS_BUFFER_WSTART - 0x0024

DMD Type, DLPC910 FW Version, and SW2 Information

Table 5-23. APPS_BUFFER_WSTART Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x00024	10:0	**buf_wstart_numrows** - number of rows of pixel data to accept and write over USB/GPIF FIFO into the frame buffer	R/W	0 at startup
	31:16	**buf_wstart_row** - starting row write address for placing first 16 bit word from USB/GPIF FIFO into the frame buffer	R/W	0 at startup

5.2.5.2.11 APPS_FIFO_BURST - 0x0028

GPIF FIFO Burst Write Size

Table 5-24. APPS_FIFO_BURST Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0028	9:0	**fifo_burst_size** - size of the general purpose interface (GPIF) FIFO burst write	R/W	N/A

5.2.5.2.12 APPS_ROW_CTRL - 0x002C

Row Mode and Row Address Controls

Table 5-25. APPS_ROW_CTRL Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x002C	1:0	**rowmd** - sets the DMD row mode in the DLPC910	R/W	0 at startup
	14:4	**rowad** - sets the row address in the DLPC910	R/W	0 at startup
	26:16	**numrows** - sets the number of rows to send from the buffer to the DLPC910 to load to the attached DMD	R/W	0 at startup
	28	**fill_1s** - fill the number of rows in **numrows** with ones instead of data from the buffer	R/W	0 at startup

5.2.5.2.13 APPS_BLK_CTRL - 0x0030

Block Mode and Block Address Control

Table 5-26. APPS_BLK_CTRL Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0030	1:0	**blkmd** - sets the DMD reset block mode in the DLPC910	R/W	0 at startup
	7:4	**blkad** - sets the DMD reset block address in the DLPC910	R/W	0 at startup
	8	**rst2blkz** - sets the DMD flag to receive quad block reset requests	R/W	0 at startup

5.2.5.2.14 APPS_ROW_LOADER - 0x0034

Row Loader Control

Table 5-27. APPS_ROW_LOADER Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0034	10:0	**load_rows** - sets how many rows to load. The loader loops to read the test pattern buffer starting at row zero and sends the rows to the DLPC910 to load to the attached DMD	R/W	N/A
	26:16	**start_row** - starting row on the DMD to load a pattern. The loader loops starting at zero until the start row specified and then load the number of rows specified	R/W	N/A

5.2.5.2.15 APPS_LOAD_TRIG_INTERVAL - 0x0038

Interval Between Pattern Loads

Table 5-28. APPS_LOAD_TRIG_INTERVAL Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0038	9:0	**load_interval** - sets the load trigger interval for the pattern loader in µs. When a pattern is displayed in the test pattern generator data is refreshed at the trigger interval. 400 µs (default) 50 µs recommended minimum - for max run speed please see APPS_LOADER_CTRL Definition **free run**.	R/W	400 µs

5.2.5.2.16 APPS_EXPOSE_TIME - 0x003C

Pattern Exposure Time

Table 5-29. APPS_EXPOSE_TIME Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x003C	15:0	**expose_time_count** - adds additional time in µs for exposure after a complete pattern is loaded(1)	R/W	0x0000

(1) When a trigger occurs, the Loader sends the pattern buffer to the DMD and performs a reset to display the pattern. Expose time is wait time added after the reset is complete before the Loader waits for the next trigger. Expose time is measured in row cycle counts:

- For DLP9000X and DLP9000XUV DMDs, row cycles are 20 dclk cycles long at 400 MHz or 480 MHz (50 ns or 41.67 ns).
- For DLP65000 DMDs, row cycles are 32 dclk cycles long at 400 MHz (80 ns).

For example, with the default *Load Interval* of 400 us, no change is seen in the pattern load frequency until the total of load time plus reset time plus expose time exceeds an integer multiple of 400 us. Therefore, the effective step size is the **APPS_LOAD_TRIG_INTERVAL** - 0x0038.

5.2.5.2.17 APPS_LOADER_CTRL - 0x0040

Loader Control Settings

Table 5-30. APPS_LOADER_CTRL Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0040	0	**enable_loader** - enables the pattern loader 0 = not enabled 1 = enabled (default on startup)	R/W	1 (at startup)
	1	**free_run** - enables the TPG free run mode. This mode loads TPG patterns back to back with no time between patterns after a reset is complete. 0 = not enabled (default on startup) 1 = enabled **Note** All desired parameters must be set before starting free run mode. Disable free run mode before doing any other operations. Not applicable to patterns run from the script window.	R/W	0 (at startup)

5.2.5.2.18 APPS_DMD_PARK - 0x0044

DMD Park (PWR_FLOAT) Operation

Table 5-31. APPS_DMD_PARK Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0044	0	**dmd_park** (PWR_FLOAT) - writing 1 parks the DMD and halts the DLPC910 **Note** Power cycle or a DLPC910 logic reset is required to resume operations on the DLPLCRC910EVM. Setting this back to 1 after a DMD Park performs a logic reset on the DLPC910.	R/W	0

5.2.5.2.19 APPS_EXT_RST_EVT - 0x0048

External Global Reset Event

Table 5-32. APPS_EXT_RST_EVT Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0048	0	**trgd** - DLPC910 sets to 1 when an external global reset is completed 0 = (default) 1 = a global reset event occurred **Note** After an event is detected reset the register to 0 to detect the next event.	R/W	0

5.2.5.2.20 APPS_BUILD_DATE - 0x0080

Date of Apps FPGA Code Build

Table 5-33. APPS_BUILD_DATE Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0080	3:0	**d0** - day digit 0	R	read from firmware
	7:4	**d1** - day digit 1	R	read from firmware
	11:8	**m0** - month digit 0	R	read from firmware
	15:12	**m1** - month digit 1	R	read from firmware
	19:16	**y0** - year digit 0	R	read from firmware
	23:20	**y1** - year digit 1	R	read from firmware
	27:24	**y2** - year digit 2	R	read from firmware
	31:28	**y3** - year digit 3	R	read from firmware

5.2.5.2.21 APPS_VERSION - 0x0084

Apps FPGA Build Version

Table 5-34. APPS_VERSION Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x00084	7:0	**minor_rev** - Apps FPGA minor revision number	R	read from firmware
	15:8	**major_rev** - Apps FPGA major revision number	R	read from firmware

5.2.5.2.22 APPS_FIXED_ID - 0x0088

Apps FPGA ID Number

Table 5-35. APPS_FIXED_ID Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x0088	31:0	**id** - Apps FPGA ID fixed at 0x000AC910	R	0x000AC910

5.2.5.2.23 APPS_GPIF_TEST - 0x008C

Apps FPGA GPIF Register Test

Table 5-36. APPS_GPIF_TEST Definition

ADDRESS	BITS	DESCRIPTION	TYPE	DEFAULT
0x008C	31:0	**test** - GPIF test register used by ***Test Apps Interface*** (set to 0x00000000 at startup - register has no functionality)	R	0x00000000

5.3 JTAG Flash Programming

The SPI Flash can be programmed over the JTAG interface using a USB-JTAG cable supported by AMD Xilinx ISE Impact Tool. The procedure has been tested with ISE Impact Tool version 14.1 (32 bit) with a Digilent® JTAG-HS2 programmer.

Note

Use of other ISE Impact Tool versions have resulted in the SPI Flash programming incorrectly.

Please contact AMD Xilinx for support with other programming platform cables.

The DLPC910 SPI Flash MCS file to use in this procedure is found here: DLPR910

1. Open up the Impact application.
2. Power on the DLPLCRC910EVM and connect the JTAG-HS2 programming cable to J17 DLPLCRC910EVM Connectors (Top View) and then to the PC that you have the IMPACT Tool installed on.

Note

Do not connect the AMD Xilinx VC-707 board.

3. Once the program is open, select either to start a new project
4. Select *Configure device using Boundary-Scan (JTAG)* which initializes the JTAG chain.
5. The IMPACT Tool prompts to assign a SPI/BPI PROM to the device. Select *Yes* to attach a SPI PROM to the Controller.

Note

Only .mcs files are able to be assigned to the SPI PROM; anything else results in an error.

6. Select *SPI PROM* and *S25FL032P* with a data width of *1* and press OK.
7. Select *Yes* to ignore the data width warning.
8. To program the device through IMPACT Tool, right-click on the *FLASH* and click *Program*. User can also select *Program* under *Impact Processes* on the bottom left of the IMPACT Tool.
9. The controller programs and reports *Program Succeeded* in the IMPACT Tool.
10. Power down the DLPLCRC910EVM and remove the JTAG-HS2 programmer.

5.4 SPI Flash Programming

The DLPC910 SPI Flash HEX file to use in this procedure is found here: DLPR910

1. To program the DLPC910 controller code into the attached SPI Flash memory via a SPI programmer the following resistors need to be temporarily removed to program the SPI Flash memory:
   - R126
   - R131
   - R132
   - R133

Note

A suggested method to *remove* these resistors is to solder them to the pad at one end or the other so that the resistors are not in the circuit, but do not get lost.

2. Connect a SPI programming cable to the SPI Programming Connector J18
3. Power up the DLPLCRC910EVM board and program the SPI Flash memory with the *.hex file using your programming software:
   a. Select the S25FL032 SPI Flash Device in your programming software
   b. Select the *.hex file in your programming software
   c. Program and verify the SPI program
4. Power down the DLPLCRC910EVM and replace the resistors removed from the circuit in step 1.
5. Power up the board and verify that the board is configuring and working correctly.

5.5 AMD Xilinx VC-707 Configuration PROM Programming

Use the following steps to program the MCS file into the VC-707 board PROM. The PROM file to use in this procedure is found here: DLPLCRC910EVM

Steps:

1. Start with the VC-707 board disconnected from the DLPLCRC910EVM board
2. Power up the VC-707 board
3. Connect to USB-JTAG port on VC-707 board shown in VC-707 USB-JTAG Port.

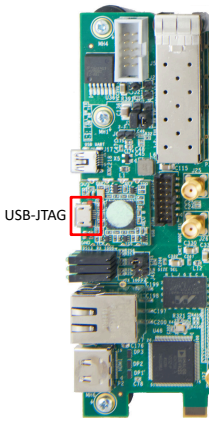

Figure 5-27. VC-707 USB-JTAG Port

4. Start Vivado Lab Edition
5. Select *Open Target* and choose *AutoConnect*
6. Add configuration Memory Device - Search for "mt28gu01gaax1e-bpi-x16"
7. Choose *Program to Device*
8. Select the VC-707 PROM file from the disk
9. Choose Program with verify (NOTE: RS Pins 25:24)
10. Power off the VC-707 board

11. Remove USB cable from USB-JTAG port

5.6 USB Firmware Programming

To update the USB firmware in the USB receiver on the DLPLCRC910EVM requires the following:

- **EZ-USB™ FX3 SDK** version 1.3.4 from Infineon. The update was tested with version 1.3.4 - Contact Infineon for support.
- A new DLPC910 USB Firmware *.iic file.

Programming Steps:

1. Start with the DLPLCRC910EVM board disconnected from the VC-707 board.
2. Install a jumper on J5.
3. Power up the DLPLCRC910EVM board.
4. Connect the PC to USB connector (J1) on the DLPLCRC910EVM.
5. Start Infineon EZ-USB FX3 SDK (USB Control Center Window) which shows **Cypress FX2LP No EEPROM Device.**:

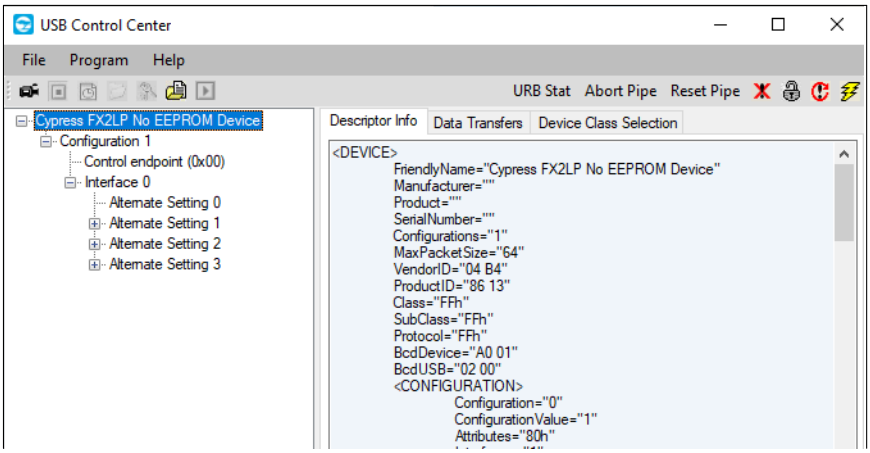

Figure 5-28. USB Control Center Window

6. Without powering off the board, carefully remove the jumper on J5.
7. Select *Program* from the menu bar.
8. Choose FX2/64KB EEPROM from the drop-down menu:

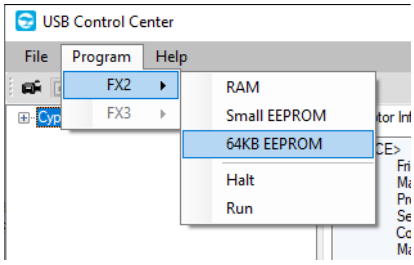

Figure 5-29. FX2/64KB EEPROM

9. In the *Select file to download . . .* dialog box, navigate to and select the new FW file and press *Open* (for example, `DLPC910_CY7C68013A_FW_v[n.nnn.nnn].iic`)

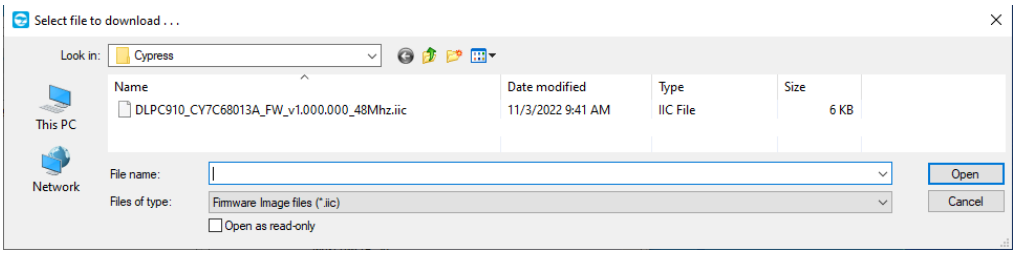

Figure 5-30. Select File to Download Dialog

10. Programming is immediate and reports *Programming succeeded* in the lower left corner of the USB Control Center window.
11. Power down the DLPLCRC910EVM board.
12. Reconnect the DLPLCRC910EVM to the VC-707 board and restart the system.
13. Start the DLPC910 GUI.
14. Select *Help/About* from the GUI menu to verify the USB firmware version.

6 Connectors

This chapter describes the connector pins of the DLP LightCrafter DLPC910 EVM.

6.1 J1 - USB - Micro B USB 2.0 Connector

The micro B USB 2.0 receptacle connector J1 pins are shown in J1 - USB - Micro B USB 2.0 Connector.

Table 6-1. Micro B USB 2.0 Receptacle Connector Pins

Description	Pin	Supply Range
VBUS	1	5.0 V
DMINUS	2	5.0 V
DPLUS	3	5.0 V
NC	4	0 V
Ground	5	0 V
Ground	6	0 V
Ground	7	0 V
Ground	8	0 V
Ground	9	0 V

6.2 J2 - DLPC910 I^{2}C Connector

The I^{2}C_1 connector J2 pins are shown in Table 6-2 (see note). Two matching four-pin, 1.25-mm connector part numbers are:

- Molex part number: 51021-0400
- Digi-Key part number: WM1722-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 50079-8100
- Digi-Key part number: WM2023-ND

Table 6-2. I^{2}C Connector Pins

Description	Pin	Supply Range
I^{2}C SCL	1	3.3 V
I^{2}C SDA	2	3.3 V
3.3 V supply	3	3.3 V
Ground	4	0 V

6.3 J4 - PMBUS (I^{2}C) Connector

The PMBUS (I^{2}C) connector J4 pins are shown in Table 6-3. Two matching four-pin, 1.25-mm connector part numbers are:

- Molex part number: 51021-0400
- Digi-Key part number: WM1722-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 50079-8100
- Digi-Key part number: WM2023-ND

Table 6-3. PMBUS (I^{2}C) Connector Pins

Description	Pin	Supply Range
I^{2}C SCL	1	3.3 V
I^{2}C SDA	2	3.3 V
3.3 V supply	3	3.3 V

Table 6-3. PMBUS (I^2C) Connector Pins (continued)

Description	Pin	Supply Range
Ground	4	0 V

6.4 J6 - USB GPIO Connector

The USB GPIO connector J6 pins are shown in USB GPIO Connector Pins(see note). Two matching eight-pin, 1.25-mm connector part numbers are:

- Molex part number: 51021-1000
- Digi-Key part number: WM1728-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 50079-8100
- Digi-Key part number: WM2023-ND

Table 6-4. USB GPIO Connector Pins

Description	Pin	Supply Range
Ground	1	0 V
USB GPIO B7	2	3.3 V
USB GPIO B6	3	3.3 V
USB GPIO B5	4	3.3 V
USB GPIO B4	5	3.3 V
USB GPIO B3	6	3.3 V
USB GPIO B2	7	3.3 V
USB GPIO B1	8	3.3 V
USB GPIO B0	9	3.3 V
Ground	10	0 V

6.5 J8 - 400 Position FMC Connector (Female)

The 400 position FMC female connector J8. Mating plug part numbers are:

- Samtec part number: ASP-134488-01 or ASP-134602-01
- Digi-Key part number: SAM8730-ND or 612-ASP-134602-01CT-ND

6.6 J14 - Power (Alternate)

The alternate power connector J14 pins on the DLPLCRC910EVM are shown in Alternate Power Connector Pins. Two matching connector part numbers are:

- Molex part number: 0039012060
- Digi-Key part number: WM3702-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 0039000186
- Digi-Key part number: WM18517-ND

Table 6-5. Alternate Power Connector Pins

Description	Pin	Supply Range
Ground	1	0 V
Ground	2	0 V
Ground	3	0 V
Input Supply	4	12-V DC –5%/+10%
Input Supply	5	12-V DC –5%/+10%
Input Supply	6	12-V DC –5%/+10%

6.7 J15 - Power

The power socket J15 pins on the DLPLCRC910EVM are shown in Table 6-6. Two matching connector part numbers are:

- Switchcraft part number: 760
- Digi-Key part number: SC1051-ND

Table 6-6. Power Connector Pins

Description	Pin	Supply Range
Input Supply	1	12-V DC –5%/+10%
Ground	2	0 V
Ground	3	0 V

6.8 J17 - JTAG Boundary Scan Connector

The JTAG Boundary connector J17 pins on the DLPLCRC910EVM pins are listed in Table 6-7. Two matching fourteen position connector part numbers are:

- Molex part number: 051110-1451
- Digi-Key part number: WM18047-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 087396-8051
- Digi-Key part number: WM23602CT-ND

Table 6-7. JTAG Boundary Scan Connector Pins

Description	Pin	Supply Range
NC	1	N/A
Supply Voltage	2	3.3 V
Ground	3	0 V
JTAG_TMS	4	3.3 V
Ground	5	0 V
JTAG_TCK	6	3.3 V
Ground	7	0 V
PROGRAMMER_TDO	8	3.3 V
Ground	9	0 V
PROGRAMMER_TDO	10	3.3 V
Ground	11	0 V
NC	12	N/A
NC	13	N/A
NC	14	N/A

6.9 J18 - SPI Programming Connector

The SPI programming connector J18 pins on the DLPLCRC910EVM are listed in Table 6-8. A matching ten position connector (with cable) part numbers is:

- Samtec part number: HCSD-05-D-10.00-01-N-P02

Table 6-8. SPI Programming Connector Pins

Description	Pin	Supply Range
Configuration CSZ (SS2)	1	2.5 V
Ground	2	0 V
NC (SS3)	3	0 V
NC	4	0 V
PICO - Configuration Data Out	5	2.5 V
NC	6	0 V
SCLK - Configuration Clock	7	2.5 V
POCI - Configuration Data In	8	2.5 V
Configuration CSZ (SS1)	9	2.5 V
Ground	10	0 V

6.10 J19, J20, and J21 - Fan Connectors

Fan connectors J19, J20, and J21 pins on the DLPLCRC910EVM are listed in Fan Connector Pins. Two matching 2-pin connector part numbers are:

- JST part number: XHP-2
- Digi-Key part number: 455-2266-ND

The corresponding terminal (crimp) part numbers are:

- JST part number: SXH-001T-P0.6
- Digi-Key part number:
  - 455-1135-1-ND - Cut Tape (CT)
  - 455-1135-2-ND - Tape & Reel (TR)

Table 6-9. Fan Connector Pins

Description	Pin	Supply Range
Ground	1	0 V
Power	2	12 V

6.11 J500, J501 - FMC Connector (Male)

The 400 position FMC male connectors J500 and J501. Mating part numbers are:

- Samtec part number: SEAF-40-05.0-S-10-2-A-K-TR
- Digi-Key part number: SAM8009CT-ND

7 DLPLCRC910EVM Power Supply Requirements

7.1 External Power Supply Requirements

The DLP LightCrafter DLPC910 EVM does not include a power supply. The external power supply requirements are:

- Nominal voltage: 12-V DC -5%/+10%
- Current: 5 A
- DC connector size:
  - Inner diameter: 2.5 mm
  - Outer diameter: 5.5 mm
  - Shaft: 9.5-mm female, center positive
- A recommended power supply is Digi-Key part number 102-3811-ND or better.

Note

External Power Supply Regulatory Compliance Certifications: Recommend selection and use of an external power supply which meets TI's required minimum electrical ratings in addition to complying with applicable regional product regulatory and safety certification requirements such as (by example) UL, CSA, VDE, CCC, PSE, etc.

8 Related Documentation from Texas Instruments

Component data sheets, technical documents, design documents, and ordering information can be found at the following links:

DLPC910 Digital Controller Product Folder
LightCrafter DLPC910 EVM Tool Folder
DLP6500FLQ DMD Product Folder
DLP LightCrafter DLP6500FLQ DMD EVM Tool Folder
DLP9000X DMD Product Folder
DLP LightCrafter DLP9000X DMD EVM Tool Folder
DLP9000XUV DMD Product Folder
DLP LightCrafter DLP9000XUV DMD EVM Tool Folder
DLPC910 Apps FPGA Guide

9 Abbreviations and Acronyms

The following lists abbreviations and acronyms used in this manual:

Apps FPGA	AMD Xilinx Virtex 7 FPGA on the VC-707 EVM or similar board for customer applications
DDR	Double Data Rate
DLL	Dynamic Link Library
DMD	Digital Micromirror Device
DPI	Dots Per Inch
EVM	Evaluation Module (Board)
FCC	Federal Communications Commission
FMC	FPGA Mezzanine Connector
FPGA	Field Programmable Gate Array
FW	Firmware
GPIF	General Purpose Interface
GPIO	General Purpose Input Output
GUI	Graphical User Interface
HPC	High Pin Count
HW	Hardware
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LED	Light Emitting Diode
MCP	Mirror Clocking Pulse
PBC	Processor Bus Control
PCB	Printed Circuit Board
PMBUS	Power Management Bus
SDK	Software Development Kit
SPI	Serial-Peripheral Interface
SW	Switch
TPG	Test Pattern Generator
USB	Universal Serial Bus
VHDL	Verification and Hardware Description Language

VSP	Very Small Pixel

10 Safety

10.1 Caution Labels

CAUTION

To minimize the risk of fire or equipment damage, make sure that air is allowed to circulate freely around the DLPLCRC910EVM board when operating.

CAUTION

The DLPLCRC910EVM contains ESD-sensitive components. Handle with care to prevent permanent damage.

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   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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