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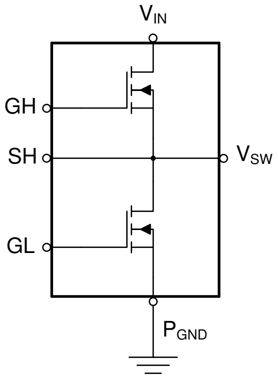
CSD88599Q5DC 60V Half-Bridge NexFET™ Power Block

1 Features

- Half-bridge power block
- High-density SON 5mm × 6mm footprint
- Low $R_{DS(ON)}$ for minimized conduction Losses
  - 3.0W P_{Loss} at 30A
- DualCool™ thermally Enhanced Package
- Ultra-low-inductance package
- RoHS compliant
- Halogen free
- Lead-free terminal plating

2 Applications

- Three-phase bridge for brushless DC motor control
- Up to 12s battery power tools
- Other half and full bridge topologies



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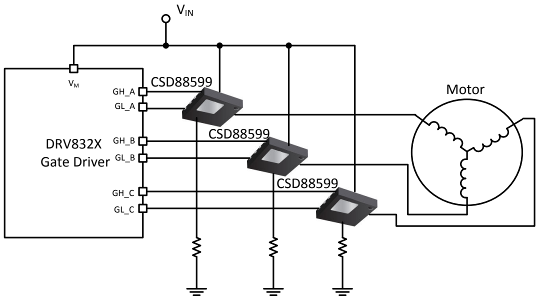
Power Block Schematic



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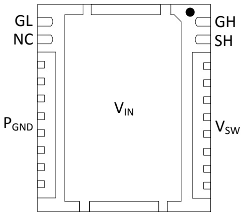
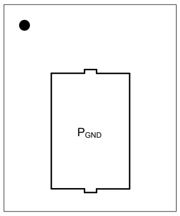
Typical Circuit

3 Description

The CSD88599Q5DC 60V power block is an optimized design for high-current motor control applications, such as handheld, cordless garden and power tools. This device utilizes TI's stacked die technology in order to minimize parasitic inductances while offering a complete half bridge in a space saving thermally enhanced DualCool™ 5mm × 6mm package. With an exposed metal top, this power block device allows for simple heat sink application to draw heat out through the top of the package and away from the PCB, for superior thermal performance at the higher currents demanded by many motor control applications.



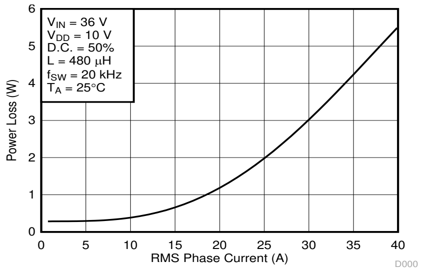
Bottom View



Top View

Device Information

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD88599Q5DC	2500	13 Inch Reel	SON 5.00mm × 6.00mm Plastic Package	Tape and Reel
CSD88599Q5DCT	250	7 Inch Reel		



Power Loss vs Output Current

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4 Specifications

4.1 Absolute Maximum Ratings

T_J = 25°C (unless otherwise noted)(1)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
Voltage	V_{IN} to P_{GND}	–0.8	60	V
	V_{SW} to P_{GND}	–0.3	60	
	GH to SH	–20	20	
	GL to P_{GND}	–20	20	
Pulsed current rating, I_{DM} (2)			400	A
Power dissipation, P_D			12	W
Avalanche energy, E_{AS}	High-side FET, I_D = 95A, L = 0.1mH		448	mJ
	Low-side FET, I_D = 95A, L = 0.1mH		448	
Operating junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Single FET conduction, max $R_{\theta JC}$ = 1.1°C/W, pulse duration ≤ 100μs, single pulse.

4.2 Recommended Operating Conditions

T_J = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{DD}	Gate drive voltage		4.5	16	V
V_{IN}	Input supply voltage(1)			54	V
f_{SW}	Switching frequency	C_{BST} = 0.1 μF (min)	5	50	kHz
I_{OUT}	RMS motor winding current			40	A
T_J	Operating temperature			125	°C

(1) Up to 42V input use one capacitor per phase, MLCC 10nF, 100V, X7S, 0402, PN: C1005X7S2A103K050BB from V_{IN} to GND return. Between 42V to 54V input operation, add RC switch-node snubber as described in the *Section 5.8.1.1* section of this data sheet.

4.3 Power Block Performance

T_J = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}	Power loss(1)	V_{IN} = 36V, V_{DD} = 10V, I_{OUT} = 30A, f_{SW} = 20kHz, T_J = 25°C, duty cycle = 50%, L = 480μH		3.0		W
P_{LOSS}	Power loss	V_{IN} = 36V, V_{DD} = 10V, I_{OUT} = 30A, f_{SW} = 20kHz, T_J = 125°C, duty cycle = 50%, L = 480μH		3.4		W

(1) Measurement made with eight 10μF 50V ±10% X5R (TDK C3225X5R1H106K250AB or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using UCC27210DDAR 100V, 4A driver IC.

4.4 Thermal Information

T_J = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu)(2)			125	°C/W
	Junction-to-ambient thermal resistance (max Cu)(2) (1)			50	

4.4 Thermal Information (continued)

T_J = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package)[2]			2.1	°C/W
	Junction-to-case thermal resistance (V_{IN} pin)[2]			1.1	

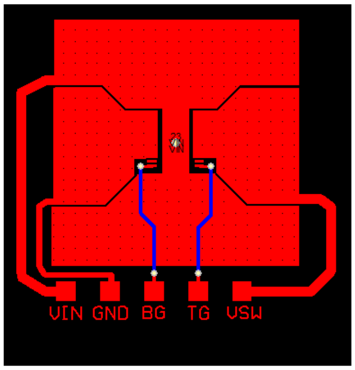
(1) Device mounted on FR4 material with 1in^2 (6.45cm^2) Cu.

(2) $R_{\theta JC}$ is determined with the device mounted on a 1in^2 (6.45cm^2), 2oz (0.071mm) thick Cu pad on a 1.5in × 1.5in (3.81cm × 3.81cm), 0.06in (1.52mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

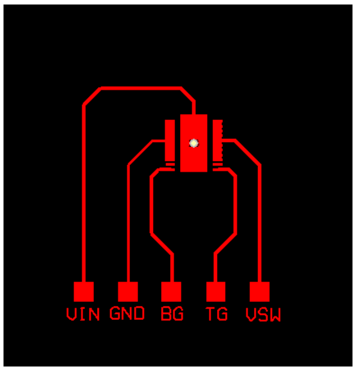
4.5 Electrical Characteristics

T_J = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_{DS} = 250μA	60			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 48V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250μA	1.4	2.0	2.5	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5V, I_{DS} = 30A		2.5	3.3	mΩ
		V_{GS} = 10V, I_{DS} = 30A		1.7	2.1	
g_{fs}	Transconductance	V_{DS} = 6V, I_{DS} = 30A		130		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 30V, f = 1MHz		3720	4840	pF
C_{OSS}	Output capacitance			670	870	pF
C_{RSS}	Reverse transfer capacitance			12	16	pF
R_G	Series gate resistance			0.9	1.8	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 30V, I_{DS} = 30A		21	27	nC
Q_g	Gate charge total (10 V)			43	56	nC
Q_{gd}	Gate charge gate-to-drain			7.0		nC
Q_{gs}	Gate charge gate-to-source			10.1		nC
$Q_{g(th)}$	Gate charge at V_{th}			6.3		nC
Q_{OSS}	Output charge	V_{DS} = 30V, V_{GS} = 0V		100		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 30V, V_{GS} = 10V, I_{DS} = 30A, R_G = 0Ω		9		ns
t_r	Rise time			20		ns
$t_{d(off)}$	Turnoff delay time			23		ns
t_f	Fall time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{DS} = 30A, V_{GS} = 0V		0.8	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS} = 30V, I_F = 30A, di/dt = 300A/μs		172		nC
t_{rr}	Reverse recovery time			36		ns



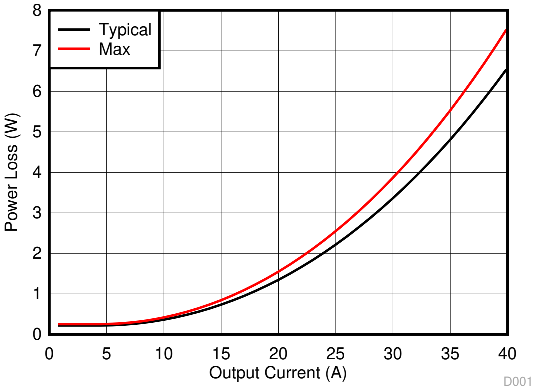
Max $R_{\theta JA}$ = 50°C/W when mounted on 1in^2 (6.45cm^2) of 2oz (0.071mm) thick Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on minimum pad area of 2oz (0.071mm) thick Cu.

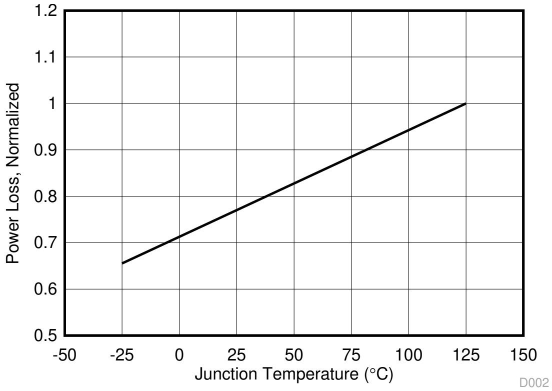
4.6 Typical Power Block Device Characteristics

The typical power block system characteristic curves (Figure 4-1 through Figure 4-6) are based on measurements made on a PCB design with dimensions of 4in (W) × 3.5in (L) × 0.062in (H) and 6 copper layers of 2oz copper thickness. See *Section 5* section for detailed explanation. T_J = 125°C, unless stated otherwise.



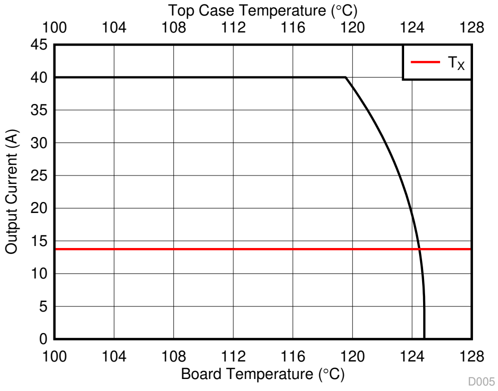
V_{IN} = 36V V_{DD} = 10V D.C. = 50%
f_{SW} = 20kHz L = 480µH

Figure 4-1. Power Loss vs Output Current



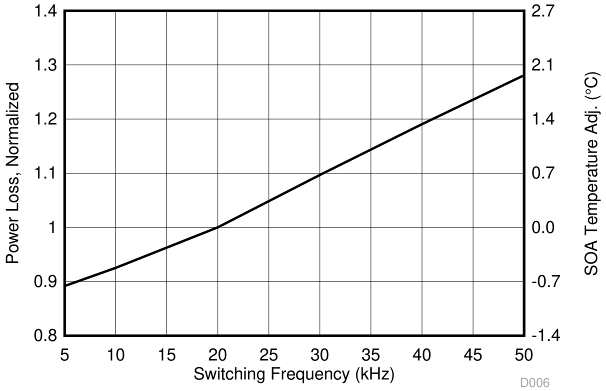
V_{IN} = 36V V_{DD} = 10V D.C. = 50%
f_{SW} = 20kHz L = 480µH I_{OUT} = 40 A

Figure 4-2. Power Loss vs Temperature



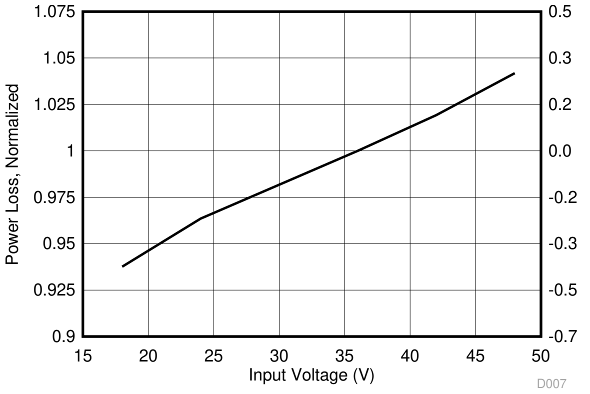
V_{IN} = 36V V_{DD} = 10V D.C. = 50%
f_{SW} = 20kHz L = 480µH

Figure 4-3. Typical Safe Operating Area



V_{IN} = 36V V_{DD} = 10V I_{OUT} = 40A
L = 480µH D.C. = 50%

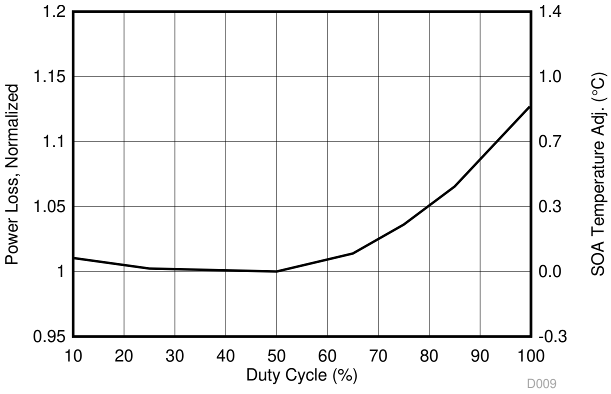
Figure 4-4. Normalized Power Loss vs Switching Frequency



D.C. = 50% V_{DD} = 10V I_{OUT} = 40A

f_{SW} = 20kHz L = 480µH

Figure 4-5. Normalized Power Loss vs Input Voltage



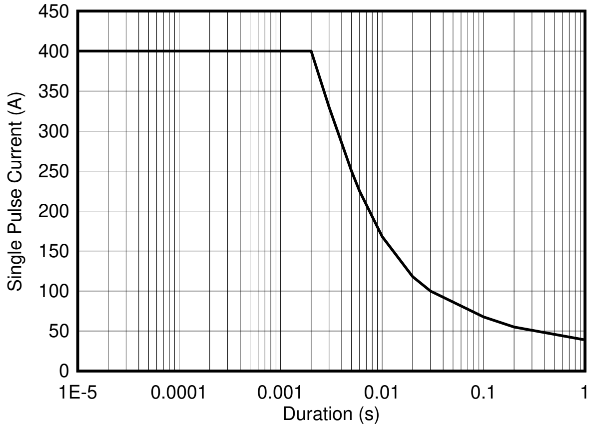
V_{IN} = 36V V_{DD} = 10V

f_{SW} = 20kHz L = 480µH

Figure 4-6. Normalized Power Loss vs Duty Cycle

4.7 Typical Power Block MOSFET Characteristics

T_J = 25°C, unless stated otherwise.



Max $R_{\theta JA}$ = 125°C/W

Figure 4-7. Single Pulse Current vs Pulse Duration

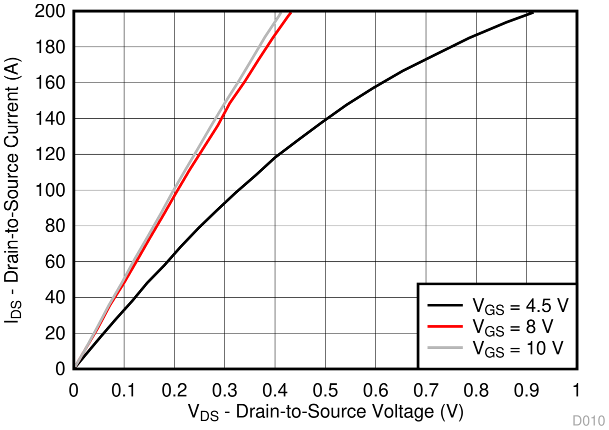
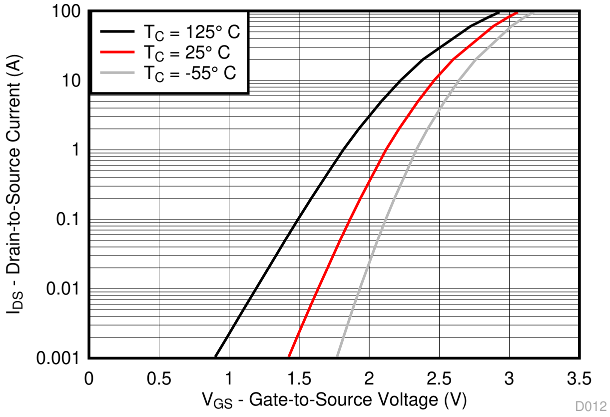
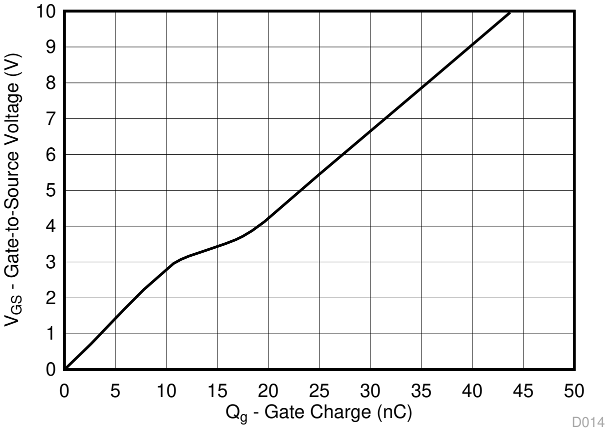


Figure 4-8. MOSFET Saturation Characteristics



V_{DS} = 5V

Figure 4-9. MOSFET Transfer Characteristics



I_D = 30A V_{DS} = 30V

Figure 4-10. MOSFET Gate Charge

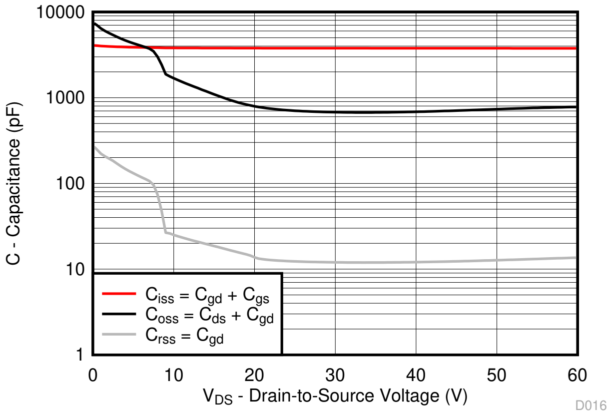
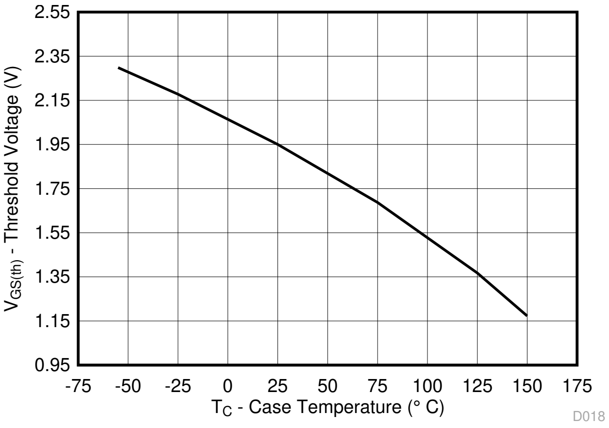


Figure 4-11. MOSFET Capacitance



I_D = 250µA

Figure 4-12. Threshold Voltage vs Temperature

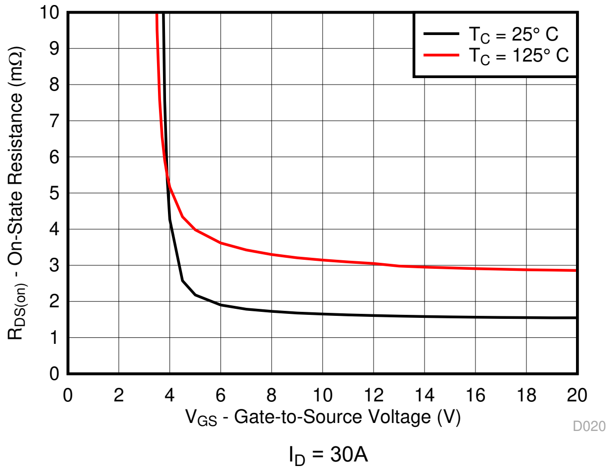


Figure 4-13. MOSFET $R_{DS(on)}$ vs V_{GS}

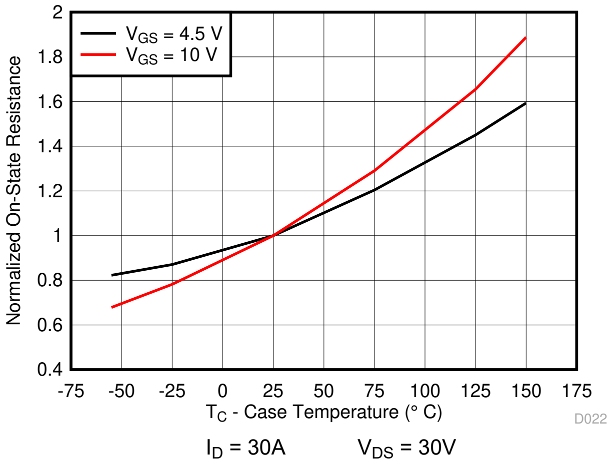


Figure 4-14. MOSFET Normalized $R_{DS(on)}$ vs Temperature

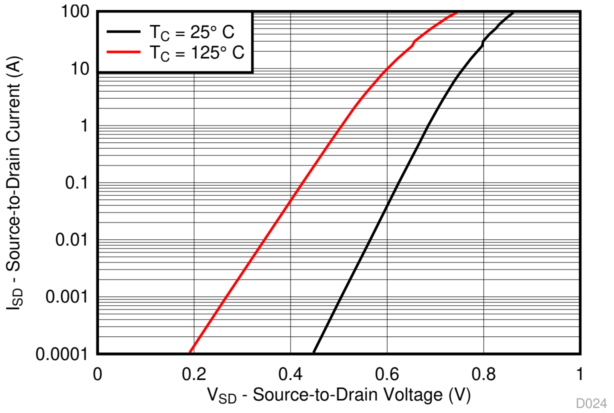


Figure 4-15. MOSFET Body Diode Forward Voltage

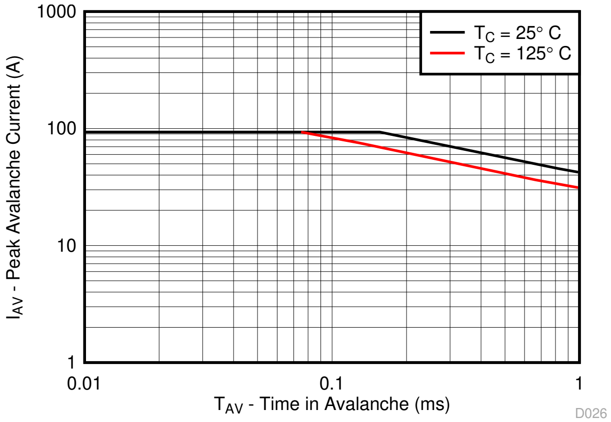


Figure 4-16. MOSFET Single Pulse Unclamped Inductive Switching

5 Application and Implementation

Note

Information in the following Application section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI customers are responsible for determining suitability of components selection for their designs. Customers should validate and test their design implementation to confirm system functionality.

5.1 Application Information

Historically, battery powered tools have favored brushed DC configurations to spin their primary motors, but more recently, the advantages offered by brushless DC operation (BLDC) operation have brought about the advent of popular designs that favor the latter. Those advantages include, but are not limited to higher efficiency and therefore longer battery life, superior reliability, greater peak torque capability, and smooth operation over a wider range of speeds. However, BLDC designs put increased demand for higher power density and current handling capabilities on the power stage responsible for driving the motor.

The CSD88599Q5DC is part of TI's power block product family and is a highly optimized product designed explicitly for the purpose driving higher current DC motors in power and gardening tools. It incorporates TI's latest generation silicon which has been optimized for low resistance to minimize conduction losses and offer excellent thermal performance. The power block utilizes TI's stacked die technology to offer one complete half bridge vertically integrated into a single 5mm × 6mm package with a DualCool exposed metal case. This feature allows the designer to apply a heatsink to the top of the package and pull heat away from the PCB, thus maximizing the power density while reducing the power stage footprint by up to 50%.

5.2 Brushless DC Motor With Trapezoidal Control

The trapezoidal commutation control is simple and has fewer switching losses compared to sinusoidal control.

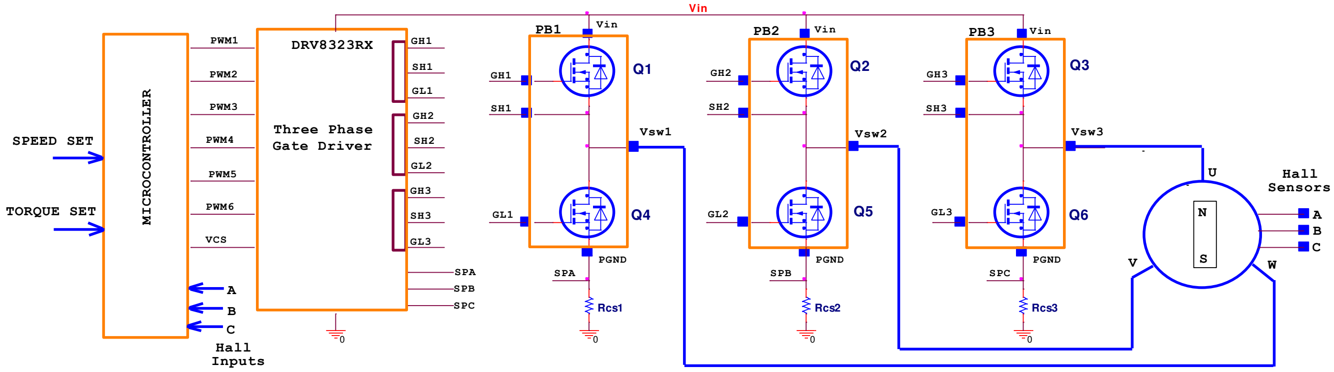


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Figure 5-1. Functional Block Diagram

The block diagram shown in Figure 5-1 offers a simple instruction of what is required to drive a BLDC motor: one microcontroller, one three-phase driver IC, three power blocks (historically six power MOSFETs) and three Hall effect sensors. The microcontroller responsible for block commutation must always know the rotor orientation or its position relative to the stator coils. This is easy achieved with a brushed DC motor due to the fixed geometry and position of the rotor windings, shaft and commutator.

A three-phase BLDC motor requires three Hall effect sensors or a rotary encoder to detect the rotor position in relation to stator armature windings. With input from these three Hall effect sensors output signals, the microcontroller can determine the proper commutation sequence. The three Hall sensors named A, B, and C are mounted on the stator core at 120° intervals and the stator phase windings are implemented in a star configuration. For every 60° of motor rotation, one Hall sensor changes its state. Based on the Hall sensors' output code, at the end of each block commutation interval the ampere conductors are commutated to the next position. There are 6 steps required to complete a full electrical cycle. The number of block commutation cycles to complete a full mechanical rotation is determined by the number of rotor pole pairs.

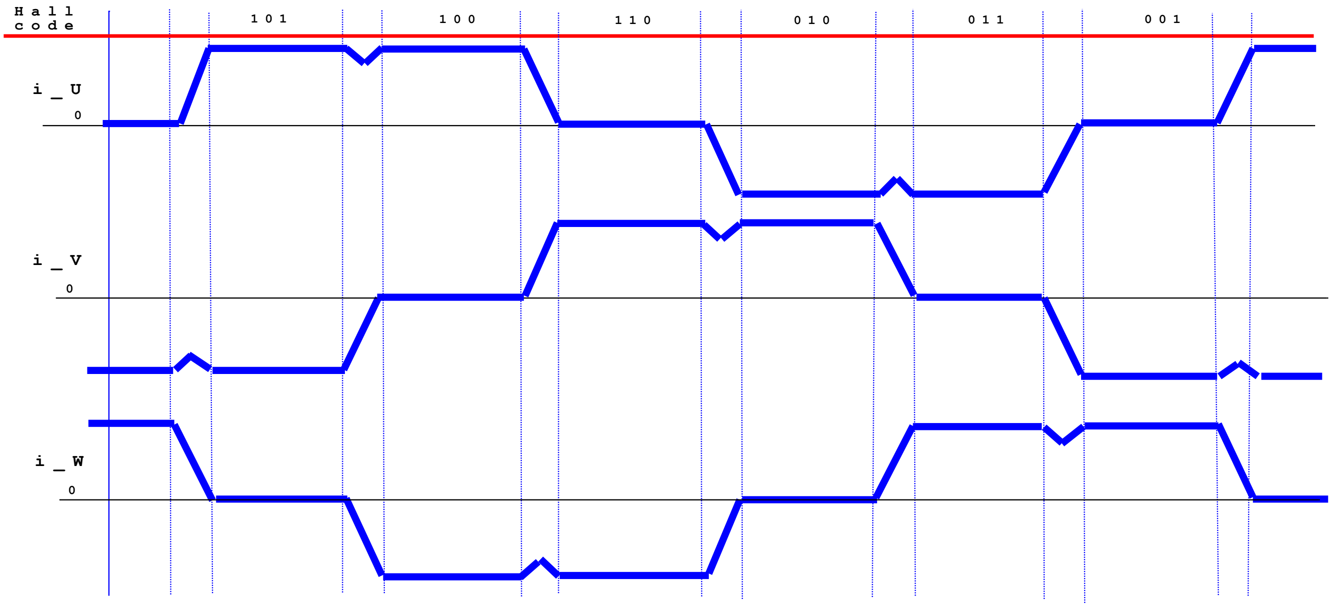

Figure 5-2. Winding Current Waveforms on a BLDC Motor

Figure 5-2 above shows the three phase motor winding currents i_U, i_V, and i_W when running at 100% duty cycle.

Trapezoidal commutation control offers the following advantages:

- Only two windings in series carry the phase winding current at any time while the third winding is open.
- Only one current sensor is necessary for all three windings U, V, and W.
- The position of the current sensor allows the use of low-cost shunt resistors.

However, trapezoidal commutation control has the disadvantage of commutation torque ripple. The current sense on a three-phase inverter can be configured to use a single-shunt or three different sense resistors. For cost sensitive applications targeting sensorless control, the three Hall effect sensors can be replaced with BEMF voltage feedback dividers.

To obtain faster motor rotations and higher revolutions per minute (RPM), shorter periods and higher V_{IN} voltage are necessary. Contrarily, to reduce the rotational speed of the motor, it is necessary to lower the RMS voltage applied across stator windings. This can easily be easily achieved by modulating the duty cycle, while maintain a constant switching frequency. Frequency for the three-phase inverter chosen is usually low between 10kHz to 50kHz to reduce winding losses and to avoid audible noise.

5.3 Power Loss Curves

CSD88599Q5DC was designed to operate up to 10-cell Li-Ion battery voltage applications ranging from 30V to 42V, typical 36V. For 11 and 12s, input voltages between 42V to 54V, RC snubbers are required for each switch-node U, V, and W. To reduce ringing, refer to the *Section 5.8.1.1* section. In an effort to simplify the design process, Texas Instruments has provided measured power loss performance curves over a variety of typical conditions.

Figure 4-1 plots the CSD88599Q5DC power loss as a function of load current. The measured power loss includes both input conversion loss and gate drive loss.

Equation 1 is used to generate the power loss curve:

$$\textbf{Power loss (W)} = (V_{IN} \times I_{IN\_SHUNT}) + (V_{DD} \times I_{DD\_SHUNT}) - (V_{SW\_AVG} \times I_{OUT}) \qquad (1)$$

The power loss measurements were made on the circuit shown in Figure 5-3. Power block devices for legs U and V, PB1 and PB2 were disabled by shorting the CSD88599Q5DC high-side and low-side FETs' gate-to-source terminals. Current shunt Iin_SHUNT provides input current and Idd_SHUNT provides driver supply current measurements. The winding current is measured from the DC load. An averaging circuit provides switch node W equivalent RMS voltage.

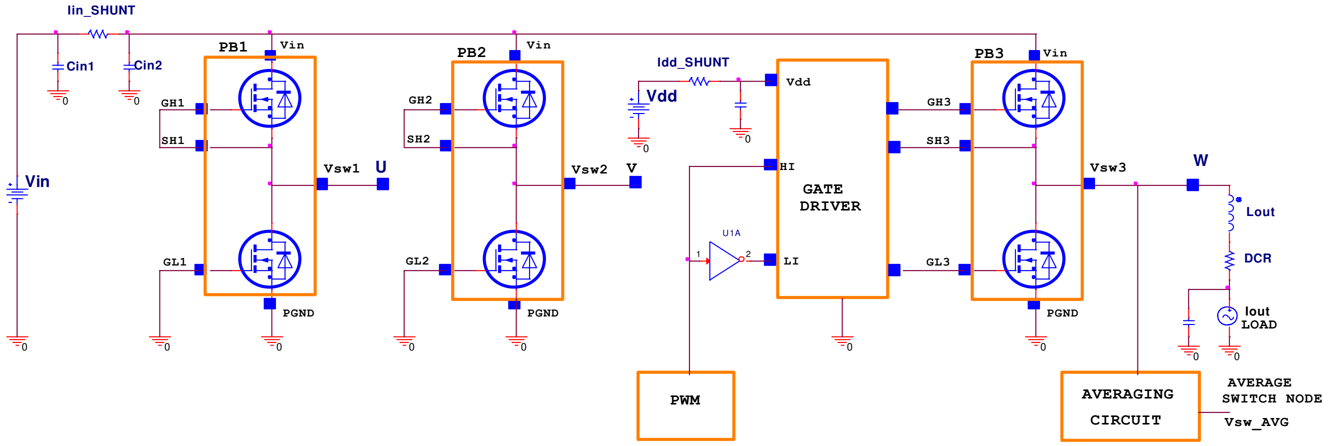

Figure 5-3. Power Loss Test Circuit

The RMS current on the CSD88599Q5DC device depends on the motor winding current. For trapezoidal control, the MOSFET RMS current is calculated using Equation 2.

$$I_{RMS} = I_{OUT} \times \sqrt{2} \qquad (2)$$

Taking into consideration system tolerances with the current measurement scheme, the inverter design needs to withstand a 20% overload current.

Table 5-1. RMS and Overload Current Calculations

Winding RMS Current (A)	CSD88599Q5DC I_{RMS} (A)	Overload 20% × I_{RMS} (A)
20	28	34
30	42	51
40	56	68

5.4 Safe Operating Area (SOA) Curve

The SOA curve in Figure 4-3 provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. This curve outlines the board and case temperatures required for a given load current. The area under the curve dictates the safe operating area. This curve is based on measurements made on a PCB design with dimensions of 4in (W) × 3.5in (L) × 0.062in (H) and 6 copper layers of 2oz copper thickness.

5.5 Normalized Power Loss Curves

The normalized curves in the CSD88599Q5DC data sheet provide guidance on the power loss and SOA adjustments based on application specific needs. These curves show how the power loss and SOA temperature boundaries will adjust for different operation conditions. The primary Y-axis is the normalized change in power loss while the secondary Y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the typical power loss. The change in SOA temperature is subtracted from the SOA curve.

5.6 Design Example – Regulate Current to Maintain Safe Operation

If the case and board temperature of the power block are known, the SOA can be used to determine the maximum allowed current that will maintain operation within the safe operating area of the device. The following procedure outlines how to determine the RMS current limit while maintaining operation within the confines of the SOA, assuming the temperatures of the top of the package and PCB directly underneath the part are known.

1. Start at the maximum current of the device on the Y-axis and draw a line from this point at the known top case temperature to the known PCB temperature.
2. Observe where this point intersects the T_X line.
3. At this intersection with the T_X line, draw vertical line until you hit the SOA current limit. This intercept is the maximum allowed current at the corresponding power block PCB and case temperatures.

In the example below, we show how to achieve this for the temperatures T_C = 124°C and T_B = 120°C. First we draw from 40 A on the Y-axis at 124°C to 120°C on the X-axis. Then, we draw a line up from where this line crosses the T_X line to see that this line intercepts the SOA at 34A. Thus we can assume if we are measuring a PCB temperature of 124°C, and a top case temperature of 120°C, the power block can handle 34A RMS, at the normalized conditions. At conditions that differ from those in Figure 4-1, the user may be required to make an SOA temperature adjustment on the T_X line, as shown in the next section.

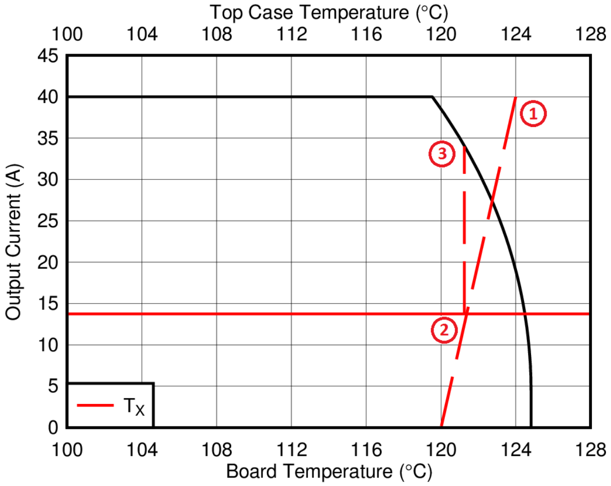

Figure 5-4. Regulating Current to Maintain Safe Operation

5.7 Design Example – Regulate Board and Case Temperature to Maintain Safe Operation

In the previous example we showed how given the PCB and case temperature, the current of the power block could be limited to ensure operation within the SOA. Conversely, if the current and other application conditions are known, one can determine from the SOA what board or case temperature the user will need to limit their design to. The user can estimate product loss and SOA boundaries by arithmetic means. Though the power loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps the user should take to predict product performance for any set of system conditions.

5.8 Layout

The two key system-level parameters that can be optimized with proper PCB design are electrical and thermal performance. A proper PCB layout will yield maximum performance in both areas. Below are some tips for how to address each.

5.8.1 Layout Guidelines

5.8.1.1 Electrical Performance

The CSD88599Q5DC power block has the ability to switch at voltage rates greater than 1kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors; high-current, high dI/dT switching path; current shunt resistors; and GND return planes. As with any high-power inverter operated in hard switching mode, there will be voltage ringing present on the switch nodes U, V, and W. Switch-node ringing appears mainly at the HS FET turnon commutation with positive winding current direction. The U, V, and W phase connections to the BLDC motor can be usually excluded from the ringing behavior since they are subjected to high-peak currents but low dI/dT slew-rates. However, a compact PCB design with short and low-parasitic loop inductances is critical to achieve low ringing and compliance with EMI specifications.

For safe and reliable operation of the three-phase inverter, motor phase currents have to be accurately monitored and reported to the system microcontroller. One current sensor needs to be connected on each motor phase winding U, V, and W. This sensing method is best for current sensing as it provides good accuracy over a wide range of duty cycles, motor torque, and winding currents. Using current sensors is recommended because it is less intrusive to the V_{IN} and GND connections.

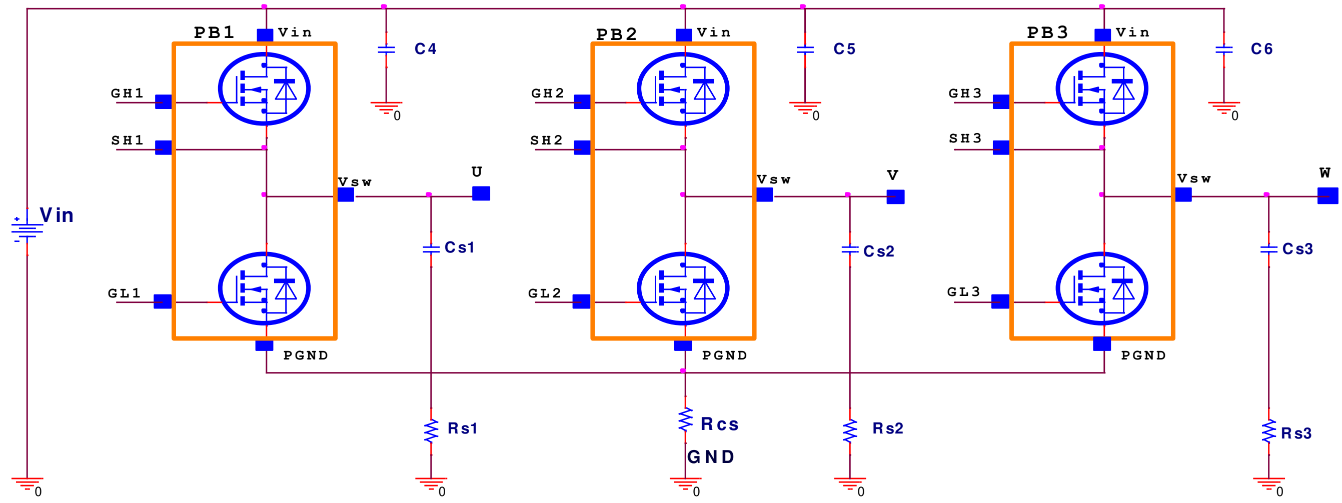

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Figure 5-5. Recommended Ringing Reduction Components

However, for cost sensitive applications, current sensors are generally replaced with current sense resistors.

- For designs using the 60V three-phase smart gate driver DRV8320SRHBR, current sense resistor R_{CS} can be placed between common source terminals for all 3 power block devices CSD88599Q5DC to P_{GND} and measured using an external current sense amplifier as depicted in Figure 5-5 above.
- For designs using the 60V three-phase gate driver DRV8323RSRGZT, three current sense resistors R_{CS1}, R_{CS2} and R_{CS3} can be used between each CSD88599Q5DC source terminal to GND and measured by the included DRV8323 current sense amplifiers. The three-phase driver IC should be placed as close as possible to the power block gate GL and GH terminals.

Breaking the high-current flow path from the source terminals of the power block to GND by introducing the R_{CS} current shunt resistors introduces parasitic PCB inductance. In the event the switch node waveforms exhibits peak ringing that reaches undesirable levels, the ringing can be reduced by using the following ringing reduction components:

- The use of a high-side gate resistor in series with the GH pin is one effective way to reduce peak ringing. The recommended HS FET gate resistor value will range between 4.7Ω to 10Ω depending on the driver IC output characteristics used in conjunction with the power block device. The low-side FET gate pin GL should connect directly to the driver IC output to avoid any parasitic cdV/dT turnon effect.
- Low-inductance MLCC caps C4, C5, and C6 can be used across each power block device from V_{IN} to the source terminal P_{GND}. MLCC 10nF, 100V, ±10%, X7S, 0402, PN: C1005X7S2A103K050BB are recommended.
- Ringing can be reduced via the implementation of RC snubbers from each switch node U, V, and W to GND. Recommended snubber component values are as follows:
  - Snubber resistors Rs1, Rs2, Rs3: 2.21Ω, 1%, 0.125W, 0805, PN: CRCW08052R21FKEA
  - Snubber caps Cs1, Cs2, and Cs3: MLCC 4.7nF, 100V, X7S, 0402, PN: C1005X7S2A472M050BB

With a switching frequency of 20kHz on the three-phase inverter, the power dissipation on the RC snubber resistor is 80mW per channel. As a result, 0805 package size for resistors Rs1, Rs2, and Rs3 is sufficient.

5.8.1.2 Thermal Considerations

The CSD88599Q5DC power block device has the ability to utilize the PCB copper planes as the primary thermal path. As such, the use of thermal vias included in the footprint is an effective way to pull away heat from the device and into the system board. Concerns regarding solder voids and manufacturability issues can be addressed through the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel.

- Intentionally space out the vias from one another to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed by the design. The example in Figure 5-6 uses vias with a 10-mil drill hole and a 16mil solder pad.
- Tent the opposite side of the via with solder-mask. Ultimately the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

To take advantage of the DualCool thermally enhanced package, an external heatsink can be applied on top of the power block devices. For low EMI, the heatsink is usually connected to GND through the mounting screws to the PCB. Gap pad insulators with good thermal conductivity should be used between the top of the package and the heatsink. The Bergquist Sil-Pad 980 is recommended which provides excellent thermal impedance of 1.07°C/W @ 50psi.

5.8.2 Layout Example

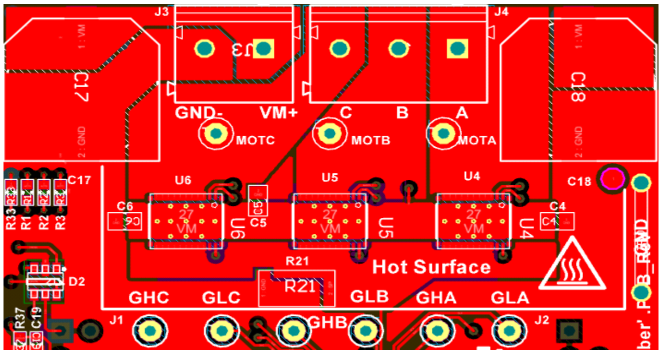

Figure 5-6. Top Layer

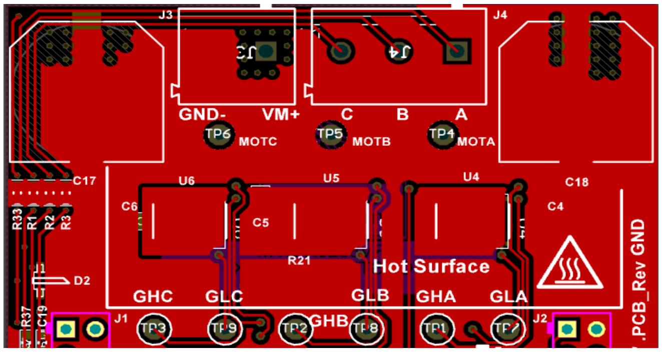

Figure 5-7. Bottom Layer

The placement of the input capacitors C4, C5, and C6 relative to V_{IN} and P_{GND} pins of CSD88599Q5DC device should have the highest priority during the component placement routine. It is critical to minimize the V_{IN} to GND parasitic loop inductance. A shunt resistor R21 is used between all three U4, U5, and U6 power block source terminals to the input supply GND return pin.

Input RMS current filtering is achieved via two bulk caps C17 and C18. Based on the RMS current ratings, the recommended part number for input bulk is CAP AL, 330µF, 63V, ±20%, PN: EMVA630ADA331MKG5S.

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

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6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2018) to Revision D (June 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added PGND to the Top View pinout diagram	1
• Added Pin Configuration Table	19

Changes from Revision B (January 2018) to Revision C (April 2018)	Page
• Corrected Figure 5-4 to show 40A maximum	13

Changes from Revision A (May 2017) to Revision B (January 2018)	Page
• Updated the mechanical data	19

Changes from Revision * (April 2017) to Revision A (May 2017)	Page
• Updated Typical Circuit drawing	1
• Changed the copper thickness to 2oz in *Typical Power Block Device Characteristics* conditions	5
• Changed the copper thickness to 2oz in *Safe Operating Area (SOA) Curve* paragraph	13

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Table 8-1. Pin Configuration Table

POSITION	PIN NAME	DESCRIPTION
1	GH	High Side Gate
2	SH	High Side Gate Return
3-11	V_{SW}	Switch Node
12-20	P_{GND}	Power Ground
21	NC	No Connect
22	GL	Low Side Gate
23-26	NC	No Connect
27	V_{IN}	Input Voltage

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD88599Q5DC	ACTIVE	VSON-CLIP	DMM	22	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	88599	Samples
CSD88599Q5DCT	ACTIVE	VSON-CLIP	DMM	22	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	88599	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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