LM2852 2A 500/1500 kHz Synchronous Buck Regulator

1 Features

- Input Voltage Range of 2.85 V to 5.5 V
- Factory EEPROM Set Output Voltages from 0.8 V to 3.3 V in 100-mV Increments
- Maximum Load Current of 2 A
- Voltage Mode Control
- Internal Type-Three Compensation
- Switching Frequency of 500 kHz or 1.5 MHz
- Low Standby Current of 10 µA
- Internal 60-mΩ MOSFET Switches
- Standard Voltage Options 0.8/1/1.2/1.5/1.8/2.5/3.3 V

2 Applications

- Low Voltage Point of Load Regulation
- Local Solution for FPGA/DSP/ASIC Core Power
- Broadband Networking and Communications Infrastructure
- Portable Computing

3 Description

The LM2852 synchronous buck regulator is a high frequency step-down switching voltage regulator capable of driving up to a 2A load with excellent line and load regulation. The LM2852 can accept an input voltage between 2.85 V and

5.5 V and deliver an output voltage that is factory programmable from 0.8 V to 3.3 V in 100-mV increments. The LM2852 is available with a choice of two switching frequencies –500 kHz (LM2852Y) or 1.5 MHz (LM2852X). It also features internal, type-three compensation to deliver a low component count solution. The exposed-pad HTSSOP-14 package enhances the thermal performance of the LM2852.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2852	HTSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

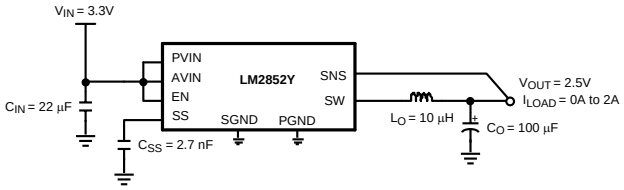
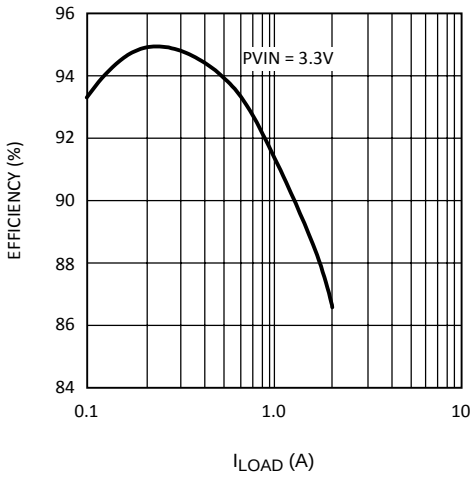


Figure 1. Efficiency vs I_{LOAD}



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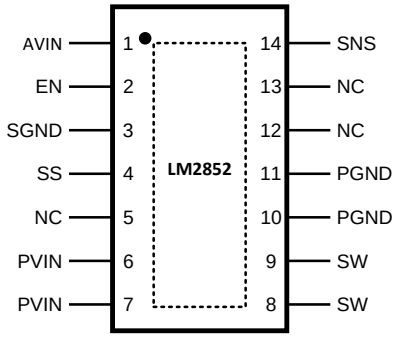
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2013) to Revision E	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

PWP Package
14-Pin HTSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVIN	1	I	Chip bias input pin. This provides power to the logic of the chip. Connect to the input voltage or a separate rail.
EN	2	I	Enable. Connect this pin to ground to disable the chip; connect to AVIN or leave floating to enable the chip; enable is internally pulled up.
Exposed			Connect to ground.
NC	5, 12, 13		No connect. These pins must be tied to ground or left floating in the application.
PGND	10, 11	G	Power ground. Connect this to an internal ground plane or other large ground plane.
PVIN	6, 7	I	Input supply pin. PVIN is connected to the input voltage. This rail connects to the source of the internal power PFET.
SGND	3	G	Signal ground.
SNS	14	O	Output voltage sense pin. Connect this pin to the output voltage as close to the load as possible.
SS	4	I	Soft-start pin. Connect this pin to a small capacitor to control startup. The soft-start capacitance range is restricted to values 1 nF to 50 nF.
SW	8, 9	O	Switch pin. Connect to the output inductor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
PVIN, AVIN, EN, SNS			6.5	V
Power dissipation		Internally limited		
14-Pin exposed pad HTSSOP package	Infrared (15 sec)		220	°C
	Vapor phase (60 sec)		215	°C
Maximum junction temperature			150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
PVIN to GND	1.5	5.5	V
AVIN to GND	2.85	5.5	V
Junction temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM2852 PWP (HTTSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

AVIN = PVIN = 5 V unless otherwise indicated under the Test Conditions column. Limits apply over the junction temperature (T_J) range of –40°C to 125°C (unless otherwise noted). Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SYSTEM PARAMETERS							
V_{OUT}	Voltage tolerance(1)	V_{OUT} = 0.8-V option		0.782		0.818	V
		V_{OUT} = 1-V option		0.9775		1.0225	
		V_{OUT} = 1.2-V option		1.173		1.227	
		V_{OUT} = 1.5-V option		1.4663		1.5337	
		V_{OUT} = 1.8-V option		1.7595		1.8405	
		V_{OUT} = 2.5-V option		2.4437		2.5563	
		V_{OUT} = 3-V option		2.9325		3.0675	
		V_{OUT} = 3.3-V option		3.2257		3.3743	
$\Delta V_{OUT}/\Delta AVIN$	Line regulation(1)	V_{OUT} = 0.8 V, 1 V, 1.2 V, 1.5 V, 1.8 V or 2.5 V, 2.85 V ≤ AVIN ≤ 5.5 V	T_J = –40°C to 125°C			0.6%	
			T_J = 25°C		0.2%		
		V_{OUT} = 3.3 V, 3.5 V ≤ AVIN ≤ 5.5 V	T_J = –40°C to 125°C			0.6%	
			T_J = 25°C		0.2%		
$\Delta V_{OUT}/\Delta I_O$	Load regulation	Normal operation	T_J = 25°C		8		mV/A
V_{ON}	UVLO threshold (AVIN)	Rising	T_J = –40°C to 125°C			2.85	V
			T_J = 25°C		2.47		
		Falling hysteresis	T_J = –40°C to 125°C	85		210	mV
			T_J = 25°C		150		
r_{DSON-P}	PFET ON resistance	Isw = 2 A	T_J = –40°C to 125°C			140	mΩ
			T_J = 25°C		75		
r_{DSON-N}	NFET ON resistance	Isw = 2 A	T_J = –40°C to 125°C			120	mΩ
			T_J = 25°C		55		
R_{SS}	Soft-start resistance	T_J = 25°C			400		kΩ
I_{CL}	Peak current limit threshold	LM2852X	T_J = –40°C to 125°C	2.75		4.95	A
			T_J = 25°C		4		
		LM2852Y	T_J = –40°C to 125°C	2.25		3.65	
			T_J = 25°C		3		
I_Q	Operating current	Non-switching	T_J = –40°C to 125°C			2	mA
			T_J = 25°C		0.85		
I_{SD}	Shutdown quiescent current	EN = 0 V	T_J = –40°C to 125°C			25	µA
			T_J = 25°C		10		
R_{SNS}	Sense pin resistance	T_J = 25°C			400		kΩ

(1) V_{OUT} measured in a non-switching, closed-loop configuration at the SNS pin.

Electrical Characteristics (continued)

AVIN = PVIN = 5 V unless otherwise indicated under the Test Conditions column. Limits apply over the junction temperature (T_J) range of –40°C to 125°C (unless otherwise noted). Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PWM							
f_{osc}	LM2852X	1500-kHz option.	T_J = –40°C to 125°C	1050		1825	kHz
			T_J = 25°C		1500		
	LM2852Y	500-kHz option.	T_J = –40°C to 125°C	325		625	kHz
			T_J = 25°C		500		
D_{range}	Duty cycle			0%		100%	
ENABLE CONTROL(2)							
V_{IH}	EN pin minimum high input			75			% of AVIN
V_{IL}	EN pin maximum low input					25	% of AVIN
I_{EN}	EN pin pullup current	EN = 0 V	T_J = 25°C		1.2		µA
THERMAL CONTROLS							
T_{SD}	T_J for thermal shutdown	T_J = 25°C			165		°C
T_{SD-HYS}	Hysteresis for thermal shutdown	T_J = 25°C			10		°C

(2) The enable pin is internally pulled up, so the LM2852 is automatically enabled unless an external enable voltage is applied.

6.6 LM2852Y Typical Characteristics (500 kHz)

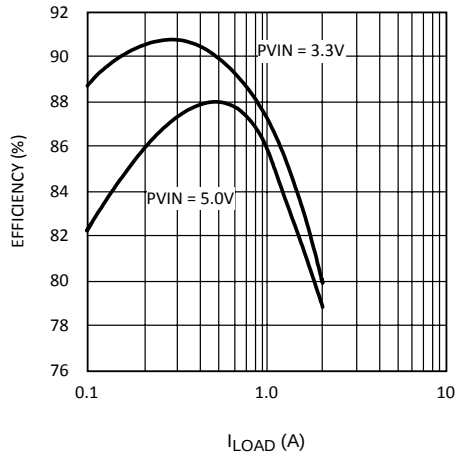


Figure 2. Efficiency vs I_{Load} V_{OUT} = 1.5 V

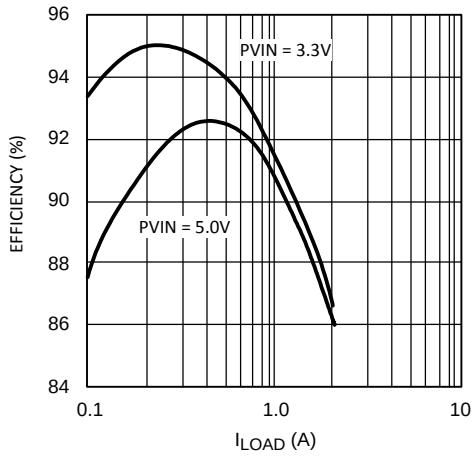


Figure 3. Efficiency vs I_{Load} V_{OUT} = 2.5 V

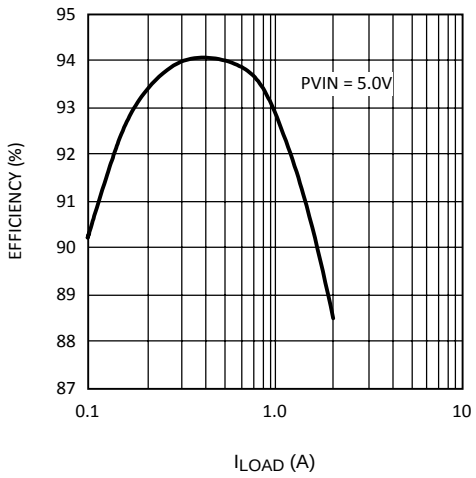


Figure 4. Efficiency vs I_{Load} V_{OUT} = 3.3 V

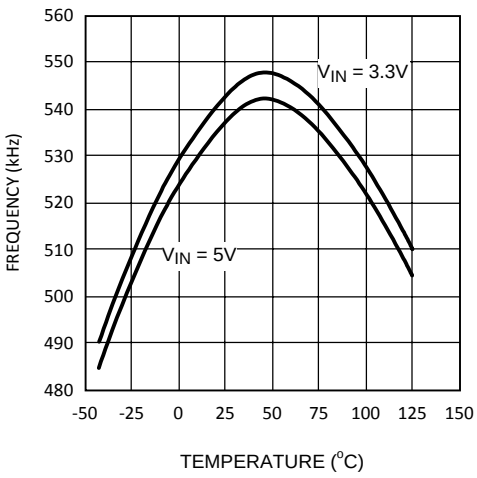


Figure 5. Frequency vs Temperature

6.7 LM2852X Typical Characteristics (1500 kHz)

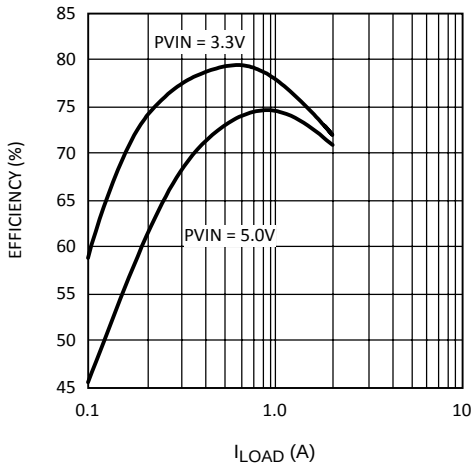


Figure 6. Efficiency vs I_{Load} V_{OUT} = 1.5 V

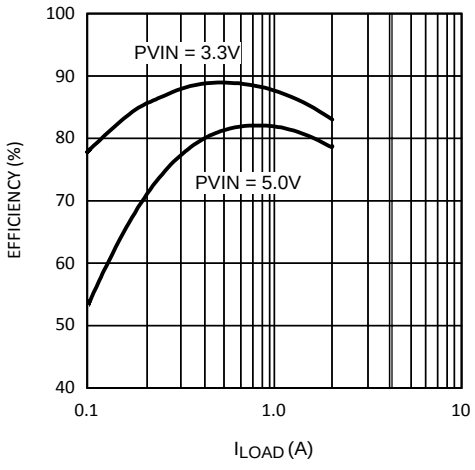


Figure 7. Efficiency vs I_{Load} V_{OUT} = 2.5 V

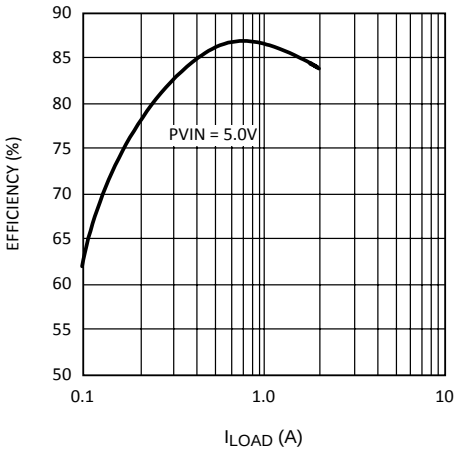


Figure 8. Efficiency vs I_{Load} V_{OUT} = 3.3 V

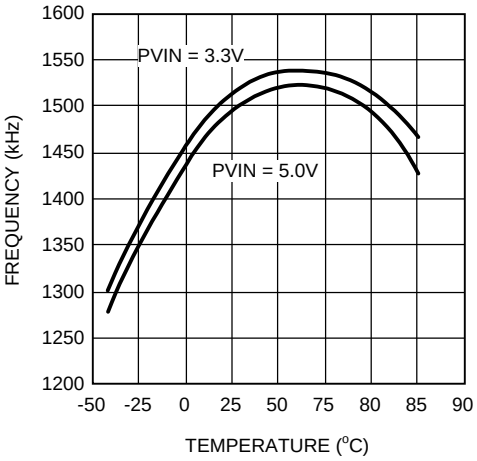


Figure 9. Frequency vs Temperature

6.8 LM2852 Typical Characteristics (Both Y and X Versions)

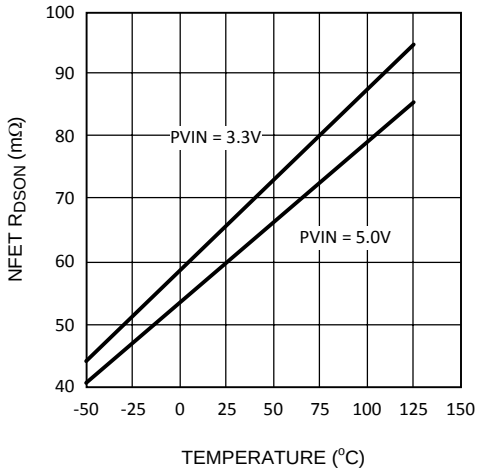


Figure 10. NMOS Switch R_{DSON} vs Temperature

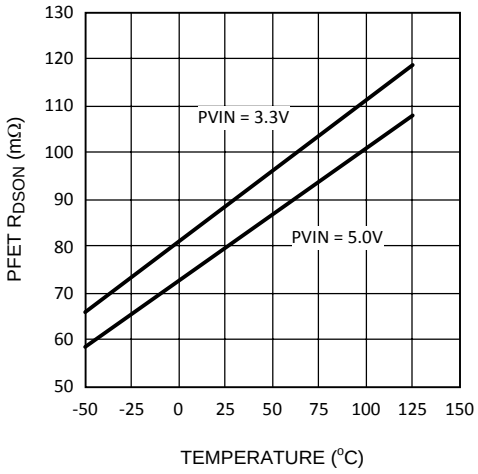


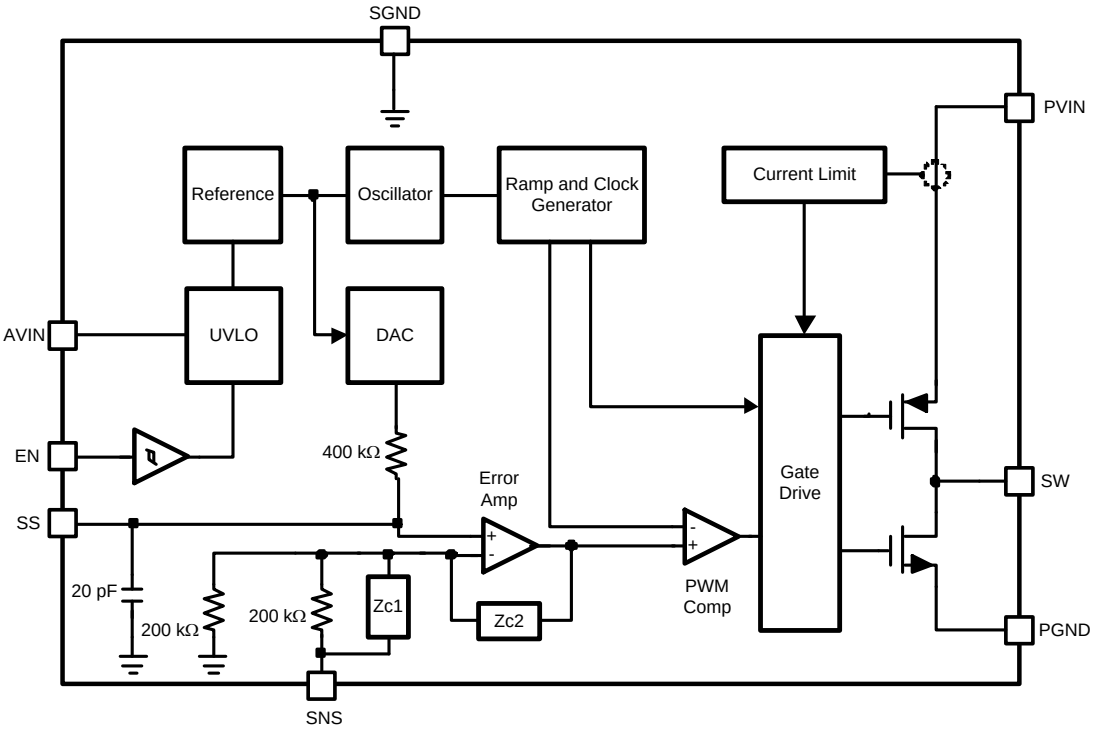
Figure 11. PMOS Switch R_{DSON} vs Temperature

7 Detailed Description

7.1 Overview

The LM2852 is a DC-DC synchronous buck regulator. Integration of the PWM controller, power switches and compensation network greatly reduces the component count required to implement a switching power supply.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Split-Rail Operation

The LM2852 can be powered using two separate voltages for AVIN and PVIN. AVIN is the supply for the control logic; PVIN is the supply for the power FETs. The output filter components need to be chosen based on the value of PVIN. For PVIN levels lower than 3.3 V, use output filter component values recommended for 3.3 V. PVIN must always be equal to or less than AVIN.

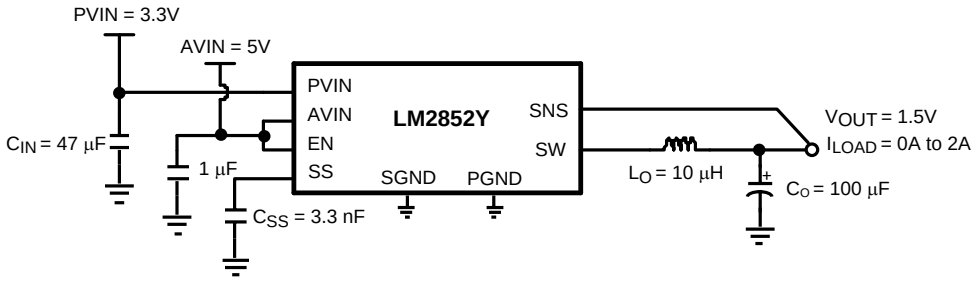


Figure 12. Split-Rail Operation

7.3.2 Switch Node Protection

The LM2852 includes protection circuitry that monitors the voltage on the switch pin. Under certain conditions, switching is disabled in order to protect the switching devices. One result of the protection circuitry may be observed when power to the LM2852 is applied with no or light load on the output. The output regulates to the rated voltage, but no switching may be observed. As soon as the output is loaded, the LM2852 begins normal switching operation.

7.4 Device Functional Modes

The LM2852 Enable pin is internally pulled up so that the part is enabled anytime the input voltage exceeds the UVLO threshold. A pulldown resistor can be used to set the enable input to low.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2852 is a DC-DC synchronous buck regulator capable of driving a maximum load current of 2A, with an input range of 2.85 V to 5.5 V and a variable output range of 0.8 V to 3.3 V. Figure 13 is a schematic example of a typical application.

8.2 Typical Application

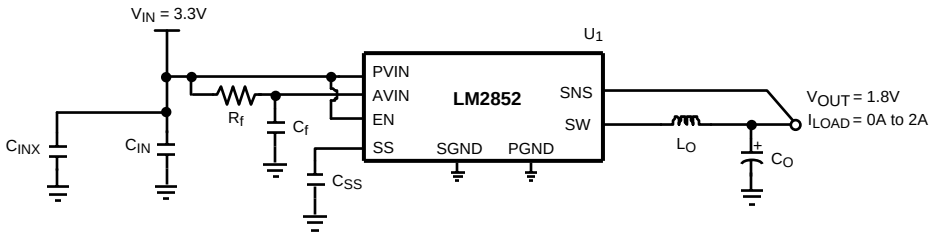


Figure 13. LM2852 Example Circuit Schematic

8.2.1 Design Requirements

A typical application requires only four components: an input capacitor, a soft-start capacitor, an output filter capacitor and an output filter inductor. To properly size the components for the application, the designer needs the following parameters: input voltage range, output voltage, output current range, and required switching frequency. These four main parameters affect the choices of component available to achieve a proper system behavior.

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor (C_{IN})

Fast switching of large currents in the buck converter places a heavy demand on the voltage source supplying PVIN. The input capacitor, C_{IN}, supplies extra charge when the switcher needs to draw a burst of current from the supply. The RMS current rating and the voltage rating of the C_{IN} capacitor are therefore important in the selection of C_{IN}. The RMS current specification can be approximated by Equation 1:

$$I_{RMS} = I_{LOAD} \sqrt{D(1-D)} \quad (1)$$

where

- D is the duty cycle, V_{OUT}/V_{IN}. C_{IN} also provides filtering of the supply.

Trace resistance and inductance degrade the benefits of the input capacitor, so C_{IN} must be placed very close to PVIN in the layout. A 22-µF or 47-µF ceramic capacitor is typically sufficient for C_{IN}. In parallel with the large input capacitance a smaller capacitor may be added such as a 1-µF ceramic for higher frequency filtering.

Typical Application (continued)

8.2.2.2 Soft-Start Capacitor (C_{SS})

The DAC that sets the reference voltage of the error amp sources a current through a resistor to set the reference voltage. The reference voltage is one half of the output voltage of the switcher due to the 200 kΩ divider connected to the SNS pin. Upon start-up, the output voltage of the switcher tracks the reference voltage with a two to one ratio as the DAC current charges the capacitance connected to the reference voltage node. Internal capacitance of 20 pF is permanently attached to the reference voltage node which is also connected to the soft-start pin, SS. Adding a soft-start capacitor externally increases the time it takes for the output voltage to reach its final level.

The charging time required for the reference voltage can be estimated using the RC time constant of the DAC resistor and the capacitance connected to the SS pin. Three RC time constant periods are needed for the reference voltage to reach 95% of its final value. The actual start-up time varies with differences in the DAC resistance and higher-order effects.

If little or no soft-start capacitance is connected, then the start-up time may be determined by the time required for the current limit current to charge the output filter capacitance. The capacitor charging equation $I = C\ \Delta V/\Delta t$ can be used to estimate the start-up time in this case. For example, a part with a 3-V output, a 100-µF output capacitance and a 3-A current limit threshold would require a time of 100 µs, seen in Equation 2:

$$\Delta t = C \frac{\Delta V}{I} = 100\ \mu F \frac{3V}{3A} = 100\ \mu s \tag{2}$$

Since it is undesirable for the power supply to start up in current limit, a soft-start capacitor must be chosen to force the LM2852 to start up in a more controlled fashion based on the charging of the soft-start capacitance. In this example, suppose a 3 ms start time is desired. Three time constants are required for charging the soft-start capacitor to 95% of the final reference voltage. So in this case RC = 1 ms. The DAC resistor, R, is 400 kΩ so C can be calculated to be 2.5 nF. A 2.7-nF ceramic capacitor can be chosen to yield approximately a 3 ms start-up time.

8.2.2.3 Soft-Start Capacitor (C_{SS}) and Fault Conditions

Various fault conditions such as short circuit and UVLO of the LM2852 activate internal circuitry designed to control the voltage on the soft-start capacitor. For example, during a short circuit current limit event, the output voltage typically falls to a low voltage. During this time, the soft-start voltage is forced to track the output so that once the short is removed, the LM2852 can restart gracefully from whatever voltage the output reached during the short circuit event. The range of soft-start capacitors is therefore restricted to values 1 nF to 50 nF.

8.2.2.4 Compensation

The LM2852 provides a highly integrated solution to power supply design. The compensation of the LM2852, which is type-three, is included on-chip. The benefit to integrated compensation is straightforward, simple power supply design. Since the output filter capacitor and inductor values impact the compensation of the control loop, the range of L, C and C_{ESR} values is restricted in order to ensure stability.

Typical Application (continued)

8.2.2.5 Output Filter Values

Table 1 details the recommended inductor and capacitor ranges for the LM2852 that are suggested for various typical output voltages. Values slightly different than those recommended may be used, however the phase margin of the power supply may be degraded.

Table 1. Output Filter Values

FREQUENCY OPTION	V_{OUT} (V)	PVIN (V)	L (µH)		C (µF)		C_{ESR} (mΩ)	
			MIN	MAX	MIN	MAX	MIN	MAX
LM2852Y (500 kHz)	0.8	3.3	10	15	100	220	70	200
	0.8	5	10	15	100	120	70	200
	1	3.3	10	15	100	180	70	200
	1	5	10	15	100	180	70	200
	1.2	3.3	10	15	100	180	70	200
	1.2	5	15	22	100	120	70	200
	1.5	3.3	10	15	100	120	70	200
	1.5	5	22	22	100	120	70	200
	1.8	3.3	10	15	100	120	100	200
	1.8	5	22	33	100	120	100	200
	2.5	3.3	6.8	10	68	120	95	275
	2.5	5	15	22	68	120	95	275
	3.3	5	15	22	68	100	100	275
LM2852X (1500 kHz)	0.8	3.3	1		10		The 1500-kHz version is designed for ceramic output capacitors, which typically have very low ESR (< 10 mΩ.)	
	0.8	5						
	1	3.3						
	1	5						
	1.2	3.3						
	1.2	5						
	1.5	3.3						
	1.5	5						
	1.8	3.3						
	1.8	5						
	2.5	3.3						
	2.5	5						
	3.3	5						

8.2.2.6 Choosing an Inductance Value

The current ripple present in the output filter inductor is determined by the input voltage, output voltage, switching frequency and inductance according to Equation 3:

$$\Delta I_L = \frac{D \times (V_{IN} - V_{OUT})}{f \times L} \quad (3)$$

where

- ΔI_L is the peak-to-peak current ripple.
- D is the duty cycle $V_{OUT}/V_{IN.}$
- V_{IN} is the input voltage applied to the PVIN pin.
- V_{OUT} is the output voltage of the switcher.
- f is the switching frequency.
- L is the inductance of the output filter inductor.

Knowing the current ripple is important for inductor selection since the peak current through the inductor is the load current plus one half the ripple current. Care must be taken to ensure the peak inductor current does not reach a level high enough to trip the current limit circuitry of the LM2852.

As an example, consider a 5-V to 1.2-V conversion and a 500-kHz switching frequency. According to Table 1, a 15-µH inductor may be used. Calculating the expected peak-to-peak ripple, as seen in Equation 4.

$$\Delta I_L = \frac{\frac{1.2V}{5V} \times (5V - 1.2V)}{500\ kHz \times 15\ \mu H} = 121.6\ mA \quad (4)$$

The maximum inductor current for a 2-A load would therefore be 2 A plus 60.8 mA, 2.0608 A. As shown in the ripple equation, the current ripple is inversely proportional to inductance.

8.2.2.7 Output Filter Inductors

Once the inductance value is chosen, the key parameter for selecting the output filter inductor is its saturation current (I_{sat}) specification. Typically I_{sat} is given by the manufacturer as the current at which the inductance of the coil falls to a certain percentage of the nominal inductance. The I_{sat} of an inductor used in an application must be greater than the maximum expected inductor current to avoid saturation. Table 2 lists the inductors that may be suitable in LM2852 applications.

Table 2. LM2852 Output Filter Inductors

INDUCTANCE (µH)	PART NUMBER	VENDOR
1	DO1608C-102	Coilcraft
1	DO1813P-102HC	Coilcraft
6.8	DO3316P-682	Coilcraft
7	MSS1038-702NBC	Coilcraft
10	DO3316P-103	Coilcraft
10	MSS1038-103NBC	Coilcraft
12	MSS1038-123NBC	Coilcraft
15	D03316P-153	Coilcraft
15	MSS1038-153NBC	Coilcraft
18	MSS1038-183NBC	Coilcraft
22	DO3316P-223	Coilcraft
22	MSS1038-223NBC	Coilcraft
22	DO3340P-223	Coilcraft
27	MSS1038-273NBC	Coilcraft
33	MSS1038-333NBC	Coilcraft
33	DO3340P-333	Coilcraft

8.2.2.8 Output Filter Capacitors

The capacitors that may be used in the output filter with the LM2852 are limited in value and ESR range according to Table 1. Table 3 lists some examples of capacitors that can typically be used in an LM2852 application.

Table 3. LM2852 Output Filter Capacitors

CAPACITANCE (µF)	PART NUMBER	CHEMISTRY	VENDOR
10	GRM31MR61A106KE19	Ceramic	Murata
10	GRM32DR61E106K	Ceramic	Murata
68	595D686X_010C2T	Tantalum	Vishay - Sprague
68	595D686X_016D2T	Tantalum	Vishay - Sprague
100	595D107X_6R3C2T	Tantalum	Vishay - Sprague
100	595D107X_016D2T	Tantalum	Vishay - Sprague
100	NOSC107M004R0150	Niobium Oxide	AVX
100	NOSD107M006R0100	Niobium Oxide	AVX
120	595D127X_004C2T	Tantalum	Vishay - Sprague
120	595D127X_010D2T	Tantalum	Vishay - Sprague
150	595D157X_004C2T	Tantalum	Vishay - Sprague
150	595D157X_016D2T	Tantalum	Vishay - Sprague
150	NOSC157M004R0150	Niobium Oxide	AVX
150	NOSD157M006R0100	Niobium Oxide	AVX
220	595D227X_004D2T	Tantalum	Vishay - Sprague
220	NOSD227M004R0100	Niobium Oxide	AVX
220	NOSE227M006R0100	Niobium Oxide	AVX

Table 4. Bill of Materials for 500kHz (LM2852Y) 3.3 V_{IN} to 1.8 V_{OUT} Conversion

ID	PART NUMBER	TYPE	SIZE	PARAMETERS	QTY	VENDOR
U_1	LM2852YMXA-1.8	2-A buck	HTSSOP-14		1	TI
L_O	DO3316P-153	Inductor		15 µH	1	Coilcraft
C_O*	595D107X_6R3C2T	Capacitor	Case Code “C”	100 µF ±20%	1	Vishay-Sprague
C_{IN}	GRM32ER60J476ME20B	Capacitor	1210	47 µF/X5R/6.3V	1	Murata
C_{INX}	GRM21BR71C105KA01B	Capacitor	0805	1 µF/X7R/16V	1	Murata
C_{SS}	VJ0805Y272KXXA	Capacitor	0805	2.7 nF ±10%	1	Vishay-Vitramon
R_f	CRCW060310R0F	Resistor	0603	10 Ω ±10%	1	Vishay-Dale
C_f	GRM21BR71C105KA01B	Capacitor	0805	1 µF/X7R/16V	1	Murata

Table 5. Bill of Materials for 1500-kHz (LM2852X) 3.3-V to 1.8-V Conversion

ID	PART NUMBER	TYPE	SIZE	PARAMETERS	QTY	VENDOR
U_1	LM2852XMXA-1.8	2-A buck	HTSSOP-14		1	TI
L_0	DO1813P-102HC	Inductor		1 µH	1	Coilcraft
C_0	GRM32DR61E106K	Capacitor	1210	10 µF/X5R/25V	1	Murata
C_{IN}	GRM32ER60J476ME20B	Capacitor	1210	47 µF/X5R/6.3V	1	Murata
C_{INX}	GRM21BR71C105KA01B	Capacitor	0805	1 µF/X7R/16V	1	Murata
C_{SS}	VJ0805Y272KXXA	Capacitor	0805	2.7 nF ±10%	1	Vishay-Vitramon
R_f	CRCW060310R0F	Resistor	0603	10 Ω ±10%	1	Vishay-Dale
C_f	GRM21BR71C105KA01B	Capacitor	0805	1 µF/X7R/16V	1	Murata

8.2.3 Application Curves

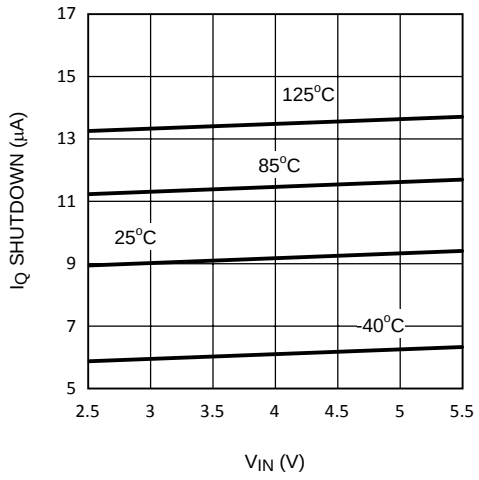


Figure 14. Shutdown Current vs V_{IN}

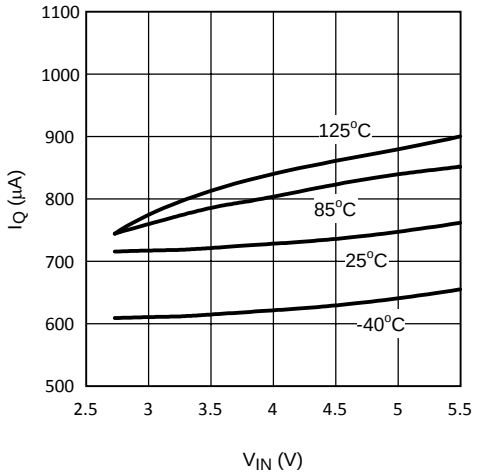


Figure 15. Quiescent Current (Non-Switching) vs V_{IN}

9 Power Supply Recommendations

The LM2852 is designed to operate from various DC power supplies. If so, VIN input must be protected from reversal voltage and voltage dump over 6.5 V. The impedance of the input supply rail must be low enough that the input current transient does not cause drop below VIN UVLO level. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to normal input capacitor.

10 Layout

10.1 Layout Guidelines

These are several guidelines to follow while designing the PCB layout for an LM2852 application.

- The input bulk capacitor, C_{IN}, must be placed very close to the PVIN pin to keep the resistance as low as possible between the capacitor and the pin. High-current levels are present in this connection
- All ground connections must be tied together. Use a broad ground plane, for example a completely filled back plane, to establish the lowest resistance possible between all ground connections
- The sense pin connection must be made as close to the load as possible so that the voltage at the load is the expected regulated value. The sense line must not run too close to nodes with high EMI (such as the switch node) to minimize interference
- The switch node connections must be low resistance to reduce power losses. Low resistance means the trace between the switch pin and the inductor must be wide. However, the area of the switch node must not be too large since EMI increases with greater area. So connect the inductor to the switch pin with a short, but wide trace. Other high current connections in the application such as PVIN and V_{OUT} assume the same trade off between low resistance and EMI
- Allow area under the chip to solder the entire exposed die attach pad to ground for improved thermal and electrical performance

10.2 Layout Example

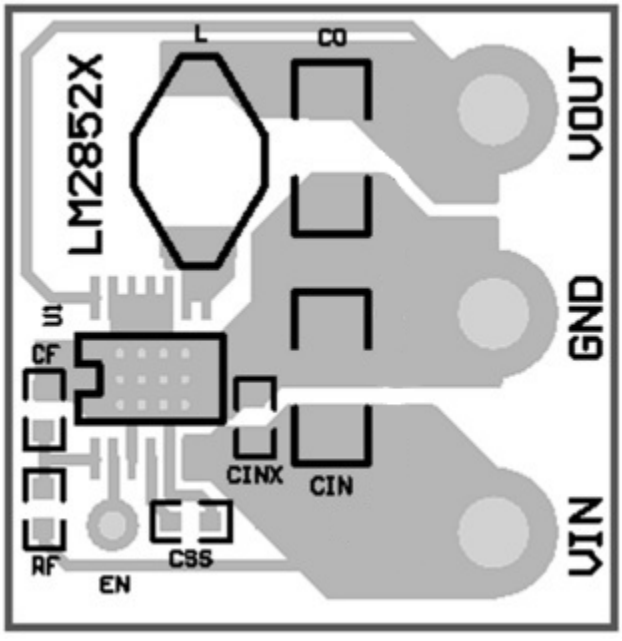


Figure 16. PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2852XMXA-1.0/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852X 1.0	Samples
LM2852XMXA-1.2/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852X 1.2	Samples
LM2852XMXA-1.5/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852X 1.5	Samples
LM2852XMXA-1.8/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852X 1.8	Samples
LM2852XMXA-2.5/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852X 2.5	Samples
LM2852XMXA-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852X 3.3	Samples
LM2852XMXAX-1.2/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852X 1.2	Samples
LM2852XMXAX-1.5/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852X 1.5	Samples
LM2852XMXAX-1.8/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852X 1.8	Samples
LM2852XMXAX-2.5/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852X 2.5	Samples
LM2852XMXAX-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852X 3.3	Samples
LM2852YMXA-1.0/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y -1.0	Samples
LM2852YMXA-1.2/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y -1.2	Samples
LM2852YMXA-1.3/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM		2852Y 1.3	Samples
LM2852YMXA-1.5/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y -1.5	Samples
LM2852YMXA-1.8/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y -1.8	Samples
LM2852YMXA-2.5/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										-2.5	
LM2852YMXA-3.3	LIFEBUY	HTSSOP	PWP	14	94	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	2852Y -3.3	
LM2852YMXA-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y -3.3	Samples
LM2852YMXAX-1.0/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y -1.0	Samples
LM2852YMXAX-1.2/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y -1.2	Samples
LM2852YMXAX-1.5/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y -1.5	Samples
LM2852YMXAX-1.8/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y -1.8	Samples
LM2852YMXAX-2.5/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y -2.5	Samples
LM2852YMXAX-3.3/NOPB	ACTIVE	HTSSOP	PWP	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2852Y -3.3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

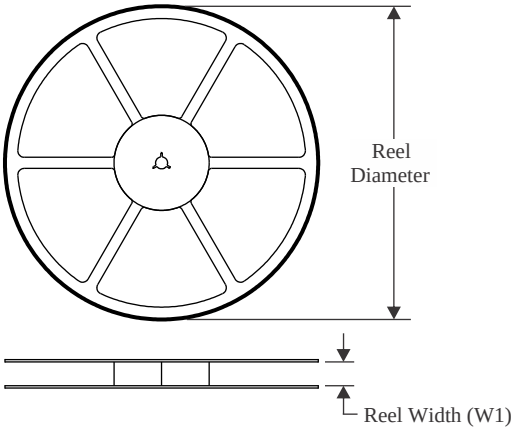
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

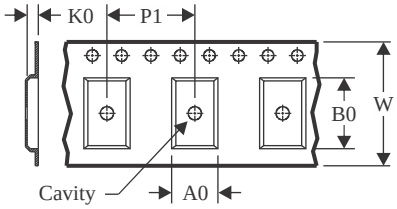
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

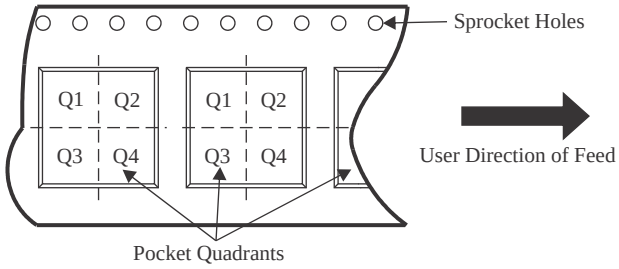


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

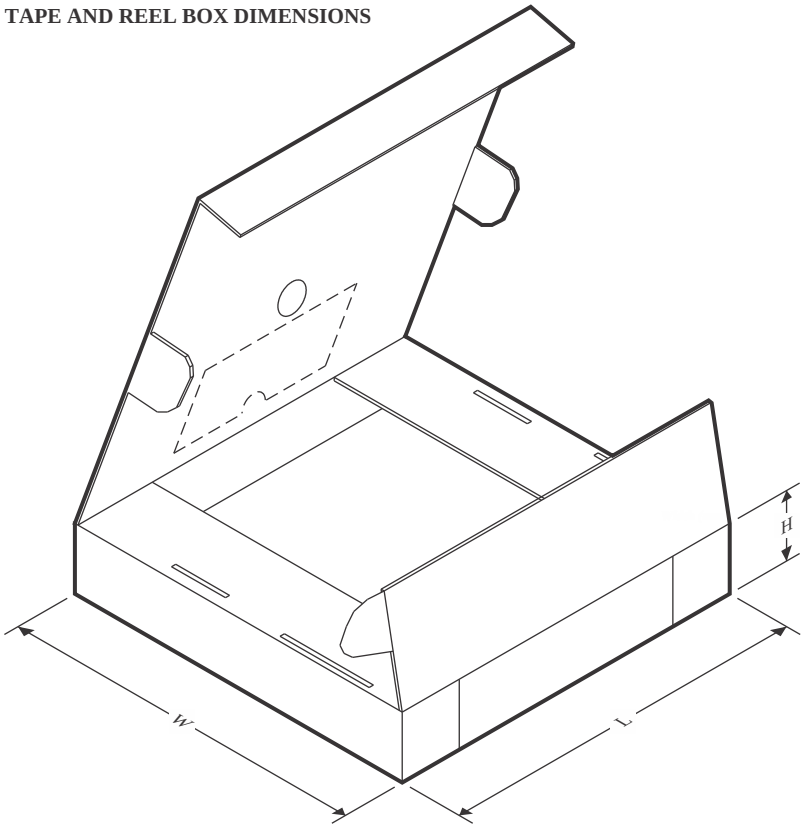


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2852XMXAX-1.2/ NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM2852XMXAX-1.5/ NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM2852XMXAX-1.8/ NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM2852XMXAX-2.5/ NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM2852XMXAX-3.3/ NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM2852YMXAX-1.0/ NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM2852YMXAX-1.2/ NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM2852YMXAX-1.5/ NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM2852YMXAX-1.8/ NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2852YMXAX-2.5/ NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM2852YMXAX-3.3/ NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

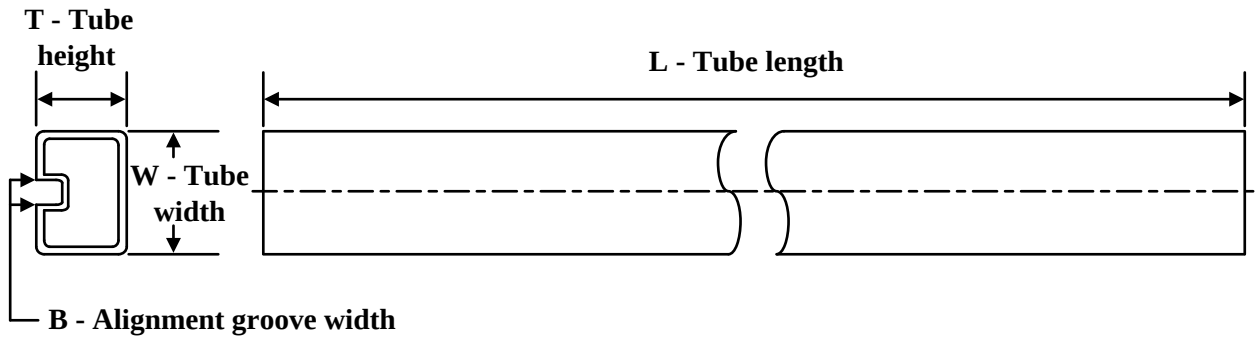
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

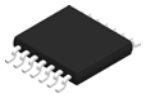
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2852XMXAX-1.2/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM2852XMXAX-1.5/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM2852XMXAX-1.8/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM2852XMXAX-2.5/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM2852XMXAX-3.3/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM2852YMXAX-1.0/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM2852YMXAX-1.2/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM2852YMXAX-1.5/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM2852YMXAX-1.8/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM2852YMXAX-2.5/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM2852YMXAX-3.3/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2852XMXA-1.0/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852XMXA-1.2/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852XMXA-1.5/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852XMXA-1.8/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852XMXA-2.5/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852XMXA-3.3/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852YMXA-1.0/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852YMXA-1.2/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852YMXA-1.3/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852YMXA-1.5/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852YMXA-1.8/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852YMXA-2.5/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852YMXA-3.3	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852YMXA-3.3	PWP	HTSSOP	14	94	495	8	2514.6	4.06
LM2852YMXA-3.3/NOPB	PWP	HTSSOP	14	94	495	8	2514.6	4.06

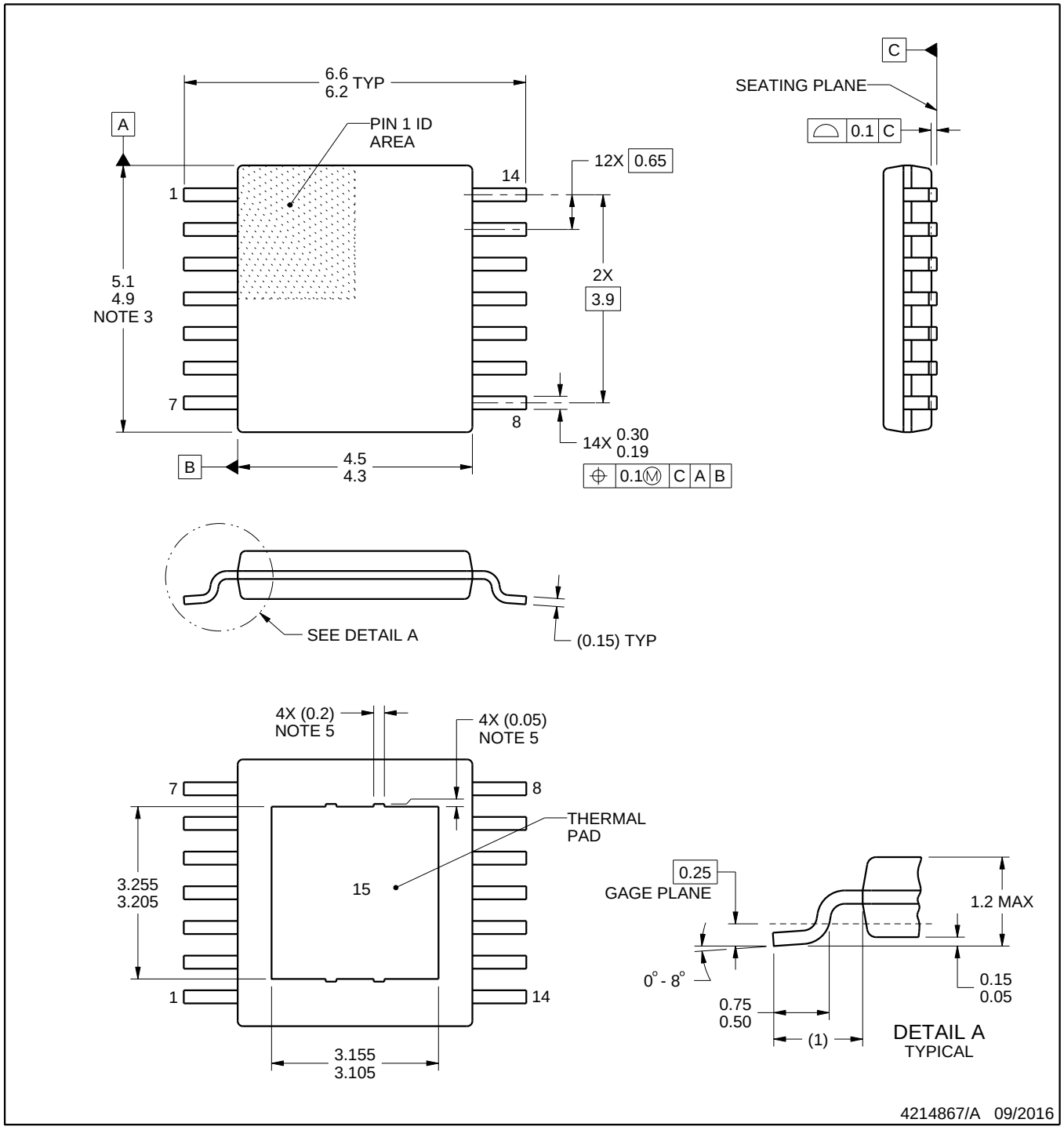


PACKAGE OUTLINE

PWP0014A

PowerPAD™ TSSOP - 1.2 mm max height

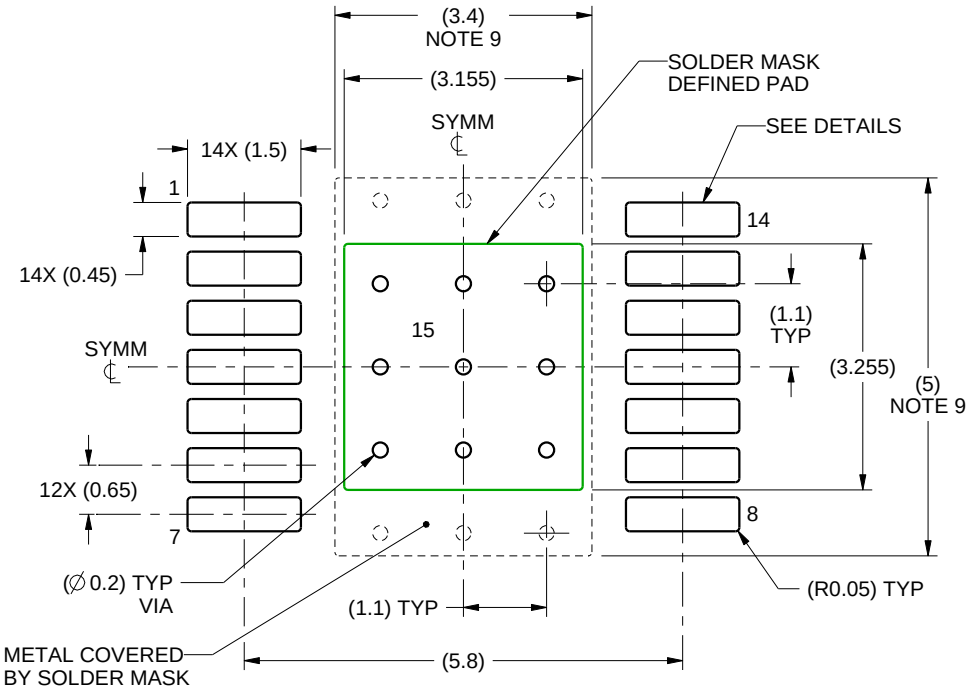
PLASTIC SMALL OUTLINE



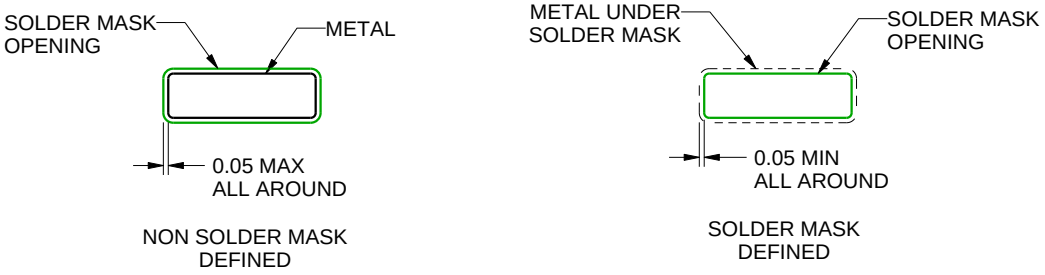
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

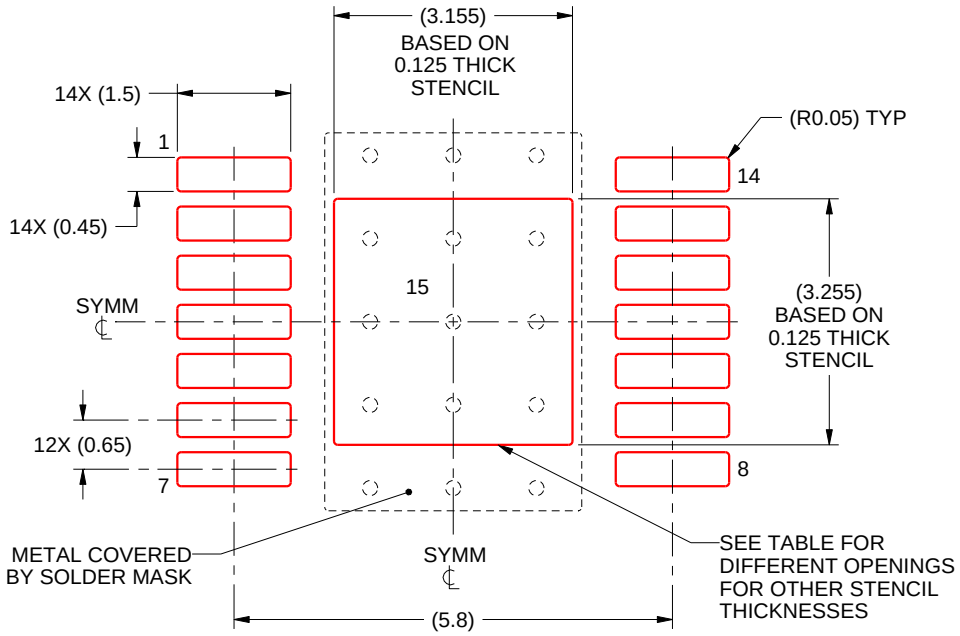


SOLDER MASK DETAILS
PADS 1-14

4214867/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.53 X 3.64
0.125	3.155 X 3.255 (SHOWN)
0.15	2.88 X 2.97
0.175	2.67 X 2.75

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265