AMC3311 Precision, 2-V Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter

1 Features

- Single-supply operation (3.3 V or 5 V) with integrated DC/DC converter
- Input voltage range (2 V) optimized for voltage measurements with high input impedance
- Fixed gain: 1.0
- Low DC errors:
  - Offset error: ±1 mV (max)
  - Offset drift: ±10 µV/°C (max)
  - Gain error: ±0.2% (max)
  - Gain drift: ±40 ppm/°C (max)
  - Nonlinearity: ±0.02% (max)
- High CMTI: 85 kV/µs (min)
- System-level diagnostic features
- Meets CISPR-11 and CISPR-25 EMI standards
- Safety-related certifications:
  - 6000-V_{PK} reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 4250-V_{RMS} isolation for 1 minute per UL1577
- Fully specified over the extended industrial temperature range: –40°C to +125°C

2 Applications

- Isolated DC voltage sensing in:
  - Motor drives
  - Photovoltaic inverters
  - Server power-supply units (PSU)
  - DC charging stations

3 Description

The AMC3311 is a precision, isolated amplifier with a fully integrated, isolated DC/DC converter that allows single-supply operation from the low-side of the device. The reinforced capacitive isolation barrier is highly resistant to magnetic interference, is certified according to DIN EN IEC 60747-17 (VDE 0884-17) and UL1577, and supports a working voltage of up to 1200 V_{RMS}.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from voltage levels that can cause electrical damage and are potentially harmful to an operator.

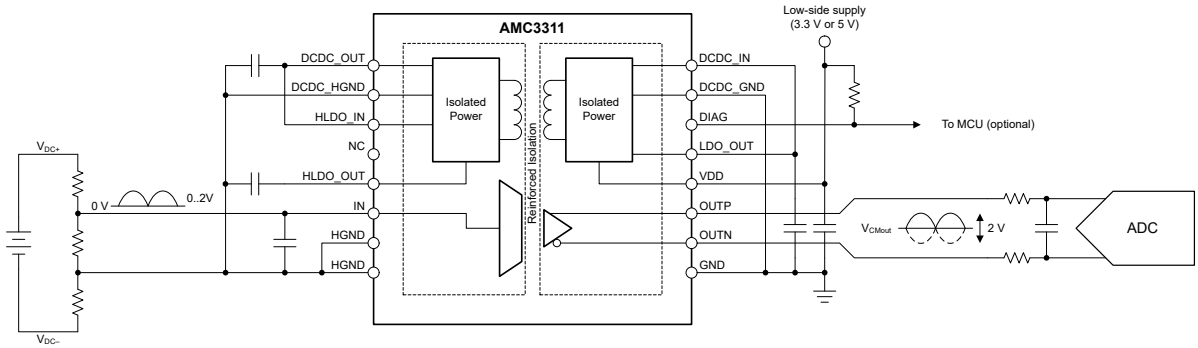
The input of the AMC3311 is optimized for direct connection to high-impedance resistive dividers that are typically used for sensing high voltages. The integrated isolated DC/DC converter allows measurement of non-ground-referenced signals and makes the device a unique solution for noisy, space-constrained applications. The high DC accuracy and low temperature drift support accurate voltage monitoring and control.

The AMC3311 is offered in a wide-body, 16-pin SOIC package, and is specified over the temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AMC3311	DWE (SOIC, 16)	10.3 mm × 10.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Example

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2023) to Revision A (August 2023)	Page
• Changed document status from *Advance Information* to *Production Data*	1

5 Pin Configuration and Functions

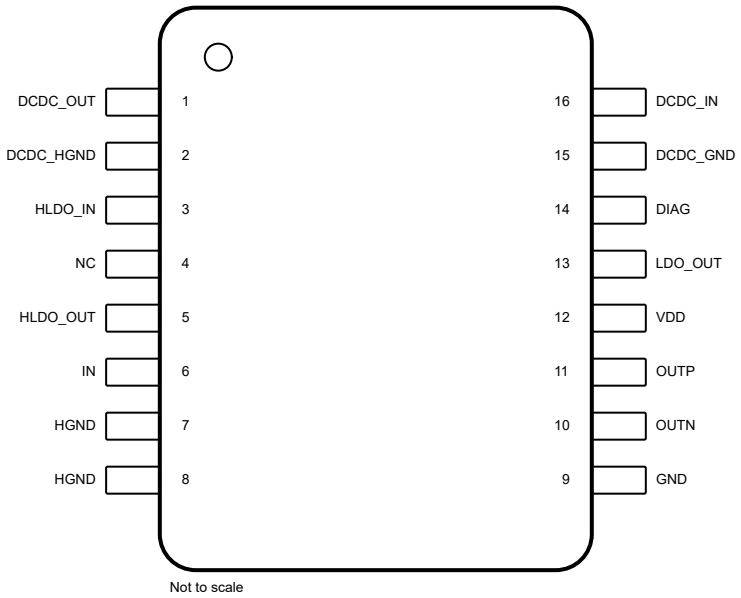


Figure 5-1. DWE Package, 16-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	DCDC_OUT	Power	High-side output of the isolated DC/DC converter; connect this pin to the HLDO_IN pin.(1)
2	DCDC_HGND	Power ground	High-side ground reference for the isolated DC/DC converter; connect this pin to the HGND pin.
3	HLDO_IN	Power	Input of the high-side low-dropout (LDO) regulator; connect this pin to the DCDC_OUT pin.(1)
4	NC	—	No internal connection. Connect this pin to the high-side ground or leave this pin unconnected (floating).
5	HLDO_OUT	Power	Output of the high-side LDO.(1)
6	IN	Analog input	Analog input.
7, 8	HGND	Signal ground	High-side analog ground; connect both pins to the DCDC_HGND pin.
9	GND	Signal ground	Low-side analog ground; connect this pin to the DCDC_GND pin.
10	OUTN	Analog output	Inverting analog output.
11	OUTP	Analog output	Noninverting analog output.
12	VDD	Power	Low-side power supply.(1)
13	LDO_OUT	Power	Output of the low-side LDO; connect this pin to the DCDC_IN pin.(1)
14	DIAG	Digital output	Active-low, open-drain status indicator output; connect this pin to the pullup supply (for example, VDD) using a resistor or leave this pin floating if not used.
15	DCDC_GND	Power ground	Low-side ground reference for the isolated DC/DC converter; connect this pin to the GND pin.
16	DCDC_IN	Power	Low-side input of the isolated DC/DC converter; connect this pin to the LDO_OUT pin.(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	6.5	V
Analog input voltage	IN	HGND – 6	V_{HLDO_OUT} + 0.5	V
Analog output voltage	OUTP, OUTN	GND – 0.5	VDD + 0.5	V
Digital output voltage	DIAG	GND – 0.5	6.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD	Low-side supply voltage	VDD to GND	3.0	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Input voltage before clipping output	IN to HGND		2.516		V
V_{FSR}	Specified linear full-scale voltage	IN to HGND	–0.1		2	V
ANALOG OUTPUT						
C_{LOAD}	Capactive load	On OUTP or OUTN to GND			500	pF
		OUTP to OUTN			250	
R_{LOAD}	Resistive load	On OUTP or OUTN to GND		10	1	kΩ
DIGITAL OUTPUT						
	Pull-up supply-voltage for DIAG pin		0		VDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		DWE (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation	VDD = 5.5 V			236.5	mW
		VDD = 3.6 V			155	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance - capacitive signal isolation)	≥ 21	µm
DTI	Distance through insulation	Minimum internal gap (internal clearance - transformer power isolation)	≥ 120	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1700	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1200	V_{RMS}
		At DC voltage	1700	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	6000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
		Method b2, at routine test (100% production)(7), $V_{pd(ini)} = V_{pd(m)} = 1.2 \times V_{IOTM}$, $t_{ini} = t_m$ = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5 V_{PP} at 1 MHz	~4.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	4250	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

6.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs.
Reinforced insulation	Single protection
Certificate number: pending	File number: pending

6.8 Safety Limiting Values

Safety limiting (1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 73.5°C/W, VDD = 5.5 V, T_J = 150°C, T_A = 25°C			309	mA
		$R_{\theta JA}$ = 73.5°C/W, VDD = 3.6 V, T_J = 150°C, T_A = 25°C			472	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 73.5°C/W, T_J = 150°C, T_A = 25°C			1700	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum low-side voltage.

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, and IN = –0.1 V to 2 V; typical specifications are at T_A = 25°C, and VDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
R_{IN}	Input resistance	T_A = 25°C		1		GΩ
I_{IB}	Input bias current	IN = HGND, T_A = 25°C	–15	3.5	15	nA
TCI_{IB}	Input bias current drift(1)			±12		pA/°C
C_{IN}	Input capacitance	f_{IN} = 275 kHz		7		pF
ANALOG OUTPUT						
	Nominal gain			1		V/V
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	V_{OUT} = (V_{OUTP} – V_{OUTN}); V_{IN} > $V_{Clipping}$		2.49		V
$V_{FAILSAFE}$	Failsafe differential output voltage	V_{OUT} = (V_{OUTP} – V_{OUTN}); V_{DCDC_OUT} ≤ V_{DCDCUV}, or V_{HLDO_OUT} ≤ V_{HLDOUV}		–2.6	–2.5	V
BW	Output bandwidth		220	275		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, IN = HGND, outputs shorted to either GND or VDD		14		mA
CMTI	Common-mode transient immunity		85	135		kV/µs
ACCURACY						
V_{OS}	Input offset voltage(1) (2)	T_A = 25°C, IN = HGND	–1	±0.1	1	mV
TCV_{OS}	Input offset thermal drift(1) (2) (4)		–10	±3	10	µV/°C
E_G	Gain error	T_A = 25°C	–0.2%	±0.05%	0.2%	
TCE_G	Gain error drift(1) (5)		–40	±5	40	ppm/°C
	Nonlinearity		–0.02%	±0.01%	0.02%	
	Nonlinearity thermal drift			1		ppm/°C
SNR	Signal-to-noise ratio	V_{IN} = 2 V_{PP}, V_{IN} > 0 V, f_{IN} = 1 kHz, BW = 10 kHz, 10 kHz filter	75.5	78.4		dB
		V_{IN} = 2 V_{PP}, V_{IN} > 0 V, f_{IN} = 10 kHz, BW = 100 kHz, 1 MHz filter		67.5		
THD	Total harmonic distortion(3)	V_{IN} = 2 Vpp, V_{IN} > 0 V, f_{IN} = 10 kHz, BW = 100 kHz		–80.6		dB
	Output noise	IN = HGND, BW = 100 kHz		250		$µV_{RMS}$
PSRR	Power-supply rejection ratio(2)	VDD from 3.0 V to 5.5 V, at DC		–85		dB
		IN = HGND, VDD from 3.0 V to 5.5 V, 10-kHz, 100-mV ripple		–70		

6.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, and IN = –0.1 V to 2 V; typical specifications are at T_A = 25°C, and VDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
IDD	Low-side supply current	No external load on HLDO		28.5	41	mA
		4 mA external load on HLDO		36.5	49	mA
VDD_{UV}	VDD analog undervoltage detection threshold	VDD rising			2.9	V
		VDD falling			2.8	
VDD_{POR}	VDD digital reset threshold	VDD rising			2.5	V
		VDD falling			2.4	
V_{DCDC_OUT}	DC/DC output voltage	DCDC_OUT to HGND	3.1	3.4	4.65	V
V_{DCDCUV}	DC/DC output undervoltage detection threshold voltage	DCDC output falling	2.1	2.25		V
V_{HLDO_OUT}	High-side LDO output voltage	HLDO to HGND, no external load	3	3.2	3.4	V
		HLDO to HGND, 4 mA external load, V_{DD} > 3.6 V	3	3.2	3.4	
V_{HLDOUV}	High-side LDO output undervoltage detection threshold voltage	HLDO output falling	2.4	2.6		V
I_H	High-side supply current for auxiliary circuitry	3 V ≤ VDD < 3.6 V, load connected from HLDO_OUT to HGND, non-switching			1	mA
		3.6 V ≤ VDD ≤ 5.5 V, load connected from HLDO_OUT to HGND, non-switching			4.0	
t_{AS}	Analog settling time	VDD step to 3.0 V, to OUTP and OUTN valid, 0.1% settling		0.6	1.1	ms

(1) The typical value includes one standard deviation ("sigma") at nominal operating conditons.
(2) This parameter is input referred.
(3) THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation: $TCV_{OS} = (V_{OS,MAX} - V_{OS,MIN}) / TempRange$ where $V_{OS,MAX}$ and $V_{OS,MIN}$ refer to the maximum and minimum V_{OS} values measured within the temperature range (–40 to 125°C).
(5) Gain error temperature drift is calculated using the box method, as described by the following equation: $TCE_G\ (ppm) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125°C).

6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.3		µs
t_f	Output signal fall time			1.3		µs
	V_{IN} to V_{OUTx} signal delay (50% – 10%)	Unfiltered output		1.0	1.5	µs
	V_{IN} to V_{OUTx} signal delay (50% – 50%)	Unfiltered output		1.6	2.1	µs
	V_{IN} to V_{OUTx} signal delay (50% – 90%)	Unfiltered output		2.5	3.0	µs

6.11 Timing Diagram

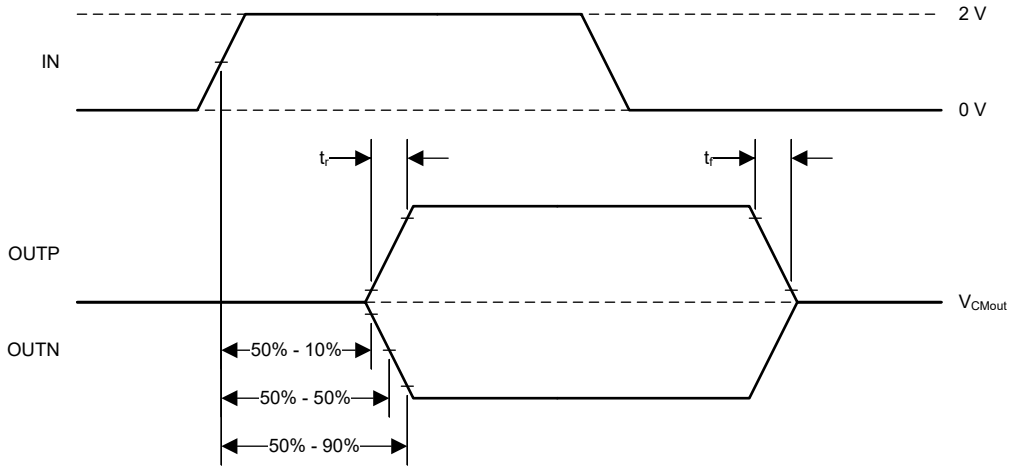


Figure 6-1. Rise, Fall, and Delay Time Waveforms

6.12 Insulation Characteristics Curves

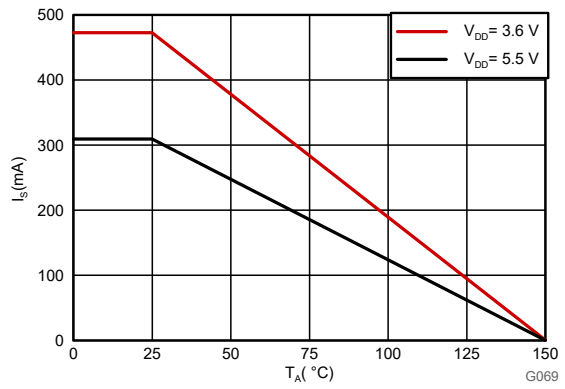


Figure 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE

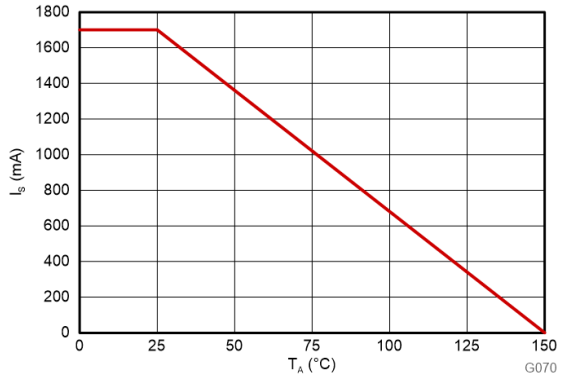
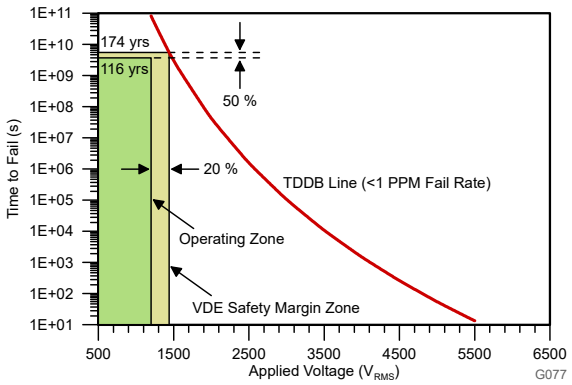


Figure 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE



V_{IOWM} = 1200 V_{RMS}, f = 60 Hz, T_A ≤ 150°C

Figure 6-4. Reinforced Isolation Capacitor Lifetime Projection

6.13 Typical Characteristics

at VDD = 3.3 V, IN = 0 V to 2 V, and f_{IN} = 10 kHz (unless otherwise noted)

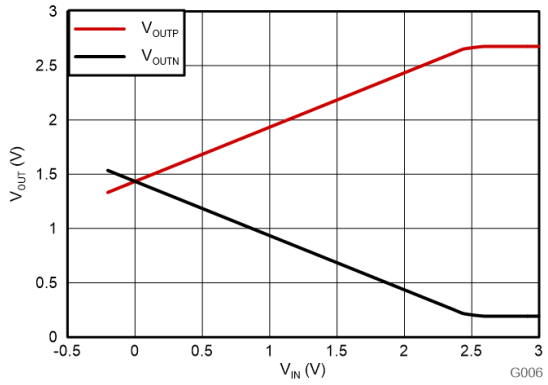
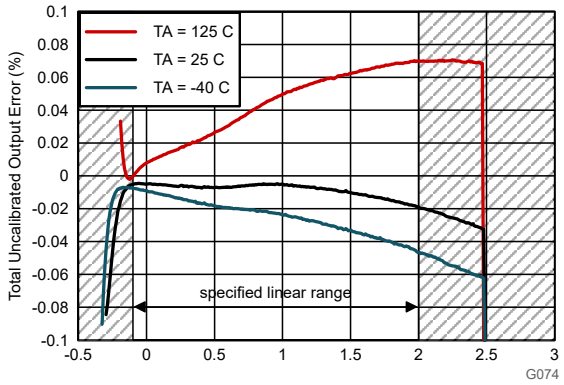


Figure 6-5. Output Voltage vs Input Voltage



Total uncalibrated output error is defined as:
$(V_{OUT} – V_{IN} × G) / (V_{Clipping} × G)$, where G is the nominal gain of the device (1 V/V) and $V_{Clipping}$ is 2.516 V

Figure 6-6. Total Uncalibrated Output Error vs Input Voltage

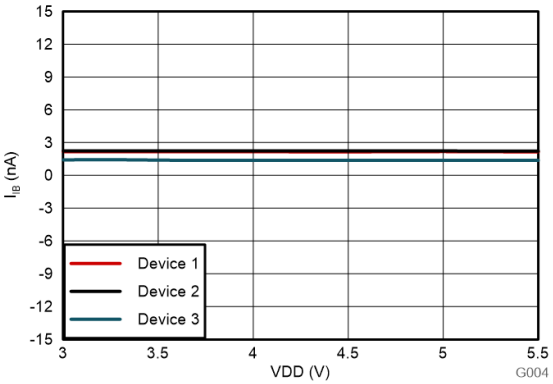


Figure 6-7. Input Bias Current vs Supply Voltage

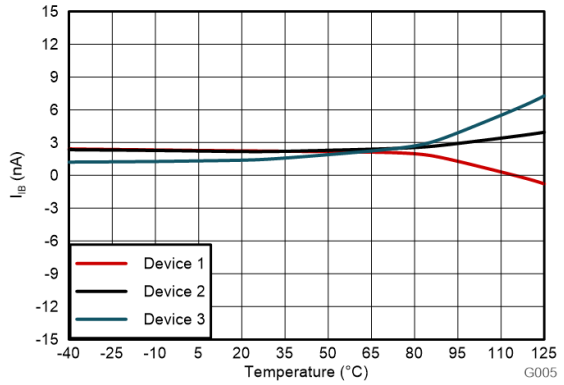


Figure 6-8. Input Bias Current vs Temperature

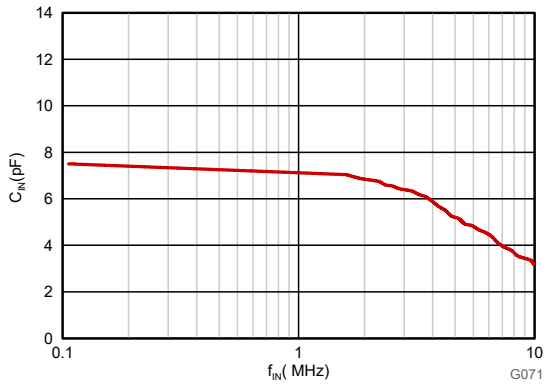


Figure 6-9. Input Capacitance vs Input Signal Frequency

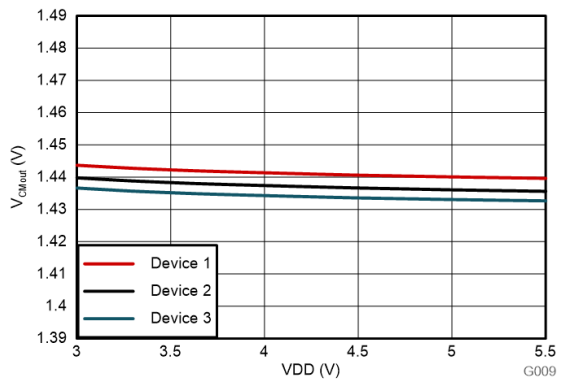


Figure 6-10. Output Common-Mode Voltage vs Supply Voltage

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, IN = 0 V to 2 V, and f_{IN} = 10 kHz (unless otherwise noted)

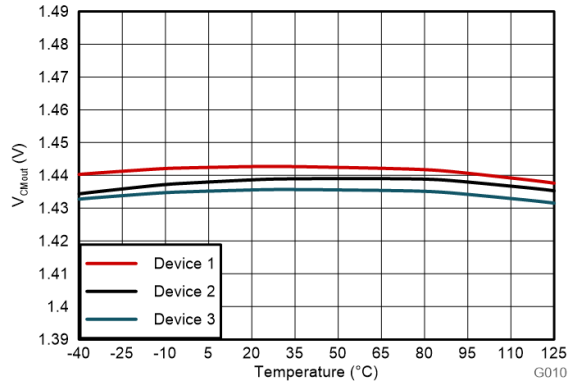


Figure 6-11. Output Common-Mode Voltage vs Temperature

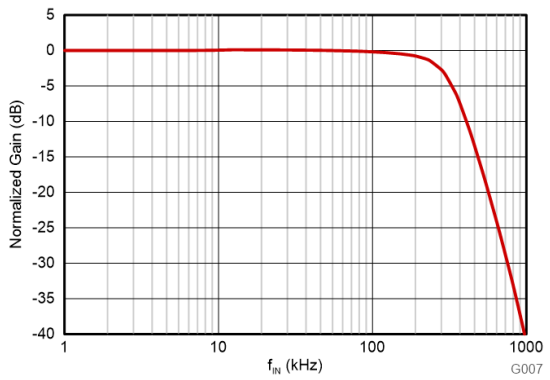


Figure 6-12. Normalized Gain vs Input Frequency

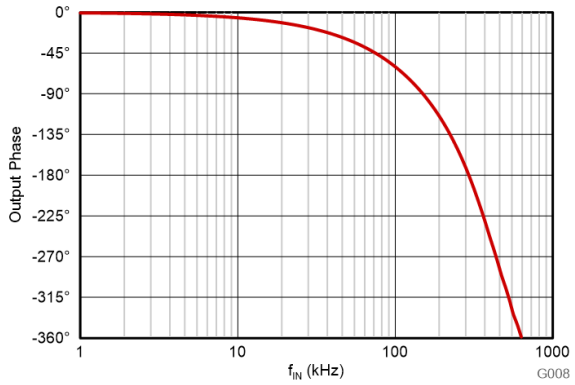


Figure 6-13. Output Phase vs Input Frequency

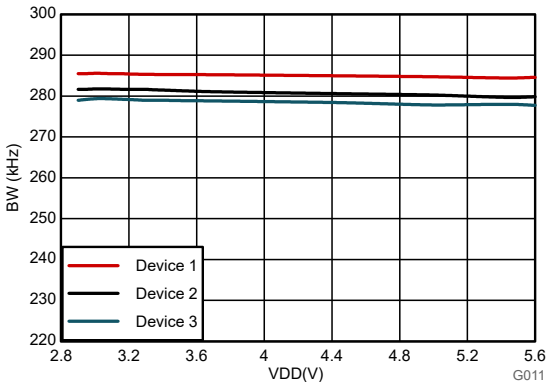


Figure 6-14. Output Bandwidth vs Supply Voltage

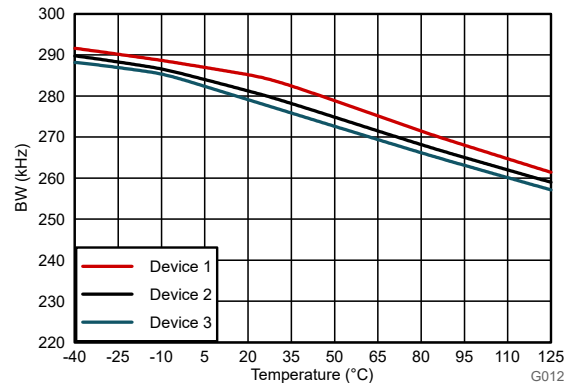


Figure 6-15. Output Bandwidth vs Temperature

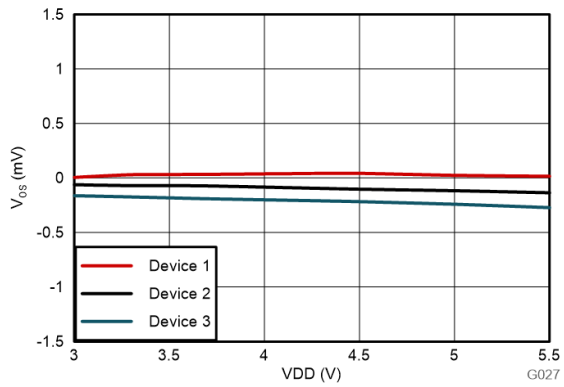


Figure 6-16. Offset Error vs Supply Voltage

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, IN = 0 V to 2 V, and f_{IN} = 10 kHz (unless otherwise noted)

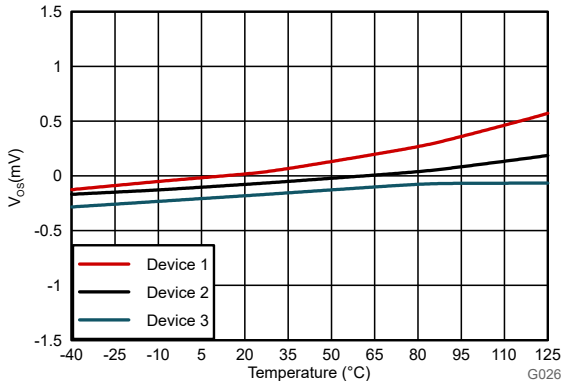


Figure 6-17. Offset Error vs Temperature

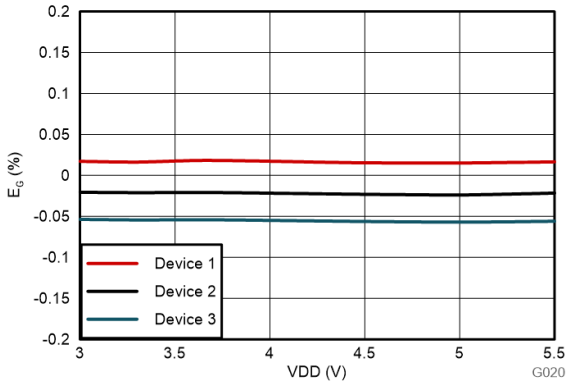


Figure 6-18. Gain Error vs Supply Voltage

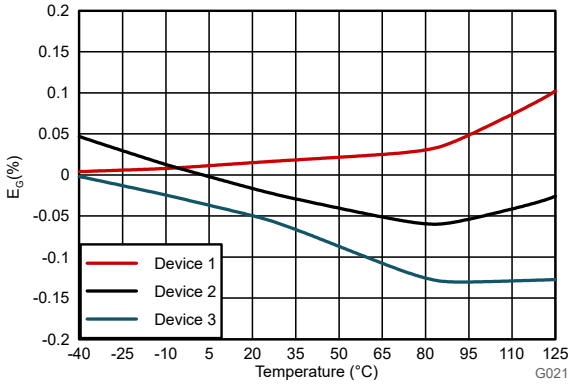


Figure 6-19. Gain Error vs Temperature

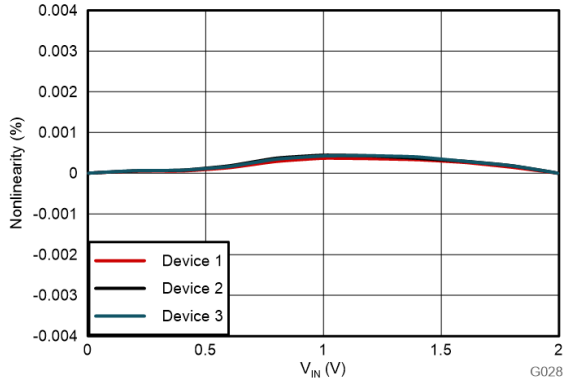


Figure 6-20. Nonlinearity vs Input Voltage

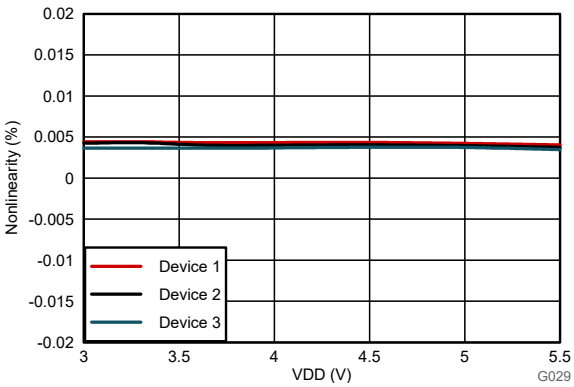


Figure 6-21. Nonlinearity vs Supply Voltage

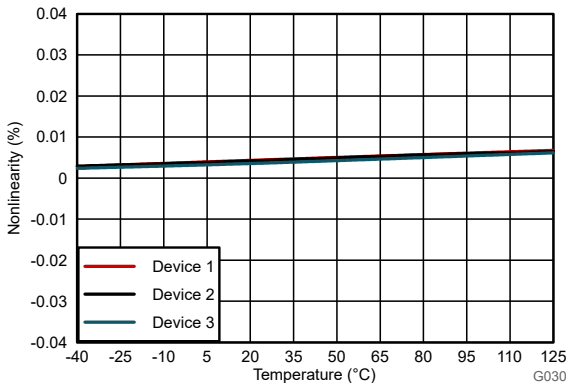


Figure 6-22. Nonlinearity vs Temperature

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, IN = 0 V to 2 V, and f_{IN} = 10 kHz (unless otherwise noted)

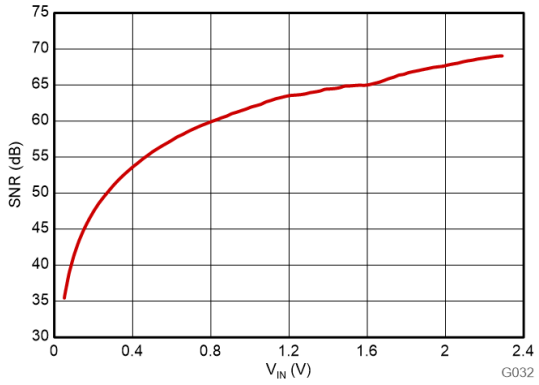
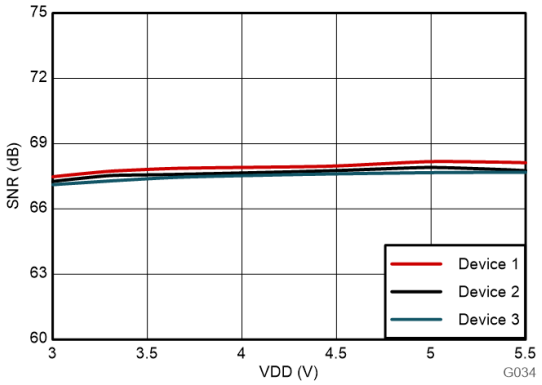
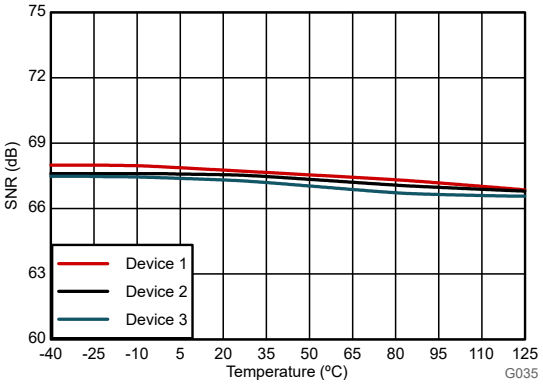


Figure 6-23. Signal to Noise Ratio vs Input Voltage



V_{IN} = 2 V

Figure 6-24. Signal-to-Noise Ratio vs Supply Voltage



V_{IN} = 2 V

Figure 6-25. Signal-to-Noise Ratio vs Temperature

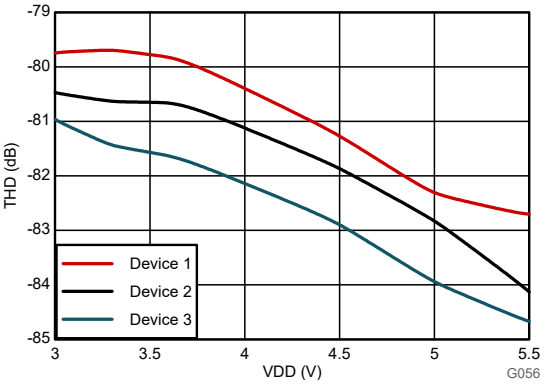


Figure 6-26. Total Harmonic Distortion vs Supply Voltage

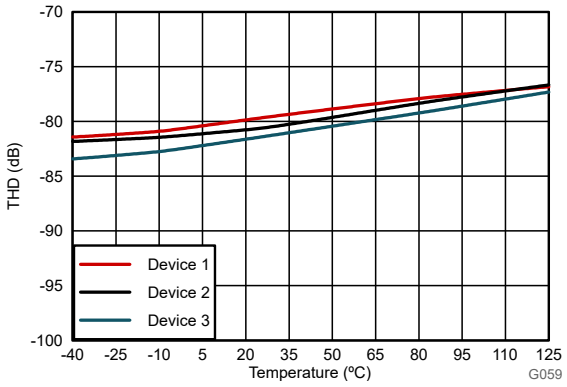


Figure 6-27. Total Harmonic Distortion vs Temperature

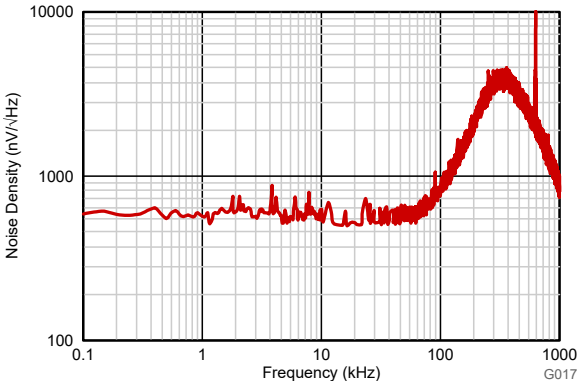


Figure 6-28. Input-Referred Noise Density vs Frequency

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, IN = 0 V to 2 V, and f_{IN} = 10 kHz (unless otherwise noted)

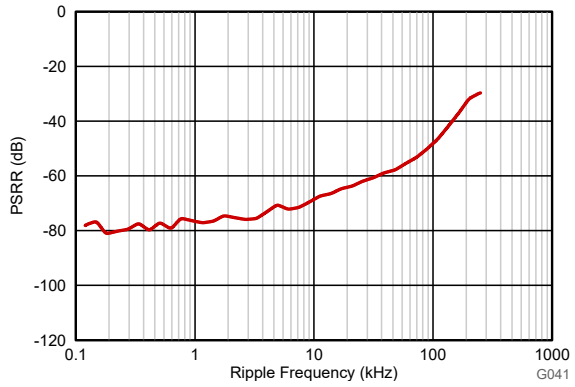


Figure 6-29. Power-Supply Rejection Ratio vs Ripple Frequency

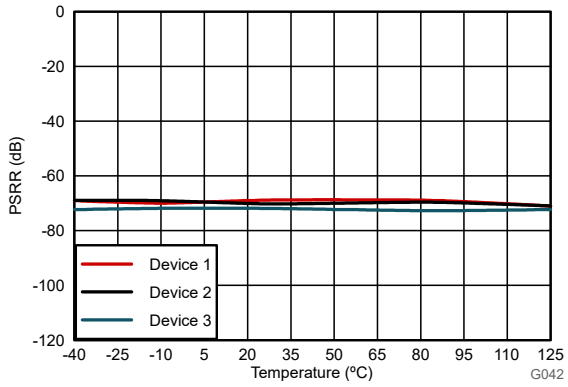


Figure 6-30. Power-Supply Rejection Ratio vs Temperature

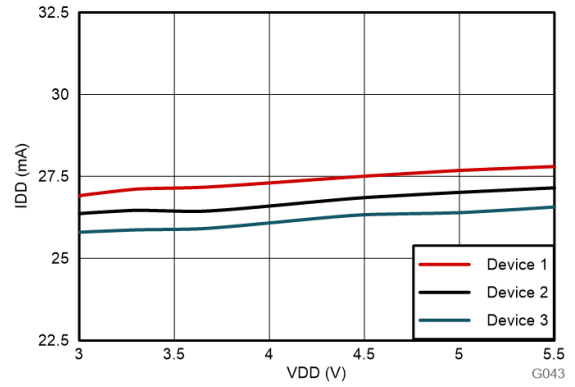


Figure 6-31. Input Supply Current vs Supply Voltage

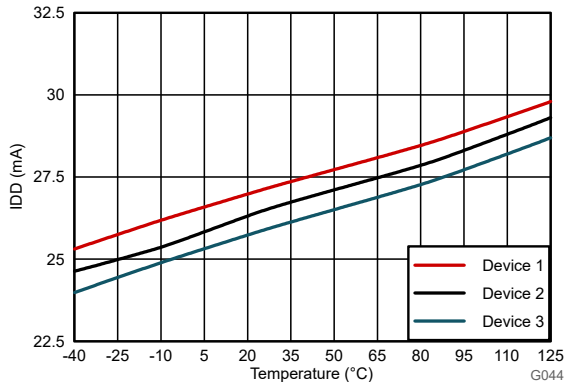


Figure 6-32. Input Supply Current vs Temperature

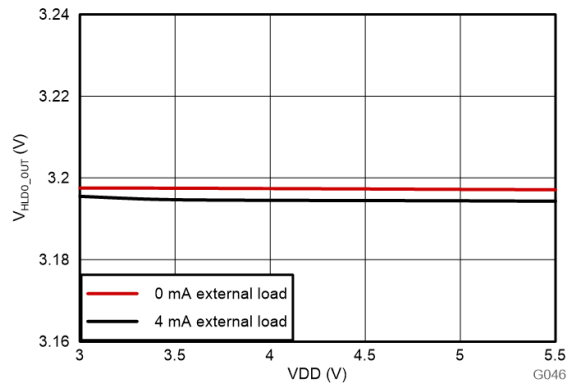


Figure 6-33. High-Side LDO Line Regulation

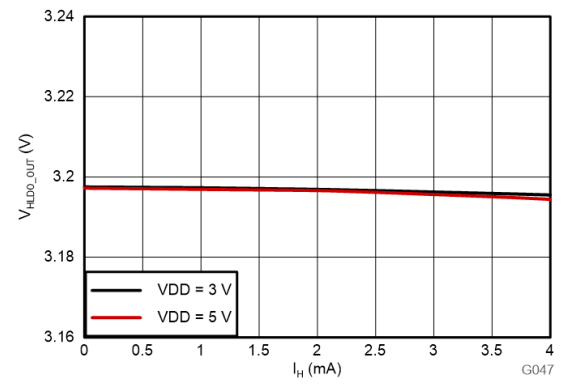


Figure 6-34. High-Side LDO Load Regulation

6.13 Typical Characteristics (continued)

at VDD = 3.3 V, IN = 0 V to 2 V, and f_{IN} = 10 kHz (unless otherwise noted)

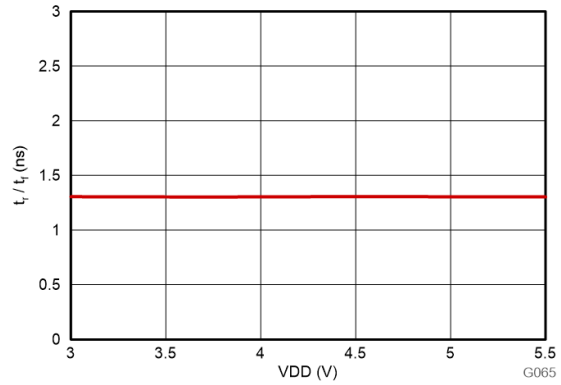


Figure 6-35. Output Rise and Fall Time vs Supply Voltage

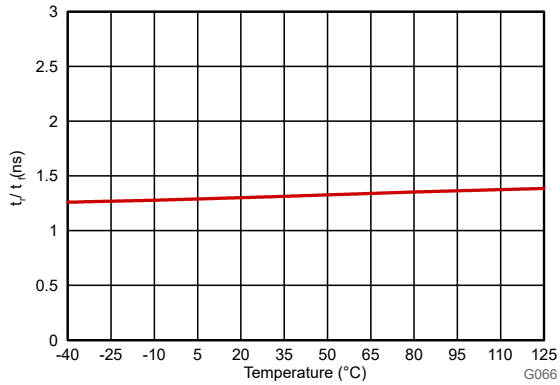


Figure 6-36. Output Rise and Fall Time vs Temperature

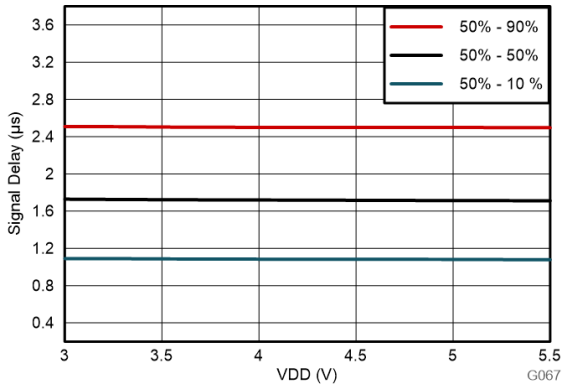


Figure 6-37. V_{IN} to V_{OUT} Signal Delay Time vs Supply Voltage

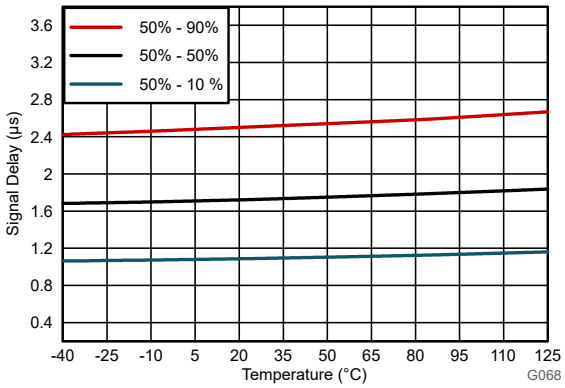


Figure 6-38. V_{IN} to V_{OUT} Signal Delay Time vs Temperature

7 Detailed Description

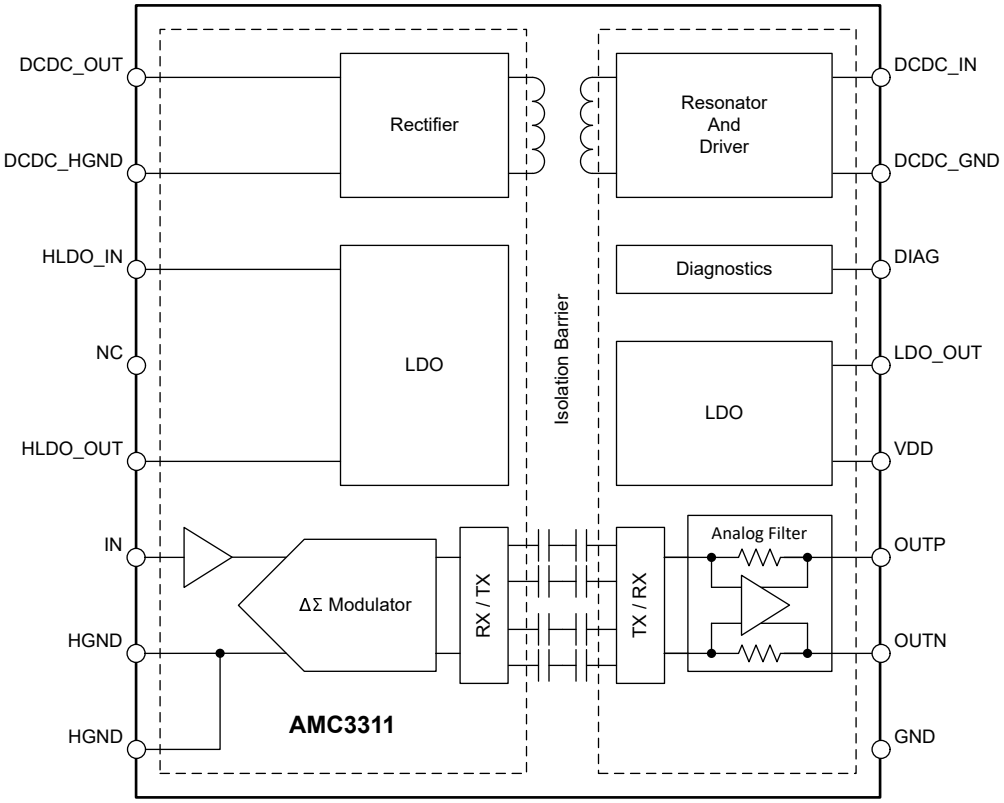
7.1 Overview

The AMC3311 is a precision, single-ended, isolated amplifier with high input impedance, wide input voltage range, and an integrated DC/DC converter that allows the device to be supplied from a single 3.3-V or 5-V voltage source on the low side. The input stage of the device drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins proportional to the input signal.

A block diagram of the AMC3311 is shown in the *Functional Block Diagram*. The 1-GΩ input impedance of the analog input stage supports low gain-error signal-sensing in high-voltage applications using high-impedance resistive dividers.

The signal path is isolated by a double capacitive silicon-dioxide (SiO_2) insulation barrier, whereas power isolation uses an on-chip transformer separated by a thin-film polymer as the insulating material.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The single-ended, high-impedance input stage of the AMC3311 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the *Isolation Channel Signal Transmission* section. With the high-impedance input and low input bias current, the AMC3311 device is designed for isolated, high-voltage-sensing applications that typically employ high-impedance resistive dividers.

There are two restrictions on the analog input signal, IN. First, if the input voltage V_{IN} exceeds the range specified in the *Absolute Maximum Ratings* table, the input current must be limited to the absolute maximum value because the electrostatic discharge (ESD) diodes turn on. Second, the linearity and noise performance of

the device are ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}), as specified in the *Recommended Operating Conditions* table.

7.3.2 Isolation Channel Signal Transmission

The AMC3311 uses an on-off keying (OOK) modulation scheme, as shown in Figure 7-1, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) depicted in the *Functional Block Diagram* transmits an internally-generated, 480-MHz carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC3311 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

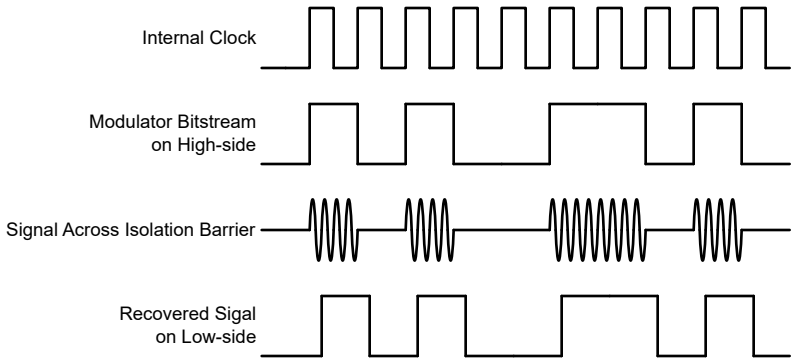


Figure 7-1. OOK-Based Modulation Scheme

7.3.3 Analog Output

The AMC3311 provides a differential analog output on the OUTP and OUTN pins. For input voltages V_{IN} in the range from –0.1 V to 2 V, the device provides a linear response with a nominal gain of 1. For example, for an input voltage of 2 V, the differential output voltage ($V_{OUTP} – V_{OUTN}$) is 2 V. At zero input (IN shorted to HGND), both pins output the same common-mode output voltage V_{CMout}, as specified in the *Electrical Characteristics* table. For input voltages greater than 2 V but less than approximately 2.5 V, the differential output voltage continues to increase but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in Figure 7-2, if the input voltage exceeds the $V_{Clipping}$ value.

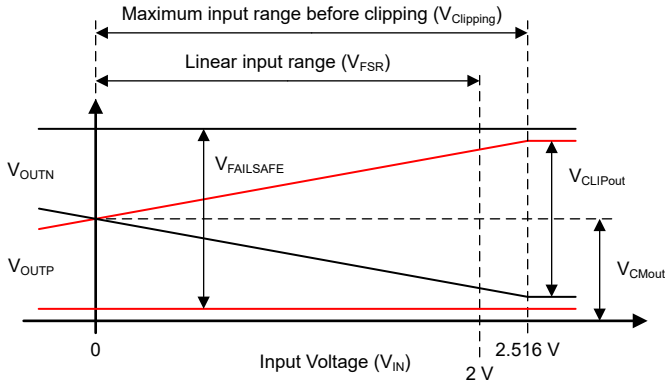


Figure 7-2. Output Behavior of the AMC3311

The AMC3311 provides a fail-safe output that simplifies diagnostics on a system level. The fail-safe output is active when the integrated DC/DC converter or high-side LDO do not deliver the required supply voltage for the high-side of the device. Figure 7-3 and Figure 7-4 show the fail-safe output of the AMC3311, which is a negative differential output voltage value that does not occur under normal operating conditions. Use the maximum $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for the fail-safe detection on a system level.

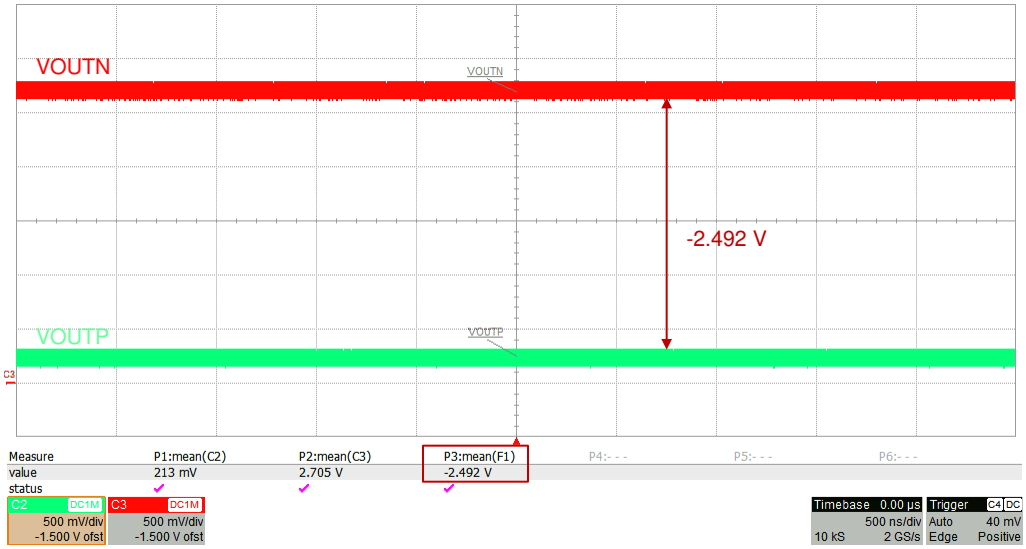


Figure 7-3. Typical Negative Clipping Output of the AMC3311

Figure 7-4. Typical Fail-Safe Output of the AMC3311

7.3.4 Isolated DC/DC Converter

The AMC3311 offers a fully integrated isolated DC/DC converter that includes the following components illustrated in the *Functional Block Diagram*:

- Low-dropout regulator (LDO) on the low-side to stabilize the supply voltage VDD that drives the low-side of the DC/DC converter
- Low-side full-bridge inverter and drivers
- Laminate-based, air-core transformer for high immunity to magnetic fields
- High-side full-bridge rectifier
- High-side LDO to stabilize the output voltage of the DC/DC converter for high analog performance of the signal path

The DC/DC converter uses a spread-spectrum clock generation technique to reduce the spectral density of the electromagnetic radiation. The resonator frequency is synchronous to the operation of the ΔΣ modulator to minimize interference with data transmission and support the high analog performance of the device.

The architecture of the DC/DC converter is optimized to drive the high-side circuitry of the AMC3311 and can source up to I_H, as specified in the *Electrical Characteristics* table, of additional current for an optional auxiliary circuit such as an active filter, preamplifier, or a high-speed isolated comparator such as an AMC23C11.

7.3.5 Diagnostic Output and Fail-Safe Behavior

The open-drain DIAG pin can be monitored to confirm the device is operational and the output voltage is valid. During power-up, the DIAG pin is actively held low until the high-side supply is in regulation and the device operates properly. The DIAG pin is actively pulled low if:

- The low-side does not receive data from the high-side (for example, because of a loss of power on the high-side). The amplifier outputs are driven to negative full-scale.
- The high-side DC/DC output voltage (DCDC_OUT) or the high-side LDO output voltage (HLDO_OUT) drop below the respective undervoltage detection thresholds V_{DCDCUV} and V_{HLDOUV}, as specified in the *Electrical Characteristics* table. In this case, the low-side can still receive data from the high-side but the data can possibly be invalid. The amplifier outputs are driven to negative full-scale.

During normal operation, the DIAG pin is in a high-impedance state. Connect the DIAG pin to a pullup supply through a resistor or leave open if not used.

7.4 Device Functional Modes

The AMC3311 is operational when the power supply VDD is applied, as specified in the *Recommended Operating Conditions* table.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Isolated amplifiers are widely used for voltage measurements in high-voltage applications that must be isolated from a low-voltage domain. A typical application is the sensing of the DC link voltage in a frequency inverter.

The high input impedance, low input bias current, low temperature drift, and high DC accuracy make the AMC3311 a high-performance solution for applications where isolated voltage measurements are required.

8.2 Typical Application

Figure 8-1 shows a simplified schematic of the AMC3311 in a typical motor drive application. The DC link voltage is divided down to an approximate 2-V level across the bottom two sense resistors (RSNS1 + RSNS2) of a high-impedance resistive divider. This voltage is sensed by the AMC3311. The AMC3311 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, and reconstructs an analog signal that is presented as a differential voltage on the output pins OUTN and OUTP.

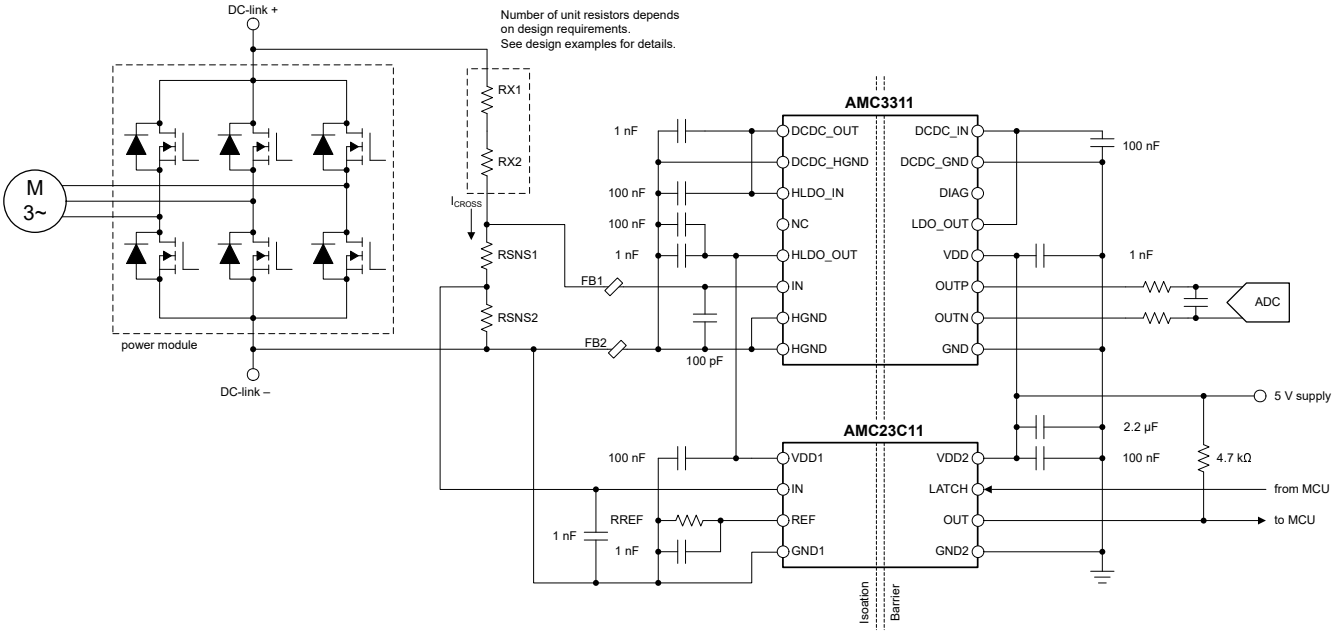


Figure 8-1. The AMC3311 in a Motor Drive Application

The AMC3311 integrates an isolated power supply for the high-voltage side and therefore is particularly easy to use in applications that do not have a high-side supply readily available. In this example, the integrated power supply of the AMC3311 is also used to power an AMC23C11 isolated, high-speed comparator that is used for low-latency overvoltage detection on the DC link.

The AMC23C11 isolated comparator senses the voltage across the bottom resistor (RSNS2) of the resistive divider and compares that value against an adjustable reference voltage (V_{REF}). The isolated comparator pulls down the open-drain output on the low-side whenever the input voltage exceeds the reference value. For a detailed description of the isolated comparator, see the *AMC23C11 data sheet* available for download at ti.com.

The bottom resistor in the resistive divider is split into two equal-value resistors (RSNS1 and RSNS2) to accommodate the headroom requirements of the reference voltage (V_{REF}) of the isolated comparator, as explained in the *Detailed Design Procedure* section.

8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

PARAMETER	VALUE
System input voltage	Single phase, 230 V, 50 Hz
DC link voltage (normal operation)	400 V (maximum)
DC link overvoltage detection level	450 V
Low-side supply voltage	5 V
Voltage drop across the sensing resistor (RSNS1 + RSNS2) for a linear response	2 V (maximum)
Current through the resistive divider, I_{CROSS}	100 µA (maximum)
Minimum headroom (VDD1 – V_{REF}) for the reference voltage of the AMC23C11 isolated comparator	1.4 V
Maximum resistor operating voltage	75 V

8.2.2 Detailed Design Procedure

The 100-µA, cross-current requirement at the maximum DC link voltage (400 V) determines that the total impedance of the resistive divider is 4 MΩ. The impedance of the resistive divider is dominated by the top portion (shown exemplary as RX1 and RX2 in Figure 8-1) and the voltage drop across RSNS1 and RSNS2 can be neglected for a moment. The maximum allowed voltage drop per unit resistor is specified as 75 V; therefore, the minimum number of unit resistors in the top portion of the resistive divider is 400 V / 75 V = 6. The calculated unit value is 4 MΩ / 6 = 667 kΩ and the next closest value from the E96 series is 665 kΩ.

The total sense resistor (RSNS = RSNS1 + RSNS2) is sized such that the voltage drop across the resistor at the maximum DC link voltage (400 V) equals the linear full-scale range input voltage (V_{FSR}) of the AMC3311, which is 2 V. This resistance is calculated as RSNS = V_{FSR} / ($V_{DC\text{-}link,\ max}$ – V_{FSR}) × R_{TOP}, where R_{TOP} is the total value of the top resistor string (6 × 665 kΩ = 3990 kΩ). RSNS is calculated as 20.05 kΩ and split into two equal resistors (RSNS1 and RSNS2) of 10 kΩ each, a value from the E96 series.

The isolated comparator senses the voltage drop across RSNS2. At the specified DC link overvoltage of 450 V, the voltage drop across RSNS2 is RSNS2 / (RTOP + RSNS1 + RSNS2) × $V_{DC\text{-}link}$ and equals 1.12 V. This value is the trip threshold value, V_{REF}. The trip threshold is set by the resistor RREF and is calculated as (1.12 V – 4 mV) / 100 µA = 11.2 kΩ. A value of 11 kΩ is selected from the E96 series, resulting in a slightly lower reference voltage of 1.1 V. The 4-mV value subtracted from V_{REF} is related to the hysteresis of the isolated comparator on the rising edge of V_{IN}. 100 µA is the value of the internal current source connected to the REF pin of the AMC23C11. For a detailed calculation of the trip threshold, see the AMC23C11 data sheet. The resulting overvoltage detection threshold is (V_{REF} + 4 mV) / RSNS1 × (RTOP + RSNS1 + RSNS2), or 443 V.

The reference of the AMC23C11 comparator requires a minimum headroom to VDD1 of 1.4 V. The minimum supply voltage (VDD1) to the isolated comparator is in the minimum output voltage of the AMC3311 high-side LDO (V_{HLDO_OUT}), which equals 3 V. Therefore, the reference operates at a minimum headroom of 3 V – 1.1 V = 1.9 V and satisfies the design requirements.

Table 8-2 summarizes the design parameters for this application.

Table 8-2. Design Summary

PARAMETER	VALUE
Unit resistor value, RX	665 kΩ
Number of unit resistors	6
Sense resistor values (RSNS1 and RSNS2)	10 kΩ
Resulting current through resistive divider (I_{CROSS} at 400 V)	99.8 µA
Resulting full-scale voltage drop across sense resistor (RSNS1 + RSNS2)	1.995 V
Total power dissipated in resistive divider	39.9 mW
Power dissipated in unit resistor RX	6.6 mW
AMC23C11 reference resistor value, RREF	11 kΩ
Resulting overvoltage detection threshold	443 V

8.2.2.1 Input Filter Design

Placing an RC filter in front of the isolated amplifier improves signal-to-noise performance of the signal path. In practice, however, the impedance of the resistor divider is high and only a small-value filter capacitor can be used to not limit the signal bandwidth to an unacceptable low value. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the internal ΔΣ modulator.
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter. Because the device has an input bias current in the low nanoampere range, IR drops across the filter impedance are usually not a concern.

Most voltage-sensing applications use high-impedance resistive dividers in front of the isolated amplifier to scale down the input voltage. In this case, a single capacitor (as shown in Figure 8-2) is sufficient to filter the input signal.

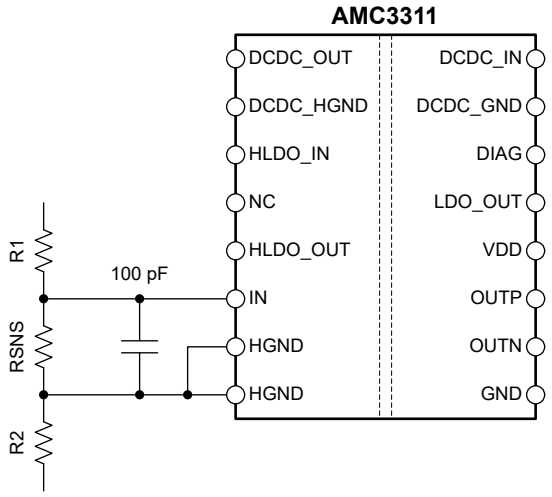


Figure 8-2. Input Filter

8.2.2.2 Differential to Single-Ended Output Conversion

Figure 8-3 shows an example of a TLV900x-based signal conversion and filter circuit for systems using single-ended input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals (V_{OUTP} – V_{OUTN}) + V_{REF}. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.

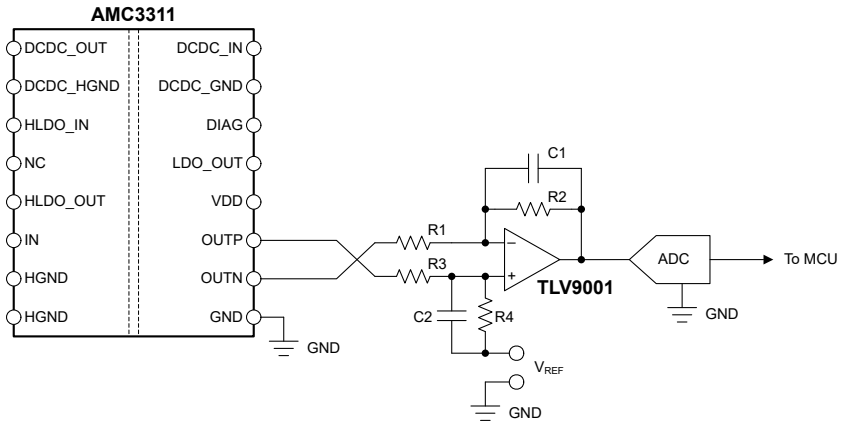


Figure 8-3. Connecting the AMC3311 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

8.2.3 Application Curve

Figure 8-4 shows the typical full-scale step response of the AMC3311.

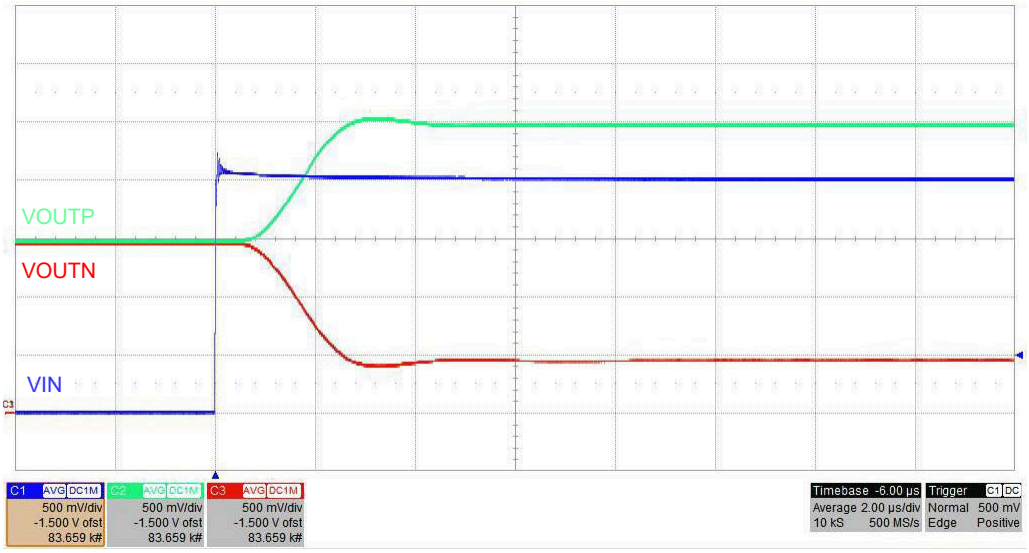


Figure 8-4. Step Response of the AMC3311

8.3 Best Design Practices

Do not leave the analog input (IN pin) of the AMC3311 unconnected (floating) when the device is powered up on the high-side. If the device input is left floating, the bias current can generate a negative input voltage that exceeds the specified input voltage range, causing the output of the device to be invalid.

Do not connect protection diodes to the input (IN pin) of the AMC3311. Diode leakage current can introduce significant measurement error especially at high temperatures. The input pin is protected against high voltages by the ESD protection circuit and the high impedance of the external restive divider.

8.4 Power Supply Recommendations

The AMC3311 is powered from the low-side power supply (VDD) with a nominal value of 3.3 V (or 5 V). Use a low-ESR decoupling capacitor of 1 nF (C8 in Figure 8-5) placed as close as possible to the VDD pin, followed by a 1-µF capacitor (C9) to filter this power-supply path.

The low-side of the DC/DC converter is decoupled with a low-ESR 100-nF capacitor (C4) positioned close to the device between the DCDC_IN and DCDC_GND pins. Use a 1-µF capacitor (C2) to decouple the high-side in addition to a low-ESR, 1-nF capacitor (C3) placed as close as possible to the device and connected to the DCDC_OUT and DCDC_HGND pins.

For the high-side LDO, use low-ESR capacitors of 1-nF (C6), placed as close as possible to the AMC3311, followed by a 100-nF decoupling capacitor (C5).

As shown in Figure 8-5, place ferrite beads in the IN and HGND signal lines for best EMI performance. For more information on reducing radiated emissions and guidelines for component selection, see the *Best Practices to Attenuate AMC3301 Family Radiated Emissions EMI* application note available for download at www.ti.com

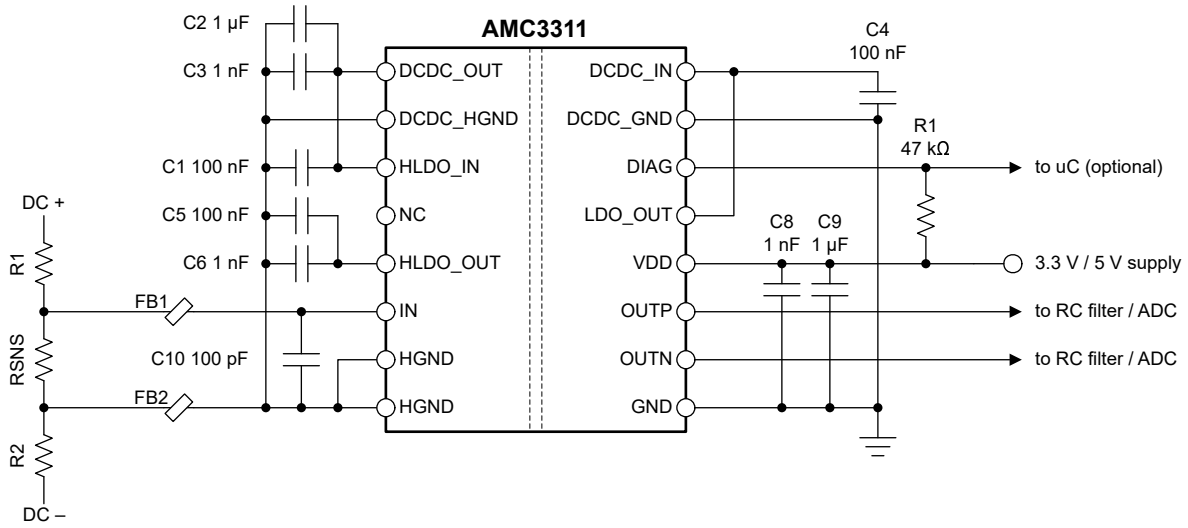


Figure 8-5. Decoupling the AMC3311

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) capacitors typically exhibit only a fraction of the nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

Table 8-3 lists components suitable for use with the AMC3311. This list is not exhaustive. Other components can exist that are equally suitable (or better), however these listed components have been validated during the development of the AMC3311.

Table 8-3. Recommended External Components

DESCRIPTION		PART NUMBER	MANUFACTURER	SIZE (EIA, L x W)
VDD				
C8	1 nF ± 10%, X7R, 50 V	12065C102KAT2A(1)	AVX	1206, 3.2 mm x 1.6 mm
		C0603C102K5RACTU	Kemet	0603, 1.6 mm x 0.8 mm
C9	1 µF ± 10%, X7R, 25 V	12063C105KAT2A(1)	AVX	1206, 3.2 mm x 1.6 mm
		CGA3E1X7R1E105K080AC	TDK	0603, 1.6 mm x 0.8 mm
DC/DC CONVERTER				
C4	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C3	1 nF ± 10%, X7R, 50 V	C0603C102K5RACTU	Kemet	0603, 1.6 mm x 0.8 mm
C2	1 µF ± 10%, X7R, 25 V	CGA3E1X7R1E105K080AC	TDK	0603, 1.6 mm x 0.8 mm
HLDO				
C1	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C5	100 nF ± 5%, NP0, 50 V	C3216NP01H104J160AA(1)	TDK	1206, 3.2 mm x 1.6 mm
	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C6	1 nF ± 10%, X7R, 50 V	12065C102KAT2A(1)	AVX	1206, 3.2 mm x 1.6 mm
		C0603C102K5RACTU	Kemet	0603, 1.6 mm x 0.8 mm
FERRITE BEADS				
FB1,FB2	Ferrite bead(2)	74269244182	Wurth Elektronik	0402, 1.0 mm x 0.5 mm
		BLM15HD182SH1	Murata	0402, 1.0 mm x 0.5 mm
		BKH1005LM182-T	Taiyo Yuden	0402, 1.0 mm x 0.5 mm

(1) Component used for parametric validation.
(2) No ferrite beads used for parametric validation.

8.5 Layout

8.5.1 Layout Guidelines

Figure 8-6 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC3311 supply pins) and placement of the other components required by the device. For best performance, place the sense resistor close to the device input pin (IN).

This layout is used on the AMC3311 EVM and supports CISPR-11 compliant electromagnetic radiation levels.

8.5.2 Layout Example

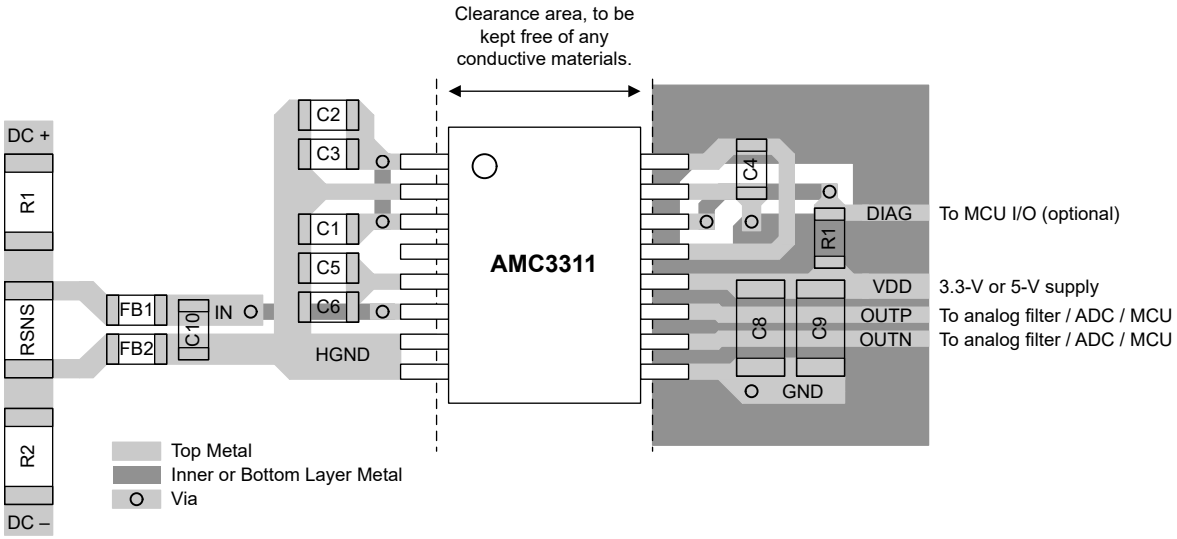


Figure 8-6. Recommended Layout of the AMC3311

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

Texas Instruments, *Isolation Glossary*

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application note
- Texas Instruments, *TLV900x Low-Power, RRIO, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *AMC23C11 Fast Response, Reinforced Isolated Comparator With Adjustable Threshold and Latch Function* data sheet
- Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC3311DWER	ACTIVE	SOIC	DWE	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC3311	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

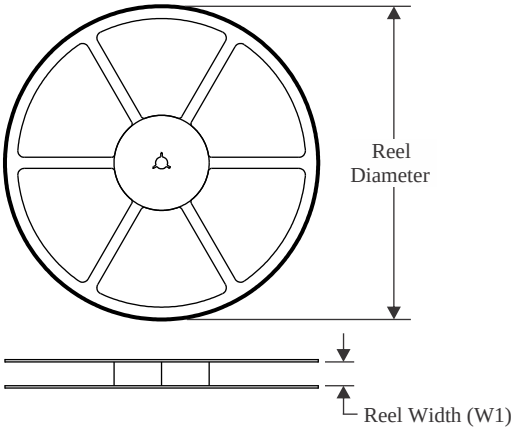
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

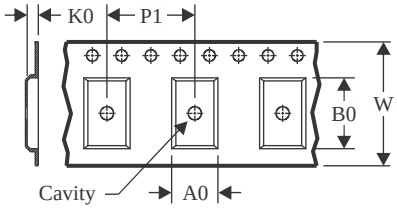
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

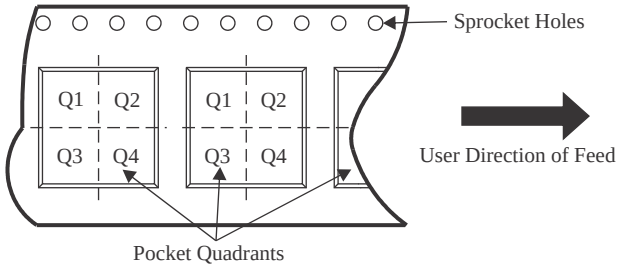


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

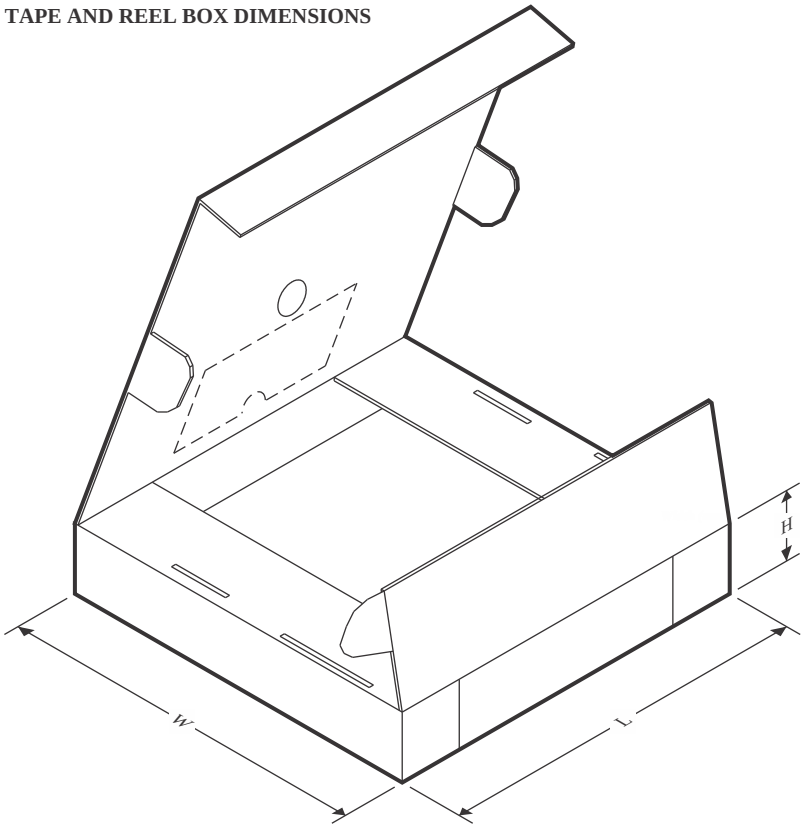
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

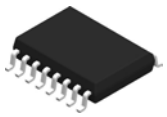
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC3311DWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC3311DWER	SOIC	DWE	16	2000	350.0	350.0	43.0

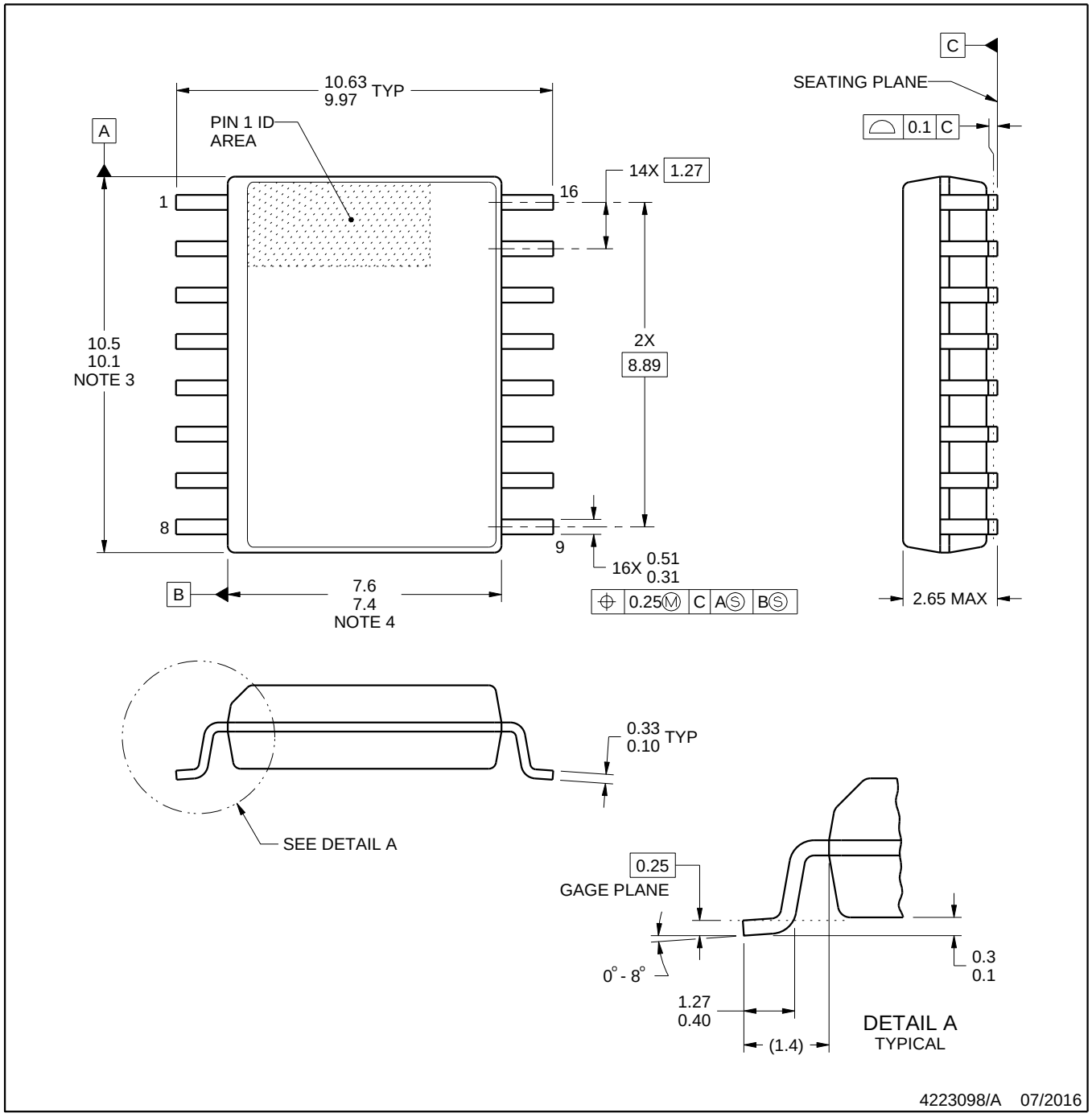


PACKAGE OUTLINE

DWE0016A

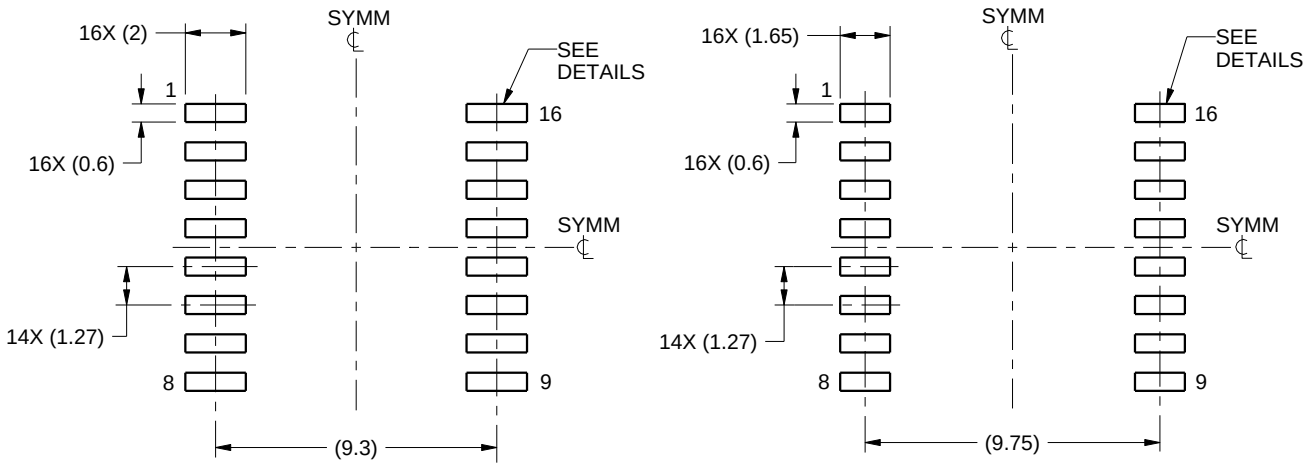
SOIC - 2.65 mm max height

SOIC



NOTES:

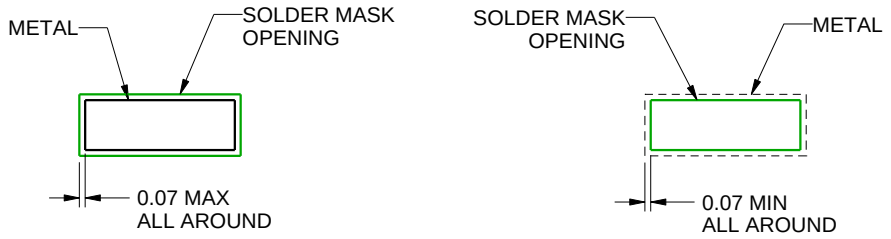
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

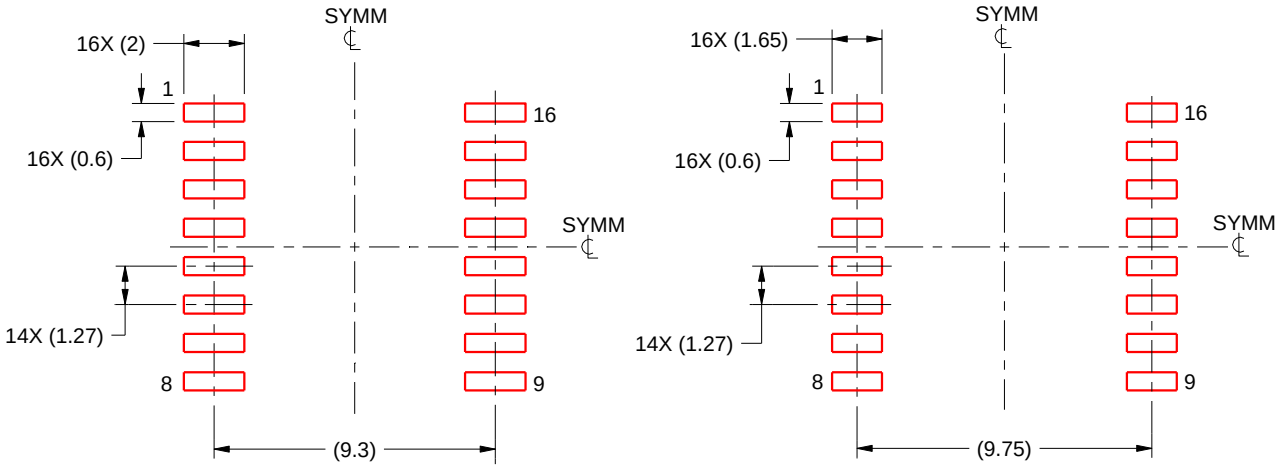
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4223098/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4223098/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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