DLPC964 Digital Micromirror Device Controller

1 Features

- Operates the DLP991U DLP® DMD
- Continuous streaming input data over 12 HSS input lanes up to 120Gbps
- Enables high-speed pattern rates up to 12.4kHz binary patterns per second
- 32 lane differential high speed serial interface (HSSI) data bus interface
- Random DMD block addressing and LOAD2 loading
- Compatible with a variety of user-defined FPGAs
- I^2C interface for control and status queries

2 Applications

- Lithography
  - Direct imaging
  - Flat panel display
  - Printed circuit board manufacturing
- Industrial
  - 3D printing
  - 3D scanners for machine vision
  - Quality control
- Displays
  - 3D imaging
  - Augmented reality and information overlay

3 Description

The DLPC964 controller works with the DLP991U digital micromirror device (DMD). The controller provides a high-speed data and control interface for the DMD to enable binary pattern rates up to 12.4kHz. These fast pattern rates set DLP technology apart from other spatial light modulators and offer a strategic advantage for equipment needing fast, accurate, and programmable light steering capability. The DLPC964 provides the required clocking pulses and timing information to the DMD. The unique capability and value offered by the controller make it well-suited to support a wide variety of direct imaging, industrial, and advanced display applications.

In DLP-based electronics solutions, image data is 100% digital from the DLPC964 input port to the projected image. The image stays in digital form and is never converted into an analog signal. The DLPC964 processes the digital input image and converts the data into a format needed by the DMD for proper display. The DMD then steers the light to the location determined by the pixel data loaded into the DMD.

For complete electrical and mechanical specifications of the DLPC964, see the AMD Virtex™ 7 product specification.

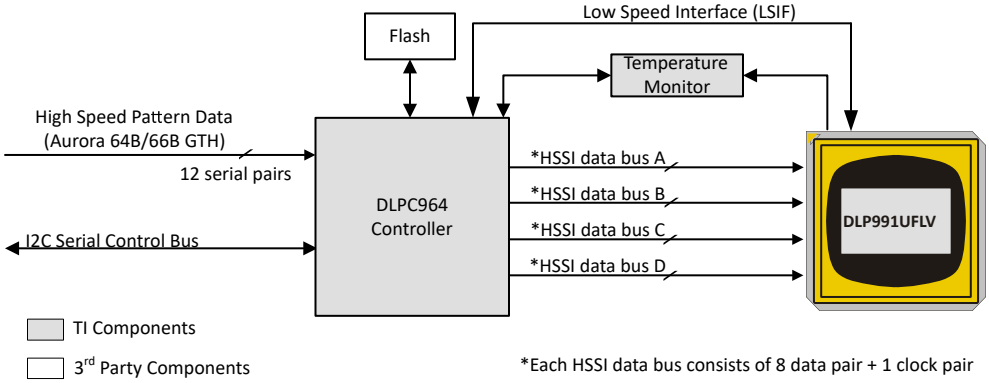
Get started with TI DLP® light-control technology page to learn how to get started with the DLPC964.

The DLP advanced light control resources on ti.com accelerate time to market, which include evaluation modules, optical modules manufacturers, and DLP design network partners.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DLPC964	FCBGA (1158)	35.00mm × 35.00mm

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.



Simplified Application

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4 Pin Configuration and Functions

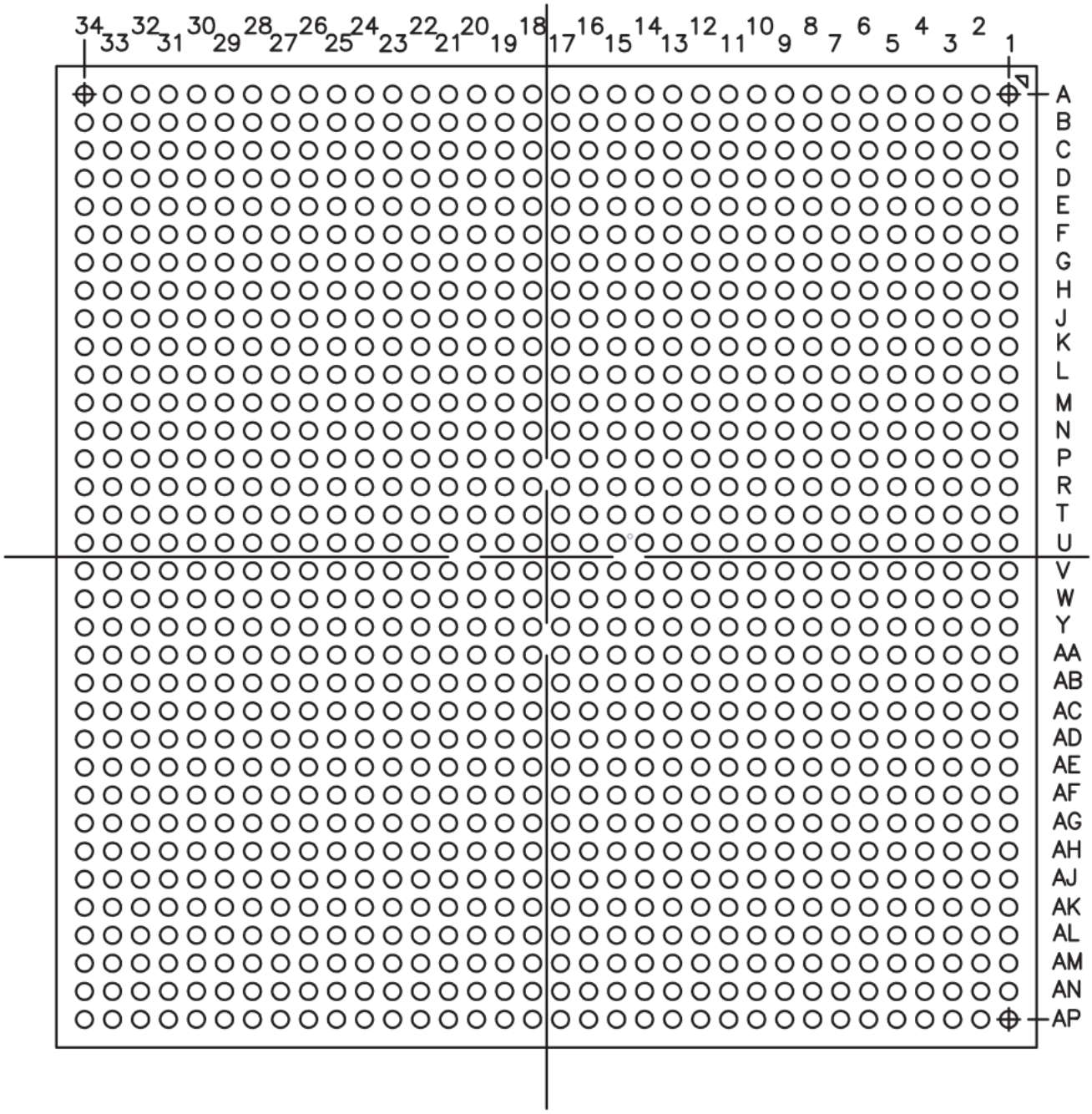


Figure 4-1. ZUM Package, 1158-Pin FCBGA, Bottom View

I/O Type Descriptions

I/O TYPE	DESCRIPTION
PWR	Power
GND	Ground
LVCMOS18_I	LVCMOS 1.8V input
LVCMOS18_O	LVCMOS 1.8V output
LVCMOS18_B	LVCMOS 1.8V bidirectional

I/O Type Descriptions (continued)

I/O TYPE	DESCRIPTION
LVDS_18_NI	LVDS 1.8V negative input
LVDS_18_PI	LVDS 1.8V positive input
LVDS_18_NO	LVDS 1.8V negative output
LVDS_18_PO	LVDS 1.8V positive output
LVDCI_18_I	Low-voltage digitally controlled impedance 1.8V input
LVDCI_18_O	Low-voltage digitally controlled impedance 1.8V output
MGTHRX_18_NI	GTH Receiver Differential 1.8V negative input
MGTHRX_18_PI	GTH Receiver Differential 1.8V positive input
MGTHTX_18_NO	GTH Receiver Differential 1.8V negative output
MGTHTX_18_PO	GTH Receiver Differential 1.8V positive output
MGTREFCLK_NI	GTH Receiver RefClk Differential 1.8V negative input
MGTREFCLK_PI	GTH Receiver RefClk Differential 1.8V positive input
NC	No connection

Table 4-1. Pin Functions

PIN		I/O TYPE[1]	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
SYS_ARSTZ	G25	LVCMOS18_I	LO = 0	—	DLPC964 Reset
I2C_ADDR_SEL[0]	M25	LVCMOS18_I	HI = 1	—	DLPC964 Slave I^2C Address Bit 0
I2C_ADDR_SEL[1]	D26	LVCMOS18_I	HI	—	DLPC964 Slave I^2C Address Bit 1
I2C_SCL	B23	LVCMOS18_B	—	—	DLPC964 Slave I^2C Clock. Requires an external 2.2kΩ pullup resistor
I2C_SDA	B25	LVCMOS18_B	—	I2C_SCL	DLPC964 Slave I^2C Data. Requires an external 2.2kΩ pullup resistor
SYS_CLK100_N	H24	LVDS_18_NI	—	Reference clock	100MHz Differential Reference Clock (N)
SYS_CLK100_P	J24	LVDS_18_PI	—	Reference clock	100MHz Differential Reference Clock (P)
CCLK_0	V25	LVCMOS18_O	—	Flash interface clock	Connect to Configuration Flash device CLK.
FLASH_MISO	A24	LVCMOS18_I	—	CCLK_0	Connect to Configuration Flash MISO.
FLASH_MOSI	A23	LVCMOS18_O	—	CCLK_0	Connect to Configuration Flash device MOSI.
FLASH_CSZ	C24	LVCMOS18_O	LO	CCLK_0	Connect to Configuration Flash device CSZ.
BLKADDR[0]	B26	LVCMOS18_I	HI	—	Block Address bit 0
BLKADDR[1]	A26	LVCMOS18_I	HI	—	Block Address bit 1
BLKADDR[2]	F24	LVCMOS18_I	HI	—	Block Address bit 2
BLKADDR[3]	F25	LVCMOS18_I	HI	—	Block Address bit 3
BLKADDR[4]	E24	LVCMOS18_I	HI	—	Block Address bit 4
BLKMODE[0]	C27	LVCMOS18_I	HI	—	Block Mode bit 0
BLKMODE[1]	A25	LVCMOS18_I	HI	—	Block Mode bit 1
BLKLOADZ	B27	LVDCI_18_O	LO	—	Connect to Apps FPGA BLKLOADZ.
LOAD2	D25	LVCMOS18_I	HI	—	Enables Load-2 functionality of the DMD. Includes an internal pulldown
WDT_ENABLEZ	J22	LVCMOS18_I	LO	—	DMD Mirror Clocking Pulse Watchdog Timer Enable. Includes an internal pulldown
MCP_START	J25	LVCMOS18_I	HI	—	Initiates a Mirror Clocking Pulse (MCP)
MCP0_ACTIVE	E27	LVDCI_18_O	HI	—	Connect to Apps FPGA MCP_ACTIVE0.
MCP1_ACTIVE	D27	LVDCI_18_O	HI	—	Connect to Apps FPGA MCP_ACTIVE1.

Table 4-1. Pin Functions (continued)

PIN		I/O TYPE[1]	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
MCP2_ACTIVE	E26	LVDCI_18_O	HI	—	Connect to Apps FPGA MCP_ACTIVE2.
MCP3_ACTIVE	H25	LVDCI_18_O	HI	—	Connect to Apps FPGA MCP_ACTIVE3.
DMDLOAD_REQ	M22	LVCMOS18_I	HI	—	Connect to Apps FPGA DMDLOAD_REQ.
DMD_GTREFCLK_IN_A_N	AB30	LVDS_18_NI	—	Reference clock	DMD Bus A Reference Clock Input. 100Ω internal LVDS termination
DMD_GTREFCLK_IN_A_P	AB29	LVDS_18_PI	—		
DMD_GTREFCLK_IN_B_N	AB5	LVDS_18_NI	—	Reference clock	DMD Bus B Reference Clock Input. 100Ω internal LVDS termination
DMD_GTREFCLK_IN_B_P	AB6	LVDS_18_PI	—		
DMD_GTREFCLK_IN_C_N	M30	LVDS_18_NI	—	Reference clock	DMD Bus C Reference Clock Input. 100Ω internal LVDS termination
DMD_GTREFCLK_IN_C_P	M29	LVDS_18_PI	—		
DMD_GTREFCLK_IN_D_N	M5	LVDS_18_NI	—	Reference clock	DMD Bus D Reference Clock Input. 100Ω internal LVDS termination
DMD_GTREFCLK_IN_D_P	M6	LVDS_18_PI	—		
DMD_DCLK_AN	AK34	MGTHTX_18_NO	—	—	Output Bus A Clock to DMD
DMD_DCLK_AP	AK33	MGTHTX_18_PO	—	—	
DMD_DCLK_BN	AJ3	MGTHTX_18_NO	—	—	Output Bus B Clock to DMD
DMD_DCLK_BP	AJ4	MGTHTX_18_PO	—	—	
DMD_DCLK_CN	G32	MGTHTX_18_NO	—	—	Output Bus C Clock to DMD
DMD_DCLK_CP	G31	MGTHTX_18_PO	—	—	
DMD_DCLK_DN	G3	MGTHTX_18_NO	—	—	Output Bus D Clock to DMD
DMD_DCLK_DP	G4	MGTHTX_18_PO	—	—	
DMD_D_AN[0]	AP34	MGTHTX_18_NO	—	DMD_DCLK_A	Output Bus A Data bit 0 to DMD
DMD_D_AP[0]	AP33	MGTHTX_18_PO	—	DMD_DCLK_A	
DMD_D_AN[1]	AN32	MGTHTX_18_NO	—	DMD_DCLK_A	Output Bus A Data bit 1 to DMD
DMD_D_AP[1]	AN31	MGTHTX_18_PO	—	DMD_DCLK_A	
DMD_D_AN[2]	AM34	MGTHTX_18_NO	—	DMD_DCLK_A	Output Bus A Data bit 2 to DMD
DMD_D_AP[2]	AM33	MGTHTX_18_PO	—	DMD_DCLK_A	
DMD_D_AN[3]	AJ32	MGTHTX_18_NO	—	DMD_DCLK_A	Output Bus A Data bit 3 to DMD
DMD_D_AP[3]	AJ31	MGTHTX_18_PO	—	DMD_DCLK_A	
DMD_D_AN[4]	AH34	MGTHTX_18_NO	—	DMD_DCLK_A	Output Bus A Data bit 4 to DMD
DMD_D_AP[4]	AH33	MGTHTX_18_PO	—	DMD_DCLK_A	
DMD_D_AN[5]	AF34	MGTHTX_18_NO	—	DMD_DCLK_A	Output Bus A Data bit 5 to DMD
DMD_D_AP[5]	AF33	MGTHTX_18_PO	—	DMD_DCLK_A	
DMD_D_AN[6]	AD34	MGTHTX_18_NO	—	DMD_DCLK_A	Output Bus A Data bit 6 to DMD
DMD_D_AP[6]	AD33	MGTHTX_18_PO	—	DMD_DCLK_A	
DMD_D_AN[7]	AB34	MGTHTX_18_NO	—	DMD_DCLK_A	Output Bus A Data bit 7 to DMD
DMD_D_AP[7]	AB33	MGTHTX_18_PO	—	DMD_DCLK_A	
DMD_D_BN[0]	AB1	MGTHTX_18_NO	—	DMD_DCLK_B	Output Bus B Data bit 0 to DMD
DMD_D_BP[0]	AB2	MGTHTX_18_PO	—	DMD_DCLK_B	
DMD_D_BN[1]	AD1	MGTHTX_18_NO	—	DMD_DCLK_B	Output Bus B Data bit 1 to DMD
DMD_D_BP[1]	AD2	MGTHTX_18_PO	—	DMD_DCLK_B	
DMD_D_BN[2]	AF1	MGTHTX_18_NO	—	DMD_DCLK_B	Output Bus B Data bit 2 to DMD
DMD_D_BP[2]	AF2	MGTHTX_18_PO	—	DMD_DCLK_B	
DMD_D_BN[3]	AH1	MGTHTX_18_NO	—	DMD_DCLK_B	Output Bus B Data bit 3 to DMD
DMD_D_BP[3]	AH2	MGTHTX_18_PO	—	DMD_DCLK_B	
DMD_D_BN[4]	AK1	MGTHTX_18_NO	—	DMD_DCLK_B	Output Bus B Data bit 4 to DMD
DMD_D_BP[4]	AK2	MGTHTX_18_PO	—	DMD_DCLK_B	
DMD_D_BN[5]	AM1	MGTHTX_18_NO	—	DMD_DCLK_B	Output Bus B Data bit 5 to DMD
DMD_D_BP[5]	AM2	MGTHTX_18_PO	—	DMD_DCLK_B	
DMD_D_BN[6]	AN3	MGTHTX_18_NO	—	DMD_DCLK_B	Output Bus B Data bit 6 to DMD
DMD_D_BP[6]	AN4	MGTHTX_18_PO	—	DMD_DCLK_B	
DMD_D_BN[7]	AP1	MGTHTX_18_NO	—	DMD_DCLK_B	Output Bus B Data bit 7 to DMD
DMD_D_BP[7]	AP2	MGTHTX_18_PO	—	DMD_DCLK_B	

Table 4-1. Pin Functions (continued)

PIN		I/O TYPE[1]	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
DMD_D_CN[0]	A32	MGTHTX_18_NO	—	DMD_DCLK_C	Output Bus C Data bit 0 to DMD
DMD_D_CP[0]	A31	MGTHTX_18_PO	—	DMD_DCLK_C	
DMD_D_CN[1]	B34	MGTHTX_18_NO	—	DMD_DCLK_C	Output Bus C Data bit 1 to DMD
DMD_D_CP[1]	B33	MGTHTX_18_PO	—	DMD_DCLK_C	
DMD_D_CN[2]	D34	MGTHTX_18_NO	—	DMD_DCLK_C	Output Bus C Data bit 2 to DMD
DMD_D_CP[2]	D33	MGTHTX_18_PO	—	DMD_DCLK_C	
DMD_D_CN[3]	F34	MGTHTX_18_NO	—	DMD_DCLK_C	Output Bus C Data bit 3 to DMD
DMD_D_CP[3]	F33	MGTHTX_18_PO	—	DMD_DCLK_C	
DMD_D_CN[4]	H34	MGTHTX_18_NO	—	DMD_DCLK_C	Output Bus C Data bit 4 to DMD
DMD_D_CP[4]	H33	MGTHTX_18_PO	—	DMD_DCLK_C	
DMD_D_CN[5]	K34	MGTHTX_18_NO	—	DMD_DCLK_C	Output Bus C Data bit 5 to DMD
DMD_D_CP[5]	K33	MGTHTX_18_PO	—	DMD_DCLK_C	
DMD_D_CN[6]	M34	MGTHTX_18_NO	—	DMD_DCLK_C	Output Bus C Data bit 6 to DMD
DMD_D_CP[6]	M33	MGTHTX_18_PO	—	DMD_DCLK_C	
DMD_D_CN[7]	N32	MGTHTX_18_NO	—	DMD_DCLK_C	Output Bus C Data bit 7 to DMD
DMD_D_CP[7]	N31	MGTHTX_18_PO	—	DMD_DCLK_C	
DMD_D_DN[0]	N3	MGTHTX_18_NO	—	DMD_DCLK_D	Output Bus D Data bit 0 to DMD
DMD_D_DP[0]	N4	MGTHTX_18_PO	—	DMD_DCLK_D	
DMD_D_DN[1]	M1	MGTHTX_18_NO	—	DMD_DCLK_D	Output Bus D Data bit 1 to DMD
DMD_D_DP[1]	M2	MGTHTX_18_PO	—	DMD_DCLK_D	
DMD_D_DN[2]	K1	MGTHTX_18_NO	—	DMD_DCLK_D	Output Bus D Data bit 2 to DMD
DMD_D_DP[2]	K2	MGTHTX_18_PO	—	DMD_DCLK_D	
DMD_D_DN[3]	H1	MGTHTX_18_NO	—	DMD_DCLK_D	Output Bus D Data bit 3 to DMD
DMD_D_DP[3]	H2	MGTHTX_18_PO	—	DMD_DCLK_D	
DMD_D_DN[4]	F1	MGTHTX_18_NO	—	DMD_DCLK_D	Output Bus D Data bit 4 to DMD
DMD_D_DP[4]	F2	MGTHTX_18_PO	—	DMD_DCLK_D	
DMD_D_DN[5]	D1	MGTHTX_18_NO	—	DMD_DCLK_D	Output Bus D Data bit 5 to DMD
DMD_D_DP[5]	D2	MGTHTX_18_PO	—	DMD_DCLK_D	
DMD_D_DN[6]	B1	MGTHTX_18_NO	—	DMD_DCLK_D	Output Bus D Data bit 6 to DMD
DMD_D_DP[6]	B2	MGTHTX_18_PO	—	DMD_DCLK_D	
DMD_D_DN[7]	A3	MGTHTX_18_NO	—	DMD_DCLK_D	Output Bus D Data bit 7 to DMD
DMD_D_DP[7]	A4	MGTHTX_18_PO	—	DMD_DCLK_D	
GTRX_CH0_REFCLK_N	R28	MGTREFCLK_NI	—	Reference clock	Input CH0 Reference Clock. 100Ω internal LVDS termination
GTRX_CH0_REFCLK_P	R27	MGTREFCLK_PI	—		
GTRX_CH1_REFCLK_N	W28	MGTREFCLK_NI	—	Reference clock	Input CH1 Reference Clock. 100Ω internal LVDS termination
GTRX_CH1_REFCLK_P	W27	MGTREFCLK_PI	—		
GTRX_CH2_REFCLK_N	R7	MGTREFCLK_NI	—	Reference clock	Input CH2 Reference Clock. 100Ω internal LVDS termination
GTRX_CH2_REFCLK_P	R8	MGTREFCLK_PI	—		
GTRX_CH3_REFCLK_N	W7	MGTREFCLK_NI	—	Reference clock	Input CH3 Reference Clock. 100Ω internal LVDS termination
GTRX_CH3_REFCLK_P	W8	MGTREFCLK_PI	—		
CH0_GTRX_N[0]	T30	MGTHRX_18_NI	—	GTRX_CH0_REFCLK	Input Bus CH0 Data bit 0. 100Ω internal LVDS termination
CH0_GTRX_P[0]	T29	MGTHRX_18_PI	—		
CH0_GTRX_N[1]	R32	MGTHRX_18_NI	—	GTRX_CH0_REFCLK	Input Bus CH0 Data bit 1. 100Ω internal LVDS termination
CH0_GTRX_P[1]	R31	MGTHRX_18_PI	—		
CH0_GTRX_N[2]	P30	MGTHRX_18_NI	—	GTRX_CH0_REFCLK	Input Bus CH0 Data bit 2. 100Ω internal LVDS termination
CH0_GTRX_P[2]	P29	MGTHRX_18_PI	—		
CH1_GTRX_N[0]	AA32	MGTHRX_18_NI	—	GTRX_CH1_REFCLK	Input Bus CH1 Data bit 0. 100Ω internal LVDS termination
CH1_GTRX_P[0]	AA31	MGTHRX_18_PI	—		
CH1_GTRX_N[1]	Y30	MGTHRX_18_NI	—	GTRX_CH1_REFCLK	Input Bus CH1 Data bit 1. 100Ω internal LVDS termination
CH1_GTRX_P[1]	Y29	MGTHRX_18_PI	—		
CH1_GTRX_N[2]	V30	MGTHRX_18_NI	—	GTRX_CH1_REFCLK	Input Bus CH1 Data bit 2. 100Ω internal LVDS termination
CH1_GTRX_P[2]	V29	MGTHRX_18_PI	—		
CH2_GTRX_N[0]	T5	MGTHRX_18_NI	—	GTRX_CH2_REFCLK	Input Bus CH2 Data bit 0. 100Ω internal LVDS termination
CH2_GTRX_P[0]	T6	MGTHRX_18_PI	—		

Table 4-1. Pin Functions (continued)

PIN		I/O TYPE[1]	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
CH2_GTRX_N[1]	R3	MGTHRX_18_NI	—	GTRX_CH2_REFCLK	Input Bus CH2 Data bit 1. 100Ω internal LVDS termination
CH2_GTRX_P[1]	R4	MGTHRX_18_PI	—		
CH2_GTRX_N[2]	P5	MGTHRX_18_NI	—	GTRX_CH2_REFCLK	Input Bus CH2 Data bit 2. 100Ω internal LVDS termination
CH2_GTRX_P[2]	P6	MGTHRX_18_PI	—		
CH3_GTRX_N[0]	AA3	MGTHRX_18_NI	—	GTRX_CH3_REFCLK	Input Bus CH3 Data bit 0. 100Ω internal LVDS termination
CH3_GTRX_P[0]	AA4	MGTHRX_18_PI	—		
CH3_GTRX_N[1]	Y5	MGTHRX_18_NI	—	GTRX_CH3_REFCLK	Input Bus CH3 Data bit 1. 100Ω internal LVDS termination
CH3_GTRX_P[1]	Y6	MGTHRX_18_PI	—		
CH3_GTRX_N[2]	V5	MGTHRX_18_NI	—	GTRX_CH3_REFCLK	Input Bus CH3 Data bit 2. 100Ω internal LVDS termination
CH3_GTRX_P[2]	V6	MGTHRX_18_PI	—		
HSSI_BUS_ERR	AJ12	LVDCI_18_O	HI	—	Connect to Apps FPGA HSSI_BUS_ERR.
HSSI_ERR_LATCH_RST	AN12	LVDCI_18_O	LO	—	Connect to Latch Clear on DMD board.
EXT_HSSI_RST	AJ14	LVCMOS18_I	HI	—	Connect to Apps FPGA EXT_HSSI_RST.
HSSI_RST_ACT	AK12	LVDCI_18_O	HI	—	Connect to Apps FPGA HSSI_RST_ACT.
DMD_LS_CLK_N	AP11	LVDS_18_NO	—	—	Output LS Bus Clock to DMD
DMD_LS_CLK_P	AP12	LVDS_18_PO	—	—	
DMD_LS_WDATA_N	AP14	LVDS_18_NO	—	DMD_LS_CLK	Output WData Bus to DMD
DMD_LS_WDATA_P	AN14	LVDS_18_PO	—	DMD_LS_CLK	
DMD_LS_RDATA_A	AM8	LVCMOS18_I	—	DMD_LS_CLK	Input Bus RData bit A
DMD_LS_RDATA_B	AN8	LVCMOS18_I	—	DMD_LS_CLK	Input Bus RData bit B
DMD_LS_RDATA_C	AN9	LVCMOS18_I	—	DMD_LS_CLK	Input Bus RData bit C
DMD_LS_RDATA_D	AP9	LVCMOS18_I	—	DMD_LS_CLK	Input Bus RData bit D
DMD_DMUX	AM12	LVCMOS18_I	HI	—	Connect to DMUX_LATCHED on DMD board.
IRQZ	E23	LVDCI_18_O	LO	—	Connect to Apps FPGA IRQZ.
DMD_RESERVED	AM13	LVCMOS18_B	—	—	Connect to RESERVED pin on DMD.
PARKZ	AK9	LVCMOS18_I	LO	—	Immediately parks the DMD when asserted Low
RXLPMEN	D24	LVCMOS18_I	HI	—	Enables Aurora 64B/66B Receiver Low Power Mode
DMD_PWREN	AL9	LVDCI_18_O	HI	—	Connect to DMD Power Enable on DMD board.
DMDPWRGOOD	P24	LVCMOS18_I	HI	—	Connect to DMDPWRGOOD on DMD board.
PWRGOOD	H22	LVCMOS18_I	HI	—	Connect to Power Good on DLPC964 Controller board.
LED_PWR	AL14	LVDCI_18_O	HI	—	Enable control output for LED Power Supply
STATUS_LED_R1	AM10	LVDCI_18_O	HI	—	Controller PLL clock circuitry NOT locked Indicator LED output
STATUS_LED_R2	AK13	LVDCI_18_O	HI	—	DMD HSSI interface Sync errors detected Indicator LED output
STATUS_LED_G1	AL10	LVDCI_18_O	HI	—	Controller PLL clock circuitry locked Indicator LED output
STATUS_LED_G2	AK8	LVDCI_18_O	HI	—	No DMD HSSI interface Sync errors detected Indicator LED output
LED_HEARTBEAT	AK14	LVDCI_18_O	HI	—	Heartbeat Indicator LED output
INIT_DONE	F23	LVDCI_18_O	HI	—	Connect to Apps FPGA C964_INIT_DONE
M0_0	AA10	LVCMOS18_I	—	—	DLPC964 Configuration — connect to 1.8V
M1_0	Y10	LVCMOS18_I	—	—	DLPC964 Configuration — connect to GND
M2_0	W10	LVCMOS18_I	—	—	DLPC964 Configuration — connect to GND

Table 4-1. Pin Functions (continued)

PIN		I/O TYPE[1]	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
TDO_0	AA25	LVCMOS18_O	—	—	JTAG Data out of DLPC964. Connects to JTAG return TDO on JTAG connector
TDI_0	AB25	LVCMOS18_I	—	—	JTAG Data into DLPC964. Connects to JTAG input TDI on JTAG connector
TMS_0	W25	LVCMOS18_I	—	—	JTAG Data. Connects to JTAG TMS on JTAG connector
TCK_0	Y25	LVCMOS18_I	—	—	JTAG Clock. Connects to JTAG TCK on JTAG connector
INIT_B_0	T10	LVCMOS18_O	—	—	DLPC964 Configuration. Pull up to 1.8V with a 4.7KΩ resistor.
CFGBVS_0	U10	LVCMOS18_I	—	—	DLPC964 Configuration. Connect to GND.
PROGRAM_B_0	V10	LVCMOS18_O	—	—	DLPC964 Configuration. Pull up to 1.8V with a 4.7KΩ resistor.
DONE_0	AB10	LVCMOS18_O	HI	—	DLPC964 Configuration. Pull up to 1.8V with a 330Ω resistor.
K_DATA[0]	K22	LVDCI_18_O	—	CLK_K	Bit 64 of user_k_tdata[]
K_DATA[1]	K23	LVDCI_18_O	—	CLK_K	Bit 65 of user_k_tdata[]
K_DATA[2]	M23	LVDCI_18_O	—	CLK_K	Bit 66 of user_k_tdata[]
K_VALID	K24	LVDCI_18_O	—	CLK_K	
K_DATA[3]	L23	LVDCI_18_O	—	CLK_K	Bit 67 of user_k_tdata[]
CLK_K	L24	LVDCI_18_I	—	—	K_DATA Clock input (156.25MHz)
K_DATA[4]	L25	LVDCI_18_O	—	CLK_K	Bit 68 of user_k_tdata[]
FAN_PWM	N22	LVDCI_18_O	—	—	To DLPC964 Controller Fan connector
TESTMUX0	AE11	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX1	AE13	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX2	AE14	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX3	AF10	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX4	AF11	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX5	AF13	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX6	AF14	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX7	AG10	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX8	AG11	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX9	AG12	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX10	AG13	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX11	AH12	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX12	AH13	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX13	AH14	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX14	AJ9	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
TESTMUX15	AJ10	LVDCI_18_O	—	—	No connect. For access to test point output route to test via.
VN_0	Y17	—	—	—	Connect to GND.
VP_0	W18	—	—	—	Connect to GND.
VREFN_0	W17	—	—	—	Connect to GND.
VREFP_0	Y18	—	—	—	Connect to GND.

Table 4-1. Pin Functions (continued)

PIN		I/O TYPE[1]	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
DXN_0	AA17	—	—	—	Connect to GND.
DXP_0	AA18	—	—	—	Connect to GND.
VCCADC_0	V18	PWR	—	—	Connect to 1.8V.
VCCBATT_0	U25	PWR	—	—	Connect to GND.
VCCO	A12, A22, AC11, AE10, AE20, AF17, AG14, AG24, AH11, AH21, AJ8, AJ18, AK15, AK25, AL12, AL22, AM9, AM19, AN16, AN26, AP13, AP23, B9, B19, C16, C26, D13, D23, E10, E20, F17, G14, G24, H11, H21, J18, K15, K25, L12, L22, M19, N16, P13, P23	PWR	—	—	Power. P1V8
VCCINT	AA12, AA16, AA22, AA24, AB11, AB15, AB17, AB23, AC10, AC12, AC16, AC18, AC22, AC24, AD11, AD15, AD17, AD23, AD25, R10, R12, R14, R16, R18, R22, R24, T11, T13, T15, T17, T21, T23, T25, U12, U14, U16, U18, U22, U24, V11, V15, V23, W12, W16, W22, W24, Y11, Y15, Y23	PWR	—	—	Power. P1V0_CORE
VCCAUX	AA14, AA20, AB13, AB21, AC14, AC20, AD13, AD21, U20, V13, V21, W14, W20, Y13, Y21	PWR	—	—	Aux Power. P1V8
VCCBRAM	AB19, AD19, R20, T19, V19, Y19	PWR	—	—	Power. P1V0_CORE
MGTAVCC	AA29, AC6, AC29, AE6, AE29, AG6, AG29, AJ6, AJ29, AL6, AL29, AN6, AN29, C6, C29, E6, E29, G6, G29, J6, J29, L6, L29, N6, N29, R6, R29	PWR	—	—	Power. P1V0_MGT
MGTVCCAUX	U6, U29, W6, W29	PWR	—	—	Aux Power. P1V8
MGTAVTT	AC2, AC33, AD3, AD32, AG2, AG33, AH3, AH32, AL2, AL33, AM3, AM32, C2, C33, D3, D32, G2, G33, H3, H32, L2, L33, M3, M32, R2, R33, T3, T32, W2, W33, Y3, Y32	PWR	—	—	Power. P1V2
GNDADC_0	V17	GND	—	—	ADC Ground

Table 4-1. Pin Functions (continued)

PIN		I/O TYPE[1]	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
GND	A1, A2, A5, A6, A7, A17, A27, A28, A29, A30, A33, A34, AA1, AA2, AA9, AA11, AA13, AA15, AA19, AA21, AA23, AA26, AA30, AA33, AA34, AB3, AB4, AB7, AB8, AB9, AB12, AB14, AB16, AB18, AB20, AB22, AB24, AB26, AB27, AB28, AB31, AB32, AC1, AC5, AC9, AC13, AC15, AC17, AC19, AC21, AC23, AC25, AC26, AC30, AC34, AD4, AD7, AD8, AD9, AD10, AD12, AD20, AD22, AD24, AD26, AD27, AD28, AD31, AE1, AE2, AE5, AE9, AE15, AE25, AE26, AE30, AE33, AE34, AF3, AF4, AF7, AF8, AF9, AF12, AF22, AF26, AF27, AF28,AF31, AF32, AG1, AG5, AG7, AG8, AG9, AG19, AG26, AG27, AG28, AG30, AG34, AH4, AH7, AH8, AH9, AH16, AH26, AH27, AH28, AH31, AJ1, AJ2, AJ5, AJ7, AJ13, AJ23, AJ28, AJ30, AJ33, AJ34, AK3, AK4, AK7, AK10, AK20, AK28, AK31, AK32, AL1, AL5, AL7, AL17, AL27, AL28, AL30, AL34, AM4, AM7, AM14, AM24, AM28, AM31, AN1, AN2, AN5, AN7, AN11, AN21, AN28, AN30, AN33, AN34, AP3, AP4, AP7, AP8, AP18, AP28, AP31, AP32, B3, B4, B7, B14, B24, B28, B31, B32, C1, C5, C7, C11, C21, C28, C30, C34, D4, D7, D8, D18, D28, D31, E1, E2, E5, E7, E15, E25, E28, E30, E33, E34, F3, F4, F7, F8, F9, F12, F22, F26, F27, F28, F31, F32, G1, G5, G9, G19, G26, G30, G34, H4, H7, H8, H9, H16, H26, H27, H28, H31, J1, J2, J5, J9, J13, J23, J26, J30, J33, J34, K3, K4, K7, K8, K9, K10, K20, K26, K27, K28, K31, K32, L1, L5, L9, L17, L26, L30, L34, M4, M7, M8, M9, M14, M24, M26, M27, M28, M31, N1, N2, N5, N9, N11, N21, N26, N30, N33, N34, P3, P4, P7, P8, P9, P18, P26, P27, P28, P31, P32, R1, R5, R9, R15, R17, R19, R21, R26, R30, R34, T4, T7, T8, T9, T12, T14, T16, T18, T20, T22, T24, T26, T27, T28, T31, U1, U2, U5, U9, U11, U13, U15, U17, U19, U21, U23, U26, U30, U33, U34, V3, V4, V7, V8, V9, V12, V14, V16, V20, V22, V24, V26, V27, V28, V31, V32, W1, W5, W9, W11, W13, W15, W19, W21, W23, W26, W30, W33, Y4, Y7, Y8, Y9, Y12, Y14, Y16, Y20, Y22, Y24, Y26, Y27, Y28, Y31	GND	—	—	—
RESERVED	R23	—	—	—	Pull up to 1.8V with 100Ω resistor
RESERVED	R25	—	—	—	Pull down to GND with 100Ω resistor
RESERVED	AE12	—	—	—	Pull up to 1.8V with 100Ω resistor
RESERVED	AD14	—	—	—	Pull down to GND with 100Ω resistor
RESERVED	G7	—	—	—	Pull up to 1.2V with 100Ω resistor
RESERVED	G8	—	—	—	Connect to 1.2V
RESERVED	G27	—	—	—	Connect to 1.2V
RESERVED	G28	—	—	—	Pull up to 1.2V with 100Ω resistor

Table 4-1. Pin Functions (continued)

PIN		I/O TYPE[1]	ACTIVE (HI OR LO)	CLOCK SYSTEM	DESCRIPTION
NAME	NO.				
UNUSED	A8, A9, A10, A11, A13, A14, A15, A16, A18, A19, A20, A21, A23, A24, AC3, AC4, AC7, AC8, AC27, AC28, AC31, AC32, AD5, AD6, AD16, AD18, AD29, AD30, AE3, AE4, AE7, AE8, AE16, AE17, AE18, AE19, AE21, AE22, AE23, AE24, AE27, AE28, AE31, AE32, AF5, AF6, AF15, AF16, AF18, AF19, AF20, AF21, AF23, AF24, AF25, AF29, AF30, AG3, AG4, AG15, AG16, AG17, AG18, AG20, AG21, AG22, AG23, AG25, AG31, AG32, AH5, AH6, AH10, AH15, AH17, AH18, AH19, AH20, AH22, AH23, AH24, AH25, AH29, AH30, AJ11, AJ15, AJ16, AJ17, AJ19, AJ20, AJ21, AJ22, AJ24, AJ25, AJ26, AJ27, AK5, AK6, AK11, AK16, AK17, AK18, AK19, AK21, AK22, AK23, AK24, AK26, AK27, AK29, AK30, AL3, AL4, AL8, AL11, AL13, AL15, AL16, AL18, AL19, AL20, AL21, AL23, AL24, AL25, AL26, AL31, AL32, AM5, AM6, AM11, AM15, AM16, AM17, AM18, AM20, AM21, AM22, AM23, AM25, AM26, AM27, AM29, AM30, AN13, AN15, AN17, AN18, AN19, AN20, AN22, AN23, AN24, AN25, AN27, AP5, AP6, AP10, AP15, AP16, AP17, AP19, AP20, AP21, AP22, AP24, AP25, AP26, AP27, AP29, AP30, B5, B6, B8, B10, B11, B12, B13, B15, B16, B17, B18, B20, B21, B22, B29, B30, C3, C4, C8, C9, C10, C12, C13, C14, C15, C17, C18, C19, C20, C22, C23, C24, C25, C31, C32, D5, D6, D9, D10, D11, D12, D14, D15, D16, D17, D19, D20, D21, D22, D29, D30, E3, E4, E8, E9, E11, E12, E13, E14, E16, E17, E18, E19, E21, E22, E31, E32, F5, F6, F10, F11, F13, F14, F15, F16, F18, F19, F20, F21, F29, F30, G10, G11, G12, G13, G15, G16, G17, G18, G20, G21, G22, G23, H5, H6, H10, H12, H13, H14, H15, H17, H18, H19, H20, H23, H29, H30, J3, J4, J7, J8, J10, J11, J12, J14, J15, J16, J17, J19, J20, J21, J27, J28, J31, J32, K5, K6, K11, K12, K13, K14, K16, K17, K18, K19, K21, K29, K30, L3, L4, L7, L8, L10, L11, L13, L14, L15, L16, L18, L19, L20, L21, L27, L28, L31, L32, M10, M11, M12, M13, M15, M16, M17, M18, M20, M21, N7, N8, N10, N12, N13, N14, N15, N17, N18, N19, N20, N23, N24, N25, N27, N28, P1, P2, P10, P11, P12, P14, P15, P16, P17, P19, P20, P21, P22, P25, P33, P34, R11, R13, T1, T2, T33, T34, U3, U4, U7, U8, U27, U28, U31, U32, V1, V2, V33, V34, W3, W4, W31, W32, Y1, Y2, Y33, Y34	NC			

(1) I = Input, O = Output, B = Input or Output, GND = Ground, PWR = Power, NC = No Connect.

5 Specifications

See (1)

5.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
ELECTRICAL				
V_{CCINT}	Internal supply voltage(2)	–0.5	1.1	V
V_{CCBRAM}	Block RAM supply voltage(2)	–0.5	1.1	V
V_{CCAUX}	Auxiliary supply voltage(2)	–0.5	2.0	V
V_{CCAUX_IO}	Auxiliary supply voltage(2)	–0.5	2.06	V
V_{CCO}	Output drivers supply voltage for 1.8V I/O banks(2)	–0.5	2.0	V
$V_{MGTAVCC}$	Supply voltage for GTH transceivers(2)	–0.5	1.1	V
$V_{MGTAVTT}$	Supply voltage for GTH transmitter and receiver termination circuits(2)	–0.5	1.32	V
$V_{MGTVCCAUX}$	Auxiliary voltage supply for the transceivers(2)	–0.5	1.935	V
V_I	Input voltage range for 1.8V I/O banks(3)	–0.55	V_{CCO} + 0.55	V
	Input voltage range for GTH receivers(3)	–0.5	1.26	V
ENVIRONMENTAL				
T_J	Junction temperature		+125	°C
T_{stg}	Storage temperature (ambient)	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal GND.
(3) Applies to external input and bidirectional buffers

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

over operating free-air temperature range (unless otherwise noted)

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
ELECTRICAL					
V_{CCINT}	1V supply voltage, core logic	0.97	1.00	1.03	V
V_{CCBRAM}	1V supply voltage, Block RAM	0.97	1.00	1.03	V
V_{CCAUX}	1.8V supply voltage, Auxiliary	1.71	1.80	1.89	V
V_{CCAUX_IO}	1.8V supply voltage, Auxiliary I/O	1.71	1.80	1.89	V
V_{CCO}	1.8V supply voltage, I/O for VCCO_0, 14, 15, 16, 17, 34, 35, 36	1.71	1.80	1.89	V
$V_{MGTAVCC}$	1V supply voltage, GTH transceivers	0.97	1.0	1.08	V
$V_{MGTAVTT}$	1.2V supply voltage, GTH transmitter and receiver termination circuits	1.17	1.2	1.23	V
$V_{MGTVCCAUX}$	1.8V supply voltage, Auxiliary voltage supply for transceivers	1.75	1.80	1.85	V

5.3 Recommended Operating Conditions (continued)

			MIN	NOM	MAX	UNIT
V_I	Input Voltage	1.8V LVCMOS	0	—	V_{CCO}	V
		GTH Differential pk-pk (DVPPIN)	0.15	—	1.250	V
		GTH Single ended	–0.4	—	$V_{MGTAVTT}$	V
		GTH Common mode	—	2/3 $V_{MGTAVTT}$	—	mV
V_O	Output voltage	1.8V LVCMOS	0	—	V_{CCO}	V
		GTH Differential pk-pk (DVPPOUT)	0.8	—	—	V
		GTH Common mode	$V_{MGTAVTT}$–DVPPOUT/4			mV
ENVIRONMENTAL						
T_A	Operating ambient temperature		0	—	85	°C
P_D	Continuous total power dissipation		—	—	18	W

5.4 Thermal Information

THERMAL METRIC(1)		DLPC964 ZUM (FCBGA) 1158 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	8.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.3	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	0.16	°C/W

(1) Refer to the *7 Series FPGAs Packaging and Pinout Product Specification Guide* for complete thermal specifications of the XC7VX415T.
(2) In still air

over operating free-air temperature range (unless otherwise noted)

5.5 Electrical Characteristics

PARAMETER			MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	1.8V LVCMOS	65% V_{CCO}	—	—	V
V_{IL}	Low-level input voltage	1.8V LVCMOS	—	—	35% V_{CCO}	V
V_{OH}	High-level output voltage	1.8V LVCMOS	V_{CCO} – 0.450	—	—	V
V_{OL}	Low-level output voltage	1.8V LVCMOS	—	—	0.450	V
V_{ID}	Differential peak-to-peak input voltage (external AC coupled)	1.0V HSTL_1	0.150	—	1.250	V
V_{ICM}	Common mode input voltage	1.0V HSTL_1	—	2/3 $V_{MGTAVTT}$	—	V
V_{IN}	Single-ended input voltage	1.0V HSTL_1	–0.400	—	$V_{MGTAVTT}$	V
V_{OD}	Differential peak-to-peak output voltage	1.0V HSTL_1	0.800	—	—	V
V_{ID}	Input differential voltage	1.8V LVDS	0.100	0.350	0.600	V
V_{ICM}	Input common-mode voltage	1.8V LVDS	0.300	1.200	1.425	V
V_{OH}	High-level output voltage	1.8V LVDS	—	—	1.675	V
V_{OL}	Low-level output voltage	1.8V LVDS	0.825	—	—	V
V_{OD}	Output differential voltage	1.8V LVDS	0.247	0.350	0.600	V
V_{OCM}	Output common-mode voltage	1.8V LVDS	1.000	1.250	1.425	V
C_I	Input capacitance		—	8	—	pF
I_{CCINT}	1.0V supply voltage range, core supply	1.0V			3.200	A

5.5 Electrical Characteristics (continued)

PARAMETER			MIN	TYP	MAX	UNIT
$I_{MGTAVCC}$ + I_{CCBRAM}	1.0V supply current range, transceiver and BRAM supply	1.0V			5.000	A
$I_{MGTAVTT}$	1.2V supply current range, I/O transceiver termination supply	1.2V			1.400	A
I_{CCAUX} + I_{CCAUX_IO} + I_{CCO}+ $I_{MGTVCCAUX}$	1.8V supply current range, auxiliary, auxiliary I/O, CCO, and auxiliary supply for transceivers	1.8V			0.160	A

5.6 Timing Requirements

			MIN	NOM	MAX	UNIT
f_{cgt}	Clock frequency, GTTX_CHn_REFCLK(1) and GTRX_CHn_REFCLK(1)			100		MHz
f_{cui}	Clock frequency, REFCLK_UI(1)			156.25		MHz
f_{cs}	Clock frequency, SYS_CLK100(1)			100		MHz
f_{cdmd}	Clock frequency, DMD_GTREFCLK_IN_n(1)				112.5	MHz
t_{cgt}	Cycle time, GTRX_CHn_REFCLK				10	ns
$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)			5	ns
$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)			5	ns
t_t	Transition time, tt = tf / tr	20% to 80% reference points (signal)		200		ps
t_{jp}	Period Jitter CHn_GTRX	Total Sinusoidal Period Jitter	0.3			UI
t_{sk}	Skew, CHn_GTRX(1)	Lane to lane within a single Input Channel			200	ps

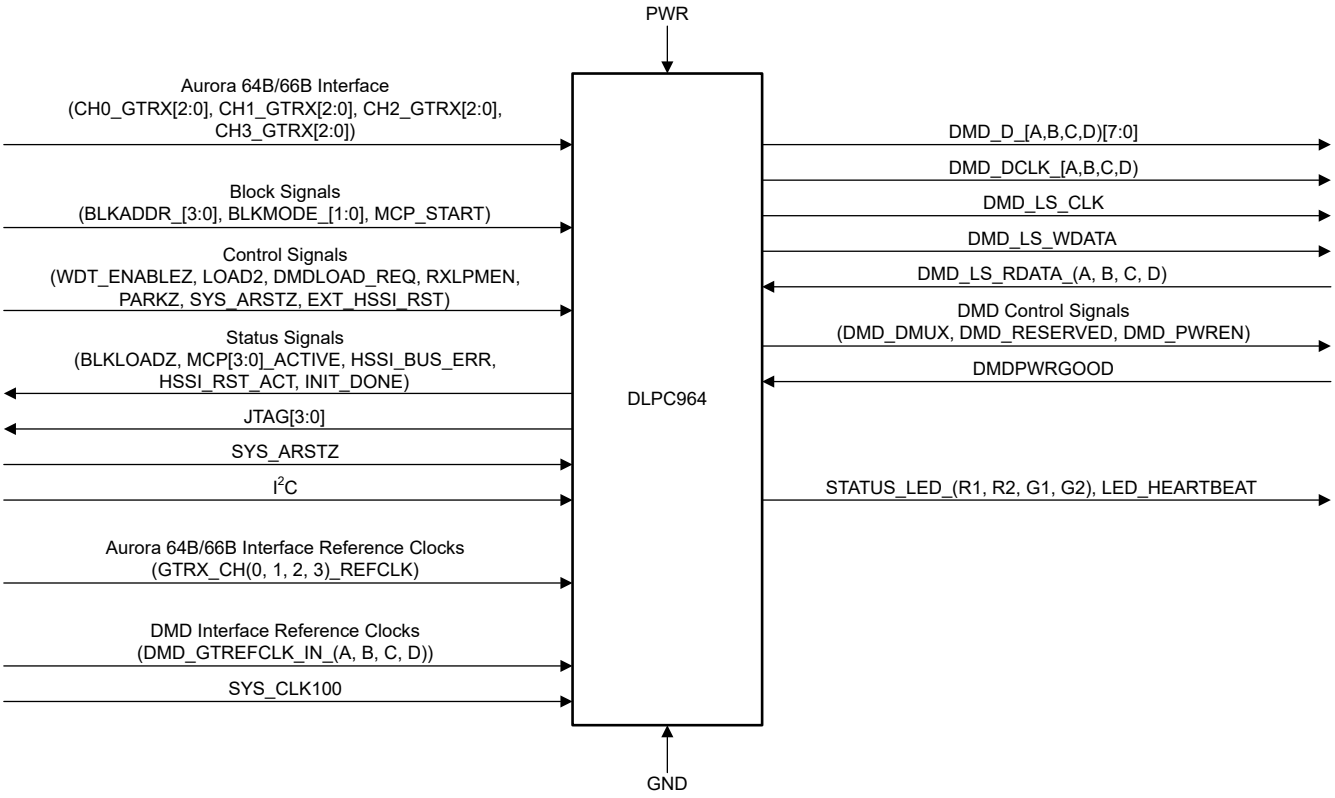
(1) Preferred Duty Cycle is 50%.

6 Detailed Description

6.1 Overview

The DLPC964 digital controller provides a reliable high speed data pipe to the DMD. The Aurora 64B/66B high speed serial (HSS) digital input for the high-speed pattern data is configured for the required timing requirements of the DMD. The DMD reflects light by using 1-bit binary encoded patterns, where each mirror is a one-to-one pixel-to-mirror mapping of the pattern data.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input High-Speed Serial (HSS) Interface

The data input interface is based upon the Advanced Micro Devices (AMD) LogiCORE™ IP Aurora 64B/66B core, and consists of four input data buses each made up of three high-speed serial data lanes: CH0_GTRX0..2, CH1_GTRX0..2, CH2_GTRX0..2, and CH3_GTRX0..2.

Each bus also includes a Data Clock for each of the four high-speed data lanes: GTTX_CH0_REFCLK, GTTX_CH1_REFCLK, GTTX_CH2_REFCLK, and GTTX_CH3_REFCLK.

6.3.2 Block Interface

The signals BLKADDR_[3:0] and BLKMODE[1:0] are used to designate which DMD Block(s) is to be issued a Mirror Clocking Pulse (MCP), Block Clear, or Block Set.

6.3.3 Control Interface

6.3.3.1 Watchdog

The DLPC964 controller contains a watchdog timer that initiates a global DMD mirror clocking pulse in the event that any DMD block did not receive a mirror clocking pulse within 10 seconds. This auto-mirror clocking pulse function can be disabled by asserting WDT_ENABLEZ high. Disabling the watchdog is not recommended unless the user ensures that a mirror clocking pulse to the entire DMD occurs within 10 seconds. During the time the DLPC964 and DMD are not actively loading patterns, park the DMD mirrors. See Park Control for information about parking the DMD mirrors.

6.3.3.2 LOAD2

LOAD2 functionality provides improved global binary pattern rates for applications that can trade diminished vertical resolution for higher pattern rates. Examples of these types of applications are shutter or chopper applications and vertical structured light patterns. Asserting LOAD2 causes the DLPC964 controller and attached DMD to load two rows for every row of data sent, reducing the pattern load time to ½ of a full DMD load. Loading each block will only require ½ the number of DMD row data (136 ÷ 2 = 68 rows per block). This function does not reduce the MCP timing.

This mode can be enabled through either asserting the LOAD2 pin high or setting a bit in the DLPC964 register to select LOAD2 mode (vs normal load mode), and then writing another bit requesting the DLPC964 update the operational mode of the DMD via the LSIF, which causes all DMD data pixel updates (and MCPs) to cease, and the DMD to reinitialize. Once the new configuration settings are reprogrammed into the DMD, the LSIF can return to processing MCP commands based on the DLPC964 inputs.

6.3.3.2.1 LOAD2 Row Addressing

In LOAD2 mode, automatic increment mode and row address mode can still be used as before, but the largest addressable row is (VRes ÷ 2) – 1, where VRes = the vertical resolution of the DMD. The addressable vertical resolution is reduced by two, although the physical resolution is unchanged. Automatic increment address mode automatically increments the row address input by one (or decrement by one for N/S flip). The row address input is remapped, as shown in Table 6-1 below:

Table 6-1. LOAD2 Row Address Mapping

ROW ADDRESS INPUT	PHYSICAL ROWS LOADED ON DMD
0	0, 1
1	2, 3
2	4, 5
3	6, 7
N	2N, 2N + 1
(VRes ÷ 2) – 1	VRes – 2, VRes – 1

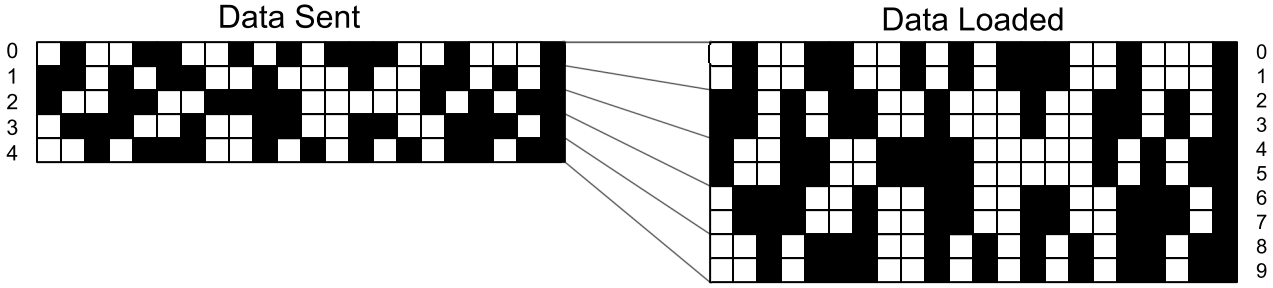


Figure 6-1. Example LOAD2 Address Mapping

6.3.3.2.2 LOAD2 Block Clears

While LOAD2 is enabled, block clear requests are ignored. To load using LOAD2 followed by block clear request(s), deassert LOAD2 at the beginning of the MCP request(s) preceding the block clear request(s). Reassert LOAD2 at the beginning of the MCP request(s) preceding the next desired LOAD2 operation. This ensures the DLPC964 controller has sufficient time to disable or enable LOAD2 before data is loaded or block clear(s) are requested. Refer to block clear regarding block clear operation.

6.3.3.3 Receiver Low Power Mode Enable

Set to 0 for low power mode equalization.

6.3.3.4 DMD High Speed Serial Interface (HSSI) Reset

The EXT_HSSI_RST signal can be asserted to signal the DLPC964 to reset the High Speed Serial Interface (HSSI) to the DMD. When reset, the system will automatically perform bus training for the HSSI interface between the DLPC964 and DMD.

6.3.3.5 DMD Power Enable

The DLPC964 controller utilizes the DMD_PWREN signal to control the power supplies for the attached DMD. When asserted, the DMD_PWREN signal will enable the power supplies for the attached DMD.

6.3.4 User K-Data Interface

The high-speed interface between the applications FPGA and DLPC964 controller allows the use of the user K-data interface within the Aurora 64B/66B Streaming Protocol. The following signals are used in this interface:

- CLK_K
- K_DATA[4:0]
- K_VALID

Use these bits to transmit information across the high-speed interface between the DLPC964 controller and the applications FPGA. USERK 0x0 packet bits 76:72 are available as follows:

- bit[72] = K_DATA0
- bit[73] = K_DATA1
- bit[74] = K_DATA2
- bit[75] = K_DATA3
- bit[76] = K_DATA4

See the *AMD PG074 Application Note* for more information on how to use the user K-data interface.

6.3.5 Status Interface

6.3.5.1 INIT_DONE

When power is applied, the INIT_DONE signal goes high to indicate the DLPC964 has completed loading the configuration file from the configuration Flash PROM.

6.3.5.2 MCP_ACTIVE

The MCP Active[3:0] signals (Mirror Clocking Pulse Active [3:0]) are four outputs from the DLPC964 to the applications FPGA or customer front end to identify when an MCP is currently in progress. A maximum of four MCPs can happen at once and are represented by each of the four MCP_Active[3:0] outputs.

6.3.5.3 BLKLOADZ

The DLPC964 controller provides an output signal to the Applications FPGA or customer front-end named BLKLOADZ that frames the loading of the most recently received block of data as it is being written to the DMD. This signal shall transition low when a DMD block load begins over the HSSI DMD interface and shall transition back high when the DMD block load is complete.

6.3.5.4 High-Speed Serial Interface (HSSI) Bus Error

The HSSI_BUS_ERR output signal from the DLPC964 controller indicates that an error has occurred on the high-speed serial interface bus between the DLPC964 controller and the attached DMD during initialization. The EXT_HSSI_RST signal can be asserted to reset the HSSI interface. The HSSI_RST_ACT signal from the DLPC964 controller is asserted to indicate the HSSI bus between the DLPC964 controller and the attached DMD is actively performing a reset. When the reset is complete, this signal is deasserted by the DLPC964 controller.

6.3.5.5 IRQZ

The DLPC964 controller provides an Event Notification signal IRQZ to the Applications FPGA indicating an important event has occurred and that the I^2C Host should query status registers to determine an appropriate course of action. The IRQZ signal is resettable by the I^2C master writing to a register bit in the DLPC964 controller.

6.3.6 Reset, System Clock, and Power Good

6.3.6.1 Controller Reset

The controller reset input SYS_ARSTZ is an active low, asynchronous reset. Asserting SYS_ARSTZ low will reset the logic in the DLPC964 controller back to default state just after configuration is complete. This reset can be sourced from the Applications FPGA or from the customer front end.

6.3.6.2 Main Oscillator Clock

The main reference clock inputs to the DLPC964 controller, SYS_CLK100_N and SYS_CLK100_P, supplied from an oscillator must be 100MHz differential. This clock should be valid prior to releasing SYS_ARSTZ.

6.3.6.3 DMD HSSI Bus Oscillator Clock

The DMD HSSI bus reference clock inputs to the DLPC964 controller, DMD_GTREFCLK_IN_A_N / DMD_GTREFCLK_IN_A_P, DMD_GTREFCLK_IN_B_N / DMD_GTREFCLK_IN_B_P, DMD_GTREFCLK_IN_C_N / DMD_GTREFCLK_IN_C_P, and DMD_GTREFCLK_IN_D_N / DMD_GTREFCLK_IN_D_P, supplied from an oscillator must be 112.5MHz differential. This clock should be valid prior to releasing SYS_ARSTZ.

6.3.6.4 POWERGOOD and DMDPOWERGOOD

The PWRGOOD signal input to the DLPC964 controller allows the controller to monitor that external power and all pertinent power supplies for the DLPC964 controller are within proper regulation. When powering up, the DLPC964 controller is held in reset until the PWRGOOD signal is asserted high. If there is a loss of external power to the power supplies for the DLPC964 controller or a loss of power from one of the DLPC964 power supplies, the PWRGOOD signal input to the DLPC964 controller should be asserted low to indicate a loss of power has occurred. Once PWRGOOD is asserted low, the DLPC964 controller immediately performs a sequence of memory loads to the DMD followed by the mirror park instruction so that the mirrors end up in an un-landed state. See Park Control for more information about parking the DMD.

The DMDPOWERGOOD signal input to the DLPC964 controller allows the controller to monitor all pertinent power supplies for the attached DMD. The interface bus to the attached DMD is not initiated until the DMDPWRGOOD signal is asserted high, indicating that the power supplies are within regulation. If DMDPWRGOOD is ever asserted low during operation, the DLPC964 will update the **MAIN_STATUS_DMDPWRGOOD_FLD** Register Value in the **FPGA_MAIN_STATUS Register** and trigger the **IRQZ** output to the Applications FPGA or customer front end.

6.3.7 I²C Interface

The I²C interface is compliant to I²C specification version 1.0 – 1992, and operates between 100kHz and 400kHz clock rate. The interface allows the user to set controller configuration and provides status information such as:

- Controller and DMD identification
- DMD Type
- Versions
- Controller operating status
- Controller operating modes

Each I²C clock and data I/O require an external 2.2KΩ pull-up resistor to 1.8V. Depending on the speed that is selected and the loading of the interface, a different pullup resistor may be required.

6.3.7.1 Configuration Pins

The I2C_ADDR_SEL[1:0] input pins allow the user to select the DLPC964 I²C secondary address. The table below describes the relationship between the I2C_ADDR_SEL[1:0] pins and the DLPC964 I²C secondary address. If pins are left unconnected, the default address is 0x0C.

The DDC_I2C_SCL is the primary controller input clock. The DDC_I2C_SDA is the bidirectional data signal. Both signals require a 2.2kΩ pullup resistor.

Table 6-2. DLPC964 I²C Secondary Address Selection Table

I2C_ADDR SEL[1]	I2C_ADDR SEL[0]	I²C secondary address
0	0	0x0F
0	1	0x0E
1	0	0x0D
1	1	0x0C

6.3.7.2 Communications Interface

Communications is performed over the I²C interface where the DLPC964 is the secondary device. The DLPC964 secondary address consists of a 7-bit address plus one R/W bit. Communicating with the DLPC964 involves writing to or reading from the registers listed in the register map.

6.3.7.2.1 Command Format

All register addresses are 32-bit in size, where each register contains a 32-bit value. The actual valid bits are shown in each respective register. Most registers contain spare or unused bits. These bits must be treated as *don't-care* during a read operation unless otherwise specified. When writing to spare or unused bits, these bits MUST be set to *0*. Both the register address and the data require the least-significant byte to be first and most-significant byte last. A SUB CMD must precede the register address to indicate the type of operation; whereas 0xF1 indicates a write operation and a 0xF2 indicates a read operation. The following figures show examples of writing and reading to the DESTOP_BUS_SWAP register.

Figure 6-2 shows an I²C primary writing data to the DLPC964, where 0xF1 is required as the SUB CMD followed by the register address and finally the register data.

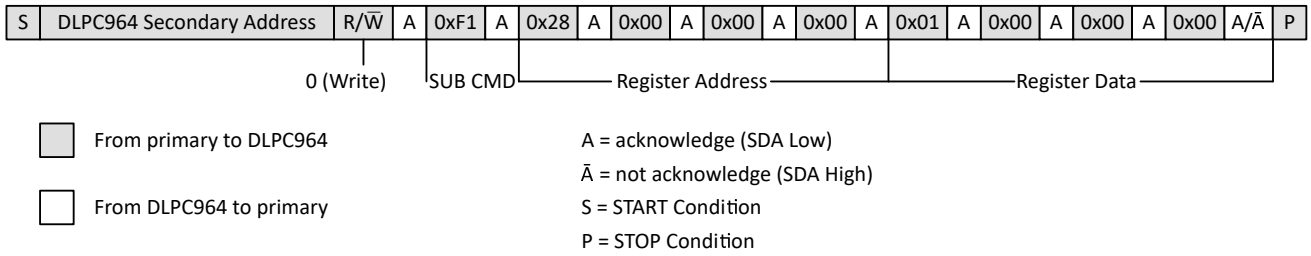


Figure 6-2. Example I²C Primary Writing DLPC964 Register Data

Figure 6-3 shows an I²C primary reading data from the DLPC964, where 0xF2 is required as the SUB CMD followed by the register address. Then the primary performs STOP followed by a START to read the register data.

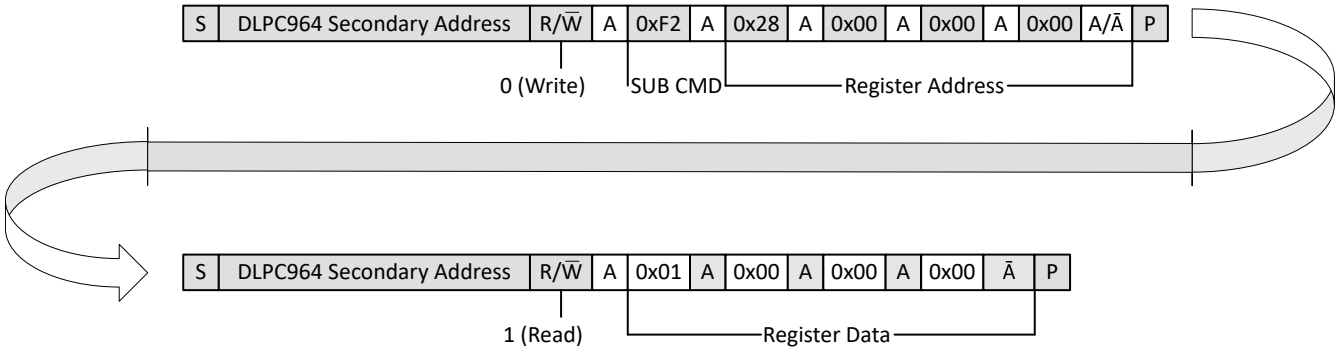


Figure 6-3. Example I²C Primary Reading DLPC964 Register Data

6.3.8 DMD (HSSI) Interface

The DLPC964 Controller DMD interface supports four High Speed Serial Interface (HSSI) output-only interfaces for data transmission, a single low speed LVDS output-only interface for command write transactions, as well as a low speed single-ended input interface used for command read transactions.

6.3.8.1 Park Control

The DLPC964 controller executes parking of the attached DMD when:

1. The PARKZ input to the DLPC964 controller is asserted.
2. The POWERGOOD input to the DLPC964 controller indicates that external power is removed.
3. The SYS_ARSTZ input to the DLPC964 controller is asserted to purposefully reset the DLPC964 controller logics, the DLPC964 controller has safety logics to park the DMD first before resetting all internal logics and registers.

When commanded to park, the DLPC964 controller immediately initiates the process of placing the DMD mirrors into the proper parked state. This includes any preconditioning required for DMD mirror parking. Deassertion of the park state by removing the external PARKZ signal reenables the DMD to update micromirror data. Note that this data is not updated to the active array until the next customer initiated MCP or a watchdog timeout occurs.

The proper sequence for parking the DMD for system power down and the sequence for temporary parking of the DMD to then restart system operation without powering down is outlined in Section 7.4.2.

6.3.8.2 Configurable HSSI Settings

The output differential voltage (V_{od}), driver preemphasis, and driver post-emphasis settings for the HSSI output drivers of the DLPC964 controller can be adjusted from the default settings to modify the performance of the DMD High Speed Serial Interface. Separate control of these settings for each data bus (A, B, C, D) and each data bus clock (A,B,C,D) are available, as well as the common-mode voltage (V_{cm}) settings for the HSSI receiver in the DMD through the I²C register interface in the DLPC964 controller.

Table 6-3 describes the different settings available for the HSSI drivers in the DLPC964 controller. When changing driver output differential voltage (V_{od}), driver preemphasis, and driver post-emphasis settings for the HSSI output drivers of the DLPC964 controller from the default settings, the common-mode voltage (V_{cm}) of the signals at the DMD HSSI receivers can change. Measurement and verification that the input differential voltage (V_{id}) and input common mode voltage (V_{cm}) are within the voltage specifications described in the *Recommended Operation Conditions* section of the DLP991U DMD data sheet is necessary to verify these voltage levels are within the correct specifications after being modified. See the *AMD 7 Series FPGAs GTX/GTH Transceivers User Guide* for more information.

Table 6-3. HSSI Driver Control Settings

TXDIFFCTRL[1]			TXPOSTCURSOR[2]				TXPRECURSOR[3]		
[3:0]	V_{PPD}		[12:8]	Emphasis (dB)	|Coefficient Units|		[20:16]	Emphasis (dB)	|Coefficient Units|
4'b0000	0.269		5'b00000	0.00	0		5'b00000	0.00	0
4'b0001	0.336		5'b00001	0.22	1		5'b00001	0.22	1
4'b0010	0.407		5'b00010	0.45	2		5'b00010	0.45	2
4'b0011	0.474		5'b00011	0.68	3		5'b00011	0.68	3
4'b0100	0.543		5'b00100	0.92	4		5'b00100	0.92	4
4'b0101	0.609		5'b00101	1.16	5		5'b00101	1.16	5
4'b0110	0.677		5'b00110	1.41	6		5'b00110	1.41	6
4'b0111	0.741		5'b00111	1.67	7		5'b00111	1.67	7
4'b1000	0.807		5'b01000	1.94	8		5'b01000	1.94	8
4'b1001	0.866		5'b01001	2.21	9		5'b01001	2.21	9
4'b1010	0.924		5'b01010	2.50	10		5'b01010	2.50	10
4'b1011	0.973		5'b01011	2.79	11		5'b01011	2.79	11
4'b1100	1.018		5'b01100	3.10	12		5'b01100	3.10	12
4'b1101	1.056		5'b01101	3.41	13		5'b01101	3.41	13
4'b1110	1.092		5'b01110	3.74	14		5'b01110	3.74	14
4'b1111	1.119		5'b01111	4.08	15		5'b01111	4.08	15
			5'b10000	4.44	16		5'b10000	4.44	16
			5'b10001	4.81	17		5'b10001	4.81	17
			5'b10010	5.19	18		5'b10010	5.19	18
			5'b10011	5.60	19		5'b10011	5.60	19
			5'b10100	6.02	20		5'b10100	6.02	20
			5'b10101	6.47	21		5'b10101	6.02	21
			5'b10110	6.94	22		5'b10110	6.02	22
			5'b10111	7.43	23		5'b10111	6.02	23
			5'b11000	7.96	24		5'b11000	6.02	24
			5'b11001	8.52	25		5'b11001	6.02	25
			5'b11010	9.12	26		5'b11010	6.02	26
			5'b11011	9.76	27		5'b11011	6.02	27
			5'b11100	10.46	28		5'b11100	6.02	28
			5'b11101	11.21	29		5'b11101	6.02	29
			5'b11110	12.04	30		5'b11110	6.02	30
			5'b11111	12.96	31		5'b11111	6.02	31

(1) The peak-to-peak differential voltage is defined when TXPOSTCURSOR = 5'b00000 and TXPRECURSOR = 5'b00000.
(2) The TXPOSTCURSOR values are defined when the TXPRECURSOR = 5'b00000. Emphasis = $20\log10(V_{high}/V_{low}) = |20\log10(V_{low}/V_{high})|$
(3) The TXPRECURSOR values are defined when the TSPOSTCURSOR = 5'b00000. Emphasis = $20\log10(V_{high}/V_{low}) = |20\log10(V_{low}/V_{high})|$

Table 6-4 describes the different common-mode voltage (V_{cm}) settings available for the HSSI receivers in the DLP991U DMD. This register must be set to best match the input common-mode voltage (V_{cm}) at the DLP991U HSSI receivers. If the common-mode voltage at the DMD HSSI receiver does not match the HSSI receiver common-mode voltage register settings in the DLPC964 controller, the performance of the DMD HSSI can be negatively affected.

Table 6-4. HSSI Receiver Common-Mode Voltage Settings

VCM REGISTER SETTING	VCM INPUT RANGE
3'b000	0.759V – 0.800V
3'b001	0.673V – 0.758V
3'b010	0.587V – 0.672V
3'b011	0.501V – 0.586V
3'b100	0.415V – 0.500V
3'b101	0.329V – 0.414V
3'b110	0.243V – 0.328V
3'b111	0.200V – 0.242V

To modify the HSSI settings at power-up:

1. Hold the PARKZ input to the DLPC964 controller low at power-up.
2. Keeping the PARKZ input held low; after configuration of the DLPC964 Controller is complete, write the desired settings into the appropriate I^2C registers.
3. After all desired registers have been written, release PARKZ to configure the DMD interface with the new settings.

To modify the HSSI settings during normal operation (after power-up):

1. Assert PARKZ low to park the DMD and stop activity on the DMD interface.
2. Wait a minimum of 500µs for the DLPC964 controller and DMD to complete DMD parking sequence.
3. While PARKZ is still asserted low, keeping the DMD in the parked state, assert SYS_ARSTZ low for minimum of 50ms to reset the DLPC964 controller.
4. After asserting SYS_ARSTZ low for a minimum of 50ms and keeping the PARKZ input held low, assert SYS_ARSTZ high.
5. Once configuration of the DLPC964 controller is complete, write the desired settings into the appropriate I^2C registers.
6. After all desired registers have been written, assert PARKZ high to configure the DMD interface with the new settings.

6.3.9 Flash PROM Interface

6.3.9.1 JTAG Interface

The JTAG interface has multiple purposes that can be used in the following manner:

- Program the configuration bit stream directly into the DLPC964
- Perform boundary test and debug of the DLPC964
- Program the configuration bit stream directly into the DLPC964 Configuration Flash

6.4 Device Functional Modes

The following section focuses on the operation of the DLP991U DMD.

6.4.1 DLPC964 Aurora 64B/66B Input Data and Command Write Cycle

Data transactions to the DLPC964 controller are carried out with twelve 10Gbps serial links, arranged into four channels that use the AMD Aurora 64B/66B serial interface. All data transactions to the DLPC964 controller are DMD block based. The DLP991U DMD has a total of 16 DMD blocks, each made up of 4096 columns by 136 rows. A single row of DMD columns is further divided into four segments of 1024 columns and mapped independently to the four Aurora 64B/66B serial input channels. Therefore, to each Aurora 64B/66B input channel, a full DMD block is an array of 1024 columns by 136 rows.

The complete input data and command write cycle to the DLPC964 is:

- Block start with block control word
- DMD bit plane data input
- Block complete (DMDLOAD_REQ and BLKLOADZ)

Please see Section 7.3 for more details and additional guidelines for loading the DLPC964 controller across the Aurora 64B/66B serial interface.

6.4.1.1 Block Mode Operation (Block Start with Block Control Word)

To define the start of a DMD load operation, the DLPC964 must receive a block control word packet through the Aurora 64B/66B channel 0 input port before receiving any DMD bit plane data. The block control word packet consists of 192 bits and defines:

- The DMD Block being loaded
- The type of DMD load operation being requested
- How many rows of the DMD Block are being loaded
- North / South Flip
- The DLPC964 Aurora 64B/66B input mode (single Aurora channel input or quad Aurora channel input)
- The DMD Segment being loaded (single channel mode only)

The block control word packet is defined according to the table below:

Table 6-5. Block Control Word Fields Definition

Field Position	Field Type	Field Description
gt0_s_axi_user_k_tx_tdata[7:0]	USERK_BLOCK_NUMBER	Must set to all zeroes (0x00). Values other than 0x00 are invalid, DLPC964 controller will ignore the entire 192 bit control word if the field is not zeroes.
gt0_s_axi_user_k_tx_tdata[11:8]	BLOCK_ADDRESS	Indicates the address of the DMD block to which the DLPC964 will apply the operation. 0000: DMD Block 0, 0001: DMD Block 1, 0010: DMD Block 2, ... 1110: DMD Block 14, 1111: DMD Block 15
gt0_s_axi_user_k_tx_tdata[15:12]		Reserved, unused
gt0_s_axi_user_k_tx_tdata[24:16]	ROW_LENGTH	Number of rows the DLPC964 will load the user data into. DLP991U has 136 rows per block, thus valid range is 1-136. All other values, including 0 are invalid. Set to 136 for full block operation, or 1-135 for partial block. Note: This field only used if LOAD_TYPE is 000.

Table 6-5. Block Control Word Fields Definition (continued)

Field Position	Field Type	Field Description
gt0_s_axi_user_k_tx_tdata[34:32]	LOAD_TYPE	000: Block loading. DLPC964 will load the user data to the DMD array area defined by the BLOCK_ADDRESS and ROW_LENGTH 001: Block Clear. DLPC964 will clear the DMD array to zeroes in the entire block defined by BLOCK_ADDRESS. 010: Block Set. DLPC964 will set the DMD array to ones in the entire block defined by BLOCK_ADDRESS Other values: reserved, do not use. Note: when in 001 (block clear) or 010 (block set) operation, the ROW_LENGTH and NORTH_SOUTH_FLIP fields are ignored. Block Set/ Clear operations do not support partial block operation.
gt0_s_axi_user_k_tx_tdata[36]	NORTH_SOUTH_FLIP	Control the direction of data loading within a DMD block. 0: DLPC964 loads data starting and counting up from row 0 1: DLPC964 loads data starting and counting down from row 135 Note: this field only used if LOAD_TYPE is 000
gt0_s_axi_user_k_tx_tdata[29:28]	DMD_SEGMENT	When SINGLE_CHANNEL_MODE = '1', select the DMD segment to which the DLPC964 will apply the operation. DLPC964 controller ignores this field if SINGLE_CHANNEL_MODE = '0'
gt0_s_axi_user_k_tx_tdata[30]	SINGLE_CHANNEL_MODE	1: Single channel operation. Loading the DMD array with only Aurora 64B/66B channel 0. 0: Normal operation. Loading the DMD array with all four Aurora 64B/66B channels.
gt0_s_axi_user_k_tx_tdata[191:31]		Reserved, unused

6.4.1.1.1 Block Clear and Block Set

As described in Table 6-5, block clear and block set operations are controlled through the use of the LOAD_TYPE bits in the block control word sent to the DLPC964 through the Aurora 64B/66B interface at the beginning of a DMD action. When the block clear operation is requested, the SRAM cells in the desired block(s) are written with logic zero data. When the block set operation is requested, the SRAM cells in the desired block(s) are written with logic one data. Both of these load types do not require mirror data to be input to the DLPC964 or mirror data to be sent from the DLPC964 to the DMD.

6.4.1.1.2 Image Orientation—Block Load Increment / Decrement

In Table 6-5, the NORTH_SOUTH_FLIP bits in the block control word determine the direction in which a DMD block is loaded. A '0' in this field loads data starting at row 0 and incrementing the desired number of rows indicated by the ROW_LENGTH bits. A '1' in this field will load data beginning at row 136 and decrementing to the desired number of rows indicated by the ROW_LENGTH bits. Please note that this field is only used if LOAD_TYPE is set to '000' for block load operation. Block clear and block set operations ignore the NORTH_SOUTH_FLIP bits.

6.4.1.1.3 Single Channel Mode

In Table 6-5, the SINGLE_CHANNEL_MODE and DMD_SEGMENT bits in the Block Control Word are used to enable and control Single Channel Mode for the DLPC964 64B/66B input interface. Single Channel Mode operation allows the DLPC964 controller to operate and load input data from a single 64B/66B Input Channel (Channel 0) instead of all four 64B/66B Input Channels. A '1' in the SINGLE_CHANNEL_MODE field enables Single Channel Mode. The DMD_SEGMENT field is utilized to instruct the DLPC964 which DMD Segment the input data is intended to be loaded.

- '00' in the DMD_SEGMENT field loads DMD Segment 0, same as 64B/66B Input Channel 0
- '01' in the DMD_SEGMENT field loads DMD Segment 1, same as 64B/66B Input Channel 1.
- '10' in the DMD_SEGMENT field loads DMD Segment 2, same as 64B/66B Input Channel 2.
- '11' in the DMD_SEGMENT field loads DMD Segment 3, same as 64B/66B Input Channel 3.

6.4.1.2 DMD Bit Plane Data Input (Quad Input Mode)

In normal operation (Quad Input Mode) and once the Block Control Word is sent, the bit plane data for the defined DMD block and rows can be transmitted to the DLPC964 across the four Aurora 64B/66B channels. The input data for each Aurora 64B/66B input channel uses three input lanes. Each lane provides 64 bits of data, which is loaded into each row, as shown in the table below. 725 data transactions are required to fill one DMD block of 136 rows. All four Aurora 64B/66B channels load data concurrently.

Figure 6-4. Single Block Load Format Columns 0–1023

	0															1023	
	0			1			2			3			4			5	Bits
Row	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	
0	0-63	64-127	128-191	192-255	256-319	320-383	384-447	448-511	512-575	576-639	640-703	704-767	768-831	832-895	896-959	960-1023	0
	5		6			7			8			9			10		Bits
	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	
1	0-63	64-127	128-191	192-255	256-319	320-383	384-447	448-511	512-575	576-639	640-703	704-767	768-831	832-895	896-959	960-1023	0
	10	11			12			13			14			15			Bits
	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	
2	0-63	64-127	128-191	192-255	256-319	320-383	384-447	448-511	512-575	576-639	640-703	704-767	768-831	832-895	896-959	960-1023	0
	720			721			722			723			724			725	Bits
	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	
135	0-63	64-127	128-191	192-255	256-319	320-383	384-447	448-511	512-575	576-639	640-703	704-767	768-831	832-895	896-959	960-1023	0
	725																Bits
	1	2															
136	n/a	n/a															
	Unused data														Total Bits		139264

This mapping scheme is repeated for the other three Aurora 64B/66B Input Channels:

- Channel 1 — columns 1024 – 2047
- Channel 2 — columns 2048 – 3071
- Channel 3 — columns 3072 – 4095

6.4.1.3 DMD Bit Plane Data Input (Single Input Mode)

In Single Input Mode, once the block control word is sent with the desired DMD segment defined, the bit plane data for the defined DMD block and rows can be transmitted to the DLPC964 across the Channel 0 Aurora 64B/66B channel. The input data utilizes three input lanes. Each lane provides 64 bits of data, which is loaded into each row, as shown in the table below. 725 data transactions are required to fill one DMD Block of 136 rows.

Table 6-6. Single Block Load Format Columns 0-1023 (DMD_SEGMENT '00')

	0															1023	
	0			1			2			3			4			5	Bits
Row	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	
0	0-63	64-127	128-191	192-255	256-319	320-383	384-447	448-511	512-575	576-639	640-703	704-767	768-831	832-895	896-959	960-1023	0
	5		6			7			8			9			10		Bits
	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	
1	0-63	64-127	128-191	192-255	256-319	320-383	384-447	448-511	512-575	576-639	640-703	704-767	768-831	832-895	896-959	960-1023	0
	10		11			12			13			14			15		Bits
	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	
2	0-63	64-127	128-191	192-255	256-319	320-383	384-447	448-511	512-575	576-639	640-703	704-767	768-831	832-895	896-959	960-1023	0
	720			721			722			723			724			725	Bits
	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	
135	0-63	64-127	128-191	192-255	256-319	320-383	384-447	448-511	512-575	576-639	640-703	704-767	768-831	832-895	896-959	960-1023	0
	725																Bits
	1	2															
136	n/a	n/a															
	Unused data														Total Bits		139264

This mapping scheme is repeated for the other three DMD segments:

- DMD Segment '01' — columns 1024 – 2047
- DMD Segment '10' — columns 2048 – 3071
- DMD Segment '11' — columns 3072 – 4095

6.4.1.4 Block Complete (DMDLOAD_REQ and BLKLOADZ)

Once an Aurora Block Data transfer is complete, the DMDLOAD_REQ signal on the DLPC964 controller must be asserted to signal the end of a DMD block, and trigger it to carry out the operation encoded in the Block Control word.

Please see Section 7.3 for more details and additional guidelines when asserting the DMDLOAD_REQ signal.

6.4.2 DMD Row Operation

The data for the DLP991U DMD is loaded one row at a time with the four HSSI buses into the DMD SRAM array. All four DMD HSSI data buses are required for correct operation. Each HSSI bus consists of a differential clock (DMD_DCLK) and eight differential signal pairs (DMD_D_n[7:0]) that are output from the DLPC964 at 3.6Gbps. All DMD control data is loaded into the DMD across a single HSSI LS bus. The HSSI LS bus consists of a differential clock pair (DMD_LS_CLK), write data differential pair (DMD_LS_WDATA), and a read data single-ended line for each HSSI bus (DMD_LS_RDATA_[D..A]. Mirror data is clocked into the DMD on both the rising and falling edges of the DMD_DCLK, and Control Data is clocked into the DMD on only the rising edge of the DMD_LS_CLK. Data loading does not cause mirror switching until an MCP operation is completed.

DMD row loads must always start on row 0 (or row 135 if north/south flip is enabled) of a particular DMD block. If the data on only one row needs to be updated, all the rows ahead of that particular row in the DMD block must also be loaded. For example, if row 4 of a particular DMD block needs to be updated, rows 0–3 must also be loaded along with the new data for row 4. The ROW_LENGTH field in the block control word be set to 4 and then the mirror data for all 4 rows would be input to the DLPC964.

6.4.3 Block Load Address Select

The DLP991U DMD has 16 MCP blocks with each MCP block being 4096 x 136 bits. The block being loaded can be any one of the 16 MCP blocks on the DMD, with access to each MCP block being independent upon which block was previously loaded or which will be loaded next.

The BLKADDR_[3:0] inputs define which of the 16 DMD blocks to update. Table 6-7 describes how BLKADDR_[3:0] is mapped to the MCP blocks for the different MCP modes available in the DMD. The effects and values of BLKADDR_[3:0] will be restricted based on the block mode selected.

- x1 mode - Use BA[3:0] for single block MCP updates
- x2 mode - Use BA[3:1] for dual block MCP updates
- x4 mode - Use BA[3:2] for quad block MCP updates
- Global mode - No need to use BA[3:0] – updates entire DMD

Block selections shall conform to restrictions inherent in the design of the DLP991U DMD, i.e. x2 and x4 modes indicate only certain blocks can be simultaneously updated at any given time.

6.4.4 Block Mode Select

The DLPC964 digital controller supports the ability to select one of the following block update modes as well as which of the 16 block addresses to update utilizing the BLKMODE_[1:0] inputs.

The block modes allowed are:

- x1 Single MCP block updates at a time is reset (can select block from 0 to 15)
- x2 Two blocks are updated concurrently (adjacent w/address of 0, 1, 2, 3, 4, 5, 6, 7)
- x4 Four blocks are updated concurrently (adjacent w/address of 0, 1, 2, 3)
- x16 All blocks are updated with one command (also called global mode).

These mode input pins must be configured at power up. If the mode is desired to be changed after power up, MCPs must be discontinued, the pins configured to their new values, and the proper I^2C command sent to reconfigure the DMD. See Table 6-7 for detailed information on which blocks are capable of being updated in each mode.

Table 6-7. Block Operations

BLKMODE_1	BLKMODE_0	BLKADDR_3	BLKADDR_2	BLKADDR_1	BLKADDR_0	OPERATION
0	0	0	0	0	0	Update Block 0
0	0	0	0	0	1	Update Block 1
0	0	0	0	1	0	Update Block 2
0	0	0	0	1	1	Update Block 3
0	0	0	1	0	0	Update Block 4
0	0	0	1	0	1	Update Block 5
0	0	0	1	1	0	Update Block 6
0	0	0	1	1	1	Update Block 7
0	0	1	0	0	0	Update Block 8
0	0	1	0	0	1	Update Block 9
0	0	1	0	1	0	Update Block 10
0	0	1	0	1	1	Update Block 11
0	0	1	1	0	0	Update Block 12
0	0	1	1	0	1	Update Block 13
0	0	1	1	1	0	Update Block 14
0	0	1	1	1	1	Update Block 15
0	1	0	0	0	x	Update Blocks 0-1
0	1	0	0	1	x	Update Blocks 2-3
0	1	0	1	0	x	Update Blocks 4-5
0	1	0	1	1	x	Update Blocks 6-7
0	1	1	0	0	x	Update Blocks 8-9
0	1	1	0	1	x	Update Blocks 10-11
0	1	1	1	0	x	Update Blocks 12-13
0	1	1	1	1	x	Update Blocks 14-15
1	0	0	0	x	x	Update Blocks 0-3
1	0	0	1	x	x	Update Blocks 4-7
1	0	1	0	x	x	Update Blocks 8-11
1	0	1	1	x	x	Update Blocks 12-15
1	1	x	x	x	x	Global Mode

6.4.5 Mirror Clocking Pulse (MCP)

A Mirror Clocking Pulse (MCP) sequence begins by setting BLKMODE_[1:0] and BLKADDR_[3:0] for a single, dual, quad, or global block operation. When asserted, MCP_Start causes an MCP on the block(s), and the data stored in the block(s) takes effect on the mirrors of the DMD. Shortly after an MCP is issued, MCPn_ACTIVE goes high, indicating an MCP operation is in progress. During this time, no additional MCPs may be initiated until MCPn_ACTIVE returns low. A typical single block load phased sequence in which consecutive DMD blocks are loaded is illustrated in Figure 6-5. An MCP time is identical for single, dual, quad, or global block operations.

It may take longer to complete an MCP on a block than it does to load a block. The single block load time for the DLP991U DMD is outlined in Table 6-8.

Table 6-8. DMD Overview

DMD	ARRAY	MIRROR SETTLING TIME (µs)	SINGLE ROW LOAD TIME (ns)	SINGLE BLOCK LOAD TIME (µs)	GLOBAL RESET MODE FULL ARRAY (PATTERNS/ SECOND)	QUAD BLOCK RESET MODE FULL ARRAY (PATTERNS/ SECOND)
DLP991U	4096 × 2176	4	37.09	5.04	11,273	12,390

See Section 7.3.1.3 for input data timing description and requirements for any case which involves sending an MCP, block clear, or block set without data loading.

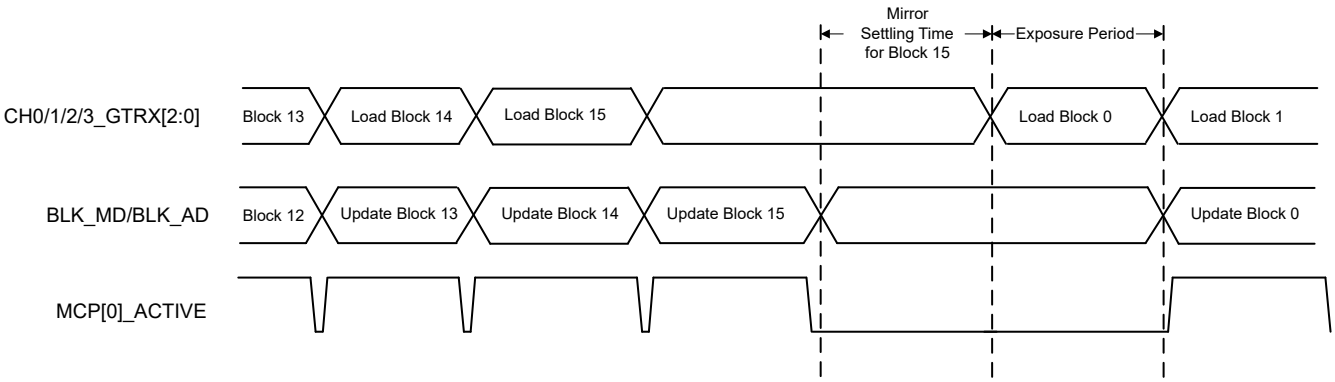


Figure 6-5. Single Block Load Phased Sequence

To fully utilize the DMD bandwidth, load four blocks and then concurrently issue an MCP to the four blocks by setting BLKMODE_[1:0] to 10 and BLKADDR_[3:0] to the proper address for the four blocks being reset. This is illustrated in Figure 6-7.

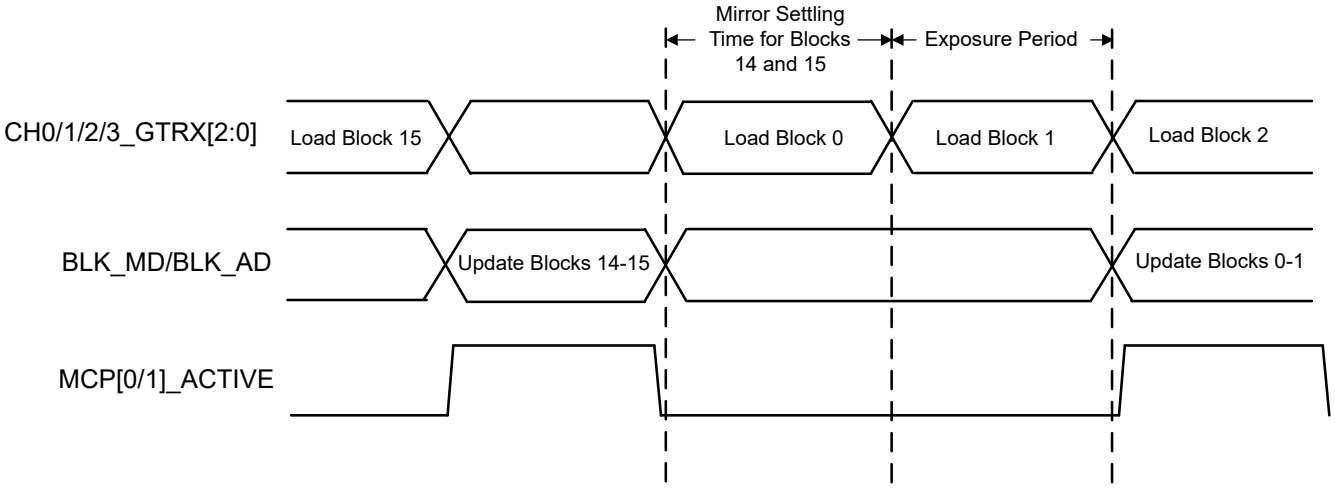


Figure 6-6. Dual Block Load Phased Sequence

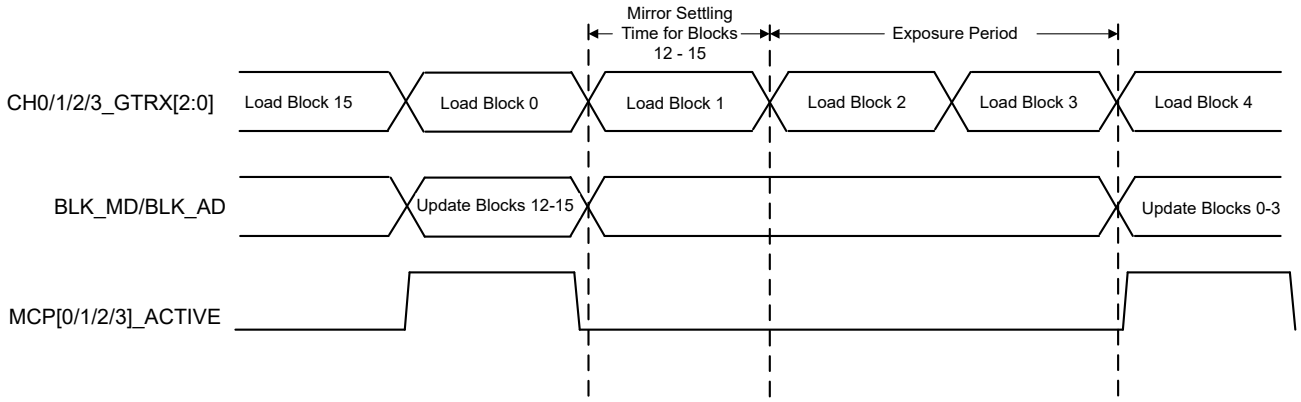


Figure 6-7. Quad Block Load Phased Sequence

It is possible to load other blocks while the block(s) previously issued an MCP is settling. This is illustrated in Figure 6-6 and Figure 6-7, where blocks are reloaded while the mirror settling time is occurring. It is also possible to load other blocks while previously loaded block(s) have an outstanding MCPn_ACTIVE. This is illustrated in Figure 6-7, where block 0 is loaded while MCPn_ACTIVE is asserted for blocks 12–15.

The DLPC964 controller handles all timing activities related to the Mirror Clocking Pulse, including setup and hold timing to reset of each block, the reset waveform generation timing, and any constraints on loading, clearing, fast clearing, or resetting adjacent or non-adjacent blocks. The DLPC964 controller holds off from accepting loading or clearing commands for a specific block while an MCP is in progress.

6.5 Register Map

6.5.1 Register Table Overview

Table 6-9 lists the I^2C accessible memory mapped registers for the DLPC964. Access to the I^2C registers does not begin until INIT_DONE transitions high (logic 1).

Table 6-9. Communication Registers

ADDRESS	REGISTER NAME	DESCRIPTION	SIZE
0x40000000	FPGA_INTERRUPT_STATUS	Input Aurora Channel 0-3 Hard Error Status. Watchdog timeout status	32
0x40000008	FPGA_INTERRUPT_ENABLE_CONTROL	Input Aurora Channel 0-3 Hard Error Output Enable. Watchdog Output Enable	32
0x4000000C	FPGA_MAIN_STATUS	PLL Lock Status. DMD Power Good Status, DMD Parked Status, DMD HSSI Power Status	32
0x40000010	FPGA_VERSION	FPGA Version information including FPGA Build Number and Version Number	32
0x40000014	FPGA_MAIN_CTRL	Watchdog Enable	32
0x4000001C	UBLAZE_INIT_DONE	DMD Init sequence completed	32
0x40000020	SELF_TEST_REG	DMD PRBS7 Test Enable for HSSI Bus and LS Interface Bus.	32
0x40000024	DMDIF_ERROR_STATUS_CLR	DMUX Latch / DMDIF Error Status Clear	32
0x40000028	DMDIF_ERROR_STATUS	DMUX Latch / DMDIF Error Status	32
0x4000002C	PRBS7_MACRO0_TEST_RESULT	DMD Macro 0 PRBS Test Results	32
0x40000030	PRBS7_MACRO1_TEST_RESULT	DMD Macro 1 PRBS Test Results	32
0x40000034	PRBS7_MACRO2_TEST_RESULT	DMD Macro 2 PRBS Test Results	32
0x40000038	PRBS7_MACRO3_TEST_RESULT	DMD Macro 3 PRBS Test Results	32
0x4000003C	PRBS7_TEST_CONTROL	Test Controls for HSSI PRBS Test	32
0x40000040	PRBS7_TEST_RUNSTATUS	Testing Status	32
0x40000044	LS_BUS_TEST_RESULT	LS Bus Testing Results	32
0x40000048	DMD_TYPE	DMD Type Status	32

Table 6-9. Communication Registers (continued)

ADDRESS	REGISTER NAME	DESCRIPTION	SIZE
0x40000100	SSF_FPGA_RST	DLPC964 Reset	32
0x40000200	HSS_RESET	Aurora Reset	32
0x40000204	HSS_CHANNEL_STATUS	Aurora 64B/66B Input Channel Status	32
0x40000208	HSS_LANE_STATUS	Aurora 64B/66B Input Lane Status	32
0x4000020C	HSS_CH0_SOFTERROR_COUNT	Aurora 64B/66B Channel 0 Soft Error Count	32
0x40000210	HSS_CH1_SOFTERROR_COUNT	Aurora 64B/66B Channel 1 Soft Error Count	32
0x40000214	HSS_CH2_SOFTERROR_COUNT	Aurora 64B/66B Channel 2 Soft Error Count	32
0x40000218	HSS_CH3_SOFTERROR_COUNT	Aurora 64B/66B Channel 3 Soft Error Count	32
0x4000021C	HSS_SOFTERROR_COUNT_RESET	Reset Soft Error Count	32
0x40000300	BPG_FEN	Bitplane Pattern Generator Enable	32
0x40000304	BPG_CFG_BLK_ACTIVE	Bitplane Pattern Generator Active Block Configuration	32
0x40000308	BPG_CFG_CTRL	Bitplane Pattern Generator Controls	32
0x40000404	HSI_CH0DMDDAT_GTCTRL	HSSI channel 0 DMD data GT cell control	32
0x40000408	HSI_CH0DMDCLK_GTCTRL	HSSI channel 0 DMD clock GT cell control	32
0x4000040C	HSI_CH1DMDDAT_GTCTRL	HSSI channel 1 DMD data GT cell control	32
0x40000410	HSI_CH1DMDCLK_GTCTRL	HSSI channel 1 DMD clock GT cell control	32
0x40000414	HSI_CH2DMDDAT_GTCTRL	HSSI channel 2 DMD data GT cell control	32
0x40000418	HSI_CH2DMDCLK_GTCTRL	HSSI channel 2 DMD clock GT cell control	32
0x4000041C	HSI_CH3DMDDAT_GTCTRL	HSSI channel 3 DMD data GT cell control	32
0x40000420	HSI_CH3DMDCLK_GTCTRL	HSSI channel 3 DMD clock GT cell control	32
0x40000424	HSI_VCM_VAL	HSSI DMD Vcm Value	32
0x4000051C	TEST_DMD_ID	DMD ID	32
0x40000520	TEST_DMD_FUSE1	DMD Fuse Group 1	32
0x40000524	TEST_DMD_FUSE2	DMD Fuse Group 2	32
0x40000528	TEST_DMD_FUSE3	DMD Fuse Group 3	32
0x4000052C	TEST_DMD_FUSE4	DMD Fuse Group 4	32

Register Definitions

The following designations are used throughout this section of the document:

- **R**—Designates read only
- **W**—Designates write only
- **R/W**—Designates read and write
- **S**—Designates status of register
- **I** —Designates interrupt only
- **P**—Designates pulse only

6.5.1.1 FPGA_INTERRUPT_STATUS Register

The FPGA_INTERRUPT_STATUS register contains the status for the Watchdog timeout and the four Aurora 64B/66B Channels Hard Error status. A '1' can be written to these registers to clear their status.

Table 6-10. FPGA_INTERRUPT_STATUS Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: Reserved	0x0		
1	SPARE	0x0		

Table 6-10. FPGA_INTERRUPT_STATUS Register (continued)

Bit(s)	Description	Reset	Type	Notes
2	Fieldname: **ERROR_RSC_WATCHDOG_FLD** Watchdog timeout. No DMD block reset occurred for 10 seconds. Write '1' to clear this error status bit.	0x0	I	
3	Fieldname: **HSS_CH0_HARD_ERROR_FLD** Input Aurora Channel 0 hard error (This indicates the HSS requires a reset 0x0200 to recover from a hard error condition.) Write '1' to clear this error status bit.	0x0	I	
4	Fieldname: **HSS_CH1_HARD_ERROR_FLD** Input Aurora Channel 1 hard error (This indicates the HSS requires a reset 0x0200 to recover from a hard error condition.) Write '1' to clear this error status bit.	0x0	I	
5	Fieldname: **HSS_CH2_HARD_ERROR_FLD** Input Aurora Channel 2 hard error (This indicates the HSS requires a reset 0x0200 to recover from a hard error condition.) Write '1' to clear this error status bit.	0x0	I	
6	Fieldname: **HSS_CH3_HARD_ERROR_FLD** Input Aurora Channel 3 hard error (This indicates the HSS requires a reset 0x0200 to recover from a hard error condition.) Write '1' to clear this error status bit.	0x0	I	
7	SPARE	0x0		
31:8	UNUSED	0x0		

6.5.1.2 FPGA_INTERRUPT_ENABLE_CONTROL Register

The FPGA_INTERRUPT_ENABLE_CONTROL register contains the Enables for the Watchdog timeout status and the four HSS Channels Hard Error status.

Table 6-11. FPGA_INTERRUPT_ENABLE_CONTROL Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: Reserved	0x0		
1	SPARE	0x0		
2	Fieldname: **ERROR_RSC_WATCHDOG_INT_EN_FLD** '1': allow Watchdog timeout to assert Controller interrupt output. If this bit and FPGA_INTERRUPT_STATUS register bit 2 are set, the Controller interrupt output would be asserted	0x0	W	
3	Fieldname: **HSS_CH0_HARD_ERROR_INT_EN_FLD** '1': allow Input Aurora Channel 0 hard error to assert Controller interrupt output. If this bit and FPGA_INTERRUPT_STATUS register bit 3 are set, the Controller interrupt output would be asserted	0x0	W	

Table 6-11. FPGA_INTERRUPT_ENABLE_CONTROL Register (continued)

Bit(s)	Description	Reset	Type	Notes
4	Fieldname: **HSS_CH1_HARD_ERROR_INT_EN_FLD** '1': allow Input Aurora Channel 1 hard error to assert Controller interrupt output. If this bit and FPGA_INTERRUPT_STATUS register bit 4 are set, the Controller interrupt output would be asserted	0x0	W	
5	Fieldname: **HSS_CH2_HARD_ERROR_INT_EN_FLD** '1': allow Input Aurora Channel 2 hard error to assert Controller interrupt output. If this bit and FPGA_INTERRUPT_STATUS register bit 5 are set, the Controller interrupt output would be asserted	0x0	W	
6	Fieldname: **HSS_CH3_HARD_ERROR_INT_EN_FLD** '1': allow Input Aurora Channel 3 hard error to assert Controller interrupt output. If this bit and FPGA_INTERRUPT_STATUS register bit 6 are set, the Controller interrupt output would be asserted	0x0	W	
7	SPARE	0x0		
31:8	UNUSED	0x0		

6.5.1.3 FPGA_MAIN_STATUS Register

The FPGA_MAIN_STATUS Register contains the status for the DLPC964 PLL Lock, DMD POWERGOOD, DMD Parked Status, and DMD High Speed Interface power status. This register is a read only register, and status bits can only be set/cleared by the DLPC964.

Table 6-12. FPGA_MAIN_STATUS Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **MAIN_STATUS_PLL_LOCKED_FLD** Read-only status 1: DLPC964 PLL locked 0: not locked	0x0	S	
1	Fieldname: **MAIN_STATUS_DMDPWRGOOD_FLD** Read-only status 1: DMD power good from external regulator 0: DMD power not good from external regulator	0x0	S	
2	Fieldname: **MAIN_STATUS_RSCDRC_DMDPARKED_FLD** Read-only status 1: DMD is parked 0: DMD is not parked	0x0	S	
3	Fieldname: **MAIN_STATUS_HSIFPWRON_FLD** Read-only status. 1: DMD high speed interface power on 0: DMD high speed interface power off	0x0	S	
31:4	UNUSED	0x0		

6.5.1.4 FPGA_VERSION Register

The FPGA_VERSION Register contains the Build Number and Version information for the DLPC964 Firmware.

Table 6-13. FPGA_VERSION Register

Bit(s)	Description	Reset	Type	Notes
11:0	Fieldname: **FPGA_BUILD_NUMBER_FLD** FPGA Bitstream Build Number	0x0	R	
19:12	Fieldname: **FPGA_VERSION_MAJOR_FLD** FPGA Bitstream Major Version	0x0	R	
27:20	Fieldname: **FPGA_VERSION_MINOR_FLD** FPGA Bitstream Minor Version	0x0	R	
31:28	Fieldname: **FPGA_BUILD_LEVEL_FLD** FPGA Build Level (not currently used)	0x0	R	

6.5.1.5 FPGA_MAIN_CTRL Register

The FPGA_MAIN_CTRL Register contains the Watchdog Enable bit. Setting this bit to a logic '1' enables the Watchdog, and setting this bit to a logic '0' disables the Watchdog. The Watchdog bit is set to a '1' and enabled as default.

Table 6-14. FPGA_MAIN_CTRL Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **MAINCTRL_WATCHDOG_EN_FLD** ‘1’: enable watchdog ‘0’: disable watchdog	0x01	W	
31:1	UNUSED	0x0		

6.5.1.6 SELF_TEST_REG Register

The SELF_TEST_REG Register contains the PRBS7 Test Enable and LS BUS Test Enable bits. Writing a '1' to either bit will enable the integrity and interface connection test, as described below.

Table 6-15. SELF_TEST_REG Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **PRBS7_TEST_EN** Write ‘1’to this bit to start the DMD interface PRBS7 integrity test. Write ‘1’ to trigger operation (bit will self-cleared back to ‘0’). Read of this bit will always return value of ‘0’.	0x0	w	
1	Fieldname: **LSBUS_TEST_EN** Write to this bit to start the DMD LS bus interface connection test Write ‘1’ to trigger operation (bit will self-cleared back to ‘0’). Read of this bit will always return value of ‘0’.	0x0	w	
31:2	UNUSED	0x0		

6.5.1.7 DMDIF_ERROR_STATUS_CLR Register

The DMDIF_ERROR_STATUS_CLR Register contains the DMUX Latch Reset bit. Writing a '1' to this bit will clear the DMD_ERROR_STATUS register. After 500ns, writing a '0' to this bit will disable the clear and ready the latch to hold the next error bit that might occur.

Table 6-16. DMDIF_ERROR_STATUS_CLR Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **DMUX_LATCH_RESET_FLD** To clear the DMDIF_ERROR_STATUS (0x40000028), write ‘1’ to this register, wait at least 500ns, then write ‘0’ to disable the clear.	0x0	w	
31:1	UNUSED	0x0		

6.5.1.8 DMDIF_ERROR_STATUS Register

The DMDIF_ERROR_STATUS Register contains the results of the DMD Interface Test. A '1' will be set in this register to indicate that the DMD Interface Sync error has occurred. Writing to the DMDIF_ERROR_STATUS_CLR register is the only way to clear this register.

Table 6-17. DMDIF_ERROR_STATUS Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **DMUX_STATUS_FLD** ‘1’: A DMD Interface Sync error has occurred. Once this bit is set, can only be cleared by writing to register 0x40000024 ‘0’: A DMD Interface Sync error has not occurred.	0x0	r	
31:1	UNUSED	0x0		

6.5.1.9 PRBS7_MACRO0_TEST_RESULT Register

The PRBS7_MACRO0_TEST_RESULT Register contains the testing results of DMD High Speed Interface Channel 0. Each lane for this (7:0) can be checked for passing results.

Table 6-18. PRBS7_MACRO0_TEST_RESULT Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **PRBS7_M0LN0_TEST_RESULT_FLD** '1' = DMD Macro 0 lane 0 test passed '0' = test failed	0x0	r	
1	Fieldname: **PRBS7_M0LN1_TEST_RESULT_FLD** '1' = DMD Macro 0 lane 1 test passed '0' = test failed	0x0	r	
2	Fieldname: **PRBS7_M0LN2_TEST_RESULT_FLD** '1' = DMD Macro 0 lane 2 test passed '0' = test failed	0x0	r	
3	Fieldname: **PRBS7_M0LN3_TEST_RESULT_FLD** '1' = DMD Macro 0 lane 3 test passed '0' = test failed	0x0	r	
4	Fieldname: **PRBS7_M0LN4_TEST_RESULT_FLD** '1' = DMD Macro 0 lane 4 test passed '0' = test failed	0x0	r	
5	Fieldname: **PRBS7_M0LN5_TEST_RESULT_FLD** '1' = DMD Macro 0 lane 5 test passed '0' = test failed	0x0	r	

Table 6-18. PRBS7_MACRO0_TEST_RESULT Register (continued)

Bit(s)	Description	Reset	Type	Notes
6	Fieldname: **PRBS7_M0LN6_TEST_RESULT_FLD** '1' = DMD Macro 0 lane 6 test passed '0' = test failed	0x0	r	
7	Fieldname: **PRBS7_M0LN7_TEST_RESULT_FLD** '1' = DMD Macro 0 lane 7 test passed '0' = test failed	0x0	r	
31:8	UNUSED	0x0		

6.5.1.10 PRBS7_MACRO1_TEST_RESULT Register

The PRBS7_MACRO1_TEST_RESULT Register contains the testing results of DMD High Speed Interface Channel 1. Each lane for this interface (7:0) can be checked for passing results.

Table 6-19. PRBS7_MACRO1_TEST_RESULT Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **PRBS7_M1LN0_TEST_RESULT_FLD** '1' = DMD Macro 1 lane 0 test passed '0' = test failed	0x0	r	
1	Fieldname: **PRBS7_M1LN1_TEST_RESULT_FLD** '1' = DMD Macro 1 lane 1 test passed '0' = test failed	0x0	r	
2	Fieldname: **PRBS7_M1LN2_TEST_RESULT_FLD** '1' = DMD Macro 1 lane 2 test passed '0' = test failed	0x0	r	
3	Fieldname: **PRBS7_M1LN3_TEST_RESULT_FLD** '1' = DMD Macro 1 lane 3 test passed '0' = test failed	0x0	r	
4	Fieldname: **PRBS7_M1LN4_TEST_RESULT_FLD** '1' = DMD Macro 1 lane 4 test passed '0' = test failed	0x0	r	
5	Fieldname: **PRBS7_M1LN5_TEST_RESULT_FLD** '1' = DMD Macro 1 lane 5 test passed '0' = test failed	0x0	r	
6	Fieldname: **PRBS7_M1LN6_TEST_RESULT_FLD** '1' = DMD Macro 1 lane 6 test passed '0' = test failed	0x0	r	
7	Fieldname: **PRBS7_M1LN7_TEST_RESULT_FLD** '1' = DMD Macro 1 lane 7 test passed '0' = test failed	0x0	r	
31:8	UNUSED	0x0		

6.5.1.11 PRBS7_MACRO2_TEST_RESULT Register

The PRBS7_MACRO2_TEST_RESULT Register contains the testing results of DMD High Speed Interface Channel 2. Each lane for this (7:0) can be checked for passing results.

Table 6-20. PRBS7_MACRO2_TEST_RESULT Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **PRBS7_M2LN0_TEST_RESULT_FLD** '1' = DMD Macro 2 lane 0 test passed '0' = test failed	0x0	r	
1	Fieldname: **PRBS7_M2LN1_TEST_RESULT_FLD** '1' = DMD Macro 2 lane 1 test passed '0' = test failed	0x0	r	
2	Fieldname: **PRBS7_M2LN2_TEST_RESULT_FLD** '1' = DMD Macro 2 lane 2 test passed '0' = test failed	0x0	r	
3	Fieldname: **PRBS7_M2LN3_TEST_RESULT_FLD** '1' = DMD Macro 2 lane 3 test passed '0' = test failed	0x0	r	
4	Fieldname: **PRBS7_M2LN4_TEST_RESULT_FLD** '1' = DMD Macro 2 lane 4 test passed '0' = test failed	0x0	r	
5	Fieldname: **PRBS7_M2LN5_TEST_RESULT_FLD** '1' = DMD Macro 2 lane 5 test passed '0' = test failed	0x0	r	
6	Fieldname: **PRBS7_M2LN6_TEST_RESULT_FLD** '1' = DMD Macro 2 lane 6 test passed '0' = test failed	0x0	r	
7	Fieldname: **PRBS7_M2LN7_TEST_RESULT_FLD** '1' = DMD Macro 2 lane 7 test passed '0' = test failed	0x0	r	
31:8	UNUSED	0x0		

6.5.1.12 PRBS7_MACRO3_TEST_RESULT Register

The PRBS7_MACRO3_TEST_RESULT Register contains the testing results of DMD High Speed Interface Channel 3. Each lane for this (7:0) can be checked for passing results.

Table 6-21. PRBS7_MACRO3_TEST_RESULT Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **PRBS7_M3LN0_TEST_RESULT_FLD** '1' = DMD Macro 3 lane 0 test passed '0' = test failed	0x0	r	

Table 6-21. PRBS7_MACRO3_TEST_RESULT Register (continued)

Bit(s)	Description	Reset	Type	Notes
1	Fieldname: **PRBS7_M3LN1_TEST_RESULT_FLD** '1' = DMD Macro 3 lane 1 test passed '0' = test failed	0x0	r	
2	Fieldname: **PRBS7_M3LN2_TEST_RESULT_FLD** '1' = DMD Macro 3 lane 2 test passed '0' = test failed	0x0	r	
3	Fieldname: **PRBS7_M3LN3_TEST_RESULT_FLD** '1' = DMD Macro 3 lane 3 test passed '0' = test failed	0x0	r	
4	Fieldname: **PRBS7_M3LN4_TEST_RESULT_FLD** '1' = DMD Macro 3 lane 4 test passed '0' = test failed	0x0	r	
5	Fieldname: **PRBS7_M3LN5_TEST_RESULT_FLD** '1' = DMD Macro 3 lane 5 test passed '0' = test failed	0x0	r	
6	Fieldname: **PRBS7_M3LN6_TEST_RESULT_FLD** '1' = DMD Macro 3 lane 6 test passed '0' = test failed	0x0	r	
7	Fieldname: **PRBS7_M3LN7_TEST_RESULT_FLD** '1' = DMD Macro 3 lane 7 test passed '0' = test failed	0x0	r	
31:8	UNUSED	0x0		

6.5.1.13 PRBS7_TEST_CONTROL Register

The PRBS7_TEST_CONTROL Register controls the PRBS7 Testing available on the DMD High Speed Interface. The duration of the test for each lane can be set, which DMD channel(s) are tested, and which lanes within the selected DMD channel(s) are tested.

Table 6-22. PRBS7_TEST_CONTROL Register

Bit(s)	Description	Reset	Type	Notes
15:0	Fieldname: **PRBS7_TESTDURATION_FLD** PRBS7 run test time for each lane. LSB = 1 ms. Default to zero = 10ms.	0x0	r/w	
16	Fieldname: **PRBS7_DMDCH0_SELECT_FLD** 1' = enable PRBS7 test running on DMD channel 0 (use lane enable to select specific lane)	0x1	r/w	
17	Fieldname: **PRBS7_DMDCH1_SELECT_FLD** 1' = enable PRBS7 test running on DMD channel 1 (use lane enable to select specific lane)	0x1	r/w	
18	Fieldname: **PRBS7_DMDCH2_SELECT_FLD** 1' = enable PRBS7 test running on DMD channel 2 (use lane enable to select specific lane)	0x1	r/w	

Table 6-22. PRBS7_TEST_CONTROL Register (continued)

Bit(s)	Description	Reset	Type	Notes
19	Fieldname: **PRBS7_DMDCH3_SELECT_FLD** 1' = enable PRBS7 test running on DMD channel 3 (use lane enable to select specific lane)	0x1	r/w	
20	Fieldname: **PRBS7_LANE0_TESTENABLE_FLD** 1' = enable PRBS7 test running on lane 0	0x1	r/w	
21	Fieldname: **PRBS7_LANE1_TESTENABLE_FLD** 1' = enable PRBS7 test running on lane 1	0x1	r/w	
22	Fieldname: **PRBS7_LANE2_TESTENABLE_FLD** 1' = enable PRBS7 test running on lane 2	0x1	r/w	
23	Fieldname: **PRBS7_LANE3_TESTENABLE_FLD** 1' = enable PRBS7 test running on lane 3	0x1	r/w	
24	Fieldname: **PRBS7_LANE4_TESTENABLE_FLD** 1' = enable PRBS7 test running on lane 4	0x1	r/w	
25	Fieldname: **PRBS7_LANE5_TESTENABLE_FLD** 1' = enable PRBS7 test running on lane 5	0x1	r/w	
26	Fieldname: **PRBS7_LANE6_TESTENABLE_FLD** 1' = enable PRBS7 test running on lane 6	0x1	r/w	
27	Fieldname: **PRBS7_LANE7_TESTENABLE_FLD** 1' = enable PRBS7 test running on lane 7	0x1	r/w	
31:28	UNUSED	0x0		

6.5.1.14 PRBS7_TEST_RUNSTATUS Register

The PRBS7_TEST_RUNSTATUS Register indicates the status of the DMD High Speed Interface PRBS7 Test. A '1' indicates that a test is currently running, and a '0' indicates that a test is not running.

Table 6-23. PRBS7_TEST_RUNSTATUS

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **PRBS7_TEST_RUNSTATUS_FLD** PRBS7 test status. '1' = PRBS7 test is running '0' = no test running	0x0	r	
31:1	UNUSED	0x0		

6.5.1.15 LS_BUS_TEST_RESULT Register

The LS_BUS_TEST_RESULT Register contains the results of the LS BUS Interface test. It includes bits that indicate if the failure is a checksum failure, bus packet failure, or LS bus parity failure. It also contains the checksum results of the test that can be compared to the desired checksum.

Table 6-24. LS_BUS_TEST_RESULT Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **LS_BUS_TEST_PASSFAIL_FLD** LS bus checksum test result '1' = checksum test passed '0' = checksum test failed	0x0	r	
1	Fieldname: **LS_BUS_IF_PKTERROR_FLD** LS bus packet error '1' = LS bus interface packet error (invalid packet received) '0' = no error	0x0	r	
2	Fieldname: **LS_BUS_IF_PARITY_ERROR_FLD** LS bus parity error '1' = LS bus interface parity error '0' = no error	0x0	r	
7:3	UNUSED	0x0		
31:8	Fieldname: **LS_BUS_TEST_CHECKSUM_FLD** LS bus 3-bytes checksum Passing checksum should be 0x3C7A55	0x0	r	

6.5.1.16 DMD_TYPE Register

The DMD_TYPE Register indicates whether or not the attached DMD is compatible with the DLPC964 Controller.

Table 6-25. DMD_TYPE Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **DMD_TYPE_FLD** '1': DLPC964 detected an un-supported DMD	0x0	r	
31:1	UNUSED	0x0		

6.5.1.17 HSS_RESET Register

The HSS_RESET Register contains the Aurora HSS_RESET bit. Writing a '1' to this register will reset the Aurora Receiver interface within the DLPC964 Controller.

Table 6-26. HSS_RESET Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **HSS_AURORA_RESET_FLD** 1: Reset HSS Aurora RX interface	0x0	w	
31:1	UNUSED	0x0		

6.5.1.18 HSS_CHANNEL_STATUS Register

The HSS_CHANNEL_STATUS Register indicates the status of the Aurora 64B/66B inputs to the DLPC964 controller.

Table 6-27. HSS_CHANNEL_STATUS Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **HSS_CH0_STATUS_FLD**	0x0	r	
	1: HSS Channel 0 up			
	0: Channel 0 Down			
1	Fieldname: **HSS_CH1_STATUS_FLD**	0x0	r	
	1: HSS Channel 1 up			
	0: Channel 1 Down			
2	Fieldname: **HSS_CH2_STATUS_FLD**	0x0	r	
	1: HSS Channel 2 up			
	0: Channel 2 Down			
3	Fieldname: **HSS_CH1_STATUS_FLD**	0x0	r	
	1: HSS Channel 3 up			
	0: Channel 3 Down			
4	Fieldname: **HSS_USERCLK_NOTLOCK_FLD**	0x0	r	
	1: user clock not lock			
	0: lock			
5	Fieldname: **HSS_GT0PLL_LOCK_FLD**	0x0	r	
	1: GT0 PLL lock. GT0 PLL is the source for the MMCM to generate user clock			
31:6	Fieldname: **Reserved**	0x0		

6.5.1.19 HSS_LANE_STATUS Register

The HSS_LANE_STATUS Register indicates the status of each individual lane of the Aurora 64B/66B input to the DLPC964 Controller.

Table 6-28.

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **HSS_CH0_LANE0_UP_FLD**	0x0	r	
	1: Channel 0 lane 0 up			
	0: Lane down			
1	Fieldname: **HSS_CH0_LANE1_UP_FLD**	0x0	r	
	1: Channel 0 lane 1 up			
	0: Lane down			
2	Fieldname: **HSS_CH0_LANE2_UP_FLD**	0x0	r	
	1: Channel 0 lane 2 up			
	0: Lane down			
3	Fieldname: **HSS_CH1_LANE0_UP_FLD**	0x0	r	
	1: Channel 1 lane 0 up			
	0: Lane down			

Table 6-28. (continued)

Bit(s)	Description	Reset	Type	Notes
4	Fieldname: **HSS_CH1_LANE1_UP_FLD** 1: Channel 1 lane 1 up 0: Lane down	0x0	r	
5	Fieldname: **HSS_CH1_LANE2_UP_FLD** 1: Channel 1 lane 2 up 0: Lane down	0x0	r	
6	Fieldname: **HSS_CH2_LANE0_UP_FLD** 1: Channel 2 lane 0 up 0: Lane down	0x0	r	
7	Fieldname: **HSS_CH2_LANE1_UP_FLD** 1: Channel 2 lane 1 up 0: Lane down	0x0	r	
8	Fieldname: **HSS_CH2_LANE2_UP_FLD** 1: Channel 2 lane 2 up 0: Lane down	0x0	r	
9	Fieldname: **HSS_CH3_LANE0_UP_FLD** 1: Channel 3 lane 0 up 0: Lane down	0x0	r	
10	Fieldname: **HSS_CH3_LANE1_UP_FLD** 1: Channel 3 lane 1 up 0: Lane down	0x0	r	
11	Fieldname: **HSS_CH3_LANE2_UP_FLD** 1: Channel 3 lane 2 up 0: Lane down	0x0	r	
31:12	UNUSED	0x0		

6.5.1.20 HSS_CH0_SOFTERROR_COUNT Register

The HSS_CH0_SOFTERROR_COUNT Register contains the Aurora 64B/66B Channel 0 total soft error count.

Table 6-29. HSS_CH0_SOFTERROR_COUNT Register

Bit(s)	Description	Reset	Type	Notes
19:0	Fieldname: **HSS_CH0_SOFTERROR_COUNT_FLD** Channel 0 soft error count	0x0	r	
31:20	UNUSED	0x0		

6.5.1.21 HSS_CH1_SOFTERROR_COUNT Register

The HSS_CH1_SOFTERROR_COUNT Register contains the Aurora 64B/66B Channel 1 total soft error count.

Table 6-30. HSS_CH1_SOFTERROR_COUNT Register

Bit(s)	Description	Reset	Type	Notes
19:0	Fieldname: **HSS_CH1_SOFTERROR_COUNT_FLD** Channel 1 soft error count	0x0	r	
31:20	UNUSED	0x0		

6.5.1.22 HSS_CH2_SOFTERROR_COUNT Register

The HSS_CH2_SOFTERROR_COUNT Register contains the Aurora 64B/66B Channel 2 total soft error count.

Table 6-31. HSS_CH2_SOFTERROR_COUNT Register

Bit(s)	Description	Reset	Type	Notes
19:0	Fieldname: **HSS_CH2_SOFTERROR_COUNT_FLD** Channel 2 soft error count	0x0	r	
31:20	UNUSED	0x0		

6.5.1.23 HSS_CH3_SOFTERROR_COUNT Register

The HSS_CH3_SOFTERROR_COUNT Register contains the Aurora 64B/66B Channel 3 total soft error count.

Table 6-32. HSS_CH3_SOFTERROR_COUNT Register

Bit(s)	Description	Reset	Type	Notes
19:0	Fieldname: **HSS_CH3_SOFTERROR_COUNT_FLD** Channel 3 soft error count	0x0	r	
31:20	UNUSED	0x0		

6.5.1.24 HSS_SOFTERROR_COUNT_RESET Register

The HSS_SOFTERROR_COUNT_RESET Register controls the reset of all the HSS_SOFTERROR_COUNT registers. Writing a '1' to this register resets all soft error counter values.

Table 6-33. HSS_SOFTERROR_COUNT_RESET Register

Bit(s)	Description	Reset	Type	Notes
0	Fieldname: **HSS_SOFTERROR_COUNT_RESET_FLD** Write ‘1’ to reset all soft error counters and trigger operation (the bit self-clears to ‘0’). A read of this bit always returns the value of ‘0’.	0x0	w	
31:0	UNUSED	0x0		

6.5.1.25 HSSI_Channel_0_DMD_Data_GT_Cell_Control Register

The HSI_CH0DMDDAT_GTCTRL Register contains the differential output voltage (Vod), pre-emphasis, and post-emphasis control settings for the DMD HSSI bus channel 0 data outputs of the DLPC964.

Table 6-34. HSI_CH0DMDDAT_GTCTRL Register

Bit(s)	Description	Reset	Type	Notes
3:0	Fieldname: **HSI_CH0DMDDAT_GTCTRL_TXDIFFCTRL_FLD** Channel 0 DMD data TX driver swing control. Default b1001 = 866mV	0x9	r/w	
7:4	UNUSED	0x0		

Table 6-34. HSI_CH0DMDDAT_GTCTRL Register (continued)

Bit(s)	Description	Reset	Type	Notes
12:8	Fieldname: **HSI_CH0DMDDAT_GTCTRL_TXPOST_FLD** Channel 0 DMD data TX post-cursor control. Default b0000 = 0dB	0x0	r/w	
15:13	UNUSED	0x0		
20:16	Fieldname: **HSI_CH0DMDDAT_GTCTRL_TXPRE_FLD** Channel 0 DMD data TX pre-cursor control. Default b0000 = 0dB	0x0	r/w	
31:21	UNUSED	0x0		

6.5.1.26 HSSI_Channel_0_DMD_Clock_GT_Cell_Control Register

The HSI_CH0DMDCLK_GTCTRL Register contains the differential output voltage (Vod), pre-emphasis, and post-emphasis control settings for the DMD HSSI bus channel 0 clock output of the DLPC964.

Table 6-35. HSI_CH0DMDCLK_GTCTRL Register

Bit(s)	Description	Reset	Type	Notes
3:0	Fieldname: **HSI_CH0DMDCLK_GTCTRL_TXDIFFCTRL_FLD** Channel 0 DMD clock TX driver swing control. Default b1001 = 866mV	0x9	r/w	
7:4	UNUSED	0x0		
12:8	Fieldname: **HSI_CH0DMDCLK_GTCTRL_TXPOST_FLD** Channel 0 DMD clock TX post-cursor control. Default b0000 = 0dB	0x0	r/w	
15:13	UNUSED	0x0		
20:16	Fieldname: **HSI_CH0DMDCLK_GTCTRL_TXPRE_FLD** Channel 0 DMD clock TX pre-cursor control. Default b0000 = 0dB	0x0	r/w	
31:21	UNUSED	0x0		

6.5.1.27 HSSI_Channel_1_DMD_Data_GT_Cell_Control Register

The HSI_CH1DMDDAT_GTCTRL Register contains the differential output voltage (Vod), pre-emphasis, and post-emphasis control settings for the DMD HSSI bus channel 1 data output of the DLPC964.

Table 6-36. HSI_CH1DMDDAT_GTCTRL Register

Bit(s)	Description	Reset	Type	Notes
3:0	Fieldname: **HSI_CH1DMDDAT_GTCTRL_TXDIFFCTRL_FLD** Channel 1 DMD data TX driver swing control. Default b1001 = 866mV	0x9	r/w	
7:4	UNUSED	0x0		
12:8	Fieldname: **HSI_CH1DMDDAT_GTCTRL_TXPOST_FLD** Channel 1 DMD data TX post-cursor control. Default b0000 = 0dB	0x0	r/w	
15:13	UNUSED	0x0		
20:16	Fieldname: **HSI_CH1DMDDAT_GTCTRL_TXPRE_FLD** Channel 1 DMD data TX pre-cursor control. Default b0000 = 0dB	0x0	r/w	
31:21	UNUSED	0x0		

6.5.1.28 HSSI_Channel_1_DMD_Clock_GT_Cell_Control Register

The HSI_CH1DMDCLK_GTCTRL Register contains the differential output voltage (Vod), pre-emphasis, and post-emphasis control settings for the DMD HSSI bus channel 1 clock output of the DLPC964.

Table 6-37. HSI_CH1DMDCLK_GTCTRL Register

Bit(s)	Description	Reset	Type	Notes
3:0	Fieldname: **HSI_CH1DMDCLK_GTCTRL_TXDIFFCTRL_FLD** Channel 1 DMD clock TX driver swing control. Default b1001 = 866mV	0x9	r/w	
7:4	UNUSED	0x0		
12:8	Fieldname: **HSI_CH1DMDCLK_GTCTRL_TXPOST_FLD** Channel 1 DMD clock TX post-cursor control. Default b0000 = 0dB	0x0	r/w	
15:13	UNUSED	0x0		
20:16	Fieldname: **HSI_CH1DMDCLK_GTCTRL_TXPRE_FLD** Channel 1 DMD clock TX pre-cursor control. Default b0000 = 0dB	0x0	r/w	
31:21	UNUSED	0x0		

6.5.1.29 HSSI_Channel_2_DMD_Data_GT_Cell_Control Register

The HSI_CH2DMDDAT_GTCTRL Register contains the differential output voltage (Vod), pre-emphasis, and post-emphasis control settings for the DMD HSSI bus channel 2 data output of the DLPC964.

Table 6-38. HSI_CH2DMDDAT_GTCTRL Register

Bit(s)	Description	Reset	Type	Notes
3:0	Fieldname: **HSI_CH2DMDDAT_GTCTRL_TXDIFFCTRL_FLD** Channel 2 DMD data TX driver swing control. Default b1001 = 866mV	0x9	r/w	
7:4	UNUSED	0x0		
12:8	Fieldname: **HSI_CH2DMDDAT_GTCTRL_TXPOST_FLD** Channel 2 DMD data TX post-cursor control. Default b0000 = 0dB	0x0	r/w	
15:13	UNUSED	0x0		
20:16	Fieldname: **HSI_CH2DMDDAT_GTCTRL_TXPRE_FLD** Channel 2 DMD data TX pre-cursor control. Default b0000 = 0dB	0x0	r/w	
31:21	UNUSED	0x0		

6.5.1.30 HSSI_Channel_2_DMD_Clock_GT_Cell_Control Register

The HSI_CH2DMDCLK_GTCTRL Register contains the differential output voltage (Vod), pre-emphasis, and post-emphasis control settings for the DMD HSSI bus channel 2 clock output of the DLPC964.

Table 6-39. HSI_CH2DMDCLK_GTCTRL Register

Bit(s)	Description	Reset	Type	Notes
3:0	Fieldname: **HSI_CH2DMDCLK_GTCTRL_TXDIFFCTRL_FLD** Channel 2 DMD clock TX driver swing control. Default b1001 = 866mV	0x9	r/w	
7:4	UNUSED	0x0		
12:8	Fieldname: **HSI_CH2DMDCLK_GTCTRL_TXPOST_FLD** Channel 2 DMD clock TX post-cursor control. Default b0000 = 0dB	0x0	r/w	
15:13	UNUSED	0x0		

Table 6-39. HSI_CH2DMDCLK_GTCTRL Register (continued)

Bit(s)	Description	Reset	Type	Notes
20:16	Fieldname: **HSI_CH2DMDCLK_GTCTRL_TXPRE_FLD** Channel 2 DMD clock TX pre-cursor control. Default b0000 = 0dB	0x0	r/w	
31:21	UNUSED	0x0		

6.5.1.31 HSSI_Channel_3_DMD_Data_GT_Cell_Control Register

The HSI_CH3DMDDAT_GTCTRL Register contains the differential output voltage (Vod), pre-emphasis, and post-emphasis control settings for the DMD HSSI bus channel 3 data output of the DLPC964.

Table 6-40. HSI_CH3DMDDAT_GTCTRL Register

Bit(s)	Description	Reset	Type	Notes
3:0	Fieldname: **HSI_CH3DMDDAT_GTCTRL_TXDIFFCTRL_FLD** Channel 3 DMD data TX driver swing control. Default b1001 = 866mV	0x9	r/w	
7:4	UNUSED	0x0		
12:8	Fieldname: **HSI_CH3DMDDAT_GTCTRL_TXPOST_FLD** Channel 3 DMD data TX post-cursor control. Default b0000 = 0dB	0x0	r/w	
15:13	UNUSED	0x0		
20:16	Fieldname: **HSI_CH3DMDDAT_GTCTRL_TXPRE_FLD** Channel 3 DMD data TX pre-cursor control. Default b0000 = 0dB	0x0	r/w	
31:21	UNUSED	0x0		

6.5.1.32 HSSI_Channel_3_DMD_Clock_GT_Cell_Control Register

The HSI_CH3DMDCLK_GTCTRL Register contains the differential output voltage (Vod), pre-emphasis, and post-emphasis control settings for the DMD HSSI bus channel 3 clock output of the DLPC964.

Table 6-41. HSI_CH3DMDCLK_GTCTRL Register

Bit(s)	Description	Reset	Type	Notes
3:0	Fieldname: **HSI_CH3DMDCLK_GTCTRL_TXDIFFCTRL_FLD** Channel 3 DMD clock TX driver swing control. Default b1001 = 866mV	0x9	r/w	
7:4	UNUSED	0x0		
12:8	Fieldname: **HSI_CH3DMDCLK_GTCTRL_TXPOST_FLD** Channel 3 DMD clock TX post-cursor control. Default b0000 = 0dB	0x0	r/w	
15:13	UNUSED	0x0		
20:16	Fieldname: **HSI_CH3DMDCLK_GTCTRL_TXPRE_FLD** Channel 3 DMD clock TX pre-cursor control. Default b0000 = 0dB	0x0	r/w	
31:21	UNUSED	0x0		

6.5.1.33 HSSI_DMD_Vcm_Value Register

The HSI_VCM_VAL Register contains the common-mode voltage (Vcm) settings for the DMD HSSI receiver in the DLP991U DMD.

Table 6-42. HSI_VCM_VAL Register

Bit(s)	Description	Reset	Type	Notes
2:0	Fieldname: **HSI_VCM_VALUE_FLD** Common-mode voltage value for programming the DMD HSSI receiver in the DLP991U DMD. Default b001 = 0.673V - 0.758V	0x1	r/w	
31:3	UNUSED	0x0		

6.5.1.34 TEST_DMD_ID Register

The TEST_DMD_ID Register contains the ID of the DMD attached to the DLPC964 Controller.

Table 6-43. TEST_DMD_ID Register

Bit(s)	Description	Reset	Type	Notes
31:0	Fieldname: **TEST_DMD_ID_FLD** DMD ID	0x0	r	

6.5.1.35 TEST_DMD_FUSE1 Register

The TEST_DMD_FUSE1 Register contains the fuse settings for DMD fuse group 1.

Table 6-44. TEST_DMD_FUSE1 Register

Bit(s)	Description	Reset	Type	Notes
31:0	Fieldname: **TEST_DMD_FUSE1_FLD** DMD fuse group 1	0x0	r	

6.5.1.36 TEST_DMD_FUSE2 Register

The TEST_DMD_FUSE2 Register contains the fuse settings for DMD fuse group 2.

Table 6-45. TEST_DMD_FUSE2 Register

Bit(s)	Description	Reset	Type	Notes
31:0	Fieldname: **TEST_DMD_FUSE2_FLD** DMD fuse group 2	0x0	r	

6.5.1.37 TEST_DMD_FUSE3 Register

The TEST_DMD_FUSE3 Register contains the fuse settings for DMD fuse group 3.

Table 6-46. TEST_DMD_FUSE3 Register

Bit(s)	Description	Reset	Type	Notes
31:0	Fieldname: **TEST_DMD_FUSE3_FLD** DMD fuse group 3	0x0	r	

6.5.1.38 TEST_DMD_FUSE4 Register

The TEST_DMD_FUSE4 Register contains the fuse settings for DMD fuse group 4.

Table 6-47. TEST_DMD_FUSE4 Register

Bit(s)	Description	Reset	Type	Notes
31:0	Fieldname: **TEST_DMD_FUSE4_FLD** DMD fuse group 4	0x0	r	

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The DLPC964 controller verifies the DMD is connected in the application system, uses that information to select appropriate configuration data for the DMD, and then initializes the DMD to ready it for operation.

The DLPC964 controller receives streaming input data from an external applications processor and passes the data on to the DMD with the appropriate DMD timing and control information. It also receives embedded instructions from the applications processor to assist in determination of which DMD rows to load and which DMD mirror blocks to activate at any given moment in time.

7.2 Typical Application

Direct-write digital imaging is regularly used in PCB manufacturing. This mask-less technology offers continuous run of printing by changing the digitally created patterns without stopping the imaging head. The DLPC964 reliably operates with the DLP991U DMD. These chipset combinations provide an ideal back-end imager that takes in digital images at [4096 × 2176] resolution to achieve speeds greater than 110 gigabits per second (Gbps).

7.2.1 High Speed Direct Imaging Application

As high-end direct imaging pushes the high speed printing envelope, providing a higher resolution imager is a must to achieve the demanding throughput of preset and future printing technology. Figure 7-1 shows a system that offers both a speed boost and a 8.9 million pixel DMD. The main chipset components that make up this system are the DLPC964 controller and the DLP991U DMD. With a few additional discrete components for power regulation and clock circuitry, a compact, high-performance design can be achieved.

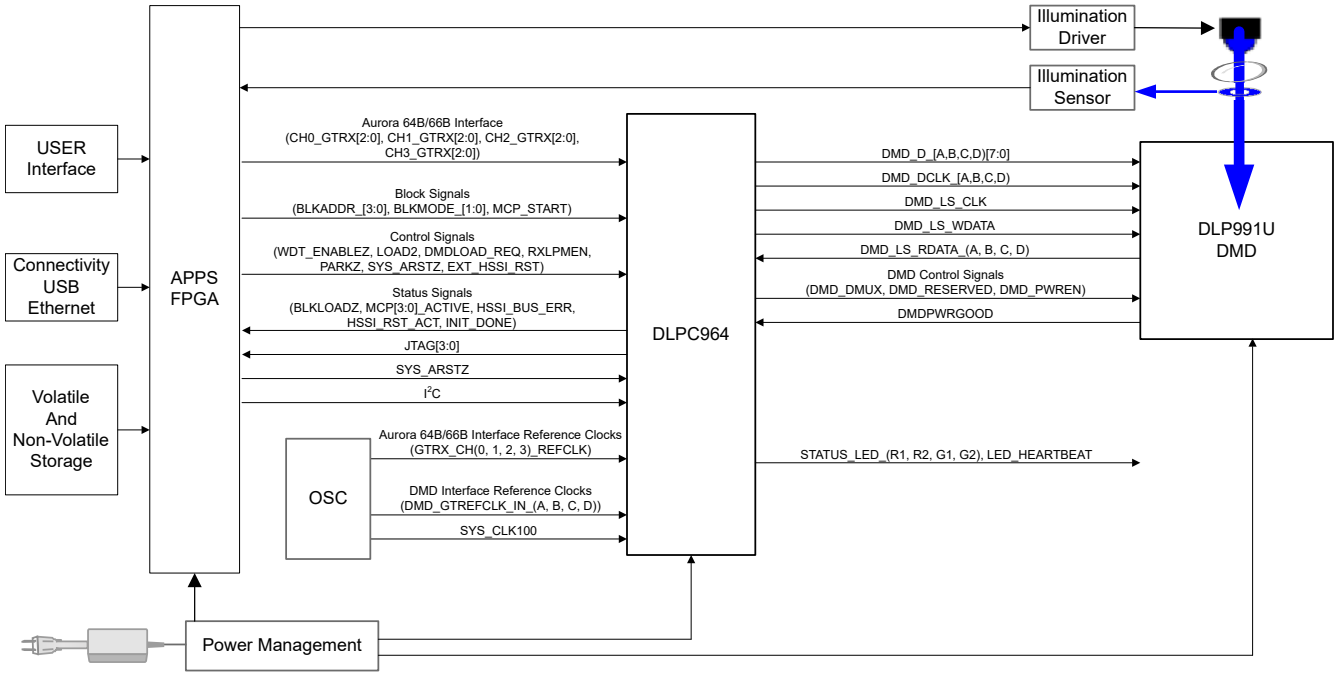


Figure 7-1. Typical DLP991U High Speed Application

7.2.2 Design Requirements

The DLPC964 interface is made up of several buses and controls signals as shown in the following list. The Aurora 64B/66B high speed serial (HSS) input buses provide the means of loading data to the DLPC964. The high speed serial interface (HSSI) output buses provide the data to the DMD. Each input and output bus has an associated clock which clocks the data into the DLPC964 or into the DMD. Block control signals define the type of mirror clock pulse to use after all the data is loaded into the DMD.

- High Speed Serial (HSS) differential inputs
  - GTRX_CHn_REFCLK - 4 buses
  - CHn_GTRX - 12 buses
- High Speed Serial Interface (HSSI) differential outputs
  - DMD_DCLK_n - 4 buses
  - DMD_D_n - 4 buses
  - DMD_LS_CLK - 1 bus
  - DMD_WDATA - 1 bus
  - DMD_RDATA_n - 4 buses
- Control output signals
  - DMD_DMUX
  - DMD_RESERVED
  - DMD_PWREN
  - HSSI_ERR_LATCH_RST
- Block control input signals
  - BLKADDR[3:0]
  - BLKMODE[1:0]
  - DMDLOAD_REQ
  - MCP_START
- Control input signals
  - LOAD2
  - WDT_ENABLEZ
  - PARKZ
  - RXLPMEN
  - EXT_HSSI_RST
- Status output signals
  - HSSI_BUS_ERR
  - HSSI_RST_ACT
  - IRQZ
  - INIT_DONE
  - LED_HEARTBEAT
  - STATUS_LED
- Controller reset
  - SYS_ARSTZ
- Configuration FLASH interface
  - PGM[4:0]
  - JTAG[3:0]

7.2.3 Detailed Design Procedure

After power is applied to the DLPC964, the APPS FPGA monitors the DONE_0 signal to determine when the DLPC964 completed configuration. The APPS FPGA next monitors the INIT_DONE signal to determine when the DLPC964 completed its internal initialization routines and configured the DMD for normal operation. An alternate method is to request the initialization status using the I^2C interface. Information regarding initialization, versions, and IDs can be requested through this interface.

To define the start of a DMD block, the APPS FPGA must send a Block Control Word packet through the HSS Channel 0 input to the DLPC964. Control word packets sent over Aurora 64B/66B Channels 1, 2, and 3 are not used and are ignored by the DLPC964 controller. After the Block Control Word is sent to the DLPC964 controller, the APPS FPGA can begin loading data across all four Aurora 64B/66B Channels to the DLPC964 controller. Once the data transfer is complete on all four Aurora 64B/66B Channels, the APPS FPGA must assert DMDLOAD_REQ to signal the DLPC964 controller the end of a DMD block, and trigger it to carry out the operation encoded in the Block Control Word. While the DLPC964 controller is carrying out the operation encoded in the Block Control Word, it asserts the BLKLOADZ signal. Once the BLKLOADZ signal is deasserted, the APPS FPGA is free to send the next Block Control Word packet to the DLPC964 controller.

During the Block Control Word packet and subsequent data loading across all four Aurora 64B/66B Channels, the APPS FPGA should set up the BLKADDR and BLKMODE signals for the desired MCP operation. Once the DLPC964 deasserts the BLKLOADZ signal, and data loading operations are complete for the desired DMD block, MCP_START can be asserted to begin the desired MCP operation and display the loaded data on the DMD mirrors. While a MCP_START operation is in progress, the DLPC964 asserts MCP_ACTIVE to signal to the APPS FPGA that a MCP mirror operation is currently in progress.

7.2.4 DMD Mirror Switching Performance Plots

In these particular applications, the performance plot shown in Figure 7-2 shows the maximum loaded and displayed pixels per second when the valid data pattern time is at the maximum time to still operate at the fastest pattern rate of each MCP mode for the different MCP modes. When the exposure period is increased, the pixels per second decreases.

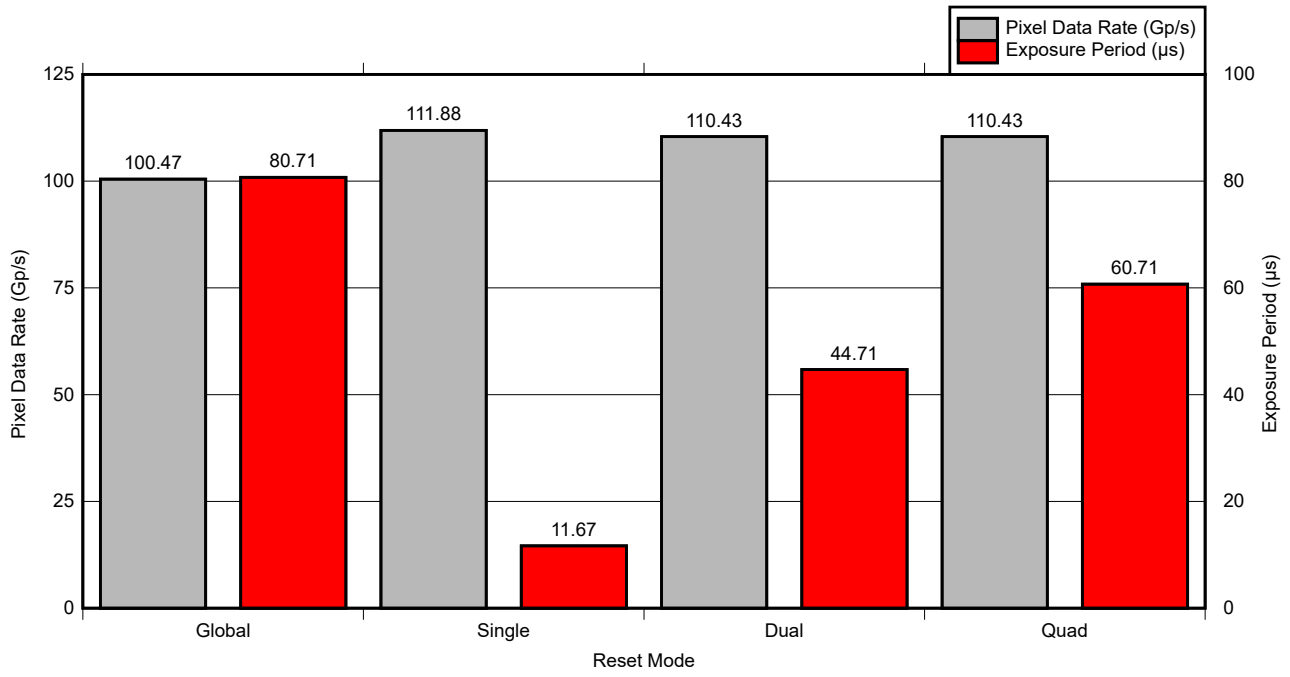


Figure 7-2. DLP991U DMD Performance Plot at 3.6Gbps Data Rate

The following equations describe how to calculate the maximum loaded and displayed pixels per second when the exposure period is set to its minimum for the different reset modes:

Global Block Exposure Period = Number of DMD Blocks Loaded × DMD Block Load Time

Cycle Period = Exposure Period + ((16 ÷ # Blocks Reset) × MCP Active Period) + Mirror Settling Time

Pattern Rate = 1 ÷ Cycle Period

Pixel Data Rate = Pattern Rate × 4096 × 2176

For Global Reset Mode, the calculations are:

Global Block Exposure Period = 16 × 5.04444µs = 80.711µs

Cycle Period = 80.711µs + 4µs + 4µs = 88.711µs

Pattern Rate = 1 ÷ 88.711µs = 11.272kHz

Pixel Data Rate = 11.272kHz × 4096 × 2176 = 100.47Gbps

For Single Block Reset Mode, the calculations are:

Single Block Exposure Period = 11.67µs

Cycle Period = 11.67µs + 64µs + 4µs = 79.67µs

Pattern Rate = 1 ÷ 79.67µs = 12.551kHz

Pixel Data Rate = 12.551kHz × 4096 × 2176 = 111.88Gbps

For Dual Block Reset Mode, the calculations are:

Dual Block Exposure Period = 44.71µs

Cycle Period = 44.71µs + 32µs + 4µs = 80.71µs

Pattern Rate = 1 ÷ 80.71µs = 12.390kHz

Pixel Data Rate = 12.390kHz × 4096 × 2176 = 110.43Gbps

For loading a single DMD row and resetting, the equations and calculations are:

DMD Row Load Time = DMD Block Load Time ÷ Number of Rows in a DMD Block

DMD Row Load Time = 5.04444µs ÷ 136 = 0.03709µs

Exposure Period = 0.03709µs

Cycle Period = 0.03709µs + 4µs + 4µs = 8.03709µs

Pattern Rate = 1 ÷ 8.03709µs = 124.423kHz

Pixel Data Rate = 124.423kHz × 4096 = 509.64Mbps

7.3 Interfacing to DLPC964 Controller High Speed Serial (HSS) Aurora 64B/66B Inputs

Data transfer between the APPS FPGA and the DLPC964 Controller is carried out with twelve High Speed Serial (HSS) Aurora 64B/66B data links, each operating at 10Gbps. The link-layer protocol utilized for these twelve HSS links is the Aurora 64B/66B LogiCORE IP available from AMD.

Figure 7-3 describes the overall data flow of the twelve HSS Aurora 64B/66B data links from the APPS FPGA to the DLPC964 Controller, and then from the DLPC964 Controller to the appropriate array segment of the DLP991U DMD.

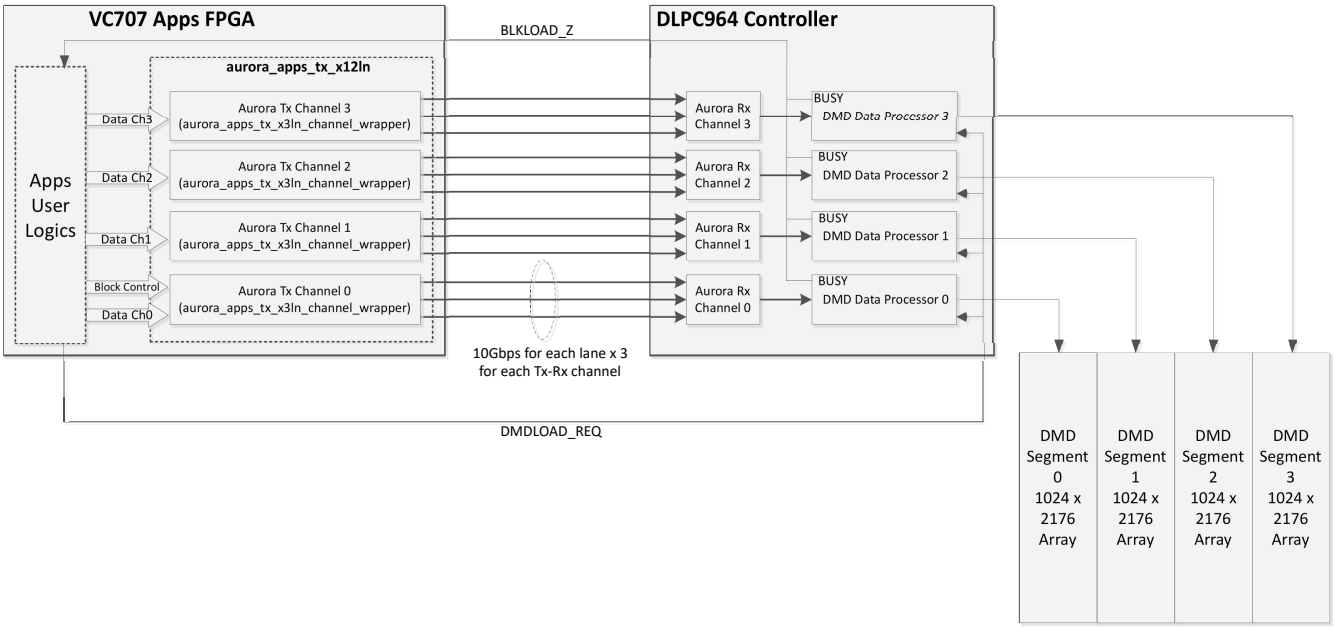


Figure 7-3. DLPC964 System Block Diagram

7.3.1 Theory of Operation

As shown in Figure 7-3, the data input to the DLPC964 controller through the AMD Aurora 64B/66B High Speed Serial (HSS) interface is arranged according to DMD array blocks. The DLP991U DMD has a total of sixteen DMD blocks, with each DMD block made up of an array of 4096 columns and 136 rows. A single row of 4096 DMD columns is then further divided into four segments of 1024 columns and independently mapped to the four HSS serial data input channels on the DLPC964. Each of the four independent HSS Aurora 64B/66B input channel cores (Channel 0, Channel 1, Channel 2, and Channel 3) control loading of 1024 columns and 136 rows, resulting in parallel loading of the full DMD block array of 4096 columns by 136 rows.

7.3.1.1 Block Start with Block Control Word

The AMD Aurora 64B/66B high speed serial (HSS) interface is a generic data transport link without any concept of how the DMD block data structure must be arranged. To define the start of a DMD block, the APPS FPGA logic must send a block control word data packet through channel 0 of the Aurora 64B/66B User-K data port before DMD data transmission can begin.

Table 7-1 below contains detailed information regarding the Aurora User-K interface port. The User-K interface ports are used to implement application-specific control functions, are independent, and are higher priority than the data interface.

Table 7-1. User-K Interface Ports

Name	Direction	Clock Domain	Description
USER_S_S_AXIS_TX			
s_axi_user_k_tx_tdata[0:(64n-1)] or s_axi_user_k_tx_tdata[(64n-1):0] (1)	Input	user_clk	USER-K block data is 64-bit aligned. Signal Mapping per lane:
			Default:
			s_axi_user_k_tx_tdata={{4'h0,user_k_blk_no[0:3],user_k_data[55:0]}*n}
			Little endian format:
			s_axi_user_k_tx_tdata={{user_k_data[55:0],4'h0,user_k_blk_no[3:0]}*n}
s_axi_user_k_tx_tvalid	Input	user_clk	Indicates valid User-K data on the s_axi_userk_tx_tdata port.
s_axi_user_k_tx_tready	Output	user_clk	Indicates the Aurora 64B/66B core is ready to accept data on the s_axi_user_k_tx_tdata interface.
USER_K_M_AXIS_RX			
m_axi_rx_user_k_tvalid	Output	user_clk	Indicates valid User-K data on the m_axi_user_k_tx_tdata port.
m_axi_rx_user_k_tdata or m_axi_rx_user_k_tdata[(64n-1):0] (1)	Output	user_clk	Received USER-K blocks from the Aurora 64B/66B lane are 64-bit aligned.
			Signal Mapping per lane:
			Default:
			m_axi_rx_user_k_tdata={{4'h0,user_k_blk_no[0:3],user_k_data[55:0]}*n}
			Little endian format:
			m_axi_rx_user_k_tdata={{user_k_data[55:0],4'h0,user_k_blk_no[3:0]}*n}

(1) n is the number of lanes.

As shown in Table 7-2 below, the HSS interface to the DLPC964 has four channels of User-K port interface exposed to the APPS FPGA user logics. Only Channel 0 is used to transmit the Block Control Word. Any Control Word packets sent over the User-K port of Channel 1, 2, and 3 are not used and are ignored by the DLPC964 Controller.

Table 7-2. Aurora 64B/66B High Speed Serial User-K Ports Usage

Signal Name	Signal Direction	DLPC964 Application Usage
gt0_s_axi_user_k_tx_tdata[191:0]	Input to Aurora Channel 0	192-bit block control word packet to be transmitted
gt0_s_axi_user_k_tx_tvalid	Input to Aurora Channel 0	User logic asserts this signal high to indicate to Aurora core the Block Control word is valid to transmit. Aurora cores ignore word if TVALID is not-asserted.
gt0_s_axi_user_k_tx_tready	Output to Aurora Channel 0	Aurora cores assert this signal high when the Block Control word is accepted. This signal is deasserted when words are ignored; that is, cores are not ready to accept input word.
gt1_s_axi_user_k_tx_tdata[191:0]	Input to Aurora Channel 1	Unused
gt1_s_axi_user_k_tx_tvalid	Input to Aurora Channel 1	Unused
gt1_s_axi_user_k_tx_tready	Output to Aurora Channel 1	Unused
gt2_s_axi_user_k_tx_tdata[191:0]	Input to Aurora Channel 2	Unused
gt2_s_axi_user_k_tx_tvalid	Input to Aurora Channel 2	Unused
gt2_s_axi_user_k_tx_tready	Output to Aurora Channel 2	Unused
gt3_s_axi_user_k_tx_tdata[191:0]	Input to Aurora Channel 3	Unused
gt3_s_axi_user_k_tx_tvalid	Input to Aurora Channel 3	Unused
gt3_s_axi_user_k_tx_tready	Output to Aurora Channel 3	Unused

Table 7-3 describes the various fields within the 192-bit block control word. The block control word not only defines the start of a DMD block, but also contains instructions and information to guide the DLPC964 Controller in processing the received DMD Block Data from the APPS FPGA.

Table 7-3. Block Control Word Fields Definition

Field Position	Field Type	Field Description
gt0_s_axi_user_k_tx_tdata[7:0]	USER_K_BLOCK_NUMBER	Must set to zeros (0x00). Values other than 0x00 are invalid. DLPC964 controller ignores the entire 192-bit control word if this field is not set to 0x00.
gt0_s_axi_user_k_tx_tdata[11:8]	BLOCK_ADDRESS	Indicates the address of the DMD block to which the DLPC964 applies the operation: 0000: DMD Block 0, 0001: DMD Block 1, 0010: DMD Block 2, …1110: DMD Block 14, 1111: DMD Block 15
gt0_s_axi_user_k_tx_tdata[15:7]		Reserved, Unused
gt0_s_axi_user_k_tx_tdata[24:16]	ROW_LENGTH	Number of DMD row to be loaded by DLPC964. DLP991U DMD has 136 rows per block, thus valid range is 1-136. All other values, including 0 are invalid. Set to 136 for full block operation. Set to 1–135 for partial block operation.
		NOTE: This field is only used if LOAD_TYPE = 000.

Table 7-3. Block Control Word Fields Definition (continued)

Field Position	Field Type	Field Description
gt0_s_axi_user_k_tx_tdata[34:32]	LOAD_TYPE	000: Block Loading. The DLPC964 loads the user data to the DMD array defined by BLOCK_ADDRESS and ROW_LENGTH.
		001: Block Clear. The DLPC964 clears the DMD array to zeroes of the entire block defined by BLOCK_ADDRESS.
		010: Block Set. The DLPC964 sets the DMD array to ones of the entire block defined by BLOCK_ADDRESS.
		Other values: reserved, do not use.
		NOTE: when in 001 (Block Clear) or 010 (Block Set) operation, the ROW_LENGTH and NORTH_SOUTH_FLIP fields are ignored. Clear and Set operations affect the entire DMD Block array. Partial Block operation for Clear and Set operations is not supported.
gt0_s_axi_user_k_tx_tdata[36]	NORTH_SOUTH_FLIP	Control the direction of data loading within a DMD Block.
		0: DLPC964 loads data starting and counting up from row 1.
		1: DLPC964 loads data starting and counting down from row 136
		NOTE: This field is only used if LOAD_TYPE is 000.
gt0_s_axi_user_k_tx_tdata[29:28]	DMD_SEGMENT	When SINGLE_CHANNEL_MODE = '1', DMD_SEGMENT is used to select which DMD segment is selected for the operation.
		00: Segment 0
		01: Segment 1
		10: Segment 2
		11: Segment 3
		NOTE: This field is ignored if SINGLE_CHANNEL_MODE = '0'.
gt0_s_axi_user_k_tx_tdata[30]	SINGLE_CHANNEL_MODE	1: Single Channel operation. DLPC964 Input Data for DMD is only received on Aurora Channel 0.
		0: Normal operation. DLPC964 Input Data for DMD is received on all four Aurora Channels.
gt0_s_axi_user_k_tx_tdata[191:31]		Reserved, unused

Figure 7-4 displays the transmission of the 192-bit block control word over the channel 0 User-K port at the start of an Aurora 64B/66B data block transfer. In this example, 136 rows of DMD block 1 are being loaded.

1. With the proper Block Control word on bus gt0_s_axi_user_k_tx_tdata[191:0], the APPS FPGA user logics asserts the TVALID flag, gt0_s_axi_user_k_tx_tvalid, and waits for the Aurora core's response.
2. The Aurora core asserts the TREADY flag and gt0_s_axi_user_k_tx_tready, indicating the core has accepted the 192 bits User-K data.
3. After the block control word is sent, the APPS FPGA user logics start the Aurora data block transfer on all four HSS data interfaces.

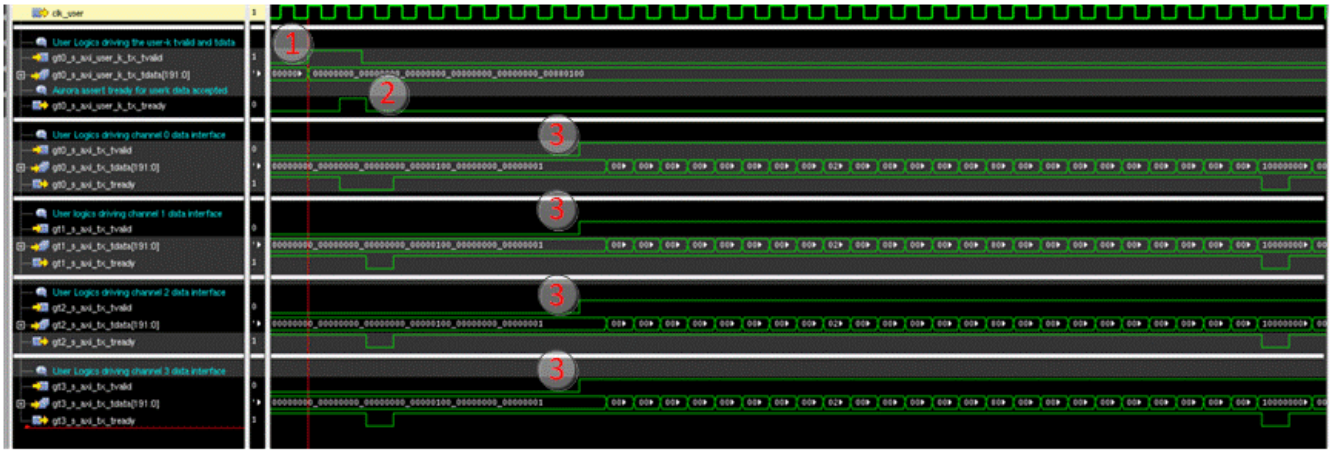


Figure 7-4. Block Start with Block Control Word Waveform

7.3.1.2 Block Complete with DMDLOAD_REQ

Refer to Figure 7-3, DMDLOAD_REQ is an output signal from the APPS FPGA to the DLPC964 Controller.

Once the Aurora Block Data transfer is complete, the APPS FPGA user logics must assert DMDLOAD_REQ to signal the end of a DMD block to the DLPC964 Controller and trigger the DLPC964 Controller to carry out the operation encoded in the Block Control Word.

Guidelines for asserting the DMDLOAD_REQ signal and sending the Block Control Word:

- APPS FPGA user logics must wait for the block data transfer to complete on all four Aurora data channels before asserting DMDLOAD_REQ. Asserting DMDLOAD_REQ before completion of the Aurora block data transfer can result in data not being properly loaded to the DMD. The APPS FPGA must take into account that the four Aurora data channel interfaces may not be fully synchronous to one another, thus data completion may not happen at the exact same clock cycle. Therefore, the APPS FPGA must monitor and ensure the Aurora block data transfer is completed on all four channels before asserting DMDLOAD_REQ.
- DMDLOAD_REQ may be asserted immediately after completing an Aurora block transfer as long as the 300ns DMDLOAD_REQ setup time is met (refer to Section 7.3.1.3 for more details).
- Apps user logics must assert DMDLOAD_REQ for the current block before initiating the transmission of the next new DMD block data. In other words, every block must start with a Block Control Word packet and end with DMDLOAD_REQ assertion.
- DMDLOAD_REQ is still required for operations that do not involve block data transfer (such as block-clear or block-set operation), and must still meet the required 300ns setup time (refer to Section 7.3.1.3 for more details).
- Refer to Figure 7-5. In most cases, after the APPS FPGA user logic has completed the transfer of the current data block, it may find that the DLPC964 Controller is still loading the previous block to the DMD (i.e. BLKLOADZ is low). If this occurs, the APPS FPGA can still assert DMDLOAD_REQ while BLKLOADZ is low. The DLPC964 Controller will detect and store the DMDLOAD_REQ request and perform the data load as soon as the transfer of the previous data block is complete.
- The DLPC964 Controller has two data-block buffers - one for receiving the incoming Aurora data block from the APPS FPGA, and the other for holding the previous data block for streaming out to the DMD. Care must

be taken by the APPS FPGA to avoid overrunning these two buffers. Refer to Figure 7-5. After completing the current Aurora data transfer of block data and asserting the DMDLOAD_REQ signal, the APPS FPGA must wait for the de-assertion of BLKLOADZ by the DLPC964 Controller (i.e. BLKLOADZ transition from low to high) before starting the next block data transfer. De-assertion of BLKLOADZ indicates that the DLPC964 Controller has completed the DMD data loading operation for previous block, and a data buffer is freed up for accepting a new data block from the Aurora interface. The buffer will be overrun and data will be incorrectly loaded to the DMD if the APPS FPGA does not synchronize the Aurora block data transfer with BLKLOADZ signal de-assertion.

- It is not necessary for the APPS FPGA to immediately assert DMDLOAD_REQ after sending a DMD data block. The APPS FPGA may send the DLPC964 Controller a DMD data block and then delay the assertion of DMDLOAD_REQ until the system is ready for the DMD be loaded. Figure 7-6 describes this operation.

Figure 7-5. End of Block DMDLOAD_REQ Assertion Followed by New Block Control Word Waveform

1. APPS FPGA user logic asserts DMDLOAD_REQ immediately after the completion of current block data transmission on all four Aurora data interfaces.
2. DLPC964 Controller de-asserts BLKLOADZ, indicating completion of the data loading operation for the previous DMD block.
3. APPS FPGA user logics detects the de-assertion of BLKLOADZ and sends a new Block Control Word on Aurora Channel 0 User-K Port for the next block data.
4. APPS FPGA user logics sending data for next block.
5. BLKLOADZ is asserted low by the DLPC964 Controller, indicating the data loading operation for current block triggered by DMDLOAD_REQ occurred at 1.

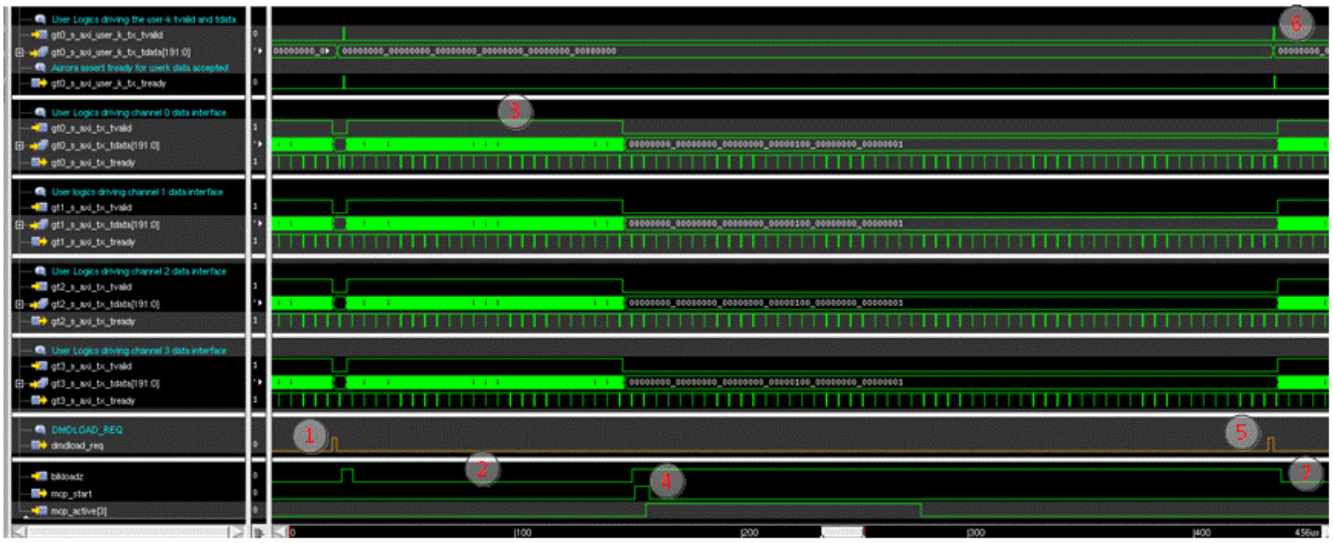


Figure 7-6. DMDLOAD_REQ Delayed Assertion Waveform

1. APPS FPGA finishes sending the last block data (block 15) of the current pattern and asserts DMDLOAD_REQ to instruct the DLPC964 Controller to carry out the data load operation.
2. DLPC964 Controller loads data to block 15, triggered by DMDLOAD_REQ from 1.
3. APPS FPGA sends the first block (block 0) of data for the next pattern over the Aurora data interfaces while the DLPC964 Controller is loading block 15 of the current pattern.
4. DLPC964 de-asserts BLKLOADZ after completing the data load for block 15 of the current pattern. APPS FPGA detects the BLKLOADZ de-assertion (because the last block data of the current pattern has been loaded on to DMD) and issues an MCP_START signal for global block MCP operation. Notice that the DLPC964 Controller asserted the MCP0_ACTIVE signal to communicate that the MCP mirror operation in process.
5. APPS FPGA delays the assertion of DMDLOAD_REQ for block 0 of next pattern due to the requirement of meeting the mirror settling time.
6. APPS FPGA sends the Block Control Word for block 1 of the next pattern after the assertion of DMDLOAD_REQ for block 0.
7. DLPC964 Controller asserts BLKLOADZ to indicate that the DMD data loading operation was triggered by DMDLOAD_REQ from 5.

7.3.1.3 DMDLOAD_REQ Setup Time Requirement

The APPS FPGA user logic can assert the DMDLOAD_REQ signal as soon as the Aurora block data transfer is complete, as long as it is at least 300ns after sending the first data packet of that block data transfer. This setup time requirement is due to the 300ns transmit latency of the Aurora TX/RX channel paths, and guarantees the DLPC964 Controller will receive the DMDLOAD_REQ flag after the arrival of Aurora block data transfer.

In most cases, this 300ns setup requirement is naturally met due to the size of a data block transfer. It is large enough to guarantee well over 300ns from the first valid data packet being sent to the last ones of a block when the APPS FPGA can assert the DMDLOAD_REQ signal. The 300ns setup window becomes critical when the APPS FPGA attempts to send a small partial DMD data block such as in Figure 7-7, showing an example of the APPS FPGA sending a total of just 3 rows (Table 7-3, ROW_LENGTH = 3) of a DMD partial data block to the DLPC964 Controller:

1. APPS FPGA transmits a Block Control Word to indicate the start of an Aurora block data transfer.
2. After sending 3 rows of data through the four Aurora data interface channels, the APPS FPGA waits for the 300ns setup time to expire before issuing a DMDLOAD_REQ. Note, 300ns is measured from the start of the first TVALID on the data interface.
3. Once the setup time has been met, the APPS FPGA asserts DMDLOAD_REQ.
4. BLKLOADZ is asserted by the DLPC964 Controller, indicating a DMD data load operation is in progress.

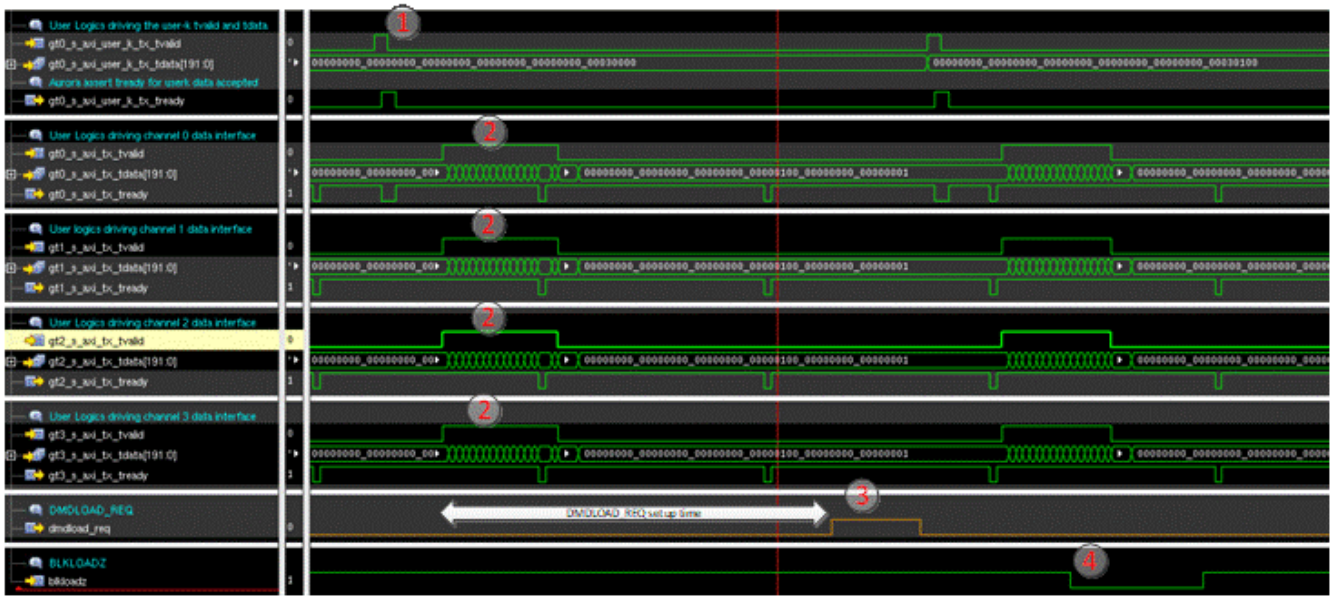


Figure 7-7. Example of DMDLOAD_REQ Setup Time for Three DMD Row Load Operation

For operations that do not require a data packet, such as block-clear (Table 7-3, LOAD_TYPE = 001) and block-set (Table 7-3, LOAD_TYPE = 010), the 300ns setup time for DMDLOAD_REQ is still required and is measured from the Block Control Word packet. An example of block-set operation is described in Figure 7-8:

1. APPS FPGA transmits a Block Control Word packet to start a block-set operation. Notice that this operation does not require any block data, and the four Aurora data interfaces stay idle (gtX_s_axi_tx_tvalid = '0').
2. APPS FPGA asserts a DMDLOAD_REQ after the 300ns setup time. 300ns is measured from the Block Control Word, because the block-set operation does not require any Aurora data block transfer.
3. DLPC964 Controller asserts BLKLOADZ, indicating block-set operation is in progress.

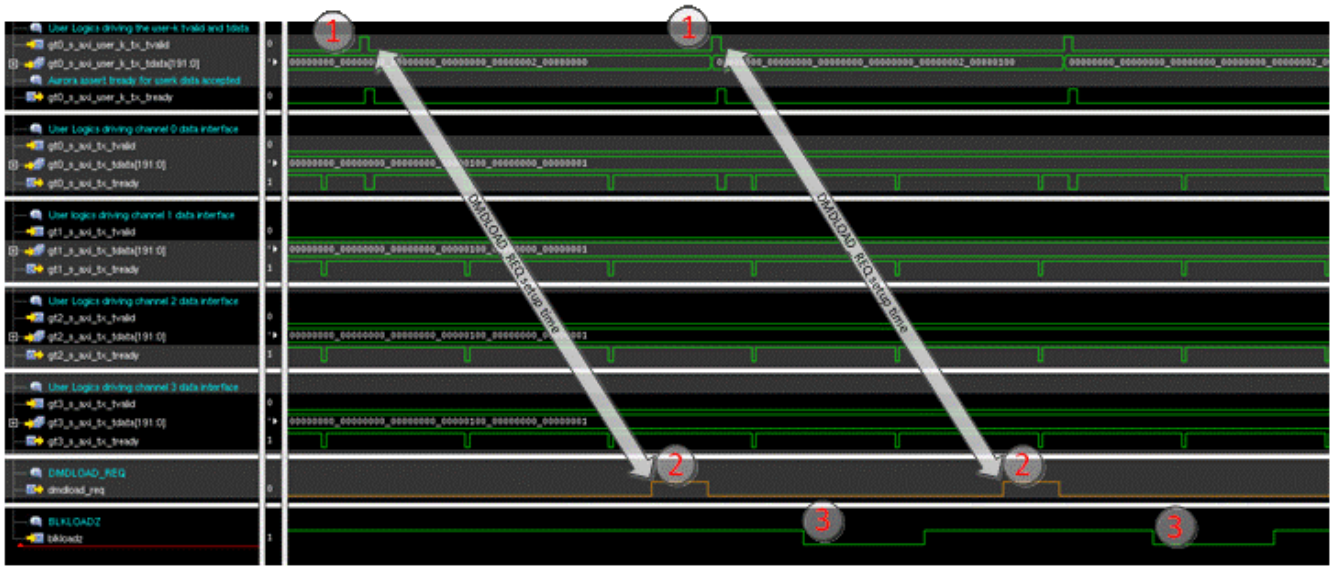


Figure 7-8. Example of DMDLOAD_REQ Setup Time for Block Set Operation

7.3.1.4 Single Channel Transfer Mode

For applications that do not require the speed of loading the DLP991U DMD with all four Aurora 64B/66B input data channels, the DLPC964 controller also supports operation from a single Aurora 64B/66B input data channel. Only Channel 0 can be set up and used in this mode of operation. No other Aurora 64B/66B input data channels can be used for this mode of operation. Figure 7-9 describes the overall data flow of the three Channel 0 Aurora 64B/66B data links from the APPS FPGA to the DLPC964 controller, and then from the DLPC964 controller to the appropriate array segment of the DLP991U DMD.

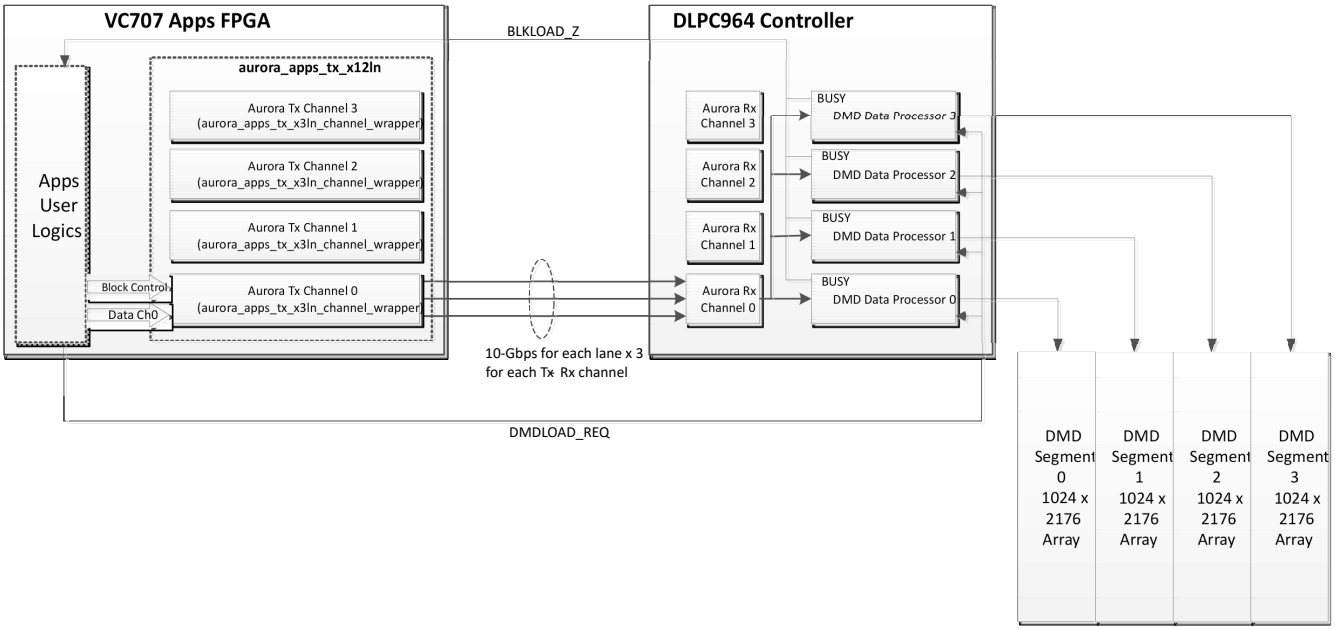


Figure 7-9. System Block Diagram for Single Channel Transfer Mode

Single channel operation is enabled by setting the 'SINGLE_CHANNEL' Block Control Word field to '1' (Table 7-3, SINGLE_CHANNEL = ‘1’), and transferring DMD block data in segment order of 3(first), 2, 1, 0(last) (Table 7-3, DMD_SEGMENT field). In other words, to control a particular DMD block data load, the APPS FPGA must first operate segment 3 of that data block, followed by segment 2, segment 1, and finally segment 0 as the last block data transfer segment.

The guidelines previously outlined for normal (Four Channel) operation mode also apply to Single Channel operation mode, where each block/segment Aurora data transfer must still begin with a Block Control Word, end with the DMDLOAD_REQ, and conform to the 300ns setup time requirement. However, there is one major difference regarding the APPS FPGA and DLPC964 Controller handshaking in this mode. The actual DMD operation triggered by the DMDLOAD_REQ only corresponds to what is sent with segment 0. BLKLOADZ is not asserted for segments 3, 2 and 1. (Figure 7-10 for details).

All four segments of the selected data block must be operated in the correct order, otherwise the DLPC964 controller does not carry out the proper DMD operation to that block.

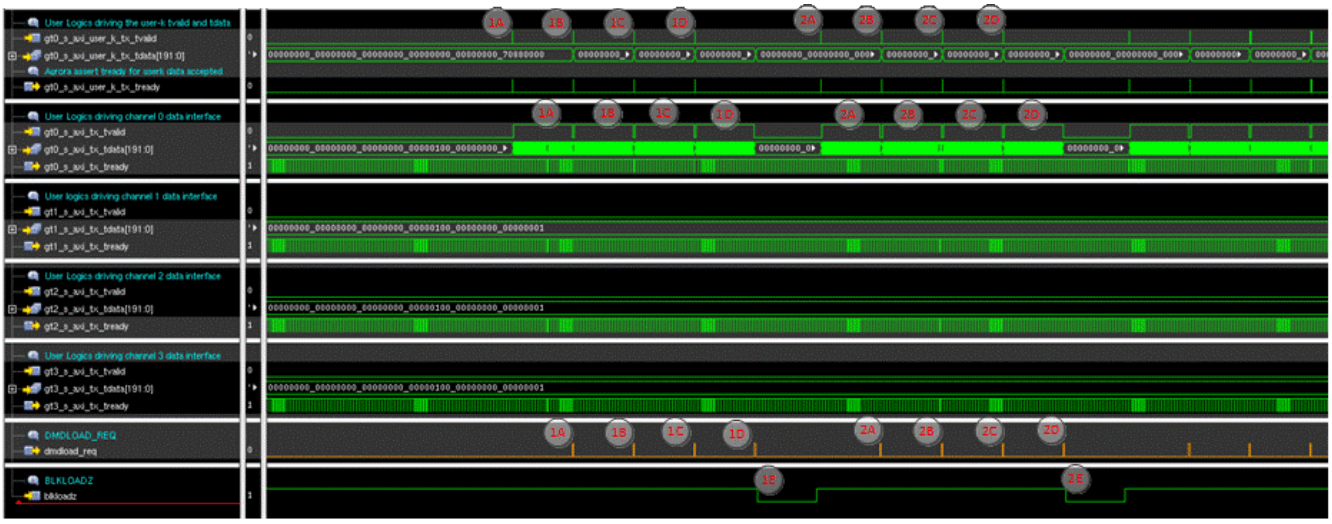


Figure 7-10. Single Channel Operation Waveform Example

1. Apps Aurora Data Transfer for DMD Block 0 in Single Channel Mode:
   a. 1A—Block Control Word, DMD data, and DMDLOAD_REQ for DMD block 0 Segment 3
   b. 1B—Block Control Word, DMD data, and DMDLOAD_REQ for DMD block 0 Segment 2
   c. 1C—Block Control Word, DMD data, and DMDLOAD_REQ for DMD block 0 Segment 1
   d. 1D—Block Control Word, DMD data, and DMDLOAD_REQ for DMD block 0 Segment 0
   e. 1E—Segment 0 DMDLOAD_REQ triggers DLPC964 Controller to begin block 0 data loading. BLKLOADZ is asserted to indicate the operation is in process.
2. Apps Aurora Data Transfer for DMD Block 1 in Single Channel Mode:
   a. 2A—Block Control Word, DMD data, and DMDLOAD_REQ for DMD block 1 Segment 3
   b. 2B—Block Control Word, DMD data, and DMDLOAD_REQ for DMD block 1 Segment 2
   c. 2C—Block Control Word, DMD data, and DMDLOAD_REQ for DMD block 1 Segment 1
   d. 2D—Block Control Word, DMD data, and DMDLOAD_REQ for DMD block 1 Segment 0
   e. 2E—Segment 0 DMDLOAD_REQ triggers DLPC964 Controller to begin block 1 data loading. BLKLOADZ is asserted to indicate the operation in process.

7.3.1.5 DMD Block Array Data Mapping

To each Aurora core, a full DMD block is an array of 1024 columns by 136 rows. Table 7-4 shows the mapping of the 192-bit Aurora data bus to a full DMD block in increment direction (first Aurora data packet starts at row 0). The data bus requires 726 Aurora data packets to transmit a full block. For the last packet, only bits 0–63 are required and bits 64–191 are ignored by DLPC964 controller.

Table 7-5 shows the data mapping in the decrement direction, with the first Aurora data packet starting at row 135.

Table 7-4. Aurora Data Bus to DMD Block Array Mapping—Increment Direction

Row 0	Data 0 [0:191]	Data 1 [0:191]	Data 2 [0:191]	Data 3 [0:191]	Data 4 [0:191]	Data 5 [0:63]
	Column 0 – 191	Column 192 – 383	Column 384 – 575	Column 576 – 767	Column 768 – 959	Column 960 – 1023
Row 1	Data 5 [64:191]	Data 6 [0:191]	Data 7 [0:191]	Data 8 [0:191]	Data 9 [0:191]	Data 10 [0:127]
	Column 0 – 127	Column 128 – 319	Column 320 – 511	Column 512 – 703	Column 704 – 895	Column 896 – 1023
Row 2	Data 10 [128:191]	Data 11 [0:191]	Data 12 [0:191]	Data 13 [0:191]	Data 14 [0:191]	Data 15 [0:191]
	Column 0 – 63	Column 64 – 255	Column 256 – 447	Column 448 – 639	Column 640 – 831	Column 832 – 1023
Row 3	Data 16 [0:191]	Data 17 [0:191]	Data 18 [0:191]	Data 19 [0:191]	Data 20 [0:191]	Data 21 [0:63]
	Column 0 – 191	Column 192 – 383	Column 384 – 575	Column 576 – 767	Column 768 – 959	Column 960 – 1023
.						
.						
.						
Row 134	Data 714 [128:191]	Data 715 [0:191]	Data 716 [0:191]	Data 717 [0:191]	Data 718 [0:191]	Data 719 [0:191]
	Column 0 – 63	Column 64 – 255	Column 256 – 447	Column 448 – 639	Column 640 – 831	Column 832 – 1023
Row 135	Data 720 [0:191]	Data 721 [0:191]	Data 722 [0:191]	Data 723 [0:191]	Data 724 [0:191]	Data 725 [0:63]
	Column 0 – 191	Column 192 – 383	Column 384 – 575	Column 576 – 767	Column 768 – 959	Column 960 – 1023

Table 7-5. Aurora Data Bus to DMD Block Array Mapping—Decrement Direction

Row 0	Data 720 [0:191]	Data 721 [0:191]	Data 722 [0:191]	Data 723 [0:191]	Data 724 [0:191]	Data 725 [0:63]
	Column 0 – 191	Column 192 – 383	Column 384 – 575	Column 576 – 767	Column 768 – 959	Column 960 – 1023
Row 1	Data 714 [128:191]	Data 715 [0:191]	Data 716 [0:191]	Data 717 [0:191]	Data 718 [0:191]	Data 719 [0:127]
	Column 0 – 63	Column 64 – 255	Column 256 – 447	Column 448 – 639	Column 640 – 831	Column 832 – 1023
Row 2	Data 709 [64:191]	Data 710 [0:191]	Data 711 [0:191]	Data 712 [0:191]	Data 713 [0:191]	Data 714 [0:127]
	Column 0 – 127	Column 128 – 319	Column 320 – 511	Column 512 – 703	Column 704 – 895	Column 896 – 1023
Row 3	Data 704 [0:191]	Data 705 [0:191]	Data 706 [0:191]	Data 707 [0:191]	Data 708 [0:191]	Data 709 [0:63]
	Column 0 – 191	Column 192 – 383	Column 384 – 575	Column 576 – 767	Column 768 – 959	Column 960 – 1023
.						
.						
.						
Row 134	Data 5 [128:191]	Data 6 [0:191]	Data 7 [0:191]	Data 8 [0:191]	Data 9 [0:191]	Data 10 [0:191]
	Column 0 – 127	Column 128 – 319	Column 320 – 511	Column 512 – 703	Column 704 – 895	Column 896 – 1023
Row 135	Data 0 [0:191]	Data 1 [0:191]	Data 2 [0:191]	Data 3 [0:191]	Data 4 [0:191]	Data 5 [0:63]
	Column 0 – 191	Column 192 – 383	Column 384 – 575	Column 576 – 767	Column 768 – 959	Column 960 – 1023

7.4 Power Supply Recommendations

7.4.1 Power Supply Distribution and Requirements

The DLPC964 controller and the DLP991U DMD are powered by a power distribution method as shown in Figure 7-11.

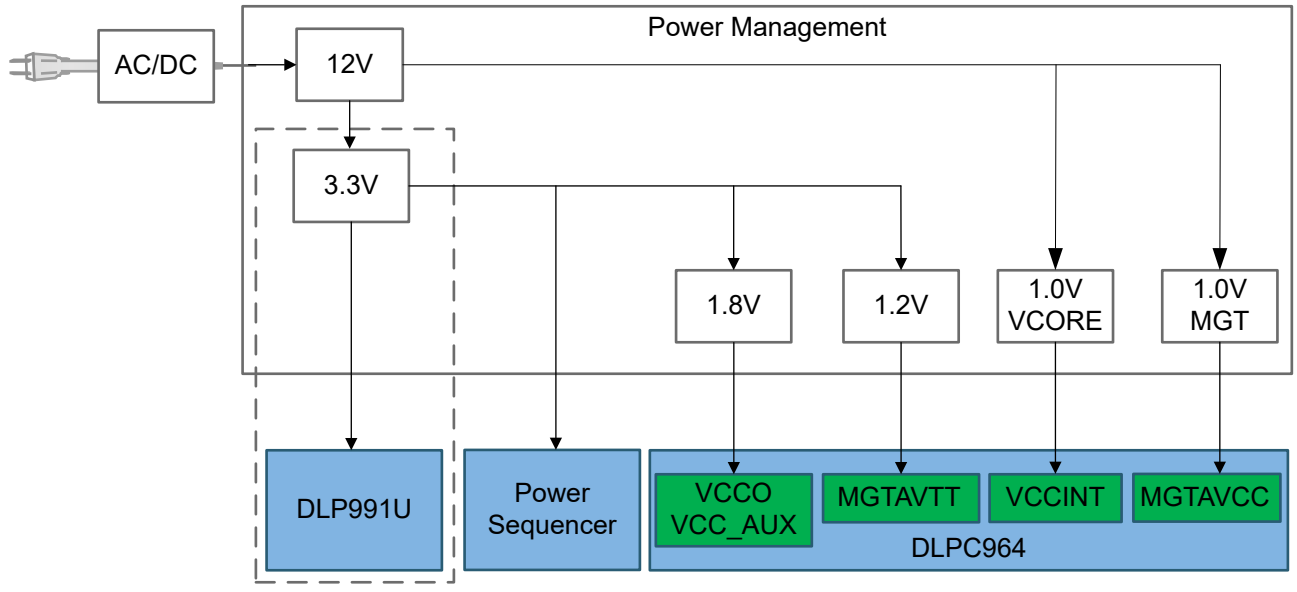


Figure 7-11. Power Distribution

7.4.2 Power Down Requirements

For correct power down operation of the DMD, the following power down procedure must be executed prior to an anticipated power removal:

1. Assert the PARKZ signal low for a minimum of 500µs to allow the DLPC964 to complete the power down procedure for the attached DMD.
2. During the 500µs the PARKZ signal is held low, the DLPC964 will complete the power down procedure and deassert DMD_PWREN low to shut down the DMD power supplies.
3. Following the deassertion of DMD_PWREN, power can be safely removed from the DLP chipset as shown in Figure 7-12.

In the event of an unanticipated power loss, the power management system must detect the input power loss, assert the POWERGOOD signal to the DLPC964, and maintain all operating power levels to the DLPC964 and the DMD for a minimum of 500µs to allow the DLPC964 to complete the power down procedure for the attached DMD.

The proper sequence for parking the DMD and restarting the system without removing power is shown in Figure 7-13 and outlined in the procedure below:

1. Assert PARKZ low to park DMD.
2. Wait a minimum of 500µs for the DLPC964 controller and DMD to complete DMD parking sequence.
3. While PARKZ is still asserted low, (keeping the DMD in parked state), assert SYS_ARSTZ low for minimum of 50ms to reset the DLPC964 controller.
4. Deassert SYS_ARSTZ to bring the DLPC964 controller back to ready.
5. Deassert PARKZ to unpark DMD.

Table 7-6. Power Down Timing Requirements

PARAMETER		MIN	MAX	UNIT
t_{pf}	PARKZ low time	500		us
t_{sa}	SYS_ARSTZ low time	50		ms
t_{ps}	Minimum delay from SYS_ARSTZ active to PARKZ inactive	0		ms

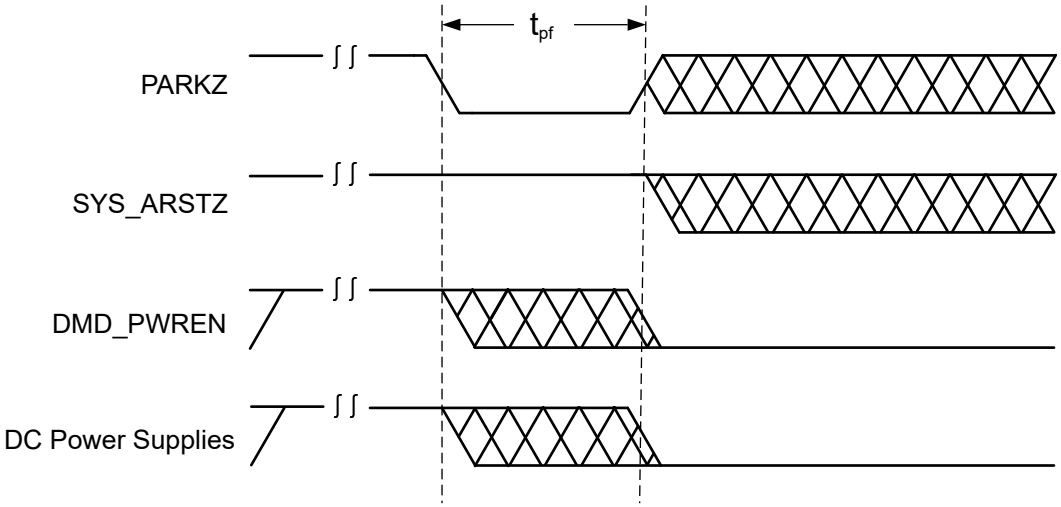


Figure 7-12. Removing Power After Asserting PARKZ

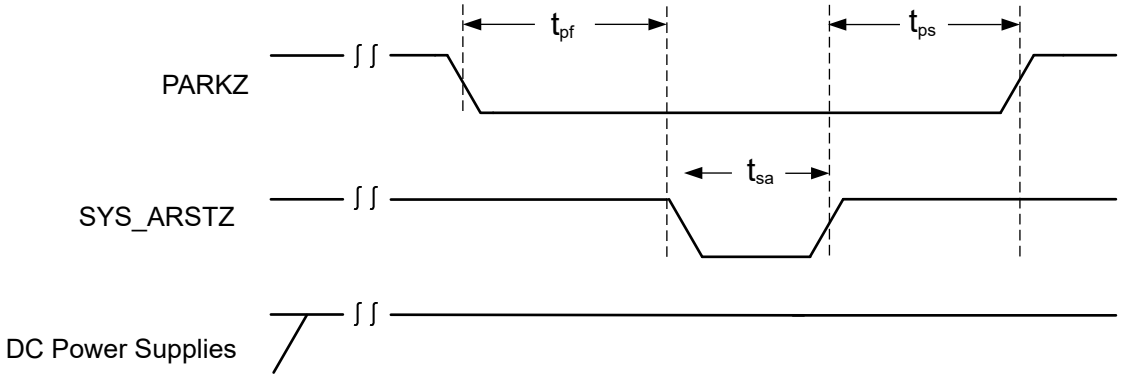


Figure 7-13. Restart Without Removing Power

7.5 Layout

7.5.1 Layout Guidelines

One of the most important factors to gain good performance is designing the PCB with the highest quality signal integrity possible. The following PCB design guidelines provide a reference of an interconnect system.

7.5.1.1 PCB Design Standards

PCBs should be designed and built in accordance with the industry specifications shown in Table 7-7.

Table 7-7. Industry Design Specifications

INDUSTRY SPECIFICATION	APPLICABLE TO
IPC-2221 and IPC2222, Type 3, Class X, at Level B producibility	Board Design
IPC-6011 and IPC-6012, Class 2	PWB fabrication
IPC-SM-840, Class 3, Color Green	Finished PWB solder mask
UL94V-0 Flammability Rating and Marking	Finished PWB
UL796 Rating and Marking	Finished PWB

PCB Fabrication:

- Etch thickness: 1/2-oz copper (0.6 mil)
- Single-ended signal impedance: 50-Ω ±10%

- Differential signal impedance: 100Ω ±10%

PCB Stack-up:

- Ground planes for proper return path.
- Power planes for proper supply to circuits.
- Dielectric material with a low Loss-Tangent, for example: Megtron 6, (Er): 3.4 (nominal).

7.5.1.2 Signal Layers

The PCB signal layers should follow typical good practice guidelines including:

- Layer changes should be minimized for single-ended signals.
- Individual differential pairs of a bus can be routed on different layers, but the signals of a given pair should not change layers.
- Stubs should be avoided.
- Low-frequency signals should be routed on the outer layers.
- Differential pair signals should be prioritized and routed first.
- 10-Gbps Aurora 64B/66B differential signals should have vias back-drilled to improve signal integrity.
- Pin swapping on components is not allowed.
- Polarized capacitors should be drawn with the same orientation.

The PCB should have a solder mask on the top and bottom layers.

- The solder mask should not cover the vias.
- Except for fine pitch devices (pitch ≤ 0.032 inches), the copper pads and the solder mask cutout should be of the same size.
- Solder mask between pads of fine pitch devices should be removed.
- In the BGA package, the copper pads and the solder mask cutout should be of the same size.

High-speed connectors that meet the following requirements should be used:

- For the 10Gbps Aurora 64B/66B interface:
  - Differential crosstalk: <1%
  - Differential impedance: 100Ω ±10%
  - Insertion loss of the total connector/cabling system should be: <3dB at 5GHz.
- For the 3.6Gbps HSSI DMD interface:
  - Differential crosstalk: <1%
  - Differential impedance: 100Ω ±10%
  - Insertion Loss of the total connector/cabling system should be: <3dB at 1.8GHz.

7.5.1.3 General PCB Routing

Fiducials for automatic component placement should be 0.05-inch copper with a 0.1-inch cutout (antipad). Fiducials for optical auto placement are placed on three corners of both sides of the PCB.

7.5.1.3.1 Trace Minimum Spacing

All single-ended 50Ω signals should have a minimum spacing relative to other signals of 3x trace-width. For example, a 5 mil wide trace should have 15 mils of spacing relative to other signals. All differential 100Ω pairs should have a minimum spacing relative to other signals of 3x the spacing between each of the pairs. Other special trace spacing requirements are listed in Table 7-8.

Table 7-8. Trace Minimum Spacing

SIGNAL	PWR	GND	SINGLE-ENDED	DIFFERENTIAL PAIRS	UNIT
				Pair-to-Pair	
PWR	15	5	15	15	mils
GND	5		5	5	mils

Table 7-8. Trace Minimum Spacing (continued)

SIGNAL	PWR	GND	SINGLE-ENDED	DIFFERENTIAL PAIRS	UNIT
				Pair-to-Pair	
SYS_CLK100	15	5	3x intra-pair (P-to-N) spacing	3x intra-pair (P-to-N) spacing	mils
GTRX_CH(0,1,2,3)_REFCLK	15	5	3x intra-pair (P-to-N) spacing	3x intra-pair (P-to-N) spacing	mils
DMD_GTREFCLK_IN_(A,B,C,D)	15	5	3x intra-pair (P-to-N) spacing	3x intra-pair (P-to-N) spacing	mils
Aurora 64B/66B Input Interface - CH(0,1,2,3)_GTRX[3:0]	15	5	3x intra-pair (P-to-N) spacing	3x intra-pair (P-to-N) spacing	mils
Control Signals - WDT_ENABLEZ, LOAD2, DMDLOAD_REQ, RXLPMEN, PARKZ, SYS_ARSTZ, EXT_HSSI_RST	15	5	3x trace width spacing	3x intra-pair (P-to-N) spacing	mils
Status Signals - BLKLOADZ, MCP(3:0)_ACTIVE, HSSI_BUS_ERR, HSSI_RST_ACT, INIT_DONE	15	5	3x trace width spacing	3x intra-pair (P-to-N) spacing	mils
HSSI DMD Interface - DMD_D_(A,B,C,D)[7:0], DMD_DCLK_(A,B,C,D),	15	5	3x intra-pair (P-to-N) spacing	3x intra-pair (P-to-N) spacing	mils
DMD LS Interface - DMD_LS_CLK, DMD_LS_WDATA, DMD_LS_RDATA_(A,B,C,D)	15	5	3x trace width spacing	3x intra-pair (P-to-N) spacing	mils
All other signals	15	5	3x trace width spacing	3x intra-pair (P-to-N) spacing	mils

7.5.1.3.2 Trace Length Matching

7.5.1.3.2.1 HSSI Output Bus Skew

Table 7-9 lists the high speed serial DMD Interface routing constraints. Refer to the *DLP991U Industrial Digital Micromirror Device Data Sheet* regarding specific DMD HSSI input bus skew requirements.

Table 7-9. High Speed Serial DMD Interface Routing Constraints

SIGNAL	REFERENCE SIGNAL	ROUTING SPEC	UNIT
DMD_D_A{0…7}_P, DMD_D_A{0…7}_N	DMD_DCLK_A_P, DMD_DCLK_A_N	± 45	ps
DMD_D_B{0…7}_P, DMD_D_B{0…7}_N	DMD_DCLK_B_P, DMD_DCLK_B_N	± 45	ps
DMD_D_C{0…7}_P, DMD_D_C{0…7}_N	DMD_DCLK_C_P, DMD_DCLK_C_N	± 45	ps
DMD_D_D{0…7}_P, DMD_D_D{0…7}_N	DMD_DCLK_D_P, DMD_DCLK_D_N	± 45	ps
DMD_D_A bus	DMD_D_B bus	± 45	ps
DMD_D_C bus	DMD_D_D bus	± 45	ps

Table 7-9. High Speed Serial DMD Interface Routing Constraints (continued)

SIGNAL	REFERENCE SIGNAL	ROUTING SPEC	UNIT
DMD_D_A bus	DMD_D_C bus	± 45	ps
Intra-pair P	Intra-pair N	± 2	ps

7.5.1.3.2.2 Aurora 64B/66B Input Bus Skew

The Aurora 64B/66B input buses of the DLPC964 Controller operate at 10Gbps, and special care should be taken with trace length matching of the traces within the bus. It is recommended that the Aurora 64B/66B input buses of the DLPC964 have no more than 1ps skew between differential pairs within a bus, and 0.2ps skew between p and n traces of a differential signal. For more detailed information about PCB layout requirements of the AMD Aurora 64B/66B Interface, please refer to AMD's website.

7.5.1.3.2.2.1 Other Timing Critical Signals

Table 7-10 lists the routing constraints that should be considered for other timing critical signals.

Table 7-10. Other Timing Critical Signals

SIGNAL	CONSTRAINTS
FLASH_CSZ, FLASH_MISO, FLASH_CCLK, FLASH_MOSI	Matched within 18ps of one another.
DMD_LS_CLK_P, DMD_LS_CLK_N DMD_LS_WDATA_P, DMD_LS_WDATA_N, DMD_LS_RDATA_{A,B,C,D}	Intrapair (P-to-N) matched within 2ps. Differential pairs matched within 4ps of one another. DMD_LS_RDATA_{A,B,C,D} matched within 1ns of DMD_LS_CLK_{P,N}.
GTTX_CH{0,1,2,3}_REFCLK_P, GTTX_CH{0,1,2,3}_REFCLK_N, GTRX_CH{0,1,2,3}_REFCLK_P, GTRX_CH{0,1,2,3}_REFCLK_N REFCLK_UI_P, REFCLK_UI_N MGT_REFCLK_P, MGT_REFCLK_N	Intrapair (P-to-N) matched within 2ps. Differential pairs matched within 18ps of one another.

7.5.1.3.3 Trace Impedance and Routing Priority

For best performance, it is recommended that the trace impedance for differential signals described in xx is followed. All signals should be 50Ω controlled impedance unless otherwise noted in Table 7-11.

Table 7-11. Trace Impedance

Signals	Differential Impedance
SYS_CLK100	100Ω differential
GTRX_CH(0,1,2,3)_REFCLK	100Ω differential
DMD_GTREFCLK_IN_(A,B,C,D)	100Ω differential
Aurora 64B/66B Input Interface - CH(0,1,2,3)_GTRX[3:0]	100Ω differential

Table 7-11. Trace Impedance (continued)

Signals	Differential Impedance
HSSI DMD Interface - DMD_D_(A,B,C,D)[7:0], DMD_DCLK_(A,B,C,D)	100Ω differential
DMD LS Interface - DMD_LS_CLK, DMD_LS_WDATA	100Ω differential

Table 7-12 lists the routing priority of the signals.

Table 7-12. Routing Priority

Signals	Priority
HSS Input Interface - CH(0,1,2,3)_GTRX[3:0]	1
HSSI DMD Interface - DMD_D_(A,B,C,D)[7:0], DMD_DCLK_(A,B,C,D)	1
DMD LS Interface - DMD_LS_CLK, DMD_LS_WDATA	2
SYS_CLK100	2
GTRX_CH(0,1,2,3)_REFCLK	2
DMD_GTREFCLK_IN_(A,B,C,D)	2
Control Signals - WDT_ENABLEZ, LOAD2, DMDLOAD_REQ, RXLPMEN, PARKZ, SYS_ARSTZ, EXT_HSSI_RST	3
Status Signals - BLKLOADZ, MCP(3:0)_ACTIVE, HSSI_BUS_ERR, HSSI_RST_ACT, INIT_DONE	4
All other signals	5

7.5.2 Power and Ground Planes

The following are recommendations for best performance:

- Solid ground planes between each signal routing layer
- Solid power planes for voltages
- Connect power and ground pins to these planes through a via for each pin.
- Minimize trace lengths for the component power and ground pins to 0.100 inches or less.
- Space apart vias to avoid forming slots in power planes.
- High-speed signals must not cross over a slot in the adjacent (reference) power planes.
- Placing extra vias is not required if there are sufficient ground vias due to normal ground connection devices.

7.5.3 Power Vias

Power and ground pins of each component shall be connected to the power and ground planes with a via for each pin. Avoid sharing vias to the power plane among multiple power pins, where possible. Trace lengths for component power and ground pins should be minimized (ideally, less than 0.100-inch). Unused or spare device pins that are connected to power or ground may be connected together with a single via to power or ground. The minimum spacing between vias shall be 0.050-inch to prevent slots from being developed on the ground plane.

7.5.4 Decoupling

Decoupling capacitors must be located as near as possible to the DLPC964 voltage supply pins. Capacitors should not share vias. The DLPC964 power pins can be connected directly to the decoupling capacitor (no via) if the trace is less than an 0.03 inch. Otherwise, the component should be tied to the voltage or ground plane through a separate via. All capacitors should be connected to the power planes with trace lengths less than an 0.05 inch.

7.6 Layout Example

The PCB layer design may vary depending on system design. However, careful attention is required to meet design considerations. Table 7-13 shows a layer definition table and Figure 7-14 shows a PCB stack-up. The

PCB stack-up uses Nelco N4000-13-SI as the dielectric material to improve the signal slew rate for better performance of the Aurora 64B/66B input interface and the HSSI DMD output interface.

Table 7-13. Layer Definition

LAYER	DESCRIPTION
Top	Top components. Low frequency signals routing, ground, voltage mini-planes
2	Ground
3	High speed signal layer
4	Ground
5	Split power plane
6	Split power plane
7	Ground
8	High speed signal layer
9	Ground
Bottom	Discrete components. Low frequency signals routing, ground, voltage mini-planes

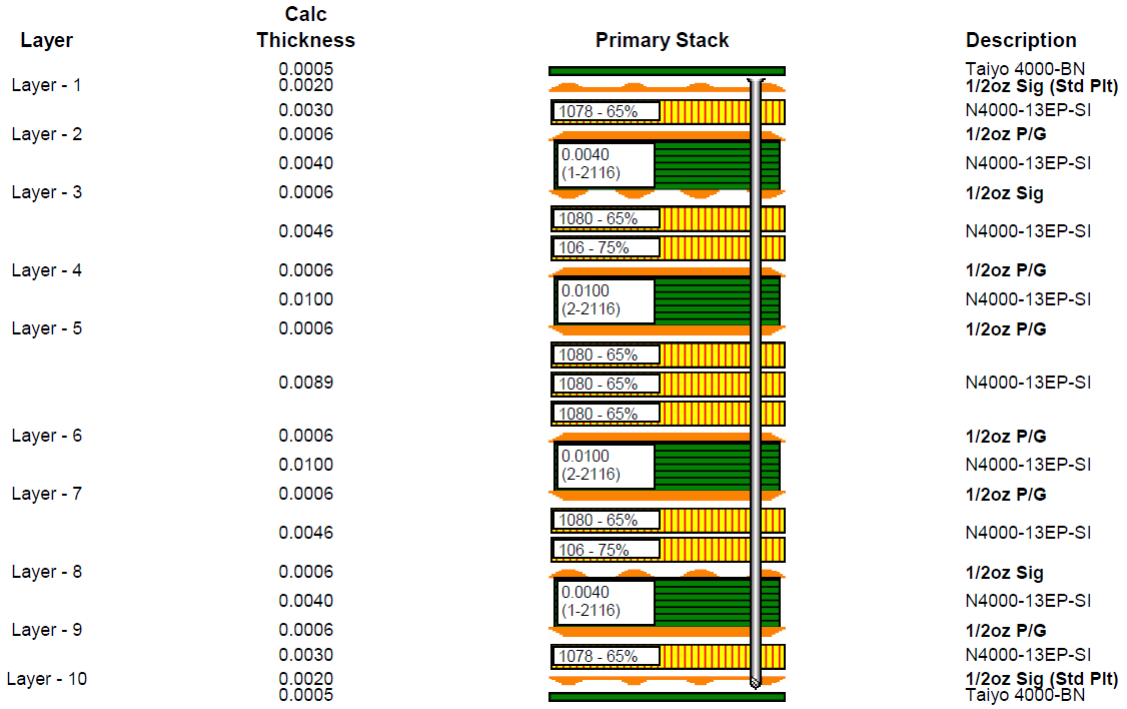


Figure 7-14. PCB Stack-Up

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

- *AMD PG074 Application Note*
- *DLP991U Industrial Digital Micromirror Device Data Sheet*
- *7-Series FPGAs Packaging and Pinout Product Specification Guide*
- *AMD 7-Series FPGAs GTX/GTH Transceivers User Guide*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC964ZUM	ACTIVE	FCBGA	ZUM	1156	1	TBD	Call TI	Call TI	0 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

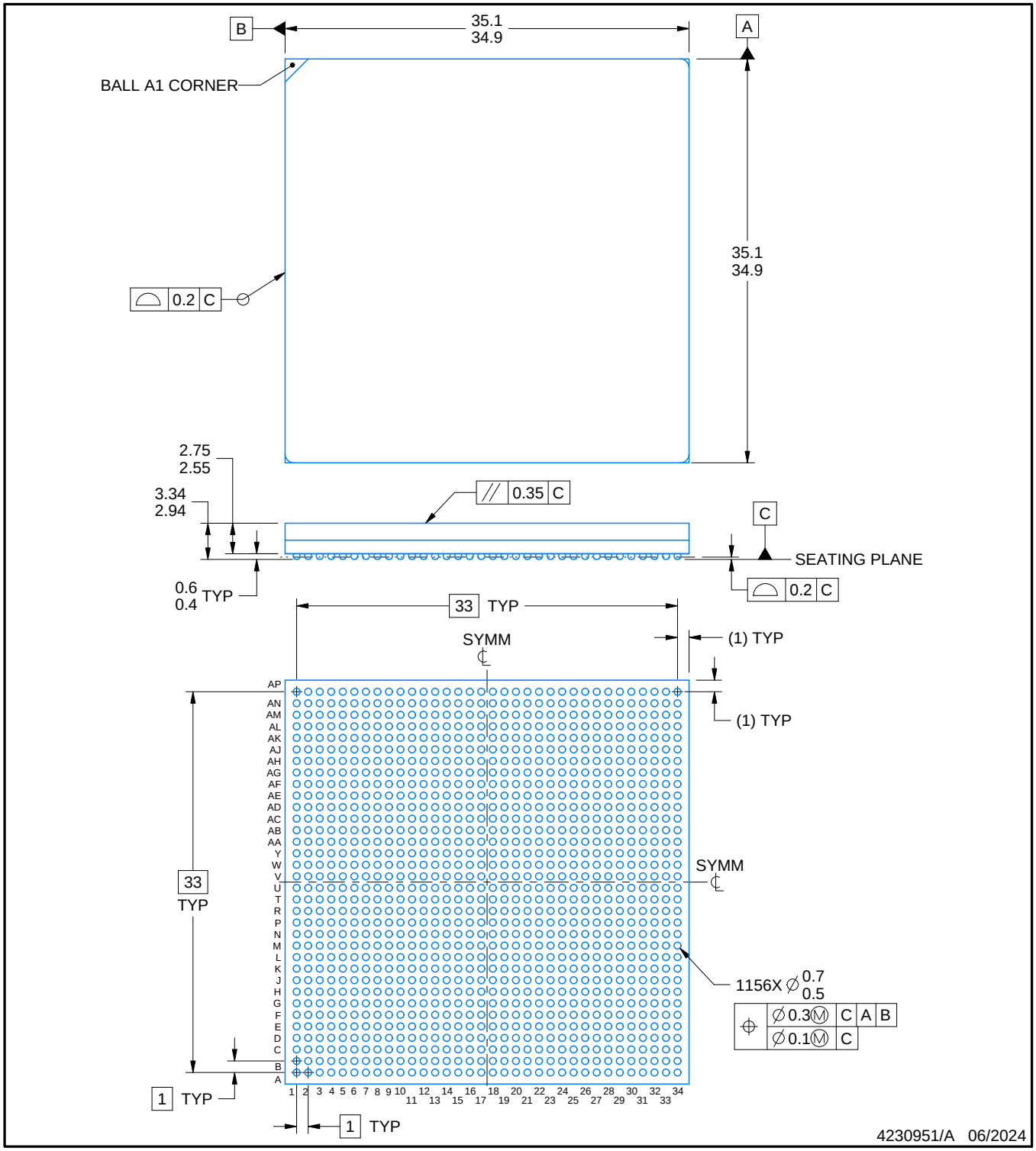
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

ZUM1156A

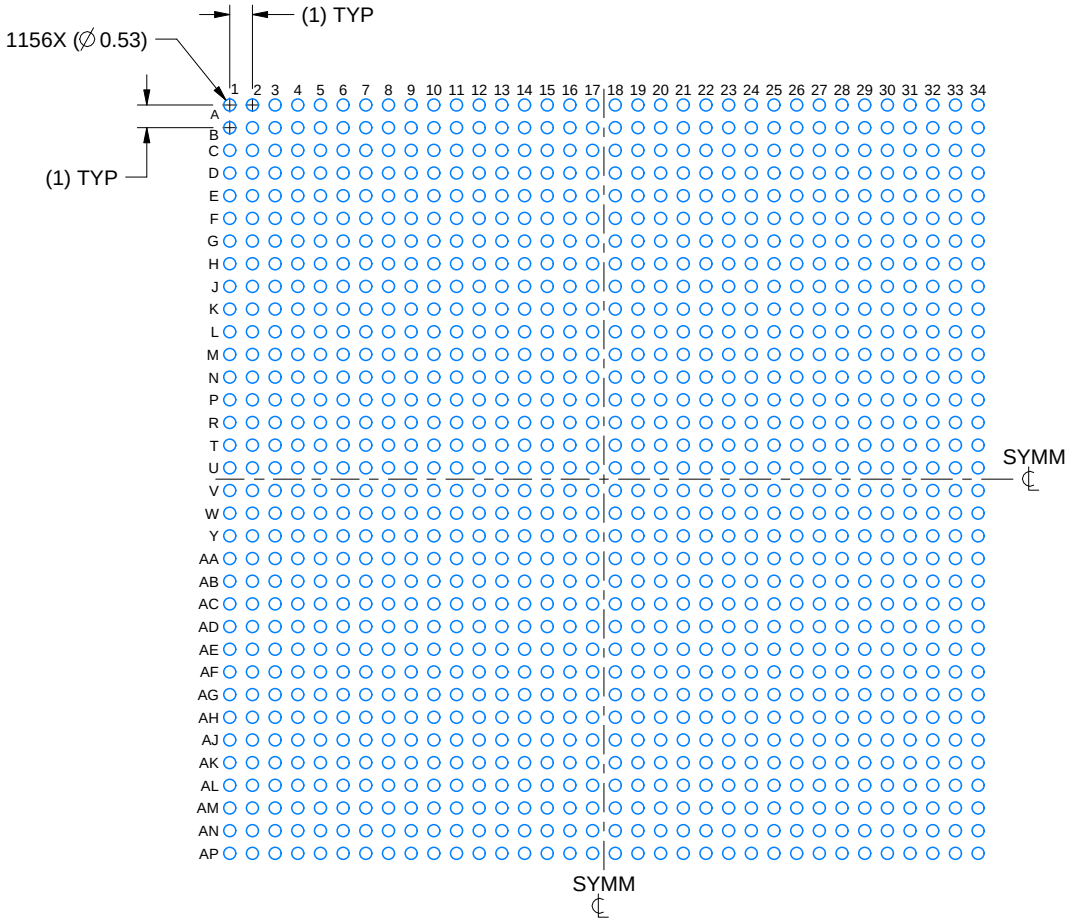
FCBGA - 3.35 mm max height

PLASTIC BALL GRID ARRAY

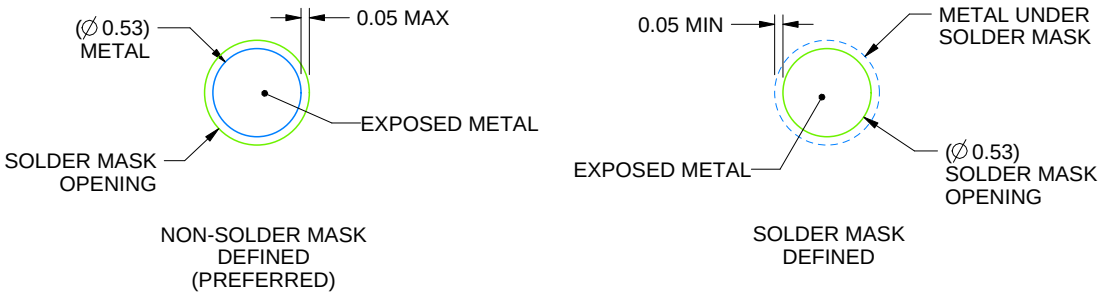


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:3X



SOLDER MASK DETAILS
NOT TO SCALE

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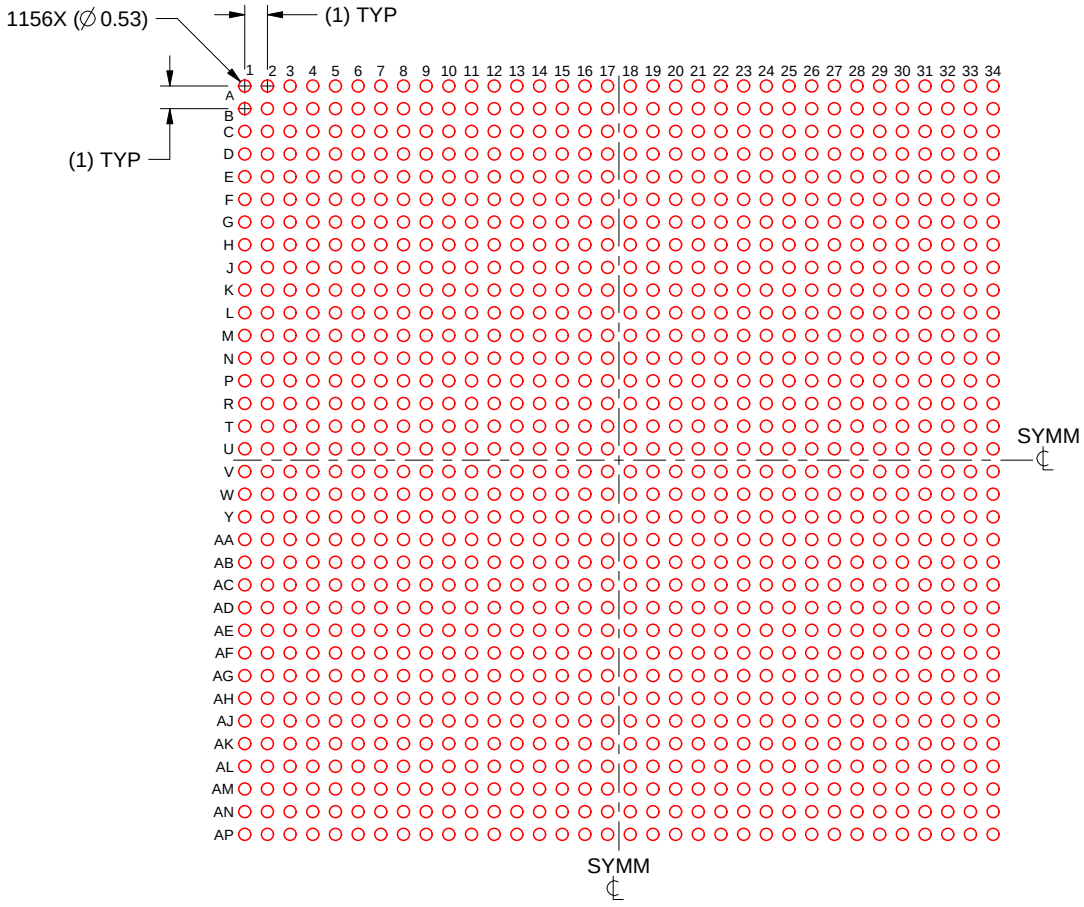
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:3X

4230951/A 06/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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