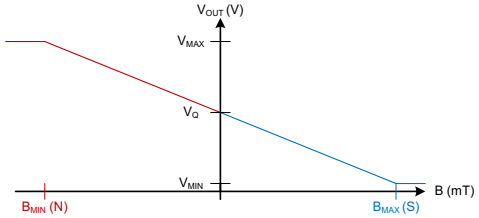
DRV5053 Analog-Bipolar Hall Effect Sensor

1 Features

- Linear output hall sensor
- Superior temperature stability
  - Sensitivity ±10% over temperature
- High sensitivity options:
  - –11 mV/mT (OA, see Figure 17)
  - –23 mV/mT (PA)
  - –45 mV/mT (RA)
  - –90 mV/mT (VA)
  - +23 mV/mT (CA)
  - +45 mV/mT (EA)
- Supports a wide voltage range
  - 2.5 V to 38 V
  - No external regulator required
- Wide operating temperature range
  - T_A = –40 to 125°C (Q, see Figure 17)
- Amplified output stage
  - 2.3-mA sink, 300-µA source
- Output voltage: 0.2 V to approximately 1.8 V
  - B = 0 mT, OUT = 1 V
- Fast power-on: 35 µs
- Small package and footprint
  - Surface mount 3-pin SOT-23 (DBZ)
    - 2.92 mm × 2.37 mm
  - Through-hole 3-pin TO-92 (LPG)
    - 4.00 mm × 3.15 mm
- **Protection features:**
  - Reverse supply protection (up to –22 V)
  - Supports up to 40-V load dump
  - Output short-circuit protection
  - Output current limitation

2 Applications

- Flow Meters
- Docking Adjustment
- Vibration Correction
- Damper Controls



Output State

3 Description

The DRV5053 device is a chopper-stabilized Hall IC that offers a magnetic sensing solution with superior sensitivity stability over temperature and integrated protection features.

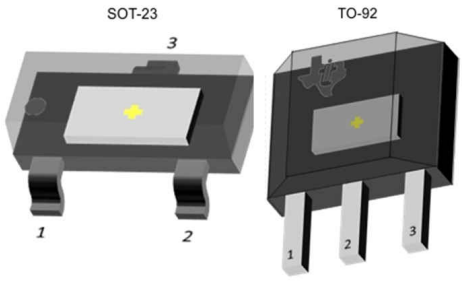
The 0-V to 2-V analog output responds linearly to the applied magnetic flux density, and distinguishes the polarity of magnetic field direction. A wide operating voltage range from 2.5 V to 38 V with reverse polarity protection up to –22 V makes the device suitable for a wide range of industrial and consumer applications.

Internal protection functions are provided for reverse supply conditions, load dump, and output short circuit or overcurrent.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV5053	SOT-23 (3)	2.92 mm × 1.30 mm
	TO-92 (3)	4.00 mm × 3.15 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Device Packages

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4 Revision History

Changes from Revision C (December 2015) to Revision D (February 2023) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Changed the *Device Information* table title to *Package Information* 1
- Moved the *Power Supply Recommendations* section to the *Application and Implementation* section....14

Changes from Revision B (September 2014) to Revision C (December 2015) **Page**

- Corrected body size of SOT-23 package and SIP package name to TO-92 1
- Added B_{MAX} to *Absolute Maximum Ratings* 4
- Removed table note from junction temperature 4
- Updated the typical value for B_N and V_N for each version....5
- Updated Figure 6-6 7
- Updated the *Functional Block Diagram* 8
- Updated *Output Stage* 11
- Updated package tape and reel options for M and blank 15

Changes from Revision A (August 2014) to Revision B (September 2014) **Page**

- Updated high sensitivity options 1
- Updated the sensitivity device values and typicals. Updated typical and max values for DRV5053VA: –80 mV/mT 5
- Updated *Typical Characteristics* graphs 7

Changes from Revision * (May 2014) to Revision A (August 2014) **Page**

- Updated device status to production data 1
- Changed the maximum T_J value from 175°C to 150°C 4
- Updated *Magnetic Characteristics* table. 5

5 Pin Configuration and Functions

For additional configuration information, see *Device Markings* and *Mechanical, Packaging, and Orderable Information*.

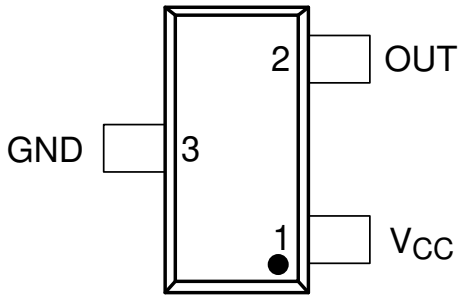


Figure 5-1. DBZ Package 3-Pin SOT-23 Top View

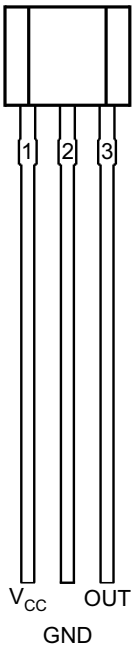


Figure 5-2. LPG Package 3-Pin TO-92 Top View

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBZ	LPG		
GND	3	2	GND	Ground pin
V_{CC}	1	1	Power	2.5 V to 38 V power supply. Bypass this pin to the GND pin with a 0.01-µF (minimum) ceramic capacitor rated for V_{CC}.
OUT	2	3	Output	Hall sensor analog output. 1 V output corresponds to B = 0 mT

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Power supply voltage	V_{CC}	–22[2]	40	V
	Voltage ramp rate (V_{CC}), V_{CC} < 5 V	Unlimited		V/µs
	Voltage ramp rate (V_{CC}), V_{CC} > 5 V	0	2	
Output pin voltage		–0.5	2.5	V
Output pin reverse current during reverse supply condition		0	–20	mA
Magnetic flux density, B_{MAX}		Unlimited		
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Specified by design. Only tested to –20 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	2.5	38	V
V_{OUT}	Output pin voltage (OUT)	0	2	V
I_{SOURCE}	Output pin current source (OUT)	0	300	µA
I_{SINK}	Output pin current sink (OUT)	0	2.3	mA
T_A	Operating ambient temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		DRV5053		UNIT
		DBZ (SOT-23)	LPG (TO-92)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	333.2	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.9	98.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.9	154.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	40	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	154.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{CC})						
V_{CC}	V_{CC} operating voltage		2.5		38	V
I_{CC}	Operating supply current	V_{CC} = 2.5 V to 38 V, T_A = 25°C		2.7		mA
		V_{CC} = 2.5 V to 38 V, T_A = 125°C		3	3.6	
t_{on}	Power-on time			35	50	µs
PROTECTION CIRCUITS						
V_{CCR}	Reverse supply voltage		–22			V
$I_{OCP,SOURCE}$	Overcurrent protection level	Sourcing current		300		µA
$I_{OCP,SINK}$	Overcurrent protection level	Sinking current		2.3		mA

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT (OUT)						
t_d	Output delay time	T_A = 25°C		13	25	µs

6.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT[2]
V_Q	Quiescent output	B = 0 mT T_A = –40°C to 125°C	0.9	1.02	1.15	V
f_{BW}	Bandwidth[3]		20			kHz
B_N	Input-referred noise[1]	C_{OUT} = 50 pF T_A = –40°C to 125°C	0.40	0.49	0.79	mT_{pp}
Le	Linearity[4]	$–B_{SAT} < B < B_{SAT}$		1%		
$V_{OUT\ MIN}$	Output saturation voltage (minimum)	$B < –B_{SAT}$			0.2	V
$V_{OUT\ MAX}$	Output saturation voltage (maximum)	$B > B_{SAT}$	1.8			V
DRV5053OA: –11 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C	–17.5	–11	–5	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF T_A ≈ –40°C to 125°C		5		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C		73		mT
DRV5053PA: –23 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C	–35	–23	–10	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF T_A ≈ –40°C to 125°C		11		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C		35		mT

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(2)
DRV5053RA: –45 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C	–70	–45	–20	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF T_A ≈ –40°C to 125°C		22		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C		18		mT
DRV5053VA: –90 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C	–140	–90	–45	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF T_A ≈ –40°C to 125°C		44		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C		9		mT
DRV5053CA: 23 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C	10	23	35	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF T_A ≈ –40°C to 125°C		11		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C		35		mT
DRV5053EA: 45 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C	20	45	70	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF T_A ≈ –40°C to 125°C		22		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V T_A ≈ –40°C to 125°C		18		mT

(1) Not tested in production; limits are based on characterization data.
(2) 1 mT = 10 Gauss
(3) Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.
(4) Linearity describes the change in sensitivity across the B-range. The sensitivity near B_{SAT} is typically within 1% of the sensitivity near B = 0 mT.

6.8 Typical Characteristics

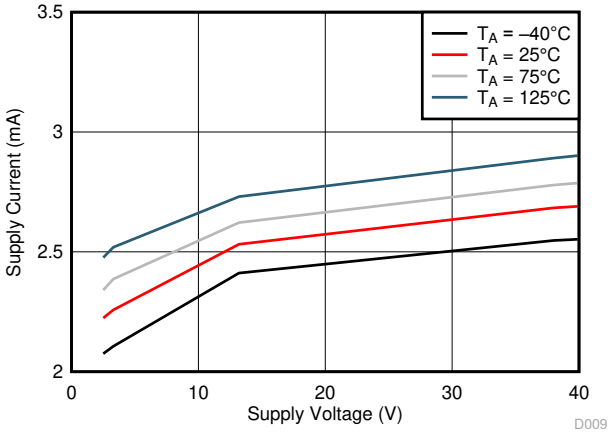


Figure 6-1. I_{CC} vs V_{CC}

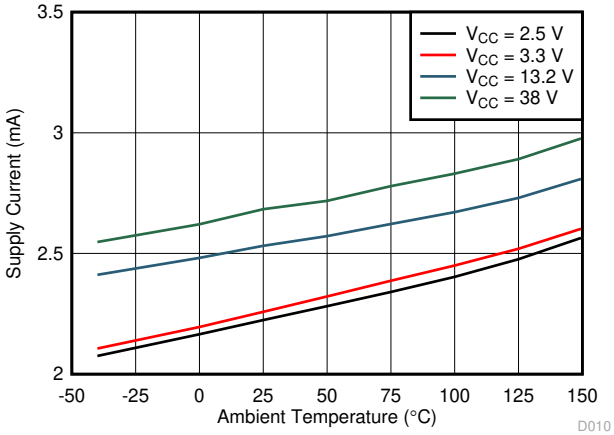
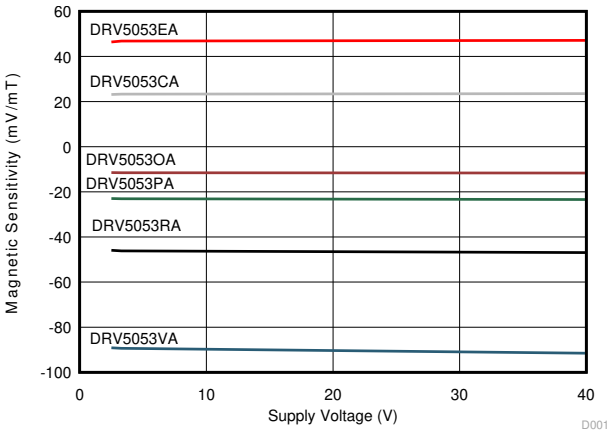
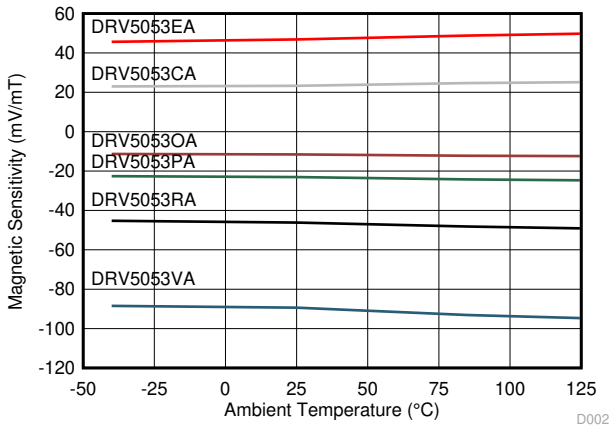


Figure 6-2. I_{CC} vs Temperature



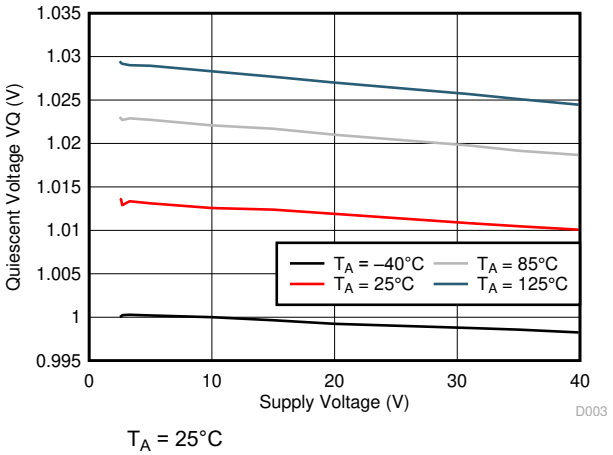
T_A = 25°C

Figure 6-3. Sensitivity vs V_{CC}



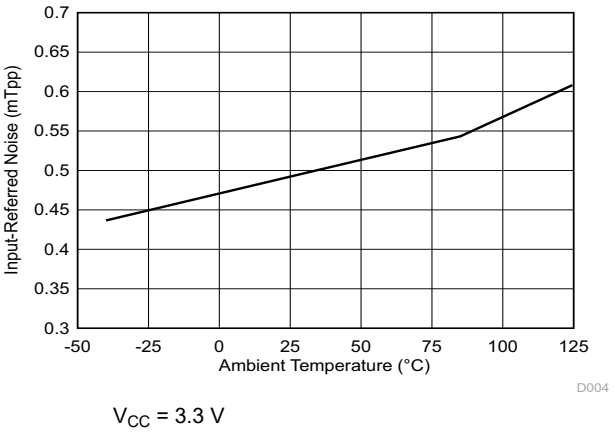
V_{CC} = 3.3 V

Figure 6-4. Sensitivity vs Temperature



T_A = 25°C

Figure 6-5. V_Q vs V_{CC}



V_{CC} = 3.3 V

Figure 6-6. B_N vs Temperature

7 Detailed Description

7.1 Overview

The DRV5053 device is a chopper-stabilized Hall sensor with an analog output for magnetic sensing applications. The DRV5053 device can be powered with a supply voltage between 2.5 V and 38 V, and will survive –22 V reverse battery conditions continuously. Note that the DRV5053 device will not be operating when approximately –22 V to 2.4 V is applied to V_{CC} (with respect to GND). In addition, the device can withstand supply voltages up to 40 V for transient durations.

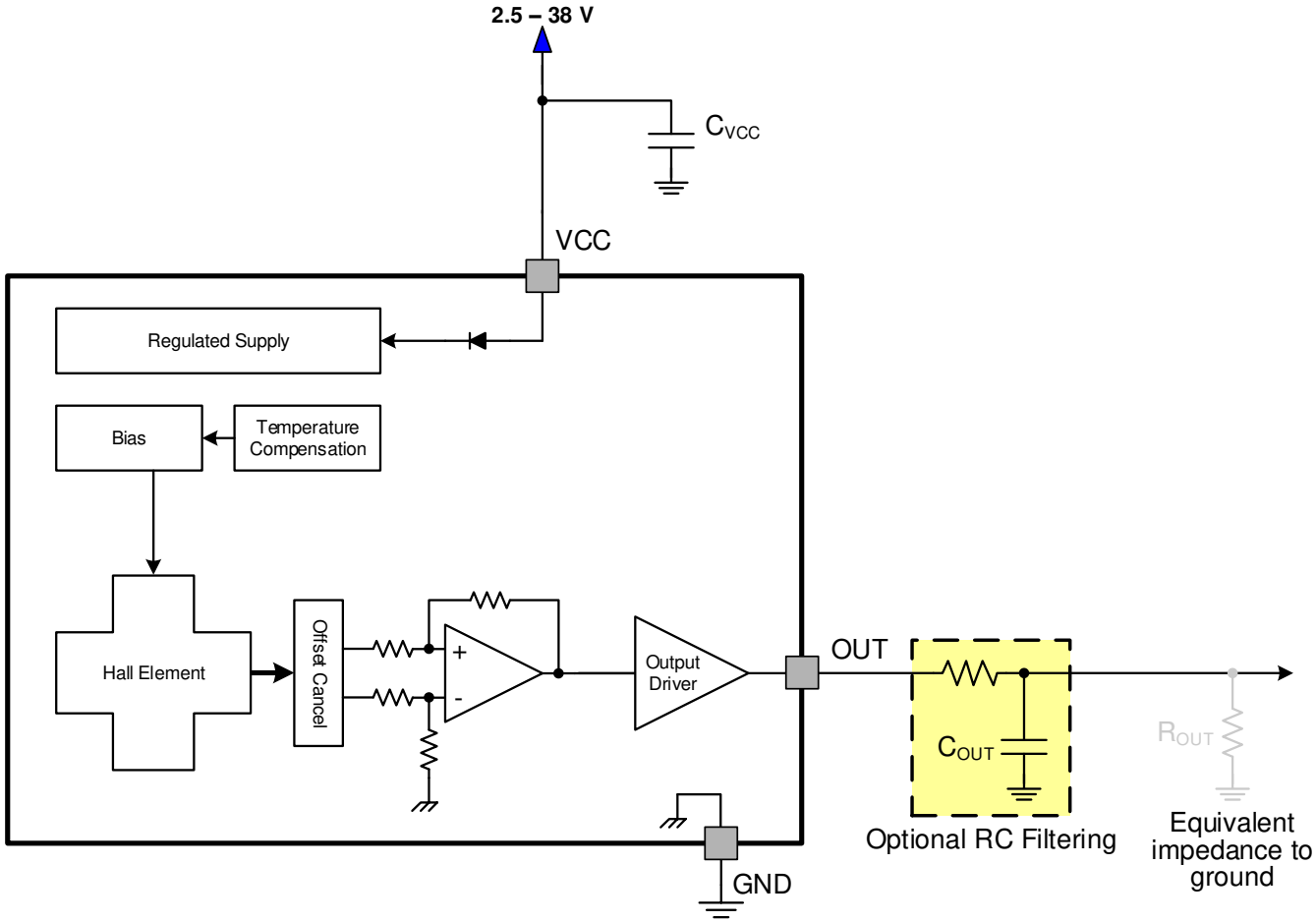
The output voltage is dependent on the magnetic field perpendicular to the package. The absence of a magnetic field will result in OUT = 1 V. A magnetic field will cause the output voltage to change linearly with the magnetic field.

The field polarity is defined as follows: a south pole near the marked side of the package is a positive magnetic field. A north pole near the marked side of the package is a negative magnetic field.

For devices with a negative sensitivity (that is, DRV5053RA: –40 mV/mT), a south pole will cause the output voltage to drop below 1 V, and a north pole will cause the output to rise above 1 V.

For devices with a positive sensitivity (that is, DRV5053EA: +40 mV/mT), a south pole will cause the output voltage to rise above 1 V, and a north pole will cause the output to drop below 1 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Field Direction Definition

Figure 7-1 shows the positive magnetic field defined as a south pole near the marked side of the package.

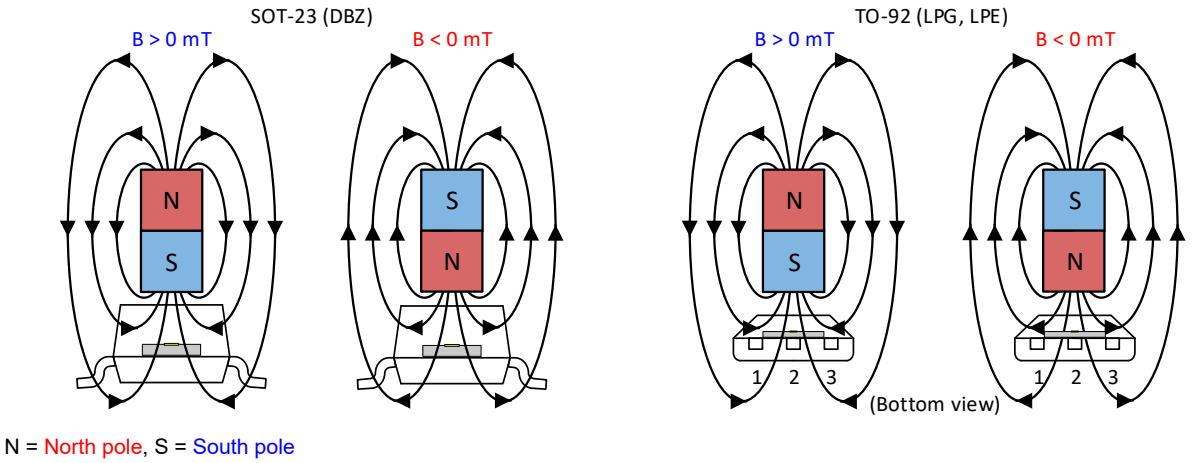


Figure 7-1. Field Direction Definition

7.3.2 Device Output

The DRV5053 device output is defined below for negative sensitivity (that is, –45 mV/mT, RA) and positive sensitivity (that is, +45 mV/mT, EA):

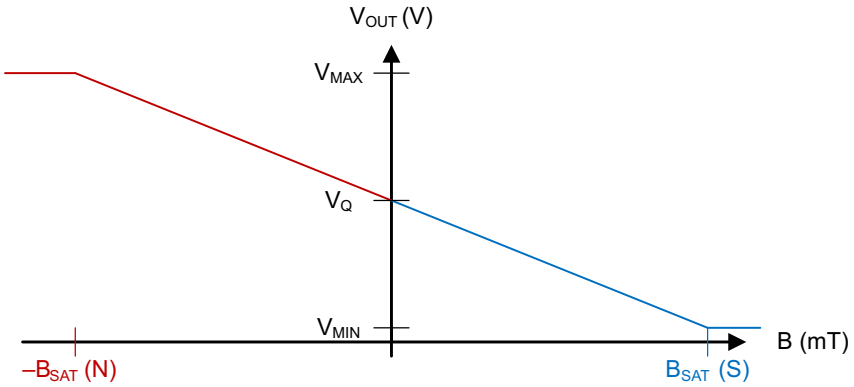


Figure 7-2. DRV5053 – Negative Sensitivity

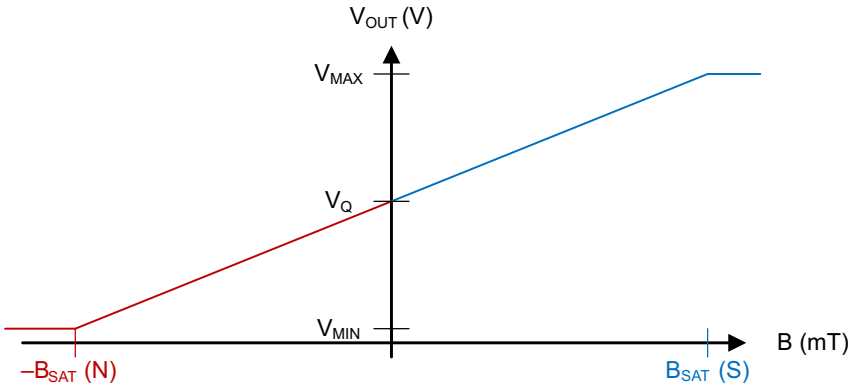


Figure 7-3. DRV5053 – Positive Sensitivity

7.3.3 Power-On Time

After applying V_{CC} to the DRV5053 device, t_{on} must elapse before OUT is valid. Figure 7-4 shows Case 1 and Figure 7-5 shows Case 2. The output is defined assuming a negative sensitivity device and a constant magnetic field $–B_{SAT} < B < B_{SAT}$.

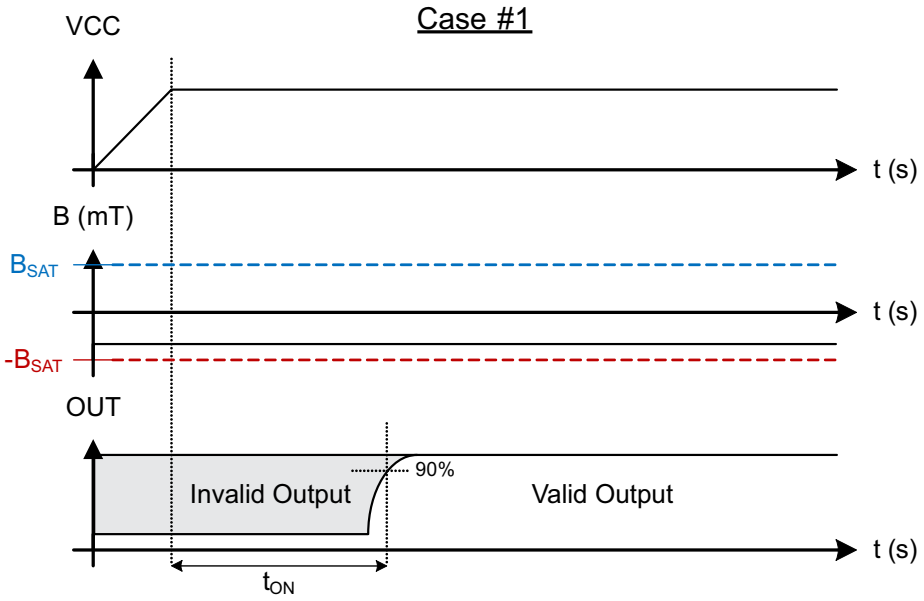


Figure 7-4. Case 1: Power On When B < 0, North

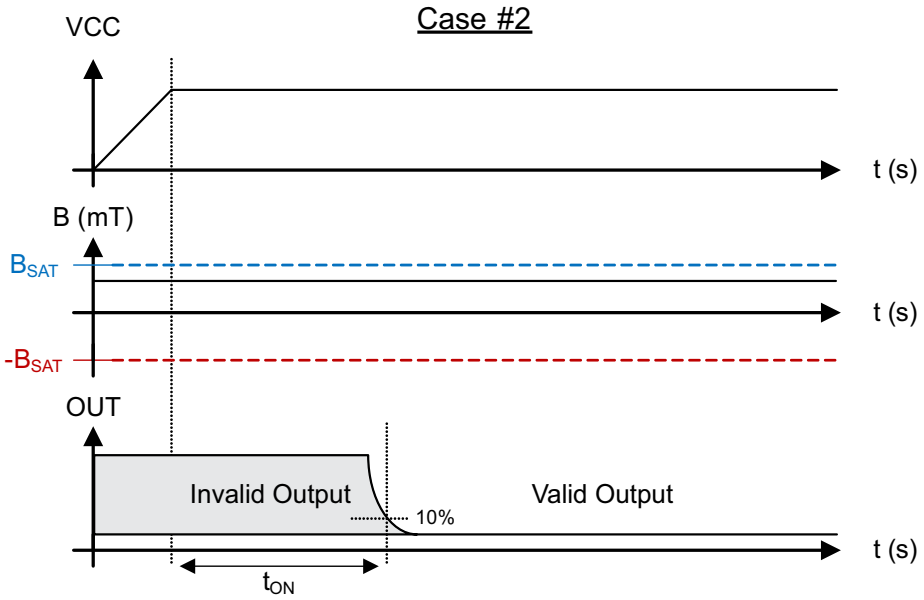


Figure 7-5. Case 2: Power On When B > 0, South

7.3.4 Output Stage

The DRV5053 output stage is capable of up to 300-µA of current source or 2.3-mA sink. For proper operation, ensure that equivalent output load R_{OUT} > 10 kΩ.

The capacitive load directly present on the OUT pin should be less than 10 nF to ensure the internal operational amplifier is stable. If an external RC filter is added to reduce noise, it is acceptable to use a resistor ≥ 200 Ω with a capacitor ≤ 0.1 µF. For an application example, see *Filtered Typical Application*.

7.3.5 Protection Circuits

An analog current limit circuit limits the current through the output driver. The driver current will be clamped to I_{OCP}.

7.3.5.1 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP}. During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

7.3.5.2 Load Dump Protection

The DRV5053 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand V_{CC} = 40 V. No current-limiting series resistor is required for this protection.

7.3.5.3 Reverse Supply Protection

The DRV5053 device is protected in the event that the V_{CC} pin and the GND pin are reversed (up to –22 V).

Note

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the *Absolute Maximum Ratings*.

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	$I_{SINK} \geq I_{OCP}$	Operating	Output current is clamped to I_{OCP}	$I_O < I_{OCP}$
Load Dump	38 V < V_{CC} < 40 V	Operating	Device will operate for a transient duration	$V_{CC} \leq$ 38 V
Reverse Supply	–22 V < V_{CC} < 0 V	Disabled	Device will survive this condition	$V_{CC} \geq$ 2.5 V

7.4 Device Functional Modes

The DRV5053 device is active only when V_{CC} is between 2.5 V and 38 V.

When a reverse supply condition exists, the device is inactive.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DRV5053 device is used in magnetic-field sensing applications.

8.2 Typical Applications

8.2.1 Typical Application With No Filter

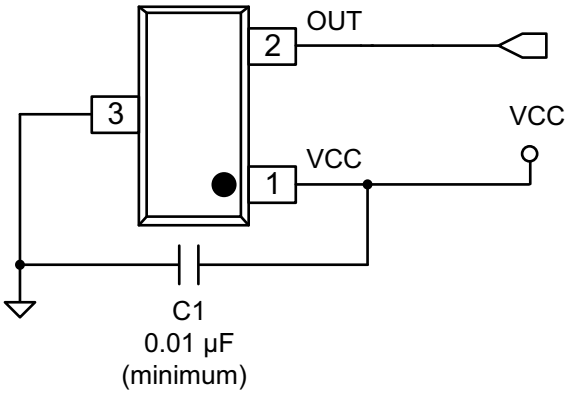


Figure 8-1. Typical Application Schematic – No Filter

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
System bandwidth	f_{BW}	15 kHz

8.2.1.2 Detailed Design Procedure

The DRV5053 has internal filtering that limits the bandwidth to at least 20 kHz. For this application no external components are required other than the C1 bypass capacitor, which is 0.01 µF minimum. If the analog output OUT is tied to a microcontroller ADC input, the equivalent load must be R > 10 kΩ and C < 10 nF.

Table 8-2. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01-µF (minimum) ceramic capacitor rated for V_{CC}

8.2.1.3 Application Curve

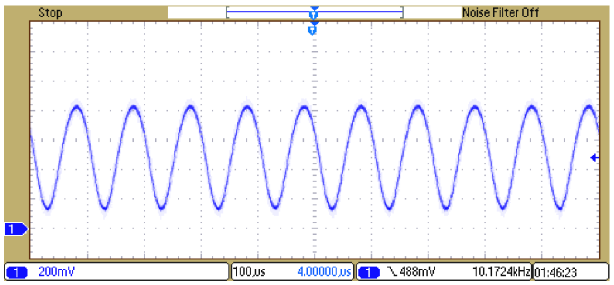


Figure 8-2. 10-kHz Switching Magnetic Field

8.2.2 Filtered Typical Application

For lower noise on the analog output OUT, additional RC filtering can be added to further reduce the bandwidth.

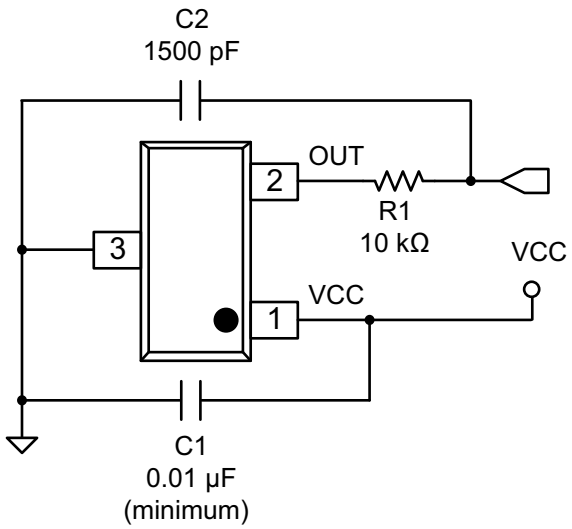


Figure 8-3. Filtered Typical Application Schematic

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-3 as the input parameters.

Table 8-3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
System bandwidth	f_{BW}	5 kHz

8.2.2.2 Detailed Design Procedure

In this example we will add an external RC filter in order to reduce the output bandwidth.

In order to preserve the signal at the frequencies of interest, we will conservatively select a low-pass filter bandwidth (–3-dB point) at twice the system bandwidth (10 kHz).

$$10\ \text{kHz} < \frac{1}{2\pi \times R_1 \times C_2} \tag{1}$$

If we guess R1 = 10 kΩ, then C2 < 1590 pF. So we select C2 = 1500 pF.

8.2.2.2.1 Typical Noise Versus Cutoff Frequency

RC filters are an effective way to reduce the noise present on OUT. The following shows typical noise measurements for different cutoff frequencies using the DRV5053VA.

Table 8-4. DRV5053VA Typical Noise Data

R (Ω)	C (µF)	f_{CUTOFF} (kHz)	NOISE (mVpp)
163	0.1	9.8	30.4
349	0.1	4.6	22.8
750	0.1	2.1	15.2
1505	0.1	1.1	9.7
3322	0.1	0.5	5.3
7510	0.1	0.2	2.5

8.2.2.3 Application Curves

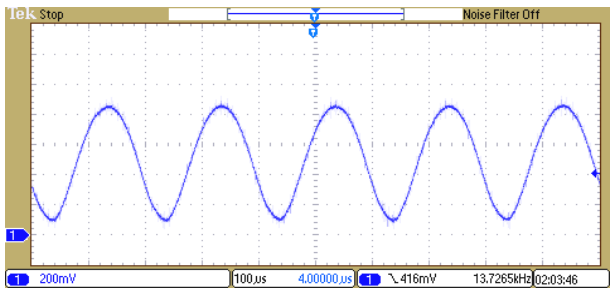
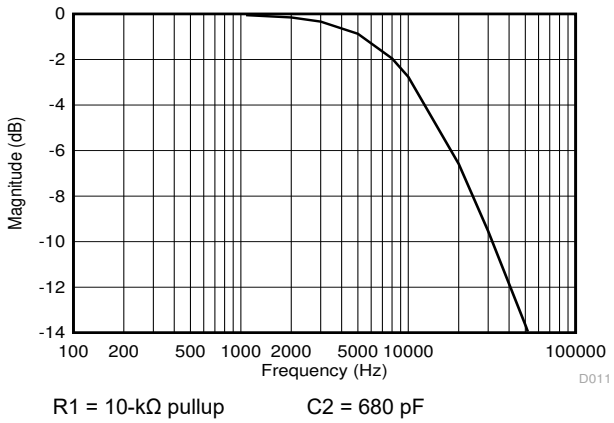


Figure 8-4. 5-kHz Switching Magnetic Field



R1 = 10-kΩ pullup C2 = 680 pF

Figure 8-5. Low-Pass Filtering

8.3 Power Supply Recommendations

The DRV5053 device is designed to operate from an input voltage supply (VM) range between 2.5 V and 38 V. A 0.01-µF (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5053 device as possible.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

Figure 9-1 shows a legend for reading the complete device name for the DRV5053 device.

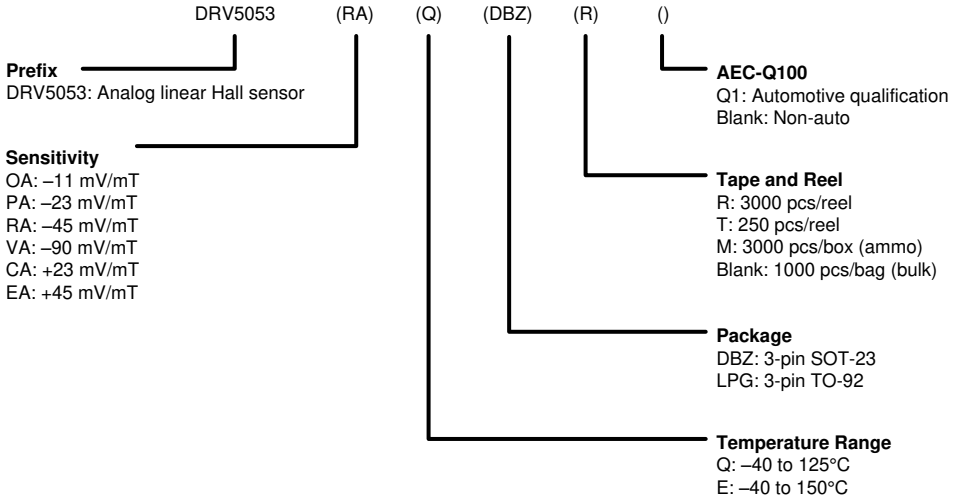


Figure 9-1. Device Nomenclature

9.1.2 Device Markings

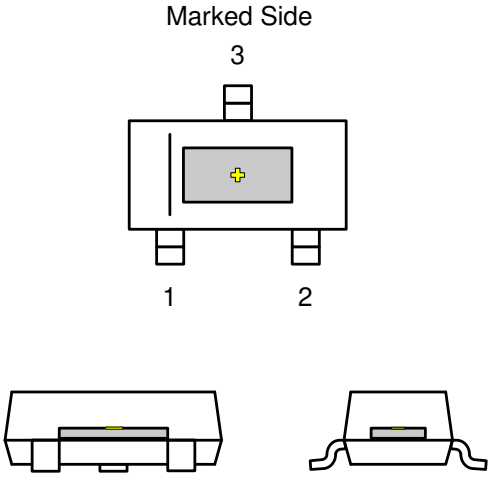


Figure 9-2. SOT-23 (DBZ) Package

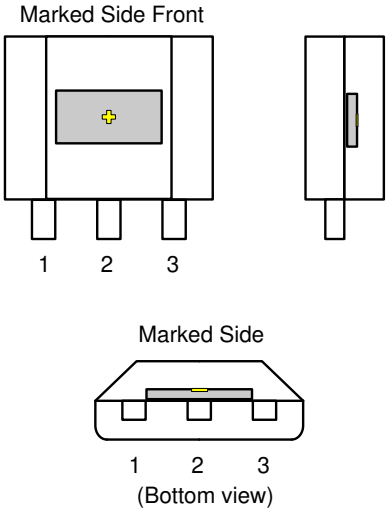


Figure 9-3. TO-92 (LPG) Package

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5053CAQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+ALCA, 1LX2)	Samples
DRV5053CAQDBZT	OBSOLETE	SOT-23	DBZ	3		TBD	Call TI	Call TI	-40 to 125	(+ALCA, 1LX2)	
DRV5053CAQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALCA	Samples
DRV5053CAQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALCA	Samples
DRV5053EAQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+ALEA, 1LZ2)	Samples
DRV5053EAQDBZT	OBSOLETE	SOT-23	DBZ	3		TBD	Call TI	Call TI	-40 to 125	(+ALEA, 1LZ2)	
DRV5053EAQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALEA	Samples
DRV5053EAQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALEA	Samples
DRV5053OAQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+ALOA, 1M12)	Samples
DRV5053OAQDBZT	OBSOLETE	SOT-23	DBZ	3		TBD	Call TI	Call TI	-40 to 125	(+ALOA, 1M12)	
DRV5053OAQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALOA	Samples
DRV5053OAQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALOA	Samples
DRV5053PAQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+ALPA, 1M22)	Samples
DRV5053PAQDBZT	OBSOLETE	SOT-23	DBZ	3		TBD	Call TI	Call TI	-40 to 125	(+ALPA, 1M22)	
DRV5053PAQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALPA	Samples
DRV5053PAQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALPA	Samples
DRV5053RAQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+ALRA, 1M32)	Samples
DRV5053RAQDBZT	OBSOLETE	SOT-23	DBZ	3		TBD	Call TI	Call TI	-40 to 125	(+ALRA, 1M32)	
DRV5053RAQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALRA	Samples
DRV5053RAQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALRA	Samples
DRV5053VAQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(+ALVA, 1M42)	Samples
DRV5053VAQDBZT	OBSOLETE	SOT-23	DBZ	3		TBD	Call TI	Call TI	-40 to 125	(+ALVA, 1M42)	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5053VAQLPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALVA	Samples
DRV5053VAQLPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+ALVA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF DRV5053 :

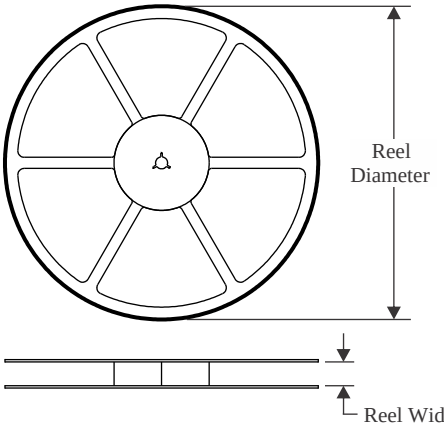
- Automotive : DRV5053-Q1

NOTE: Qualified Version Definitions:

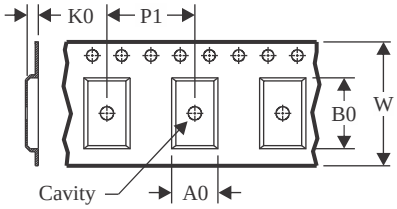
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

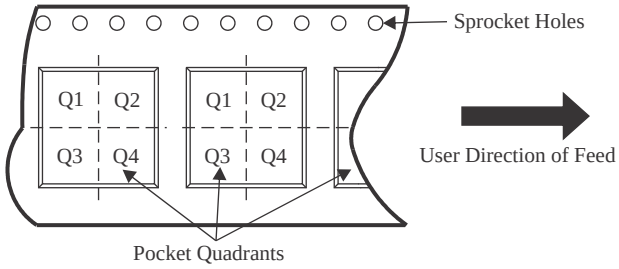


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

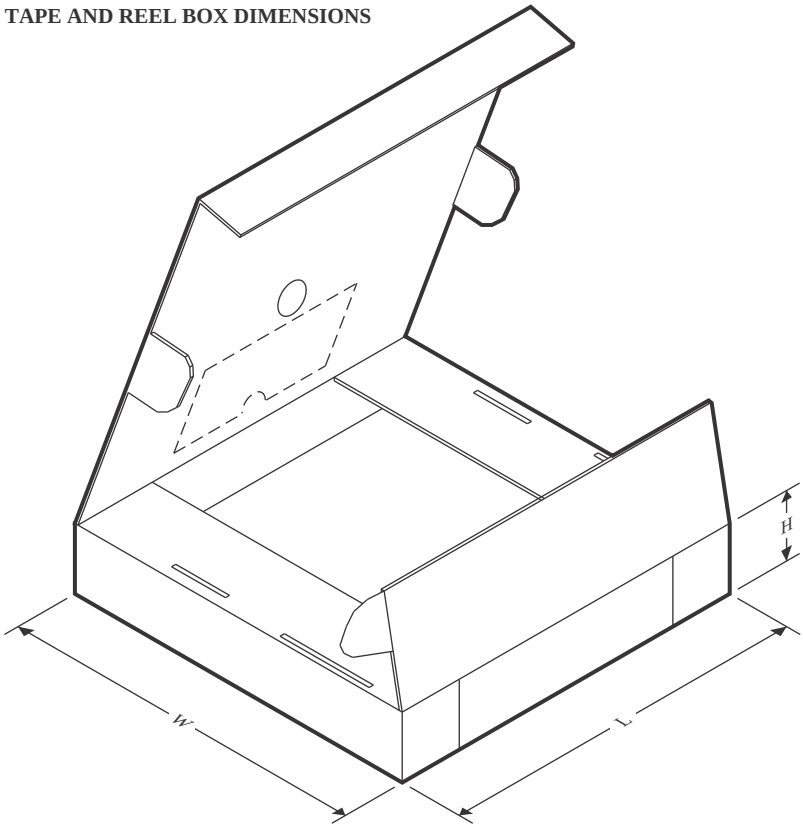
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5053CAQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
DRV5053CAQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053CAQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053EAQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053EAQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053OAQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053PAQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053RAQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053RAQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053VAQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053VAQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

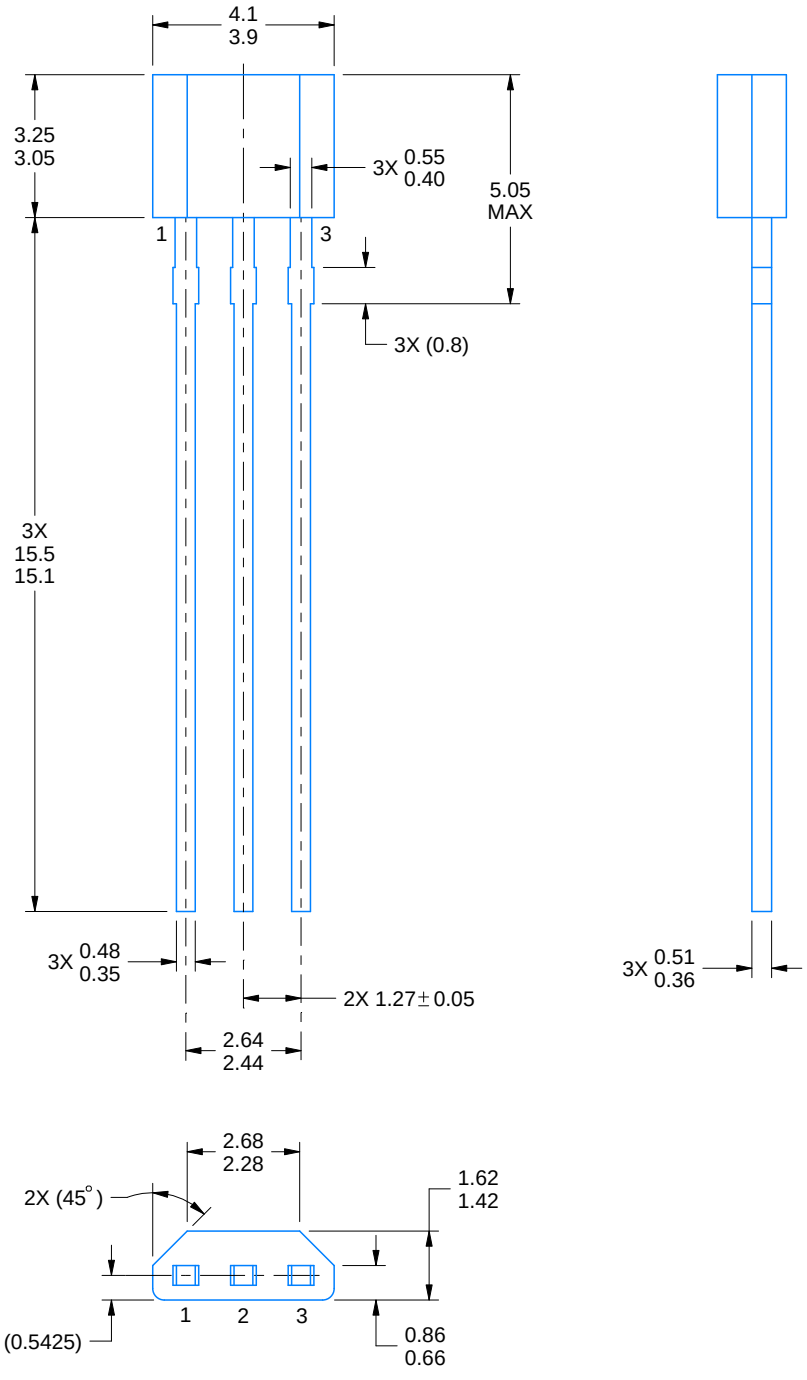
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5053CAQDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
DRV5053CAQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053CAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5053EAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5053EAQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053OAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5053PAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5053RAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
DRV5053RAQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053VAQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053VAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0

PACKAGE OUTLINE

LPG0003A

TO-92 - 5.05 mm max height

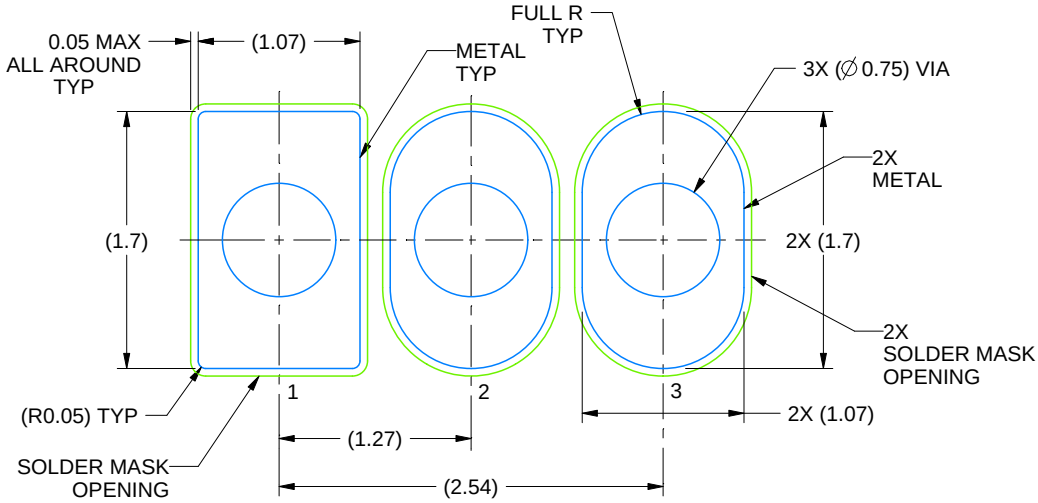
TRANSISTOR OUTLINE



4221343/C 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

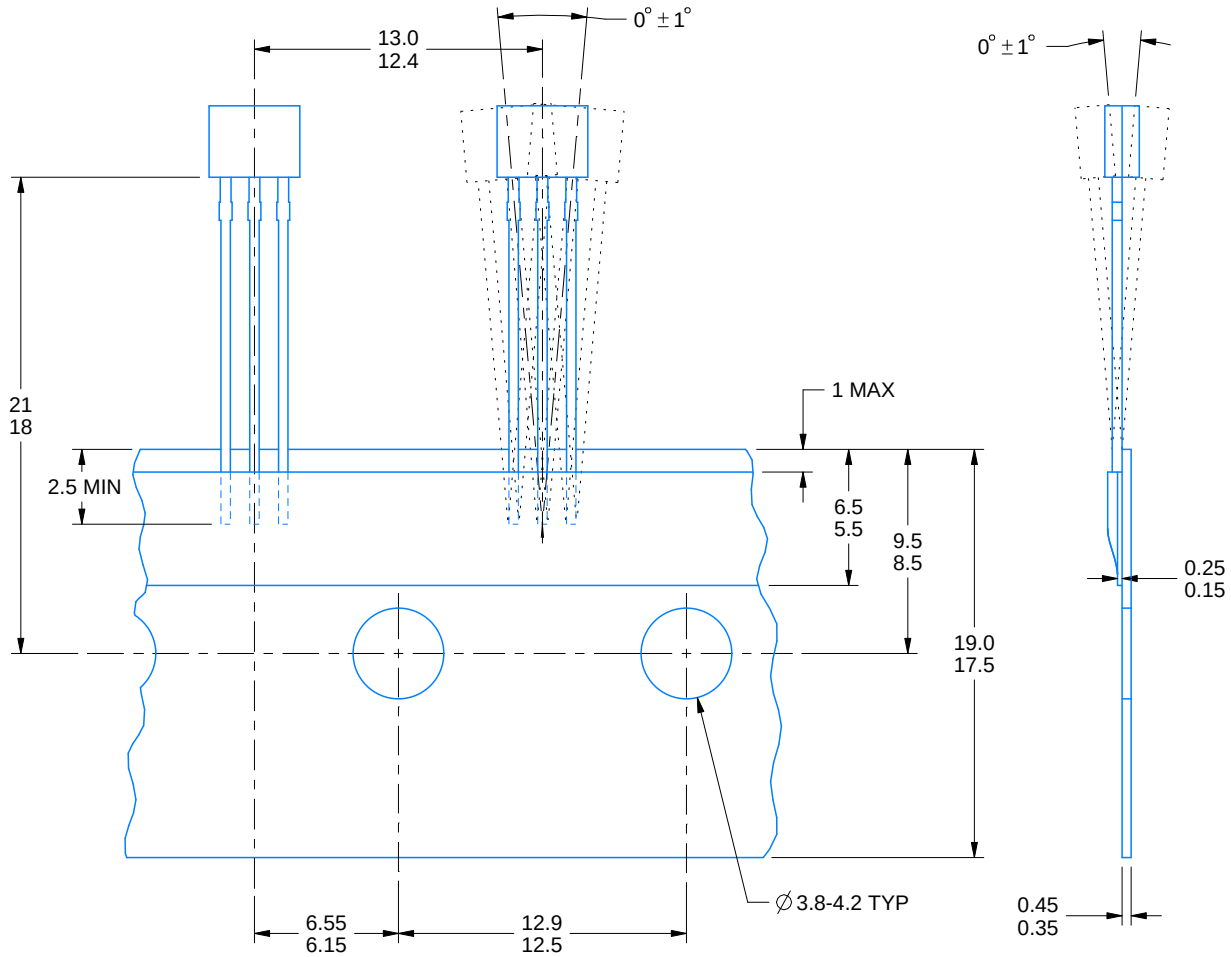
4221343/C 01/2018

TAPE SPECIFICATIONS

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



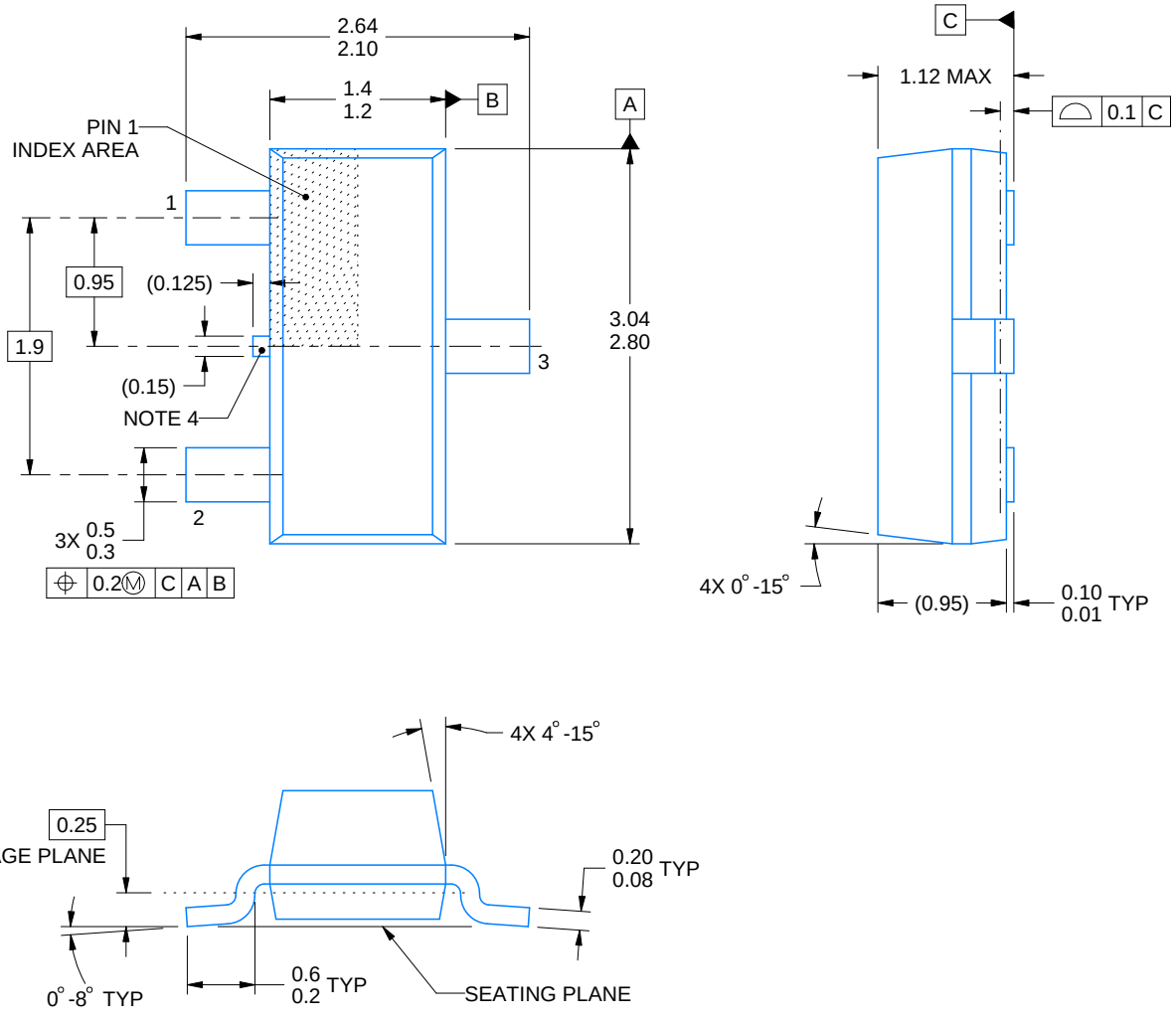
4221343/C 01/2018

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

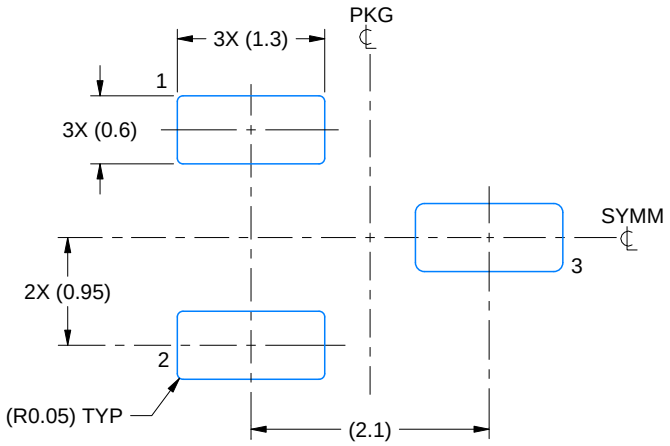
SMALL OUTLINE TRANSISTOR



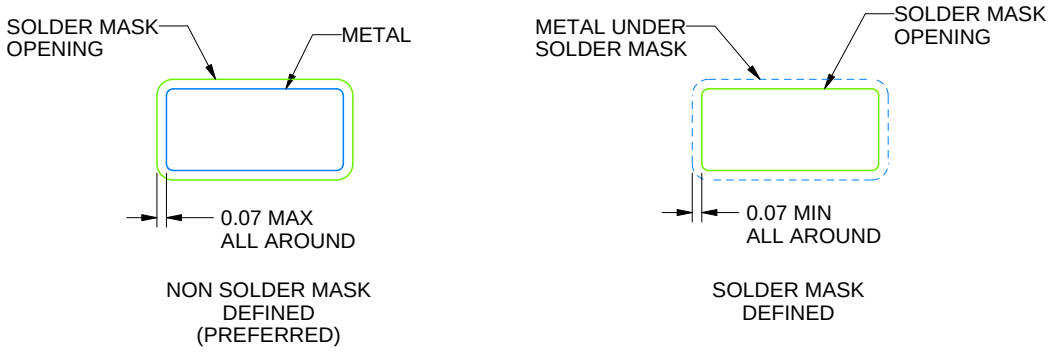
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

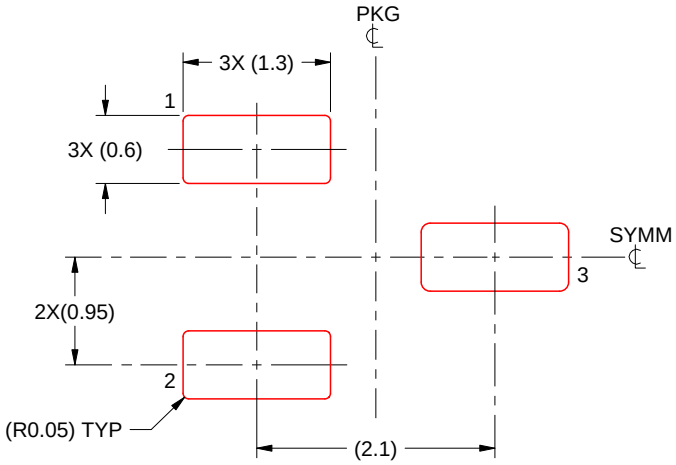


SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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