

# ESD752 and ESD762 24-V, 2-Channel, ESD Protection With 5.7 A of 8/20 $\mu$ s Surge Protection in a SOT-23 and SOT-323 / SC-70 Package

## 1 Features

- Robust surge protection:
  - IEC 61000-4-5 (8/20  $\mu$ s): 5.7 A or 2.5 A
- IEC 61000-4-2 level 4 ESD protection:
  - $\pm$ 30-kV or  $\pm$ 20-kV contact discharge
  - $\pm$ 30-kV or  $\pm$ 20-kV air-gap discharge
- 24 V working voltage
- Bidirectional ESD protection
- 2-channel device provides complete ESD and surge protection with single component
- Low clamping voltage protects downstream components
- I/O capacitance = 3 pF or 1.7 pF (typical)
- SOT-23 (DBZ) small, standard, common footprint
- SOT-323 / SC-70 (DCK) very small, standard, space saving, common footprint
- Leaded packages used for automatic optical inspection (AOI)

## 2 Applications

- USB power delivery (USB-PD):
  - VBUS protection
  - IO protection (withstand short to VBUS)
- Industrial control networks:
  - Smart distribution system (SDS)
  - DeviceNet IEC 62026-3
  - CANopen – CiA 301/302-2 and EN 50325-4
  - 4/20 mA circuits
  - PLC surge protection
  - ADC surge protection

## 3 Description

The ESD752 and ESD762 are bidirectional ESD protection diodes for USB power delivery (USB-PD) and industrial interfaces. The ESD752 and ESD762 are rated to dissipate contact ESD that meets or exceeds the maximum level specified in the IEC 61000-4-2 level 4 standard ( $\pm$ 30-kV or  $\pm$ 20-kV contact and  $\pm$ 30-kV or  $\pm$ 20-kV airgap). The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key because industrial systems require a high level of robustness and reliability.

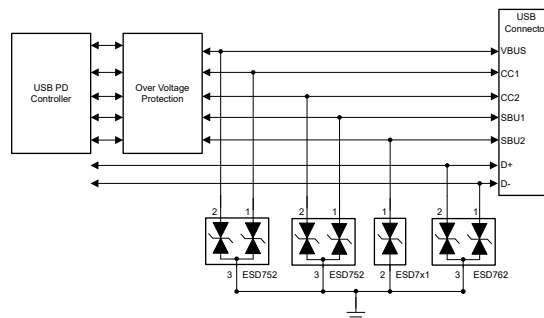
These devices feature a low IO capacitance per channel and a pin-out to suit two IO lines from damage caused by electrostatic discharge (ESD) and other transients. The  $I_{PP} = 5.7$  A (8/20  $\mu$ s surge waveform) capability of the ESD752 makes it suitable for protecting USB VBUS against transient surge events as well as industrial I/O lines. Additionally, the 3 pF or 1.7 pF line capacitance of the ESD752 and ESD762 are suitable for protecting the slower speed signals for USB power delivery and IO signals for industrial applications.

The ESD752 and ESD762 are offered in two leaded packages for easy flow through routing.

### Package Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ESD752	DCK (SOT-323 / SC-70, 3)	2.00 mm $\times$ 1.25 mm
	DBZ (SOT-23, 3)	2.92 mm $\times$ 1.30 mm
ESD762	DBZ (SOT-23, 3)	2.92 mm $\times$ 1.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



USB Power Delivery Application

### USB Power Delivery Typical Application



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## 4 Revision History

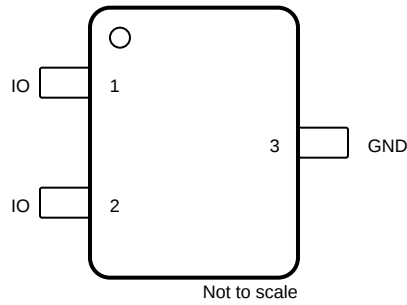
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (August 2022) to Revision B (November 2022)</b>	<b>Page</b>
• Added ESD762 Specifications to the data sheet.....	1
• Added the <i>Application Curves</i> section.....	11

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<b>Changes from Revision * (May 2022) to Revision A (August 2022)</b>	<b>Page</b>
• Changed the status of the data sheet from: <i>Advanced Information</i> to: <i>Production Data</i> .....	1

## 5 Pin Configuration and Functions



**Figure 5-1. DCK and DBZ Package,  
3-Pin SOT-323 / SC-70 and SOT-23  
(Top View)**

**Table 5-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER		DEVICE	MIN	MAX	UNIT
P <sub>pp</sub>	IEC 61000-4-5 Power (t <sub>p</sub> – 8/20 μs) at 25°C	ESD752		210	W
	IEC 61000-4-5 Power (t <sub>p</sub> – 8/20 μs) at 25°C	ESD762		90	W
I <sub>pp</sub>	IEC 61000-4-5 current (t <sub>p</sub> – 8/20 μs) at 25°C	ESD752		5.7	A
	IEC 61000-4-5 current (t <sub>p</sub> – 8/20 μs) at 25°C	ESD762		2.5	A
T <sub>A</sub>	Operating free-air temperature		-55	150	°C
T <sub>J</sub>	Junction temperature		-55	150	°C
T <sub>stg</sub>	Storage temperature		-65	155	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings—JEDEC Specification

PARAMETER		TEST CONDITION	VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002 <sup>(2)</sup>	± 1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings—IEC Specification

over T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	DEVICE	VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD752	±30000	V
			ESD762	±20000	V
		IEC 61000-4-2 Air Discharge, all pins	ESD752	±30000	V
			ESD762	±20000	V

### 6.4 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage	-24		24	V
T <sub>A</sub>	Operating free-air temperature	-55		150	°C

### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ESD752		ESD762	UNIT
		DBZ (SOT-23)	DCK (SOT-323 / SC-70)	DBZ (SOT-23)	
		3 PINS	3 PINS	3 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	291.5	283.0	325.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	147.1	164.1	178.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	131.1	105.1	165.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	32.0	67.1	52.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	130.2	104.4	164.4	°C/W

## 6.5 Thermal Information (continued)

THERMAL METRIC <sup>(1)</sup>		ESD752		ESD762	UNIT
		DBZ (SOT-23)	DCK (SOT-323 / SC-70)	DBZ (SOT-23)	
		3 PINS	3 PINS	3 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

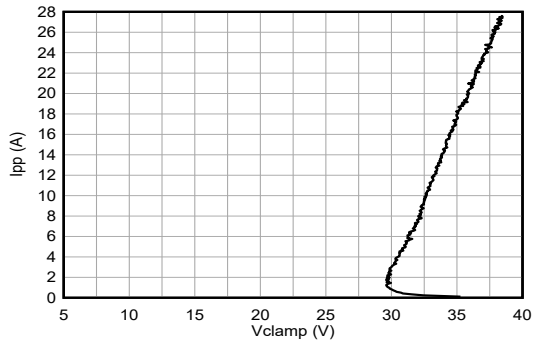
## 6.6 Electrical Characteristics

over  $T_A = 25^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
$V_{RWM}$	Reverse stand-off voltage			-24		24	V
$V_{BRF}$	Forward breakdown voltage <sup>(2)</sup>	$I_{IO} = 10\text{ mA}$ , IO to GND		25.5		35.5	V
$V_{BRR}$	Reverse breakdown voltage <sup>(2)</sup>	$I_{IO} = -10\text{ mA}$ , IO to GND		-35.5		-25.5	V
$V_{CLAMP}$	Clamping voltage <sup>(3)</sup>	$I_{PP} = 5.7\text{ A}$ , $t_p = 8/20\ \mu\text{s}$ , IO to GND	ESD752		37		V
		$I_{PP} = 2.5\text{ A}$ , $t_p = 8/20\ \mu\text{s}$ , from IO to GND	ESD762		36		V
$V_{CLAMP}$	Clamping voltage <sup>(4)</sup>	$I_{PP} = 16\text{ A}$ , TLP, IO to GND or GND to IO	ESD752		35		V
			ESD762		38		V
$V_{Hold}$	Holding voltage after snapback <sup>(5)</sup>	TLP	ESD752		30		V
			ESD762		30		V
$I_{LEAK}$	Leakage current	$V_{IO} = \pm 24\text{ V}$ , IO to GND		-50	5	50	nA
$R_{DYN}$	Dynamic resistance <sup>(4)</sup>	IO to GND and GND to IO	ESD752		0.35		$\Omega$
			ESD762		0.57		$\Omega$
$C_L$	Line capacitance <sup>(6)</sup>	$V_{IO} = 0\text{ V}$ , $f = 1\text{ MHz}$ , $V_{pp} = 30\text{ mV}$	ESD752		3	5	pF
			ESD762		1.7	2.8	pF

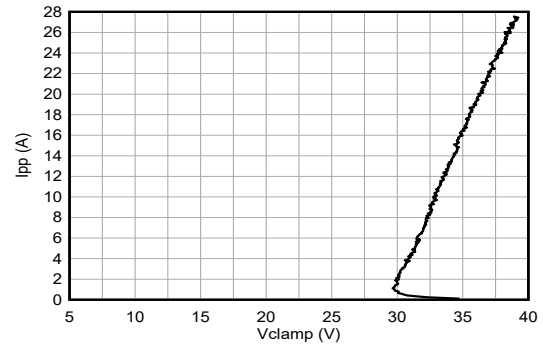
- (1) Measurements made on each IO channel.  
(2)  $V_{BRF}$  and  $V_{BRR}$  are defined as the voltage when +/- 10 mA is applied in the positive or negative direction respectively, before the device latches into the snapback state.  
(3) Device stressed with 8/20  $\mu\text{s}$  exponential decay waveform according to IEC 61000-4-5.  
(4) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008  
(5)  $V_{HOLD}$  is defined as the lowest voltage on the TLP plot once the trigger threshold is reached and the device snapbacks and begins clamping the voltage.  
(6) Measured from IO to GND on each channel.

## 6.7 Typical Characteristics – ESD752



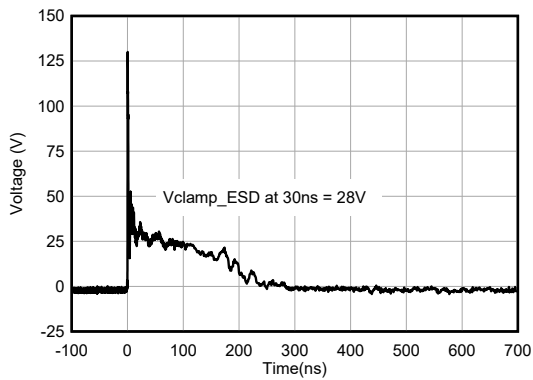
tp = 100 ns, Transmission Line Pulse (TLP)

**Figure 6-1. Positive TLP Curve**

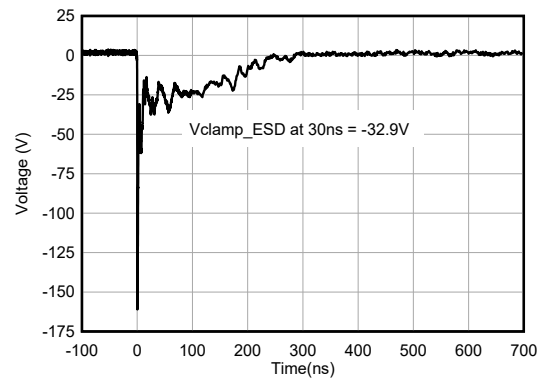


tp = 100 ns, Transmission Line Pulse (TLP)

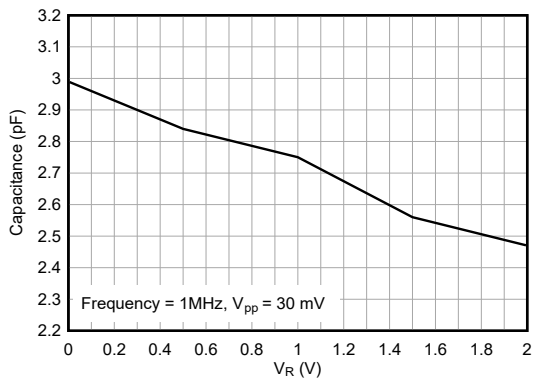
**Figure 6-2. Negative TLP Curve**



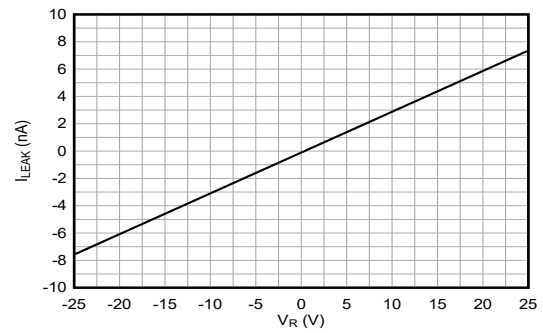
**Figure 6-3. +8-kV Clamped IEC Waveform**



**Figure 6-4. -8-kV Clamped IEC Waveform**



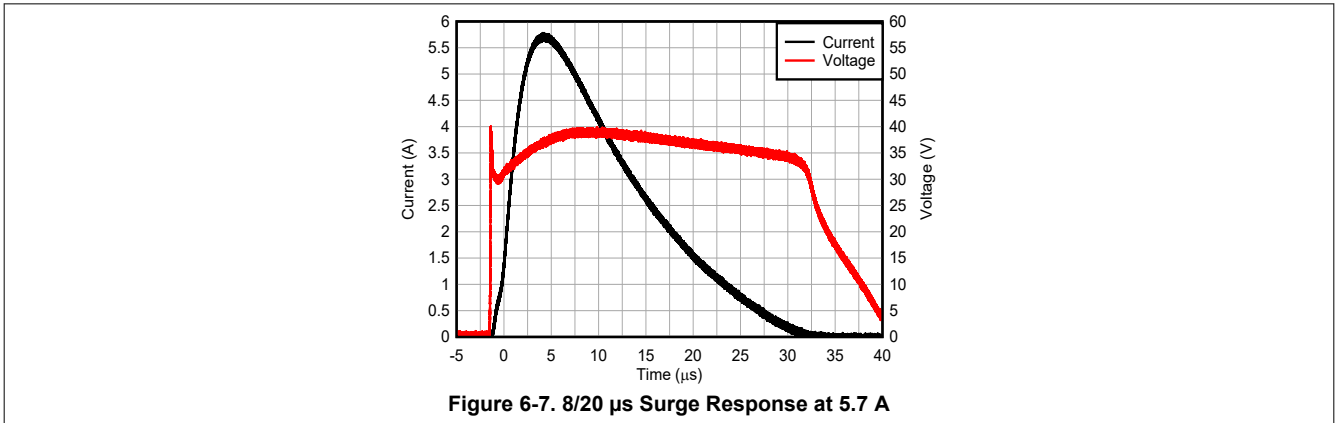
**Figure 6-5. Capacitance vs. Bias Voltage**



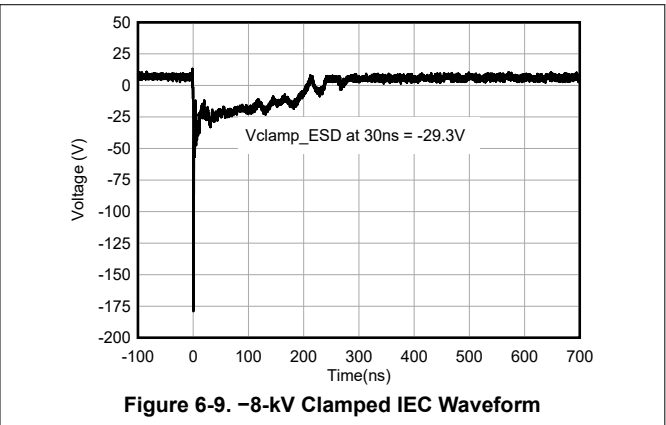
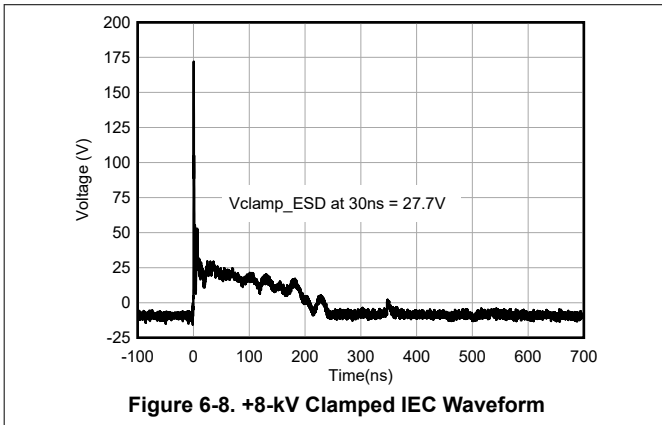
TA = 150 °C  
ILEAK is less than 1 nA at -55 °C and 25 °C.

**Figure 6-6. Leakage Current vs. Bias Voltage Across Temperature**

### 6.7 Typical Characteristics – ESD752 (continued)



### 6.8 Typical Characteristics – ESD762



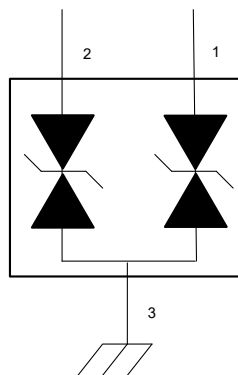
## 7 Detailed Description

### 7.1 Overview

The ESD752 and ESD762 are dual-channel ESD TVS diodes in SOT-23 and SOT-323 (SC-70) leaded packages which are convenient for automatic optical inspection. This product offers IEC 61000-4-2  $\pm 30$ -kV or  $\pm 20$ -kV air-gap,  $\pm 30$ -kV or  $\pm 20$ -kV contact ESD protection respectively, and has a clamp circuit with a back-to-back TVS diode for bidirectional signal support.

A typical application of this product is the ESD protection for USB-PD slower speed signals (CC1, CC2, SBU1, SBU2, D+, and D-). The  $I_{PP} = 5.7$  A (8/20  $\mu$ s surge waveform) capability of the ESD752 makes it suitable for protecting VBUS. The ESD752 device is also a good fit for protecting industrial IOs requiring 5.7 A or less of surge current protection. The 3 pF or 1.7 pF line capacitance of these ESD protection diodes are suitable for USB-PD slower speed signals and industrial IO applications.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The ESD752 and ESD762 are bidirectional TVS diodes with a high ESD protection level. This device protects the circuit from ESD strikes up to  $\pm 30$ -kV or  $\pm 20$ -kV contact and  $\pm 30$ -kV or  $\pm 20$ -kV air-gap respectively as specified in the IEC 61000-4-2 standard. The ESD752 and ESD762 can also handle up to 5.7 A or 2.5 A of surge current (IEC 61000-4-5 8/20  $\mu$ s) respectively. The I/O capacitance of 3 pF or 1.7 pF (typical) are suitable for USB power delivery slower speed signals and industrial applications. These clamping devices have a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits.

For example, the ESD752 clamping voltage is only 37 V when the device is taking 5.7 A transient current. The breakdown is bidirectional so these protection devices are a good fit for applications requiring positive and negative polarity protection. Low leakage allows these diodes to conserve power when working below the  $V_{RWM}$ . The temperature range of  $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$  makes this ESD device work at extensive temperatures in most environments. The leaded SOT-23 and SOT-323 (SC-70) packages are good for applications requiring automatic optical inspection (AOI).

#### 7.3.1 Temperature Range

These devices are qualified to operate from  $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ .

#### 7.3.2 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 5.7 A and 2.5 A (8/20  $\mu$ s waveform) for the ESD752 and ESD762 respectively. An ESD-surge clamp diverts this current to ground.

#### 7.3.3 IO Capacitance

The capacitance between the I/O pins is 3 pF and 1.7 pF for the ESD752 and ESD762 respectively. These capacitances are suitable for USB power delivery slower speed signals and industrial applications.



### 7.3.4 Dynamic Resistance

The IO pins feature an ESD clamp that has a low  $R_{DYN}$  of 0.35  $\Omega$  for the ESD752 device, and 0.57  $\Omega$  for the ESD762 device, which prevents system damage during ESD events.

### 7.3.5 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of  $\pm 25.5$  V. This protects sensitive equipment is protected from surges above the reverse standoff voltage of  $\pm 24$  V.

### 7.3.6 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of 50 nA (maximum) with a bias of  $\pm 24$  V.

### 7.3.7 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 37 V ( $I_{PP} = 5.7$  A for 8/20  $\mu$ s surge waveform), 35 V ( $I_{PP} = 16$  A for TLP), 36 V ( $I_{PP} = 2.5$  A for 8/20  $\mu$ s surge waveform), and 38 V ( $I_{PP} = 16$  A for TLP) for the ESD752 and ESD762, respectively.

### 7.3.8 Industry Standard Leaded Packages

These devices feature industry standard SOT-23 (DBZ) and SC-70 (DCK) leaded packages for automatic optical inspection (AOI).

## 7.4 Device Functional Modes

The ESD752 and ESD762 are dual channel passive clamp devices that have low leakage during normal operation when the voltage between IO and GND is below  $V_{RWM}$ , and activate when the voltage between IO and GND goes above  $V_{BR}$ . During IEC 61000-4-2 ESD events, transient voltages as high as  $\pm 30$  kV can be clamped on either channel. When the voltages on the protected lines fall below the  $V_{HOLD}$ , the device reverts back to the low leakage passive state.

## 8 Application and Implementation

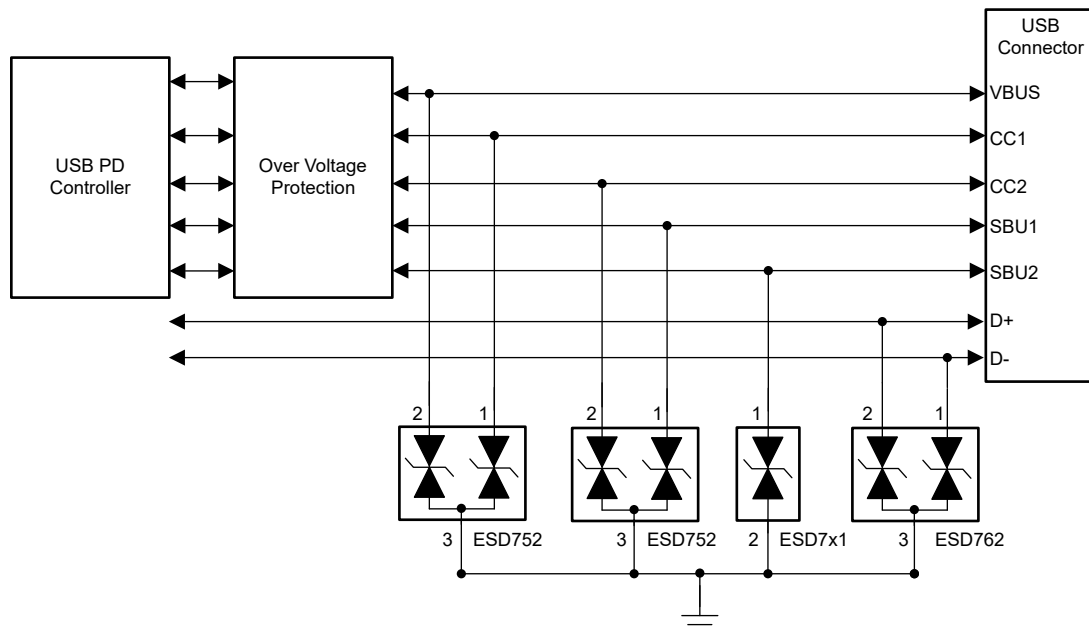
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The ESD752 and ESD762 are dual channel TVS diodes which are used to provide a path to ground for dissipating ESD events on USB-PD or industrial IO signal lines. As the current from the ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage ( $V_{CLAMP}$ ) to a safe level for the protected IC.

### 8.2 Typical Application



USB Power Delivery Application

Figure 8-1. USB Power Delivery Typical Application

#### 8.2.1 Design Requirements

For this design example, the ESD752 and ESD762 are used to provide ESD protection on a USB-PD connector. [Table 8-1](#) lists the known design parameters for this application.

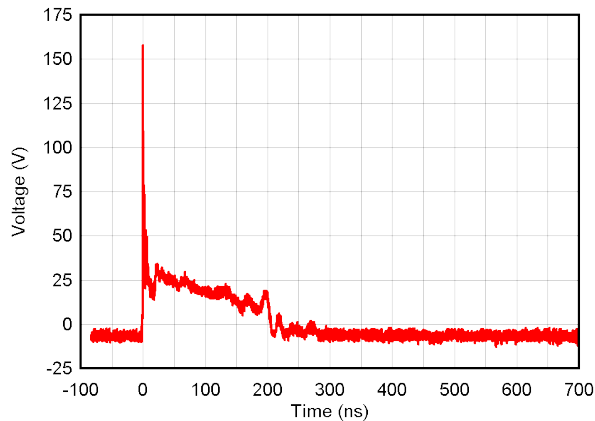
Table 8-1. Design Parameters for the USB Power Delivery Typical Application

Design Parameter	Value
Diode configuration	Bidirectional
VBUS Voltage	+ 20 V
$V_{IO}$ signal range	+ 3.3 V
$V_{RWM}$	± 24 V
Short to VBUS event on $V_{IO}$	± 20 V
Data rate	Up to 480 Mbps

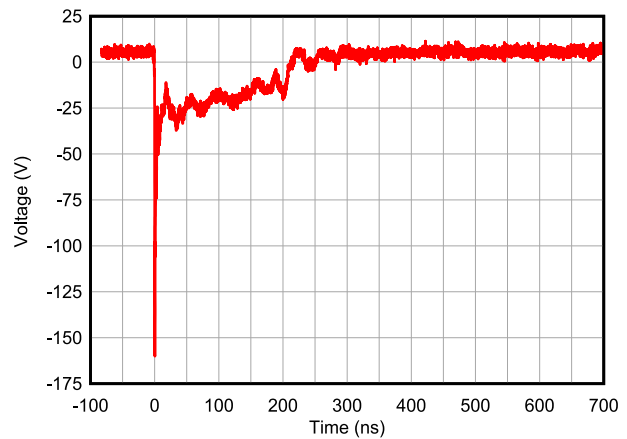
### 8.2.2 Detailed Design Procedure

The ESD752 and ESD762 has a  $V_{RWM}$  of  $\pm 24$  V to prevent the diode from being damaged during a short event that can occur when one of the USB-PD slower speed lines (CC1, CC2, SBU1, SBU2, D+, and D-) is shorted to VBUS. The bidirectional characteristic protects both positive and negative polarity. The low 1.7 pF capacitance of the ESD762 device enables data rates up to 480 Mbps, which allows the designer to meet the requirements for the D+ and D- signals. The ESD752 has an  $I_{PP} = 5.7$  A (8/20  $\mu$ s) surge current capability making it suitable for protecting the VBUS power rail.

### 8.2.3 Application Curves



**Figure 8-2. +8-kV Clamped IEC Waveform**



**Figure 8-3. -8-kV Clamped IEC Waveform**

## 9 Power Supply Recommendations

These are passive TVS diode-based ESD protection devices; therefore, there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.

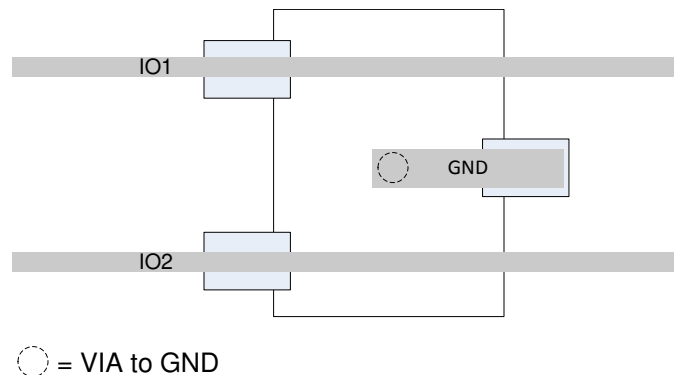
## 10 Layout

### 10.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 3 is connected to ground, use a thick and short trace for this return path.

### 10.2 Layout Example

This is a typical example of a dual channel IO routing.



**Figure 10-1. Routing with DBZ and DCK Package**

## 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [ESD Layout Guide user's guide](#)
- Texas Instruments, [ESD and Surge Protection for USB Interfaces application note](#)
- Texas Instruments, [ESD Protection Diodes EVM user's guide](#)
- Texas Instruments, [Generic ESD Evaluation Module user's guide](#)
- Texas Instruments, [Reading and Understanding an ESD Protection data sheet](#)

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD752DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RP8	<a href="#">Samples</a>
ESD752DCKR	ACTIVE	SC70	DCK	3	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 150	1MP	<a href="#">Samples</a>
ESD762DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RK8	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD752DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD752DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
ESD762DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

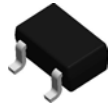


**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD752DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD752DCKR	SC70	DCK	3	3000	180.0	180.0	18.0
ESD762DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0

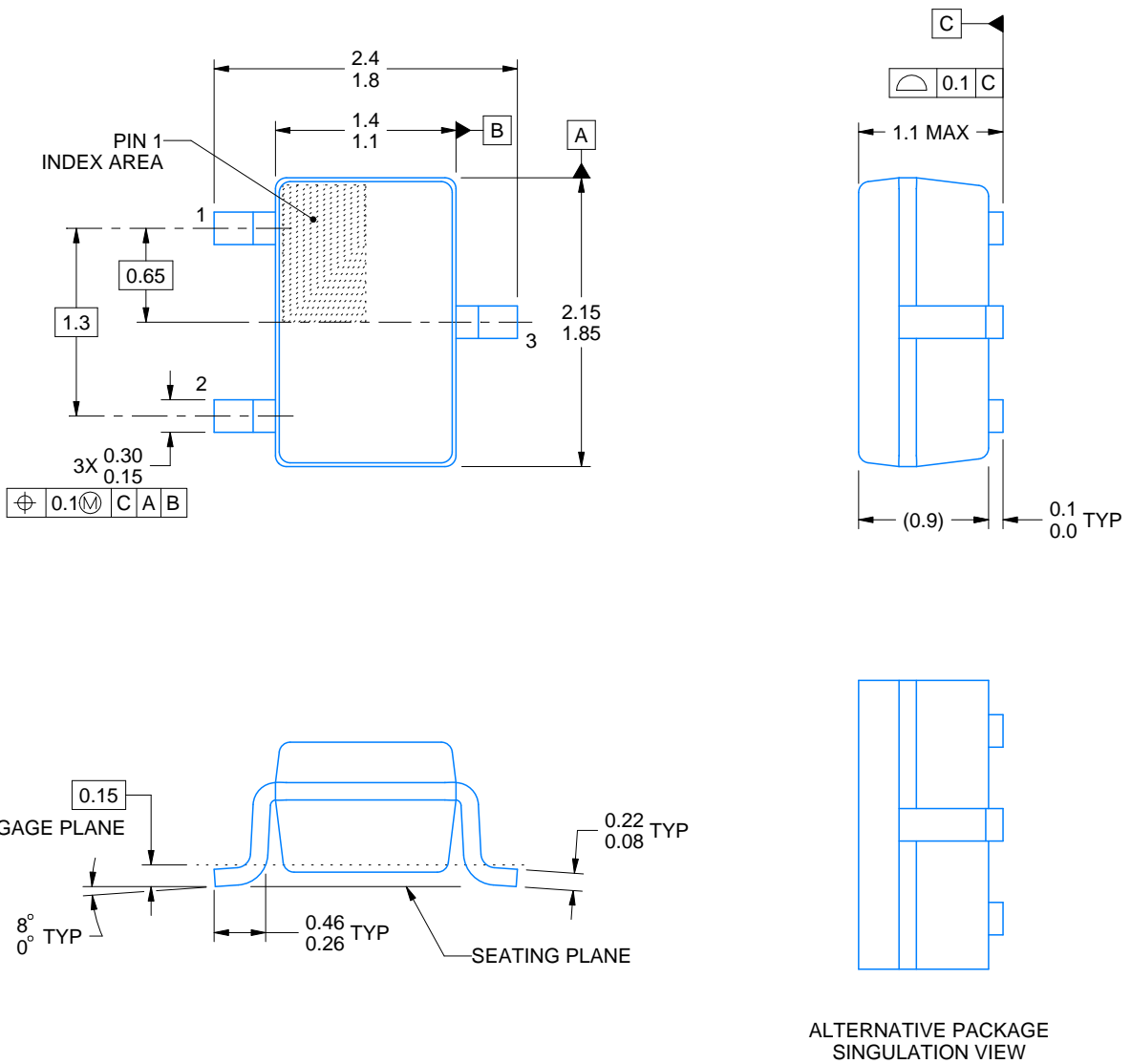
DCK0003A



# PACKAGE OUTLINE

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



4220745/D 06/2024

NOTES:

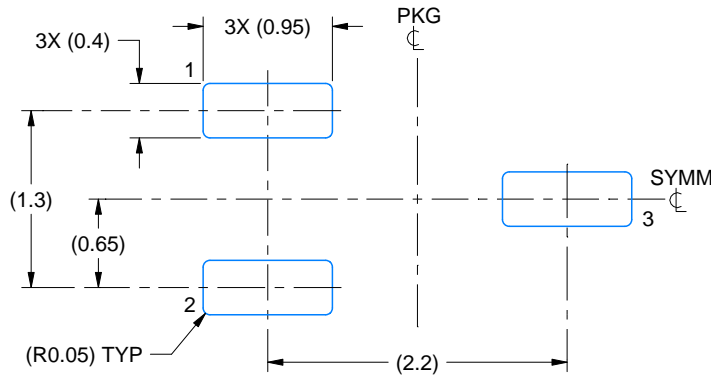
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

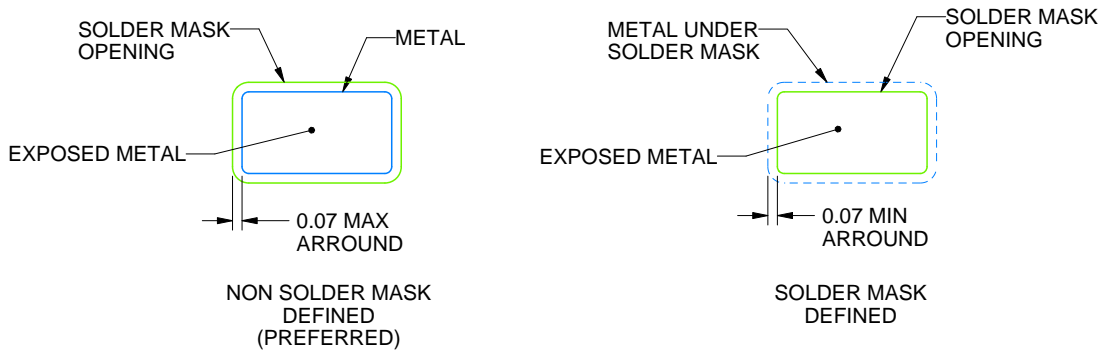
DCK0003A

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

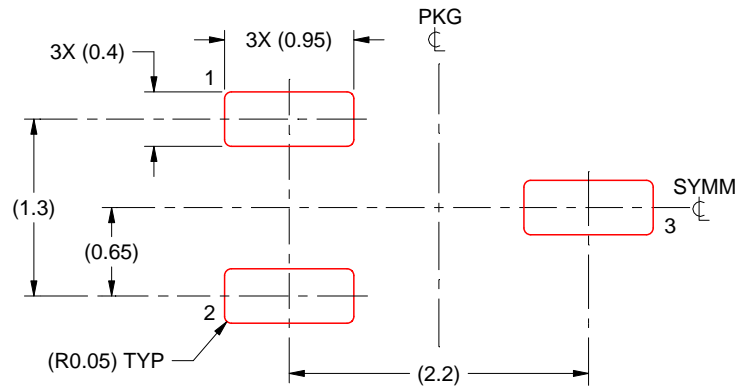
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0003A

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

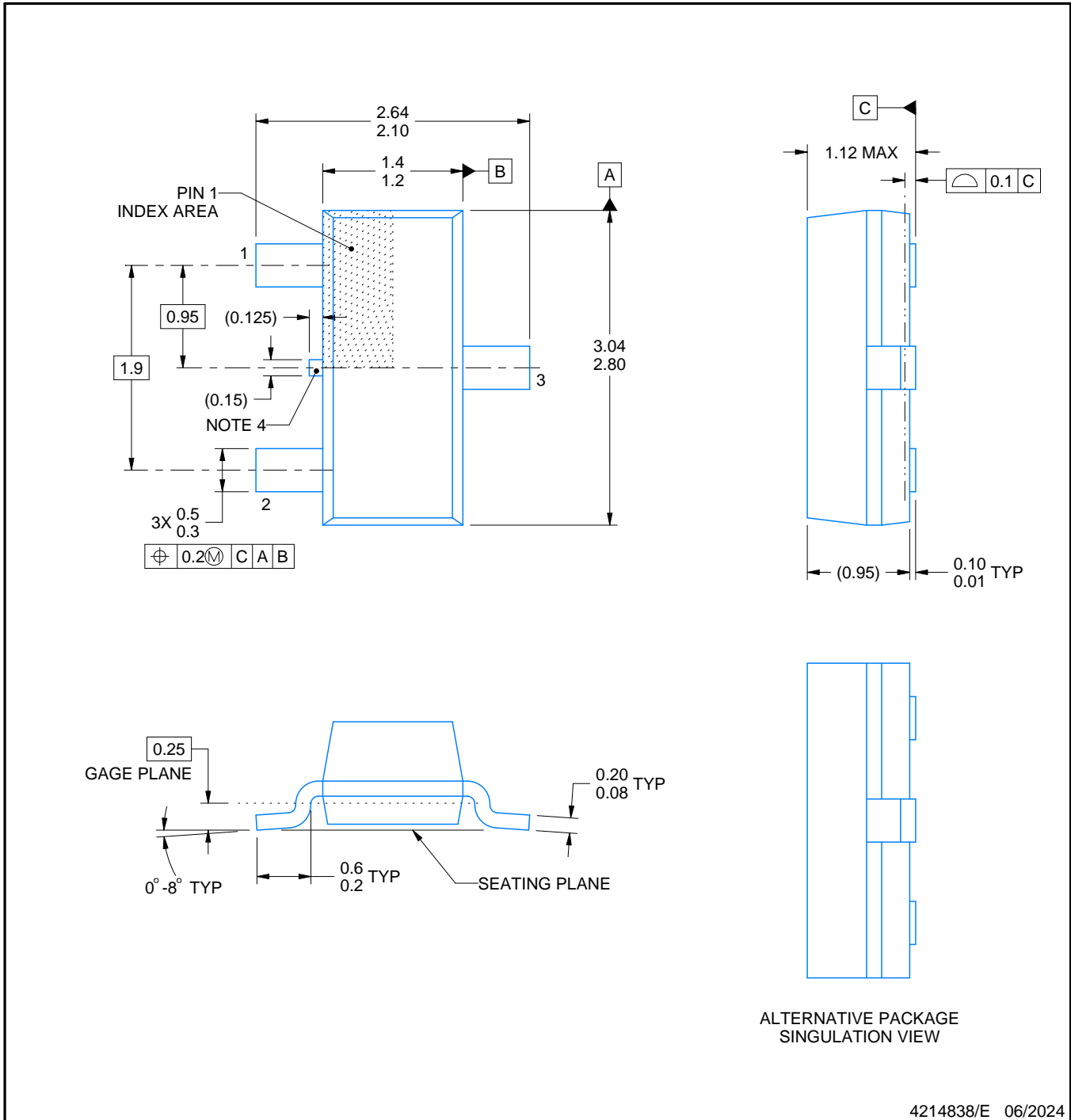
# DBZ0003A



# PACKAGE OUTLINE

## SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



4214838/E 06/2024

### NOTES:

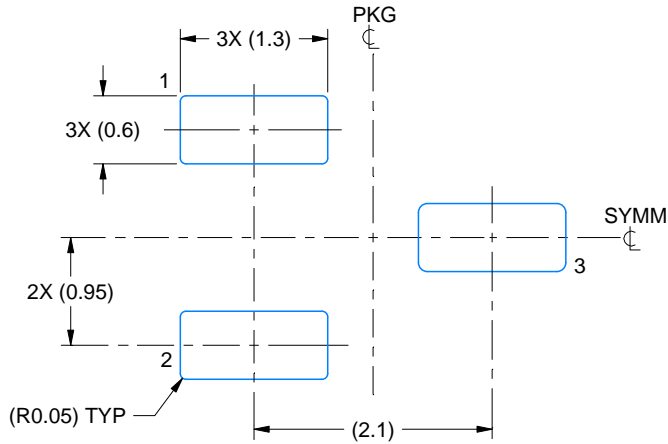
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

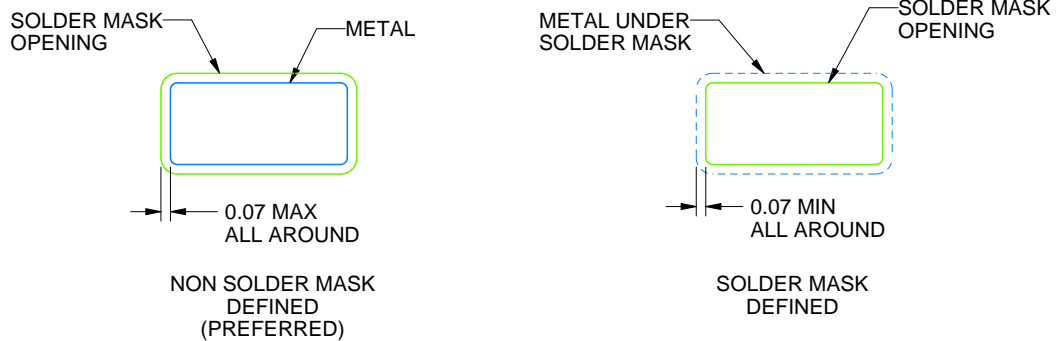
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

4214838/E 06/2024

NOTES: (continued)

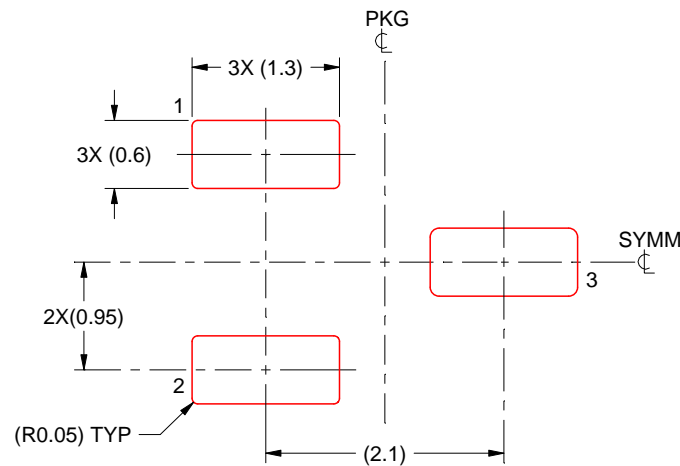
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214838/E 06/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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