

# Functionally Isolated Normally Open Opto-emulator Switch With Integrated FETs

## 1 Features

- Drop-in replacement and pin-to-pin upgrade to industry-standard photorelays
- Single-channel, diode-emulator input
- Single-pole, normally-open, symmetrical 80V output switch
- Primary-side current controlled switch, no additional isolated high voltage supply required for 80V switching
- Ultra-low off-state leakage at  $V_{OFF} = 70V$ 
  - $< 250nA$  at operating temperature of  $25^{\circ}C$
  - $< 1\mu A$  across operating temperature of  $-55^{\circ}C$  to  $125^{\circ}C$
- Fast Response time:  $10\mu s$  (typical) at  $I_F = 5mA$ ,  $V_{CC} = 20V$ ,  $R_L = 200\Omega$ ,  $C_L = 50pF$
- Ultra-low input trigger current of  $800\mu A$  (at  $25^{\circ}C$ )
- Functional isolation :  $500V_{RMS}$  Working voltage
- Supports Industrial Temperature Range:  $-55^{\circ}C$  to  $125^{\circ}C$
- Small SO-4 package

## 2 Applications

- [Factory automation and control](#)
- [Building automation](#)
- [Appliances](#)
- [Test and Measurement](#)

## 3 Description

The ISOM8600 is an 80V single-pole, normally-open switch with an opto-emulator input. The opto-emulator inputs control the back-to-back MOSFETs without any power supply required on the secondary side. The devices are pin-compatible and drop-in replaceable for many traditional optocouplers, allowing enhancement to industry-standard packages with no PCB redesign.

The ISOM8600 opto-emulator switch offers significant reliability and performance advantages compared to optocouplers, like wider temperature ranges and tight process controls resulting in small part-to-part variations. Since there is no aging effect to compensate for, the emulated diode-input stage consumes less power than optocouplers that have LED aging and require higher bias currents over the device lifetime. ISOM8600 switch output can be controlled by just  $0.8mA$  current through anode/cathode pins over the lifetime of the device, enabling system power savings.

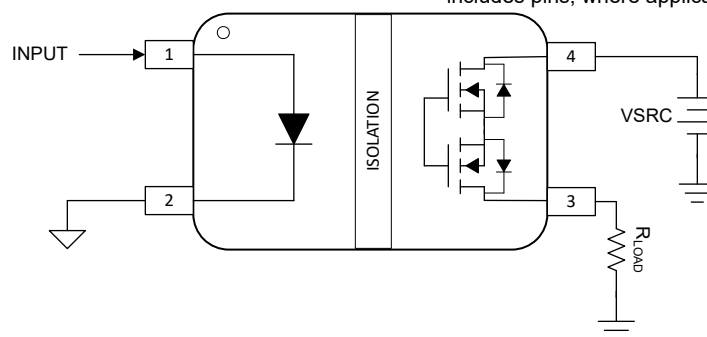
The ISOM8600 is offered in a small SO-4 package, supporting a  $500V_{RMS}$  functional isolation. The high performance and reliability of the device enable the devices use in applications like Building automation, Factory automation, Semiconductor test, I/O modules in industrial controllers, factory automation applications, and more spaces.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE (NOM)
ISOM8600	DFG (SO, 4)	7.0mm × 3.5mm	4.8mm × 3.5mm

(1) For more information, see [Section 12](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



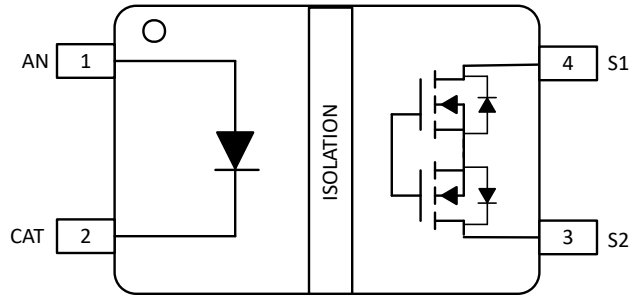
**Simplified Application Example**



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## 4 Pin Configuration and Functions



**Figure 4-1. ISOM8600 DFG Package, 4-Pin SOIC (Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	Description
NAME	NO.		
AN	1	I	Anode connection of diode emulator
CAT	2	I	Cathode connection of diode emulator
S2	3	I/O	Switch input
S1	4	I/O	Switch input

(1) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

See <sup>(1)</sup> <sup>(2)</sup>

			MIN	MAX	UNIT
Input	$I_{F(max)}$	LED forward current		50	mA
	$V_R$	Input reverse voltage at $I_R = 10\mu A$		7	V
	$P_I$	Input power dissipation		100	mW
Output	$V_{OFF}$	Blocking voltage		80	V
	$I_O$	Output continuous load current		200	mA
	$\Delta I_O/^\circ C$	Output continuous load current		-1.1	mA/°C
	$I_{OP}$	Output pulse current (1 $\mu s$ width)		600	mA
	$P_O$	Output power dissipation		150	mW
	$P_T$	Total power dissipation		200	mW
	$T_{stg}$	Storage temperature	-65	150	°C

- Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- All specifications are at  $T_A = 25^\circ C$  unless otherwise noted

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	$\pm 2000$	V
		Charged device model (CDM), ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup>	$\pm 1000$	

- JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$T_A$	Ambient temperature	-55		125	°C
$T_J$	Junction temperature	-55		150	
$I_{F(ON)}$	Input ON-state forward current	0.8		20	mA
$I_O$	Output continuous load current at $I_F=3mA$ <sup>(1)</sup>			150	
$V_{OFF}$	Output Blocking Voltage			70	V

- For  $T_A=25^\circ C$ , Current available to load must be derated by 1mA/°C for  $T_A > 25^\circ C$

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ISOM8610	
		DFG	UNIT
		4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	130.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	52.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	127.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_D$	Maximum power dissipation (both sides)	$I_F = 20\text{mA}$ , $T_J = 150^\circ\text{C}$ , $I_O = 150\text{mA}$ , $T_A = 25^\circ\text{C}$			310	mW
$P_{D1}$	Maximum power dissipation (side-1)				36	mW
$P_{D2}$	Maximum power dissipation (side-2)				274	mW

## 5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			4-DFG	
<b>IEC 60664-1</b>				
CLR	External clearance <sup>(1)</sup>	Side 1 to side 2 distance through air	> 5	mm
CPG	External creepage <sup>(1)</sup>	Side 1 to side 2 distance across package surface	> 5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	μm
CTI	Comparative tracking index	IEC 60112; UL 746A	>400	V
	Material Group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 300V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 600V <sub>RMS</sub>	I-III	
<b>DIN EN IEC 60747-17 (VDE 0884-17) (2)</b>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	707	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test	500	V <sub>RMS</sub>
		DC voltage	707	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1s (100% production)	5303	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50μs waveform per IEC 62368-1	7200	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 62368-1, 1.2/50μs waveform, V <sub>TEST</sub> = 1.6 × V <sub>IMP</sub> or min 10 kV <sub>PK</sub> (qualification)	6250	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60s; V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> , t <sub>m</sub> = 10s	≤ 5	
		Method b: At routine test (100% production), V <sub>ini</sub> = 1.2 × V <sub>IOTM</sub> , t <sub>ini</sub> = 1s; V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> , t <sub>m</sub> = 1s (method b1) or V <sub>pd(m)</sub> = V <sub>ini</sub> , t <sub>m</sub> = t <sub>ini</sub> (method b3)	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.4 × sin (2 πft), f = 1MHz	1	pF
R <sub>IO</sub>	Insulation resistance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 500V, T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500V, 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	
		V <sub>IO</sub> = 500V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		55/125/21	
<b>UL 1577</b>				
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1s (100% production)	3750	V <sub>RMS</sub>

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) Testing is carried out in air to determine the surge immunity of the package.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-pin device.

## 5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 61010-1 and IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010/A1:2019 and EN 62368-1:2014
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

## 5.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SOP-4 PACKAGE (DFG)</b>						
I <sub>S</sub>	Safety limiting input current	R <sub>θJA</sub> =206.3°C/W, V <sub>F</sub> =1.5V, I <sub>O</sub> =0mA, T <sub>J</sub> =150°C, T <sub>A</sub> =25°C			400	mA
	Safety limiting output current	R <sub>θJA</sub> =206.3°C/W, V <sub>F</sub> =1.5V, I <sub>F</sub> =20mA, T <sub>J</sub> =150°C, T <sub>A</sub> =25°C			270	mA
P <sub>S</sub>	Safety limiting total power	R <sub>θJA</sub> =206.3°C/W, T <sub>J</sub> =150°C, T <sub>A</sub> =25°C			610	mW
T <sub>S</sub>	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>. The junction-to-air thermal resistance, R<sub>θJA</sub>, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:  
 $T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.  
 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where T<sub>J(max)</sub> is the maximum allowed junction temperature.  
 $P_S = I_S \times V_I$ , where V<sub>I</sub> is the maximum input voltage.

## 5.9 Electrical Characteristics

All specifications are at  $T_A = 25^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>INPUT</b>							
$V_F$	Input forward voltage	$I_F = I_{FT}$	25°C	0.9	1.1	1.3	V
			-55°C to 125°C	0.85	1.1	1.35	
		$I_F = 5\text{mA}$	25°C	1.1	1.3	1.5	
			-55°C to 125°C	1.1	1.3	1.55	
$I_R$	Input reverse current	$V_R = 5\text{V}$	-55°C to 125°C			10	$\mu\text{A}$
$C_{IN}$	Input capacitance	$f = 1\text{MHz}$ , $V_F = 0\text{V}$	25°C		17	28	pF
$I_{FT}$	Input Trigger forward current; see Figure 7-3	$I_o = 100\text{mA}$ (1), $R_{ON} = 10\Omega$ (2)	25°C		0.65	0.8	mA
			-55°C to 125°C		0.65	1.2	
$I_{FT,release}$	Release Trigger Current	$I_{OFF} = 1\mu\text{A}$ at 70V	-55°C to 125°C	0.1			mA
$V_{F,release}$	Release Trigger Voltage	$I_{OFF} = 1\mu\text{A}$ at 70V	-55°C to 125°C	0.7			V
$I_{F(ON)}$	Input on-state forward current	$I_o = 100\text{mA}$ , $R_{ON} < 10\Omega$ $I_o = 100\text{mA}$ (1), $R_{ON} < 15\Omega$	25°C	0.8		20	mA
			-55°C to 125°C	1.2		20	
<b>OUTPUT</b>							
$V_{OFF}$	Output Blocking voltage	$I_F = 0\text{mA}$	-55°C to 125°C			70	V
$R_{ON}$	Output on-state resistance; see Figure 7-3	$I_F = I_{FT}$ , $I_o = 20\text{mA}$	25°C		6.5	9	$\Omega$
			-55°C to 125°C		6.5	12	
	Output on-state resistance; see Figure 7-3 (1)	$I_F = I_{FT}$ , $I_o = 100\text{mA}$	25°C		7	10	
			-55°C to 125°C		7	13	
	Output on-state resistance; see Figure 7-3	$I_F = I_{FT}$ , $I_o = 100\text{mA}$ , $t < 1\text{s}$	25°C		7	10	
			-55°C to 125°C		5.5	7	
	Output on-state resistance; see Figure 7-3 (1)	$I_F = 3\text{mA}$ , $I_o = 20\text{mA}$	25°C		5.5	7	
			-55°C to 125°C		5.5	12	
Output on-state resistance; see Figure 7-3 (1)	$I_F = 3\text{mA}$ , $I_o = 100\text{mA}$	25°C		6	7.5		
		-55°C to 125°C		6	12		
Output on-state resistance; see Figure 7-3 (1)	$I_F = 3\text{mA}$ , $I_o = 100\text{mA}$ , $t < 1\text{s}$	25°C		5	7		
		-55°C to 125°C		5	7		
$C_{OFF}$	Output off-state capacitance	$I_F = 0\text{mA}$ , $V_L = 60\text{V}$ , $f = 1\text{MHz}$	-55°C to 125°C		6.5	8	pF
$I_{LEAK}$	Output off-state leakage; see Figure 7-2	$I_F = 0\text{mA}$ , $V_{OFF} = 70\text{V}$	25°C			250	nA
			-55°C to 125°C			1	$\mu\text{A}$
$R_{ON\ FLAT}$	On-state resistance flatness	$I_F = 5\text{mA}$	25°C		45	75	m $\Omega$
			-55°C to 125°C		45	115	
$R_{ON\ DRIFT}$	On-state resistance drift across temperature	$I_F = 3\text{mA}$ , $I_o = 40\text{mA}$	-55°C to 125°C		23	60	m $\Omega/^\circ\text{C}$
BW	-3dB Bandwidth; see Figure 7-4	$I_F = 5\text{mA}$ , $R_L = 50\Omega$	25°C	100			MHz
$I_L$	Insertion Loss (LED On); see Figure 7-4	$I_F = 5\text{mA}$ , $R_L = 50\Omega$ , $f = 1\text{MHz}$	25°C		-0.45		dB
$O_{ISO}$	Off-state Isolation; see Figure 7-5	$I_F = 0\text{mA}$ , $R_L = 50\Omega$ , $f = 1\text{MHz}$	25°C		-45		dB

(1) Current available to load must be derated by 1mA/°C for  $T_A > 75^\circ\text{C}$

(2)  $I_{FT}$  measured for  $R_{ON}=15\Omega$  for  $T_A > 75^\circ\text{C}$



### 5.10 Switching Characteristics

All specifications are at  $T_A = 25^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
<b>AC</b>							
$T_{ON}$	Output turn-on time; see Figure 7-1	$I_F = 5\text{mA}$ , $V_{CC} = 20\text{V}$ , $R_L = 200\Omega$ , $C_L = 50\text{pF}$	$-55^\circ\text{C}$ to $125^\circ\text{C}$			0.2	ms
$T_{OFF}$	Output turn-off time; see Figure 7-1	$I_F = 5\text{mA}$ , $V_{CC} = 20\text{V}$ , $R_L = 200\Omega$ , $C_L = 50\text{pF}$	$-55^\circ\text{C}$ to $125^\circ\text{C}$			0.2	ms

### 6 Typical Characteristics

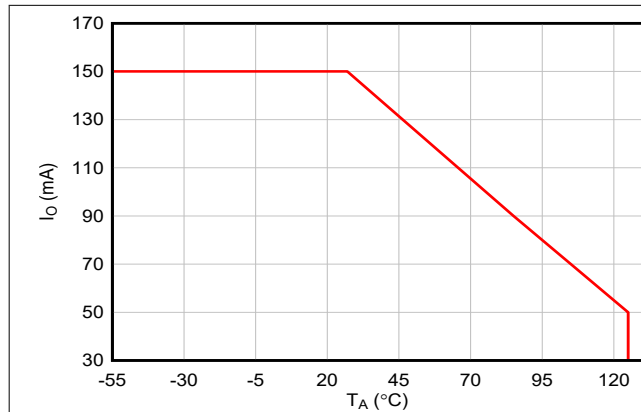


Figure 6-1. Typical Maximum Load Current vs Temperature

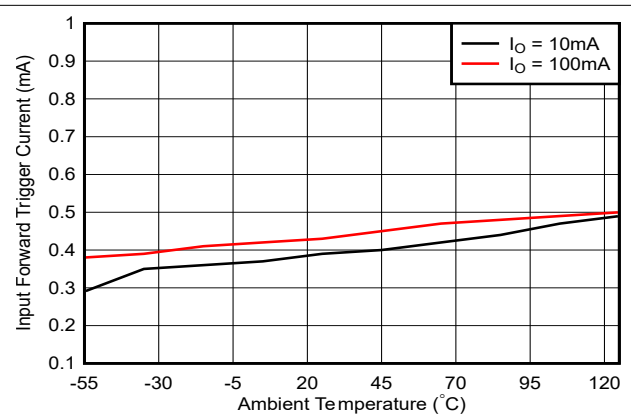


Figure 6-2. Input Forward Trigger Current vs Ambient Temperature

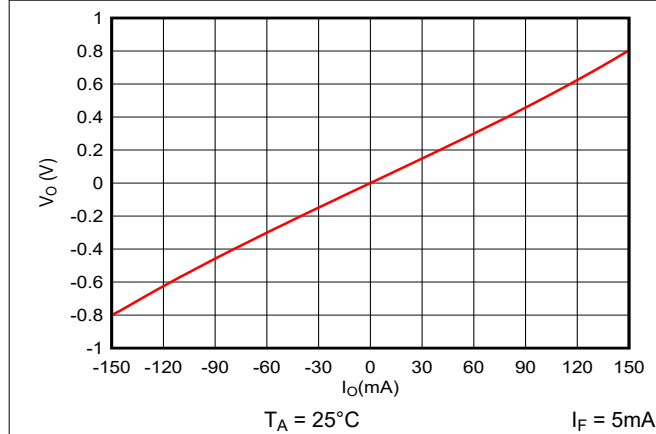


Figure 6-3. Continuous Load Current vs On-State Voltage

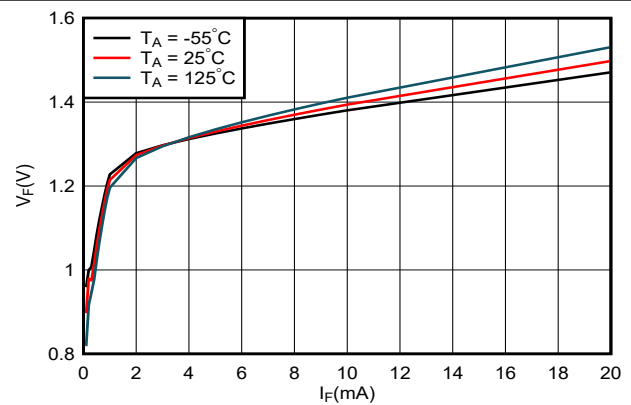


Figure 6-4. Forward Current vs LED Forward Voltage

## 6 Typical Characteristics (continued)

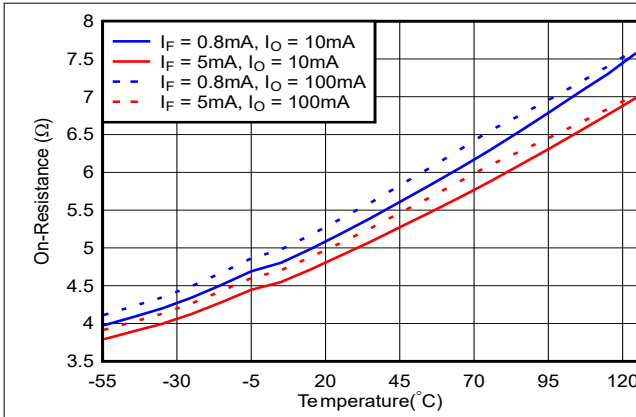


Figure 6-5. On-State Resistance vs Ambient Temperature

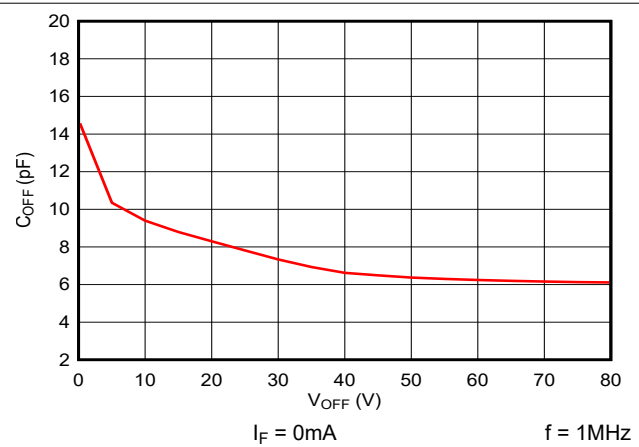


Figure 6-6. Output Capacitance vs Load Voltage

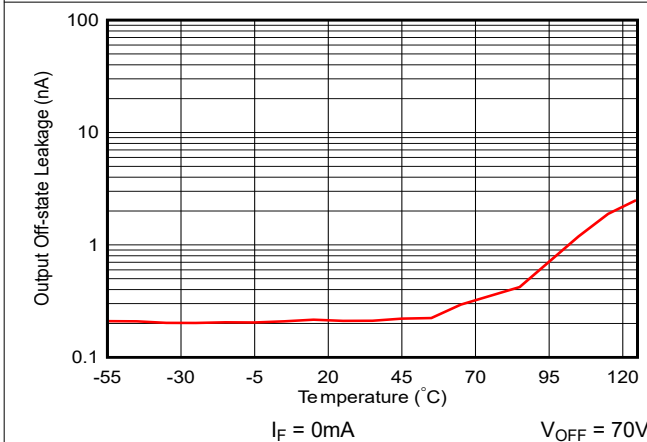


Figure 6-7. Off-State Leakage vs Ambient Temperature

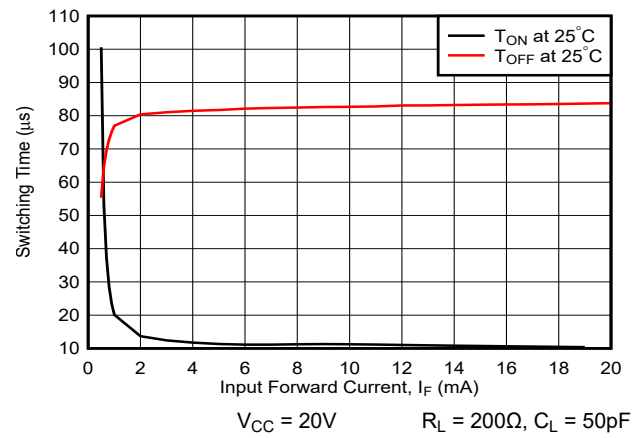


Figure 6-8. Turn-On, Turn-Off Time vs Forward Current

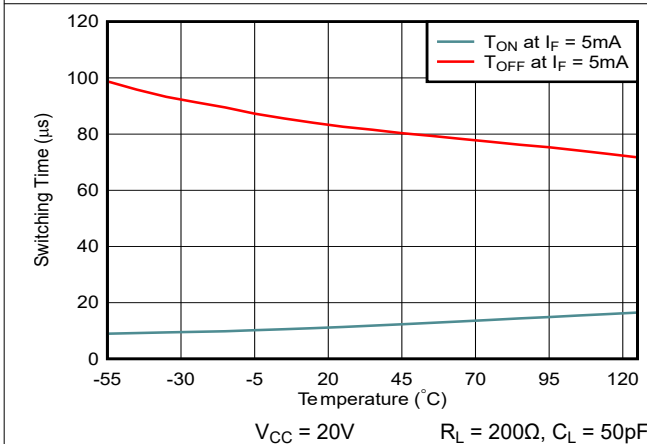


Figure 6-9. Turn-On, Turn-Off Time vs Ambient Temperature

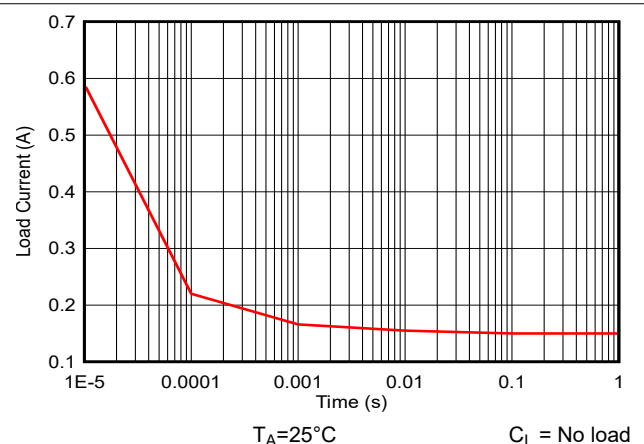
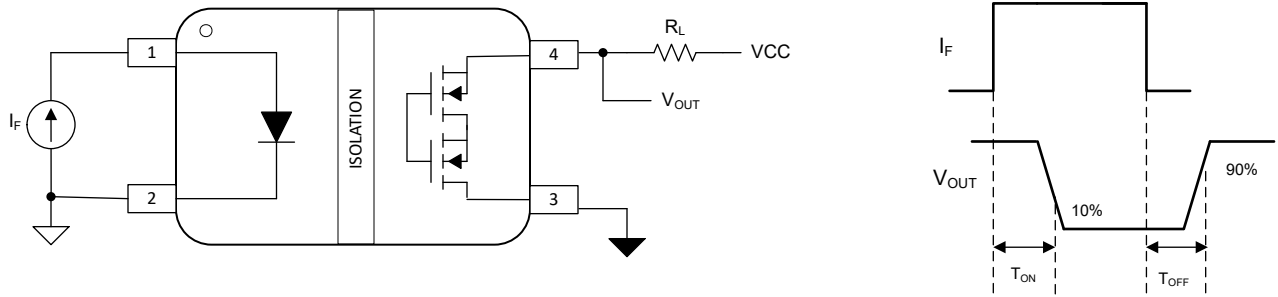
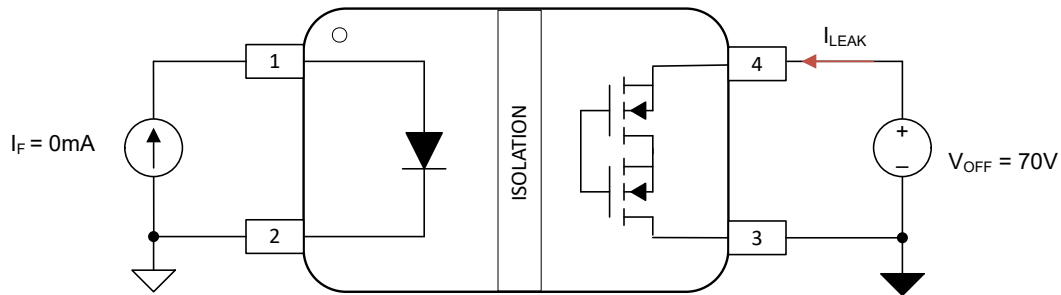


Figure 6-10. Pulse Current Rating Curve at 25°C

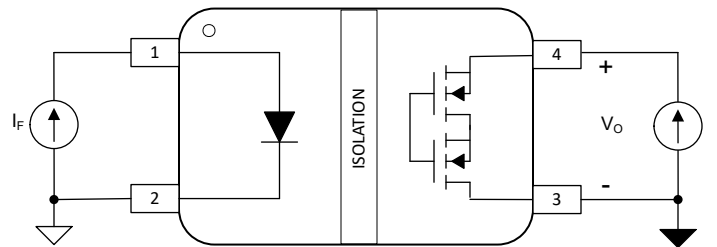
## 7 Parameter Measurement Information



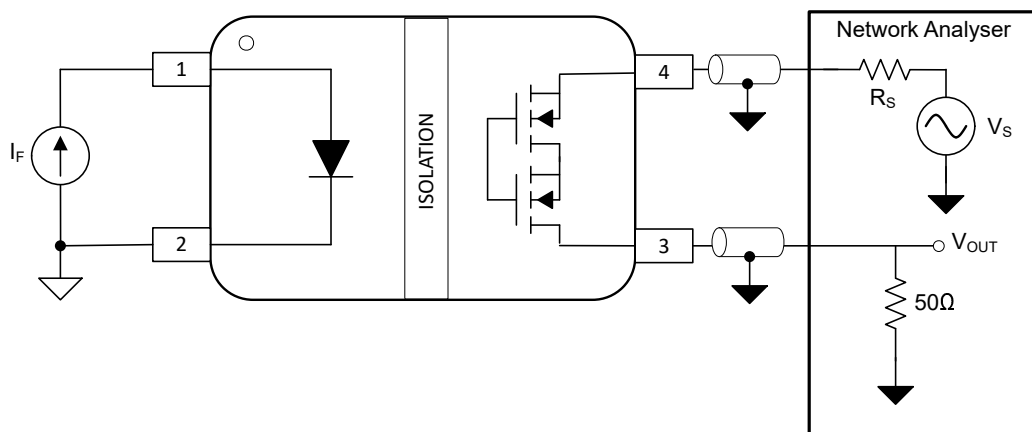
**Figure 7-1. ISOM8600 Test Circuit for Turn-On and Turn-Off Time**



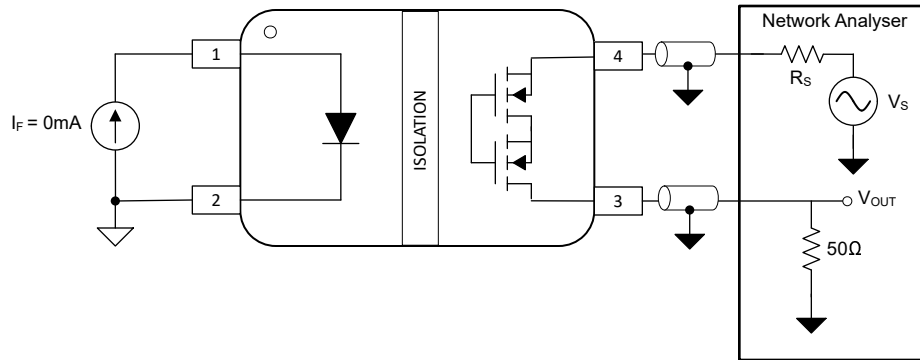
**Figure 7-2. ISOM8600 Test Circuit Off-State Leakage**



**Figure 7-3. ISOM8600 Test Circuit for On-State Resistance**



**Figure 7-4. ISOM8600 Test Circuit for Insertion Loss**



**Figure 7-5. ISOM8600 Test Circuit for Off-State Isolation**

## 8 Detailed Description

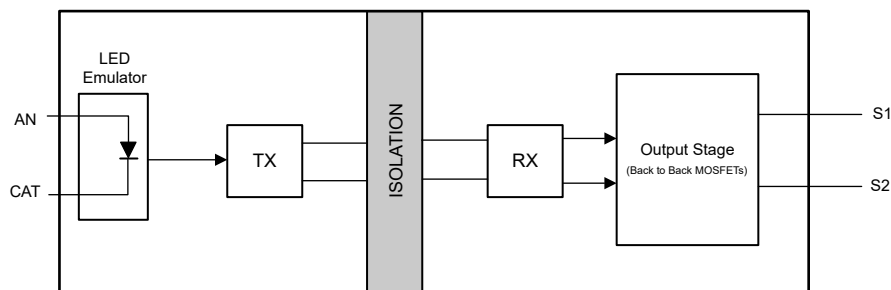
### 8.1 Overview

The ISOM8600 are functionally isolated opto-emulator switches that are pin-compatible, drop-in replacements to popular photo-relays. While standard optocouplers use an LED as the input stage, the ISOM8600 uses a current controlled emulated diode as the input stage. The input stage is isolated from the driver stage by TI's proprietary silicon dioxide-based ( $\text{SiO}_2$ ) isolation barrier, which not only provides robust isolation, but also offers best-in-class performance.

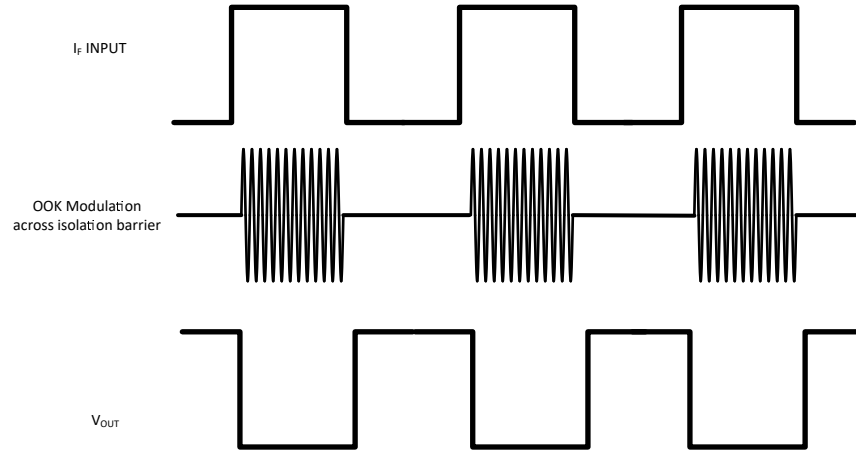
The ISOM8600 isolates high voltage signals and offer performance, reliability, and flexibility advantages over traditional optocouplers which age over time. The devices are based on CMOS isolation technology for low-power and high-speed operation, therefore the devices are resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age.

The functional block diagram of the ISOM8600 is shown in [Functional Block Diagram](#). The input signal is transmitted across the isolation barrier using an on-off keying (OOK) modulation scheme. The transmitter sends a high-frequency carrier across the barrier to represent switch-ON state and sends no signal to represent the switch-OFF state. The receiver demodulates the signal after advanced signal conditioning and controls the state of the output MOSFETs. These devices also incorporate advanced circuit techniques to maximize CMTI performance and minimize radiated emissions. [Figure 8-2](#) shows conceptual detail of how the OOK scheme works.

### 8.2 Functional Block Diagram



**Figure 8-1. Conceptual Block Diagram of an Opto-Emulator**



**Figure 8-2. On-Off Keying (OOK) Based Modulation Scheme**

### 8.3 Feature Description

The ISOM8600 is a current controlled isolated switch, and is a reliable pin-to-pin replacement of to existing Opto-MOS devices in DFG package. The isolated switch is normally open, which means the switch on secondary side is in OFF state when the primary LED emulator current is lower than the input trigger current level. In the OFF state, the back-to-back MOSFETs on the secondary side block up to 80V of difference between S1 and S2. Once the primary side LED emulator current goes above input trigger current, the switch on the secondary side turns ON. During the ON state, the secondary side back-to-back FETs can conduct currents up to 150mA. The robust SiO<sub>2</sub> dielectric isolation in the ISOM8600 provides a functionally isolated isolation barrier side 1 and side 2 for applications that do not safety certifications.

### 8.4 Device Functional Modes

Table 8-1 lists the functional modes for the ISOM86xx devices.

**Table 8-1. Function Table**

INPUT CURRENT $I_F$	OUTPUT SWITCH STATE	COMMENTS
$0 < I_F < I_{FT}$	OFF	Switch is in OFF state and presents an off state capacitance ( $C_{OFF}$ ) across S1 and S2.
$I_{FT} \leq I_F$	ON	Switch is in ON state and presents an on resistance ( $R_{ON}$ ) across S1 and S2

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The ISOM8600 is a single-channel isolated switch with diode-emulator inputs which control an output stage with back-to-back MOSFETs. The devices use robust on-off keying modulation to transmit data across the isolation barrier. Since an isolation barrier separates the two sides of these devices, each side can be sourced independently with voltages and currents within recommended operating conditions. The ISOM8600 is designed to be implemented in a variety of applications like realizing switchable termination in communication lines like CAN and RS485, switching burden resistors in analog input modules and small footprint sink/source capable digital output module in AC Servo motor drives.

The opto-emulators do not conform to any specific interface standard and are intended for isolated switching operations. The ISOM8600 is typically placed between a data controller (that is, an MCU or FPGA), and a sensor or a line transceiver, regardless of the interface type or standard.

### 9.2 Typical Application

The ISOM8600 can be used in numerous industrial applications. For instance, ISOM8600 can be used in a digital output module in servo drive modules. Typically, these digital outputs for these modules support sink or source mode or both. The output modules are implemented for about 100mA source/sink current, and for blocking voltage up to 60V. Traditionally the digital output stages require just functional isolation. The digital output stages are implemented using discrete elements like opto-transistors for isolation, discrete transistor for increasing output source/sink current and also a bridge rectifier stage to enable source and sink capable outputs. The entire design is bulky and often requires additional power to compensate for lifetime operation. Biasing conditions with external components has to be carefully handled to provide reliable operation across use conditions. ISOM8600 is a smaller and easier alternate to the discrete implementation with the device allowing up to 150mA bidirectional source and sink capable output in ON state with up to 80V blocking voltage in OFF state. The ISOM8600 can be easily used as an 80V isolated switch when used within the *Recommended Operating Conditions*.

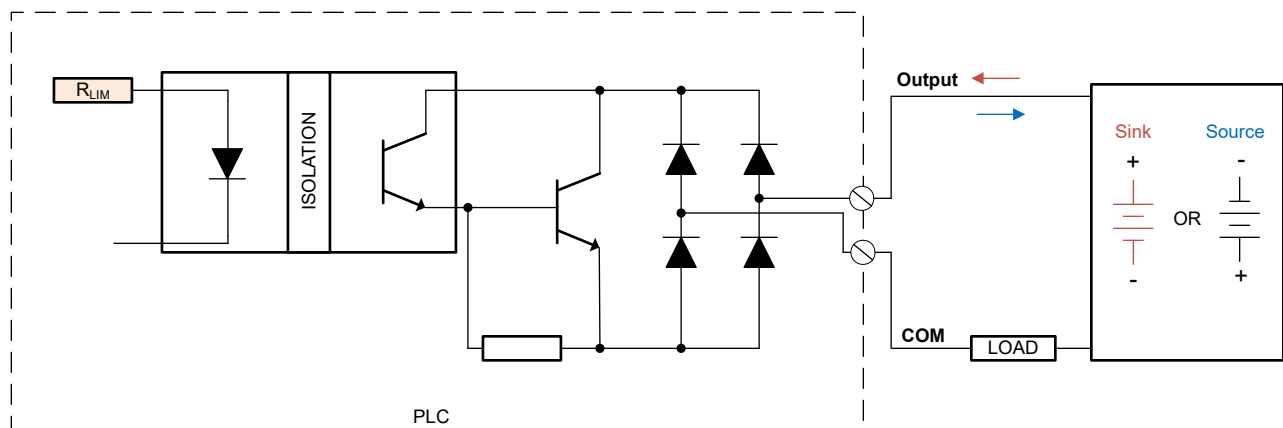


Figure 9-1. Typical Digital Output Stage With Discrete Implementation

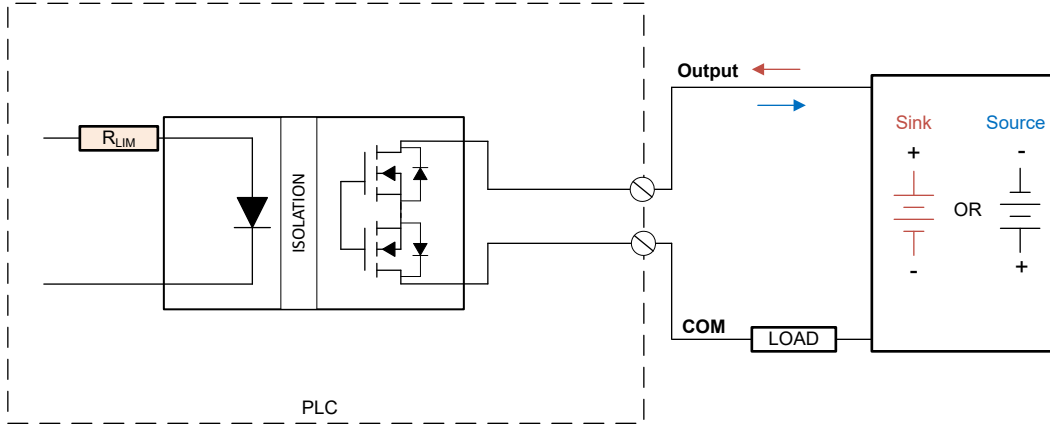


Figure 9-2. Recommended Digital Output Stage implementation With ISOM8600

### 9.2.1 Design Requirements

To design with the ISOM8600 device, use the parameters listed in [Table 9-1](#).

Table 9-1. Design Parameters

PARAMETER	VALUE	EXAMPLE VALUE
Input forward current, $I_F$	0.8mA to 20mA	2mA

### 9.2.2 Detailed Design Procedure

This section presents the design procedure for using the ISOM8600 opto-emulators. External components must be selected to operate the ISOM8600 within the *Recommended Operating Conditions*. The following recommendations on components selection focus on the design of a typical isolated signal circuit with considerations for input current and data rate.

#### 9.2.2.1 Sizing $R_{IN}$

The input side of the ISOM8600 is current-driven. Placing a series resistor,  $R_{IN}$ , in series with the input as shown in [Figure 9-1](#) is recommended to limit the amount of current flowing into the AN pin.

$R_{IN}$  can be sized to minimize current flow and power consumption through the ISOM8600 input-side.  $R_{IN}$  must be a value that limits the input forward current to be within the *Recommended Operating Conditions* for the ISOM8600. The equation to calculate  $R_{IN}$  for a given input voltage,  $V_{IN}$ , and desired input forward current,  $I_F$ , is shown in [Equation 1](#) where  $V_F$  is the maximum specification for the ISOM8600 input forward voltage:

$$R_{IN} = \frac{V_{IN} - V_F [MAX]}{I_F} \quad (1)$$

For example, with a 24V input and 2mA desired  $I_F$ ,  $R_{IN}$  can be calculated as:

$$R_{IN} = \frac{24V - 1.5V}{2mA} = 11.25k\Omega \quad (2)$$

### 9.2.3 Application Curve

The following typical switching curve shows data transmission using the ISOM8600.

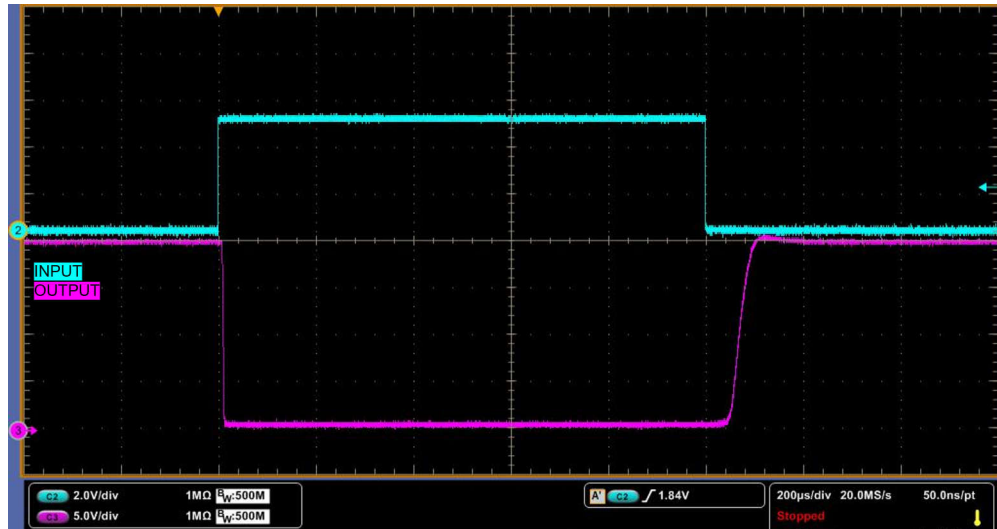


Figure 9-3. Typical Waveform at  $I_F = 5\text{mA}$ ,  $V_{CC} = 20\text{V}$ ,  $R_L = 200\Omega$  and  $C_L = 50\text{pF}$

### 9.3 Power Supply Recommendations

The ISOM8600 does not require a dedicated power supply to operate since there is no supply pin. Take care not to violate recommended operating I/O specifications for proper device functionality.

### 9.4 Layout

#### 9.4.1 Layout Guidelines

- The device connections to ground must be tied to the PCB ground plane using a direct connection or two vias to help minimize inductance.
- The connections of capacitors and other components to the PCB ground plane must use a direct connection or two vias for minimum inductance.

#### 9.4.2 Layout Example

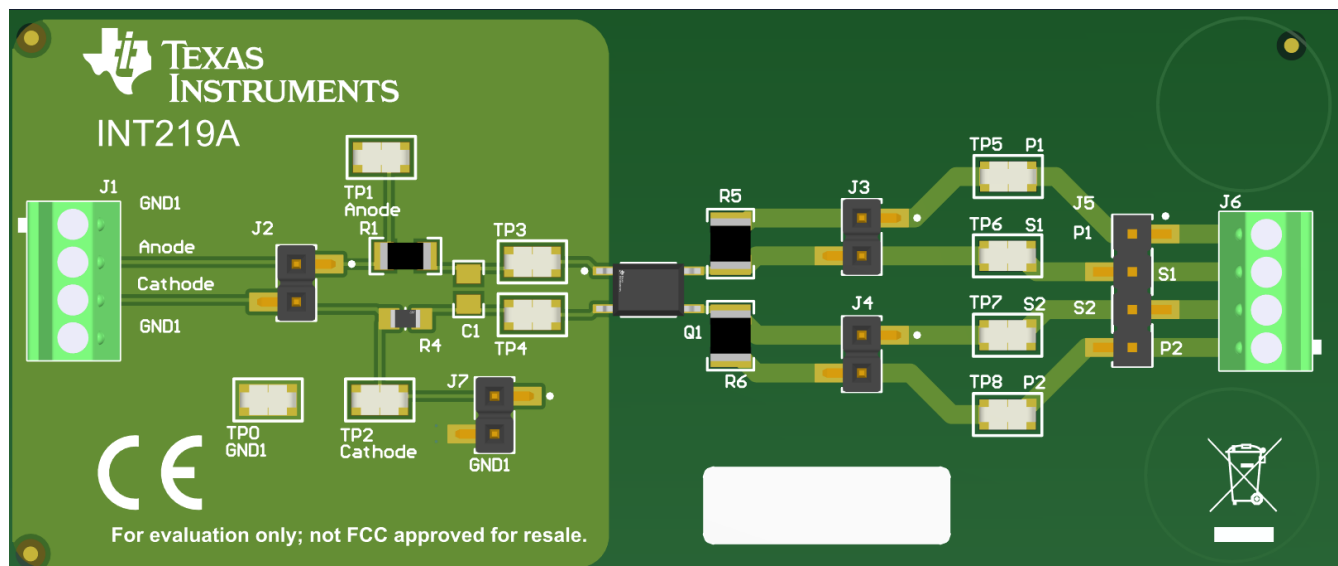


Figure 9-4. Layout Example of ISOM8600 With a 2-Layer Board



## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Isolation Glossary](#), application note

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.4 Trademarks

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### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (April 2024) to Revision A (May 2024)</b>	<b>Page</b>
• Updated the number format for tables, figures, and cross-references throughout the document.....	1
• Added layout guidelines for LED placement .....	16

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

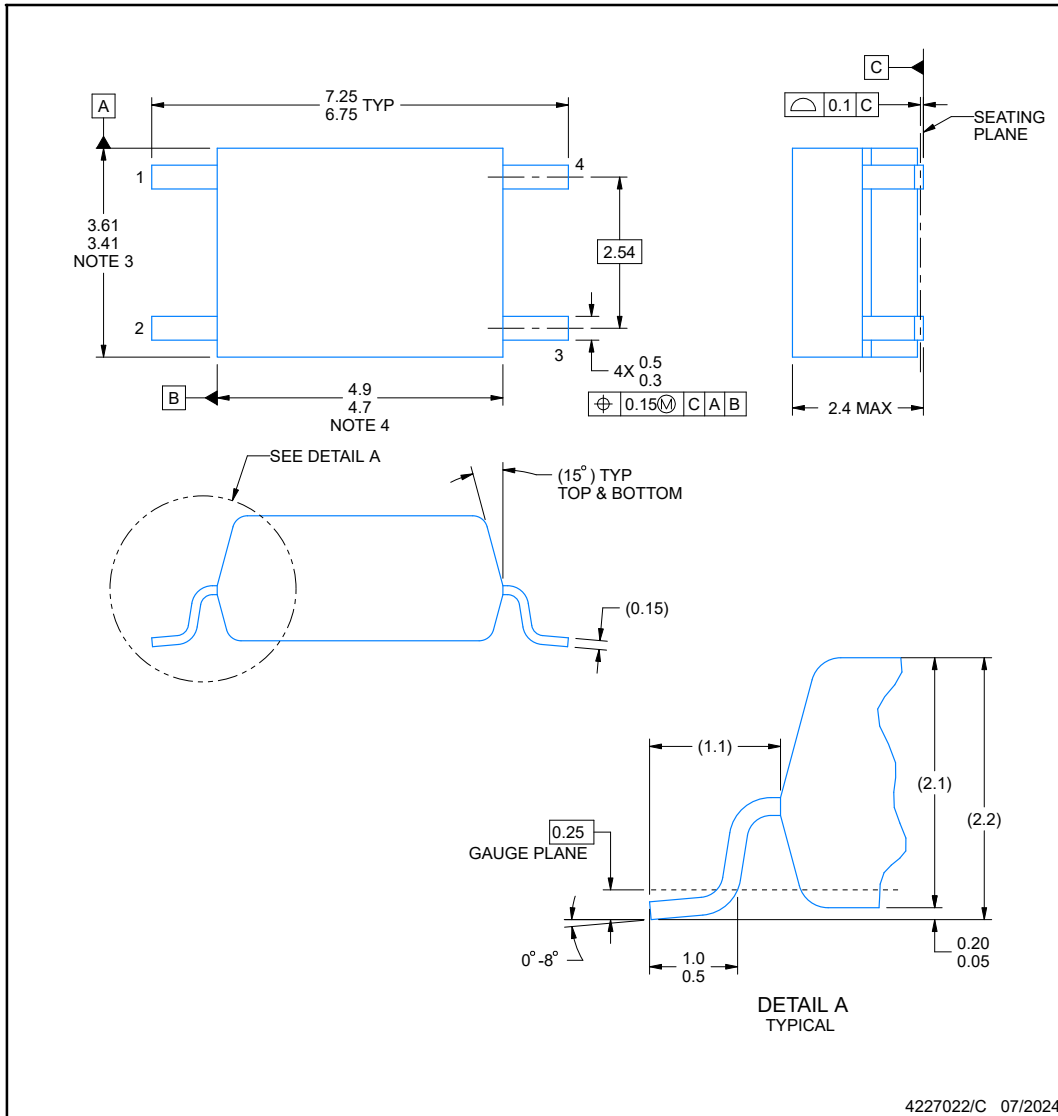


**DFG0004A**

**PACKAGE OUTLINE**

**SOIC - 2.4 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



**NOTES:**

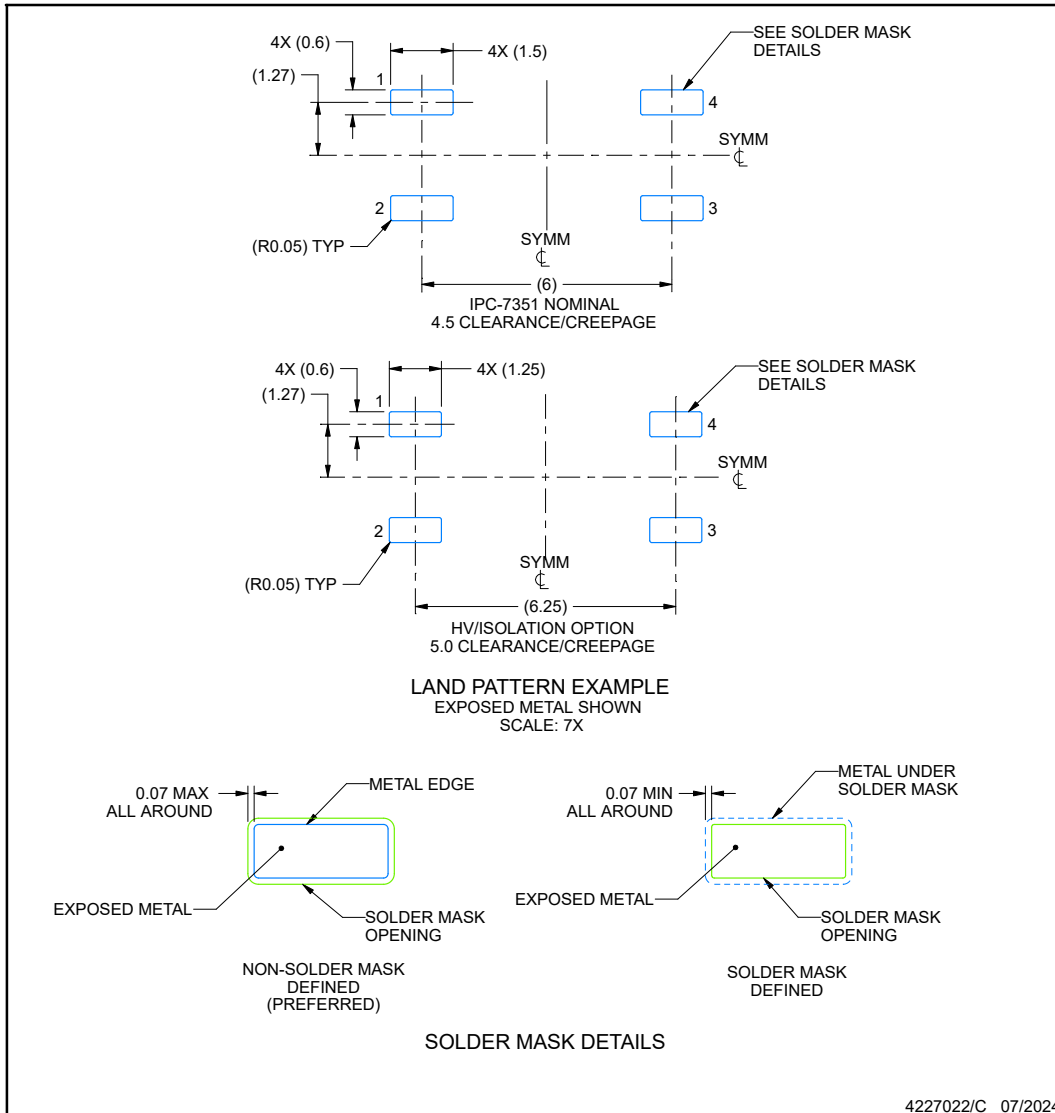
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash.

## EXAMPLE BOARD LAYOUT

DFG0004A

SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

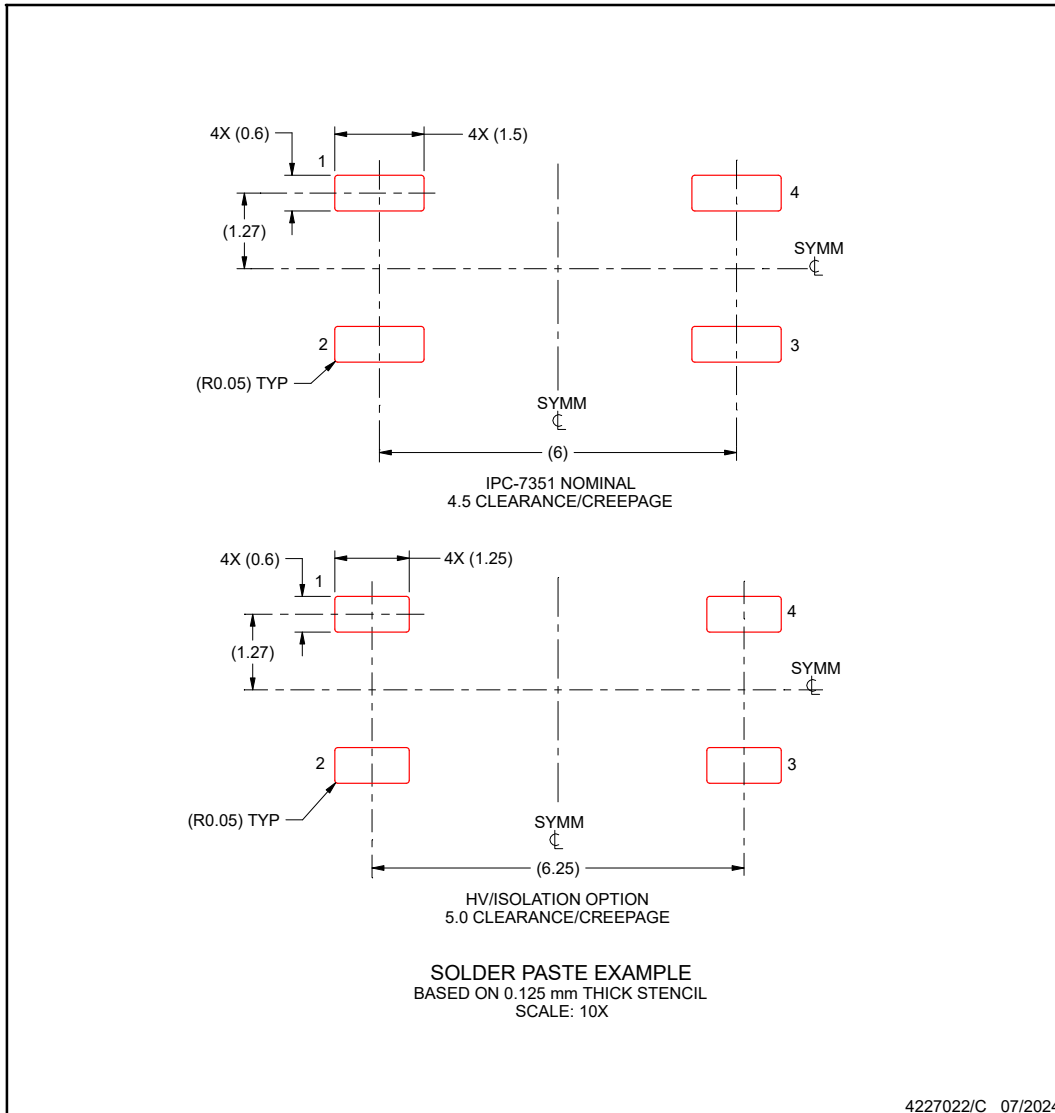
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**DFG0004A**

**SOIC - 2.4 mm max height**

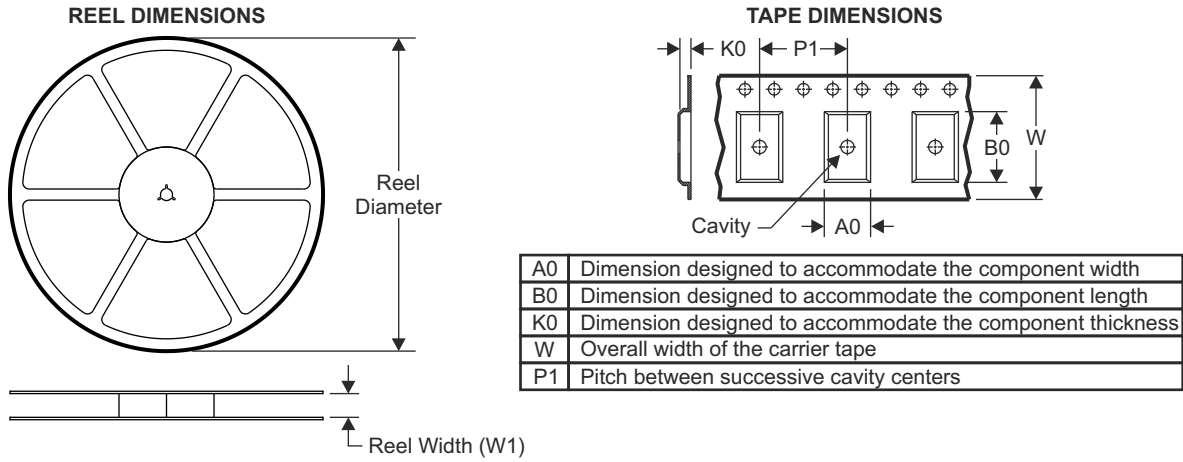
SMALL OUTLINE INTEGRATED CIRCUIT



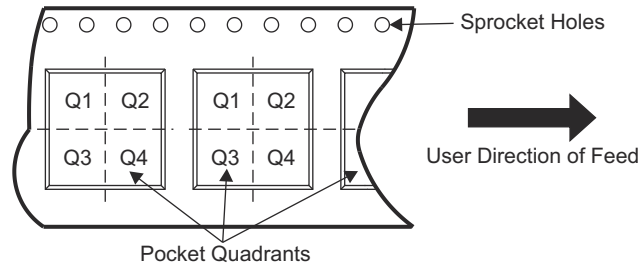
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

### 13 Tape and Reel Information

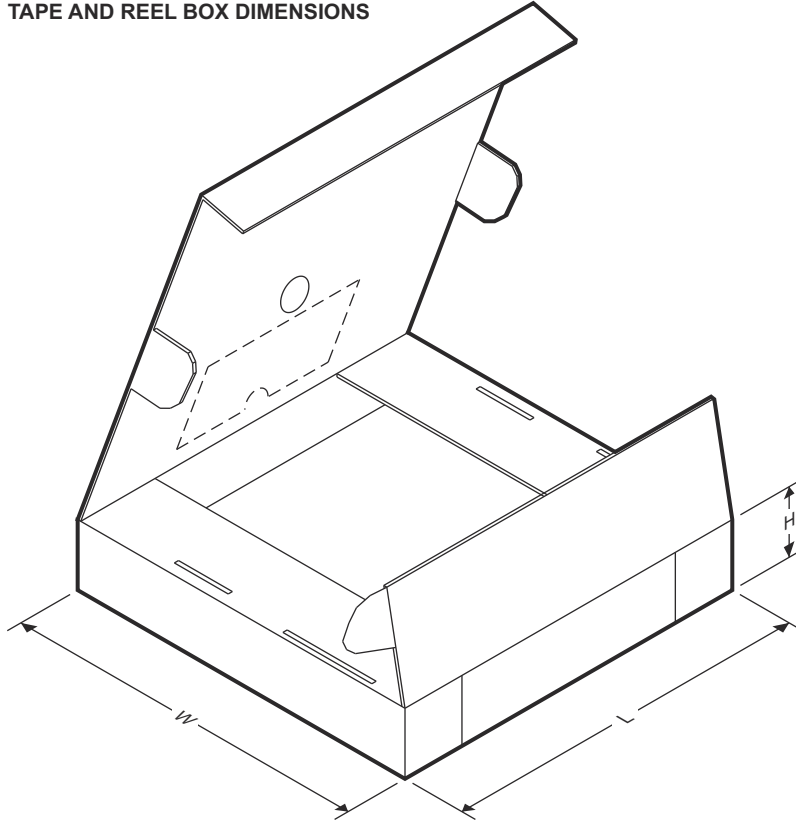


#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOM8610DFGR	SOIC	DFG	4	2000	330	12.4	8	3.8	2.7	12	12	Q1

**TAPE AND REEL BOX DIMENSIONS**



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOM8610DFGR	SOIC	DFG	4	2000	353	353	32

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISOM8610DFGR	ACTIVE	SOIC	DFG	4	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	8610	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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