LMV301 Low Input Bias Current, 1.8V Op Amp w/ Rail-to-Rail Output

Check for Samples: LMV301

FEATURES

- **Input Bias Current: 0.182 pA**
- **Gain Bandwidth Product: 1 MHz**
- **Supply Voltage at 1.8V: 1.8 to 5 V**
- **Supply Current: 150 µA**
- **Input Referred Voltage Noise at 1kHz: 40nV/√Hz**
- **DC Gain (600Ω Load): 100 dB**
- **Output Voltage Range at 1.8V: 0.024 to 1.77 V**
- **Input Common-Mode Voltage Range: −0.3 to ±1.2 V**

APPLICATIONS

- **Thermocouple Amplifiers**
- **Photo Current Amplifiers**
- **Transducer Amplifiers**
- **Sample and Hold Circuits**
- **Low Frequency Active Filters**

DESCRIPTION

The LMV301 CMOS operational amplifier is ideal for single supply, low voltage operation with an ensured operating voltage range from 1.8V to 5V. The low input bias current of less than 0.182pA typical, eliminates input voltage errors that may originate from small input signals. This makes the LMV301 ideal for electrometer applications requiring low input leakage such as sensitive photodetection transimpedance amplifiers and sensor amplifiers. The LMV301 also features a rail-to-rail output voltage swing in addition to a input common-mode range that includes ground. The LMV301 will drive a 600Ω resistive load and up to 1000pF capacitive load in unity gain follower applications. The low supply voltage also makes the LMV301 well suited for portable two-cell battery systems and single cell Li-Ion systems.

The LMV301 exhibits excellent speed-power ratio, achieving 1MHz at unity gain with low supply current. The high DC gain of 100dB makes it ideal for other low frequency applications.

The LMV301 is offered in a space saving SC70 package, which is only 2.0X2.1X1.0mm. It is also similar to the LMV321 except the LMV301 has a CMOS input.

Connection Diagram

Top View

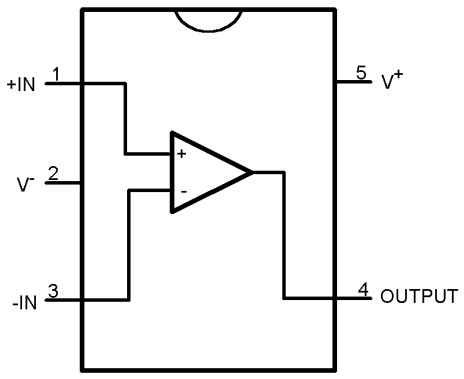

Figure 1. SC70-5 Package
See Package Number DCK0005A

Applications Circuit

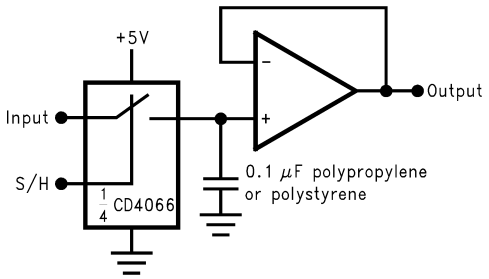

Figure 2. Low Leakage Sample and Hold

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings (1) (2)

ESD Tolerance (3)	Machine Model	200V
	Human Body Model	2000V
Differential Input Voltage		±Supply Voltage
Supply Voltage (V^+ - V^-)		5.5V
Output Short Circuit to V^+ (4)		
Output Short Circuit to V^- (4)		
Storage Temperature Range		−65°C to 150°C
Mounting Temperature	Infrared or Convection (20 sec)	235°C
Junction Temperature (5)		150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF. Machine model, 200Ω in series with 100pF.
(4) Applies to both single supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings (1)

Supply Voltage			1.8V to 5.0V
Temperature Range			$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	Ultra Tiny SC70-5 Package	5-pin Surface Mount	478°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

1.8V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions		Min(1)	Typ(2)	Max(1)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.4V, V^+ = 1.3V, = V^- = −0.5V			0.9	8 **9**	mV
I_B	Input Bias Current				0.182	35 **50**	pA
I_S	Supply Current	V_{CM} = 0.4V, V^+ = 1.3V, = V^- = −0.5V			150	250 **275**	µA
CMRR	Common Mode Rejection Ratio	0.3V ≤ V_{CM} ≤ 0.9V		62 **60**	108		dB
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V, 0.9 ≤ V_{CM} ≤ 2.5V		67 **62**	110		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		−0.3 **0**		0.6	V
A_V	Large Signal Voltage Gain Sourcing	R_L = 600Ω to 0V, V^+ = 1.2V, V^- = −0.6V, V_O = −0.2V to 0.8V, V_{CM} = 0V		80 **75**	119		dB
		R_L = 2kΩ to 0V, V^+ = 1.2V, V^- = −0.6V, V_O = −0.2V to 0.8V, V_{CM} = 0V		80 **75**	111		
	Sinking	R_L = 600Ω to 0V, V^+ = 1.2V, V^- = −0.6V, V_O = −0.2V to 0.8V, V_{CM} = 0V		80 **75**	94		dB
		R_L = 2kΩ to 0V, V^+ = 1.2V, V^- = −0.6V, V_O = −0.2V to 0.8V, V_{CM} = 0V		80 **75**	96		
V_O	Output Swing	R_L = 600Ω to 0.9V V_{IN} = ±100mV	V_{OH}	1.65 **1.63**	1.72		V
			V_{OL}		0.074	0.100	V
		R_L = 2kΩ to 0.9V V_{IN} = ±100mV	V_{OH}	1.75 **1.74**	1.77		V
			V_{OL}		0.024	0.035 **0.040**	V
I_O	Output Short Circuit Current	Sourcing, V_O = 0V, V_{IN} = 100mV		4 **3.3**	8.4		mA
		Sinking, V_O = 1.8V, V_{IN} = −100mV		7	9.8		mA

(1) All limits are ensured by testing or statistical analysis.
(2) Typical value represent the most likely parametric norm.

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ(1)	Units
SR	Slew Rate	See(2)	0.57	V/µs
GBW	Gain Bandwidth Product		1	MHz
φm	Phase Margin		60	Deg
G_m	Gain Margin		10	dB
e_n	Input-Referred Voltage Noise	f = 1kHz, V_{CM} = 0.5V f = 100kHz	40 30	nV/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 RL = 600kΩ, V_{IN} = 1V_{PP}	0.089	%

(1) Typical value represent the most likely parametric norm.
(2) V^+ = 5V. Connected as voltage follower with 5V step input. Number specified is the slower of the positive and negative slew rates.

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions		Min(1)	Typ(2)	Max(1)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.35V, V^+ = 1.7V, V^- = −1V			0.9	8 **9**	mV
I_B	Input Bias Current				0.182	35 **50**	pA
I_S	Supply Current	V_{CM} = 0.35V, V^+ = 1.7V, V^- = −1V			153	250 **275**	µA
CMRR	Common Mode Rejection Ratio	−0.15V ≤ V_{CM} ≤ 1.35V		62 **60**	115		dB
PSRR	Power Supply Rejection Ratio	1.8V ≤ V+ ≤ 5V		67 **62**	110		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		−0.3 **0**		1.5	V
A_V	Large Signal Voltage Gain Sourcing	R_L = 600Ω to 0V, V^+ = 1.35V, V^- = −1.35V, V_O = −1V to 1V, V_{CM} = 0V		80 **75**	100		dB
		R_L = 2kΩ to 0V, V^+ = 1.35V, V^- = −1.35V, V_O = −1V to 1V, V_{CM} = 0V		83 **77**	114		
	Sinking	R_L = 600Ω to 0V, V^+ = 1.35V, V^- = −1.35V, V_O = −1V to 1V, V_{CM} = 0V		80 **75**	98		dB
		R_L = 2kΩ to 0V, V^+ = 1.35V, V^- = −1.35V, V_O = −1V to 1V, V_{CM} = 0V		80 **75**	99		
V_O	Output Swing	R_L = 600Ω to 1.35V V_{IN} = ±100mV	V_{OH}	2.550 **2.530**	2.62		V
			V_{OL}		0.078	0.100	V
		R_L = 2kΩ to 1.35V V_{IN} = ±100mV	V_{OH}	2.650 **2.640**	2.675		V
			V_{OL}		0.024	0.045	V
I_O	Output Short Circuit Current	Sourcing, V_O = 0V, V_{IN} = 100mV		20 **15**	32		mA
		Sinking, V_O = 2.7V, V_{IN} = −100mV		19 **12**	24		mA

(1) All limits are ensured by testing or statistical analysis.
(2) Typical value represent the most likely parametric norm.

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ(1)	Units
SR	Slew Rate	See(2)	0.60	V/µs
GBW	Gain Bandwidth Product		1	MHz
φm	Phase Margin		65	Deg
G_m	Gain Margin		10	dB
e_n	Input-Referred Voltage Noise	f = 1kHz, V_{CM} = 0.5V f = 100kHz	40 30	nV/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600kΩ, V_{IN} = $1V_{PP}$	0.077	%

(1) Typical value represent the most likely parametric norm.
(2) V^+ = 5V. Connected as voltage follower with 5V step input. Number specified is the slower of the positive and negative slew rates.

5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions		Min(1)	Typ(2)	Max(1)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V, V^+ = 3V, V^- = −2V			0.9	8 **9**	mV
I_B	Input Bias Current				0.182	35 **50**	pA
I_S	Supply Current	V_{CM} = 0.5V, V^+ = 3V, V^- = −2V			163	260 **285**	µA
CMRR	Common Mode Rejection Ratio	−1.3V ≤ V_{CM} ≤ 2.5V		62 **61**	111		dB
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V		67 **62**	110		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		−0.3 **0**		3.8	V
A_V	Large Signal Voltage Gain Sourcing	R_L = 600Ω to 0V, V^+ = 2.5V, V^- = −2.5V, V_O = −2V to 2V, V_{CM} = 0V		86 **82**	117		dB
		R_L = 2kΩ to 0V, V^+ = 2.5V, V^- = −2.5V, V_O = −2V to 2V, V_{CM} = 0V		89 **85**	116		
	Sinking	R_L = 600Ω to 0V, V^+ = 2.5V, V^- = −2.5V, V_O = −2V to 2V, V_{CM} = 0V		80 **75**	105		dB
		R_L = 2kΩ to 0V, V^+ = 2.5V, V^- = −2.5V, V_O = −2V to 2V, V_{CM} = 0V		80 **75**	107		
V_O	Output Swing	R_L = 600Ω to 2.5V V_{IN} = ±100mV	V_{OH}	4.850 **4.840**	4.893		V
			V_{OL}		0.1	0.150 **1.160**	V
		R_L = 2kΩ to 2.5V V_{IN} = ±100mV	V_{OH}	4.935	4.966		V
			V_{OL}		0.034	0.065 **0.075**	V
I_O	Output Short Circuit Current	Sourcing, V_O = 0V, V_{IN} = 100mV		85 68	108		mA
		Sinking, V_O = 5V, V_{IN} = −100mV		60 **45**	69		mA

(1) All limits are ensured by testing or statistical analysis.
(2) Typical value represent the most likely parametric norm.

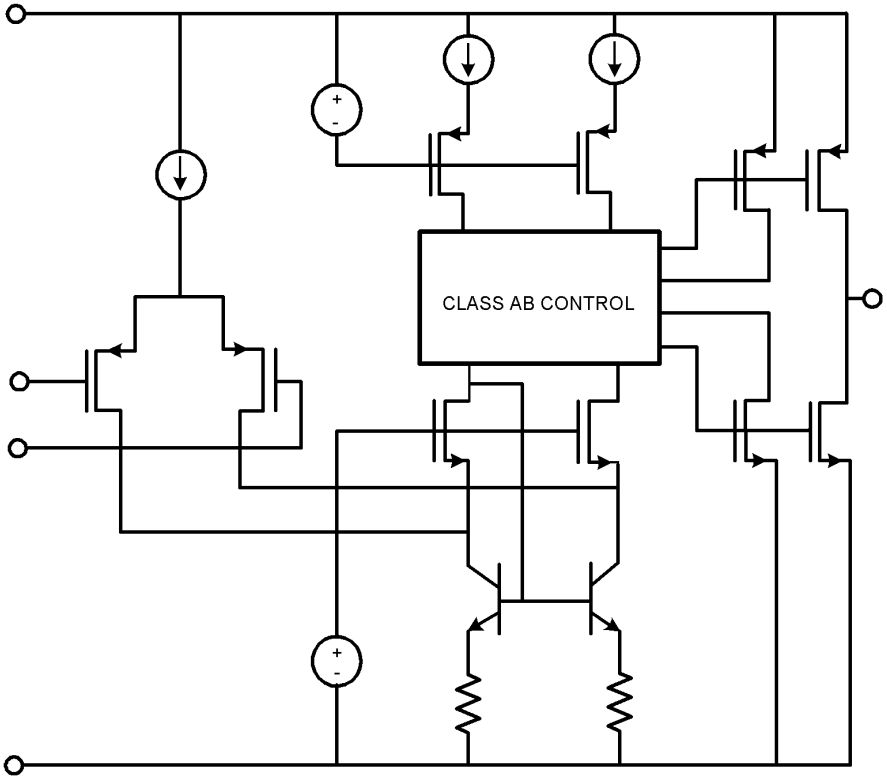
5V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = 2.5V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ(1)	Units
SR	Slew Rate	See(2)	0.66	V/µs
GBW	Gain Bandwidth Product		1	MHz
φm	Phase Margin		70	Deg
G_m	Gain Margin		15	dB
e_n	Input-Referred Voltage Noise	f = 1kHz, V_{CM} = 1V f = 100kHz	40 30	nV/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_O = $1V_{PP}$	0.069	%

(1) Typical value represent the most likely parametric norm.
(2) V^+ = 5V. Connected as voltage follower with 5V step input. Number specified is the slower of the positive and negative slew rates.

Simplified Schematic



Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C.

Supply Current vs. Supply Voltage

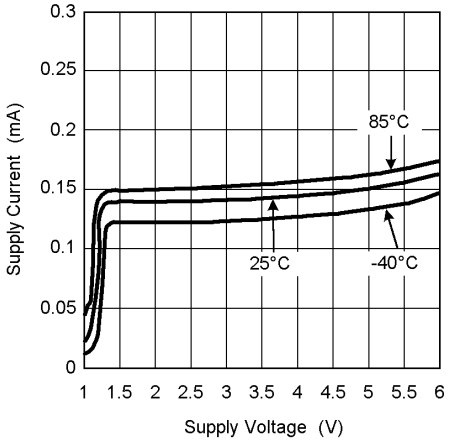


Figure 3.

Output Negative Swing vs. Supply Voltage

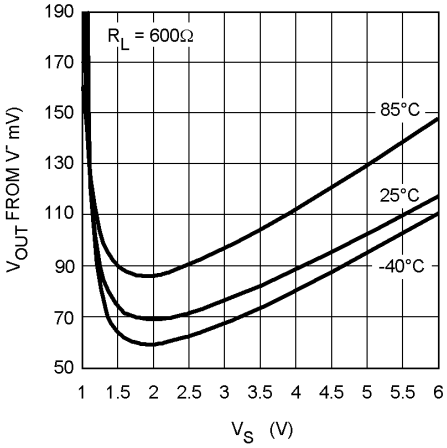


Figure 4.

Output Negative Swing vs. Supply Voltage

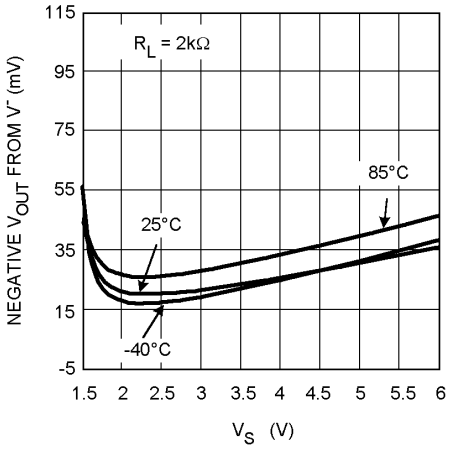


Figure 5.

Output Positive Swing vs. Supply Voltage

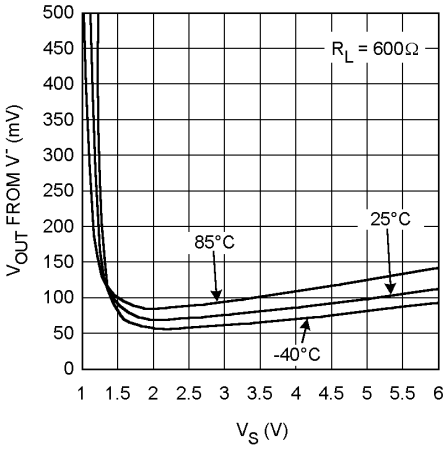


Figure 6.

Output Positive Swing vs. Supply Voltage

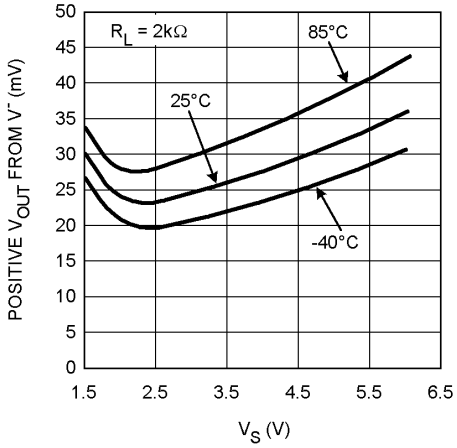


Figure 7.

V_{OS} vs. V_{CM}

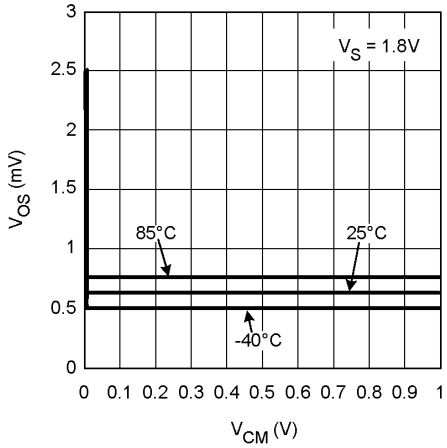


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

V_{OS} vs. V_{CM}

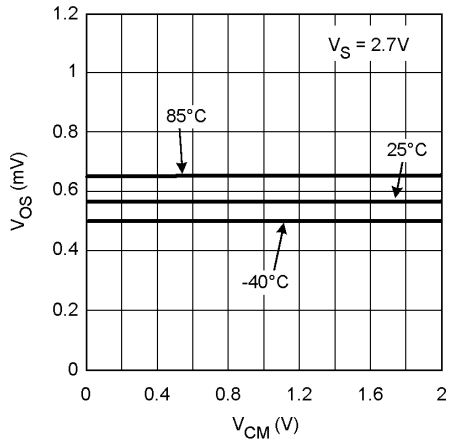


Figure 9.

V_{OS} vs. V_{CM}

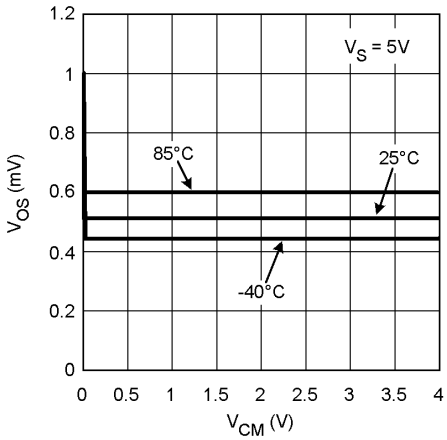


Figure 10.

Sourcing Current vs. Output Voltage

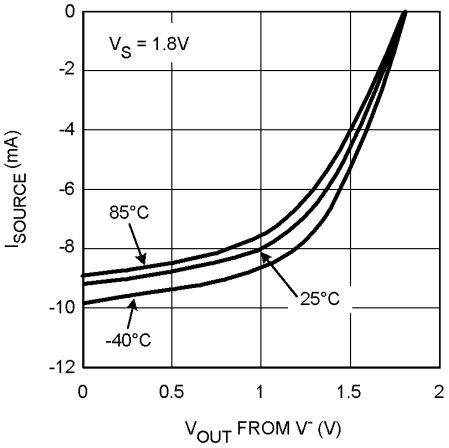


Figure 11.

Sinking Current vs. Output Voltage

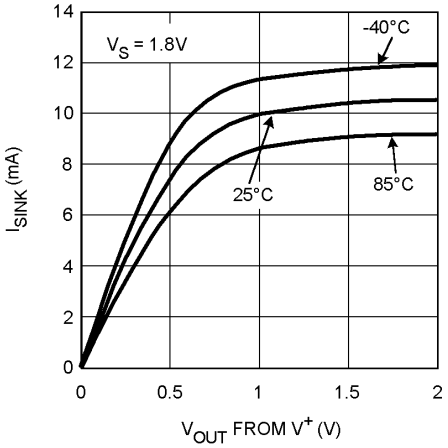


Figure 12.

Sourcing Current vs. Output Voltage

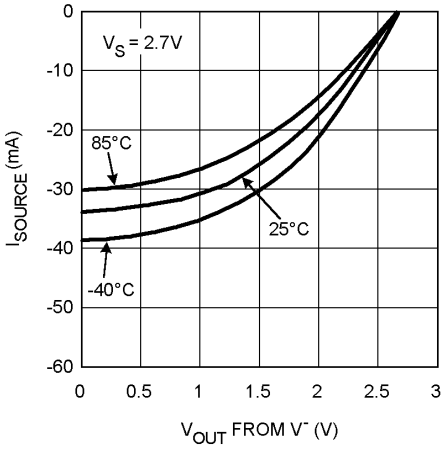


Figure 13.

Sinking Current vs. Output Voltage

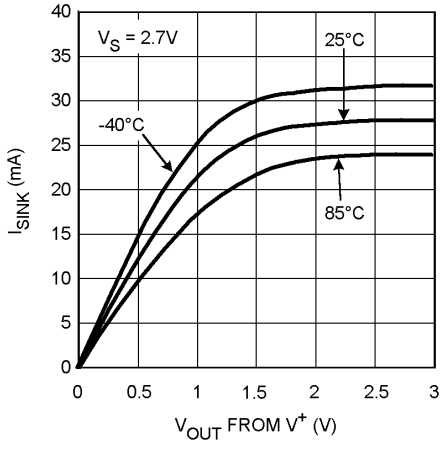


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

Sourcing Current vs. Output Voltage

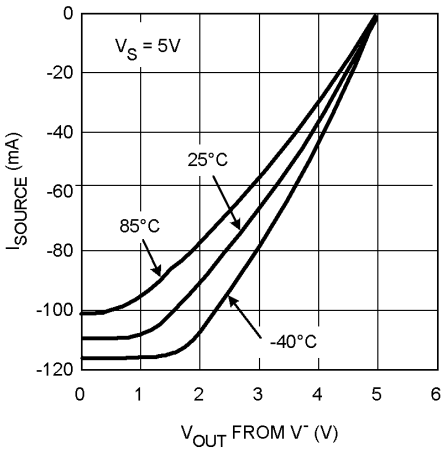


Figure 15.

Sinking Current vs. Output Voltage

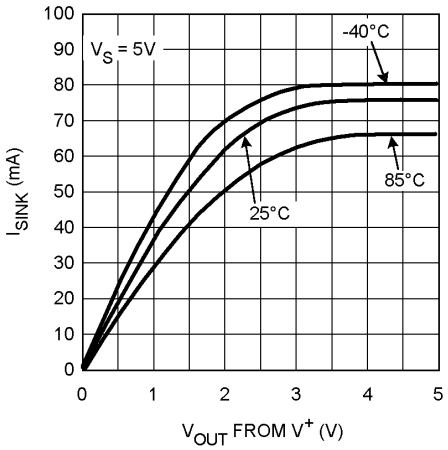


Figure 16.

I_{BIAS} Current vs. V_{CM}

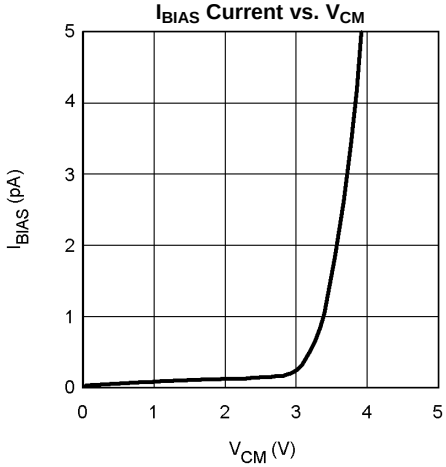


Figure 17.

Open Loop Frequency Response

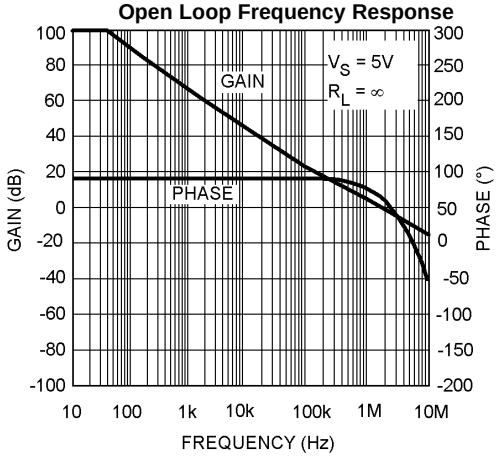


Figure 18.

Open Loop Frequency Response

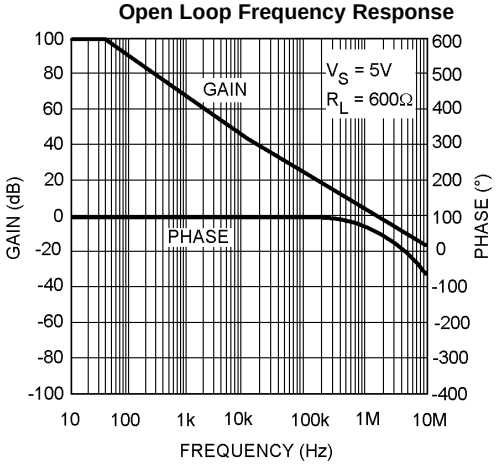


Figure 19.

Open Loop Frequency Response

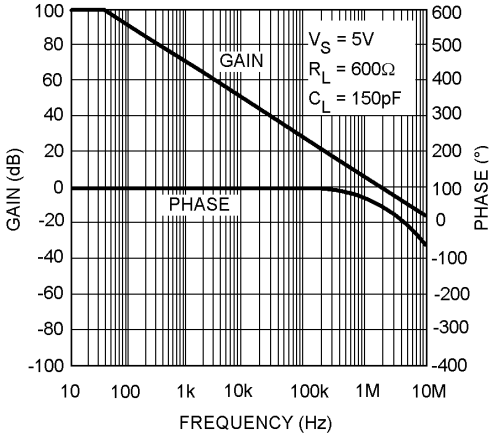


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

Open Loop Frequency Response

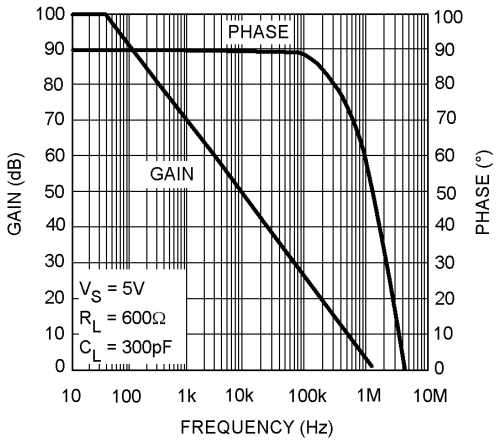


Figure 21.

Open Loop Frequency Response

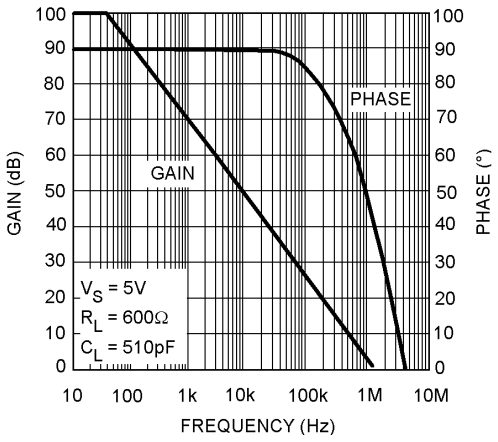


Figure 22.

Open Loop Frequency Response

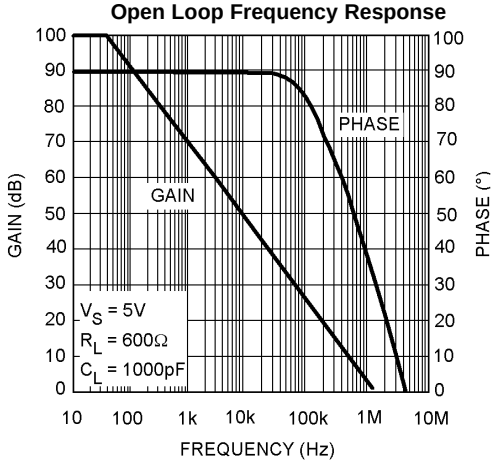


Figure 23.

Noise vs. Frequency Response

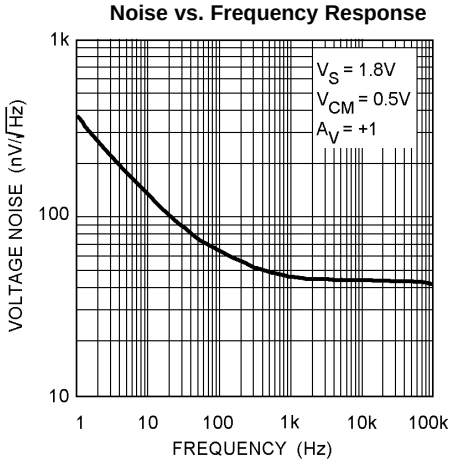


Figure 24.

Noise vs. Frequency Response

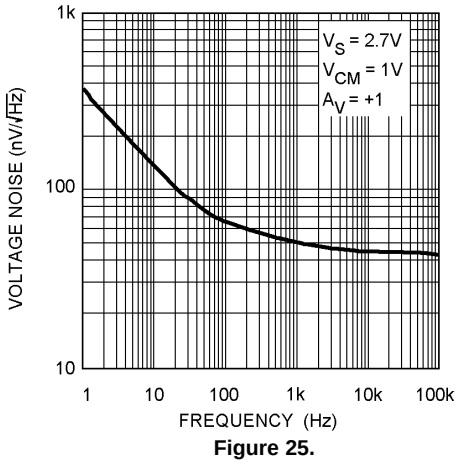


Figure 25.

Noise vs. Frequency Response

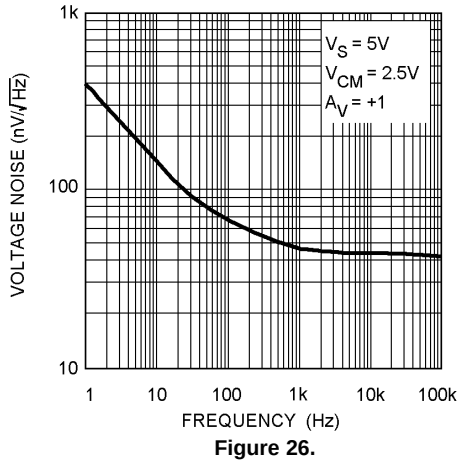


Figure 26.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

Small Signal Response

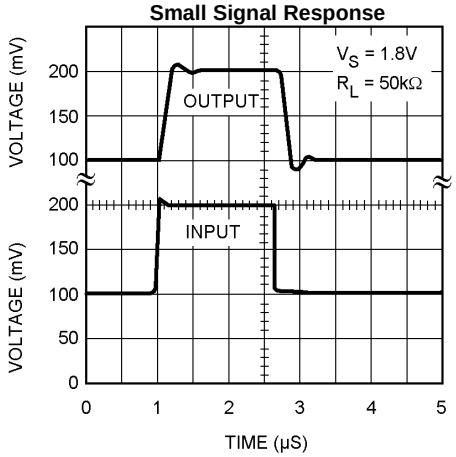


Figure 27.

Large Signal Response

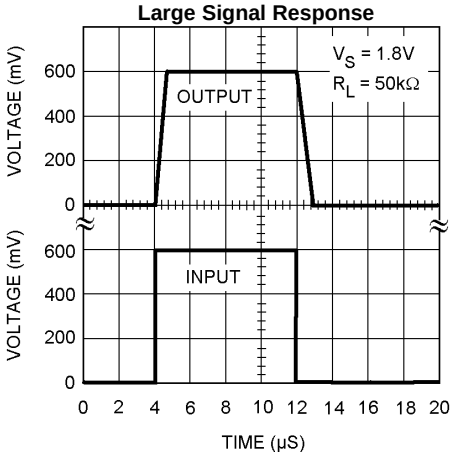


Figure 28.

Small Signal Response

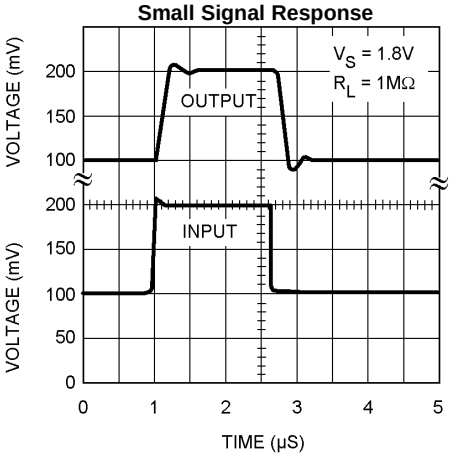


Figure 29.

Large Signal Response

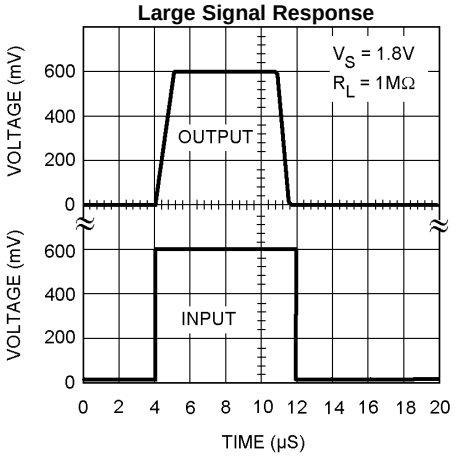


Figure 30.

Small Signal Response

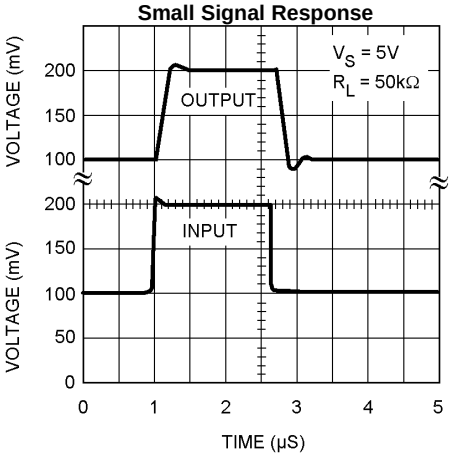


Figure 31.

Large Signal Response

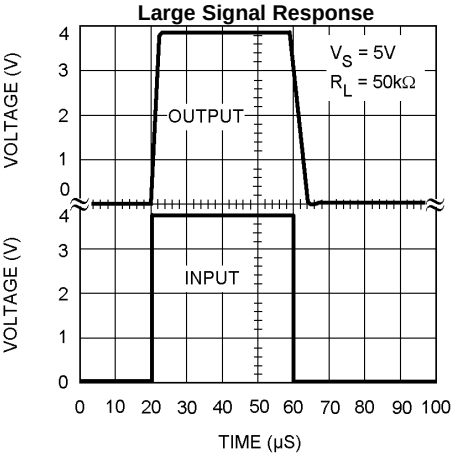


Figure 32.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C.

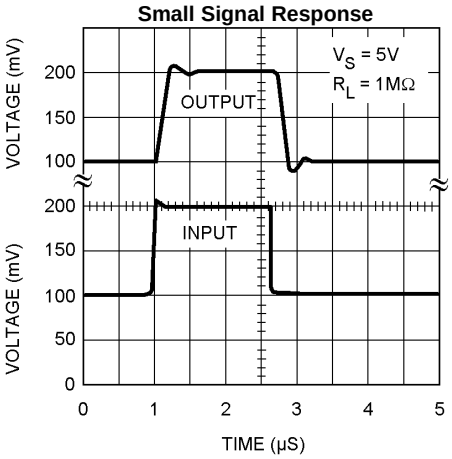


Figure 33.

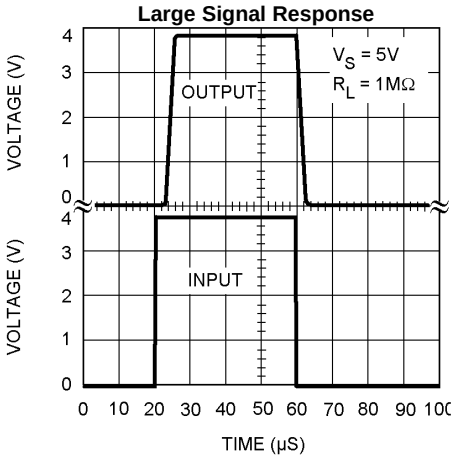


Figure 34.

APPLICATION HINTS

Compensating Input Capacitance

The high input resistance of the LMV301 op amp allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier circuit, Figure 35, the frequency of this pole is

$$fp = \frac{1}{2\pi C_S R_P} \tag{1}$$

where

- C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc.,
- R_P is the parallel combination of R_F and R_{IN}

This formula, as well as all formulae derived below, apply to inverting and non-inverting op amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10pF. If the frequency of the feedback pole is much higher than the “ideal” closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the “ideal” −3dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low frequency noise gain. To maintain stability a feedback capacitor will probably be needed if

$$(\frac{R_F}{R_{IN}} + 1) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S} \tag{2}$$

Where

$$\left(\frac{R_F}{R_{IN}} + 1\right) \tag{3}$$

is the amplifier's low frequency noise gain and GBW is the amplifier's gain bandwidth product.

An amplifier's low frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1\right) \tag{4}$$

regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S,} \tag{5}$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)} \tag{6}$$

If

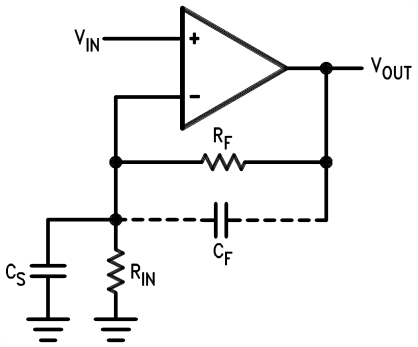
$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S} \tag{7}$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}} \tag{8}$$

Note that these capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F} \tag{9}$$



C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

Figure 35. General Operational Amplifier Circuit

Using the smaller capacitor will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

Capacitive Load Tolerance

Like many other op amps, the LMV301 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity gain follower. The load capacitance interacts with the op amp’s output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable. As shown in Figure 36, the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5pF to 10pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

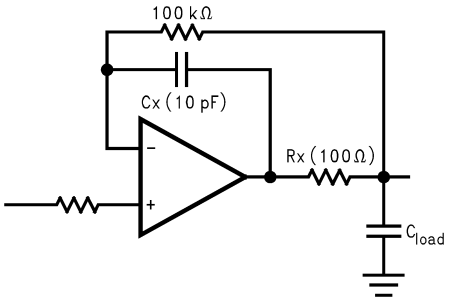


Figure 36. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 37). Typically a pull up resistor conducting 500µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor.

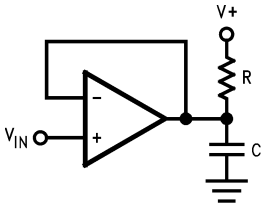


Figure 37. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 100pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the low bias current of the LMV301, typically less than 0.182pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptable low, because under conditions of the high humidity or dust or contamination, the surface leakage will be appreciable. To minimized the effect of any surface leakage, lay out a ring of foil completely surrounding the LMV301's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See Figure 38. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. The PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMV301's actual performance. However, if a guard ring is held within 5mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier performance. See Figure 39, Figure 40, and Figure 41 for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 42.

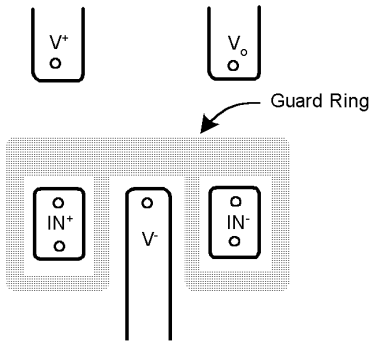


Figure 38. Example, using the LMV301, of Guard Ring in P.C. Board Layout

Guard Ring Connections

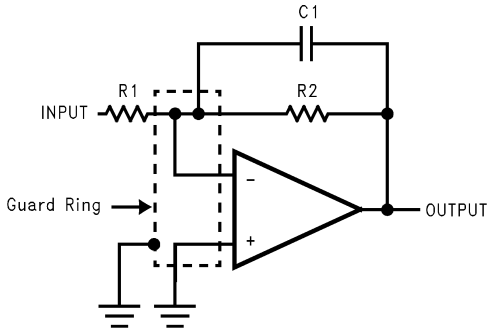


Figure 39. Inverting Amplifier

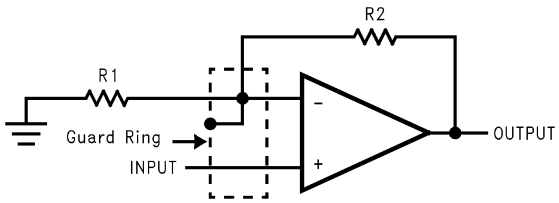


Figure 40. Non-Inverting Amplifier

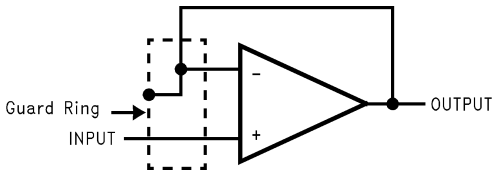


Figure 41. Follower

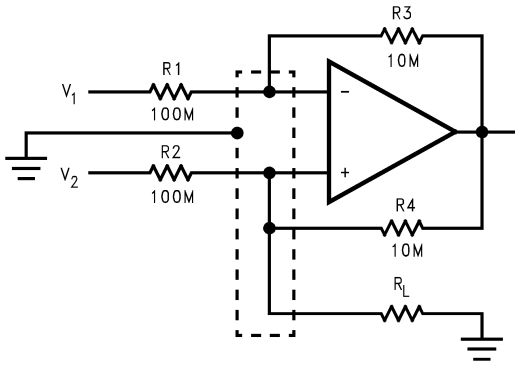
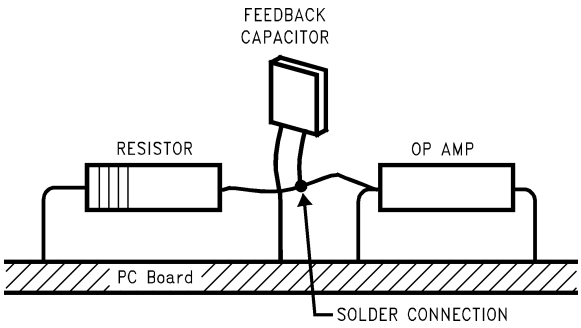


Figure 42. Howland Current Pump

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 43.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 43. Air Wiring

Typical Single-Supply Applications

(V_+ = 5.0 VDC)

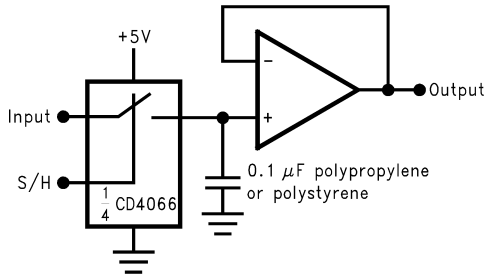


Figure 44. Low-Leakage Sample-and-Hold

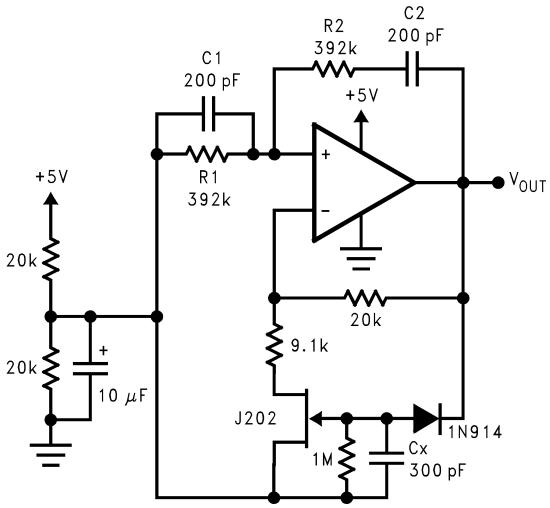


Figure 45. Sine-Wave Oscillator

Oscillator frequency is determined by R1, R2, C1, and C2:

$$fosc = 1/2\pi RC \quad (10)$$

where

- R = R1 = R2
- C = C1 = C2

This circuit, as shown, oscillates at 2.0kHz with a peak-to-peak output swing of 4.5V.

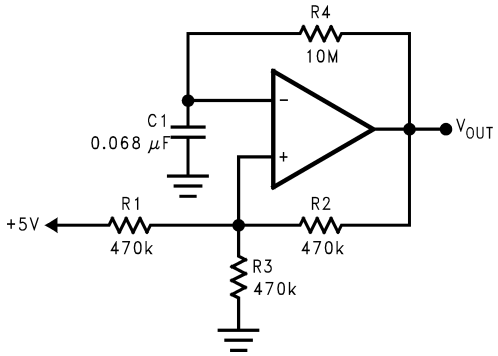


Figure 46. 1 Hz Square-Wave Oscillator

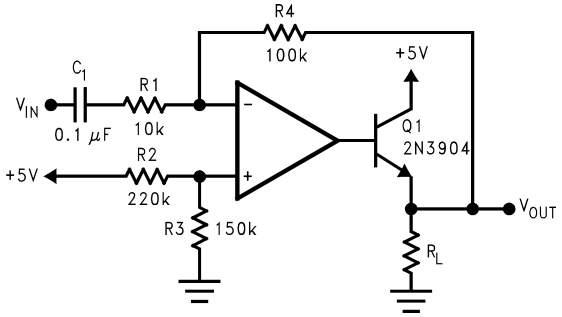
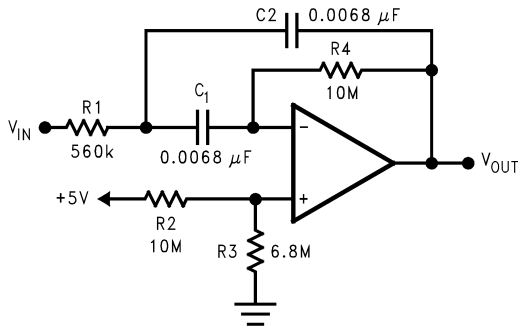
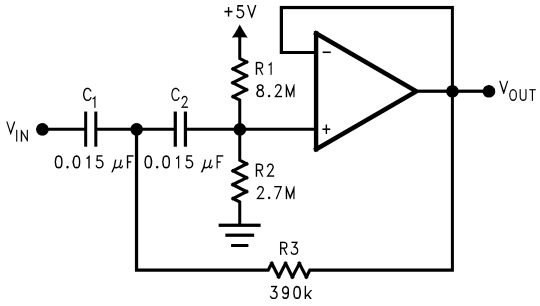


Figure 47. Power Amplifier



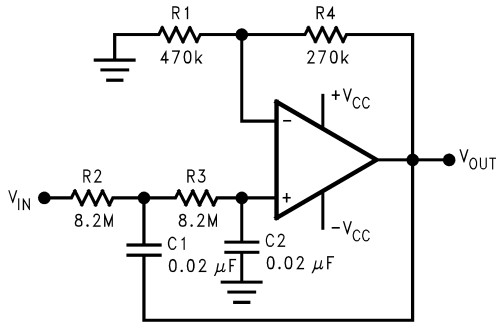
f_O = 10 Hz
Q = 2.1
Gain = −8.8

Figure 48. 10Hz Bandpass Filter



f_c = 10 Hz
d = 0.895
Gain = 1
2 dB passband ripple

Figure 49. 10 Hz High-Pass Filter



f_c = 1 Hz
d = 1.414
Gain = 1.57

Figure 50. 1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)

REVISION HISTORY

Changes from Original (May 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV301MG/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A48	Samples
LMV301MGX/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A48	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

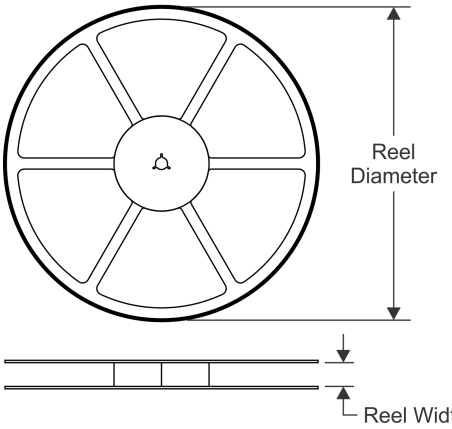
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

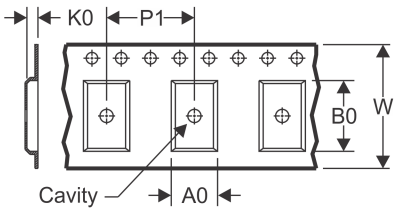
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

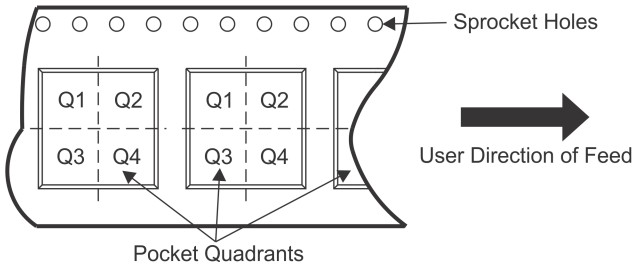


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

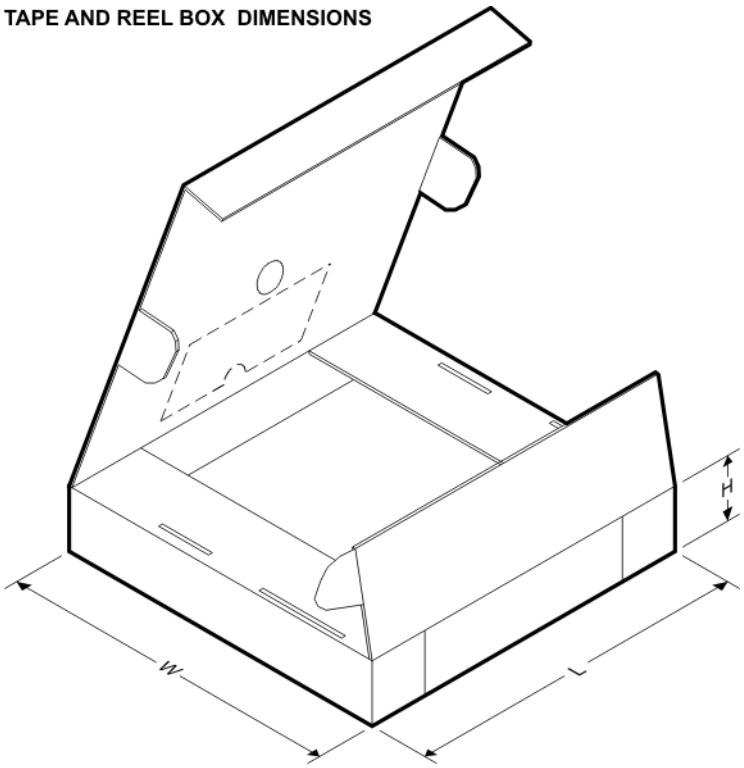
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV301MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV301MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

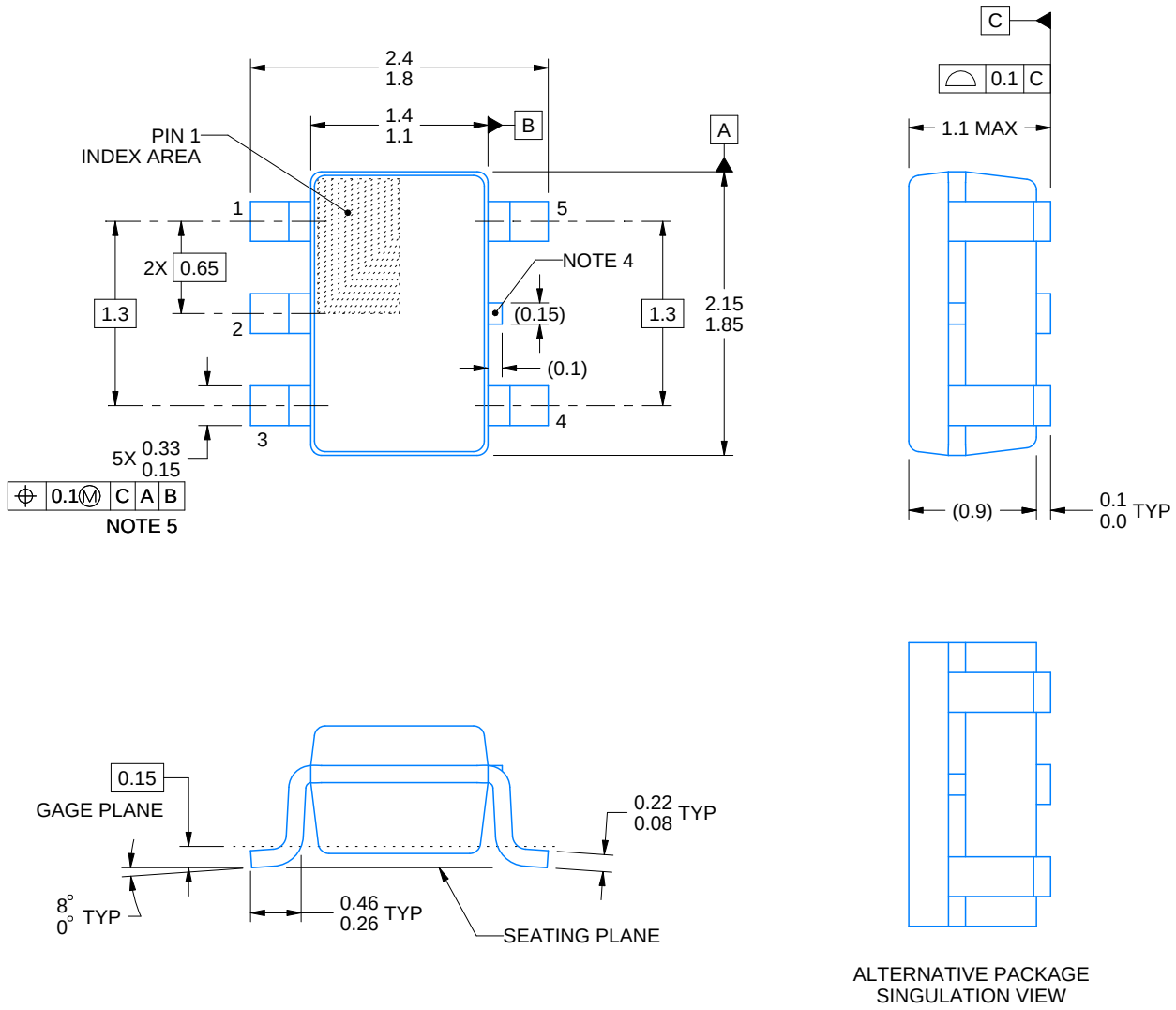
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV301MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV301MGX/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

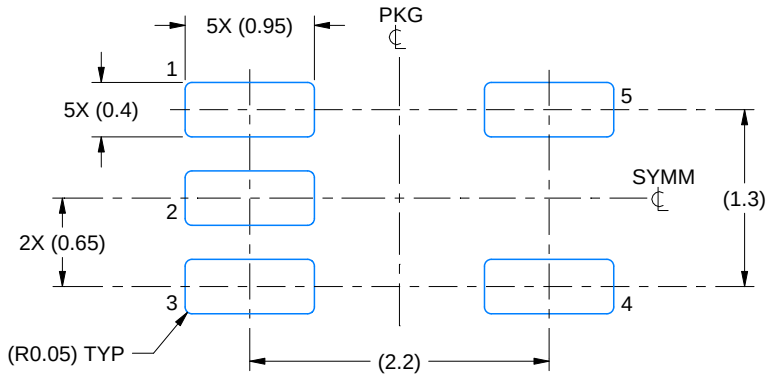
SMALL OUTLINE TRANSISTOR



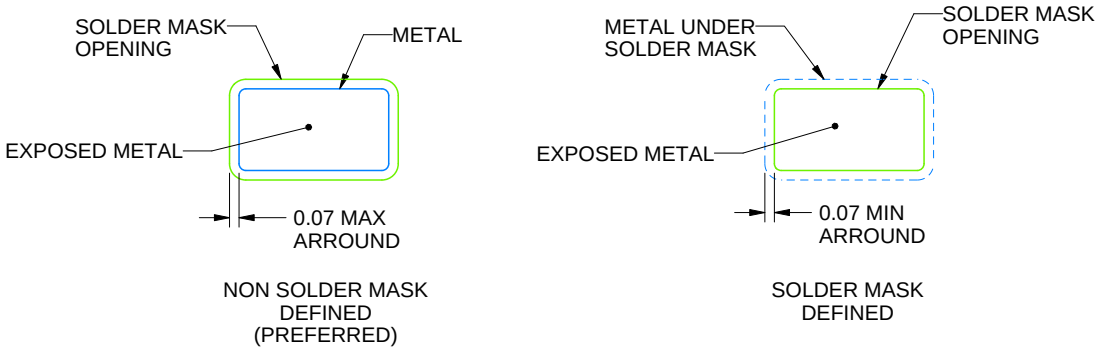
4214834/E 06/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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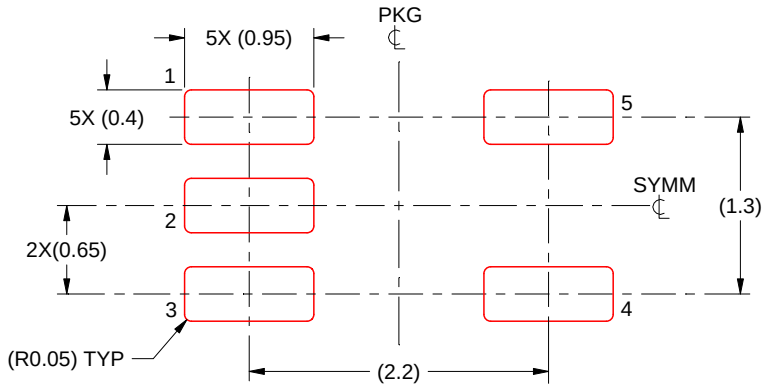
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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