

MSPM0G110x Mixed-Signal Microcontrollers

1 Features

- **Core**
 - Arm® 32-bit Cortex®-M0+ CPU with memory protection unit, frequency up to 80 MHz
- **Operating characteristics**
 - Extended temperature: –40°C up to 105°C
 - Wide supply voltage range: 1.62 V to 3.6 V
- **Memories**
 - Up to 128KB of flash memory with built-in error correction code (ECC)
 - Up to 32KB of SRAM with hardware parity
- **High-performance analog peripherals**
 - Two simultaneous sampling 12-bit 4-Msps analog-to-digital converters (ADCs) with up to 17 external channels
 - 14-bit effective resolution at 250-ksps with hardware averaging
 - One general-purpose amplifier (GPAMP)
 - Configurable 1.4-V or 2.5-V internal shared voltage reference (VREF)
 - Integrated temperature sensor
 - Integrated supply monitor
- **Optimized low-power modes**
 - RUN: 96 µA/MHz (CoreMark)
 - SLEEP: 467 µA at 4 MHz
 - STOP: 46 µA at 32 kHz
 - STANDBY: 1.5 µA with RTC and SRAM retention
 - SHUTDOWN: 80 nA with IO wakeup capability
- **Intelligent digital peripherals**
 - 7-channel DMA controller
 - Two 16-bit advanced control timers support dead band insertion and fault handling
 - Seven timers supporting up to 22 PWM channels
 - One 16-bit general purpose timer
 - One 16-bit general purpose timer supports QEI
 - Two 16-bit general-purpose timers support low-power operation in STANDBY mode
 - One 32-bit general-purpose timer
 - Two 16-bit advanced timers with deadband
 - Two window-watchdog timers
 - RTC with alarm and calendar mode
- **Enhanced communication interfaces**
 - Four UART interfaces; one supports LIN, IrDA, DALI, Smart Card, Manchester, and three support low-power operation in STANDBY mode
- Two I²C interfaces supporting up to FM+ (1 Mbit/s), SMBus, PMBus, and wakeup from STOP mode
- Two SPIs, one SPI supports up to 32 Mbits/s
- **Clock system**
 - Internal 4- to 32-MHz oscillator with up to ±3% accuracy (SYSOSC) across temperature
 - Phase-locked loop (PLL) up to 80 MHz
 - Internal 32-kHz oscillator (LFOSC)
 - External 4- to 48-MHz crystal oscillator (HFXT)
 - External 32-kHz crystal oscillator (LFXT)
 - External clock input
- **Data integrity and encryption**
 - Cyclic redundancy checker (CRC-16, CRC-32)
- **Flexible I/O features**
 - Up to 60 GPIOs
 - Two 5-V tolerant IOs
 - Two high-drive IOs with 20-mA drive strength
- **Development support**
 - 2-pin serial wire debug (SWD)
- **Package options**
 - 64-pin LQFP
 - 48-pin LQFP, VQFN
 - 32-pin VQFN
 - 28-pin VSSOP
 - 24-pin VQFN
- **Family members** (also see [Device Comparison](#))
 - MSPM0G1105: 32KB flash, 16KB RAM
 - MSPM0G1106: 64KB flash, 32KB RAM
 - MSPM0G1107: 128KB flash, 32KB RAM
- **Development kits and software** (also see [Tools and Software](#))
 - [LP-MSPM0G3507 LaunchPad™ development kit](#)
 - MSP Software Development Kit (SDK)

2 Applications

- [Motor control](#)
- [Home appliances](#)
- [Uninterruptible power supplies and inverters](#)
- [Electronic point of sale systems](#)
- [Medical and healthcare](#)
- [Test and measurement](#)
- [Factory automation and control](#)
- [Industrial transport](#)
- [Grid infrastructure](#)
- [Smart metering](#)
- [Communication modules](#)
- [Lighting](#)



3 Description

MSPM0G110x microcontrollers (MCUs) are part of the MSP highly-integrated, ultra-low-power 32-bit MCU family based on the enhanced Arm® Cortex®-M0+ 32-bit core platform operating at up to 80-MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 105°C, and operate with supply voltages ranging from 1.62 V to 3.6 V.

The MSPM0G110x devices provide up to 128KB embedded flash program memory with built-in error correction code (ECC) and up to 32KB SRAM with hardware parity option. The devices also incorporate a memory protection unit, 7-channel DMA, and a variety of high-performance analog peripherals such as two 12-bit 4-Msps ADCs, configurable internal shared voltage reference, and one general-purpose amplifier. These devices also offer intelligent digital peripherals such as two 16-bit advanced control timers, five general purpose timers (with one 16-bit general-purpose timer for QEI interface, two 16-bit general-purpose timers for STANDBY mode, and one 32-bit general-purpose timer), two windowed-watchdog timers, and one RTC with alarm and calendar mode. These devices provide data integrity and encryption peripherals (CRC) and enhanced communication interfaces (four UART, two I2C, two SPI).

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers find the MCU that meets their project's needs. The MSPM0 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

MSPM0G110x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a [LaunchPad](#) available for purchase. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of [Code Composer Studio™](#) IDE desktop and cloud version within the [TI Resource Explorer](#). MSPM0 MCUs are also supported by extensive online collateral, training with [MSP Academy](#), and online support through the [TI E2E™ support forums](#).

For complete module descriptions, see the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See [MSP430™ System-Level ESD Considerations](#) for more information. The principles in this application note are applicable to MSPM0 MCUs.

4 Functional Block Diagram

Figure 4-1 shows the MSPM0G110x functional block diagram.

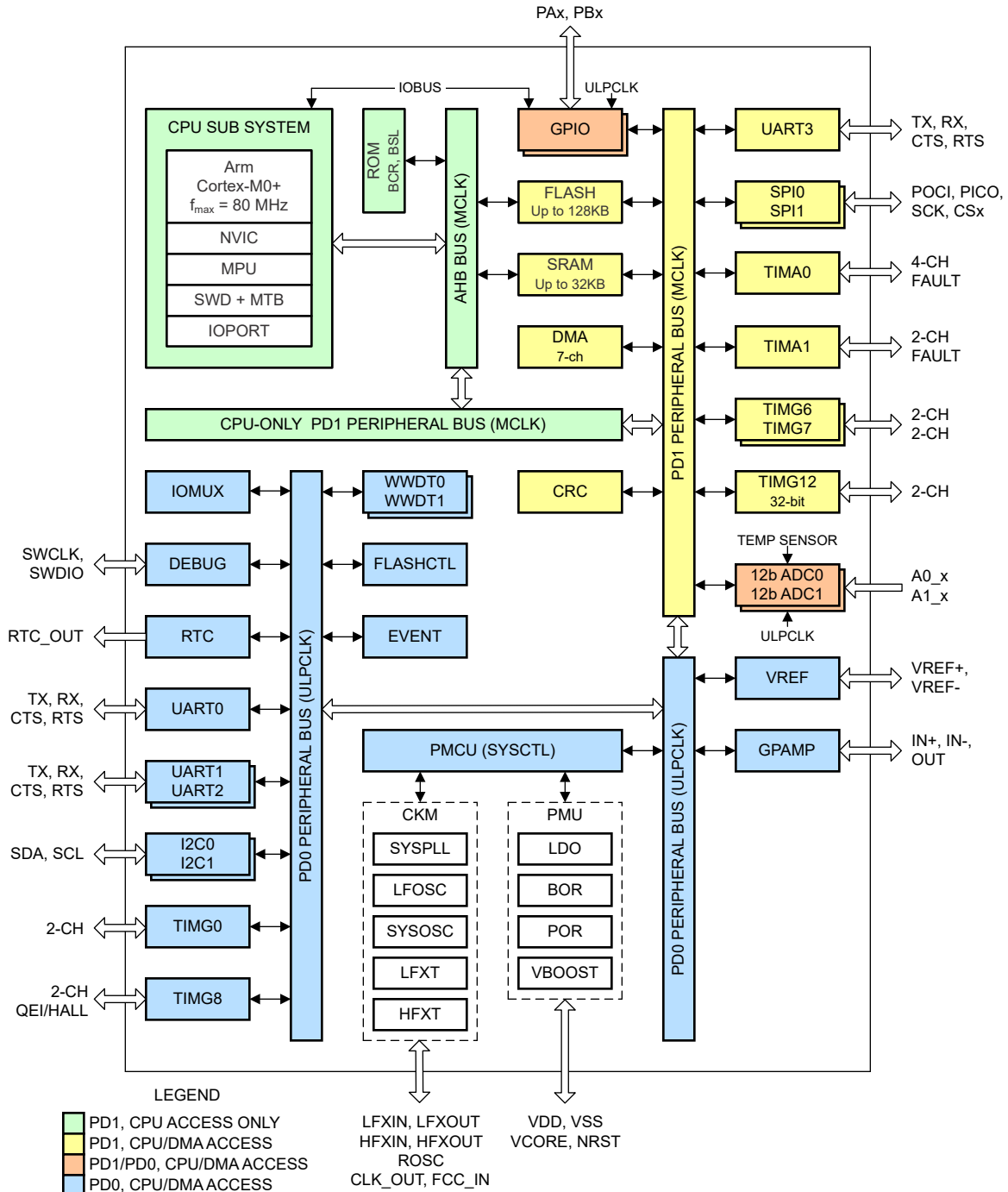


Figure 4-1. MSPM0G110x Functional Block Diagram

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5 Device Comparison

Table 5-1. Device Comparison

| DEVICE NAME ^{(1) (4)} | FLASH / SRAM (KB) | QUAL ⁽²⁾ | ADC / CHAN | GPAMP | UART / I2C / SPI | TIMA | TIMG | GPIO | PACKAGE [PACKAGE SIZE] ⁽³⁾ |
|--------------------------------|-------------------|---------------------|------------|-------|------------------|------|------|------|---------------------------------------|
| MSPM0G1106xPM | 64 / 32 | T | 2 / 17 | 1 | 4 / 2 / 2 | 2 | 5 | 60 | 64 LQFP [12 mm × 12 mm] |
| MSPM0G1107xPM | 128 / 32 | | | | | | | | |
| MSPM0G1105xPT | 32 / 16 | T | 2 / 16 | 1 | 4 / 2 / 2 | 2 | 5 | 44 | 48 LQFP [9 mm × 9 mm] |
| MSPM0G1106xPT | 64 / 32 | | | | | | | | |
| MSPM0G1107xPT | 128 / 32 | | | | | | | | |
| MSPM0G1105xRGZ | 32 / 16 | T | 2 / 16 | 1 | 4 / 2 / 2 | 2 | 5 | 44 | 48 VQFN [7 mm × 7 mm] |
| MSPM0G1106xRGZ | 64 / 32 | | | | | | | | |
| MSPM0G1107xRGZ | 128 / 32 | | | | | | | | |
| MSPM0G1106xRHB | 64 / 32 | T | 2 / 11 | 1 | 4 / 2 / 2 | 2 | 5 | 28 | 32 VQFN [5 mm × 5 mm] |
| MSPM0G1107xRHB | 128 / 32 | | | | | | | | |
| MSPM0G1107xDGS28 | 128 / 32 | T | 2 / 11 | 1 | 4 / 2 / 2 | 2 | 5 | 24 | 28 VSSOP [7.1 mm × 4.9 mm] |
| MSPM0G1107xRGE | 128 / 32 | T | 2 / 9 | 1 | 4 / 2 / 2 | 2 | 5 | 20 | 24 VQFN [4 mm × 4 mm] |

- (1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in [Section 11](#), or see the [TI website](#).
- (2) Device Qualifications:
 - T = –40°C to 105°C
- (3) The package size (length × width) is a nominal value and includes pins, where applicable. For the package dimensions with tolerances, see [Section 11](#).
- (4) For more information about the device name, see [Section 10.2](#).

6 Pin Configuration and Functions

The [System Configuration tool](#) provides a graphical interface to enable, configurable, and generate initialization code for pin multiplexing and simplifying pin settings. The following pin diagrams show the primary peripheral functions, some of the integrated device features, and available clock signals to simplify the device pinout. For full descriptions of the pin functions, see the *Pin Attributes* and *Signal Descriptions* sections.

6.1 Pin Diagrams

- Power
- Reset
- High-Speed I/O (HSIO)
- 5-V Tolerant Open-Drain I/O (ODIO)
- High-Drive I/O (HDIO)

Figure 6-1. Pin Diagram Color Coding

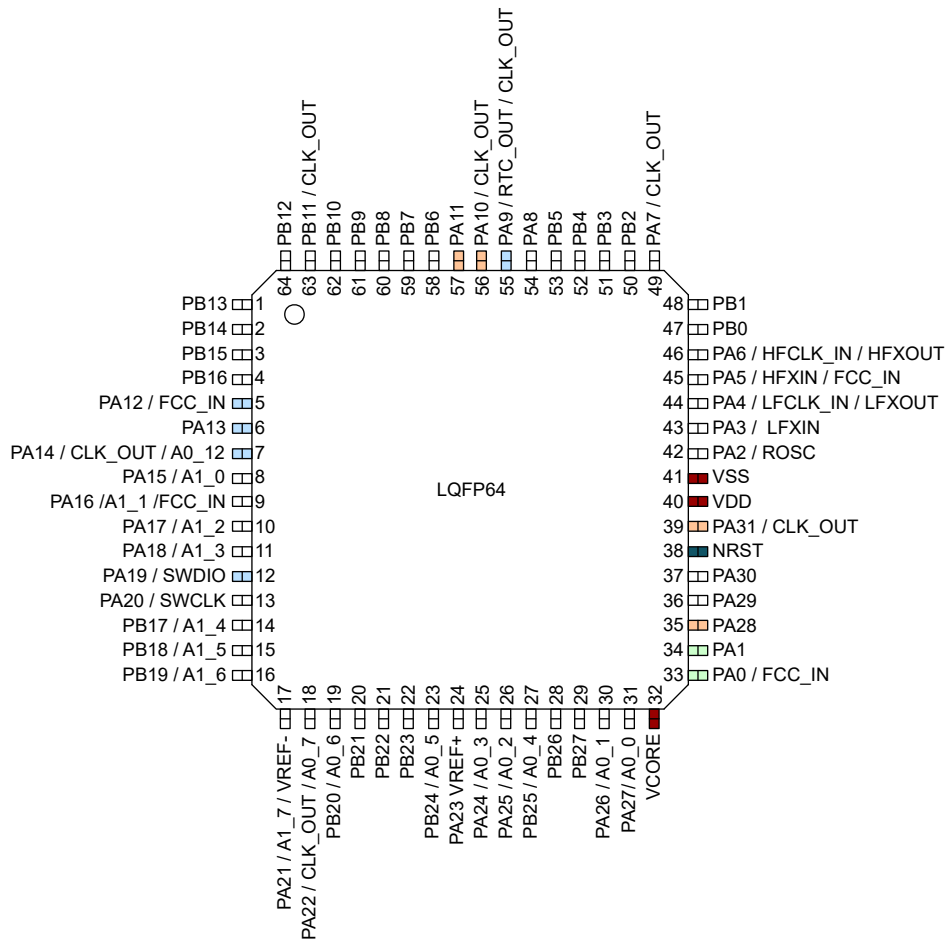


Figure 6-2. 64-Pin PM (LQFP) (Top View)

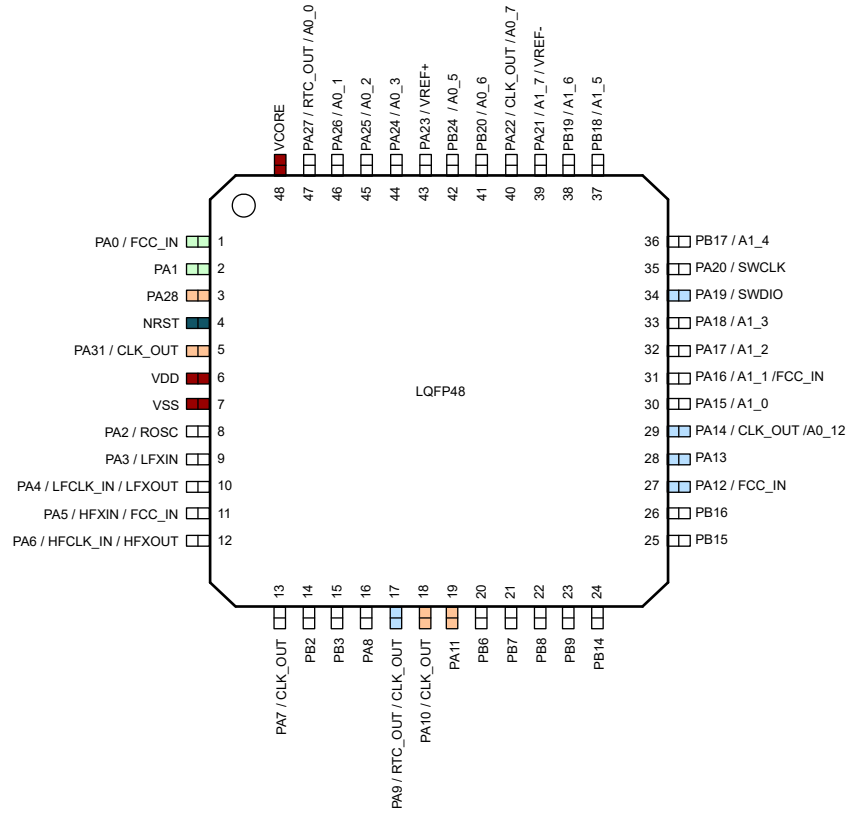


Figure 6-3. 48-Pin PT (LQFP) (Top View)

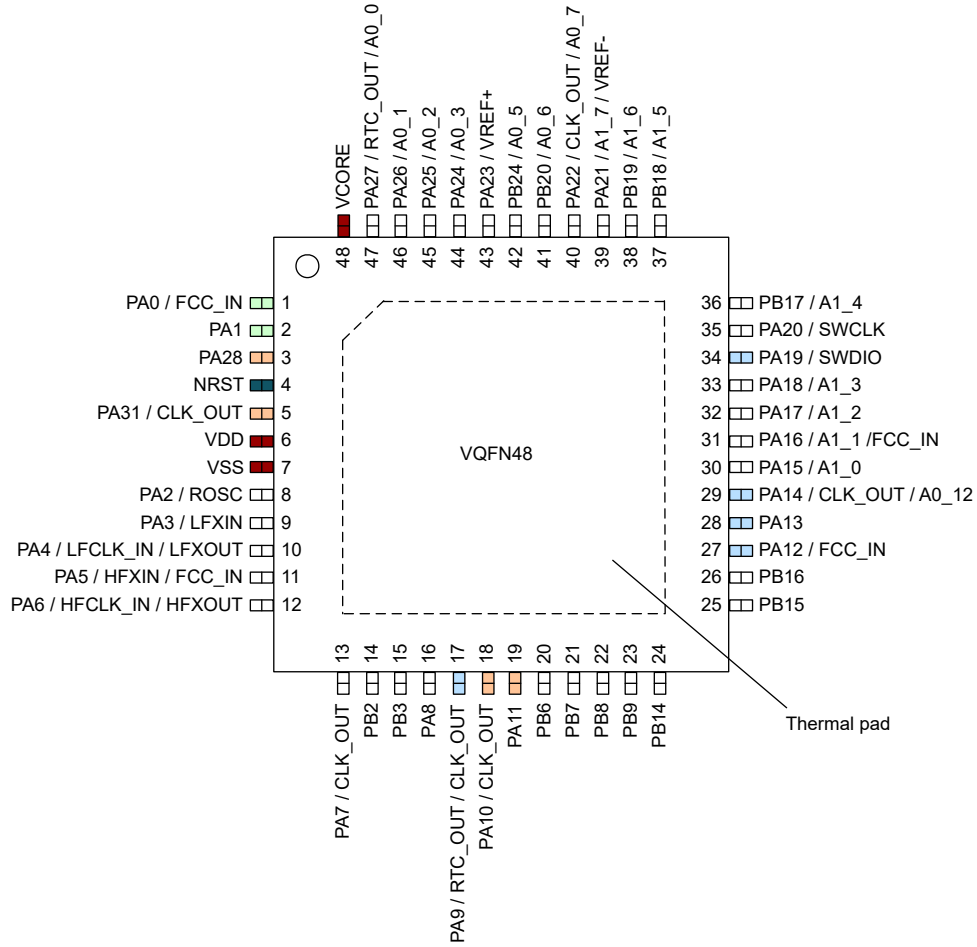


Figure 6-4. 48-Pin RGZ (VQFN) (Top View)

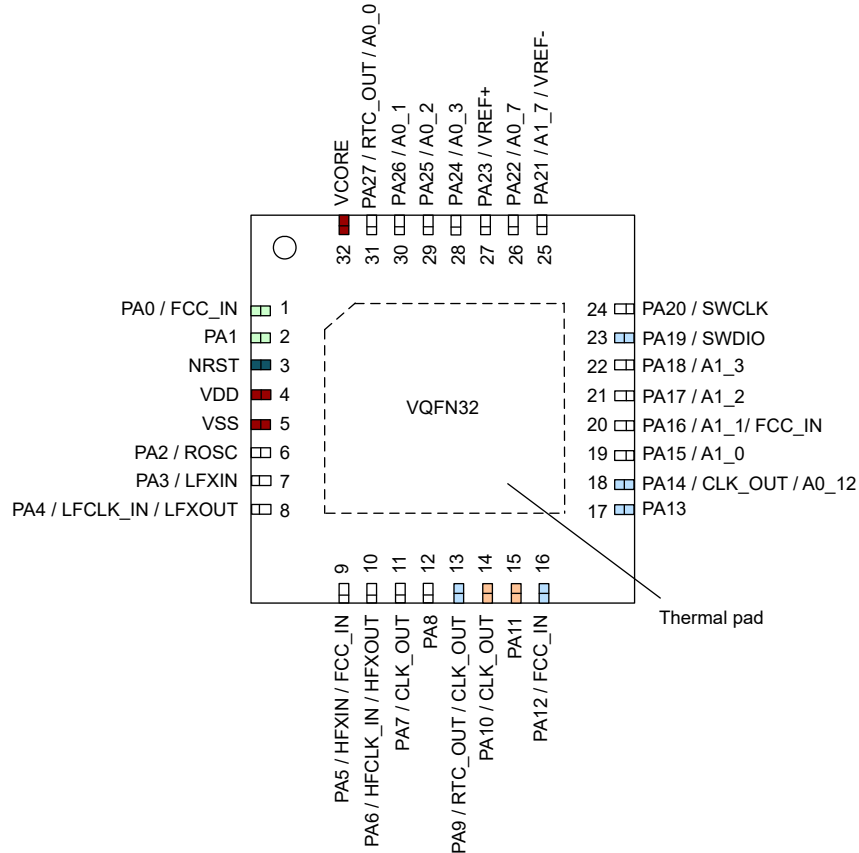


Figure 6-5. 32-Pin RHB (VQFN) (Top View)

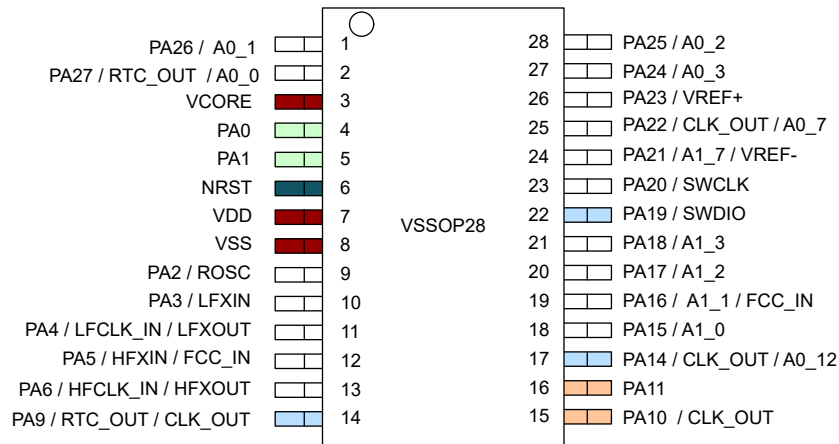


Figure 6-6. 28-Pin DGS28 (VSSOP) (Top View)

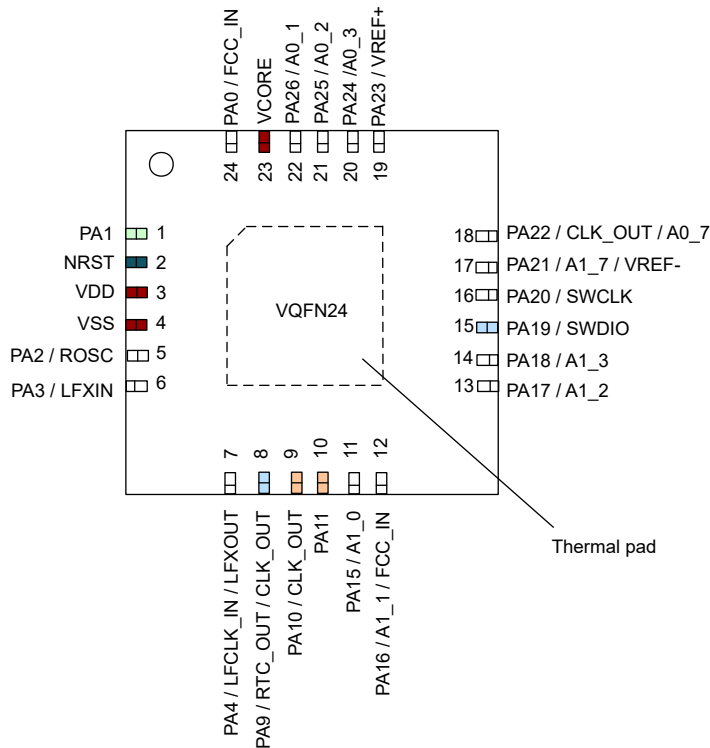


Figure 6-7. 24-Pin RGE (VQFN) (Top View)

Note

For full pin configuration and functions for each package option, refer to [Pin Attributes](#) and [Signal Descriptions](#).

6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) which allows users to configure the desired *Pin Function* using the PINCM.PF control bits.

Table 6-1. Pin Attributes

| PINCMx | PIN NAME | SIGNAL NAMES | | PIN NUMBER | | | | | IO STRUCTURE |
|--------|----------|--------------|--|------------|---------------|---------|----------|---------|-------------------------|
| | | ANALOG | DIGITAL [PIN FUNCTION] ⁽¹⁾ | 64 LQFP | 48 LQFP, VQFN | 32 VQFN | 28 VSSOP | 24 VQFN | |
| N/A | | | VDD | 40 | 6 | 4 | 7 | 3 | Power |
| N/A | | | VSS | 41 | 7 | 5 | 8 | 4 | Power |
| N/A | | | VCORE | 32 | 48 | 32 | 3 | 23 | Power |
| N/A | | | NRST | 38 | 4 | 3 | 6 | 2 | Reset |
| 1 | PA0 | | UART0_TX [2] / I2C0_SDA [3] / TIMA0_C0 [4] / TIMA_FAL1 [5] / TIMG8_C1 [6] / FCC_IN [7] / (Default BSL I2C_SDA) | 33 | 1 | 1 | 4 | 24 | 5-V tolerant open drain |
| 2 | PA1 | | UART0_RX [2] / I2C0_SCL [3] / TIMA0_C1 [4] / TIMA_FAL2 [5] / TIMG8_IDX [6] / TIMG8_C0 [7] / (Default BSL I2C_SCL) | 34 | 2 | 2 | 5 | 1 | 5-V tolerant open drain |
| 7 | PA2 | ROSC | TIMG8_C1 [2] / SPI0_CS0 [3] / TIMG7_C1 [4] / SPI1_CS0 [5] | 42 | 8 | 6 | 9 | 5 | Standard |
| 8 | PA3 | LFXIN | TIMG8_C0 [2] / SPI0_CS1 [3] / UART2_CTS [4] / TIMA0_C2 [5] / TIMG7_C0 [7] / TIMA0_C1 [8] / I2C1_SDA [9] | 43 | 9 | 7 | 10 | 6 | Standard |
| 9 | PA4 | LFXOUT | TIMG8_C1 [2] / SPI0_POCI [3] / UART2_RTS [4] / TIMA0_C3 [5] / LFCLK_IN [6] / TIMG7_C1 [7] / TIMA0_C1N [8] / I2C1_SCL [9] | 44 | 10 | 8 | 11 | 7 | Standard |
| 10 | PA5 | HFXIN | TIMG8_C0 [2] / SPI0_PICO [3] / TIMA_FAL1 [4] / TIMG0_C0 [5] / TIMG6_C0 [6] / FCC_IN [7] | 45 | 11 | 9 | 12 | - | Standard |
| 11 | PA6 | HFXOUT | TIMG8_C1 [2] / SPI0_SCK [3] / TIMA_FAL0 [4] / TIMG0_C1 [5] / HFCLK_IN [6] / TIMG6_C1 [7] / TIMA0_C2N [8] | 46 | 12 | 10 | 13 | - | Standard |
| 14 | PA7 | | CLK_OUT [3] / TIMG8_C0 [4] / TIMA0_C2 [5] / TIMG8_IDX [6] / TIMG7_C1 [7] / TIMA0_C1 [8] | 49 | 13 | 11 | - | - | Standard |
| 19 | PA8 | | UART1_TX [2] / SPI0_CS0 [3] / UART0_RTS [4] / TIMA0_C0 [5] / TIMA1_CON [6] | 54 | 16 | 12 | - | - | Standard |
| 20 | PA9 | | UART1_RX [2] / SPI0_PICO [3] / UART0_CTS [4] / TIMA0_C1 [5] / RTC_OUT [6] / TIMA0_C0N [7] / TIMA1_C1N [8] / CLK_OUT [9] | 55 | 17 | 13 | 14 | 8 | High-Speed |
| 21 | PA10 | | UART0_TX [2] / SPI0_POCI [3] / I2C0_SDA [4] / TIMA1_C0 [5] / TIMG12_C0 [6] / TIMA0_C2 [7] / I2C1_SDA [8] / CLK_OUT [9] / (Default BSL UART_TX) | 56 | 18 | 14 | 15 | 9 | High-Drive |
| 22 | PA11 | | UART0_RX [2] / SPI0_SCK [3] / I2C0_SCL [4] / TIMA1_C1 [5] / TIMA0_C2N [6] / I2C1_SCL [7] / (Default BSL UART_RX) | 57 | 19 | 15 | 16 | 10 | High-Drive |
| 34 | PA12 | | UART3_CTS [2] / SPI0_SCK [3] / TIMG0_C0 [4] / TIMA0_C3 [6] / FCC_IN [7] | 5 | 27 | 16 | - | - | High-Speed |
| 35 | PA13 | | UART3_RTS [2] / SPI0_POCI [3] / UART3_RX [4] / TIMG0_C1 [5] / TIMA0_C3N [7] | 6 | 28 | 17 | - | - | High-Speed |

Table 6-1. Pin Attributes (continued)

| PINCMx | PIN NAME | SIGNAL NAMES | | PIN NUMBER | | | | | IO STRUCTURE |
|--------|----------|------------------|--|------------|---------------|---------|----------|---------|-----------------------------------|
| | | ANALOG | DIGITAL [PIN FUNCTION] ⁽¹⁾ | 64 LQFP | 48 LQFP, VQFN | 32 VQFN | 28 VSSOP | 24 VQFN | |
| 36 | PA14 | A0_12 | UART0_CTS [2] / SPI0_PICO [3] / UART3_TX [4] / TIMG12_C0 [5] / CLK_OUT [6] | 7 | 29 | 18 | 17 | - | High-Speed |
| 37 | PA15 | A1_0 | UART0_RTS [2] / SPI1_CS2 [3] / I2C1_SCL [4] / TIMA1_C0 [5] / TIMG8_IDX [6] / TIMA1_CON [7] / TIMA0_C2 [8] | 8 | 30 | 19 | 18 | 11 | Standard |
| 38 | PA16 | A1_1 | SPI1_POCI [3] / I2C1_SDA [4] / TIMA1_C1 [5] / TIMA1_C1N [6] / TIMA0_C2N [7] / FCC_IN [8] | 9 | 31 | 20 | 19 | 12 | Standard |
| 39 | PA17 | A1_2 | UART1_TX [2] / SPI1_SCK [3] / I2C1_SCL [4] / TIMA0_C3 [5] / TIMG7_C0 [6] / TIMA1_C0 [7] | 10 | 32 | 21 | 20 | 13 | Standard with wake ⁽²⁾ |
| 40 | PA18 | A1_3 / GPAMP_IN- | UART1_RX [2] / SPI1_PICO [3] / I2C1_SDA [4] / TIMA0_C3N [5] / TIMG7_C1 [6] / TIMA1_C1 [7]/Default BSL_Invoke | 11 | 33 | 22 | 21 | 14 | Standard with wake ⁽²⁾ |
| 41 | PA19 | | SWDIO [2] | 12 | 34 | 23 | 22 | 15 | High-Speed |
| 42 | PA20 | | SWCLK [2] | 13 | 35 | 24 | 23 | 16 | Standard |
| 46 | PA21 | A1_7 / VREF- | UART2_TX [2] / TIMG8_C0 [3] / UART1_CTS [4] / TIMA0_C0 [5] / TIMG6_C0 [6] | 17 | 39 | 25 | 24 | 17 | Standard |
| 47 | PA22 | A0_7 / GPAMP_OUT | UART2_RX [2] / TIMG8_C1 [3] / UART1_RTS [4] / TIMA0_C1 [5] / CLK_OUT [6] / TIMA0_CON [7] / TIMG6_C1 [8] | 18 | 40 | 26 | 25 | 18 | Standard |
| 53 | PA23 | VREF+ | UART2_TX [2] / SPI0_CS3 [3] / TIMA0_C3 [4] / TIMG0_C0 [5] / UART3_CTS [6] / TIMG7_C0 [7] / TIMG8_C0 [8] | 24 | 43 | 27 | 26 | 19 | Standard |
| 54 | PA24 | A0_3 | UART2_RX [2] / SPI0_CS2 [3] / TIMA0_C3N [4] / TIMG0_C1 [5] / UART3_RTS [6] / TIMG7_C1 [7] / TIMA1_C1 [8] | 25 | 44 | 28 | 27 | 20 | Standard |
| 55 | PA25 | A0_2 | UART3_RX [2] / SPI1_CS3 [3] / TIMG12_C1 [4] / TIMA0_C3 [5] / TIMA0_C1N [6] | 26 | 45 | 29 | 28 | 21 | Standard |
| 59 | PA26 | A0_1 / GPAMP_IN+ | UART3_TX [2] / SPI1_CS0 [3] / TIMG8_C0 [4] / TIMA_FAL0 [5] / TIMG7_C0 [7] | 30 | 46 | 30 | 1 | 22 | Standard |
| 60 | PA27 | A0_0 | RTC_OUT [2] / SPI1_CS1 [3] / TIMG8_C1 [4] / TIMA_FAL2 [5] / TIMG7_C1 [7] | 31 | 47 | 31 | 2 | | Standard |
| 3 | PA28 | | UART0_TX [2] / I2C0_SDA [3] / TIMA0_C3 [4] / TIMA_FAL0 [5] / TIMG7_C0 [6] / TIMA1_C0 [7] | 35 | 3 | - | - | - | High-Drive |
| 4 | PA29 | | I2C1_SCL [2] / UART2_RTS [3] / TIMG8_C0 [4] / TIMG6_C0 [5] | 36 | - | - | - | - | Standard |
| 5 | PA30 | | I2C1_SDA [2] / UART2_CTS [3] / TIMG8_C1 [4] / TIMG6_C1 [5] | 37 | - | - | - | - | Standard |
| 6 | PA31 | | UART0_RX [2] / I2C0_SCL [3] / TIMA0_C3N [4] / TIMG12_C1 [5] / CLK_OUT [6] / TIMG7_C1 [7] / TIMA1_C1 [8] | 39 | 5 | - | - | - | High-Drive |
| 12 | PB0 | | UART0_TX [2] / SPI1_CS2 [3] / TIMA1_C0 [4] / TIMA0_C2 [5] | 47 | - | - | - | - | Standard |
| 13 | PB1 | | UART0_RX [2] / SPI1_CS3 [3] / TIMA1_C1 [4] / TIMA0_C2N [5] | 48 | - | - | - | - | Standard |
| 15 | PB2 | | UART3_TX [2] / UART2_CTS [3] / I2C1_SCL [4] / TIMA0_C3 [5] / UART1_CTS [6] / TIMG6_C0 [7] / TIMA1_C0 [8] | 50 | 14 | - | - | - | Standard |

Table 6-1. Pin Attributes (continued)

| PINCMx | PIN NAME | SIGNAL NAMES | | PIN NUMBER | | | | | IO STRUCTURE |
|--------|----------|--------------|---|------------|---------------|---------|----------|---------|--------------|
| | | ANALOG | DIGITAL [PIN FUNCTION] ⁽¹⁾ | 64 LQFP | 48 LQFP, VQFN | 32 VQFN | 28 VSSOP | 24 VQFN | |
| 16 | PB3 | | UART3_RX [2] / UART2_RTS [3] / I2C1_SDA [4] / TIMA0_C3N[5] / UART1_RTS [6] / TIMG6_C1 [7] / TIMA1_C1 [8] | 51 | 15 | - | - | - | Standard |
| 17 | PB4 | | UART1_TX [2] / UART3_CTS [3] / TIMA1_C0 [4] / TIMA0_C2 [5] / TIMA1_CON [6] | 52 | - | - | - | - | Standard |
| 18 | PB5 | | UART1_RX [2] / UART3_RTS [3] / TIMA1_C1 [4] / TIMA0_C2N [5] / TIMA1_C1N [6] | 53 | - | - | - | - | Standard |
| 23 | PB6 | | UART1_TX [2] / SPI1_CS0 [3] / SPI0_CS1 [4] / TIMG8_C0 [5] / UART2_CTS [6] / TIMG6_C0 [7] / TIMA1_CON [8] | 58 | 20 | - | - | - | Standard |
| 24 | PB7 | | UART1_RX [2] / SPI1_POCI [3] / SPI0_CS2 [4] / TIMG8_C1 [5] / UART2_RTS [6] / TIMG6_C1 [7] / TIMA1_C1N [8] | 59 | 21 | - | - | - | Standard |
| 25 | PB8 | | UART1_CTS [2] / SPI1_PICO [3] / TIMA0_C0 [4] | 60 | 22 | - | - | - | Standard |
| 26 | PB9 | | UART1_RTS [2] / SPI1_SCK [3] / TIMA0_C1 [4] / TIMA0_CON [5] | 61 | 23 | - | - | - | Standard |
| 27 | PB10 | | TIMG0_C0 [2] / TIMG8_C0 [3] / TIMG6_C0 [5] | 62 | - | - | - | - | Standard |
| 28 | PB11 | | TIMG0_C1 [2] / TIMG8_C1 [3] / CLK_OUT [4] / TIMG6_C1 [5] | 63 | - | - | - | - | Standard |
| 29 | PB12 | | UART3_TX [2] / TIMA0_C2 [3] / TIMA_FAL1 [4] / TIMA0_C1 [5] | 64 | - | - | - | - | Standard |
| 30 | PB13 | | UART3_RX [2] / TIMA0_C3 [3] / TIMG12_C0 [4] / TIMA0_C1N [5] | 1 | - | - | - | - | Standard |
| 31 | PB14 | | SPI1_CS3 [2] / SPI1_POCI [3] / SPI0_CS3 [4] / TIMG12_C1 [5] / TIMG8_IDX [6] / TIMA0_C0 [7] | 2 | 24 | - | - | - | Standard |
| 32 | PB15 | | UART2_TX [2] / SPI1_PICO [3] / UART3_CTS [4] / TIMG8_C0 [5] / TIMG7_C0 [6] | 3 | 25 | - | - | - | Standard |
| 33 | PB16 | | UART2_RX [2] / SPI1_SCK [3] / UART3_RTS [4] / TIMG8_C1 [5] / TIMG7_C1 [6] | 4 | 26 | - | - | - | Standard |
| 43 | PB17 | A1_4 | UART2_TX [2] / SPI0_PICO [3] / SPI1_CS1 [4] / TIMA1_C0 [5] / TIMA0_C2 [6] | 14 | 36 | - | - | - | Standard |
| 44 | PB18 | A1_5 | UART2_RX [2] / SPI0_SCK [3] / SPI1_CS2 [4] / TIMA1_C1 [5] / TIMA0_C2N [6] | 15 | 37 | - | - | - | Standard |
| 45 | PB19 | A1_6 | SPI0_POCI [3] / TIMG8_C1 [4] / UART0_CTS [5] / TIMG7_C1 [6] | 16 | 38 | - | - | - | Standard |
| 48 | PB20 | A0_6 | SPI0_CS2 [2] / SPI1_CS0 [3] / TIMA0_C2 [4] / TIMG12_C0 [5] / TIMA_FAL1 [6] / TIMA0_C1 [7] / TIMA1_C1N [8] | 19 | 41 | - | - | - | Standard |
| 49 | PB21 | | SPI1_POCI [2] / TIMG8_C0 [3] | 20 | - | - | - | - | Standard |
| 50 | PB22 | | SPI1_PICO [2] / TIMG8_C1 [3] | 21 | - | - | - | - | Standard |
| 51 | PB23 | | SPI1_SCK [2] / TIMA_FAL0 [4] | 22 | - | - | - | - | Standard |
| 52 | PB24 | A0_5 | SPI0_CS3 [2] / SPI0_CS1 [3] / TIMA0_C3 [4] / TIMG12_C1 [5] / TIMA0_C1N [6] / TIMA1_CON [7] | 23 | 42 | - | - | - | Standard |
| 56 | PB25 | A0_4 | UART0_CTS [2] / SPI0_CS0 [3] / TIMA_FAL2 [4] | 27 | - | - | - | - | Standard |
| 57 | PB26 | | UART0_RTS [2] / SPI0_CS1 [3] / TIMA0_C3 [4] / TIMG6_C0 [5] | 28 | - | - | - | - | Standard |

Table 6-1. Pin Attributes (continued)

| PINCMx | PIN NAME | SIGNAL NAMES | | | | PIN NUMBER | | | | | IO STRUCTURE |
|--------|----------|--------------|--|--|--|------------|---------------|---------|----------|---------|--------------|
| | | ANALOG | DIGITAL [PIN FUNCTION] ⁽¹⁾ | | | 64 LQFP | 48 LQFP, VQFN | 32 VQFN | 28 VSSOP | 24 VQFN | |
| 58 | PB27 | | SPI1_CS1 [3] / TIMA0_C3N [4] / TIMG6_C1 [5] / TIMA1_C1 [6] | | | 29 | - | - | - | - | Standard |

- (1) Set PINCM.PF and PINCM.PC in IOMUX to 0 for analog functions (for example, OPA inputs/outputs or COMP inputs). Each digital I/O on a device is mapped to a specific Pin Control Management register (PINCMx) that lets users configure the desired pin function using the PINCM.PF control bits.
- (2) Standard with Wake allows the I/O to wake up the device from the lowest low-power mode of SHUTDOWN. All I/O can be configured to wakeup the MCU from higher low-power modes. See section *GPIO FastWake* in the *MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual* for details.

Table 6-2. Digital IO Features by IO Type

| IO STRUCTURE | INVERSION CONTROL | DRIVE STRENGTH CONTROL | HYSTERESIS CONTROL | PULLUP RESISTOR | PULLDOWN RESISTOR | WAKEUP LOGIC |
|---|-------------------|------------------------|--------------------|-----------------|-------------------|--------------|
| Standard-drive | Y | | | Y | Y | |
| Standard-drive with wake ⁽¹⁾ | Y | | | Y | Y | Y |
| High-drive | Y | Y | | Y | Y | Y |
| High-speed | Y | Y | | Y | Y | |
| 5-V tolerant open drain | Y | | Y | | Y | Y |

6.3 Signal Descriptions

Table 6-3. Signal Descriptions

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------|-------------|------------------------|------------|--------|----------|---------|-------------------------|-------------------------------------|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS28 | 24 VQFN | | |
| ADC | A0_0 | 31 | 47 | 31 | 2 | - | I | ADC0 analog input 0 |
| | A0_1 | 30 | 46 | 30 | 1 | 22 | I | ADC0 analog input 1 |
| | A0_2 | 26 | 45 | 29 | 28 | 21 | I | ADC0 analog input 2 |
| | A0_3 | 25 | 44 | 28 | 27 | 20 | I | ADC0 analog input 3 |
| | A0_4 | 27 | - | - | - | - | I | ADC0 analog input 4 |
| | A0_5 | 23 | 42 | - | - | - | I | ADC0 analog input 5 |
| | A0_6 | 19 | 41 | - | - | - | I | ADC0 analog input 6 |
| | A0_7 | 18 | 40 | 26 | 25 | 18 | I | ADC0 analog input 7 |
| | A0_12 | 7 | 29 | 18 | 17 | - | I | ADC0 analog input 12 |
| | A1_0 | 8 | 30 | 19 | 18 | 11 | I | ADC1 analog input 0 |
| | A1_1 | 9 | 31 | 20 | 19 | 12 | I | ADC1 analog input 1 |
| | A1_2 | 10 | 32 | 21 | 20 | 13 | I | ADC1 analog input 2 |
| | A1_3 | 11 | 33 | 22 | 21 | 14 | I | ADC1 analog input 3 |
| | A1_4 | 14 | 36 | - | - | - | I | ADC1 analog input 4 |
| | A1_5 | 15 | 37 | - | - | - | I | ADC1 analog input 5 |
| A1_6 | 16 | 38 | - | - | - | I | ADC1 analog input 6 | |
| A1_7 | 17 | 39 | 25 | 24 | 17 | I | ADC1 analog input 7 | |
| BSL | BSL_invoke | 11 | 33 | 22 | 21 | 14 | I | Input pin used to invoke bootloader |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|---------------------------|-------------|------------------------|---------------------|--------------------|---------------|----------|--|-------------------------------------|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS2 8 | 24 VQFN | | |
| BSL (I ² C) | BSLSCL | 34 | 2 | 2 | 5 | 1 | I/O | Default I ² C BSL clock |
| | BSLSDA | 33 | 1 | 1 | 4 | 24 | I/O | Default I ² C BSL data |
| BSL (UART) | BSLRX | 57 | 19 | 15 | 16 | 10 | I | Default UART BSL receive |
| | BSLTX | 56 | 18 | 14 | 15 | 9 | O | Default UART BSL transmit |
| Clock | CLK_OUT | 7 | 5 | 11 | | | O | Configurable clock output |
| | | 18 | 13 | 13 | 14 | 8 | | |
| | | 39 | 17 | 14 | 15 | 9 | | |
| | | 49 | 18 | 14 | 17 | 18 | | |
| | | 55 | 29 | 18 | 25 | | | |
| | | 56 | 40 | 26 | | | | |
| | | 63 | | | | | | |
| | HFCLK_IN | 46 | 12 | 10 | 13 | – | I | Digital high-frequency clock input |
| HFXIN | 45 | 11 | 9 | 12 | – | I | Input for high-frequency crystal oscillator HFXT | |
| HFXOUT | 46 | 12 | 10 | 13 | – | O | Output for high-frequency crystal oscillator HFXT | |
| LFCLK_IN | 44 | 10 | 8 | 11 | 7 | I | Digital low-frequency clock input | |
| LFXIN | 43 | 9 | 7 | 10 | – | I | Input for low-frequency crystal oscillator LFXT | |
| LFXOUT | 44 | 10 | 8 | 11 | 7 | O | Output of low-frequency crystal oscillator LFXT | |
| ROSC | 42 | 8 | 6 | 9 | 5 | I | External resistor used for improving oscillator accuracy | |
| Debug | SWCLK | 13 | 35 | 24 | 23 | 16 | I | Serial wire debug input clock |
| | SWDIO | 12 | 34 | 23 | 22 | 15 | I/O | Serial wire debug data input/output |
| FCC | FCC_IN | 5 9 33 45 | 1 11 27 31 | 1 9 16 20 | 4 12 19 | 12 24 | I | Frequency clock counter input |
| General-Purpose Amplifier | GPAMP_IN+ | 30 | 46 | 30 | 1 | 22 | I | GPAMP noninverting terminal input |
| | GPAMP_IN- | 11 | 33 | 22 | 21 | 14 | I | GPAMP inverting terminal input |
| | GPAMP_OUT | 18 | 40 | 26 | 25 | 18 | O | GPAMP output |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------|-------------|------------------------|------------|--------|-----------|---------|--|--|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS2 8 | 24 VQFN | | |
| GPIO | PA0 | 33 | 1 | 1 | 4 | 24 | I/O | General-purpose digital I/O with wake up from SHUTDOWN |
| | PA1 | 34 | 2 | 2 | 5 | 1 | I/O | General-purpose digital I/O with wake up from SHUTDOWN |
| | PA2 | 42 | 8 | 6 | 9 | 5 | I/O | General-purpose digital I/O |
| | PA3 | 43 | 9 | 7 | 10 | 6 | I/O | General-purpose digital I/O |
| | PA4 | 44 | 10 | 8 | 11 | 7 | I/O | General-purpose digital I/O |
| | PA5 | 45 | 11 | 9 | 12 | – | I/O | General-purpose digital I/O |
| | PA6 | 46 | 12 | 10 | 13 | – | I/O | General-purpose digital I/O |
| | PA7 | 49 | 13 | 11 | – | – | I/O | General-purpose digital I/O |
| | PA8 | 54 | 16 | 12 | – | – | I/O | General-purpose digital I/O |
| | PA9 | 55 | 17 | 13 | 14 | 8 | I/O | General-purpose digital I/O |
| | PA10 | 56 | 18 | 14 | 15 | 9 | I/O | General-purpose digital I/O with wake up from SHUTDOWN |
| | PA11 | 57 | 19 | 15 | 16 | 10 | I/O | General-purpose digital I/O with wake up from SHUTDOWN |
| | PA12 | 5 | 27 | 16 | – | – | I/O | General-purpose digital I/O |
| | PA13 | 6 | 28 | 17 | – | – | I/O | General-purpose digital I/O |
| | PA14 | 7 | 29 | 18 | 17 | – | I/O | General-purpose digital I/O |
| | PA15 | 8 | 30 | 19 | 18 | 11 | I/O | General-purpose digital I/O |
| | PA16 | 9 | 31 | 20 | 19 | 12 | I/O | General-purpose digital I/O |
| | PA17 | 10 | 32 | 21 | 20 | 13 | I/O | General-purpose digital I/O with wake up from SHUTDOWN |
| | PA18 | 11 | 33 | 22 | 21 | 14 | I/O | General-purpose digital I/O with wake up from SHUTDOWN |
| | PA19 | 12 | 34 | 23 | 22 | 15 | I/O | General-purpose digital I/O |
| | PA20 | 13 | 35 | 24 | 23 | 16 | I/O | General-purpose digital I/O |
| | PA21 | 17 | 39 | 25 | 24 | 17 | I/O | General-purpose digital I/O |
| | PA22 | 18 | 40 | 26 | 25 | 18 | I/O | General-purpose digital I/O |
| | PA23 | 24 | 43 | 27 | 26 | 19 | I/O | General-purpose digital I/O |
| | PA24 | 25 | 44 | 28 | 27 | 20 | I/O | General-purpose digital I/O |
| | PA25 | 26 | 45 | 29 | 28 | 21 | I/O | General-purpose digital I/O |
| | PA26 | 30 | 46 | 30 | 1 | 22 | I/O | General-purpose digital I/O |
| | PA27 | 31 | 47 | 31 | 2 | – | I/O | General-purpose digital I/O |
| | PA28 | 35 | 3 | – | – | – | I/O | General-purpose digital I/O with wake up from SHUTDOWN |
| | PA29 | 36 | – | – | – | – | I/O | General-purpose digital I/O |
| | PA30 | 37 | – | – | – | – | I/O | General-purpose digital I/O |
| PA31 | 39 | 5 | – | – | – | I/O | General-purpose digital I/O with wake up from SHUTDOWN | |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|------------------|-------------|---------------------------------|----------------------------|---------------------|----------------------|---------------------|-----------------------------|-----------------------------|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS2 8 | 24 VQFN | | |
| GPIO | PB0 | 47 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB1 | 48 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB2 | 50 | 14 | – | – | – | I/O | General-purpose digital I/O |
| | PB3 | 51 | 15 | – | – | – | I/O | General-purpose digital I/O |
| | PB4 | 52 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB5 | 53 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB6 | 58 | 20 | – | – | – | I/O | General-purpose digital I/O |
| | PB7 | 59 | 21 | – | – | – | I/O | General-purpose digital I/O |
| | PB8 | 60 | 22 | – | – | – | I/O | General-purpose digital I/O |
| | PB9 | 61 | 23 | – | – | – | I/O | General-purpose digital I/O |
| | PB10 | 62 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB11 | 63 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB12 | 64 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB13 | 1 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB14 | 2 | 24 | – | – | – | I/O | General-purpose digital I/O |
| | PB15 | 3 | 25 | – | – | – | I/O | General-purpose digital I/O |
| | PB16 | 4 | 26 | – | – | – | I/O | General-purpose digital I/O |
| | PB17 | 14 | 36 | – | – | – | I/O | General-purpose digital I/O |
| | PB18 | 15 | 37 | – | – | – | I/O | General-purpose digital I/O |
| | PB19 | 16 | 38 | – | – | – | I/O | General-purpose digital I/O |
| | PB20 | 19 | 41 | – | – | – | I/O | General-purpose digital I/O |
| | PB21 | 20 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB22 | 21 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB23 | 22 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB24 | 23 | 42 | – | – | – | I/O | General-purpose digital I/O |
| | PB25 | 27 | – | – | – | – | I/O | General-purpose digital I/O |
| | PB26 | 28 | – | – | – | – | I/O | General-purpose digital I/O |
| PB27 | 29 | – | – | – | – | I/O | General-purpose digital I/O | |
| I ² C | I2C0_SCL | 34 39 57 | 2 5 19 | 2 15 | 5 16 | 1 10 | I/O | I2C0 serial clock |
| | I2C0_SDA | 33 35 56 | 1 3 18 | 1 14 | 4 15 | 9 24 | I/O | I2C0 serial data |
| | I2C1_SCL | 8 10 36 44 50 57 | 10 14 19 30 32 | 8 15 19 21 | 11 16 18 20 | 7 10 11 13 | I/O | I2C1 serial clock |
| | I2C1_SDA | 9 11 37 43 51 56 | 9 15 18 31 33 | 7 14 20 22 | 10 15 19 21 | 6 9 12 14 | I/O | I2C1 serial data |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------|-------------|------------------------|------------|----------|-----------|---------|-------------------------|--|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS2 8 | 24 VQFN | | |
| Power | VSS | 41 | 7 | 5 | 8 | 4 | P | Ground supply |
| | VDD | 40 | 6 | 4 | 7 | 3 | P | Power supply |
| | VCORE | 32 | 48 | 32 | 3 | 23 | P | Regulated core power supply output |
| | QFN Pad | – | Pad | Pad | – | Pad | P | QFN package exposed thermal pad. TI recommends connection to V _{SS} . |
| RTC | RTC_OUT | 31 55 | 17 47 | 13 31 | 2 14 | 8 | O | RTC clock output |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------|-------------|------------------------|----------------------|----------------|----------------|---------|-------------------------|--|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS2 8 | 24 VQFN | | |
| SPI | SPI0_CS0 | 27 42 54 | 8 16 | 6 12 | 9 | 5 | I/O | SPI0 chip-select 0 |
| | SPI0_CS1 | 23 28 43 58 | 9 20 42 | 7 | 10 | 6 | I/O | SPI0 chip-select 1 |
| | SPI0_CS2 | 19 25 59 | 21 41 44 | 28 | 27 | 20 | I/O | SPI0 chip-select 2 |
| | SPI0_CS3 | 2 23 24 | 24 42 43 | 27 | 26 | 19 | I/O | SPI0 chip-select 3 |
| | SPI0_SCK | 5 15 46 57 | 12 19 27 37 | 10 15 16 | 13 16 | 10 | I/O | SPI0 clock signal input – SPI peripheral mode Clock signal output – SPI controller mode |
| | SPI0_POCI | 6 16 44 56 | 10 18 28 38 | 8 14 17 | 11 15 | 7 9 | I/O | SPI0 controller in/peripheral out |
| | SPI0_PICO | 7 14 45 55 | 11 17 29 36 | 9 13 18 | 12 14 17 | 8 | I/O | SPI0 controller out/peripheral in |
| | SPI1_CS0 | 19 30 42 58 | 8 20 41 46 | 6 30 | 1 9 | 5 22 | I/O | SPI1 chip-select 0 |
| | SPI1_CS1 | 14 29 31 | 36 47 | 31 | 2 | – | I/O | SPI1 chip-select 1 |
| | SPI1_CS2 | 8 15 47 | 30 37 | 19 | 18 | 11 | I/O | SPI1 chip-select 2 |
| | SPI1_CS3 | 2 26 48 | 24 45 | 29 | 28 | 21 | I/O | SPI1 chip-select 3 |
| | SPI1_SCK | 4 10 22 61 | 23 26 32 | 21 | 20 | 13 | I/O | SPI1 clock signal input – SPI peripheral mode Clock signal output – SPI controller mode |
| | SPI1_POCI | 2 9 20 59 | 21 24 31 | 20 | 19 | 12 | I/O | SPI1 controller in/peripheral out |
| | SPI1_PICO | 3 11 21 60 | 22 25 33 | 22 | 21 | 14 | I/O | SPI1 controller out/peripheral in |
| System | NRST | 38 | 4 | 3 | 6 | 2 | I | Reset input active low |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------|-------------|---|--|-------------------------------------|--------------------------------|--------------------------|-------------------------|--|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS2 8 | 24 VQFN | | |
| Timer | TIMG0_C0 | 5 24 45 62 | 11 27 43 | 9 16 27 | 12 26 | 19 | I/O | General purpose timer 0 CCR0 capture input or compare output |
| | TIMG0_C1 | 6 25 46 63 | 12 28 44 | 10 17 28 | 13 27 | 20 | I/O | General purpose timer 0 CCR1 capture input or compare output |
| | TIMG6_C0 | 17 28 36 45 50 58 62 | 11 14 20 39 | 9 25 | 12 24 | 17 | I/O | General purpose timer 6 CCR0 capture input or compare output |
| | TIMG6_C1 | 18 29 37 46 51 59 63 | 12 15 21 40 | 10 26 | 13 25 | 18 | I/O | General purpose timer 6 CCR1 capture input or compare output |
| | TIMG7_C0 | 3 10 24 30 35 43 | 3 9 25 32 43 46 | 7 21 27 30 | 1 10 20 26 | 6 13 19 22 | I/O | General purpose timer 7 CCR1 capture input or compare output |
| | TIMG7_C1 | 4 11 16 25 31 39 42 44 49 | 5 8 10 13 26 33 38 44 47 | 6 8 11 22 28 31 | 2 9 11 21 27 | 5 7 14 20 | I/O | General purpose timer 7 CCR1 capture input or compare output |
| | TIMG8_C0 | 3 17 20 24 30 34 36 43 45 49 58 62 | 2 9 11 13 20 25 39 43 46 | 2 7 9 11 25 27 30 | 1 5 10 12 24 26 | 1 6 17 19 22 | I/O | General purpose timer 8 CCR0 capture input or compare output |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------------------|-------------|---|--|--------------------------|-------------------------|--------------------|-------------------------|---|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS2 8 | 24 VQFN | | |
| Timer (continued) | TIMG8_C1 | 4 16 18 21 31 33 37 42 44 46 59 63 | 1 8 10 12 21 26 38 40 47 | 1 6 8 10 31 | 2 4 9 11 25 | 5 7 18 24 | I/O | General purpose timer 8 CCR1 capture input or compare output |
| | TIMG8_IDX | 2 8 34 49 | 2 13 24 30 | 2 11 19 | 5 18 | 1 11 | I | General purpose timer 8 quadrature encoder index pulse input |
| | TIMG12_C0 | 1 7 19 56 | 18 29 41 | 14 18 | 15 17 | 9 | I/O | 32-bit general purpose timer 0 CCR0 capture input or compare output |
| | TIMG12_C1 | 2 23 26 39 | 5 24 42 45 | 29 | 28 | 21 | I/O | 32-bit general purpose timer 0 CCR1 capture input or compare output |
| | TIMA0_C0 | 2 17 33 54 60 | 1 16 22 24 39 | 1 12 25 | 4 24 | 17 24 | I/O | Advanced control timer 0 CCR0 capture input/compare output |
| | TIMA0_CON | 18 55 61 | 17 23 40 | 13 26 | 14 25 | 8 18 | I/O | Advanced control timer 0 CCR0 compare output (inverting) |
| | TIMA0_C1 | 18 34 43 49 55 61 64 | 2 9 13 17 23 40 | 2 7 11 13 26 | 5 10 14 25 | 1 6 8 18 | I/O | Advanced control timer 0 CCR1 capture input or compare output |
| | TIMA0_C1N | 1 19 23 26 44 55 | 10 17 41 42 45 | 8 13 29 | 11 14 28 | 7 21 | I/O | Advanced control timer 0 CCR1 compare output (inverting) |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------------------|-------------|---|---|---------------------------|----------------------|----------------------|-------------------------|---|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS2 8 | 24 VQFN | | |
| Timer (continued) | TIMA0_C2 | 8 14 19 43 47 49 52 56 64 | 9 13 18 30 36 41 | 7 11 14 19 | 10 15 18 | 6 9 11 | I/O | Advanced control timer 0 CCR2 capture input or compare output |
| | TIMA0_C2N | 9 15 46 48 53 57 | 12 19 31 37 | 10 15 20 | 13 16 19 | 10 12 | I/O | Advanced control timer 0 CCR2 compare output (inverting) |
| | TIMA0_C3 | 1 5 10 23 24 26 28 35 44 50 | 3 10 14 27 32 42 43 45 | 8 16 21 27 29 | 11 20 26 28 | 7 13 19 21 | I/O | Advanced control timer 0 CCR3 capture input or compare output |
| | TIMA0_C3N | 6 11 25 29 39 51 | 5 15 28 33 44 | 17 22 28 | 21 27 | 14 20 | I/O | Advanced control timer 0 CCR3 compare output (inverting) |
| | TIMA1_C0 | 8 10 14 28 35 47 50 52 56 | 3 14 18 30 32 36 | 14 19 21 | 15 18 20 | 9 11 13 | I/O | Advanced control timer 1 CCR0 capture input or compare output |
| | TIMA1_C0N | 8 23 52 54 58 | 16 20 30 42 | 12 19 | 18 | 11 | I/O | Advanced control timer 0 CCR3 compare output (inverting) |
| | TIMA1_C1 | 9 11 15 25 29 39 48 51 53 57 | 5 15 19 31 33 37 44 | 15 20 22 28 | 16 19 21 27 | 10 12 14 20 | I/O | Advanced control timer 1 CCR1 capture input or compare output |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------------------|-------------|---------------------------|----------------------|----------|-----------|---------|-------------------------|--|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS2 8 | 24 VQFN | | |
| Timer (continued) | TIMA1_C1N | 9 19 53 55 59 | 17 21 31 41 | 13 20 | 14 19 | 8 12 | I/O | Advanced control timer 1 CCR1 compare output (inverting) |
| | TIMA_FAL0 | 22 30 35 46 | 3 12 46 | 10 30 | 1 13 | 22 | I | Advanced control timer 0 fault handling input |
| | TIMA_FAL1 | 19 33 45 64 | 1 11 41 | 1 9 | 4 12 | 24 | I | Advanced control timer 1 fault handling input |
| | TIMA_FAL2 | 27 31 34 | 2 47 | 2 31 | 2 5 | 1 | I | Advanced control timer 2 fault handling input |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------|-------------|------------------------|----------------------|----------|-----------|----------|-------------------------|---|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS2 8 | 24 VQFN | | |
| UART | UART0_TX | 33 35 47 56 | 1 3 18 | 1 14 | 4 15 | 9 24 | O | UART0 transmit data |
| | UART0_RX | 34 39 48 57 | 2 5 19 | 2 15 | 5 16 | 1 10 | I | UART0 receive data |
| | UART0_CTS | 7 16 27 55 | 17 29 38 | 13 18 | 14 17 | 8 | I | UART0 "clear to send" flow control input |
| | UART0_RTS | 8 28 54 | 16 30 | 12 19 | 18 | 11 | O | UART0 "request to send" flow control output |
| | UART1_TX | 10 52 54 58 | 16 20 32 | 12 21 | 20 | 13 | O | UART1 transmit data |
| | UART1_RX | 11 53 55 59 | 17 21 33 | 13 22 | 14 21 | 8 14 | I | UART1 receive data |
| | UART1_CTS | 17 50 60 | 14 22 39 | 25 | 24 | 17 | I | UART1 "clear to send" flow control input |
| | UART1_RTS | 18 51 61 | 15 23 40 | 26 | 25 | 18 | O | UART1 "request to send" flow control output |
| | UART2_TX | 3 14 17 24 | 25 36 39 43 | 25 27 | 24 26 | 17 19 | O | UART2 transmit data |
| | UART2_RX | 4 15 18 25 | 26 37 40 44 | 26 28 | 25 27 | 18 20 | I | UART2 receive data |
| | UART2_CTS | 37 43 50 58 | 9 14 20 | 7 | 10 | 6 | I | UART2 "clear to send" flow control input |
| | UART2_RTS | 36 44 51 59 | 10 15 21 | 8 | 11 | 7 | O | UART2 "request to send" flow control output |

Table 6-3. Signal Descriptions (continued)

| FUNCTION | SIGNAL NAME | PIN NO. ⁽¹⁾ | | | | | PIN TYPE ⁽²⁾ | DESCRIPTION |
|----------------------------------|-------------|------------------------|----------------|----------|-----------|---------|-------------------------|---|
| | | 64 PM | 48 PT, RGZ | 32 RHB | 28 DGS2 8 | 24 VQFN | | |
| UART (continued) | UART3_TX | 7 30 50 64 | 14 29 46 | 18 30 | 1 17 | 22 | O | UART3 transmit data |
| | UART3_RX | 1 6 26 51 | 15 28 45 | 17 29 | 28 | 21 | I | UART3 receive data |
| | UART3_CTS | 3 5 24 52 | 25 27 43 | 16 27 | 26 | 19 | I | UART3 "clear to send" flow control input |
| | UART3_RTS | 4 6 25 53 | 26 28 44 | 17 28 | 27 | 20 | O | UART3 "request to send" flow control output |
| Voltage Reference ⁽³⁾ | VREF+ | 24 | 43 | 27 | 26 | 19 | I/O | Voltage reference (VREF) power supply; external reference input or internal reference output |
| | VREF- | 17 | 39 | 25 | 24 | 17 | I/O | Voltage reference (VREF) ground supply; external reference input or internal reference output |

(1) -- = not available

(2) I = input, O = output, I/O = input or output, P = power

(3) When using VREF+ and VREF- to bring in an external voltage reference for analog peripherals such as the ADC, a decoupling capacitor must be placed on VREF+ to VREF-/GND with a capacitance based on the external reference source

6.4 Connections for Unused Pins

Table 6-4 lists the correct termination of unused pins.

Table 6-4. Connection of Unused Pins

| PIN ⁽¹⁾ | POTENTIAL | COMMENT |
|--------------------|-----------|---|
| PAx and PBx | Open | Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with the internal pullup or pulldown resistor enabled. |
| NRST | VCC | NRST is an active-low reset signal. Pull the pin high to VCC, or the device cannot start. For more information, see Section 9.1 . |

- (1) Any unused pin with a function that is shared with general-purpose I/O must follow the "PAx and PBx" unused pin connection guidelines.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------|-------------------------------|---|------|------------------------------------|------|
| VDD | Supply voltage | At VDD pin | -0.3 | 4.1 | V |
| V _I | Input voltage | Applied to any 5-V tolerant open-drain pins | -0.3 | 5.5 | V |
| V _I | Input voltage | Applied to any common tolerance pins | -0.3 | V _{DD} + 0.3 (4.1 MAX) | V |
| I _{VDD} | Current into VDD pin (source) | -40°C ≤ T _J ≤ 130°C | | 80 | mA |
| | Current into VDD pin (source) | -40°C ≤ T _J ≤ 85°C | | 100 | mA |
| I _{VSS} | Current out of VSS pin (sink) | -40°C ≤ T _J ≤ 130°C | | 80 | mA |
| | Current out of VSS pin (sink) | -40°C ≤ T _J ≤ 85°C | | 100 | mA |
| I _{IO} | Current of SDIO pin | Current sunk or sourced by SDIO pin | | 6 | mA |
| | Current of HS_IO pin | Current sunk or sourced by HSIO pin | | 6 | mA |
| | Current of HDIO pin | Current sunk or sourced by HDIO pin | | 20 | mA |
| | Current of ODIO pin | Current sunk by ODIO pin | | 20 | mA |
| I _D | Supported diode current | Diode current at any device pin | | ±2 | mA |
| T _J | Junction temperature | Junction temperature | -40 | 130 | °C |
| T _{stg} | Storage temperature | Storage temperature | -40 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|-------------------------------|--|--|------|------|-----|------|
| VDD | Supply voltage | | 1.62 | | 3.6 | V |
| V _{CORE} | Voltage on V _{CORE} pin ⁽²⁾ | | | 1.35 | | V |
| C _{VDD} | Capacitor connected between VDD and VSS ⁽¹⁾ | | | 10 | | μF |
| C _{V_{CORE}} | Capacitor connected between V _{CORE} and VSS ^{(1) (2)} | | | 470 | | nF |
| T _A | Ambient temperature, T version | | -40 | | 105 | °C |
| | Ambient temperature, S version | | -40 | | 125 | |
| T _J | Max junction temperature, T version | | | | 125 | °C |
| T _J | Max junction temperature, S version | | | | 130 | °C |

7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-------------------------------------|--|-----|-----|-----|------|
| f_{MCLK} (PD1 bus clock) | MCLK, CPUCLK frequency with 2 flash wait states ⁽³⁾ | | | 80 | MHz |
| | MCLK, CPUCLK frequency with 1 flash wait state ⁽³⁾ | | | 48 | |
| | MCLK, CPUCLK frequency with 0 flash wait states ⁽³⁾ | | | 24 | |
| f_{ULPCLK} (PD0 bus clock) | ULPCLK frequency | | | 40 | MHz |

- Connect C_{VDD} and C_{VCORE} between VDD/VSS and VCORE/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of $\pm 20\%$ or better is required for C_{VDD} and C_{VCORE} .
- The VCORE pin must only be connected to C_{VCORE} . Do not supply any voltage or apply any external load to the VCORE pin.
- Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software unless MCLK is sourced from a high speed clock source (HSCLK sourced from HFCLK or SYSPLL).

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | PACKAGE | VALUE | UNIT |
|-------------------------------|--|------------------|-------|-----------------------------|
| $R_{\theta\text{JA}}$ | Junction-to-ambient thermal resistance | LQFP-64 (PM) | 63.9 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JC(top)}}$ | Junction-to-case (top) thermal resistance | | 23.8 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JB}}$ | Junction-to-board thermal resistance | | 35.3 | $^{\circ}\text{C}/\text{W}$ |
| Ψ_{JT} | Junction-to-top characterization parameter | | 2.2 | $^{\circ}\text{C}/\text{W}$ |
| Ψ_{JB} | Junction-to-board characterization parameter | | 35 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JC(bot)}}$ | Junction-to-case (bottom) thermal resistance | | N/A | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JA}}$ | Junction-to-ambient thermal resistance | VQFN-48 (RGZ) | 30.1 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JC(top)}}$ | Junction-to-case (top) thermal resistance | | 20.7 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JB}}$ | Junction-to-board thermal resistance | | 12.5 | $^{\circ}\text{C}/\text{W}$ |
| Ψ_{JT} | Junction-to-top characterization parameter | | 0.3 | $^{\circ}\text{C}/\text{W}$ |
| Ψ_{JB} | Junction-to-board characterization parameter | | 12.4 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JC(bot)}}$ | Junction-to-case (bottom) thermal resistance | | 4.2 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JA}}$ | Junction-to-ambient thermal resistance | LQFP-48 (PT) | 69.2 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JC(top)}}$ | Junction-to-case (top) thermal resistance | | 27.4 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JB}}$ | Junction-to-board thermal resistance | | 32.6 | $^{\circ}\text{C}/\text{W}$ |
| Ψ_{JT} | Junction-to-top characterization parameter | | 2.6 | $^{\circ}\text{C}/\text{W}$ |
| Ψ_{JB} | Junction-to-board characterization parameter | | 32.3 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JC(bot)}}$ | Junction-to-case (bottom) thermal resistance | | N/A | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JA}}$ | Junction-to-ambient thermal resistance | VQFN-32 (RHB) | 32.1 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JC(top)}}$ | Junction-to-case (top) thermal resistance | | 23.6 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JB}}$ | Junction-to-board thermal resistance | | 13.0 | $^{\circ}\text{C}/\text{W}$ |
| Ψ_{JT} | Junction-to-top characterization parameter | | 0.3 | $^{\circ}\text{C}/\text{W}$ |
| Ψ_{JB} | Junction-to-board characterization parameter | | 13.0 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JC(bot)}}$ | Junction-to-case (bottom) thermal resistance | | 3.3 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JA}}$ | Junction-to-ambient thermal resistance | VSSOP-28 (DGS28) | 78.9 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JC(top)}}$ | Junction-to-case (top) thermal resistance | | 38.6 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JB}}$ | Junction-to-board thermal resistance | | 41.3 | $^{\circ}\text{C}/\text{W}$ |
| Ψ_{JT} | Junction-to-top characterization parameter | | 3.4 | $^{\circ}\text{C}/\text{W}$ |
| Ψ_{JB} | Junction-to-board characterization parameter | | 41.0 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\theta\text{JC(bot)}}$ | Junction-to-case (bottom) thermal resistance | | N/A | $^{\circ}\text{C}/\text{W}$ |

7.4 Thermal Information (continued)

| THERMAL METRIC ⁽¹⁾ | | PACKAGE | VALUE | UNIT |
|-------------------------------|--|---------------|-------|------|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | VQFN-24 (RGE) | 44.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | | 38.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | | 21.9 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | | 1.1 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | | 21.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | | 7.1 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

| PARAMETER | | MCLK | -40°C | | 25°C | | 85°C | | 105°C | | 125°C | | UNIT |
|---|---|-------|-------|------|------|------|------|------|-------|------|-------|------|--------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| RUN Mode | | | | | | | | | | | | | |
| IDD _{RUN} | MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from flash | 80MHz | 7.5 | | 7.6 | | 8.0 | | 8.0 | | 8.6 | | mA |
| | | 48MHz | 4.8 | | 4.9 | | 5.1 | | 5.2 | | 5.7 | | |
| | MCLK=SYSOSC, CoreMark, execute from flash | 32MHz | 3.3 | | 3.4 | | 3.7 | | 3.7 | | 4.1 | | |
| | | 4MHz | 0.6 | | 0.7 | | 0.8 | | 1.0 | | 1.4 | | |
| | MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from SRAM | 80MHz | 5.9 | | 6.0 | | 6.3 | | 6.4 | | 6.8 | | |
| | | 48MHz | 3.7 | | 3.8 | | 3.8 | | 4.5 | | 5.0 | | |
| MCLK=SYSOSC, CoreMark, execute from SRAM | 32MHz | 2.5 | | 2.6 | | 2.7 | | 3.0 | | 3.4 | | | |
| | 4MHz | 0.6 | | 0.6 | | 0.8 | | 0.9 | | 1.0 | | | |
| IDD _{RUN, per MHz} | MCLK=SYSPLL, SYSPLLREF=SYSOSC, CoreMark, execute from flash | 80MHz | 94 | | 96 | | 99 | | 100 | | 107 | | μA/MHz |
| | MCLK=SYSPLL, SYSPLLREF=SYSOSC, While(1), execute from flash | 80MHz | 52 | 55 | 53 | 57 | 55 | 61 | 57 | 68 | 64 | 74 | |
| SLEEP Mode | | | | | | | | | | | | | |
| IDD _{SLEEP} | MCLK=SYSPLL, SYSPLLREF=SYSOSC, CPU is halted | 80MHz | 2974 | 3154 | 3039 | 3211 | 3262 | 3350 | 3350 | 3389 | 3439 | 4900 | μA |
| | | 48MHz | 2025 | 2174 | 2075 | 2330 | 2262 | 2437 | 2337 | 2998 | 2778 | 4000 | |
| | MCLK=SYSOSC, CPU is halted | 32MHz | 1355 | 1460 | 1399 | 1506 | 1567 | 1750 | 1675 | 2320 | 2094 | 3000 | |
| | | 4MHz | 440 | 513 | 467 | 620 | 662 | 898 | 737 | 1400 | 1140 | 2834 | |

7.5.2 STOP/STANDBY Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

| PARAMETER | | ULPCLK | -40°C | | 25°C | | 85°C | | 105°C | | 125°C | | UNIT |
|----------------------|--|--------|---|-----|------|-----|------|-----|-------|-----|-------|-----|------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| STOP Mode | | | | | | | | | | | | | |
| IDD _{STOP0} | SYSOSC=32MHz, USE4MHZSTOP=0, DISABLESTOP=0 | 4MHz | 331 | 355 | 338 | 360 | 343 | 362 | 346 | 364 | 357 | 380 | μA |
| IDD _{STOP1} | | | SYSOSC=4MHz, USE4MHZSTOP=1, DISABLESTOP=0 | 174 | 196 | 179 | 198 | 185 | 203 | 188 | 206 | 198 | |
| IDD _{STOP2} | SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK | 32kHz | 44 | 54 | 46 | 56 | 51 | 61 | 53 | 64 | 62 | 83 | |
| STANDBY Mode | | | | | | | | | | | | | |
| IDD _{STBY0} | LFCLK=LFXT, STOPCLKSTBY=0, RTC enabled | 32kHz | 2 | 5 | 2 | 5 | 4 | 10 | 7 | 18 | 16 | 42 | μA |
| IDD _{STBY1} | LFCLK=LFOSC, STOPCLKSTBY=1, RTC enabled | | 1.4 | 3 | 1.5 | 4 | 3 | 10 | 6 | 17 | 13 | 40 | |
| | LFCLK=LFXT, STOPCLKSTBY=1, RTC enabled | | 1.4 | 3 | 1.5 | 4 | 4 | 10 | 6 | 17 | 13 | 40 | |
| | LFCLK=LFXT, STOPCLKSTBY=1, GPIOA enabled | | 1.4 | 3 | 1.5 | 4 | 4 | 10 | 6 | 17 | 13 | 40 | |

7.5.3 SHUTDOWN Mode

All inputs tied to 0V or VDD. Outputs do not source or sink any current. Core regulator is powered down.

| PARAMETER | | VDD | -40°C | 25°C | 85°C | 105°C | 125°C | UNIT |
|---------------------|---------------------------------|------|---------|---------|---------|---------|---------|------|
| | | | TYP MAX | TYP MAX | TYP MAX | TYP MAX | TYP MAX | |
| IDD _{SHDN} | Supply current in SHUTDOWN mode | 3.3V | 40 | 80 | 730 | 1730 | 4800 | nA |

7.6 Power Supply Sequencing

7.6.1 POR and BOR

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|---|-----------------------------------|------|------|------|------|
| dVDD/dt | VDD (supply voltage) slew rate | Rising | | | 1 | V/us |
| | | Falling ⁽²⁾ | | | 0.01 | |
| | | Falling, STANDBY | | | 0.1 | V/ms |
| V _{POR+} | Power-on reset voltage level | Rising ⁽¹⁾ | 1.04 | 1.30 | 1.5 | V |
| V _{POR-} | | Falling ⁽¹⁾ | 0.99 | 1.25 | 1.48 | V |
| V _{HYS, POR} | POR hysteresis | | 30 | 58 | 74 | mV |
| V _{BOR0+, COLD} | Brown-out reset voltage level 0 (default level) | Cold start, rising ⁽¹⁾ | 1.48 | 1.54 | 1.61 | V |
| V _{BOR0+} | | Rising ^{(1) (2)} | 1.56 | 1.58 | 1.61 | |
| V _{BOR0-} | | Falling ^{(1) (2)} | 1.56 | 1.57 | 1.61 | |
| V _{BOR0, STBY} | | STANDBY mode ⁽¹⁾ | 1.54 | 1.56 | 1.60 | |
| V _{BOR1+} | Brown-out-reset voltage level 1 | Rising ^{(1) (2)} | 2.15 | 2.17 | 2.23 | V |
| V _{BOR1-} | | Falling ^{(1) (2)} | 2.12 | 2.14 | 2.19 | |
| V _{BOR1, STBY} | | STANDBY mode ⁽¹⁾ | 2.06 | 2.13 | 2.20 | |
| V _{BOR2+} | Brown-out-reset voltage level 2 | Rising ^{(1) (2)} | 2.74 | 2.77 | 2.83 | V |
| V _{BOR2-} | | Falling ^{(1) (2)} | 2.71 | 2.73 | 2.80 | |
| V _{BOR2, STBY} | | STANDBY mode ⁽¹⁾ | 2.68 | 2.71 | 2.82 | |
| V _{BOR3+} | Brown-out-reset voltage level 3 | Rising ^{(1) (2)} | 2.88 | 2.96 | 3.04 | V |
| V _{BOR3-} | | Falling ^{(1) (2)} | 2.85 | 2.93 | 3.01 | |
| V _{BOR3, STBY} | | STANDBY mode ⁽¹⁾ | 2.80 | 2.92 | 3.02 | |
| V _{HYS, BOR} | Brown-out reset hysteresis | Level 0 ⁽¹⁾ | | 14 | 18 | mV |
| | | Levels 1-3 ⁽¹⁾ | | 34 | 38 | |
| T _{PD, BOR} | BOR propagation delay | RUN/SLEEP/STOP mode | | | 5 | us |
| | | STANDBY mode | | | 100 | us |

(1) |dVDD/dt| ≤ 3V/s

(2) Device operating in RUN, SLEEP, or STOP mode.

7.6.2 Power Supply Ramp

Figure 7-1 shows the relationships of POR-, POR+, BOR0-, and BOR0+ during powerup and powerdown.

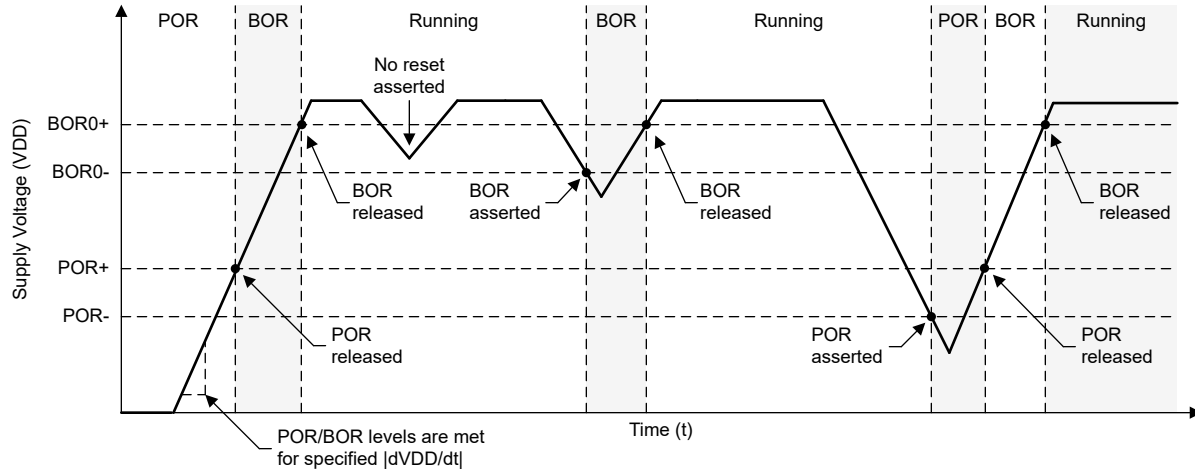


Figure 7-1. Power Cycle POR and BOR Conditions

7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|---|--|------|-----|-----|--------------------|
| Supply | | | | | | |
| VDD _{PGM/ERASE} | Program and erase supply voltage | | 1.62 | | 3.6 | V |
| IDDERASE | Supply current from VDD during erase operation | Supply current delta | | | 10 | mA |
| IDDPGM | Supply current from VDD during program operation | Supply current delta | | | 10 | mA |
| Endurance | | | | | | |
| NWEC _(LOWER) | Erase/program cycle endurance (lower 32kB flash) ⁽¹⁾ | | 100 | | | k cycles |
| NWEC _(UPPER) | Erase/program cycle endurance (remaining flash) ⁽¹⁾ | | 10 | | | k cycles |
| NE _(MAX) | Total erase operations before failure ⁽²⁾ | | 802 | | | k erase operations |
| NW _(MAX) | Write operations per word line before sector erase ⁽³⁾ | | | | 83 | write operations |
| Retention | | | | | | |
| t _{RET_85} | Flash memory data retention | -40°C ≤ T _j ≤ 85°C | 60 | | | years |
| t _{RET_105} | Flash memory data retention | -40°C ≤ T _j ≤ 105°C | 11.4 | | | years |
| Program and Erase Timing | | | | | | |
| t _{PROG (WORD, 64)} | Program time for flash word ^{(4) (6)} | | | 50 | 275 | μs |
| t _{PROG (SEC, 64)} | Program time for 1kB sector ^{(5) (6)} | | | 6.4 | | ms |
| t _{ERASE (SEC)} | Sector erase time | ≤2k erase/program cycles, T _j ≥ 25°C | | 4 | 20 | ms |
| t _{ERASE (SEC)} | Sector erase time | ≤10k erase/program cycles, T _j ≥ 25°C | | 20 | 150 | ms |
| t _{ERASE (SEC)} | Sector erase time | <10k erase/program cycles | | 20 | 200 | ms |
| t _{ERASE (BANK)} | Bank erase time | <10k erase/program cycles | | 22 | 220 | ms |

- (1) The lower 32kB flash address space supports higher erase/program endurance to enable EEPROM emulation applications. On devices with ≤32kB flash memory, the entire flash memory supports NWEC_(LOWER) erase/program cycles.
- (2) Total number of cumulative erase operations supported by the flash before failure. A sector erase or bank erase operation is considered to be one erase operation.
- (3) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.

- (4) Program time is defined as the time from when the program command is triggered until the command completion interrupt flag is set in the flash controller.
- (5) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.
- (6) Flash word size is 64 data bits (8 bytes). On devices with ECC, the total flash word size is 72 bits (64 data bits plus 8 ECC bits).

7.8 Timing Characteristics

VDD=3.3V, T_a=25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--------------------|-----|------|-----|------|
| Wakeup Timing | | | | | | |
| t _{WAKE, SLEEP1} | Wakeup time from SLEEP1 to RUN ⁽¹⁾ | | | 1.5 | | us |
| t _{WAKE, SLEEP2} | Wakeup time from SLEEP2 to RUN ⁽¹⁾ | | | 2.1 | | us |
| t _{WAKE, STANDBY0} | Wakeup time from STANDBY0 to RUN ⁽¹⁾ | | | 15.2 | | us |
| t _{WAKE, STANDBY1} | Wakeup time from STANDBY1 to RUN ⁽¹⁾ | | | 15.2 | | us |
| t _{WAKE, STOP0} | Wakeup time from STOP0 to RUN (SYSOSC enabled) ⁽¹⁾ | | | 12.1 | | us |
| t _{WAKE, STOP1} | Wakeup time from STOP1 to RUN (SYSOSC enabled) ⁽¹⁾ | | | 13.5 | | us |
| t _{WAKE, STOP2} | Wakeup time from STOP2 to RUN (SYSOSC disabled) ⁽¹⁾ | | | 12.9 | | |
| t _{WAKEUP, SHDN} | Wakeup time from SHUTDOWN to RUN ⁽²⁾ | Fast boot enabled | | 240 | | us |
| | | Fast boot disabled | | 252 | | |
| Asynchronous Fast Clock Request Timing | | | | | | |
| t _{DELAY, SLEEP1} | Delay time from edge of asynchronous request to first 32MHz MCLK edge | Mode is SLEEP1 | | 0.33 | | us |
| t _{DELAY, SLEEP2} | Delay time from edge of asynchronous request to first 32MHz MCLK edge | Mode is SLEEP2 | | 0.93 | | us |
| t _{DELAY, STANDBY0} | Delay time from edge of asynchronous request to first 32MHz MCLK edge | Mode is STANDBY0 | | 3.2 | | us |
| t _{DELAY, STANDBY1} | Delay time from edge of asynchronous request to first 32MHz MCLK edge | Mode is STANDBY1 | | 3.2 | | us |
| t _{DELAY, STOP0} | Delay time from edge of asynchronous request to first 32MHz MCLK edge | Mode is STOP0 | | 0.1 | | us |
| t _{DELAY, STOP1} | Delay time from edge of asynchronous request to first 32MHz MCLK edge | Mode is STOP1 | | 2.4 | | us |
| t _{DELAY, STOP2} | Delay time from edge of asynchronous request to first 32MHz MCLK edge | Mode is STOP2 | | 0.9 | | us |
| Startup Timing | | | | | | |
| t _{START, RESET} | Device cold startup time from reset/power-up ⁽³⁾ | Fast boot enabled | | 260 | | us |
| | | Fast boot disabled | | 308 | | |
| NRST Timing | | | | | | |
| t _{RST, BOOTRST} | Pulse length on NRST pin to generate BOOTRST | ULPCLK≥4MHz | | 1.5 | | us |
| | | ULPCLK=32kHz | | 80 | | |
| t _{RST, POR} | Pulse length on NRST pin to generate POR | | | 1 | | s |

- (1) The wake-up time is measured from the edge of an external wake-up signal (GPIO wake-up event) to the time that the first instruction of the user program is executed, with glitch filter disabled (FILTEREN=0x0) and fast wake enabled (FASTWAKEONLY=1).
- (2) The wake-up time is measured from the edge of an external wake-up signal (IOMUX wake-up event) to the time that first instruction of the user program is executed.

- (3) The start-up time is measured from the time that VDD crosses VBOR0- (cold start-up) to the time that the first instruction of the user program is executed.

7.9 Clock Specifications

7.9.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|--|--|-------|-----|------|------|
| f _{SYSOSC} | Factory trimmed SYSOSC frequency | SYSOSCCFG.FREQ=00 (BASE) | | 32 | | MHz |
| | | SYSOSCCFG.FREQ=01 | | 4 | | |
| | User trimmed SYSOSC frequency | SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=10 | | 24 | | |
| | | SYSOSCCFG.FREQ=10, SYSOSCTRIMUSER.FREQ=01 | | 16 | | |
| f _{SYSOSC} | SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled and an ideal ROSC resistor is assumed ⁽¹⁾ ⁽²⁾ | SETUSEFCL=1, T _a = 25 °C | -0.41 | | 0.58 | % |
| | | SETUSEFCL=1, -40 °C ≤ T _a ≤ 85 °C | -0.80 | | 0.93 | |
| | | SETUSEFCL=1, -40 °C ≤ T _a ≤ 105 °C | -0.80 | | 1.09 | |
| | | SETUSEFCL=1, -40 °C ≤ T _a ≤ 125 °C | -0.80 | | 1.30 | |
| f _{SYSOSC} | SYSOSC accuracy when frequency correction loop (FCL) is enabled with R _{OSC} resistor put at R _{OSC} pin, for factory trimmed frequencies ⁽¹⁾ | SETUSEFCL=1, T _a = 25 °C, ±0.1% ±25ppm R _{OSC} | -0.5 | | 0.7 | % |
| | | SETUSEFCL=1, -40 °C ≤ T _a ≤ 85 °C, ±0.1% ±25ppm R _{OSC} | -1.1 | | 1.2 | |
| | | SETUSEFCL=1, -40 °C ≤ T _a ≤ 105 °C, ±0.1% ±25ppm R _{OSC} | -1.1 | | 1.4 | |
| | | SETUSEFCL=1, -40 °C ≤ T _a ≤ 125 °C, ±0.1% ±25ppm R _{OSC} | -1.1 | | 1.7 | |
| f _{SYSOSC} | SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled when the internal ROSC resistor is used ⁽⁴⁾ | SETUSEFCL=1 -40 °C ≤ T _a ≤ 125 °C | -1.4 | | 1.8 | % |
| f _{SYSOSC} | SYSOSC accuracy when frequency correction loop (FCL) is disabled, 32MHz | SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 °C ≤ T _a ≤ 125 °C | -2.6 | | 1.8 | % |
| f _{SYSOSC} | SYSOSC accuracy when frequency correction loop (FCL) is disabled, for factory trimmed frequencies, 4MHz | SETUSEFCL=0, SYSOSCCFG.FREQ=01, -40 °C ≤ T _a ≤ 125 °C | -2.7 | | 2.3 | |
| f _{SYSOSC} | External resistor put between ROSC pin and VSS ⁽¹⁾ | SETUSEFCL=1 | | 100 | | kΩ |
| f _{SYSOSC} | Settling time to target accuracy ⁽³⁾ | SETUSEFCL=1, ±0.1% 25ppm R _{OSC} ⁽¹⁾ | | | 30 | us |
| f _{SYSOSC} | f _{SYSOSC} additional undershoot accuracy during t _{settle} ⁽³⁾ | SETUSEFCL=1, ±0.1% 25ppm R _{OSC} ⁽¹⁾ | -11 | | | % |

- (1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an external reference resistor (R_{OSC}) which must be connected between the device ROSC pin and VSS when using the FCL. Accuracies are shown for a ±0.1% ±25ppm R_{OSC}; relaxed tolerance resistors may also be used (with reduced SYSOSC accuracy). See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy for various R_{OSC} accuracies. R_{OSC} does not need to be populated if the FCL is not enabled.
- (2) Represents the device accuracy only. The tolerance and temperature drift of the ROSC resistor used must be combined with this spec to determine final accuracy. Performance for a ±0.1% ±25ppm R_{OSC} is given as a reference point.
- (3) When SYSOSC is waking up (for example, when exiting a low power mode) and FCL is enabled, the SYSOSC will initially undershoot the target frequency f_{SYSOSC} by an additional error of up to f_{settle,SYSOSC} for the time t_{settle,SYSOSC}, after which the target accuracy is achieved.
- (4) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.

7.9.1.1 SYSOSC Typical Frequency Accuracy

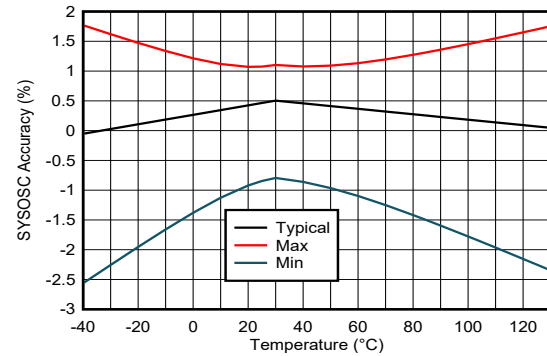
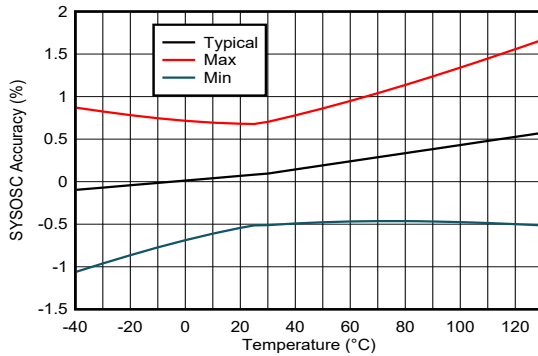


Figure 7-2. SYSOSC Accuracy with FCL On (32MHz) Figure 7-3. SYSOSC Accuracy with FCL Off (32MHz)

FCL-on accuracy is based on a 0.1% tolerance 25 ppm/°C ROSC resistor.

7.9.2 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|---------------------------|----------------------------------|-----|-------|-----|------|
| f _{LFOSC} | LFOSC frequency | | | 32768 | | Hz |
| | LFOSC accuracy | -40 °C ≤ T _a ≤ 125 °C | -5 | | 5 | % |
| | | -40 °C ≤ T _a ≤ 85 °C | -3 | | 3 | % |
| I _{LFOSC} | LFOSC current consumption | | | 300 | | nA |
| t _{start, LFOSC} | LFOSC start-up time | | | 1.7 | | ms |

7.9.3 System Phase Lock Loop (SYSPLL)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|-----------------------------------|---|-----|------|-----|------|
| f _{SYSPLLREF} | SYSPLL reference frequency range | | 4 | | 48 | MHz |
| f _{VCO} | VCO output frequency | | 80 | | 400 | MHz |
| f _{SYSPLL} | SYSPLL output frequency range (1) | SYSPLLCLK0, SYSPLLCLK1 | 1 | | 200 | MHz |
| | | SYSPLLCLK2X | 4 | | 800 | |
| DC _{PLL} | SYSPLL output duty cycle | f _{SYSPLLREF} =32MHz, f _{VCO} =160MHz | 45 | | 55 | % |
| Jitter _{SYSPLL} | SYSPLL RMS cycle-to-cycle jitter | f _{SYSPLLREF} =32MHz, f _{VCO} =160MHz | | 24 | | ps |
| | SYSPLL RMS period jitter | | | 15.5 | | |
| I _{SYSPLL} | SYSPLL current consumption | f _{SYSPLLREF} =32MHz, f _{VCO} =160MHz | | 316 | | μA |
| t _{start, SYSPLL} | SYSPLL start-up time | f _{SYSPLLREF} =32MHz, f _{VCO} =160MHz, ±0.5% accuracy | | 7 | 18 | us |

(1) The SYSPLL may support higher output frequencies than the device clock system supports. Ensure that the device maximum frequency specifications are not violated when configuring the SYSPLL output frequencies.

7.9.4 Low Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|----------------|-----------------|-----|-------|-----|------|
| Low frequency crystal oscillator (LFXT) | | | | | | |
| f _{LFXT} | LFXT frequency | | | 32768 | | Hz |

7.9.4 Low Frequency Crystal/Clock (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|----------------------|-------|-------|-------|------|
| DC _{LFXT} | LFXT duty cycle | | 30 | | 70 | % |
| OA _{LFXT} | LFXT crystal oscillation allowance | | | 419 | | kΩ |
| C _{L, eff} | Integrated effective load capacitance ⁽¹⁾ | | | 1 | | pF |
| t _{start, LFXT} | LFXT start-up time | | | 483 | 640 | ms |
| I _{LFXT} | LFXT current consumption | XT1DRIVE=0, LOWCAP=1 | | 200 | | nA |
| Low frequency digital clock input (LFCLK_IN) | | | | | | |
| f _{LFIN} | LFCLK_IN frequency ⁽²⁾ | SETUSEEXLF=1 | 29491 | 32768 | 36045 | Hz |
| DC _{LFIN} | LFCLK_IN duty cycle ⁽²⁾ | SETUSEEXLF=1 | 40 | | 60 | % |
| LFCLK Monitor | | | | | | |
| f _{FAULTLF} | LFCLK monitor fault frequency ⁽³⁾ | MONITOR=1 | 2800 | 4200 | 8400 | Hz |

(1) This includes parasitic bond and package capacitance ($\approx 2\text{pF}$ per pin), calculated as $C_{\text{LFXIN}} \times C_{\text{LFXOUT}} / (C_{\text{LFXIN}} + C_{\text{LFXOUT}})$, where C_{LFXIN} and C_{LFXOUT} are the total capacitance at LFXIN and LFXOUT, respectively.

(2) The digital clock input (LFCLK_IN) accepts a logic level square wave clock.

(3) The LFCLK monitor may be used to monitor the LFXT or LFCLK_IN. It will always fault below the MIN fault frequency, and will never fault above the MAX fault frequency.

7.9.5 High Frequency Crystal/Clock

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---|-------|-----|-----|------|
| High frequency crystal oscillator (HFXT) | | | | | | |
| f _{HFXT} | HFXT frequency | HFXTRSEL=00 | 4 | | 8 | MHz |
| | | HFXTRSEL=01 | 8.01 | | 16 | |
| | | HFXTRSEL=10 | 16.01 | | 32 | |
| | | HFXTRSEL=11 | 32.01 | | 48 | |
| DC _{HFXT} | HFXT duty cycle | HFXTRSEL=00 | 40 | | 65 | % |
| | | HFXTRSEL=01 | 40 | | 60 | |
| | | HFXTRSEL=10 | 40 | | 60 | |
| | | HFXTRSEL=11 | 40 | | 60 | |
| OA _{HFXT} | HFXT crystal oscillation allowance | HFXTRSEL=00 (4 to 8MHz range) | | 2 | | kΩ |
| C _{L, eff} | Integrated effective load capacitance ⁽¹⁾ | | | 1 | | pF |
| t _{start, HFXT} | HFXT start-up time ⁽²⁾ | HFXTRSEL=11, 32MHz crystal | | 0.5 | | ms |
| I _{HFXT} | HFXT current consumption ⁽²⁾ | f _{HFXT} =4MHz, R _m =300Ω, C _L =12pF | | 75 | | μA |
| | | f _{HFXT} =48MHz, R _m =30Ω, C _L =12pF, C _m =6.26fF, L _m =1.76mH | | 600 | | |
| High frequency digital clock input (HFCLK_IN) | | | | | | |
| f _{HFIN} | HFCLK_IN frequency ⁽³⁾ | USEEXTHFCLK=1 | 4 | | 48 | MHz |
| DC _{HFIN} | HFCLK_IN duty cycle ⁽³⁾ | USEEXTHFCLK=1 | 40 | | 60 | % |

(1) This includes parasitic bond and package capacitance ($\approx 2\text{pF}$ per pin), calculated as $C_{\text{HFxIN}} \times C_{\text{HFxOUT}} / (C_{\text{HFxIN}} + C_{\text{HFxOUT}})$, where C_{HFxIN} and C_{HFxOUT} are the total capacitance at HFxIN and HFxOUT, respectively.

(2) The HFXT startup time (t_{start, HFXT}) is measured from the time the HFXT is enabled until stable oscillation for a typical crystal. Start-up time is dependent upon crystal frequency and crystal specifications. Refer to the HFXT section of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#). Current consumption increases with higher RSEL and start up time is decreases with higher RSEL.

(3) The digital clock input (HFCLK_IN) accepts a logic level square wave clock.

7.10 Digital IO

7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | |
|------------------|---------------------------|-----------------------------|---|---|---------|-------------------|------|--|
| V _{IH} | High level input voltage | ODIO ⁽¹⁾ | VDD ≥ 1.62V | 0.7*VDD | | 5.5 | V | |
| | | | VDD ≥ 2.7V | 2 | | 5.5 | V | |
| | | All I/O except ODIO & Reset | VDD ≥ 1.62V | 0.7*VDD | | VDD+0.3 | V | |
| V _{IL} | Low level input voltage | ODIO | VDD ≥ 1.62V | -0.3 | | 0.3*VDD | V | |
| | | | VDD ≥ 2.7V | -0.3 | | 0.8 | V | |
| | | All I/O except ODIO & Reset | VDD ≥ 1.62V | -0.3 | | 0.3*VDD | V | |
| V _{HYS} | Hysteresis | ODIO | | 0.05*VDD | | | V | |
| | | All I/O except ODIO | | 0.1*VDD | | | V | |
| I _{lkg} | High-Z leakage current | SDIO ^{(2) (3)} | | | | 50 ⁽⁴⁾ | nA | |
| R _{PU} | Pull up resistance | All I/O except ODIO | | | 40 | | kΩ | |
| R _{PD} | Pull down resistance | | | | 40 | | kΩ | |
| C _I | Input capacitance | | | | 5 | | pF | |
| V _{OH} | High level output voltage | SDIO | VDD ≥ 2.7V, I _{IO} _{max} = 6mA VDD ≥ 1.71V, I _{IO} _{max} = 2mA VDD ≥ 1.62V, I _{IO} _{max} = 1.5mA -40 °C ≤ T _j ≤ 25 °C | VDD-0.4 | | | V | |
| | | | VDD ≥ 2.7V, I _{IO} _{max} = 6mA VDD ≥ 1.71V, I _{IO} _{max} = 2mA VDD ≥ 1.62V, I _{IO} _{max} = 1.5mA -40 °C ≤ T _j ≤ 130 °C | VDD-0.45 | | | | |
| | | HSIO | VDD ≥ 2.7V, DRV=1, I _{IO} _{max} = 6mA VDD ≥ 1.71V, DRV=1, I _{IO} _{max} = 3mA VDD ≥ 1.62V, DRV=1, I _{IO} _{max} = 2mA -40 °C ≤ T _j ≤ 25 °C | VDD-0.4 | | | | |
| | | | VDD ≥ 2.7V, DRV=1, I _{IO} _{max} = 6mA VDD ≥ 1.71V, DRV=1, I _{IO} _{max} = 3mA VDD ≥ 1.62V, DRV=1, I _{IO} _{max} = 2mA -40 °C ≤ T _j ≤ 130 °C | VDD-0.4 | | | | |
| | | | VDD ≥ 2.7V, DRV=0, I _{IO} _{max} = 4mA VDD ≥ 1.71V, DRV=0, I _{IO} _{max} = 2mA VDD ≥ 1.62V, DRV=0, I _{IO} _{max} = 1.5mA -40 °C ≤ T _j ≤ 25 °C | VDD-0.45 | | | | |
| | | | VDD ≥ 2.7V, DRV=0, I _{IO} _{max} = 4mA VDD ≥ 1.71V, DRV=0, I _{IO} _{max} = 2mA VDD ≥ 1.62V, I _{IO} _{max} = 1.5mA -40 °C ≤ T _j ≤ 130 °C | VDD-0.45 | | | | |
| | | | HDIO | VDD ≥ 2.7V, DRV=1, I _{IO} _{max} = 20mA VDD ≥ 1.71V, DRV=1, I _{IO} _{max} = 10mA | VDD-0.4 | | | |
| | | | | VDD ≥ 2.7V, DRV=0, I _{IO} _{max} = 6mA VDD ≥ 1.71V, DRV=0, I _{IO} _{max} = 2mA | VDD-0.4 | | | |

7.10.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------|-----------------|--|-----|-----|------|------|
| V _{OL} | Low level output voltage | SDIO | VDD ≥ 2.7V, I _{IO} _{max} = 6mA VDD ≥ 1.71V, I _{IO} _{max} = 2mA VDD ≥ 1.62V, I _{IO} _{max} = 1.5mA -40 °C ≤ T _j ≤ 25 °C | | | 0.4 | V |
| | | SDIO | VDD ≥ 2.7V, I _{IO} _{max} = 6mA VDD ≥ 1.71V, I _{IO} _{max} = 2mA VDD ≥ 1.62V, I _{IO} _{max} = 1.5mA -40 °C ≤ T _j ≤ 130 °C | | | 0.45 | |
| | | HSIO | VDD ≥ 2.7V, DRV = 1, I _{IO} _{max} = 6mA VDD ≥ 1.71V, DRV = 1, I _{IO} _{max} = 3mA VDD ≥ 1.62V, DRV = 1, I _{IO} _{max} = 2mA T _j ≤ 85 °C | | | 0.4 | |
| | | HSIO | VDD ≥ 2.7V, DRV = 1, I _{IO} _{max} = 6mA VDD ≥ 1.71V, DRV = 1, I _{IO} _{max} = 3mA VDD ≥ 1.62V, DRV = 1, I _{IO} _{max} = 2mA -40 °C ≤ T _j ≤ 130 °C | | | 0.45 | |
| | | HSIO | VDD ≥ 2.7V, DRV = 0, I _{IO} _{max} = 4mA VDD ≥ 1.71V, DRV = 0, I _{IO} _{max} = 2mA VDD ≥ 1.62V, DRV = 0, I _{IO} _{max} = 1.5mA T _j ≤ 85 °C | | | 0.4 | |
| | | HSIO | VDD ≥ 2.7V, DRV = 0, I _{IO} _{max} = 4mA VDD ≥ 1.71V, DRV = 0, I _{IO} _{max} = 2mA VDD ≥ 1.62V, DRV = 0, I _{IO} _{max} = 1.5mA -40 °C ≤ T _j ≤ 130 °C | | | 0.45 | |
| | | HDIO | VDD ≥ 2.7V, DRV = 1, I _{IO} _{max} = 20mA VDD ≥ 1.71V, DRV = 1, I _{IO} _{max} = 10mA | | | 0.4 | |
| | | HDIO | VDD ≥ 2.7V, DRV = 0, I _{IO} _{max} = 6mA VDD ≥ 1.71V, DRV = 0, I _{IO} _{max} = 2mA | | | 0.4 | |
| | | ODIO | VDD ≥ 2.7V, I _{OL,max} = 8mA VDD ≥ 1.71V, I _{OL,max} = 4mA -40 °C ≤ T _j ≤ 25 °C | | | 0.4 | |
| | | ODIO | VDD ≥ 2.7V, I _{OL,max} = 8mA VDD ≥ 1.71V, I _{OL,max} = 4mA -40 °C ≤ T _j ≤ 130 °C | | | 0.45 | |

(1) I/O Types: ODIO = 5V Tolerant Open-Drain, SDIO = Standard-Drive, HSIO = High-Speed

(2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.

(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

(4) This value is for SDIO not muxed with any analog inputs. If the SDIO is muxed with analog inputs then the leakage can be as high as 100nA.

7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--|-----------------------|-----------------|---|-----|-----|-----|------|
| f _{max} | Port output frequency | SDIO | VDD ≥ 1.71V, C _L = 20pF | | | 16 | MHz |
| | | | VDD ≥ 2.7V, C _L = 20pF | | | 32 | |
| | | HSIO | VDD ≥ 1.71V, DRV = 0, C _L = 20pF | | | 16 | |
| | | | VDD ≥ 1.71V, DRV = 1, C _L = 20pF | | | 24 | |
| | | | VDD ≥ 2.7V, DRV = 0, C _L = 20pF | | | 32 | |
| | | HDIO | VDD ≥ 2.7V, DRV = 1, C _L = 20pF | | | 40 | |
| | | | VDD ≥ 1.71V, DRV = 0, C _L = 20pF | | | 16 | |
| | | ODIO | VDD ≥ 2.7V, DRV = 0, C _L = 20pF | | | 20 | |
| VDD ≥ 1.71V, FM ⁺ , C _L = 20pF - 100pF | | | | 1 | | | |

7.10.2 Switching Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------|-----------------------|------------------------------|--|-----------------------|-----|---------------------|------|
| t_r, t_f | Output rise/fall time | All output ports except ODIO | $V_{DD} \geq 1.71V$ | | | $0.3 \cdot f_{max}$ | s |
| t_f | Output fall time | ODIO | $V_{DD} \geq 1.71V, FM^+, CL = 20pF-100pF$ | $20 \cdot V_{DD}/5.5$ | | 120 | ns |

7.11 Analog Mux VBOOST

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|----------------------|--|-----|------|-----|---------|
| I_{VBST} | VBOOST current adder | MCLK/ULPCLK is LFCLK | | 0.7 | | μA |
| | | MCLK/ULPCLK is not LFCLK, SYSOSC frequency is 4MHz | | 10.6 | | |
| $t_{START,VBST}$ | VBOOST startup time | | | 12 | 20 | us |

7.12 ADC

7.12.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|--|------|--------------------|-----|------------|
| $V_{in(ADC)}$ | Analog input voltage range ⁽¹⁾ | Applies to all ADC analog input pins | 0 | | VDD | V |
| V_{R+} | Positive ADC reference voltage | V_{R+} sourced from VDD | | VDD | | V |
| | | V_{R+} sourced from external reference pin (VREF+) | 1.4 | | VDD | V |
| | | V_{R+} sourced from internal reference (VREF) | | VREF | | V |
| V_{R-} | Negative ADC reference voltage | | | 0 | | V |
| F_S | ADC sampling frequency | RES = 0x0 (12-bit mode) | | | 4 | MSPS |
| | | RES = 0x1 (10-bit mode) | | | 4 | |
| | | RES = 0x2 (8-bit mode), SCOMP = 2 | | | 5.3 | |
| $I_{(ADC)}$ | Operating supply current into VDD terminal | $F_S = 4MSPS, V_{R+} = V_{DD}$ | | 1.5 ⁽²⁾ | | mA |
| $C_{S/H}$ | ADC sample-and-hold capacitance | | | 3.3 | | pF |
| R_{in} | ADC input resistance | | | 0.5 | | k Ω |
| ENOB | Effective number of bits | External reference ⁽³⁾ | 10.9 | 11.1 | | bit |
| | | External reference ⁽⁴⁾ , HW Averaging Enabled, 16 Samples and 2bit shift | 12.3 | 12.5 | | |
| | | Internal reference, $V_{R+} = V_{REF} = 2.5V$ (VRSEL = 1h) ⁽⁵⁾ | 9.9 | 10.8 | | |
| | | Internal reference, $V_{R+} = V_{REF} = 2.5V$ (VRSEL = 2h) | | 9.2 | | |
| SNR | Signal-to-noise ratio | External reference ⁽³⁾ | | 68 | | dB |
| | | External reference ⁽⁴⁾ , HW Averaging Enabled, 16 Samples and 2bit shift | | 78 | | |
| | | Internal reference, $V_{R+} = V_{REF} = 2.5V$ (VRSEL = 1h) ⁽⁵⁾ | | 66 | | |
| | | Internal reference, $V_{R+} = V_{REF} = 2.5V$ (VRSEL = 2h) | | 57 | | |
| PSRR _{DC} | Power supply rejection ratio, DC | External reference ⁽³⁾ , $V_{DD} = V_{DD(min)}$ to $V_{DD(max)}$ | | 62 | | dB |
| | | $V_{DD} = V_{DD(min)}$ to $V_{DD(max)}$ Internal reference, $V_{R+} = V_{REF} = 2.5V$ | | 53 | | |
| PSRR _{AC} | Power supply rejection ratio, AC | External reference ⁽³⁾ , $\Delta V_{DD} = 0.1V$ at 1 kHz | | 61 | | dB |
| | | $\Delta V_{DD} = 0.1V$ at 1 kHz Internal reference, $V_{R+} = V_{REF} = 2.5V$ | | 52 | | |
| T_{wakeUp} | ADC Wakeup Time | Assumes internal reference is active | | | 5 | us |

7.12.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|---|------|-----|-----|------|
| V _{SupplyMon} | Supply Monitor voltage divider (VDD/3) accuracy | ADC input channel: Supply Monitor ⁽⁴⁾⁽⁶⁾ | -1.5 | | 1 | % |
| I _{SupplyMon} | Supply Monitor voltage divider current consumption | ADC input channel: Supply Monitor | | 10 | | μA |

- (1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
- (2) The internal reference (VREF) supply current is not included in current consumption parameter $I_{(ADC)}$.
- (3) All external reference specifications are measured with $V_{R+} = VREF+ = VDD = 3.3V$ and $V_{R-} = VREF- = VSS = 0V$ and external 1μF cap on VREF+ pin
- (4) Analog power supply monitor. Analog input on channel 15 is disconnected and is internally connected to the voltage divider which is VDD/3.
- (5) Please note that to achieve this ENOB using internal reference VREF, VRSEL bit in MEMCTL register needs to be set to the external reference mode. This will set the REFN as VREF- and REFP as VREF+. In this configuration, no external connections can be made on the VREF- and VREF+ pins. The REFN pin should be connected to device ground.
- (6) Characterized using external reference (VREFSEL = 1)

7.12.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|---|---------------------------|------|-----|---------------|
| f _{ADCCLK} | ADC clock frequency | | 4 | | 48 | MHz |
| t _{ADC trigger} | Software trigger minimum width | | 3 | | | ADCCLK cycles |
| t _{Sample} | Sampling time without OPA | 12-bit mode, R _S = 50Ω, C _{pext} = 10pF | 62.5 | | | ns |
| t _{Sample_PGA} | Sampling time with OPA ⁽¹⁾ | 12-bit mode | GBW = 0x1, PGA gain = x1 | 0.22 | | μs |
| | | | GBW = 0x1, PGA gain = x32 | 2.6 | | μs |
| t _{Sample_DAC} | Sampling time with DAC as input ⁽²⁾ | | 0.5 | | | μs |
| t _{Sample_GPAMP} | Sampling time with GPAMP | | 3 | | | μs |
| t _{Sample_SupplyMon} | Sample time with Supply Monitor (VDD/3) | | 5 | | | μs |

- (1) Only applies for devices with OPA
- (2) Only applies for devices with DAC

7.12.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25°C and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--|---|-----|-----|-----|------|
| E _I | Integral linearity error (INL) | External reference ⁽²⁾ | -2 | | 2 | LSB |
| E _D | Differential linearity error (DNL) No missing codes | External reference ⁽²⁾ | -1 | | 1 | LSB |
| E _O | Offset error | Internal or External reference ⁽²⁾ | -2 | | 2 | mV |
| E _G | Gain error | External reference ⁽²⁾ | -3 | | 3 | LSB |

- (1) Total Unadjusted Error (TUE) can be calculated from E_I, E_O, and E_G using the following formula: $TUE = \sqrt{(E_I)^2 + |E_O|^2 + E_G^2}$
Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate
- (2) All external reference specifications are measured with $V_{R+} = VREF+ = VDD$ and $V_{R-} = VSS = 0V$, external 1μF cap on VREF+ pin.

7.12.4 Typical Connection Diagram

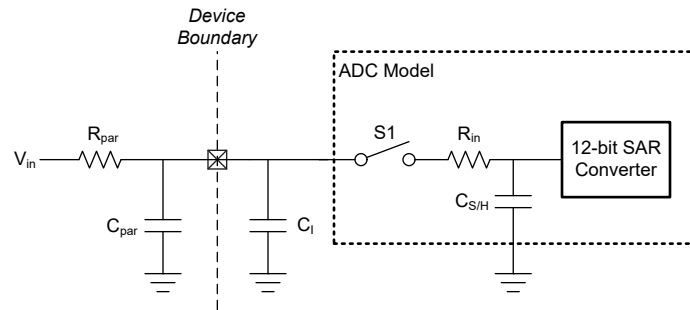


Figure 7-4. ADC Input Network

1. Refer to [ADC Electrical Characteristics](#) for the values of R_{in} and $C_{S/H}$
2. Refer to [Digital IO Electrical Characteristics](#) for the value of C_I
3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. $\tau = (R_{par} + R_{in}) \times C_{S/H} + R_{par} \times (C_{par} + C_I)$
2. $K = \ln(2^n / \text{Settling error}) - \ln((C_{par} + C_I) / C_{S/H})$
3. $T \text{ (Min sampling time)} = K \times \tau$

7.13 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|----------------------|---|--------------------------------|------|------|------|-------|
| TS _{TRIM} | Factory trim temperature ⁽¹⁾ | 27 | 30 | 33 | °C | |
| TS _c | Temperature coefficient | -40°C ≤ T _j ≤ 130°C | -1.9 | -1.8 | -1.7 | mV/°C |
| t _{SET, TS} | Temperature sensor settling time ⁽²⁾ | | | 10 | us | |

- (1) Higher absolute accuracy may be achieved through user calibration. Please refer to temperature sensor chapter in detailed description section.
- (2) This is the minimum required ADC sampling time when measuring the temperature sensor.

7.14 VREF

7.14.1 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--------------------|--|---------------|------|-----|------|---|
| VDD _{min} | Minimum supply voltage needed for VREF operation | BUFCONFIG = 0 | 2.7 | | V | |
| | | BUFCONFIG = 1 | 1.62 | | | |
| VREF | Voltage reference output voltage | BUFCONFIG = 1 | 1.38 | 1.4 | 1.42 | V |
| | | BUFCONFIG = 0 | 2.46 | 2.5 | 2.54 | |

7.14.2 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|---|-----|-----|-----|------|
| I _{VREF} | VREF operating supply current | | 166 | 330 | μA |
| I _{Drive} | VREF output drive strength ⁽¹⁾ | | | 100 | μA |
| I _{Sc} | VREF short circuit current | | | 100 | mA |

7.14.2 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---------------|---|---|-----------------|-------|-----|------|---------------|
| TC_{VREF} | Temperature coefficient of VREF (Bandgap+VRBUF) ⁽³⁾ | BUFCONFIG = {1} | BUFCONFIG = {1} | | | 75 | ppm/°C |
| TC_{VREF} | Temperature coefficient of VREF (Bandgap+VRBUF) ⁽³⁾ | BUFCONFIG = {0} | BUFCONFIG = {0} | | | 75 | ppm/°C |
| TC_{drift} | Long term VREF drift | Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25°C | | | | 300 | ppm |
| $PSRR_{DC}$ | VREF Power supply rejection ratio, DC | VDD = 1.7 V to VDDmax, BUFCONFIG = 1 | | -57 | -63 | | dB |
| | | VDD = 2.7 V to VDDmax, BUFCONFIG = 0 | | -49 | -53 | | |
| V_{noise} | RMS noise at VREF output (0.1 Hz to 100 MHz) | BUFCONFIG = 1 | | | 500 | | μV_{rms} |
| | | BUFCONFIG = 0 | | | 900 | | |
| C_{VREF} | Recommended VREF decoupling capacitor on VREF+ pin ^{(3) (4) (5)} | | | 0.7 | 1 | 1.15 | μF |
| $T_{startup}$ | VREF startup time | | | | | 200 | μS |
| $T_{refresh}$ | VREF External capacitor refresh time | BUFCONFIG = {0, 1}, VDD = 2.8 V, C_{VREF} = 1 μF | | 31.25 | | | |

- (1) The specified MAX output drive strength is supported regardless of which peripherals are being used in the device.
- (2) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.
- (3) Decoupling capacitor (C_{VREF}) is required when using the internal voltage reference VREF and should be connected from the VREF+ pin to VREF-/GND. When using the VREF+/- pins to supply an external reference, a decoupling capacitor value should be selected based on the external reference source.
- (4) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to $\pm 20\%$ tolerance is acceptable
- (5) The VREF module should only be enabled when C_{VREF} is connected and should not be enabled otherwise.

7.15 GPAMP

7.15.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------|--|--|---------------|------------|------------|---------|------------------|
| V_{CM} | Common mode voltage range | RRI = 0x0 | | -0.1 | | VDD-1 | V |
| | | RRI = 0x1 | | 1 | | VDD-0.2 | |
| | | RRI = 0x2 | | -0.1 | | VDD-0.2 | |
| I_q | Quiescent current, per op-amp | I_O = 0 mA, RRI = 0x0 | | | 97 | | μA |
| | | I_O = 0 mA, RRI = 0x1 or 0x2 | | | 93 | | |
| GBW | Gain-bandwidth product | C_L = 200pF | | | 0.32 | | MHz |
| V_{OS} | Input offset voltage | Noninverting, unity gain, T_A = 25°C, VDD = 3.3V | CHOP = 0x0 | ± 0.2 | ± 6.5 | | mV |
| | | | CHOP = 0x1 | ± 0.08 | ± 0.4 | | |
| dV_{OS}/dT | Input offset voltage temperature drift | Noninverting, unity gain | CHOP = 0x0 | | 7.7 | | $\mu V/^\circ C$ |
| | | | CHOP = 0x1 | | 0.34 | | |
| I_{bias} | Input bias for muxed I/O pin at SoC | 0.1V < V_{in} < VDD-0.3V, VDD=3.3V, CHOP=0x0 | T_A = 25°C | | ± 40 | | pA |
| | | | T_A = 125°C | | ± 4000 | | |
| | | 0.1V < V_{in} < VDD-0.3V, VDD=3.3V, CHOP = 0x1 | T_A = 25°C | | ± 200 | | |
| | | | T_A = 125°C | | ± 4000 | | |
| $CMRR_{DC}$ | Common mode rejection ratio, DC | Over common mode voltage range | CHOP = 0x0 | 48 | 77 | | dB |
| | | | CHOP = 0x1 | 56 | 105 | | |
| e_n | Input voltage noise density | Noninverting, unity gain | f = 1 kHz | | 43 | | nV/ \sqrt{Hz} |
| e_n | | | f = 10 kHz | | 19 | | |
| R_{in} | Input resistance ⁽¹⁾ | | | | 0.65 | | k Ω |

7.15.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|-----------------------------------|---|-----|-------|-----|--------|
| C _{in} | Input capacitance | Common mode | | 4 | | pF |
| | | Differential | | 2 | | |
| A _{OL} | Open-loop voltage gain, DC | R _L = 350 kΩ, 0.3 < V _o < VDD-0.3 | 82 | 90 | 107 | dB |
| PM | phase margin | C _L = 200 pF, R _L = 350 kΩ | 69 | 70 | 72 | degree |
| SR | Slew rate | Noninverting, unity gain, C _L = 40 pF | | 0.32 | | V/μs |
| THDN | Total Harmonic Distortion + Noise | | | 0.012 | | % |
| I _{Load} | Output load current | | | 4 | | mA |
| C _{Load} | Output load capacitance | | | | 200 | pF |

(1) R_{in} here means the input resistance of mux in GPAMP.

7.15.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------|---------------------|---|-----|-----|-----|---------------|
| t _{EN} | GPAMP enable time | ENABLE = 0x0 to 0x1, Bandgap reference ON, 0.1% | | 12 | 20 | μs |
| t _{disable} | GPAMP disable time | | | 4 | | ULPCLK Cycles |
| t _{SETTLE} | GPAMP settling time | C _L = 200 pF, Vstep = 0.3V to VDD - 0.3V, 0.1%, ENABLE = 0x1 | | 9 | | μs |

7.16 I2C

7.16.1 I²C Timing Diagram

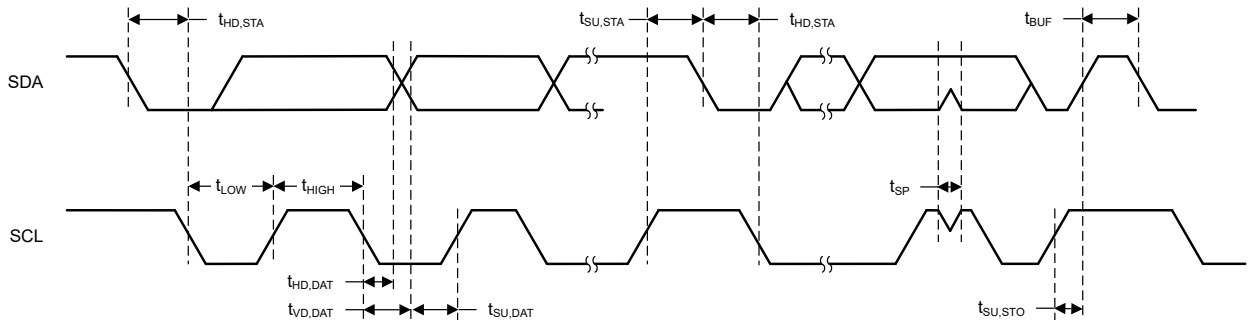


Figure 7-5. I2C Timing Diagram

7.16.2 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | TEST CONDITIONS | Standard mode | | Fast mode | | Fast mode plus | | UNIT |
|---------------------|---------------------------------|---------------|-----|-----------|-----|----------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{I2C} | I2C input clock frequency | 2 | 32 | 8 | 32 | 20 | 32 | MHz |
| f _{SCL} | SCL clock frequency | | 0.1 | | 0.4 | | 1 | MHz |
| t _{HD,STA} | Hold time (repeated) START | 4 | | 0.6 | | 0.26 | | us |
| t _{LOW} | LOW period of the SCL clock | 4.7 | | 1.3 | | 0.5 | | us |
| t _{HIGH} | High period of the SCL clock | 4 | | 0.6 | | 0.26 | | us |
| t _{SU,STA} | Setup time for a repeated START | 4.7 | | 0.6 | | 0.26 | | us |

7.16.2 I2C Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | Standard mode | | Fast mode | | Fast mode plus | | UNIT |
|--------------|--|-----------------|---------------|------|-----------|-----|----------------|------|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{HD,DAT}$ | Data hold time | | 0 | | 0 | | 0 | | ns |
| $t_{SU,DAT}$ | Data setup time | | 250 | | 100 | | 50 | | ns |
| $t_{SU,STO}$ | Setup time for STOP | | 4 | | 0.6 | | 0.26 | | us |
| t_{BUF} | bus free time between a STOP and START condition | | 4.7 | | 1.3 | | 0.5 | | us |
| $t_{VD,DAT}$ | data valid time | | | 3.45 | | 0.9 | | 0.45 | us |
| $t_{VD,ACK}$ | data valid acknowledge time | | | 3.45 | | 0.9 | | 0.45 | us |

7.16.3 I2C Filter

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|---|-----------------|-----|-----|-----|------|
| f_{SP} | Pulse duration of spikes suppressed by input filter | AGFSELx = 0 | | 6 | | ns |
| | | AGFSELx = 1 | | 14 | 35 | ns |
| | | AGFSELx = 2 | | 22 | 60 | ns |
| | | AGFSELx = 3 | | 35 | 90 | ns |

7.17 SPI

7.17.1 SPI

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|---------------------|---|-----|-----|-----|------|
| SPI | | | | | | |
| f_{SPI} | SPI clock frequency | Clock max speed = 32MHz 1.62 < VDD < 3.6V Controller mode | | | 16 | MHz |
| f_{SPI} | SPI clock frequency | Clock max speed = 32MHz 1.62 < VDD < 3.6V Peripheral mode | | | 16 | MHz |
| f_{SPI} | SPI clock frequency | Clock max speed >= 32MHz 1.62 < VDD < 3.6V Controller mode | | | 16 | MHz |
| f_{SPI} | SPI clock frequency | Clock max speed >= 48MHz 1.62 < VDD < 2.7V Controller mode with High speed IO | | | 24 | MHz |
| f_{SPI} | SPI clock frequency | Clock max speed >= 64MHz 2.7 < VDD < 3.6V Controller mode with High speed IO | | | 32 | MHz |
| f_{SPI} | SPI clock frequency | Clock max speed >= 32MHz 1.62 < VDD < 3.6V Peripheral mode | | | 16 | MHz |
| f_{SPI} | SPI clock frequency | Clock max speed >= 48MHz 1.62 < VDD < 2.7V Peripheral mode with High speed IO | | | 24 | MHz |
| f_{SPI} | SPI clock frequency | Clock max speed >= 64MHz 2.7 < VDD < 3.6V Peripheral mode with High speed IO | | | 32 | MHz |
| DC_{SCK} | SCK Duty Cycle | | 40 | 50 | 60 | % |
| Controller | | | | | | |

7.17.1 SPI (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|---|---------------------------|----------------------|---------------------------|------|
| t _{SCLK_H/L} | SCLK High or Low time | | (t _{SPI/2}) - 1 | t _{SPI} / 2 | (t _{SPI/2}) + 1 | ns |
| t _{CS.LEAD} | CS lead-time, CS active to clock | SPH=0 | 1 SPI Clock | | | |
| t _{CS.LEAD} | CS lead-time, CS active to clock | SPH=1 | 1/2 SPI Clock | | | |
| t _{CS.LAG} | CS lag time, Last clock to CS inactive | | 1 SPI Clock | | | |
| t _{CS.ACC} | CS access time, CS active to PICO data out | | | | 1/2 SPI Clock | |
| t _{CS.DIS} | CS disable time, CS inactive to PICO high impedance | | | | 1 SPI Clock | |
| t _{SU.CI} | POCI input data setup time ⁽¹⁾ | 2.7 < VDD < 3.6V, delayed sampling enabled | 1 | | | ns |
| t _{SU.CI} | POCI input data setup time ⁽¹⁾ | 1.62 < VDD < 2.7V, delayed sampling enabled | 1 | | | ns |
| t _{SU.CI} | POCI input data setup time ⁽¹⁾ | 2.7 < VDD < 3.6V, no delayed sampling | 29 | | | ns |
| t _{SU.CI} | POCI input data setup time ⁽¹⁾ | 1.62 < VDD < 2.7V, no delayed sampling | 37 | | | ns |
| t _{HD.CI} | POCI input data hold time | delayed sampling enabled | 24 | | | ns |
| t _{HD.CI} | POCI input data hold time | no delayed sampling | 0 | | | ns |
| t _{VALID.CO} | PICO output data valid time ⁽²⁾ | | | | 10 | ns |
| t _{HD.CO} | PICO output data hold time ⁽³⁾ | | 6 | | | ns |
| Peripheral | | | | | | |
| t _{CS.LEAD} | CS lead-time, CS active to clock | | 11 | | | ns |
| t _{CS.LAG} | CS lag time, Last clock to CS inactive | | 1 | | | ns |
| t _{CS.ACC} | CS access time, CS active to POCI data out | | | | 26 | ns |
| t _{CS.DIS} | CS disable time, CS inactive to POCI high impedance | | | | 26 | ns |
| t _{SU.PI} | PICO input data setup time | | 7 | | | ns |
| t _{HD.PI} | PICO input data hold time | | 0 | | | ns |
| t _{VALID.PO} | POCI output data valid time ⁽²⁾ | 2.7 < VDD < 3.6V | | | 25 | ns |
| t _{VALID.PO} | POCI output data valid time ⁽²⁾ | 1.62 < VDD < 2.7V | | | 31 | ns |
| t _{HD.PO} | POCI output data hold time ⁽³⁾ | | 5 | | | ns |

- (1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.17.2 SPI Timing Diagram

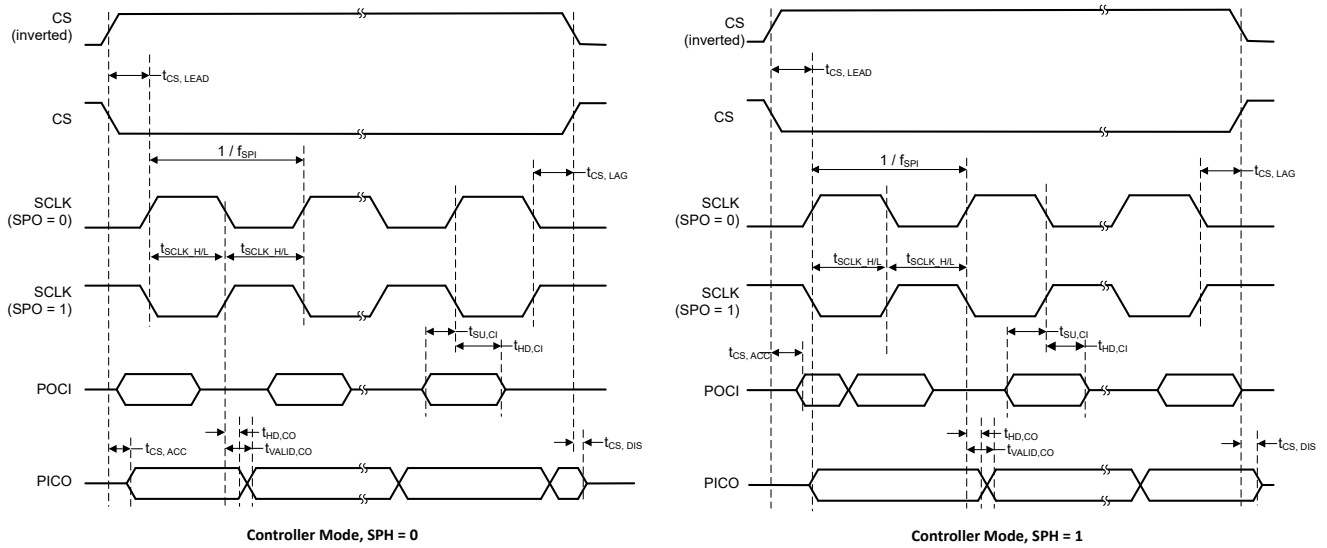


Figure 7-6. SPI Timing Diagram - Controller Mode

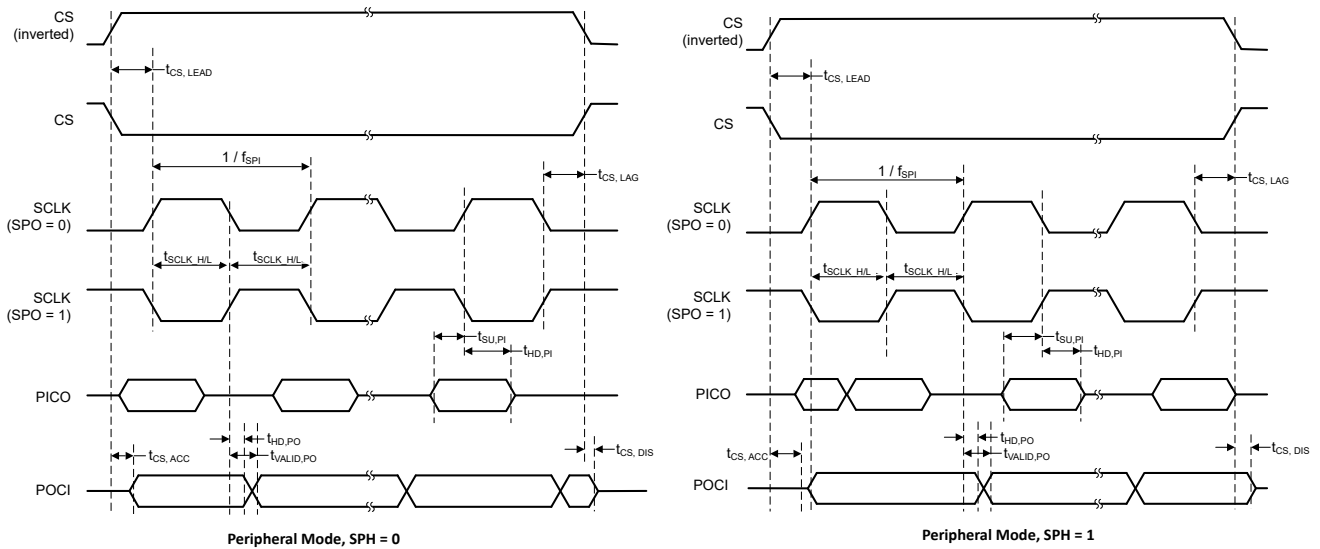


Figure 7-7. SPI Timing Diagram - Peripheral Mode

7.18 UART

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---|-----------------------|-----|-----|-----|------|
| f_{UART} | UART input clock frequency | UART in Power Domain1 | | | 80 | MHz |
| f_{UART} | UART input clock frequency | UART in Power Domain0 | | | 40 | MHz |
| f_{BITCLK} | BITCLK clock frequency(equals baud rate in MBaud) | UART in Power Domain1 | | | 10 | MHz |
| f_{BITCLK} | BITCLK clock frequency(equals baud rate in MBaud) | UART in Power Domain0 | | | 5 | MHz |

7.18 UART (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---|-----------------|-----|-----|-----|------|
| t _{SP} | Pulse duration of spikes suppressed by input filter | AGFSELx = 0 | | 6 | | ns |
| | | AGFSELx = 1 | | 14 | 35 | ns |
| | | AGFSELx = 2 | | 22 | 60 | ns |
| | | AGFSELx = 3 | | 35 | 90 | ns |

7.19 TIMx

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|-----------------------|--|------|-----|-----|----------------------|
| t _{res} | Timer resolution time | TIMx in Power Domain 1, f _{TIMxCLK} = 80MHz | 12.5 | | | ns |
| | | TIMx in Power Domain 0, f _{TIMxCLK} = 40MHz | 25 | | | ns |
| | | | 1 | | | t _{TIMxCLK} |

7.20 Emulation and Debug

7.20.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---------------|-----------------|-----|-----|-----|------|
| f _{SWD} | SWD frequency | | | | 10 | MHz |

8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.1 CPU

The CPU sub system (MCPUSS) implements an Arm Cortex-M0+ CPU, an instruction pre-fetch/cache, a system timer, a memory protection unit, and interrupt management features. The Arm Cortex-M0+ is a cost-optimized, 32-bit CPU which delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- Arm Cortex-M0+ CPU supporting clock frequencies from 32kHz to 80 MHz
 - Armv6-M Thumb instruction set (little endian) with single-cycle 32x32 multiply instruction
 - Single-cycle access to GPIO registers via Arm single-cycle IO port
- Pre-fetch logic to improve sequential code execution, and I-cache with 4 64-bit cache lines
- System timer (SysTick) with 24-bit down counter and automatic reload
- Memory protection unit (MPU) with 8 programmable regions
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail-chaining
- Interrupt groups for expanding the total interrupt sources, with jump index for low interrupt latency

8.2 Operating Modes

MSPM0G MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST, SWD, or a logic level match on certain IOs. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (for example, RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0G devices implement two power domains: PD1 (for the CPU, memories, and high performance peripherals), and PD0 (for low speed, low power peripherals). PD1 is always powered in RUN and SLEEP modes, but is disabled in all other modes. PD0 is always powered in RUN, SLEEP, STOP, and STANDBY modes. PD1 and PD0 are both disabled in SHUTDOWN mode.

8.2.1 Functionality by Operating Mode (MSPM0G110x)

Supported functionality in each operating mode is given in [Table 8-1](#).

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode, but its use is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained. When waking up from an OFF state, all module registers must be re-configured to the desired settings by application software.

Table 8-1. Supported Functionality by Operating Mode

| OPERATING MODE | | RUN | | | SLEEP | | | STOP | | | STANDBY | | SHUTDOWN |
|-----------------|-----------------------------|--------------------|------|------|--------|--------|--------|--------------------------|-------|-------|--------------------|----------|----------|
| | | RUN0 | RUN1 | RUN2 | SLEEP0 | SLEEP1 | SLEEP2 | STOP0 | STOP1 | STOP2 | STANDBY0 | STANDBY1 | |
| Oscillators | SYSOSC | EN | EN | DIS | EN | EN | DIS | OPT ⁽¹⁾ | EN | DIS | DIS | DIS | OFF |
| | LFOSC or LFXT | EN (LFOSC or LFXT) | | | | | | | | | | OFF | |
| | HFXT | OPT | DIS | DIS | OPT | DIS | DIS | DIS | DIS | DIS | DIS | DIS | OFF |
| | SYSPLL | OPT | DIS | DIS | OPT | DIS | DIS | DIS | DIS | DIS | DIS | DIS | OFF |
| Clocks | CPUCLK | 80M | 32k | 32k | DIS | | | | | | | | OFF |
| | MCLK to PD1 | 80M | 32k | 32k | 80M | 32k | 32k | DIS | | | | | OFF |
| | ULPCLK to PDO | 40M | 32k | 32k | 40M | 32k | 32k | 4M ⁽¹⁾ | 4M | 32k | DIS | DIS | OFF |
| | ULPCLK to TIMG0, TIMG8 | 40M | 32k | 32k | 40M | 32k | 32k | 4M ⁽¹⁾ | 4M | 32k | DIS | DIS | OFF |
| | RTCCLK | 32kHz | | | | | | | | | | OFF | |
| | MFCLK | OPT | DIS | DIS | OPT | DIS | DIS | OPT | DIS | DIS | DIS | DIS | OFF |
| | MFPCLK | OPT | DIS | DIS | OPT | DIS | DIS | OPT | DIS | DIS | DIS | DIS | OFF |
| | LFCLK | 32k | | | | | | | | | | DIS | OFF |
| | LFCLK to TIMG0, TIMG8 | 32k | | | | | | | | | | OFF | |
| | LFCLK Monitor | OPT | | | | | | | | | | OFF | |
| | MCLK Monitor | OPT | | | | | | | | | | DIS | OFF |
| PMU | POR monitor | EN | | | | | | | | | | | |
| | BOR monitor | EN | | | | | | | | | | | OFF |
| | Core regulator | FULL DRIVE | | | | | | REDUCED DRIVE | | | LOW DRIVE | | OFF |
| Core Functions | CPU | EN | | | DIS | | | | | | | | OFF |
| | DMA | OPT | | | | | | DIS (triggers supported) | | | | | OFF |
| | Flash | EN | | | | | | DIS | | | | | OFF |
| | SRAM | EN | | | | | | DIS | | | | | OFF |
| PD1 Peripherals | CRC | OPT | | | | | | DIS | | | | | OFF |
| | UART3 | OPT | | | | | | OFF | | | | | |
| | SPI0, SPI1 | OPT | | | | | | OFF | | | | | |
| | TIMA0, TIMA1 | OPT | | | | | | OFF | | | | | |
| | TIMG6, TIMG7 | OPT | | | | | | OFF | | | | | |
| | TIMG12 | OPT | | | | | | OFF | | | | | |
| PD0 Peripherals | TIMG0, TIMG8 | OPT | | | | | | | | | | OFF | |
| | RTC | OPT | | | | | | | | | | OFF | |
| | UART0, UART1, UART2 | OPT | | | | | | | | | OPT ⁽²⁾ | OFF | |
| | I2C0, I2C1 | OPT | | | | | | | | | OPT ⁽²⁾ | OFF | |
| | GPIOA, GPIOB ⁽³⁾ | OPT | | | | | | | | | OPT ⁽²⁾ | OFF | |
| | WWDT0, WWDT1 | OPT | | | | | | | | | DIS | OFF | |
| Analog | ADC0, ADC1 ⁽³⁾ | OPT | | | | | | NS (triggers supported) | | | | | OFF |
| | GPAMP | OPT | | | | | | | | | NS | OFF | |

Table 8-1. Supported Functionality by Operating Mode (continued)

| OPERATING MODE | RUN | | | SLEEP | | | STOP | | | STANDBY | | SHUTDOWN |
|---------------------|------|------|------|---------|--------|--------|---------|-------|-------|---------------------|----------|----------------|
| | RUN0 | RUN1 | RUN2 | SLEEP0 | SLEEP1 | SLEEP2 | STOP0 | STOP1 | STOP2 | STANDBY0 | STANDBY1 | |
| IOMUX and IO Wakeup | EN | | | | | | | | | | | DIS w/ WAKE |
| Wake Sources | N/A | | | ANY IRQ | | | PD0 IRQ | | | IOMUX, NRST, SWD | | |

- (1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as it was in RUN1, and ULPCCLK remains at 32 kHz as it was in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as it was in RUN2, and ULPCCLK remains at 32 kHz as it was in RUN2.
- (2) When using the STANDBY1 policy for STANDBY, only TIMG0/8 and the RTC are clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity, but they are not actively clocked.
- (3) For ADCx and GPIO Ports A and B, the digital logic is in PD0 and the register interface is in PD1. These peripherals support fast single-cycle register access when PD1 is active and also support basic operation down to STANDBY mode where PD0 is still active.

8.3 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brownout reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption
- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.4 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32 kHz)
- **SYSOSC**: Internal high-frequency oscillator (4 MHz or 32 MHz with factory trim, 16 MHz or 24 MHz with user trim)
- **LFXT/LFCKIN**: Low-frequency external crystal oscillator or digital clock input (32 kHz)
- **HFXT/HFCKIN**: High-frequency external crystal oscillator or digital clock input (4 to 48 MHz)
- **SYSPLL**: System phase locked loop with 3 outputs (32 to 80 MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC, LFCLK, or HSCLK, active in RUN and SLEEP modes
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4-MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **MFPCCLK**: 4-MHz fixed mid-frequency precision clock, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32-kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes
- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes
- **HFCLK**: High-frequency clock derived from HFXT or HFCLK_IN, available in RUN and SLEEP mode
- **HSCLK**: High-speed clock derived from HFCLK or the SYSPLL, available in RUN and SLEEP mode

For more details, see the CKM chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.5 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA in these devices support the following key features:

- 7 independent DMA transfer channels
 - 3 full-feature channel (DMA0, DMA1 and DMA2), supporting repeated transfer modes
 - 4 basic channels (DMA3, DMA4, DMA5 and DMA6) supporting single transfer modes
- Configurable DMA channel priorities
- Byte (8-bit), short word (16-bit), word (32-bit) and long word (64-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection
- Active channel interruption to service other channels
- Early interrupt generation for ping-pong buffer architecture
- Cascading channels upon completion of activity on another channel
- Stride mode to support data re-organization, such as 3-phase metering applications

[Table 8-2](#) lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Table 8-2. DMA Trigger Mapping

| Trigger 0:12 | Source | Trigger 13:24 | Source |
|--------------|-------------------------------|---------------|-------------------|
| 0 | Software | 13 | SPI1 Publisher 1 |
| 1 | Generic Subscriber 0 (FSUB_0) | 14 | SPI1 Publisher 2 |
| 2 | Generic Subscriber 1 (FSUB_1) | 15 | UART3 Publisher 1 |
| 7 | I2C0 Publisher 1 | 20 | UART1 Publisher 2 |
| 8 | I2C0 Publisher 2 | 21 | UART2 Publisher 1 |
| 9 | I2C1 Publisher 1 | 22 | UART2 Publisher 2 |
| 10 | I2C1 Publisher 2 | 23 | ADC0 Publisher 2 |
| 11 | SPI0 Publisher 1 | 24 | ADC1 Publisher 2 |
| 12 | SPI0 Publisher 2 | | |

For more details, see the DMA chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.6 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA, or the CPU). The event manager implements event transfer through a defined set of event publishers (generators) and subscribers (receivers) which are interconnected through an event fabric containing a combination of static and programmable routes.

Events that are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
 - Example: RTC interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
 - Example: UART data receive trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)

- Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

Refer to the Event chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#) for more information.

Table 8-3. Generic Event Channels

A generic route is either a point-to-point (1:1) route or a point-to-two (1:2) splitter route in which the peripheral publishing the event is configured to use one of several available generic route channels to publish its event to another entity (or entities, in the case of a splitter route), where an entity may be another peripheral, a generic DMA trigger event, or a generic CPU event.

| CHANID | Generic Route Channel Selection | Channel Type |
|--------|-----------------------------------|------------------|
| 0 | No generic event channel selected | N/A |
| 1 | Generic event channel 1 selected | 1 : 1 |
| 2 | Generic event channel 2 selected | 1 : 1 |
| 3 | Generic event channel 3 selected | 1 : 1 |
| 4 | Generic event channel 4 selected | 1 : 1 |
| 5 | Generic event channel 5 selected | 1 : 1 |
| 6 | Generic event channel 6 selected | 1 : 1 |
| 7 | Generic event channel 7 selected | 1 : 1 |
| 8 | Generic event channel 8 selected | 1 : 1 |
| 9 | Generic event channel 9 selected | 1 : 1 |
| 10 | Generic event channel 10 selected | 1 : 1 |
| 11 | Generic event channel 11 selected | 1 : 1 |
| 12 | Generic event channel 12 selected | 1 : 2 (splitter) |
| 13 | Generic event channel 13 selected | 1 : 2 (splitter) |
| 14 | Generic event channel 14 selected | 1 : 2 (splitter) |
| 15 | Generic event channel 15 selected | 1 : 2 (splitter) |

8.7 Memory

8.7.1 Memory Organization

The following table summarizes the memory map of the devices. For more information about the memory region detail, see [Platform Memory Map](#) section in the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

Table 8-4. Memory Organization

| MEMORY REGION | SUBREGION | MSPM0G1105 | MSPM0G1106 | MSPM0G1107 |
|---------------|-----------------|---|---|--|
| Code (Flash) | ECC Corrected | 32KB-8B ⁽¹⁾ 0x0000.0000 to 0x0000.7FF8 | 64KB-8B ⁽¹⁾ 0x0000.0000 to 0x0000.FFF8 | 128KB-8B ⁽¹⁾ 0x0000.0000 to 0x0001.FFF8 |
| | ECC Uncorrected | 0x0040.0000 to 0x0040.7FF8 | 0x0040.0000 to 0x0040.FFF8 | 0x0040.0000 to 0x0041.FFF8 |
| SRAM (SRAM) | Parity checked | 0x2010.0000 to 0x2010.3FFF | 0x2010.0000 to 0x2010.7FFF | 0x2010.0000 to 0x2010.7FFF |
| | Unchecked | 0x2020.0000 to 0x2020.3FFF | 0x2020.0000 to 0x2020.7FFF | 0x2020.0000 to 0x2020.7FFF |
| | Parity code | 0x2030.0000 to 0x2030.3FFF | 0x2030.0000 to 0x2030.7FFF | 0x2030.0000 to 0x2030.7FFF |

Table 8-4. Memory Organization (continued)

| MEMORY REGION | SUBREGION | MSPM0G1105 | MSPM0G1106 | MSPM0G1107 |
|---------------|--|--|--|--|
| Peripheral | Peripherals | 0x4000.0000 to 0x40FF.FFFF | 0x4000.0000 to 0x40FF.FFFF | 0x4000.0000 to 0x40FF.FFFF |
| | Flash ECC Corrected | 0x4100.0000 to 0x4100.8000 | 0x4100.0000 to 0x4101.0000 | 0x4100.0000 to 0x4102.0000 |
| | Flash ECC Uncorrected | 0x4140.0000 to 0x4140.8000 | 0x4140.0000 to 0x4141.0000 | 0x4140.0000 to 0x4142.0000 |
| | Flash ECC code | 0x4180.0000 to 0x4180.8000 | 0x4180.0000 to 0x4181.0000 | 0x4180.0000 to 0x4182.0000 |
| | Configuration NVM (NONMAIN) ECC Corrected | 512 bytes 0x41C0.0000 to 0x41C0.0200 | 512 bytes 0x41C0.0000 to 0x41C0.0200 | 512 bytes 0x41C0.0000 to 0x41C0.0200 |
| | Configuration NVM(NONMAIN) ECC Uncorrected | 0x41C1.0000 to 0x41C1.0200 | 0x41C1.0000 to 0x41C1.0200 | 0x41C1.0000 to 0x41C1.0200 |
| | Configuration NVM(NONMAIN) ECC code | 0x41C2.0000 to 0x41C2.0200 | 0x41C2.0000 to 0x41C2.0200 | 0x41C2.0000 to 0x41C2.0200 |
| | FACTORY Corrected | 0x41C4.0000 to 0x41C4.0080 | 0x41C4.0000 to 0x41C4.0080 | 0x41C4.0000 to 0x41C4.0080 |
| | FACTORY Uncorrected | 0x41C5.0000 to 0x41C5.0080 | 0x41C5.0000 to 0x41C5.0080 | 0x41C5.0000 to 0x41C5.0080 |
| | FACTORY ECC code | 0x41C6.0000 to 0x41C6.0080 | 0x41C6.0000 to 0x41C6.0080 | 0x41C6.0000 to 0x41C6.0080 |
| Subsystem | 0x6000.0000 to 0x7FFF.FFFF | 0x6000.0000 to 0x7FFF.FFFF | 0x6000.0000 to 0x7FFF.FFFF | |
| System PPB | 0xE000.0000 to 0xE00F.FFFF | 0xE000.0000 to 0xE00F.FFFF | 0xE000.0000 to 0xE00F.FFFF | |

(1) The first 32KB flash memory (address 0x0000.0000 to 0x0000.8000) has up to 100000 program/erase cycles.

8.7.2 Peripheral File Map

Table 8-5 lists the available peripherals and the register base address for each.

Table 8-5. Peripherals Summary

| Peripheral Name | Base Address | Size |
|-----------------|--------------|--------|
| VREF | 0x40030000 | 0x2000 |
| WWDT0 | 0x40080000 | 0x2000 |
| WWDT1 | 0x40082000 | 0x2000 |
| TIMG0 | 0x40084000 | 0x2000 |
| TIMG8 | 0x40090000 | 0x2000 |
| RTC | 0x40094000 | 0x2000 |
| GPIO0 | 0x400A0000 | 0x2000 |
| GPIO1 | 0x400A2000 | 0x2000 |
| SYCTL | 0x400AF000 | 0x3000 |
| DEBUGSS | 0x400C7000 | 0x2000 |
| EVENT | 0x400C9000 | 0x3000 |
| NVMNW | 0x400CD000 | 0x2000 |
| I2C0 | 0x400F0000 | 0x2000 |
| I2C1 | 0x400F2000 | 0x2000 |
| UART1 | 0x40100000 | 0x2000 |
| UART2 | 0x40102000 | 0x2000 |

Table 8-5. Peripherals Summary (continued)

| Peripheral Name | Base Address | Size |
|---------------------|--------------|--------|
| UART0 | 0x40108000 | 0x2000 |
| MCPUSS | 0x40400000 | 0x2000 |
| MATHACL | 0x40410000 | 0x2000 |
| WUC | 0x40424000 | 0x1000 |
| IOMUX | 0x40428000 | 0x2000 |
| DMA | 0x4042A000 | 0x2000 |
| CRC | 0x40440000 | 0x2000 |
| SPI0 | 0x40468000 | 0x2000 |
| SPI1 | 0x4046A000 | 0x2000 |
| UART3 | 0x40500000 | 0x2000 |
| ADC0 | 0x40000000 | 0x1000 |
| ADC1 | 0x40002000 | 0x1000 |
| ADC0 ⁽¹⁾ | 0x40556000 | 0x1000 |
| ADC1 ⁽¹⁾ | 0x40558000 | 0x1000 |
| TIMA0 | 0x40860000 | 0x2000 |
| TIMA1 | 0x40862000 | 0x2000 |
| TIMG6 | 0x40868000 | 0x2000 |
| TIMG7 | 0x4086A000 | 0x2000 |
| TIMG12 | 0x40870000 | 0x2000 |

(1) Aliased region of ADC0 and ADC1 memory-mapped registers

8.7.3 Peripheral Interrupt Vector

Table 8-6 shows the IRQ number and the interrupt group number for each peripherals in this device.

Table 8-6. Interrupt Vector Number

| Peripheral Name | NVIC IRQ | Group IIDX |
|-----------------|----------|------------|
| WWDT0 | 0 | 0 |
| WWDT1 | 0 | 1 |
| DEBUGSS | 0 | 2 |
| NVMNW | 0 | 3 |
| EVENT SUB PORT0 | 0 | 4 |
| EVENT SUB PORT1 | 0 | 5 |
| SYSCTL | 0 | 6 |
| GPIO0 | 1 | 0 |
| GPIO1 | 1 | 1 |
| TIMG8 | 2 | - |
| UART3 | 3 | - |
| ADC0 | 4 | - |
| ADC1 | 5 | - |
| SPI0 | 9 | - |
| SPI1 | 10 | - |
| UART1 | 13 | - |
| UART2 | 14 | - |
| UART0 | 15 | - |
| TIMG0 | 16 | - |
| TIMG16 | 17 | - |
| TIMA0 | 18 | - |
| TIMA1 | 19 | - |
| TIMG7 | 20 | - |
| TIMG12 | 21 | - |
| I2C0 | 24 | - |
| I2C1 | 25 | - |
| RTC | 30 | - |
| DMA | 31 | - |

8.8 Flash Memory

A single bank of non-volatile flash memory is provided for storing executable program code and application data.

Key features of the flash include:

- Hardware ECC protection (encode and decode) with single bit error correction and double-bit error detection
- In-circuit program and erase operations supported across the entire recommended supply range
- Small 1KB sector sizes (minimum erase resolution of 1KB)
- Up to 100,000 program/erase cycles on the lower 32KB of the flash memory, with up to 10,000 program/erase cycles on the remaining flash memory (devices with 32KB support 100,000 cycles on the entire flash memory)

For a complete description of the flash memory, see the NVM chapter of the technical reference manual.

8.9 SRAM

MSPM0Gxx MCUs include a low power, high performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. MSPM0Gxx MCUs also provides up to 32KB of SRAM with hardware parity. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in run, sleep, stop, and standby operating modes and is lost in shutdown mode. A write protection mechanism is provided to allow the application to prevent unintended modifications to the SRAM memory. Write protection is useful when placing executable code into SRAM as it provides a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

8.10 GPIO

The general purpose input/output (GPIO) peripheral provides the user with a means to write data out and read data in to and from the device pins. Through the use of the Port A and Port B GPIO peripherals, these devices support up to 60 GPIO pins.

The key features of the GPIO module include:

- 0 wait state MMR access from CPU
- Set/Clear/Toggle multiple bits without the need of a read-modify-write construct in software
- GPIOs with "Standard with Wake" drive functionality able to wake the device from SHUTDOWN mode
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

For more details, see the GPIO chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.11 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO Pad configuration registers allow for programmable drive strength, speed, pullup-down, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.12 ADC

Both 12-bit analog-to-digital converter (ADC) modules in these devices, ADC0 and ADC1, support fast 12-bit conversions with single-ended inputs and simultaneous sampling operation.

ADC features include:

- 12-bit output resolution at 4Msps with greater than 11 ENOB
- Hardware averaging enables 14-bit effective resolution at 250 ksps
- Up to 17 total external input channels with individual result storage registers
- Internal channels for temperature sensing, supply monitoring, and analog signal chain
- Software selectable reference:
 - Configurable internal reference voltage of 1.4 V and 2.5 V (requires decoupling capacitor on VREF+ and VREF- pins)
 - MCU supply voltage (VDD)
 - External reference supplied to the ADC through the VREF+ and VREF- pins
- Operates in RUN, SLEEP, and STOP modes

Table 8-7. ADC Channel Mapping

| CHANNEL[0:7] | SIGNAL NAME ⁽²⁾ | | CHANNEL[8:15] | SIGNAL NAME ^{(1) (2)} | |
|--------------|----------------------------|------|---------------|--------------------------------|-------------------------------|
| | ADC0 | ADC1 | | ADC0 | ADC1 |
| 0 | A0_0 | A1_0 | 8 | A1_7 ⁽³⁾ | A0_7 ⁽³⁾ |
| 1 | A0_1 | A1_1 | 9 | - | - |
| 2 | A0_2 | A1_2 | 10 | - | - |
| 3 | A0_3 | A1_3 | 11 | <i>Temperature Sensor</i> | - |
| 4 | A0_4 | A1_4 | 12 | A0_12 | <i>Temperature Sensor</i> |
| 5 | A0_5 | A1_5 | 13 | | |
| 6 | A0_6 | A1_6 | 14 | <i>GPAMP output</i> | <i>GPAMP output</i> |
| 7 | A0_7 | A1_7 | 15 | <i>Supply/Battery Monitor</i> | <i>Supply/Battery Monitor</i> |

- (1) *Italicized* signal names are purely internal to the SoC. These signals are used for internal peripheral interconnections.
(2) For more information about device analog connections please refer to [Section 8.23](#).
(3) Note that channel 8 of each ADC can be sampled by the opposite ADC. Channel 8 of each ADC samples channel Ax_7 of the other ADC. Every ADC channel is available on a dedicated device pin.

For more details, see the ADC chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.13 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 1.4-V internal VREF at the factory trim temperature (T_{TRIM}). The ADC and VREF configuration for the above measurement is as the following: RES=0 (12-bit mode), VRSEL=2h (internal VREF), BUFCONFIG=1h (1.4V VREF), ADC t_{Sample}=12.5μs. This calibration value can be used with the temperature sensor temperature coefficient (T_{S_c}) to estimate the device temperature. See the temperature sensor section of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#) for guidance on estimating the device temperature with the factory trim value.

8.14 VREF

The shared voltage reference module (VREF) in these devices contain a configurable voltage reference buffer which allows users to supply a stable reference to on-board analog peripherals. It also supports bringing in an external reference for applications where higher accuracy is required.

VREF features include:

- 1.4V and 2.5V user-selectable internal references
- Internal reference supports full speed ADC operation
- Support for bringing in an external reference on VREF+/- device pins
- Requires a decoupling capacitor placed on VREF+/- pins for proper operation. See [VREF specification section](#) for more details

For more details, see the VREF chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.15 GPAMP

The general-purpose amplifier (GPAMP) peripheral is a chopper-stabilized general-purpose operational amplifier with rail-to-rail input and output.

The GPAMP supports the following features:

- Software selectable chopper stabilization

- Rail-to-rail input and output
- Programmable internal unity gain feedback loop

For more details, see the ADC chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.16 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for 32-bit CRC based on CRC32-ISO3309
- Support for bit reversal

For more details, see the CRC chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.17 UART

The UART peripherals (UART0, UART1, UART2, and UART3) provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
 - 5, 6, 7 or 8 data bits
 - Even, odd, stick, or no-parity bit generation and detection
 - 1 or 2 stop bit generation
 - Line-break detection
 - Glitch filter on the input signals
 - Programmable baud rate generation with oversampling by 16, 8 or 3
 - Local Interconnect Network (LIN) mode support
- Separated transmit and receive FIFOs support DAM data transfer
- Support transmit and receive loopback mode operation
- See [Table 8-8](#) for detail information on supported protocols

Table 8-8. UART Features

| UART Features | UART0 (Extend) | UART1 and 2 (Main) | UART3 (Main) |
|-------------------------------------|----------------|--------------------|--------------|
| Active in Stop and Standby Mode | Yes | Yes | - |
| Separate transmit and receive FIFOs | Yes | Yes | Yes |
| Support hardware flow control | Yes | Yes | Yes |
| Support 9-bit configuration | Yes | Yes | Yes |
| Support LIN mode | Yes | - | - |
| Support DALI | Yes | - | - |
| Support IrDA | Yes | - | - |
| Support ISO7816 Smart Card | Yes | - | - |
| Support Manchester coding | Yes | - | - |

For more details, see the UART chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.18 I2C

The inter-integrated circuit interface (I²C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100 kbit/s

- Support Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
 - Supported on open drain IOs (ODIO) and high-drive (HDIO) IOs only
- Separated transmit and receive FIFOs support DMA data transfer
- Support SMBus 3.0 with PEC, ARP, timeout detection and host support
- Wakeup from low power mode on address match
- Support analog and digital glitch filter for input signal glitch suppression
- 8-entry transmit and receive FIFOs

For more details, see the I2C chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.19 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support ULPClk/2 bit rate and up to 32Mbits/s in both controller and peripheral mode ¹
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode) and 7 bits to 16 bit (peripheral mode)
- Supports PACKEN feature that allows the packing of 2 16 bit FIFO entries into a 32-bit value to improve CPU performance
- Transmit and receive FIFOs (4 entries each with 16 bits per entry) supporting DMA data transfer
- Supports TI mode, Motorola mode and National Microwire format

For more details, see the SPI chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.20 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the [MSPM0 L-Series 32-MHz Microcontrollers Technical Reference Manual](#).

8.21 RTC

The real-time clock (RTC) operates off of a 32kHz input clock source (typically a low frequency crystal) and provides a time base to the application with multiple options for interrupts to the CPU. Key features of the RTC include:

- Counters for seconds, minutes, hours, day of the week, day of the month, month, and year
- Binary or BCD format
- Leap-year handling
- One customizable alarm interrupt based on minute, hour, day of the week, and day of the month
- Interval alarm interrupt to wake every minute, every hour, at midnight, or at noon
- Interval alarm interrupt providing periodic wake-up at 4096, 2048, 1024, 512, 256, or 128 Hz
- Interval alarm interrupt providing periodic wake-up at 64, 32, 16, 8, 4, 2, 1, and 0.5 Hz

¹ Only SPI signals on HSIO pins support data rate > 16 Mbits/s; see the *Pin Diagrams* section for HSIO pins.

- Calibration for crystal offset error (up to +/- 240ppm)
- Compensation for temperature drift (up to +/- 240ppm)
- RTC clock output to pin for calibration

For more details, see the RTC chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.22 Timers (TIMx)

The timer peripherals in these devices support the following key features, for specific configuration see [Table 8-9](#):

Specific features for the general-purpose timer (TIMGx) include:

- 16-bit up, down, up-down or down-up counter, with repeat-reload mode
- 32-bit up, down, up-down or down-up counter, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent channels for
 - Output compare
 - Input capture
 - PWM output
 - One-shot mode
- CC register available in TIMG7 and TIMG12
- Shadow register for load available in TIMG7
- Support quadrature encoder interface (QEI) for positioning and movement sensing available in TIMG8
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt/DMA trigger generation and cross peripherals (such as ADC) trigger capability
- Cross trigger event logic for Hall sensor inputs

Specific features for the advanced timer (TIMAx) include:

- 16-bit down or up-down counter, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter
- Up to four independent channels for
 - Output compare
 - Input capture
 - PWM output
 - One-shot mode
- Shadow register for load and CC register available in both TIMA0 and TIMA1
- Complementary output PWM
- Asymmetric PWM with programmable dead band insertion
- Fault handling mechanism to ensure the output signals in a safe user-defined state when a fault condition is encountered
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt and DMA trigger generation and cross peripherals (such as ADC) trigger capability
- Two additional capture/compare channels for internal events

Table 8-9. TIMx Configurations

| TIMER NAME | POWER DOMAIN | RESOLUTION | PRESCALE R | REPEAT COUNTER | CAPTURE / COMPARE CHANNELS | PHASE LOAD | SHADOW LOAD | SHADOW CC | DEADBAND | FAULT | QEI |
|------------|--------------|------------|------------|----------------|----------------------------|------------|-------------|-----------|----------|-------|-----|
| TIMG0 | PD0 | 16-bit | 8-bit | – | 2 | – | – | – | – | – | – |
| TIMG6 | PD1 | 16-bit | 8-bit | – | 2 | – | – | – | – | – | – |
| TIMG7 | PD1 | 16-bit | 8-bit | – | 2 | – | Yes | Yes | – | – | – |
| TIMG8 | PD0 | 16-bit | 8-bit | – | 2 | – | – | – | – | – | Yes |

Table 8-9. TIMx Configurations (continued)

| TIMER NAME | POWER DOMAIN | RESOLUTION | PRESCALE R | REPEAT COUNTER | CAPTURE / COMPARE CHANNELS | PHASE LOAD | SHADOW LOAD | SHADOW CC | DEADBAND | FAULT | QEI |
|------------|--------------|------------|------------|----------------|----------------------------|------------|-------------|-----------|----------|-------|-----|
| TIMG12 | PD1 | 32-bit | – | – | 2 | – | – | Yes | – | – | – |
| TIMA0 | PD1 | 16-bit | 8-bit | 8-bit | 4 | Yes | Yes | Yes | Yes | Yes | – |
| TIMA1 | PD1 | 16-bit | 8-bit | 8-bit | 2 | Yes | Yes | Yes | Yes | Yes | – |

Table 8-10. TIMx Cross Trigger Map (PD1)

| TSEL.ETSEL Selection | TIMA0 | TIMA1 | TIMG6 | TIMG7 | TIMG12 |
|----------------------|-------------------------|--------------|--------------|--------------|--------------|
| 0 | TIMA0.TRIG0 | TIMA0.TRIG0 | TIMA0.TRIG0 | TIMA0.TRIG0 | TIMA0.TRIG0 |
| 1 | TIMA1.TRIG0 | TIMA1.TRIG0 | TIMA1.TRIG0 | TIMA1.TRIG0 | TIMA1.TRIG0 |
| 2 | TIMG6.TRIG0 | TIMG6.TRIG0 | TIMG6.TRIG0 | TIMG6.TRIG0 | TIMG6.TRIG0 |
| 3 | TIMG7.TRIG0 | TIMG7.TRIG0 | TIMG7.TRIG0 | TIMG7.TRIG0 | TIMG7.TRIG0 |
| 4 | TIMG12.TRIG0 | TIMG12.TRIG0 | TIMG12.TRIG0 | TIMG12.TRIG0 | TIMG12.TRIG0 |
| 5 | TIMG8.TRIG0 | TIMG8.TRIG0 | TIMG8.TRIG0 | TIMG8.TRIG0 | TIMG8.TRIG0 |
| 6 to 15 | Reserved | | | | |
| 16 | Event Subscriber Port 0 | | | | |
| 17 | Event Subscriber Port 1 | | | | |
| 18-31 | Reserved | | | | |

Table 8-11. TIMx Cross Trigger Map (PD0)

| TSEL.ETSEL Selection | TIMG0 | TIMG8 |
|----------------------|-------------------------|-------------|
| 0 | TIMG0.TRIG0 | TIMG0.TRIG0 |
| 1 | TIMG8.TRIG0 | TIMG8.TRIG0 |
| 2 to 15 | Reserved | |
| 16 | Event Subscriber Port 0 | |
| 17 | Event Subscriber Port 1 | |
| 18-31 | Reserved | |

For more details, see the TIMx chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

8.23 Device Analog Connections

Figure 8-1 shows the internal analog connection of the device

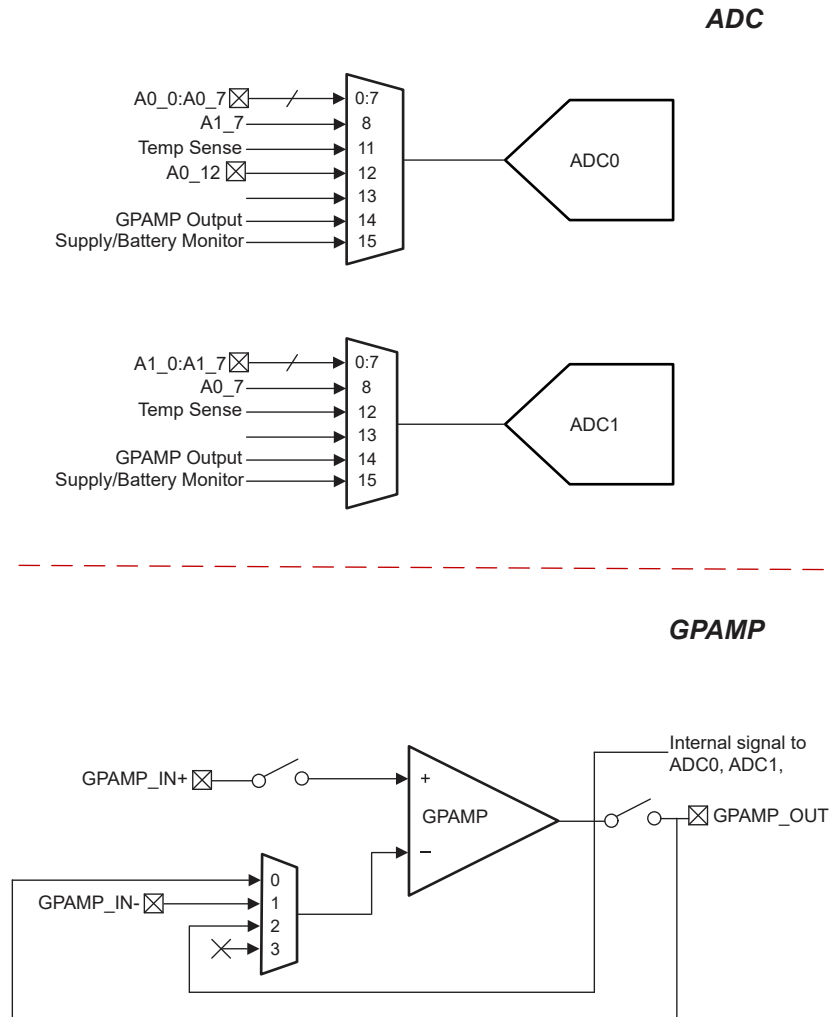


Figure 8-1. Analog Connections

8.24 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO. It also provides the controls for the output driver, input path, and the wake-up logic for wakeup from SHUTDOWN mode. For more information, refer to the IOMUX section of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in [Figure 8-2](#). Not all pins will have analog functions, wake-up logic, drive strength control, and pullup or pulldown resistors available. See the device-specific data sheet for detailed information on what features are supported for a specific pin.

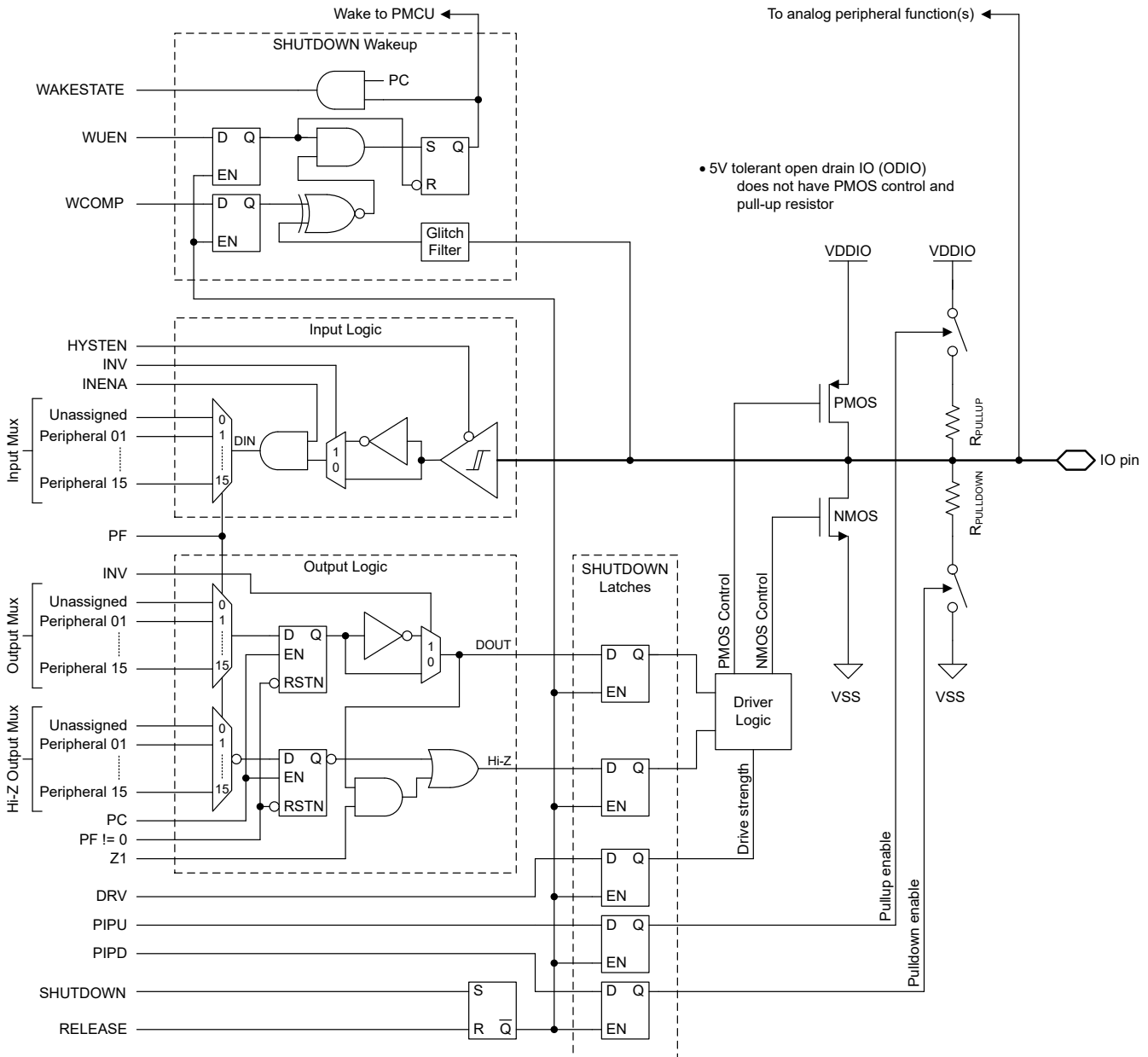


Figure 8-2. Superset Input/Output Diagram

8.25 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality offered on MSPM0 devices, see the debug chapter of the technical reference manual.

Table 8-12. Serial Wire Debug Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | SWD FUNCTION |
|---------------|--------------|--|
| SWCLK | Input | Serial wire clock from debug probe |
| SWDIO | Input/Output | Bi-directional (shared) serial wire data |

8.26 Bootstrap Loader (BSL)

The bootstrap loader (BSL) enables configuration of the device as well as programming of the device memory through a UART or I2C serial interface. Access to the device memory and configuration through the BSL is protected by a 256-bit user-defined password, and it is possible to completely disable the BSL in the device configuration, if desired. The BSL is enabled by default from TI to support use of the BSL for production programming.

A minimum of two pins are required to use the BSL: the BSLRX and BSLTX signals (for UART), or the BSLSCL and BLSLSDA signals (for I2C). Additionally, one or two additional pins (BSL_invoke and NRST) may be used for controlled invocation of the bootloader by an external host.

If enabled, the BSL may be invoked (started) in the following ways:

- The BSL is invoked during the boot process if the BSL_invoke pin state matches the defined BSL_invoke logic level. If the device fast boot mode is enabled, this invocation check is skipped. An external host can force the device into the BSL by asserting the invoke condition and applying a reset pulse to the NRST pin to trigger a BOOTRST, after which the device will verify the invoke condition during the reboot process and start the BSL if the invoke condition matches the expected logic level.
- The BSL is automatically invoked during the boot process if the reset vector and stack pointer are left unprogrammed. As a result, a blank device from TI will invoke the BSL during the boot process without any need to provide a hardware invoke condition on the BSL_invoke pin. This enables production programming using just the serial interface signals.
- The BSL may be invoked at runtime from application software by issuing a SYSRST with BSL entry command.

Table 8-13. BSL Pin Requirements and Functions

| DEVICE SIGNAL | CONNECTION | BSL FUNCTION |
|---------------|-------------------|---|
| BSLRX | Required for UART | UART receive signal (RXD), an input |
| BSLTX | Required for UART | UART transmit signal (TXD) an output |
| BSLSCL | Required for I2C | I2C BSL clock signal (SCL) |
| BLSLSDA | Required for I2C | I2C BSL data signal (SDA) |
| BSL_invoke | Optional | Active-high digital input used to start the BSL during boot |
| NRST | Optional | Active-low reset pin used to trigger a reset and subsequent check of the invoke signal (BSL_invoke) |

For a complete description of the BSL functionality and command set, see the [MSPM0 Bootloader User's Guide](#).

8.27 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to Factory Constants chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#).

Table 8-14. DEVICEID

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

| Device | DEVICEID.PARTNUM | DEVICEID.MANUFACTURER |
|------------|------------------|-----------------------|
| MSPM0G1105 | 0xBB88 | 0x17 |
| MSPM0G1106 | 0xBB88 | 0x17 |
| MSPM0G1107 | 0xBB88 | 0x17 |

Table 8-15. USERID

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

| Device | PART | VARIANT | Device | PART | VARIANT |
|-------------------|--------|---------|-----------------|--------|---------|
| MSPM0G1107TPMR | 0x807B | 0xB3 | MSPM0G1106TPMR | 0x477B | 0xD4 |
| MSPM0G1107TRGZR | 0x807B | 0x20 | MSPM0G1106TRGZR | 0x477B | 0xBB |
| MSPM0G1107TPTR | 0x807B | 0x32 | MSPM0G1106TPTR | 0x477B | 0x71 |
| MSPM0G1107TRHBR | 0x807B | 0xBC | MSPM0G1106TRHBR | 0x477B | 0x01 |
| MSPM0G1107TDGS28R | 0x807B | 0x82 | MSPM0G1105TRGZR | 0x8934 | 0xFE |
| MSPM0G1107TRGER | 0x807B | 0x79 | MSPM0G1105TPTR | 0x8934 | 0xD |

8.28 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region, refer to Device Factory Constants section, which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. Refer to Factory Constants chapter of the [MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#) for more information.

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata sheet describes these markings (see [Section 10.4](#))

9 Applications, Implementation, and Layout

9.1 Typical Application

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1.1 Schematic

TI recommends connecting a combination of a 10- μF and a 0.1- μF low-ESR ceramic decoupling capacitor across the VDD and VSS pins, as well as placing these capacitors as close as possible to the supply pins that they decouple (within a few millimeters) to achieve a minimal loop area. The 10- μF bulk decoupling capacitor is a recommended value for most applications, but this capacitance can be adjusted if needed based upon the PCB design and application requirements. For example, larger bulk capacitors can be used, but this can affect the supply rail ramp-up time.

The NRST reset pin must be pulled up to VDD (supply level) for the device to release from RESET state and start the boot process. TI recommends connecting an external 47-k Ω pullup resistor with a 10-nF pulldown capacitor for most applications, enabling the NRST pin to be controlled by another device or a debug probe.

The SYSOSC frequency correction loop (FCL) circuit utilizes an external 100-k Ω with 0.1% tolerance resistor between the ROSC pin and VSS. This resistor establishes a reference current to stabilize the SYSOSC frequency through a correction loop. This resistor is required if the FCL feature is used for higher accuracy, and it is not required if the SYSOSC FCL is not enabled. When the FCL mode is not used, the PA2 pin can be used as a digital input/output pin.

A 0.47- μF tank capacitor is required for the VCORE pin and must be placed close to the device with minimum distance to the device ground. Do not connect other circuits to the VCORE pin.

For the 5-V-tolerant open drain (ODIO), a pullup resistor is required to output high for I2C and UART functions, as the open drain IO only implement a low-side NMOS driver and no high-side PMOS driver. The 5-V-tolerant open drain IOs are fail-safe and can have a voltage present even if VDD is not supplied.

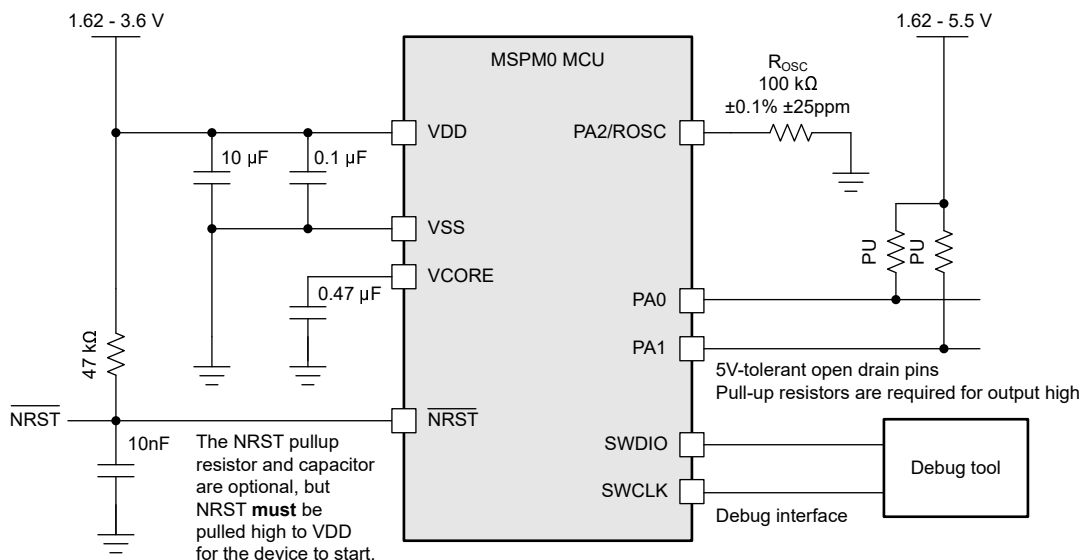


Figure 9-1. Basic Application Schematic

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Getting Started and Next Steps

For more information on the MSP low-power microcontrollers and the tools and libraries that are available to help with development, visit the Texas Instruments [Arm Cortex-M0+ MCUs](#) page.

10.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [Figure 10-1](#) provides a legend for reading the complete device name.

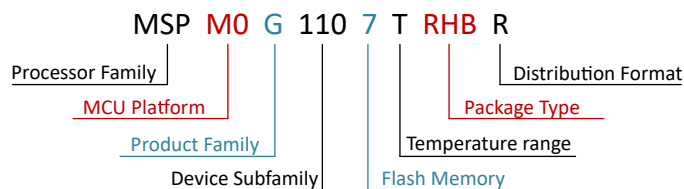


Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

| | |
|----------------------------|--|
| Processor Family | MSP = Mixed-signal processor X= Experimental silicon |
| MCU Platform | M0 = Arm based 32-bit M0+ |
| Product Family | G = 80-MHz frequency |
| Device Subfamily | 110 = 2x ADC |
| Flash Memory | 5 = 32KB 6 = 64KB 7 = 128KB |
| Temperature Range | T = -40°C to 105°C |
| Package Type | See the <i>Device Comparison</i> section and https://www.ti.com/packaging |
| Distribution Format | R = Large reel |

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, [ti.com](https://www.ti.com), or contact your TI sales representative.

10.3 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP)
Boards: LP-MSPM0G3507 Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming/debugging/EnergyTrace.

The LP ecosystem includes dozens of **BoosterPack** stackable plug-in modules to extend functionality.

Embedded Software

MSPM0 Software Development Kit (SDK) Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

TI Developer Zone Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.

TI Resource Explorer Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.

SysConfig Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE ,in TI Cloud Tools or a standalone version. ([offline version](#))

MSP Academy Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.

GUI Composer GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE & compiler toolchains

Code Composer Studio™ (CCS) Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. It comprises a suite of tools used to develop and debug embedded applications. CCS is completely free to use and is available on Eclipse and Theia frameworks.

IAR Embedded Workbench® IDE IAR Embedded Workbench for Arm delivers a complete development toolchain for building and debugging embedded applications for MSPM0. The included IAR C/C++ Compiler generates highly optimized code for your application, and the C-SPY Debugger is a fully integrated debugger for source and disassembly level debugging with support for complex code and data breakpoint.

Keil® MDK IDE Arm Keil MDK is a complete debugger and C/C++ compiler toolchain for building and debugging embedded applications for MSPM0. Keil MDK includes a fully integrated debugger for source and disassembly level debugging. MDK provides full CMSIS compliance.

TI Arm-Clang TI Arm Clang is included in the Code Composer Studio IDE.

GNU Arm Embedded Toolchain The MSPM0 SDK supports development using the open-source Arm GNU Toolchain. Arm GCC is supported by Code Composer Studio IDE (CCS).

10.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the MSPM0 MCUs. Copies of these documents are available on the Internet at www.ti.com.

Technical Reference Manual

[MSPM0 G-Series 80-MHz Microcontrollers Technical Reference Manual](#)

This manual describes the modules and peripherals of the MSPM0G family of devices. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals are present on all devices. In addition, modules or peripherals can differ in their exact implementation on different devices. Pin functions, internal signal connections, and operational parameters differ from device to device. See the device-specific data sheet for these details.

10.5 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.6 Trademarks

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10.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|--------------|----------|--|
| October 2023 | C | Changes throughout for final characterization and production release |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSPM0G1105TPTR | ACTIVE | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M0G1105T | Samples |
| MSPM0G1105TRGZR | ACTIVE | VQFN | RGZ | 48 | 4000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | MSPM0 G1105T | Samples |
| MSPM0G1106TPMR | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M0G1106T | Samples |
| MSPM0G1106TPTR | ACTIVE | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M0G1106T | Samples |
| MSPM0G1106TRGZR | ACTIVE | VQFN | RGZ | 48 | 4000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | MSPM0 G1106T | Samples |
| MSPM0G1106TRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | MSPM0 G1106T | Samples |
| MSPM0G1107TPMR | ACTIVE | LQFP | PM | 64 | 1000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M0G1107T | Samples |
| MSPM0G1107TPTR | ACTIVE | LQFP | PT | 48 | 1000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | M0G1107T | Samples |
| MSPM0G1107TRGER | ACTIVE | VQFN | RGE | 24 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | MSPM0 G1107T | Samples |
| MSPM0G1107TRGZR | ACTIVE | VQFN | RGZ | 48 | 4000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | MSPM0 G1107T | Samples |
| MSPM0G1107TRHBR | ACTIVE | VQFN | RHB | 32 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | MSPM0 G1107T | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSPM0G1105TPTR | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |
| MSPM0G1105TRGZR | VQFN | RGZ | 48 | 4000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSPM0G1106TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSPM0G1106TPTR | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |
| MSPM0G1106TRGZR | VQFN | RGZ | 48 | 4000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSPM0G1106TRHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |
| MSPM0G1107TPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSPM0G1107TPTR | LQFP | PT | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.9 | 12.0 | 16.0 | Q2 |
| MSPM0G1107TRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| MSPM0G1107TRGZR | VQFN | RGZ | 48 | 4000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| MSPM0G1107TRHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSPM0G1105TPTR | LQFP | PT | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| MSPM0G1105TRGZR | VQFN | RGZ | 48 | 4000 | 367.0 | 367.0 | 35.0 |
| MSPM0G1106TPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSPM0G1106TPTR | LQFP | PT | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| MSPM0G1106TRGZR | VQFN | RGZ | 48 | 4000 | 367.0 | 367.0 | 35.0 |
| MSPM0G1106TRHBR | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0G1107TPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSPM0G1107TPTR | LQFP | PT | 48 | 1000 | 336.6 | 336.6 | 31.8 |
| MSPM0G1107TRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| MSPM0G1107TRGZR | VQFN | RGZ | 48 | 4000 | 367.0 | 367.0 | 35.0 |
| MSPM0G1107TRHBR | VQFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |

RGE 24

GENERIC PACKAGE VIEW

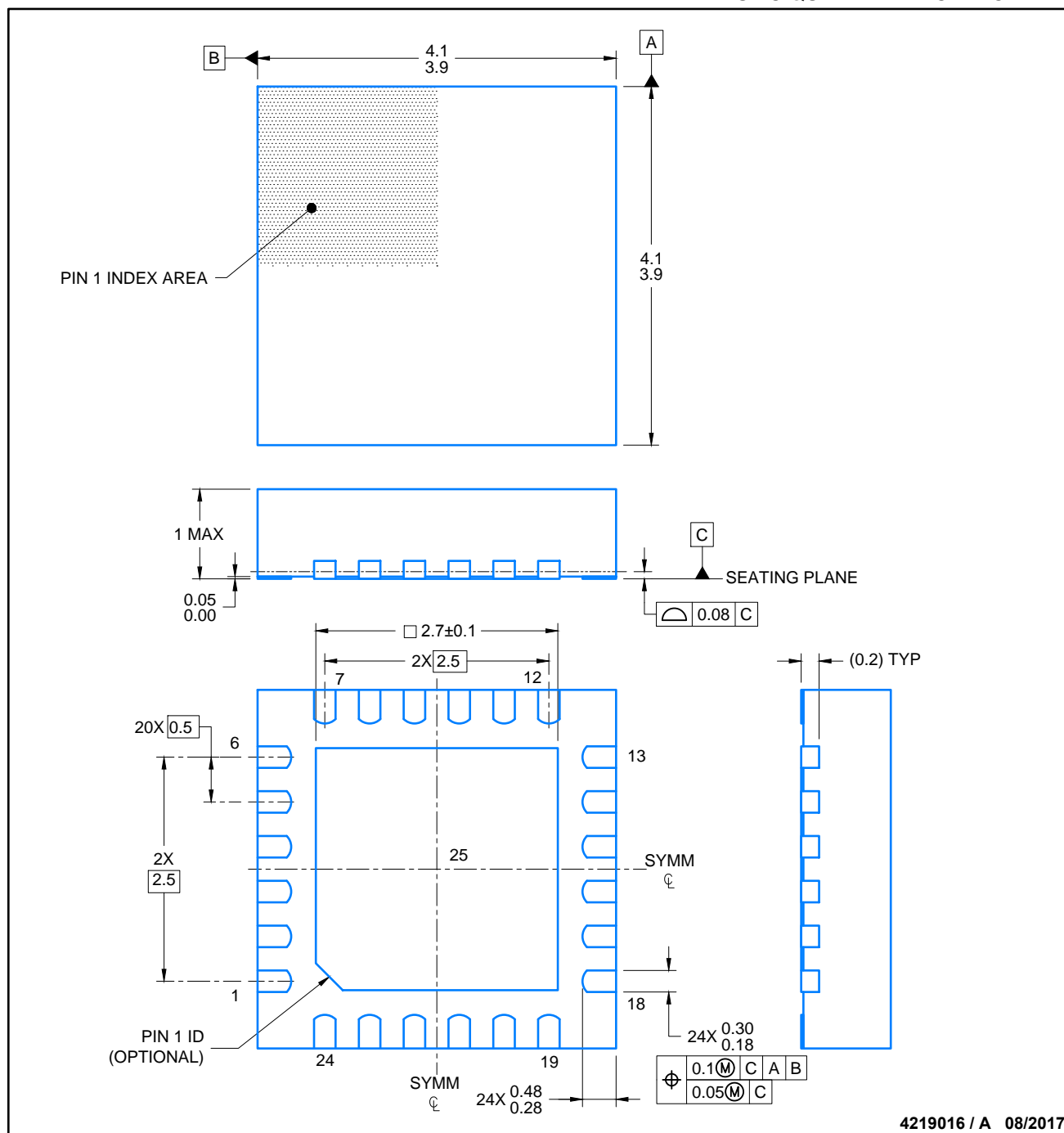
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



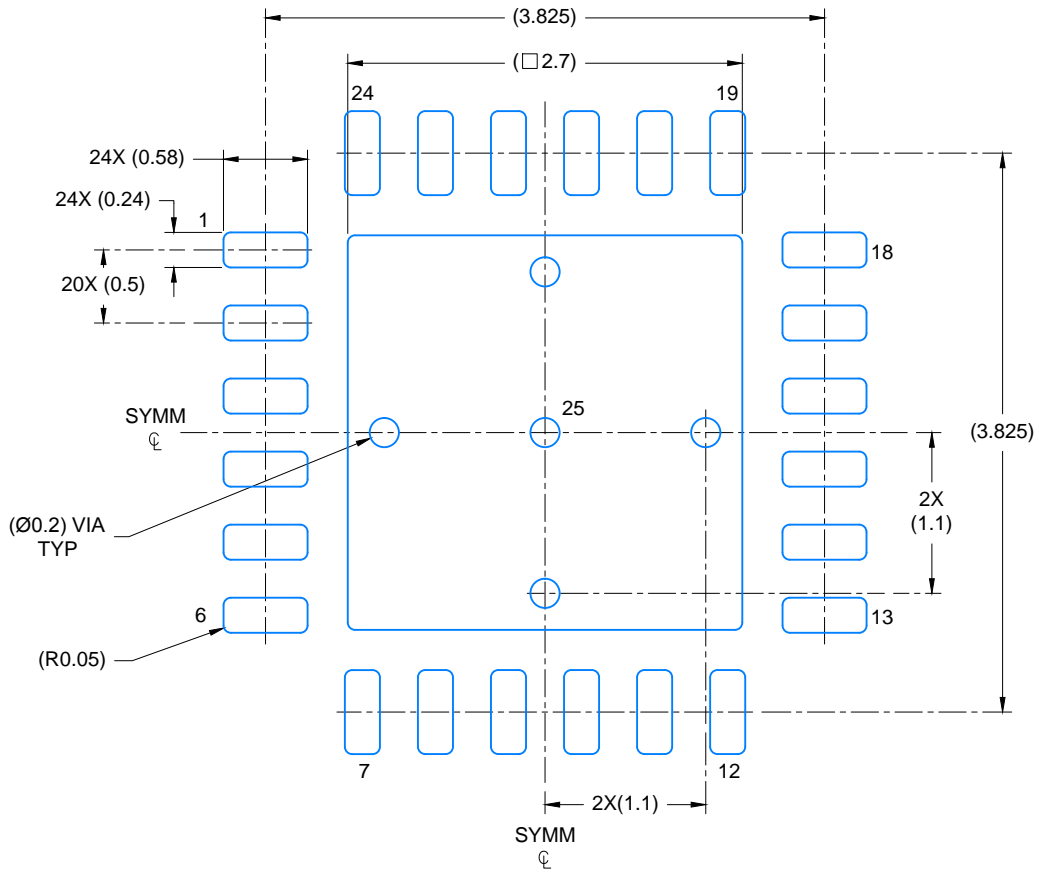
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

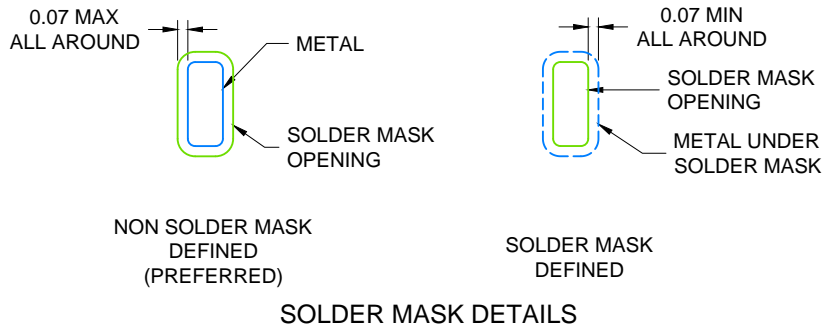


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



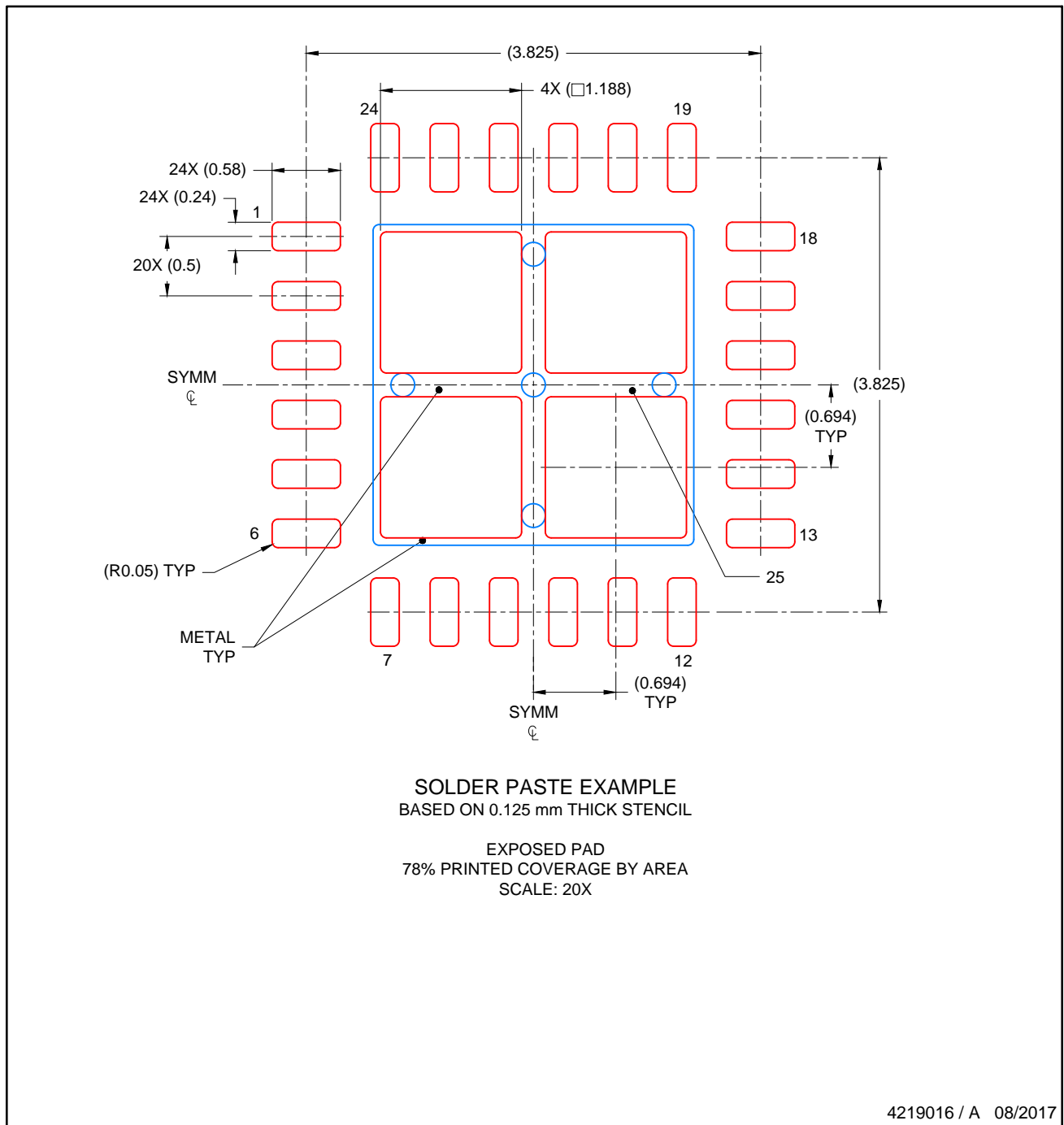
LAND PATTERN EXAMPLE
SCALE: 20X



4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

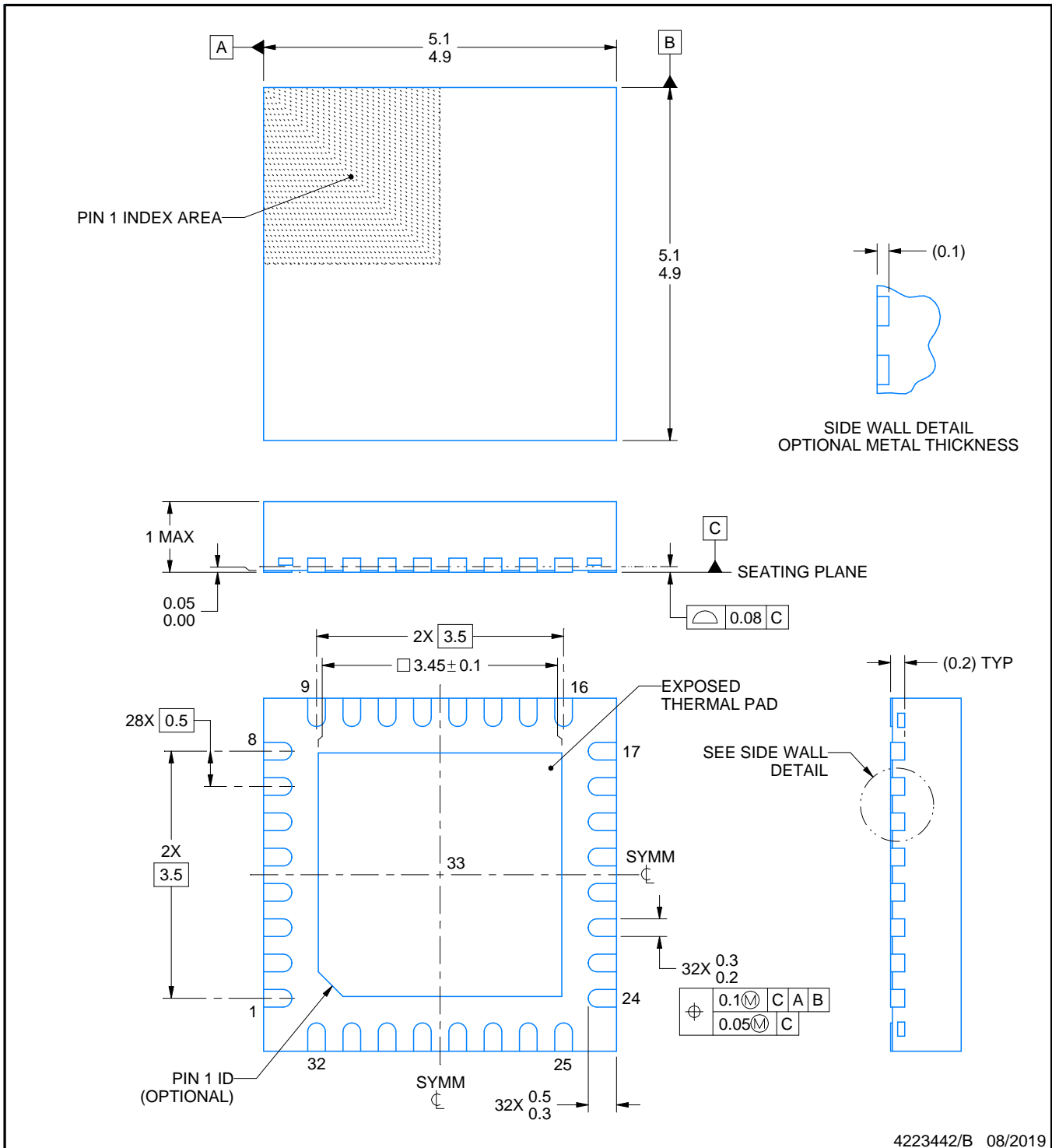
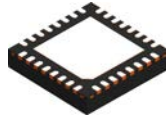
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A



4223442/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
 75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PM0064A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

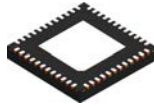
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

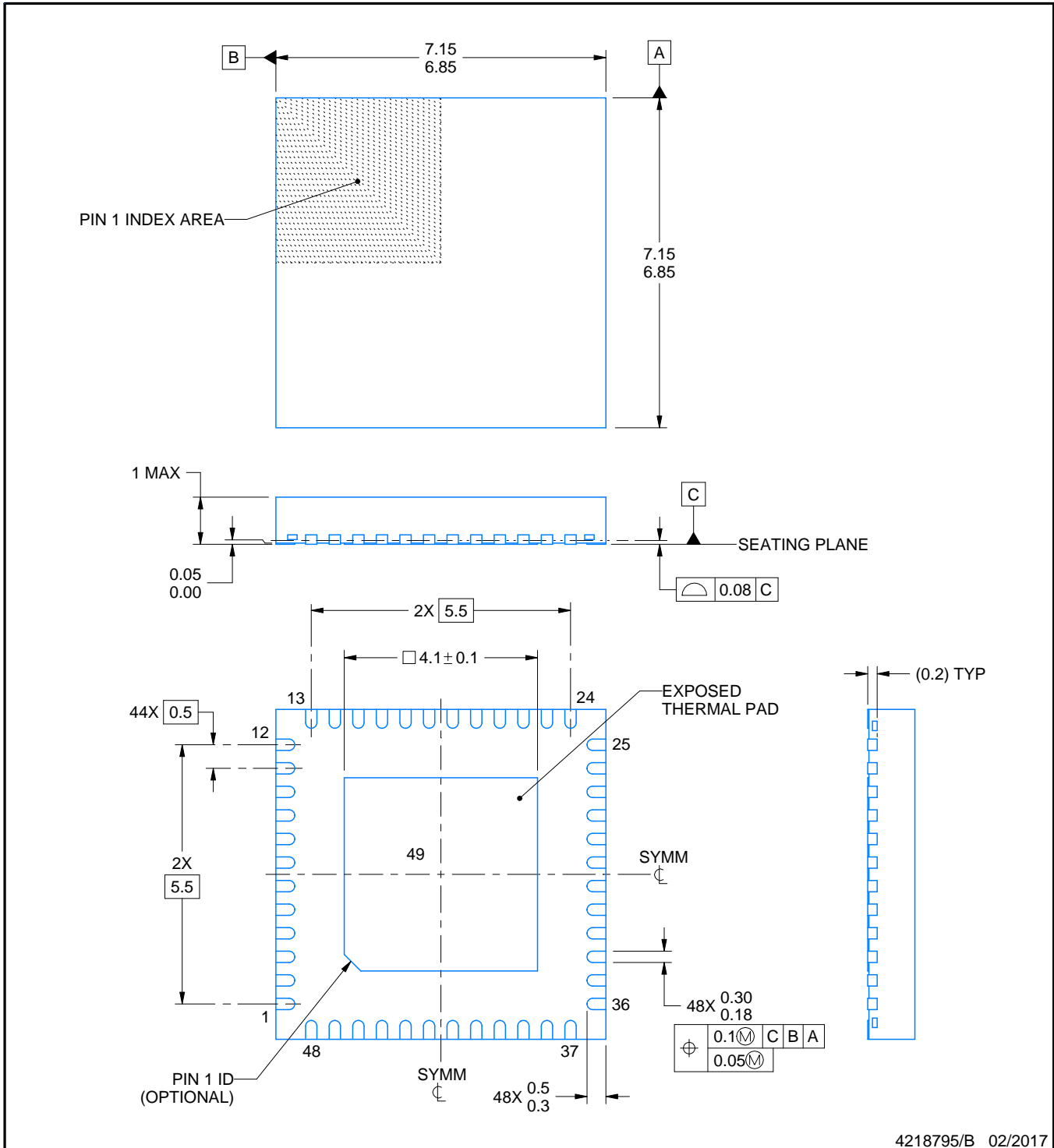
RGZ0048B



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4218795/B 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

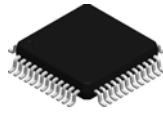
EXPOSED PAD 49
 73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

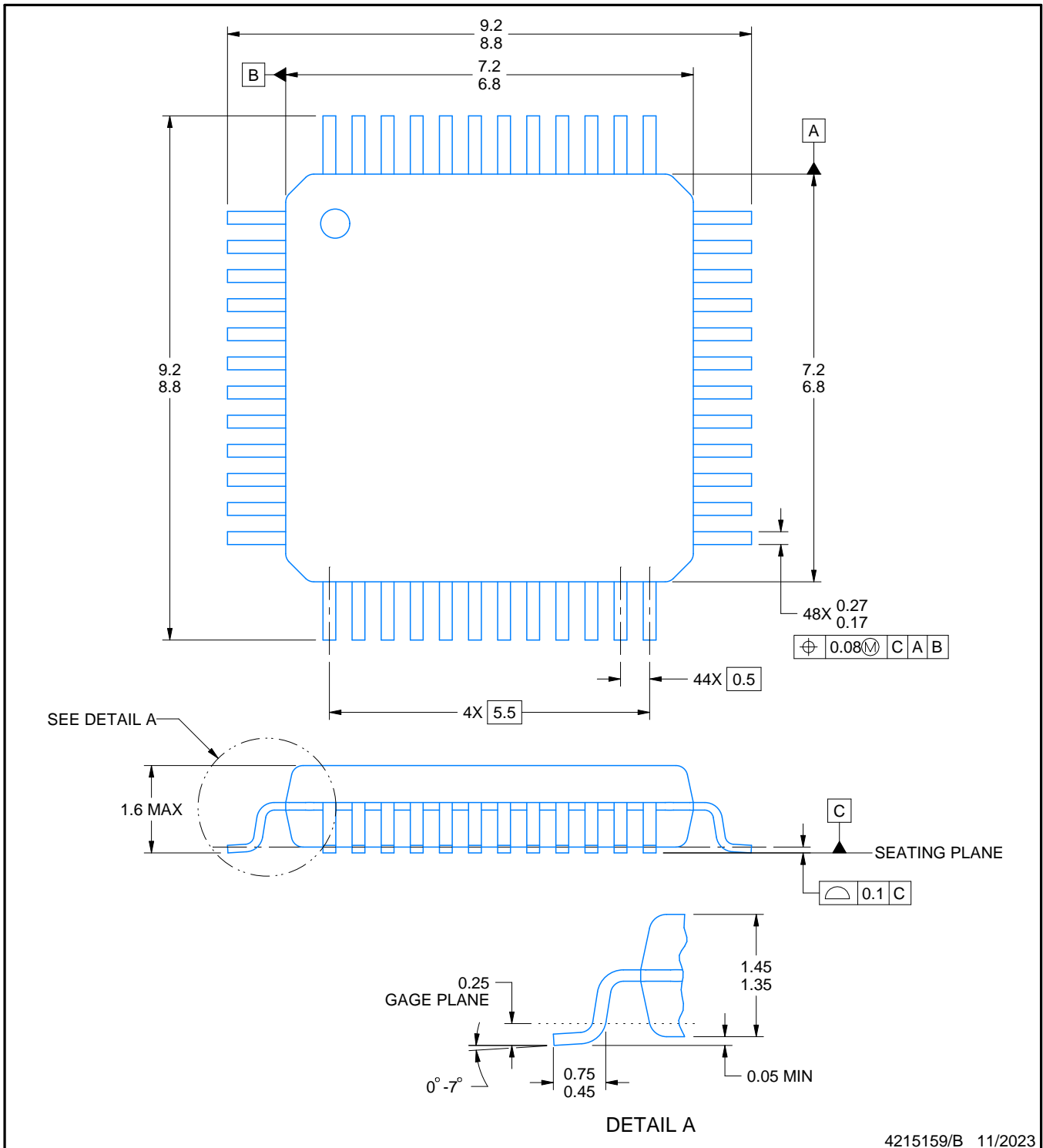
PT0048A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



4215159/B 11/2023

NOTES:

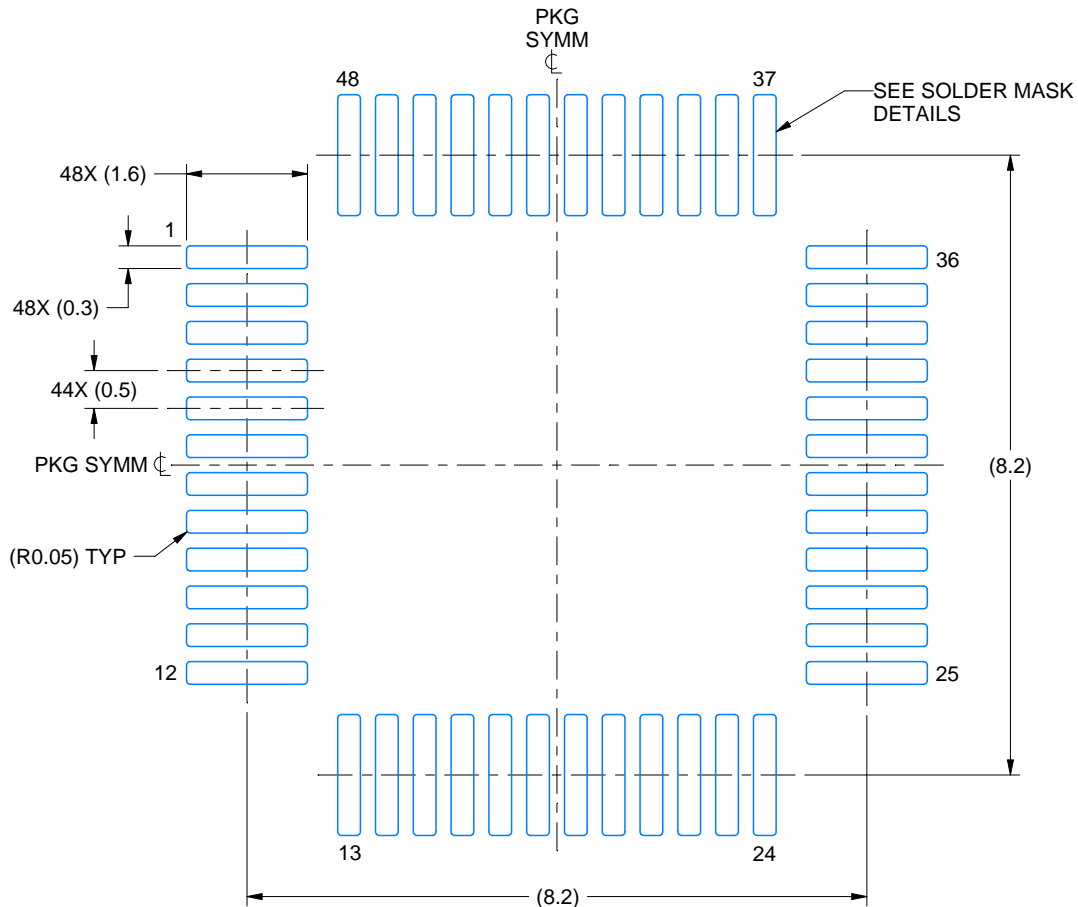
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads connected to the die pads.

EXAMPLE BOARD LAYOUT

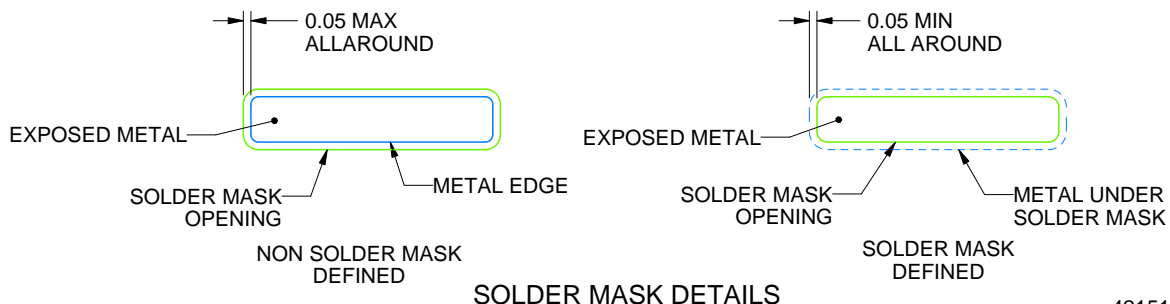
PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

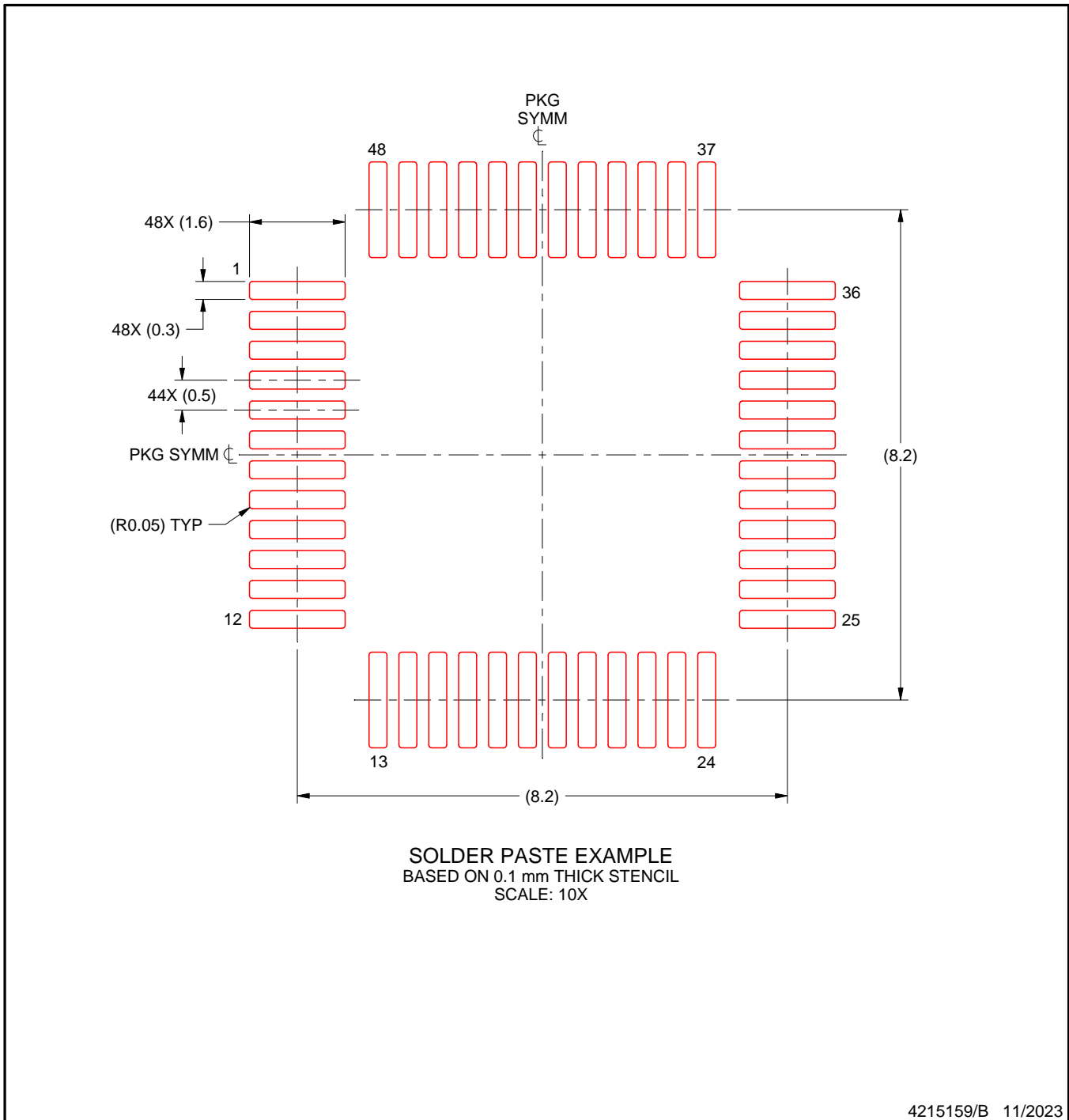
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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