SN74LVC1G16 Inverting Buffer with Schmitt-Trigger Input and Open-Drain Output

1 Features

- Operating range from 1.1V to 5.5V
- 5.5V tolerant input pins
- Supports standard pinouts
- Latch-up performance exceeds 100mA per JESD 17

2 Applications

- Combining power good signals
- Enable digital signals

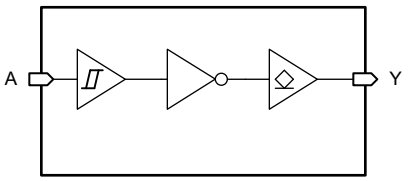
3 Description

This device is an Inverter Buffer with a Schmitt-Trigger input and an Open-Drain output.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LVC1G16	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DCK (SOT-SC70, 5)	2mm × 1.25mm	2mm × 1.25mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram

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4 Pin Configuration and Functions

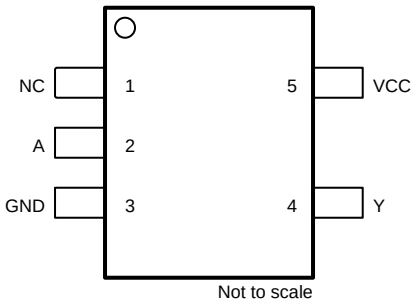

Figure 4-1. SN74LVC1G16 DBV Package, 5-Pin SOT-23 (Top View)

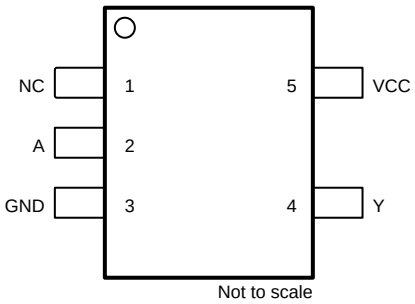

Figure 4-2. SN74LVC1G16-Q1 DCK Package, 5-Pin SOT-SC70 (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
NC	1	—	No Connect, Leave floating or connect to ground
A	2	Input	Input A
GND	3	—	Ground
Y	4	Output	Output Y
V_{CC}	5	—	Positive Supply

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range(2)		-0.5	6.5	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
V_O	Output voltage range (2)		-0.5	6.5	V
I_{IK}	Input clamp current	V_I < 0 V		-50	mA
I_{OK}	Output clamp current	V_O < 0 V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.1	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	(High or low state)	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		-4	mA
		V_{CC} = 2.3 V		-8	
		V_{CC} = 3.0 V		-16	
				-24	
		V_{CC} = 4.5 V		-32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3.0 V		16	
				24	
		V_{CC} = 4.5 V		32	
Δt/Δv	Input transition rise or fall rate	V_{cc} = 1.2 V to 5.0V		20	ns/V
Δt/Δv	Input transition rise or fall rate	V_{cc} = 1.8 V ± 0.15 V		20	ns/V
Δt/Δv	Input transition rise or fall rate	V_{cc} = 2.5 V ± 0.2V		20	ns/V
Δt/Δv	Input transition rise or fall rate (1G04, 1G06, 1G07, 1G34)	V_{cc} = 3.3 V ± 0.3 V		10	ns/V

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
Δt/Δv	Input transition rise or fall rate (1G34)	V_{cc} = 5.0 V ± 0.5 V		10	ns/V
Δt/Δv	Input transition rise or fall rate (1G04, 1G06, 1G07)	V_{cc} = 5.0 V ± 0.5 V		5	ns/V
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DBV (SOT-23, 5)	5	141.8	74	87.1	22.3	86.6	-	°C/W
DCK (SOT-SC70, 5)	5	98.8	94.3	67.6	15.4	67.6	46.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{T+}	Positive-going input threshold voltage	1.1 V	0.5	0.77	0.9	V
V_{T+}	Positive-going input threshold voltage	1.3 V	0.6	0.89	1.0	V
V_{T+}	Positive-going input threshold voltage	1.5 V	0.7	1.0	1.11	V
V_{T+}	Positive-going input threshold voltage	1.65 V	0.76	1.08	1.16	V
V_{T+}	Positive-going input threshold voltage	2.3 V	1.08	1.35	1.56	V
V_{T+}	Positive-going input threshold voltage	3 V	1.3	1.66	1.92	V
V_{T+}	Positive-going input threshold voltage	4.5 V	2.16	2.37	2.74	V
V_{T+}	Positive-going input threshold voltage	5.5 V	2.61	2.86	3.33	V
V_{T-}	Negative-going input threshold voltage	1.1 V	0.2	0.37	0.6	V
V_{T-}	Negative-going input threshold voltage	1.3 V	0.26	0.45	0.65	V
V_{T-}	Negative-going input threshold voltage	1.5 V	0.34	0.52	0.65	V
V_{T-}	Negative-going input threshold voltage	1.65 V	0.35	0.57	0.7	V
V_{T-}	Negative-going input threshold voltage	2.3 V	0.56	0.79	0.89	V
V_{T-}	Negative-going input threshold voltage	3 V	0.84	1.04	1.2	V
V_{T-}	Negative-going input threshold voltage	4.5 V	1.41	1.59	1.97	V
V_{T-}	Negative-going input threshold voltage	5.5 V	1.71	1.94	2.4	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	1.1 V	0.25	0.49	0.53	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	1.3 V	0.25	0.50	0.54	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	1.5 V	0.25	0.51	0.60	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	1.65 V	0.3	0.52	0.8	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	2.3 V	0.4	0.56	0.78	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	3 V	0.4	0.62	0.87	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	4.5 V	0.58	0.78	1.04	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	5.5 V	0.69	0.91	1.14	V
V_{OL}	I_{OL}= 100 µA	Over Recommended Operating Conditions			0.2	V
V_{OL}	I_{OL}= 4 mA	1.65 V			0.45	V
V_{OL}	I_{OL}= 8 mA	2.3 V			0.3	V
V_{OL}	I_{OL}= 12 mA	2.7 V			0.4	V

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over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OL}	I_{OL}= 16 mA	3 V			0.4	V
V_{OL}	I_{OL}= 24 mA	3 V			0.55	V
V_{OL}	I_{OL}= 32 mA	4.5 V			0.55	V
I_I	V_I = V_{CC} or GND	V_{CC} = 0V to 5.5 V		±1	±5	µA
I_{off}	V_I or V_O = V_{CC}	V_{CC} = 0 V		±1	±10	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	V_{CC} = 1.1 V to 5.5 V		1	10	µA
ΔI_{CC}	One input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND	3.0 V to 5.5 V			500	µA
C_I	V_I = V_{CC} or GND	3.3 V		3.5		pF
C_O	V_O = V_{CC} or GND	3.3 V		6.3		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See #i#Parameter Measurement Information

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	A	Y	C_L = 15 pF	1.2 V ± 0.1 V		14	20	ns
t_{pd}	A	Y	C_L = 15 pF	1.5 V ± 0.12 V		11	15	ns
t_{pd}	A	Y	C_L = 15 pF	1.8 V ± 0.15 V	2.7		9.9	ns
t_{pd}	A	Y	C_L = 15 pF	2.5 V ± 0.2 V	1.6		5.5	ns
t_{pd}	A	Y	C_L = 15 pF	3.3 V ± 0.3 V	1.5		4.6	ns
t_{pd}	A	Y	C_L = 15 pF	5.0 V ± 0.5 V	0.9		4.4	ns
t_{pd}	A	Y	C_L = 30 pF	1.8 V ± 0.15 V	3.0		13	ns
t_{pd}	A	Y	C_L = 30 pF	2.5 V ± 0.2 V	2		8	ns
t_{pd}	A	Y	C_L = 50 pF	3.3 V ± 0.3 V	1.8		6.5	ns
t_{pd}	A	Y	C_L = 50 pF	5.0 V ± 0.5 V	1.2		6	ns
C_{pd}			No Load, f = 10 MHz	1.8 V		3		pF
C_{pd}			No Load, f = 10 MHz	2.5 V		3		pF
C_{pd}			No Load, f = 10 MHz	3.3 V		3		pF
C_{pd}			No Load, f = 10 MHz	5.0 V		4		pF

5.7 Noise Characteristics

VCC = 3.3 V, CL = 50 pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8	-0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	2.2	3.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.0			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

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5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

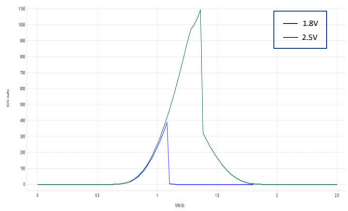

Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

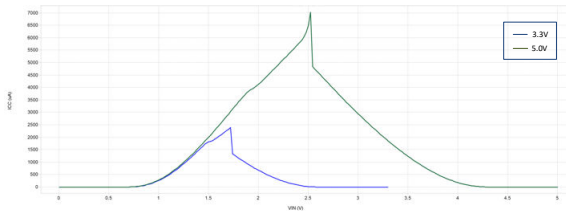

Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

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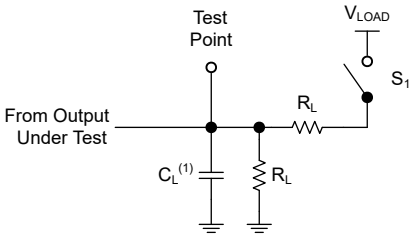
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

The outputs are measured individually with one input transition per measurement.

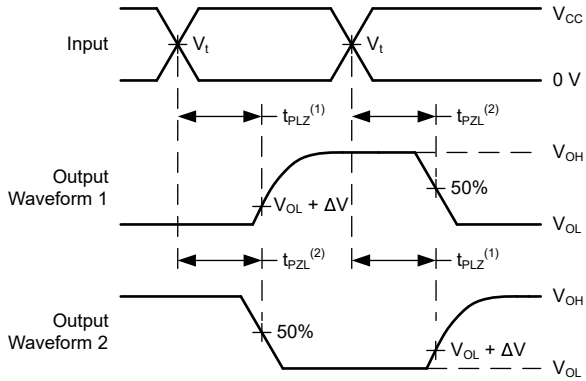
TEST	S1	R_L	C_L	ΔV	V_{LOAD}
t_{PLZ}, t_{PZL}	CLOSED	500Ω	50pF	0.3V	2×V_{CC}

V_{CC}	V_t	R_L	C_L	ΔV	V_{LOAD}
1.2V ± 0.1V	V_{CC}/2	2kΩ	15pF	0.1V	2×V_{CC}
1.5V ± 0.12V	V_{CC}/2	2kΩ	15pF	0.1V	2×V_{CC}
1.8V ± 0.15V	V_{CC}/2	1kΩ	15pF/30pF	0.15V	2×V_{CC}
2.5V ± 0.2V	V_{CC}/2	500Ω	15pF/30pF	0.15V	2×V_{CC}
3.3V ± 0.3V	1.5V	500Ω	15pF/50pF	0.3V	6V
5.0V ± 0.5V	1.5V	500Ω	15pF/50pF	0.3V	6V



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Open-Drain Outputs



(1) t_{PLZ} is the same as t_{dis}.

(2) t_{PZL} is the same as t_{en}.

Figure 6-2. Voltage Waveforms Propagation Delays

7 Detailed Description

7.1 Feature Description

7.1.1 Open-Drain CMOS Outputs

This device includes open-drain CMOS outputs. Open-drain outputs can only drive the output low. When in the high logical state, open-drain outputs will be in a high-impedance state. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused open-drain CMOS outputs should be left disconnected.

7.1.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

7.1.3 Clamp Diode Structure

Figure 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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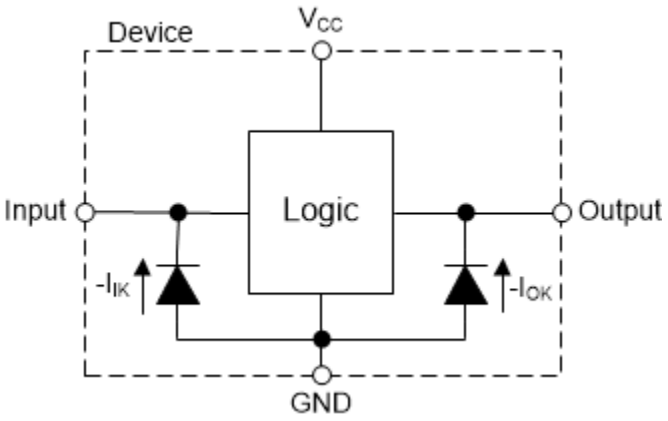

Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, an open-drain inverter is used to drive an LED as shown in Figure 8-1.

8.2 Typical Application

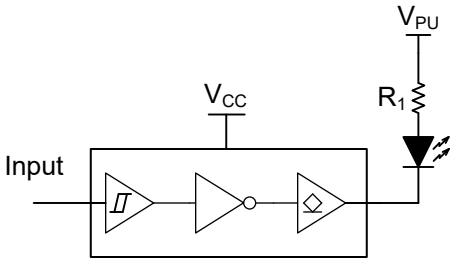

Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC1G16 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC1G16 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LVC1G16 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC1G16 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC1G16 has no input signal transition rate requirements because it has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

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8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC1G16 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.3 Application Curves

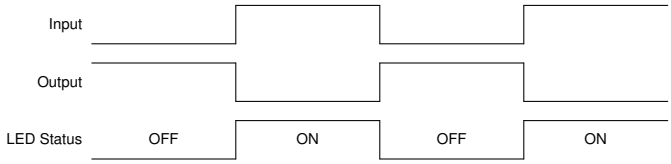

Figure 8-2. Application Curve

8.4 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.5 Layout

8.5.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.5.2 Layout Example

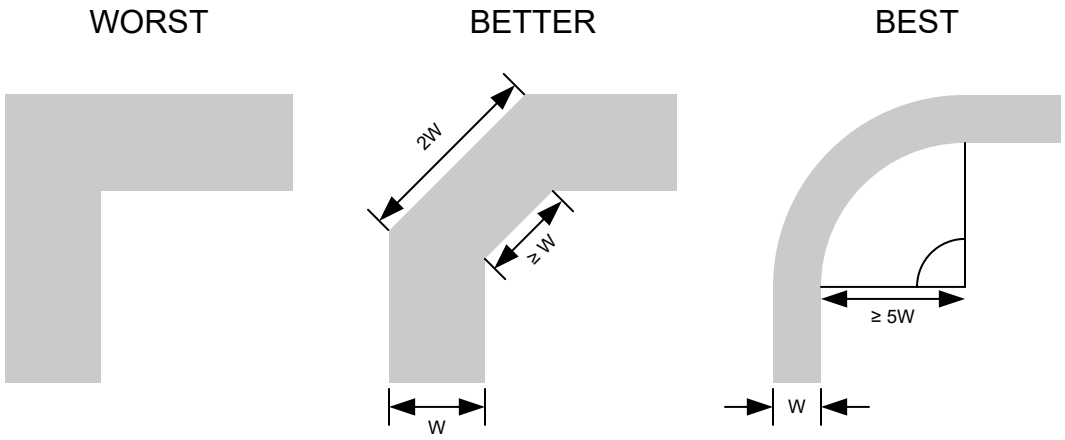

Figure 8-3. Example Trace Corners for Improved Signal Integrity

ADVANCE INFORMATION

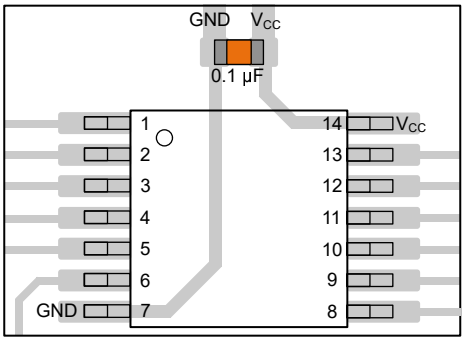

Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

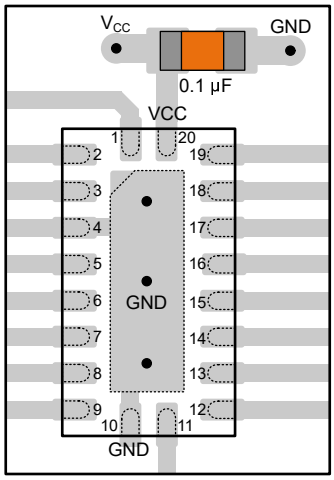

Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

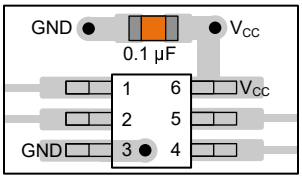

Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

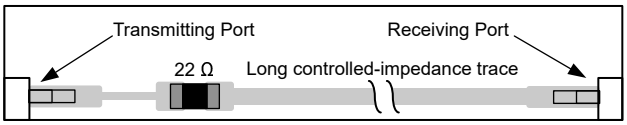

Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

ADVANCE INFORMATION

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
October 2024	*	Advance Information release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PSN74LVC1G16DBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PSN74LVC1G16DCKR	ACTIVE	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVC1G16 :

- Automotive : SN74LVC1G16-Q1

NOTE: Qualified Version Definitions:

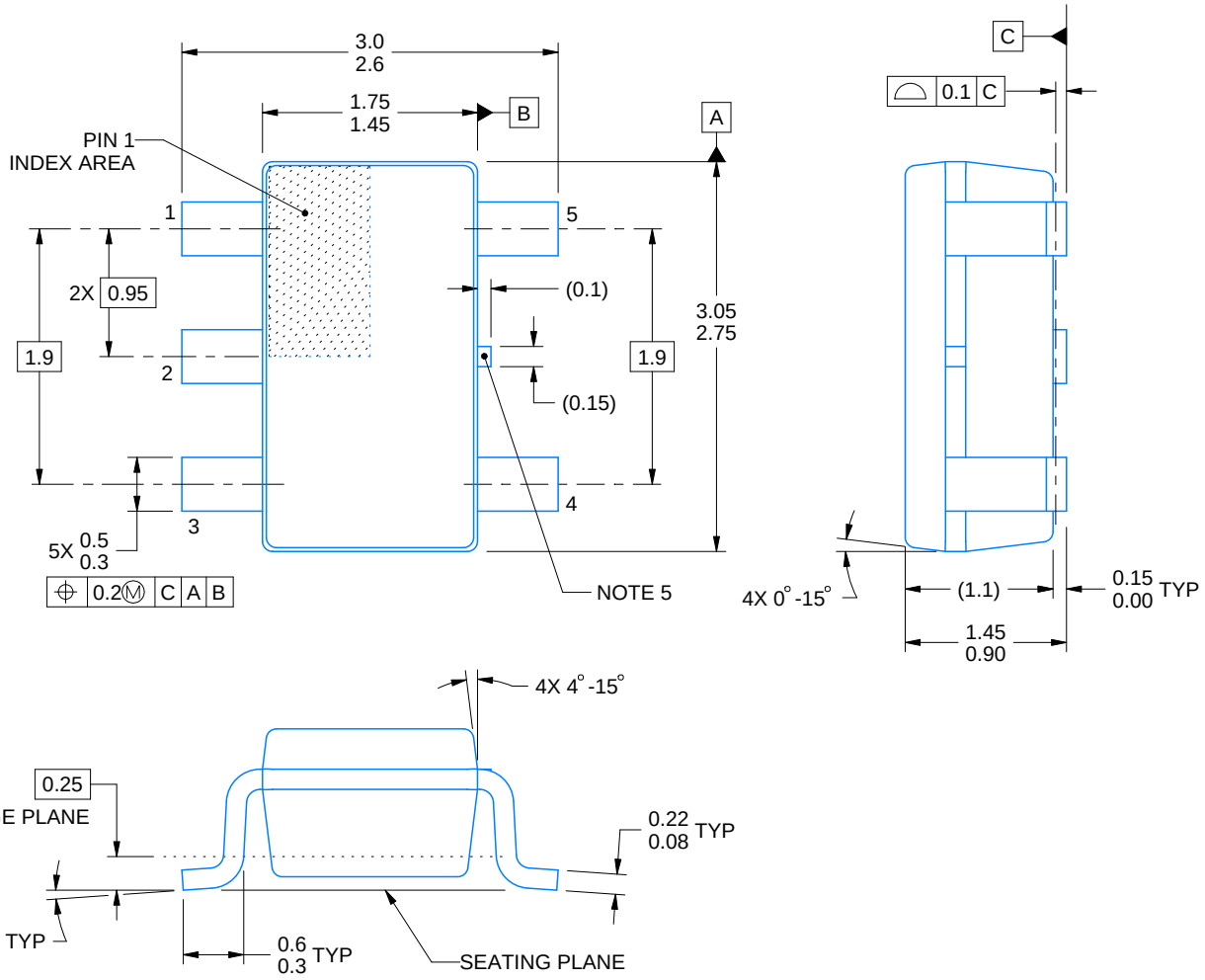
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

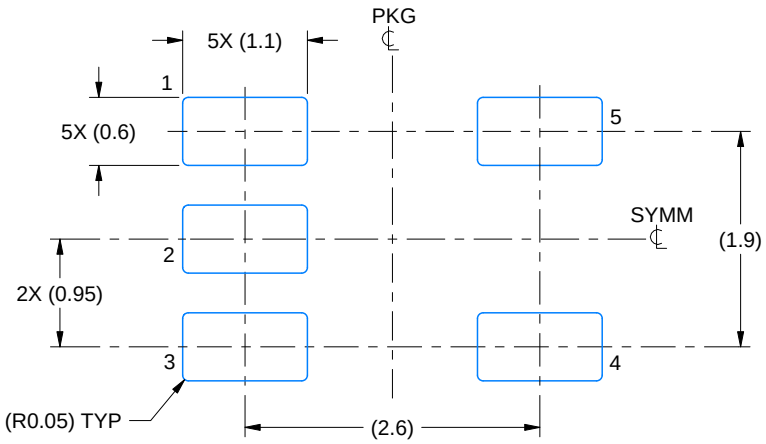
SMALL OUTLINE TRANSISTOR



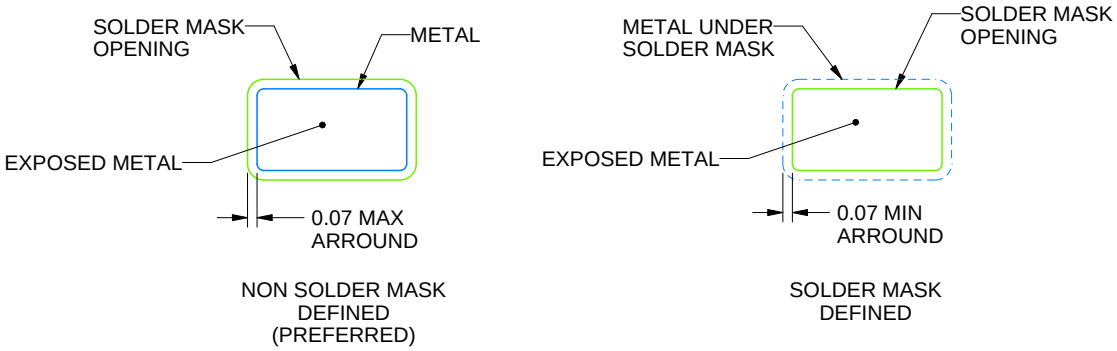
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

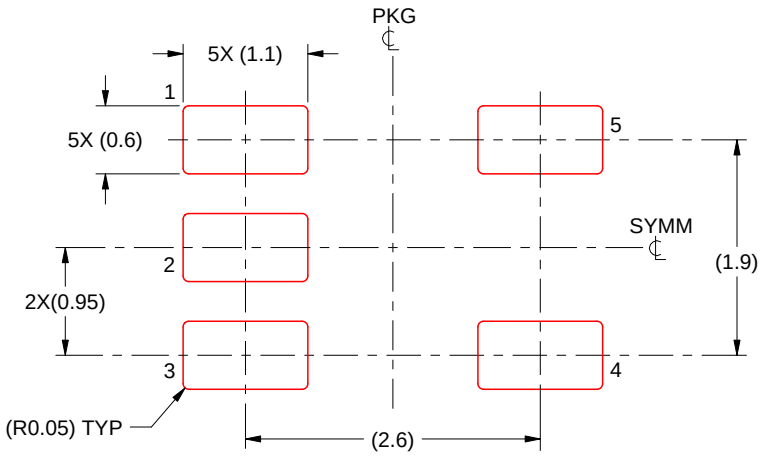


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

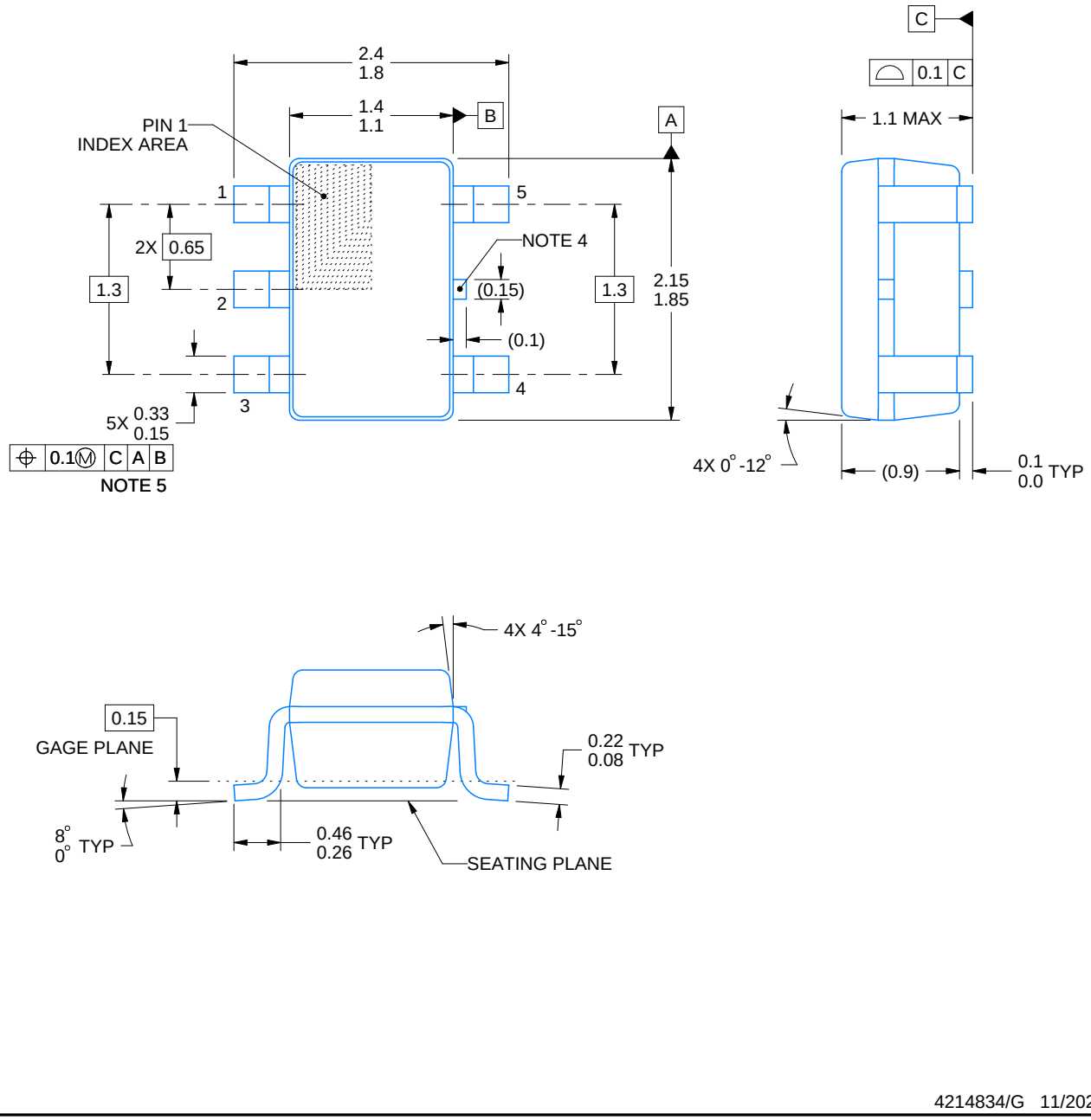
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

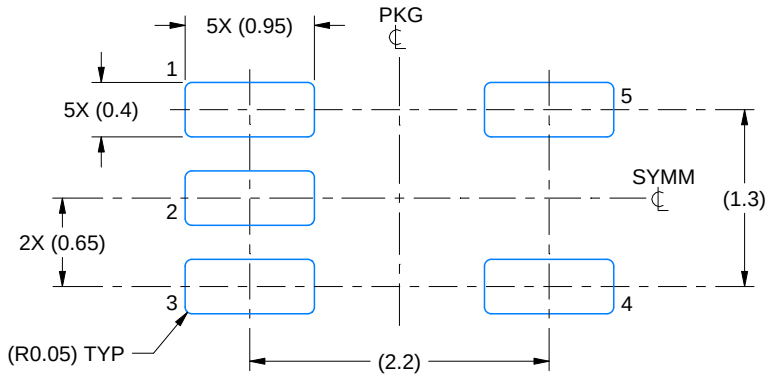
SMALL OUTLINE TRANSISTOR



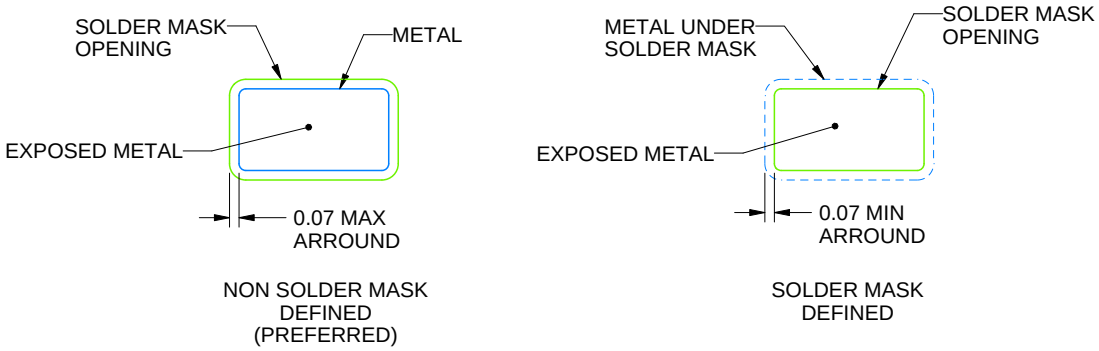
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

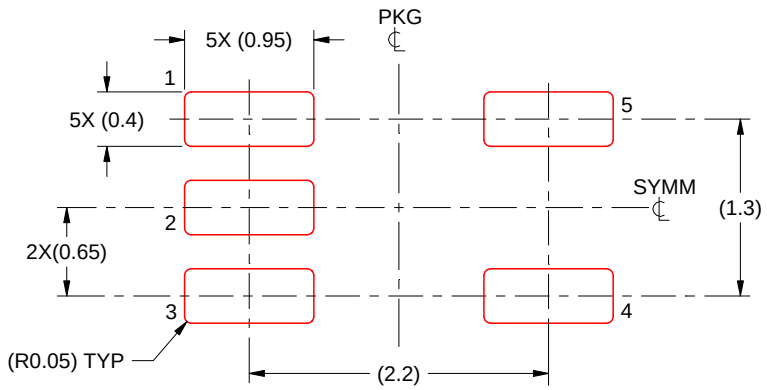


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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