SN74LVC2G101 Dual D-Type Flip-Flop with Configurable Multiple-Function Gated Clock

1 Features

- Operating range from 1.1V to 3.6V
- Over-voltage tolerant inputs support up to 5.5V independent of V_{CC}
- Supports partial-power-down with back drive protection (I_{off})
- High push-pull output drive strength:
  - ±24mA at 3.3V
  - ±8mA at 2.3V
  - ±4mA at 1.65V
- Maximum propagation delay of 7ns at 3.3V supply
- Latch-up performance exceeds 100mA per JESD78

2 Applications

- Convert a momentary switch to a toggle switch
- Divide a clock signal by 2 or 4

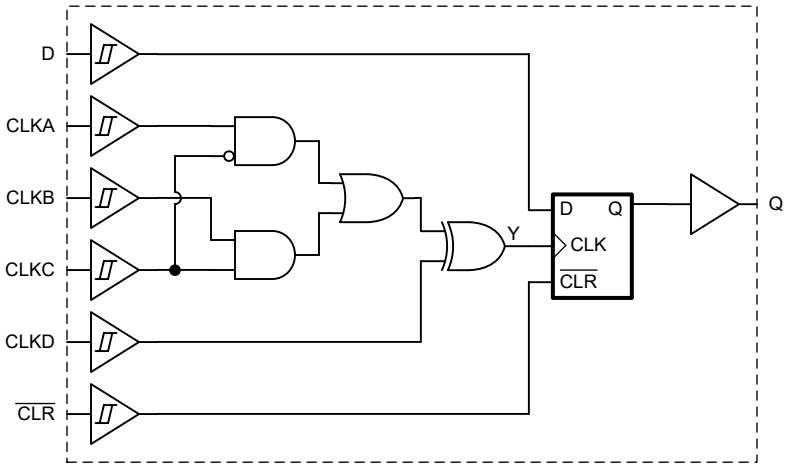
3 Description

The SN74LVC2G101 contains two independent D-type flip-flops. Each channel has data (D), clear ($\overline{CLR}$), and clock (CLKA, CLKB, CLKC, CLKD) inputs and a non-inverted output (Q). The clock inputs can be configured for use in a wide variety of applications, allowing for configuration as 2-input AND, OR, NAND, NOR, XOR, XNOR, as well as 1-input inverted or non-inverted operation. All inputs include Schmitt-trigger architecture.

Package Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE(2)	BODY SIZE (NOM)(3)
SN74LVC2G101	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	PW (TSSOP, 16)(4)	5mm × 6.4mm	5mm × 4.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable
(3) The body size (length × width) is a nominal value and does not include pins.
(4) Preview package.



Functional Diagram

Table of Contents

4 Pin Configuration and Functions

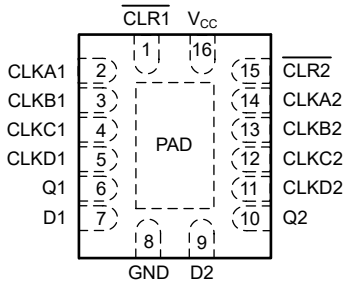


Figure 4-1. BQB Package, 16-Pin WQFN (Top View)

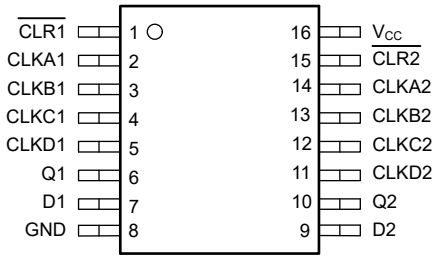


Figure 4-2. PW Package, 16-Pin TSSOP (Preview) (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{CLR1}$	1	I	Channel 1, clear, active low
CLKA1	2	I	Channel 1, clock input A
CLKB1	3	I	Channel 1, clock input B
CLKC1	4	I	Channel 1, clock input C
CLKD1	5	I	Channel 1, clock input D
Q1	6	O	Channel 1, non-inverted output
D1	7	I	Channel 1, data input
GND	8	G	Ground
D2	9	I	Channel 2, data input
Q2	10	O	Channel 2, non-inverted output
CLKD2	11	I	Channel 2, clock input D
CLKC2	12	I	Channel 2, clock input C
CLKB2	13	I	Channel 2, clock input B
CLKA2	14	I	Channel 2, clock input A
$\overline{CLR2}$	15	I	Channel 2, clear, active low
V_{CC}	16	P	Positive supply
Thermal Pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) BQB package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range(2)		-0.5	6.5	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.1	3.6	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8V		-4	mA
		V_{CC} = 2.3V		-8	
		V_{CC} = 2.7V		-12	
		V_{CC} = 3V		-24	
I_{OL}	Low-level output current	V_{CC} = 1.8V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 2.7V		12	
		V_{CC} = 3V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
PW (TSSOP)	16	141.8	74	87.1	22.3	86.6	-	°C/W
BQB (WQFN)	16	98.8	94.3	67.6	15.4	67.6	46.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{T+}	Positive-going input threshold voltage	1.1V	0.5	0.64	0.8	V
		1.2V	0.53	0.72	0.9	V
		1.5V	0.7	0.86	1.11	V
		1.65V	0.4	0.93	1.3	V
		1.95V	0.6	1.07	1.5	V
		2.3V	0.8	1.22	1.7	V
		2.5V	0.8	1.3	1.7	V
		2.7V	0.8	1.38	2	V
		3V	0.9	1.5	2	V
		3.6V	1.1	1.76	2	V
V_{T-}	Negative-going input threshold voltage	1.1V	0.2	0.31	0.6	V
		1.2V	0.26	0.46	0.65	V
		1.5V	0.34	0.42	0.75	V
		1.65V	0.2	0.47	0.9	V
		1.95V	0.3	0.56	1	V
		2.3V	0.4	0.68	1.2	V
		2.5V	0.4	0.74	1.2	V
		2.7V	0.4	0.81	1.4	V
		3V	0.6	0.91	1.5	V
		3.6V	0.8	1.1	1.7	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	1.1V	0.07	0.34	0.53	V
		1.2V	0.08	0.31	0.54	V
		1.5V	0.18	0.43	0.60	V
		1.65V	0.1	0.46	1.2	V
		1.95V	0.2	0.51	1.3	V
		2.3V	0.3	0.54	1.3	V
		2.5V	0.3	0.56	1.3	V
		2.7V	0.3	0.58	1.1	V
		3V	0.3	0.6	1.2	V
		3.6V	0.3	0.66	1.2	V
V_{OH}	I_{OH}= –100µA	1.1V to 3.6V	V_{CC} - 0.2	V_{CC} - 0.01		V
V_{OH}	I_{OH}= –4mA	1.65V	1.2			V
V_{OH}	I_{OH}= –8mA	2.3V	1.75			V

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH}= –12mA	2.7V	2.2			V
V_{OH}		3V	2.4			V
V_{OH}	I_{OH}= –24mA	3V	2.2			V
V_{OL}	I_{OL} = 100µA	1.1V to 3.6V		0.01	0.2	V
V_{OL}	I_{OL} = 4mA	1.65V			0.45	V
V_{OL}	I_{OL} = 8mA	2.3V			0.7	V
V_{OL}	I_{OL} = 12mA	2.7V			0.4	V
V_{OL}	I_{OL} = 24mA	3V			0.55	V
I_I	V_I = V_{CC} or GND	3.6V			±5	µA
I_{off}	V_I or V_O = V_{CC}	0V			±10	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6V			40	µA
ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND	2.7V to 3.6V			5000	µA
C_I	V_I = V_{CC} or GND	3.3V		4.9		pF
C_O	V_O = V_{CC} or GND	3.3V		6.3		pF
C_{PD}	f = 10MHz	1.8V		12		pF
C_{PD}	f = 10MHz	2.5V		15		pF
C_{PD}	f = 10MHz	3.3V		17		pF

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
f_{clock}	Clock frequency		1.2V ± 0.1V		10	MHz
			1.5V ± 0.15V		40	
f_{clock}	Clock frequency		1.8V ± 0.15V		70	MHz
			2.5V ± 0.2V		150	
			3.3V ± 0.3V		160	
t_W	Pulse duration	$\overline{CLR}$ low	1.2V ± 0.1V	4.3		ns
			1.5V ± 0.15V	1.6		
		CLK	1.2V ± 0.1V	7		
			1.5V ± 0.15V	2.8		
t_W	Pulse duration	$\overline{CLR}$ low	1.8V ± 0.15V	4.1		ns
			2.5 ± 0.2V	3.3		
			3.3V ± 0.3V	3.3		
		CLK	1.8V ± 0.15V	4.1		
			2.5 ± 0.2V	3.3		
			3.3V ± 0.3V	3.3		
t_{SU}	Setup time before CLK↑	D input pin relative to CLKx pins	1.2V ± 0.1V	3.9		ns
			1.5V ± 0.15V	2.5		
		$\overline{CLR}$ Inactive	1.2V ± 0.1V	11.6		
			1.5V ± 0.15V	8.8		

5.6 Timing Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
t_{SU}	Setup time before CLK↑	D input pin relative to CLKx pins	1.8V ± 0.15V	3.6		ns
			2.5 ± 0.2V	2.3		
			3.3V ± 0.3V	2.3		
		$\overline{CLR}$ Inactive	1.8V ± 0.15V	4.3		
			2.5 ± 0.2V	2.5		
			3.3V ± 0.3V	2.3		
t_{CLKA_SU}	Set up time between CLKx inputs	CLKA input pin relative to CLKB, CLKC and CLKD pins	1.2V ± 0.1V	21		ns
t_{CLKA_SU}	Set up time between CLKx inputs	CLKA input pin relative to CLKB, CLKC and CLKD pins	1.5V ± 0.15V	9.7		ns
t_{CLKA_SU}	Set up time between CLKx inputs	CLKA input pin relative to CLKB, CLKC and CLKD pins	1.8V ± 0.15V	21		ns
t_{CLKA_SU}	Set up time between CLKx inputs	CLKA input pin relative to CLKB, CLKC and CLKD pins	2.5V ± 0.2V	9.8		ns
t_{CLKA_SU}	Set up time between CLKx inputs	CLKA input pin relative to CLKB, CLKC and CLKD pins	3.3V ± 0.3V	21		ns
t_{CLKB_SU}	Set up time between CLKx inputs	CLKB input pin relative to CLKA, CLKC and CLKD pins	1.2V ± 0.1V	9.8		ns
t_{CLKB_SU}	Set up time between CLKx inputs	CLKB input pin relative to CLKA, CLKC and CLKD pins	1.5V ± 0.15V	15		ns
t_{CLKB_SU}	Set up time between CLKx inputs	CLKB input pin relative to CLKA, CLKC and CLKD pins	1.8V ± 0.15V	7.8		ns
t_{CLKB_SU}	Set up time between CLKx inputs	CLKB input pin relative to CLKA, CLKC and CLKD pins	2.5V ± 0.2V	7		ns
t_{CLKB_SU}	Set up time between CLKx inputs	CLKB input pin relative to CLKA, CLKC and CLKD pins	3.3V ± 0.3V	5.1		ns
t_{CLKC_SU}	Set up time between CLKx inputs	CLKC input pin relative to CLKA, CLKB and CLKD pins	1.2V ± 0.1V	5.1		ns
t_{CLKC_SU}	Set up time between CLKx inputs	CLKC input pin relative to CLKA, CLKB and CLKD pins	1.5V ± 0.15V	7		ns
t_{CLKC_SU}	Set up time between CLKx inputs	CLKC input pin relative to CLKA, CLKB and CLKD pins	1.8V ± 0.15V	5		ns
t_{CLKC_SU}	Set up time between CLKx inputs	CLKC input pin relative to CLKA, CLKB and CLKD pins	2.5V ± 0.2V	5		ns
t_{CLKC_SU}	Set up time between CLKx inputs	CLKC input pin relative to CLKA, CLKB and CLKD pins	3.3V ± 0.3V	7		ns
t_{CLKD_SU}	Set up time between CLKx inputs	CLKD input pin relative to CLKA, CLKB and CLKC pins	1.2V ± 0.1V	5		ns
t_{CLKD_SU}	Set up time between CLKx inputs	CLKD input pin relative to CLKA, CLKB and CLKC pins	1.5V ± 0.15V	5		ns
t_{CLKD_SU}	Set up time between CLKx inputs	CLKD input pin relative to CLKA, CLKB and CLKC pins	1.8V ± 0.15V	5.4		ns
t_{CLKD_SU}	Set up time between CLKx inputs	CLKD input pin relative to CLKA, CLKB and CLKC pins	2.5V ± 0.2V	3.9		ns
t_{CLKD_SU}	Set up time between CLKx inputs	CLKD input pin relative to CLKA, CLKB and CLKC pins	3.3V ± 0.3V	3.9		ns
t_H	Hold time, data after CLK↑	D input pin relative to CLKx pins	1.2V ± 0.1V	10		ns
			1.5V ± 0.15V	4		

5.6 Timing Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
t_H	Hold time, data after CLK↑	D input pin relative to CLKx pins	1.8V ± 0.15V	2.8		ns
			2.5 ± 0.2V	2.3		
			3.3 ± 0.3V	2.3		

5.7 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	CLK	Q	C_L = 15pF	1.2V ± 0.1V		17.7	33	ns
t_{pd}	CLK	Q	C_L = 15pF	1.5V ± 0.12V		9.9	18	ns
t_{pd}	CLK	Q	C_L = 30pF	1.8V ± 0.15V		7.7	13	ns
t_{pd}	CLK	Q	C_L = 30pF	2.5V ± 0.2V		5.1	8	ns
t_{pd}	CLK	Q	C_L = 50pF	2.7V		5	8	ns
t_{pd}	CLK	Q	C_L = 50pF	3.3V ± 0.3V		4.7	7	ns
t_{pd}	$\overline{CLR}$	Q	C_L = 15pF	1.2V ± 0.1V		29.8	51	ns
t_{pd}	$\overline{CLR}$	Q	C_L = 15pF	1.5V ± 0.12V		11.8	19	ns
t_{pd}	$\overline{CLR}$	Q	C_L = 30pF	1.8V ± 0.15V		8.5	14	ns
t_{pd}	$\overline{CLR}$	Q	C_L = 30pF	2.5V ± 0.2V		5.7	10	ns
t_{pd}	$\overline{CLR}$	Q	C_L = 50pF	2.7V		5.5	9	ns
t_{pd}	$\overline{CLR}$	Q	C_L = 50pF	3.3V ± 0.3V		5.2	9	ns
$t_{sk(o)}$				3.3V ± 0.3V			1	ns

5.8 Noise Characteristics

VCC = 3.3V, CL = 50pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8	-0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	2.2	3.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.0			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

5.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

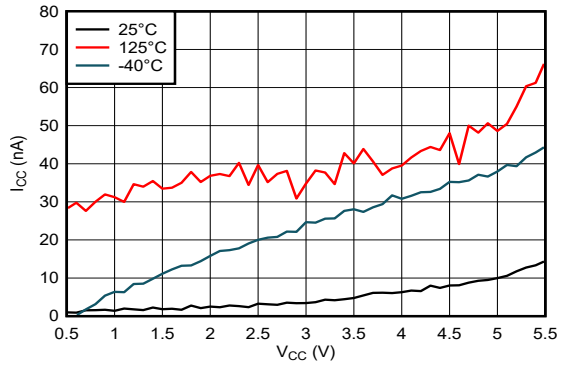


Figure 5-1. Supply Current Across Supply Voltage

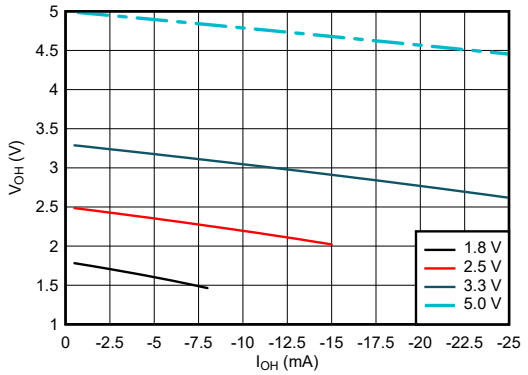


Figure 5-2. Output Voltage vs Current in HIGH State

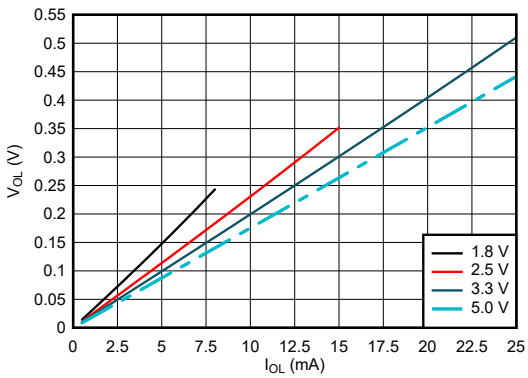


Figure 5-3. Output Voltage vs Current in LOW State

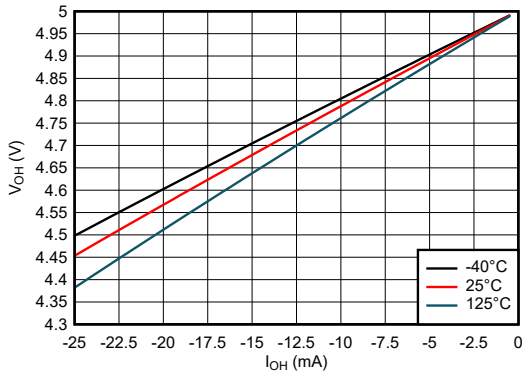


Figure 5-4. Output Voltage vs Current in HIGH State; 5V Supply

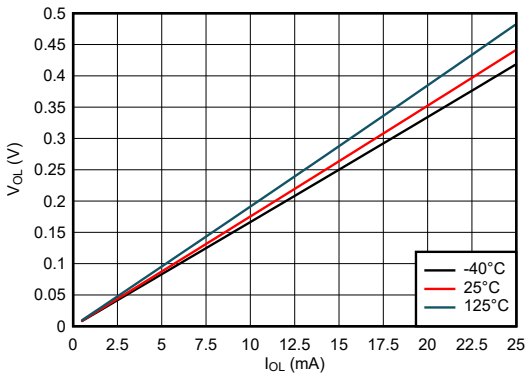


Figure 5-5. Output Voltage vs Current in LOW State; 5V Supply

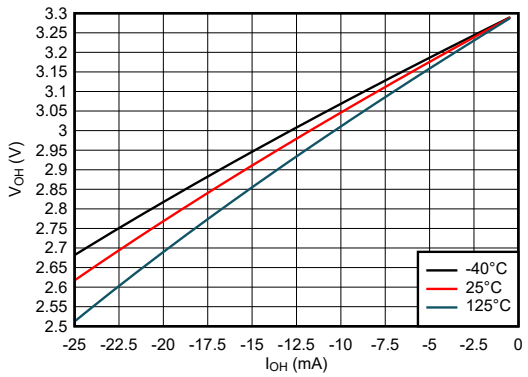


Figure 5-6. Output Voltage vs Current in HIGH State; 3.3V Supply

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

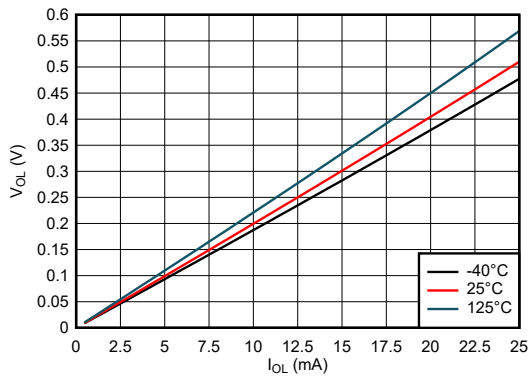


Figure 5-7. Output Voltage vs Current in LOW State; 3.3V Supply

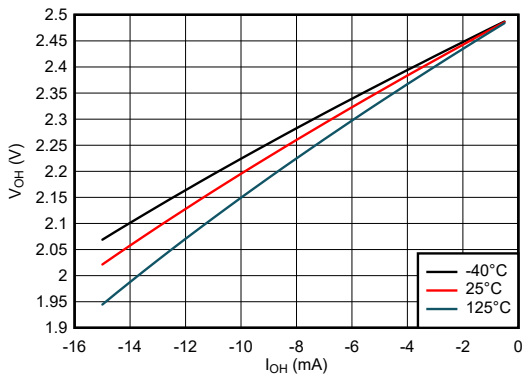


Figure 5-8. Output Voltage vs Current in HIGH State; 2.5V Supply

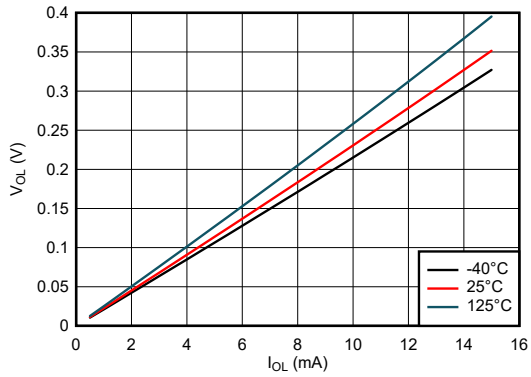


Figure 5-9. Output Voltage vs Current in LOW State; 2.5V Supply

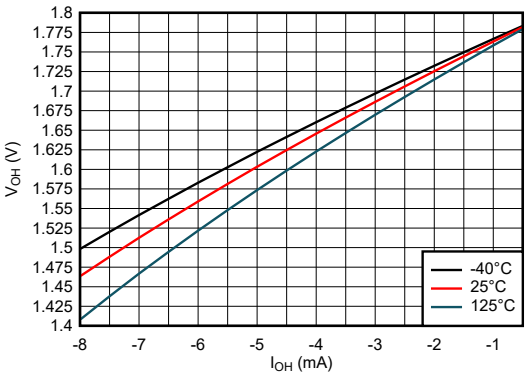


Figure 5-10. Output Voltage vs Current in HIGH State; 1.8V Supply

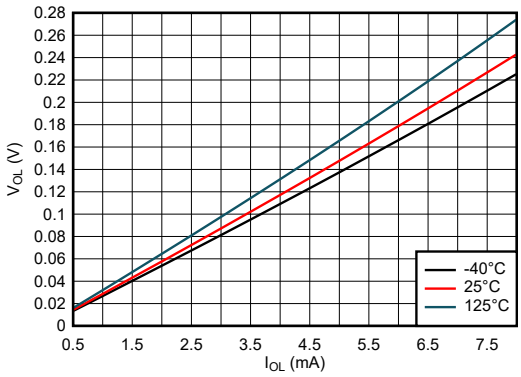


Figure 5-11. Output Voltage vs Current in LOW State; 1.8V Supply

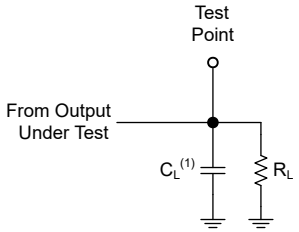
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured individually with one input transition per measurement.

V_{CC}	V_t	R_L	C_L	ΔV
1.2V ± 0.1V	V_{CC}/2	2kΩ	15pF	0.1V
1.5V ± 0.12V	V_{CC}/2	2kΩ	15pF	0.1V
1.8V ± 0.15V	V_{CC}/2	1kΩ	30pF	0.15V
2.5V ± 0.2V	V_{CC}/2	500Ω	30pF	0.15V
2.7V	1.5V	500Ω	50pF	0.3V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

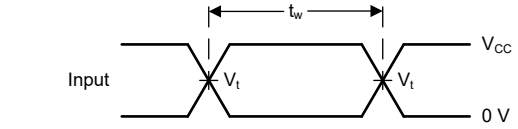


Figure 6-2. Voltage Waveforms, Pulse Duration

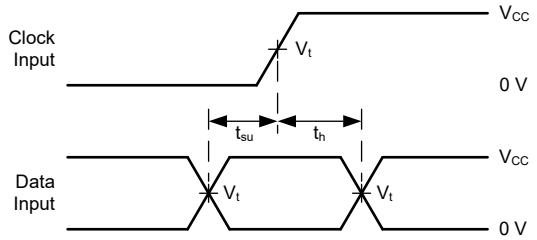
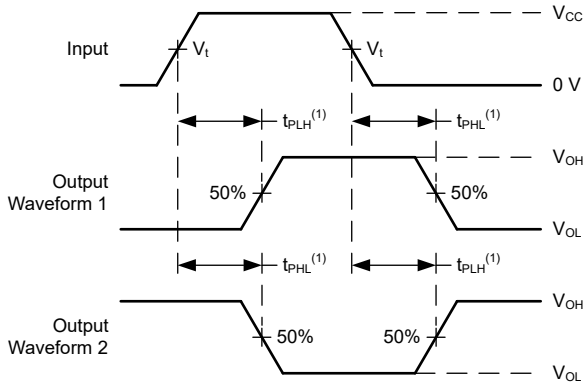
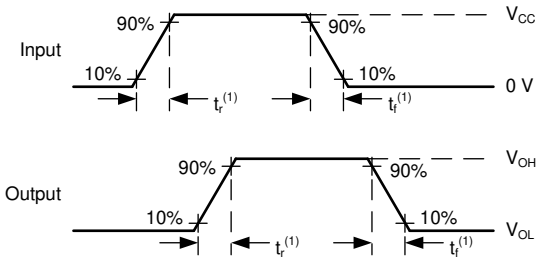


Figure 6-3. Voltage Waveforms, Setup and Hold Times



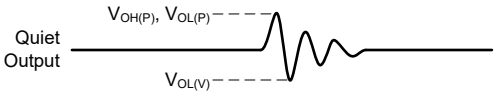
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-5. Voltage Waveforms, Input and Output Transition Times



Noise values measured with all other outputs simultaneously switching.

Figure 6-6. Voltage Waveforms, Noise

7 Detailed Description

7.1 Overview

The SN74LVC2G101 contains two independent D-type flip-flops. Each channel has separate data (D) and asynchronous active-low clear ($\overline{CLR}$) inputs, output (Q), as well as configurable clock inputs (CLKA, CLKB, CLKC, CLKD). The clock inputs utilize combinational logic to provide a variety of possible logic combinations, including common 2-input gates as well as inverted and non-inverted configurations.

7.2 Functional Block Diagram

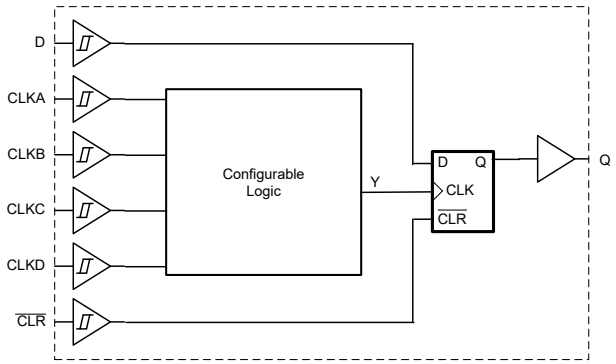


Figure 7-1. Each channel

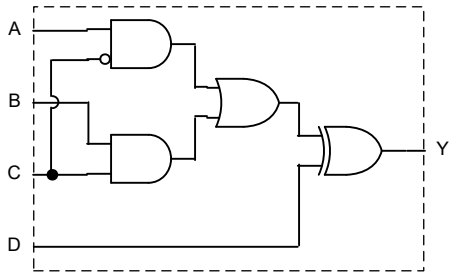


Figure 7-2. Configurable logic

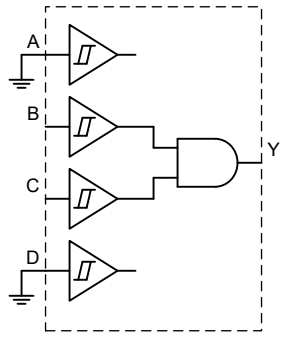


Figure 7-3. 2-input AND configuration

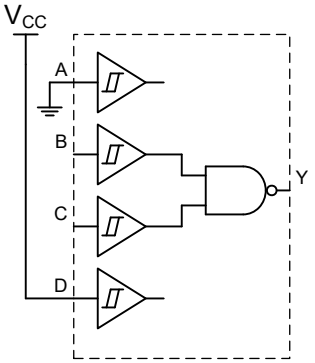


Figure 7-4. 2-input NAND configuration

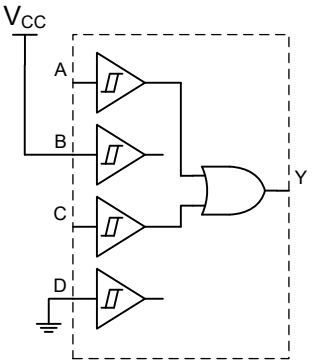


Figure 7-5. 2-input OR configuration

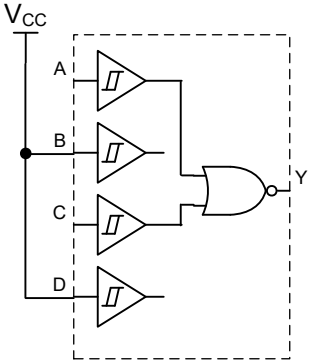


Figure 7-6. 2-input NOR configuration

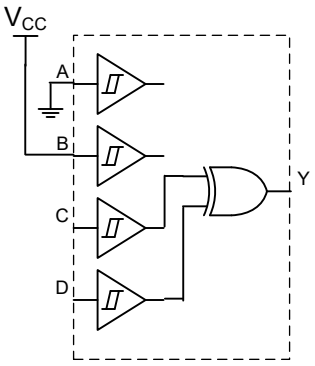


Figure 7-7. 2-input XOR configuration

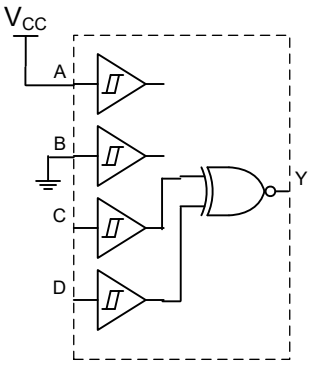


Figure 7-8. 2-input XNOR configuration

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

7.3.3 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

7.3.4 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

7.3.5 Clamp Diode Structure

Figure 7-9 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

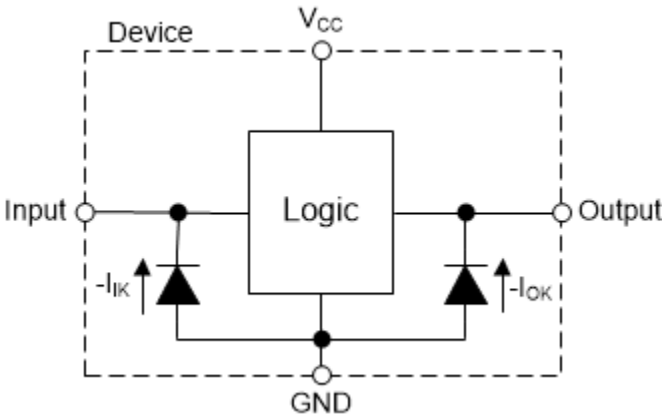


Figure 7-9. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Flip-Flop Function Table

INPUTS(1)			OUTPUT(2)
$\overline{CLR}$	CLK(3)	D	Q
L	X	X	L
H	L, H, ↓	X	Q0
H	↑	L	L
H	↑	H	H

(1) L = Input low, H = Input high, ↑ = Input transitioning from low to high, ↓ = Input transitioning from high to low, X = Don't care
(2) L = Output low, H = Output high, Q_0 = Previous state
(3) Internal flip-flop input, denoted as Y on functional block diagram

Table 7-2. Combinational Logic Function Table

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	L
L	L	L	H	H
L	L	H	L	L
L	L	H	H	H
L	H	L	L	L
L	H	L	H	H
L	H	H	L	H
L	H	H	H	L
H	L	L	L	H
H	L	L	H	L
H	L	H	L	L
H	L	H	H	H
H	H	L	L	H
H	H	L	H	L

Table 7-2. Combinational Logic Function Table (continued)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	L	H
H	H	H	H	L

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74LVC2G101 is used to read in two different active-high fault signals (FAULT1, FAULT2) and latch an output signal (LATCHED FAULT) high when the boolean logic FAULT1 OR FAULT2 has a rising edge.

At power-up, the initial state of the flip-flop is unknown. To give it a defined state of zero, the device can be cleared by applying a low signal to the clear ($\overline{CLR}$) input.

8.2 Typical Application

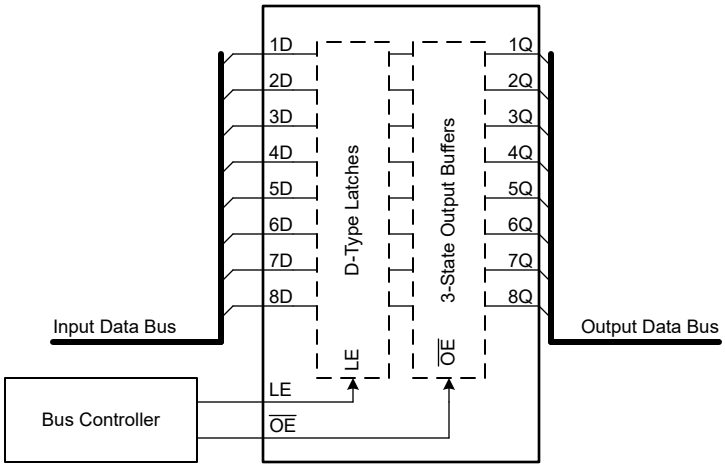


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC2G101 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC2G101 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC2G101 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LVC2G101 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC2G101 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC2G101 has no input signal transition rate requirements because it has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC2G101 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.2.3 Reference

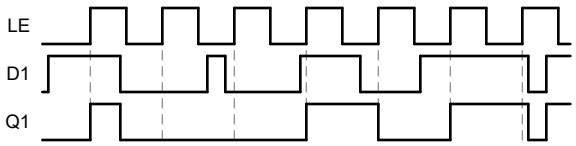


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

During startup, the power supply should ramp within the provided power-up ramp rate range in the *Recommended Operating Conditions* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For the SN74LVC2G101, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

8.4.2 Layout Example

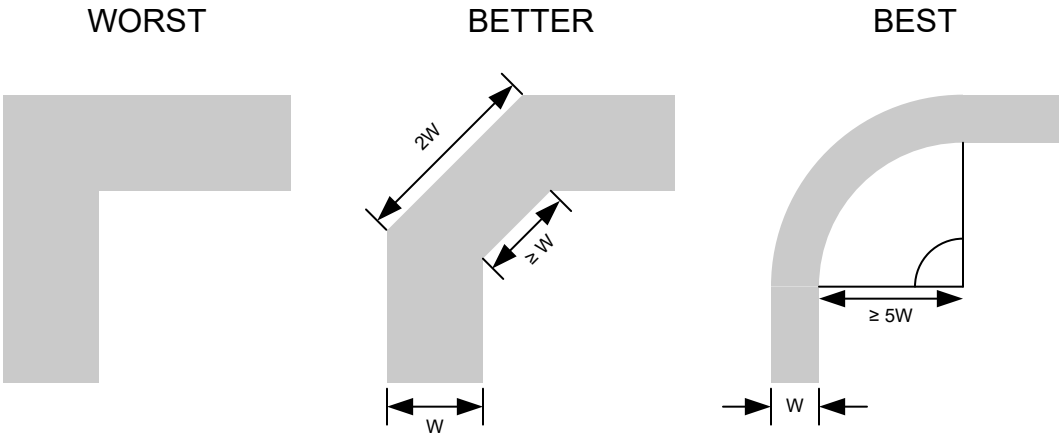


Figure 8-3. Example trace corners for improved signal integrity

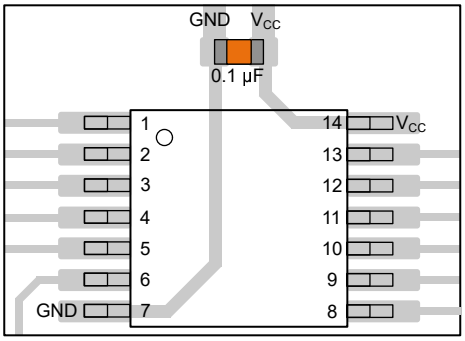


Figure 8-4. Example bypass capacitor placement for TSSOP and similar packages

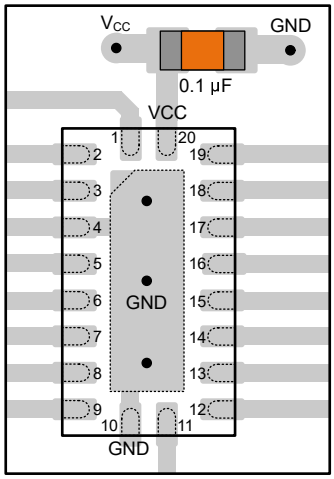


Figure 8-5. Example bypass capacitor placement for WQFN and similar packages

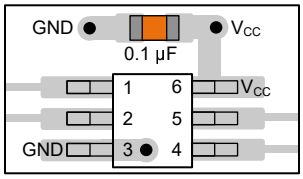


Figure 8-6. Example bypass capacitor placement for SOT, SC70 and similar packages

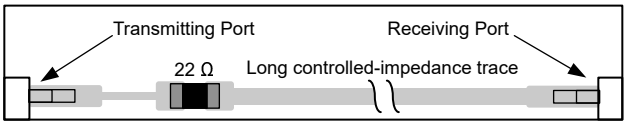


Figure 8-7. Example damping resistor placement for improved signal integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
June 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G101BQBR	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2G101	Samples
SN74LVC2G101PWR	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LC2G101	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVC2G101 :

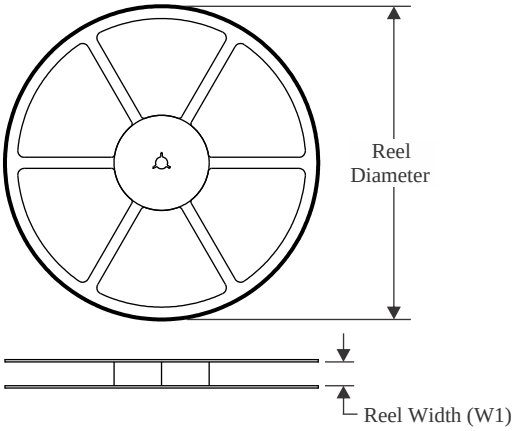
- Automotive : SN74LVC2G101-Q1

NOTE: Qualified Version Definitions:

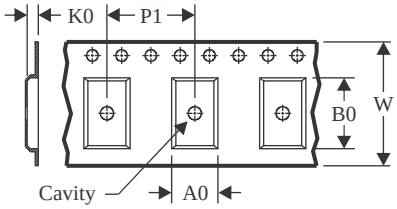
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

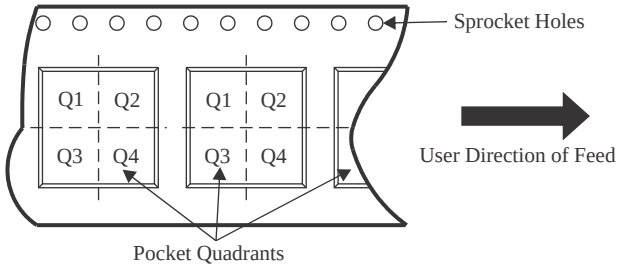


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

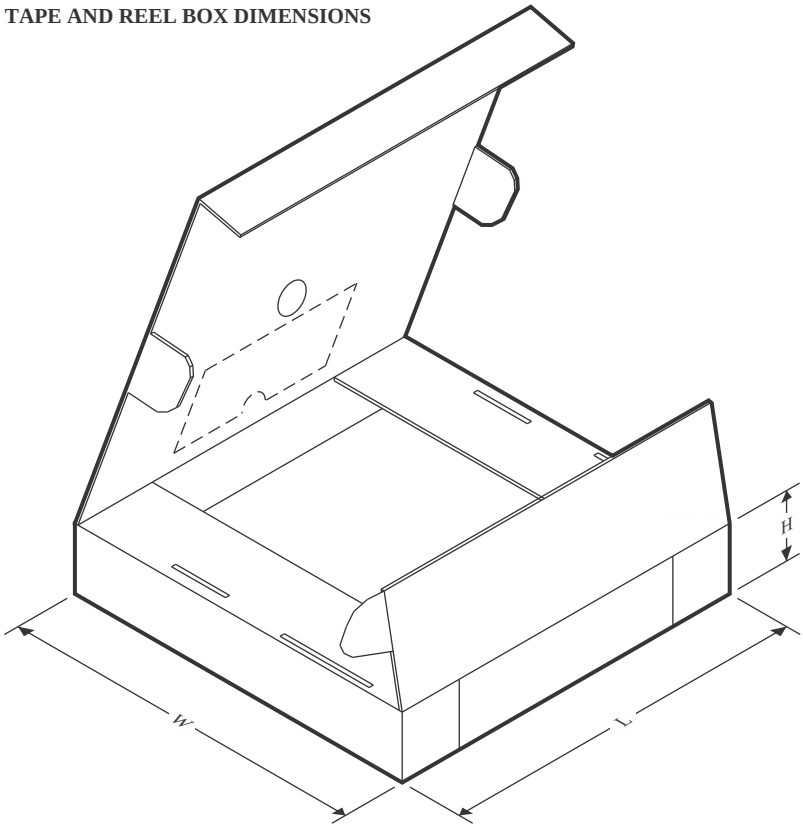
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G101PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

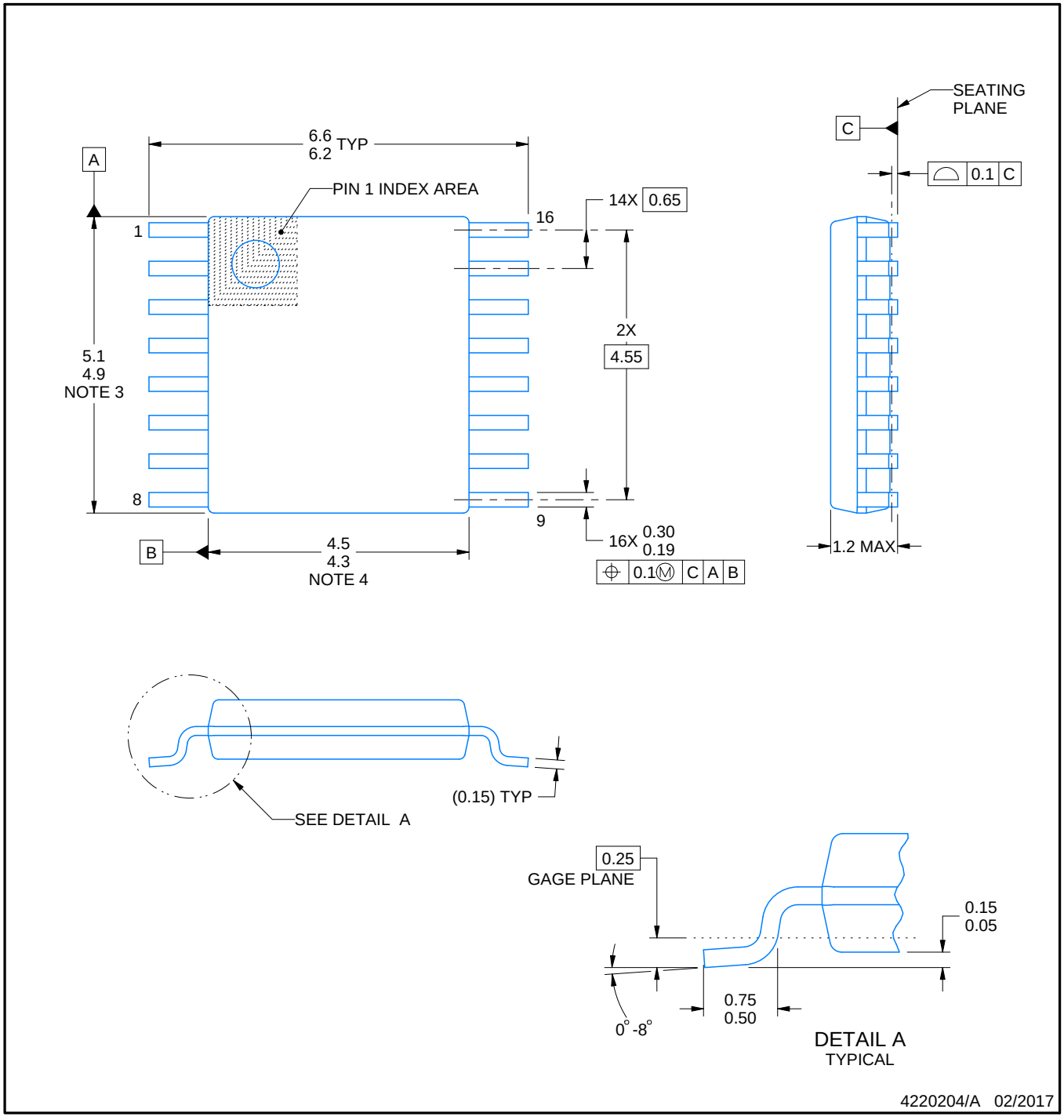
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G101PWR	TSSOP	PW	16	3000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

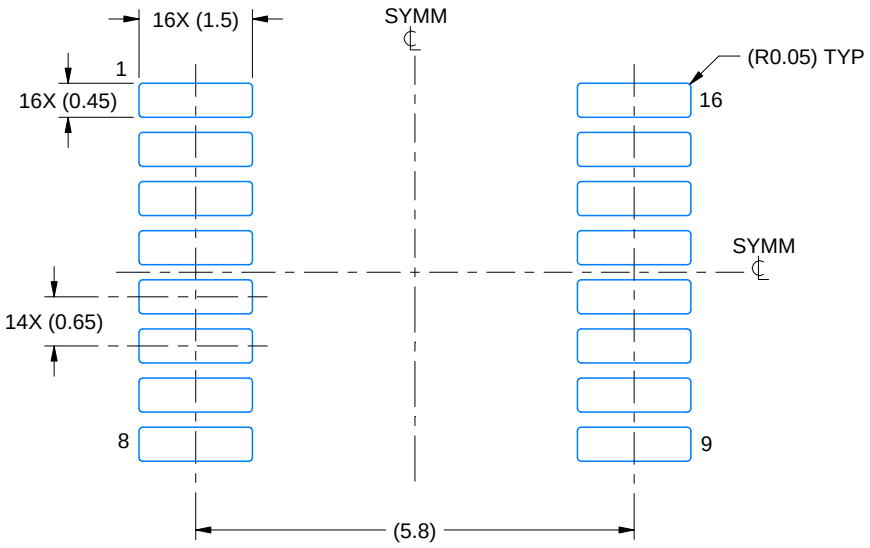
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

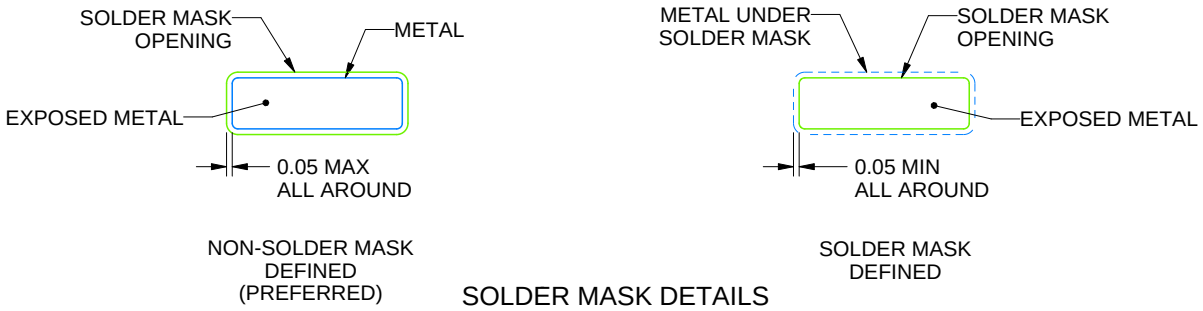


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

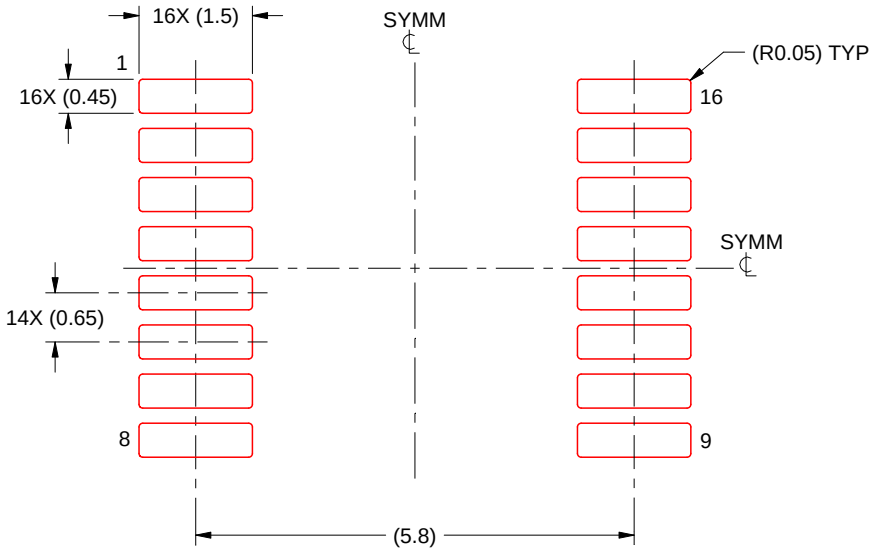


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

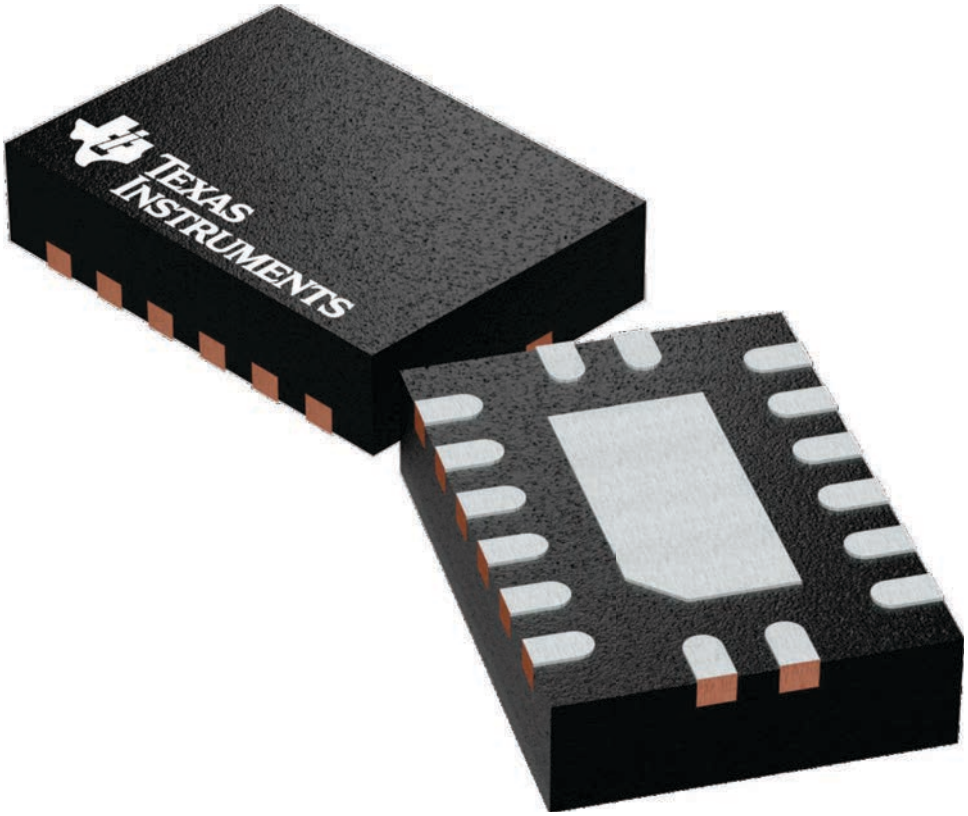
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



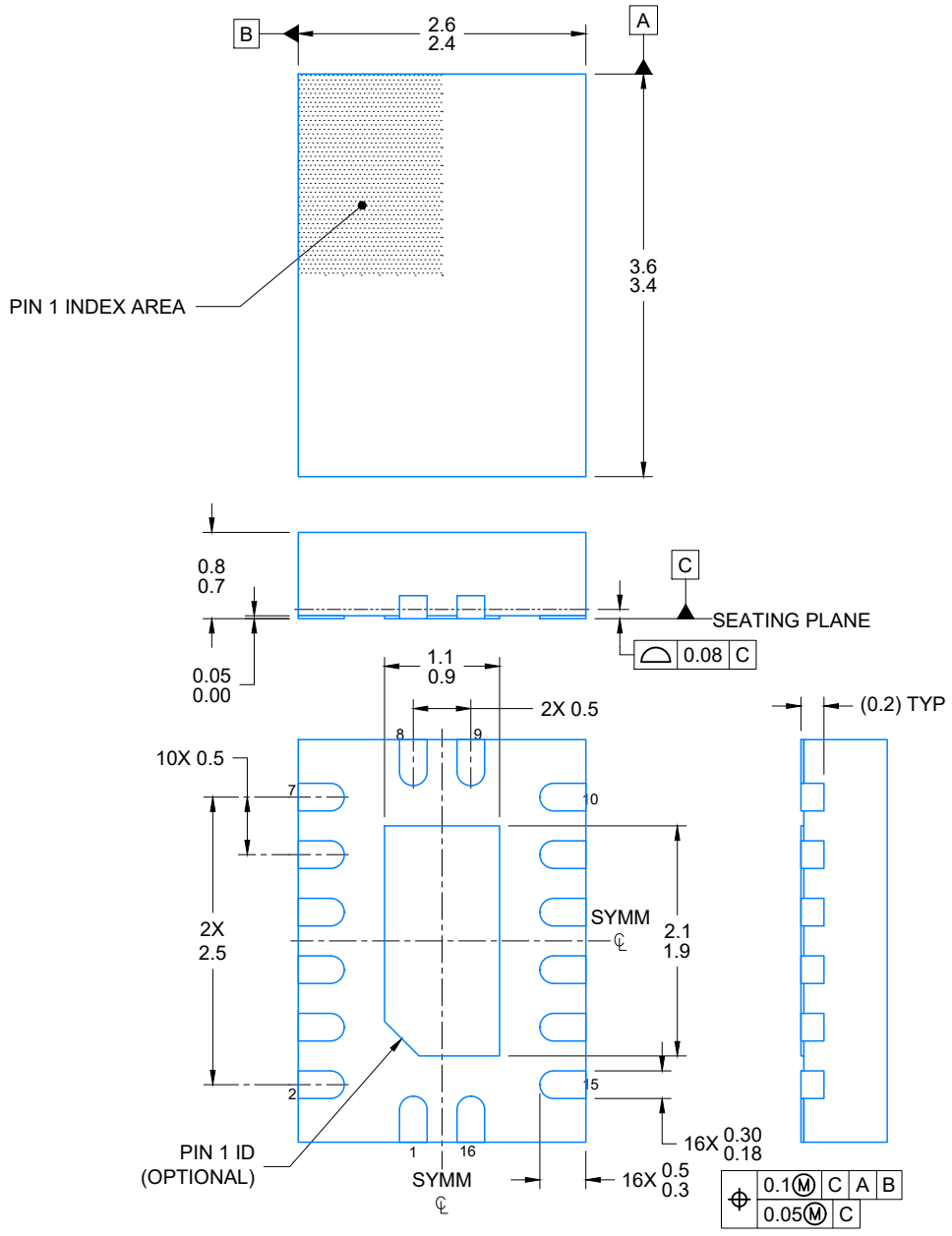
4226161/A

PACKAGE OUTLINE

BQB0016A

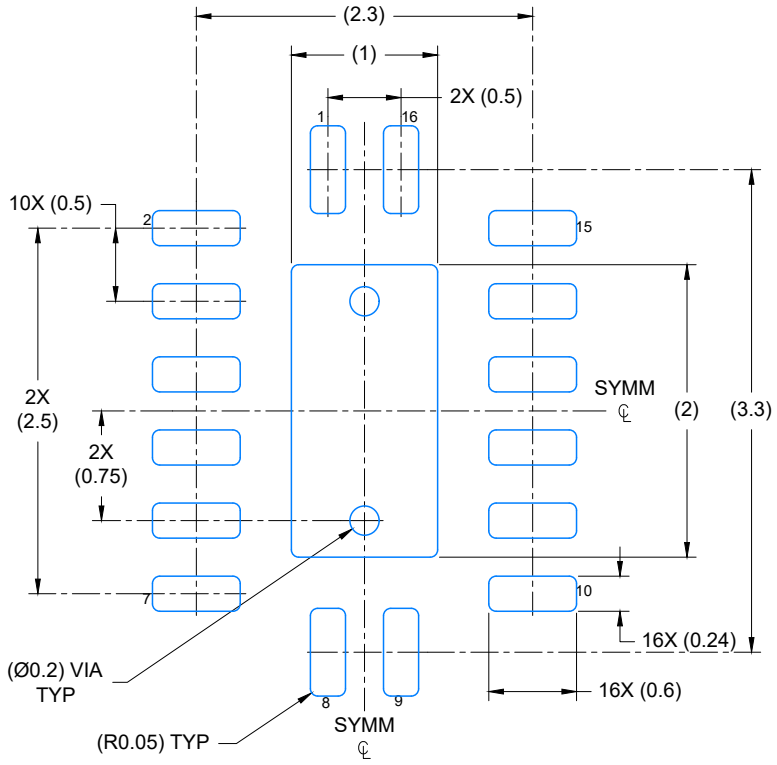
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

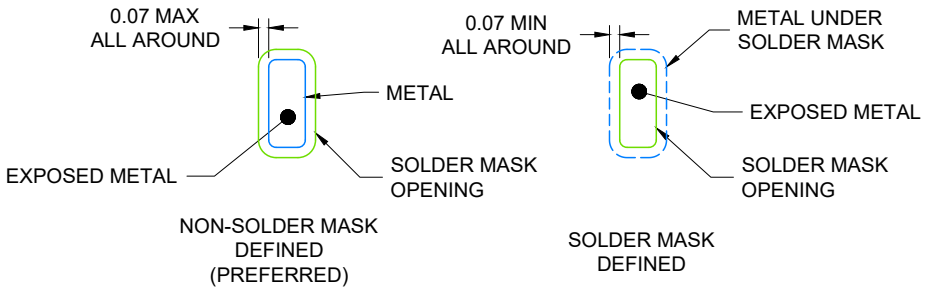


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



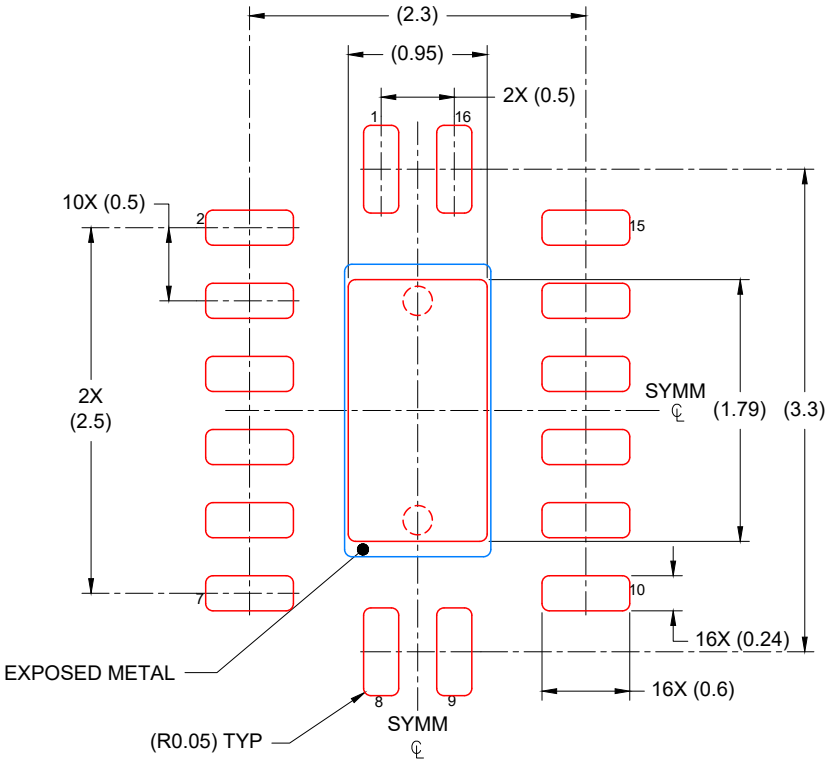
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265