

## TCA9511A Hot Swappable I<sup>2</sup>C Bus and SMBus Buffer

### 1 Features

- Supports bidirectional data transfer of I<sup>2</sup>C bus signals
- Operating power-supply voltage range of 2.3 V to 5.5 V
- T<sub>A</sub> ambient air temperature range of -40 °C to 125 °C
- 1-V Precharge on all SDA and SCL lines prevents corruption during live insertion
- Accommodates standard mode and fast mode I<sup>2</sup>C devices
- Supports clock stretching, arbitration and synchronization
- Powered-off high-impedance I<sup>2</sup>C pins

### 2 Applications

- [Servers](#)
- [Enterprise Switching](#)
- [Telecom switching equipment](#)
- [Base stations](#)
- [Industrial automation equipment](#)

### 3 Description

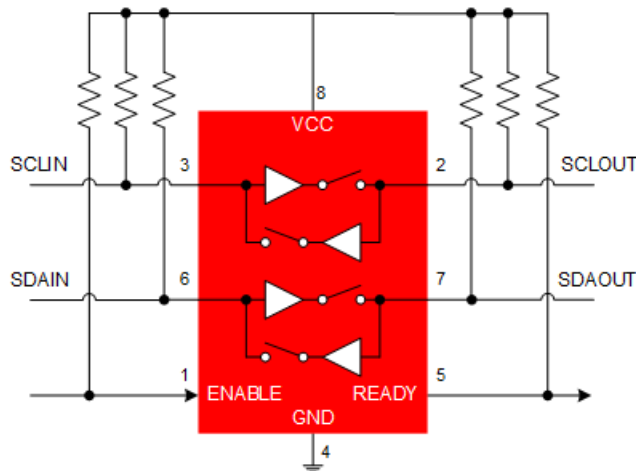
The TCA9511A is a hot-swappable I<sup>2</sup>C bus buffer that supports I/O card insertion into a live backplane without corruption of the data and clock lines. Control circuitry prevents the backplane-side I<sup>2</sup>C lines (in) from being connected to the card-side I<sup>2</sup>C lines (out) until a stop command or bus idle condition occurs on the backplane without bus contention on the card. When the connection is made, this device provides bidirectional buffering, keeping the backplane and card capacitances isolated. During insertion, the SDA and SCL lines are pre-charged to 1 V to minimize the current required to charge the parasitic capacitance of the device.

When the I<sup>2</sup>C bus is idle, the TCA9511A can be put into shutdown mode by setting the EN pin low, reducing power consumption. When EN is pulled high, the TCA9511A resumes normal operation. It also includes an open drain READY output pin, which indicates that the backplane and card sides are connected together. When READY is high, the SDAIN and SCLIN are connected to SDAOUT and SCLOUT. When the two sides are disconnected, READY is low.

#### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
TCA9511A	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Schematic**

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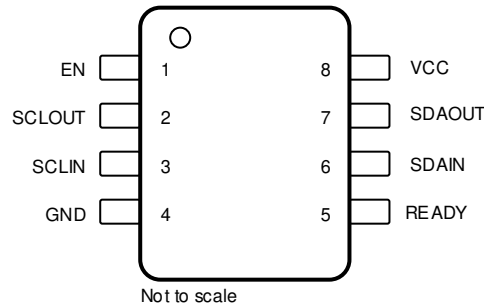
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (March 2020) to Revision C (January 2021)</b>	<b>Page</b>
• Deleted the <i>Device Comparison Table</i> .....	3
• Changed the VCC pin recommended capacitance From: 0.01 $\mu$ F To: 0.1 $\mu$ F to match typical application section.....	3
• Changed HBM ESD from 1500 V to 3500 V.....	4
• Changed ICC values from 6 mA max to 4.5 mA, and typical improved to 2.5 mA.....	5
• Changed $V_{OS}$ typical from 50 mV to 60 mV.....	5
<b>Changes from Revision A (December 2019) to Revision B (March 2020)</b>	<b>Page</b>
• Changed pin 7 From: SDAOUTL To: SDAOUT.....	3
• Changed text From: "pulled to roughly 160 mV." To: "pulled to roughly 150 mV" in the <i>Bus active</i> section.....	11
• Changed the device number of <a href="#">Figure 11-1</a> to TCA9511A .....	18
<b>Changes from Revision * (October 2019) to Revision A (December 2019)</b>	<b>Page</b>
• Changed the device status From: <i>Advanced Information</i> To: <i>Production data</i> .....	1

## 5 Pin Configuration and Functions



**Figure 5-1. 8-Pin VSSOP, DGK Package (Top View)**

**Table 5-1. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Active-high chip enable pin. If EN is low, the TCA9511A is in a low current mode. It also disables the rise-time accelerators, disables the bus pre-charge circuitry, drives READY low, isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT. EN should be high (at VCC) for normal operation. Connect EN to VCC if this feature is not being used.
SCLOUT	2	I/O	Serial clock output. Connect this pin to the SCL bus on the card.
SCLIN	3	I/O	Serial clock input. Connect this pin to the SCL bus on the backplane.
GND	4	-	Supply ground
READY	5	O	Connection flag/rise-time accelerator control. Ready is low when either EN is low or the start-up sequence has not been completed. READY goes high when EN is high and start-up is complete. Connect a 10-kΩ resistor from this pin to V <sub>CC</sub> to provide the pull-up current.
SDAIN	6	I/O	Serial data input. Connect this pin to the SDA bus on the backplane.
SDAOUT	7	I/O	Serial data output. Connect this pin to the SDA bus on the card.
VCC	8	-	Supply Power. Main input power supply from backplane. This is the supply voltage for the devices on the backplane I <sup>2</sup> C buses. Connect pull-up resistors from SDAIN and SCLIN (and also from SDAOUT and SCLOUT) to this supply. It is recommended to place a bypass capacitor of 0.1 μF close to this pin for best results.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
Input Voltage	VCC		-0.5	7	V
	SDAIN, SCLIN, SDAOUT, SCLOUT		-0.5	7	V
	EN, READY		-0.5	7	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current	SDAIN, SDAOUT, SCLIN, SCLOUT, EN, READY		±50	mA
I <sub>CC</sub>	Continuous current through VCC or GND			±100	mA
T <sub>J</sub>	Maximum junction temperature			130	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	±3500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	5.5	V
V <sub>I</sub>	Input voltage range	EN input	0	5.5	
V <sub>IO</sub>	Input/output voltage range	SDAIN, SCLIN, SDAOUT, SCLOUT	0	5.5	
V <sub>O</sub>	Output voltage range	READY	0	5.5	
T <sub>A</sub>	Ambient temperature		-40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TCA9511		UNIT
		DGK		
		8 Pin		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	177.1		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	64.5		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	99.6		°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	9.5		°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	97.9		°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A		°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted). Typical specifications are at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
$I_{CC}$	Supply current	$V_{CC} = 5.5\text{ V}$ SDAIN, SCLIN = 0V SDAOUT, SCLOUT = 10k $R_{PU}$		2.5	4.5	mA
$I_{SD}$	Supply current in shutdown mode through the $V_{CC}$ pin <sup>(1)</sup>	EN = 0 V SDAIN, SCLIN, SDAOUT, SCLOUT = 0V or $V_{CC}$ READY pin = Hi-Z EN pulled low after bus connection event (disable precharge)		5	30	$\mu\text{A}$
UVLO	Under voltage lockout (rising)	EN = $V_{CC}$		2.1		V
	Under voltage lockout (falling)	READY = 10 k $\Omega$ to $V_{CC}$		2		V
<b>START-UP CIRCUITRY</b>						
$V_{PRE}$	Pre-charge voltage	SDA, SCL = Hi-Z	0.8	1	1.2	V
<b>RISE-TIME ACCELERATORS</b>						
$I_{PU}$	RTA pull-up current <sup>(2)</sup>	Position transition on SDA, SCL $V_{SDA/SCL} = 0.6\text{ V}$ , Slew rate = 1.25 V/ $\mu\text{s}$ . $V_{CC} = 3.3\text{ V}$	2	5		mA
<b>INPUT-OUTPUT CONNECTION</b>						
$I_{LI}$	Input pin leakage	SDA/SCL pins = 90% $V_{CC}$ , EN = $V_{CC}$ , GND SDA/SCL pins = 10% $V_{CC}$ , EN = GND	-1		1	$\mu\text{A}$
$V_{OS}$	Input-output offset voltage (SCLIN to SCLOUT, SCLOUT to SCLIN and SDAIN to SDAOUT, SDAOUT to SDAIN)	$R_{PU}$ for SDA/SCL = 10 k $\Omega$		60	100	mV
$I_{I\_RDY}$	Ready pin leakage	EN = $V_{CC}$ , READY = $V_{CC}$ , Bus connected	-1		1	$\mu\text{A}$
<b>DIGITAL IO THRESHOLD</b>						
$V_{IH}$	High-level input voltage	EN	$0.7 \times V_{CC}$		$V_{CC}$	V
$V_{IL}$	Low-level input voltage	EN	0		$0.3 \times V_{CC}$	
$V_{OL}$	Low-level output voltage	SDAIN, SCLIN, SDAOUT, SCLOUT $I_{OL} = 4\text{ mA}$ $V_{IN} = 0.1\text{ V}$		0.15	0.4	
		READY $I_{OL} = 3\text{ mA}$	0		0.4	
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{IN(EN)}$	EN input capacitance	$V_{EN} = 0\text{ V}$ or $V_{CC}$ $f = 400\text{ kHz}$		1.6	4	pF
$C_{IO(READY)}$	READY output capacitance	$V_{READY} = 0\text{ V}$ or $V_{CC}$ $f = 400\text{ kHz}$		7	10	
$C_{IO(SDA/SCL)}$	SDA/SCL pin capacitance	$V_{PIN} = 0\text{ V}$ or $V_{CC}$ $f = 400\text{ kHz}$		5	10	

(1) In shutdown mode there will also be current flowing from  $V_{CC}$  through the ready pin as this pin is pulled down to indicate the bus is disconnected.

(2) Determined by design, not tested in production.

## 6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
$f_{SCL\_MAX}$	Maximum SCL clock frequency	400			kHz

## 6.6 Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
$t_{BUF}^{(1)}$	Bus free time between a STOP and START condition	1.3			$\mu\text{s}$
$t_{HD,STA}^{(1)}$	Hold time for a repeated START condition	0.6			$\mu\text{s}$
$t_{SU,STA}^{(1)}$	Set-up time for a repeated START condition	0.6			$\mu\text{s}$
$t_{SU,STO}^{(1)}$	Set-up time for a STOP condition	0.6			$\mu\text{s}$
$t_{HD,DAT}^{(1)}$	Data hold time	0			ns
$t_{SU,DAT}^{(1)}$	Data set-up time	100			ns
$t_{LOW}^{(1)}$	LOW period of the SCL clock	1.3			$\mu\text{s}$
$t_{HIGH}^{(1)}$	HIGH period of the SCL clock	0.6			$\mu\text{s}$
$t_f^{(1)}$	Fall time of both SDA and SCL signals	$20 \times (V_{CC}/5.5 \text{ V})$		300	ns
$t_r^{(1)}$	Rise time of both SDA and SCL signals	$20 \times (V_{CC}/5.5 \text{ V})$		300	ns

(1) These are system-level timing specs and are dependent upon bus capacitance and pull up resistor value. It is up to the system designer to ensure they are met

## 6.7 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted). Typical specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V}$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>START-UP CIRCUITRY</b>					
$t_{PRECHARGE}$	Time from $V_{CC}$ to precharge enabled	SDA,SCL = Hi-Z EN = $V_{CC}$ , GND	15	60	$\mu\text{s}$
$t_{EN}$	Time from $V_{POR}$ to digital being ready	$V_{CC}$ transition from 0V to $V_{CC}$ Time from $V_{PORR}$ to earliest stop bit recongized	35	95	$\mu\text{s}$
$t_{IDLE}$	Bus idle time to READY active	SDA,SCL = 10 k $\Omega$ to $V_{CC}$ EN = $V_{CC}$ Measured at $0.5 \times V_{CC}$	95	150	$\mu\text{s}$
$t_{DISABLE}$	Time from EN high to low to READY low	SDA,SCL = 10 k $\Omega$ to $V_{CC}$ READY = 10 k $\Omega$ to $V_{CC}$ Measured at $0.5 \times V_{CC}$	30	200	ns
$t_{STOP}$	SDAIN to READY delay after stop condition	SDA,SCL = 10 k $\Omega$ to $V_{CC}$ READY = 10 k $\Omega$ to $V_{CC}$ Measured at $0.5 \times V_{CC}$	1.2	2	$\mu\text{s}$
$t_{READY}$	SCLOUT/SDAOUT to READY	SDA,SCL = 10 k $\Omega$ to $V_{CC}$ READY = 10 k $\Omega$ to $V_{CC}$ Measured at $0.5 \times V_{CC}$	0.8	1.5	$\mu\text{s}$
<b>INPUT-OUTPUT CONNECTION</b>					
$t_{PLZ}$	Low to high propagation delay	$R_{PU}$ for SDA/SCL = 10 k $\Omega$ $C_L$ = 100 pF per pin Measured at $0.5 \times V_{CC}$	0	10	ns
$t_{PZL}$	High to low propagation delay	$R_{PU}$ for SDA/SCL = 10 k $\Omega$ $C_L$ = 100 pF per pin Measured at $0.5 \times V_{CC}$	70	150	ns

## 6.8 Typical Characteristics

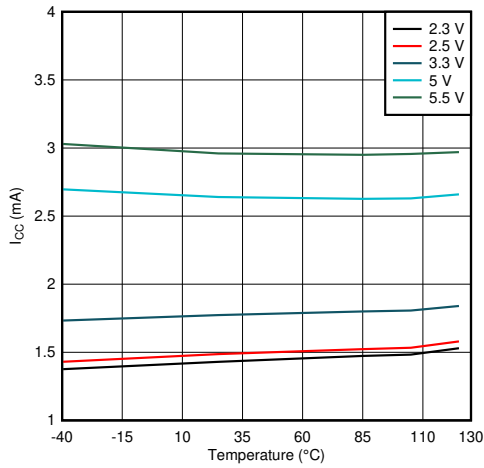


Figure 6-1.  $I_{CC}$  vs Temperature

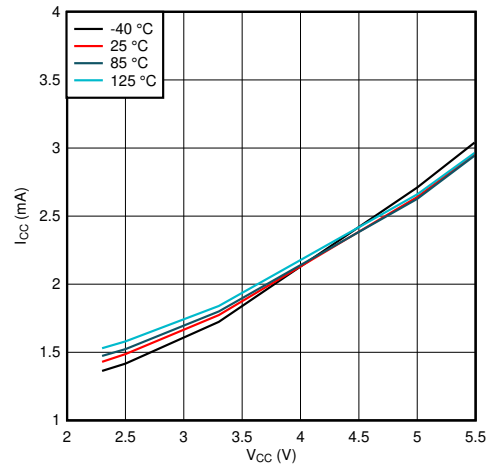


Figure 6-2.  $I_{CC}$  vs  $V_{CC}$

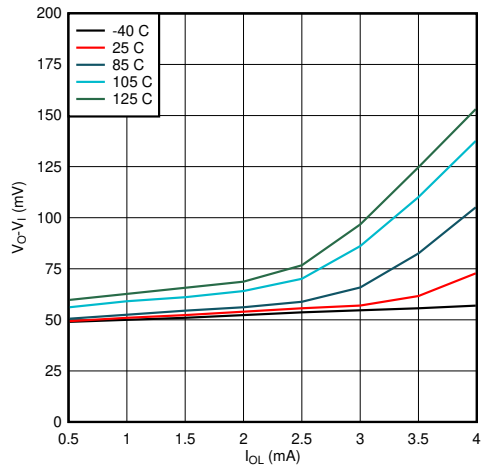


Figure 6-3.  $V_{OS}$  vs  $I_{OL}$  ( $V_{CC} = 2.3$  V,  $V_I = 0$  V)

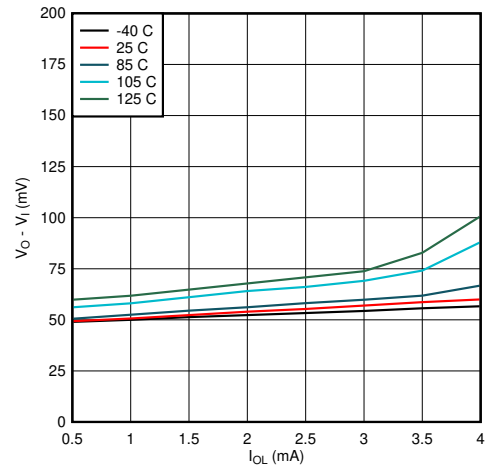


Figure 6-4.  $V_{OS}$  vs  $I_{OL}$  ( $V_{CC} = 3.3$  V,  $V_I = 0$  V)

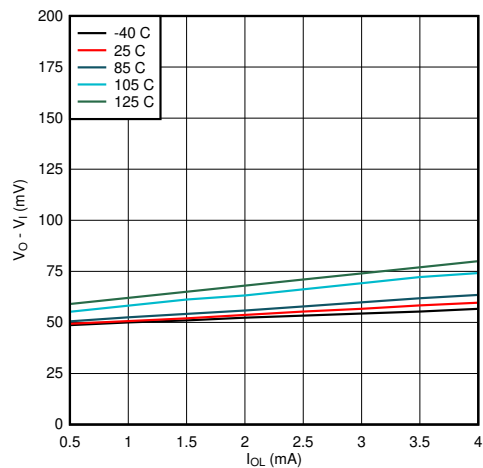
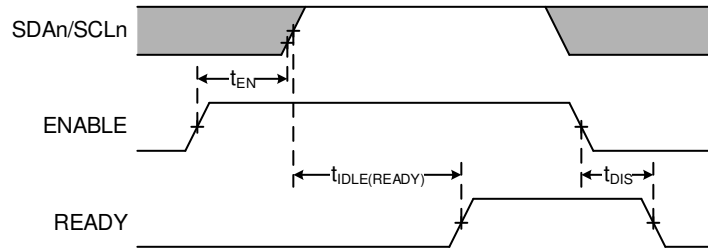
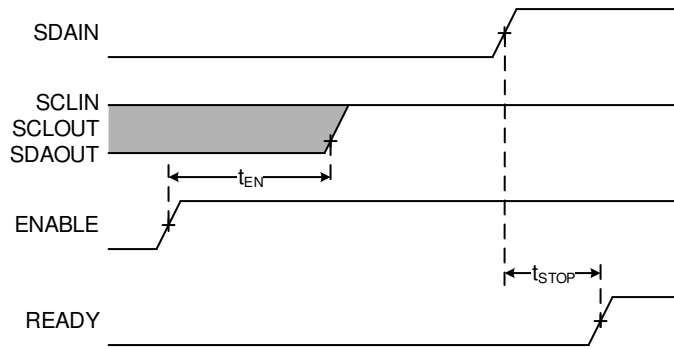


Figure 6-5.  $V_{OS}$  vs  $I_{OL}$  ( $V_{CC} = 5.5$  V,  $V_I = 0$  V)

## 7 Parameter Measurement Information



**Figure 7-1. Timing for  $t_{EN}$ ,  $t_{IDLE(READY)}$ , and  $t_{DIS}$**



**Figure 7-2. Timing for  $t_{STOP}$**



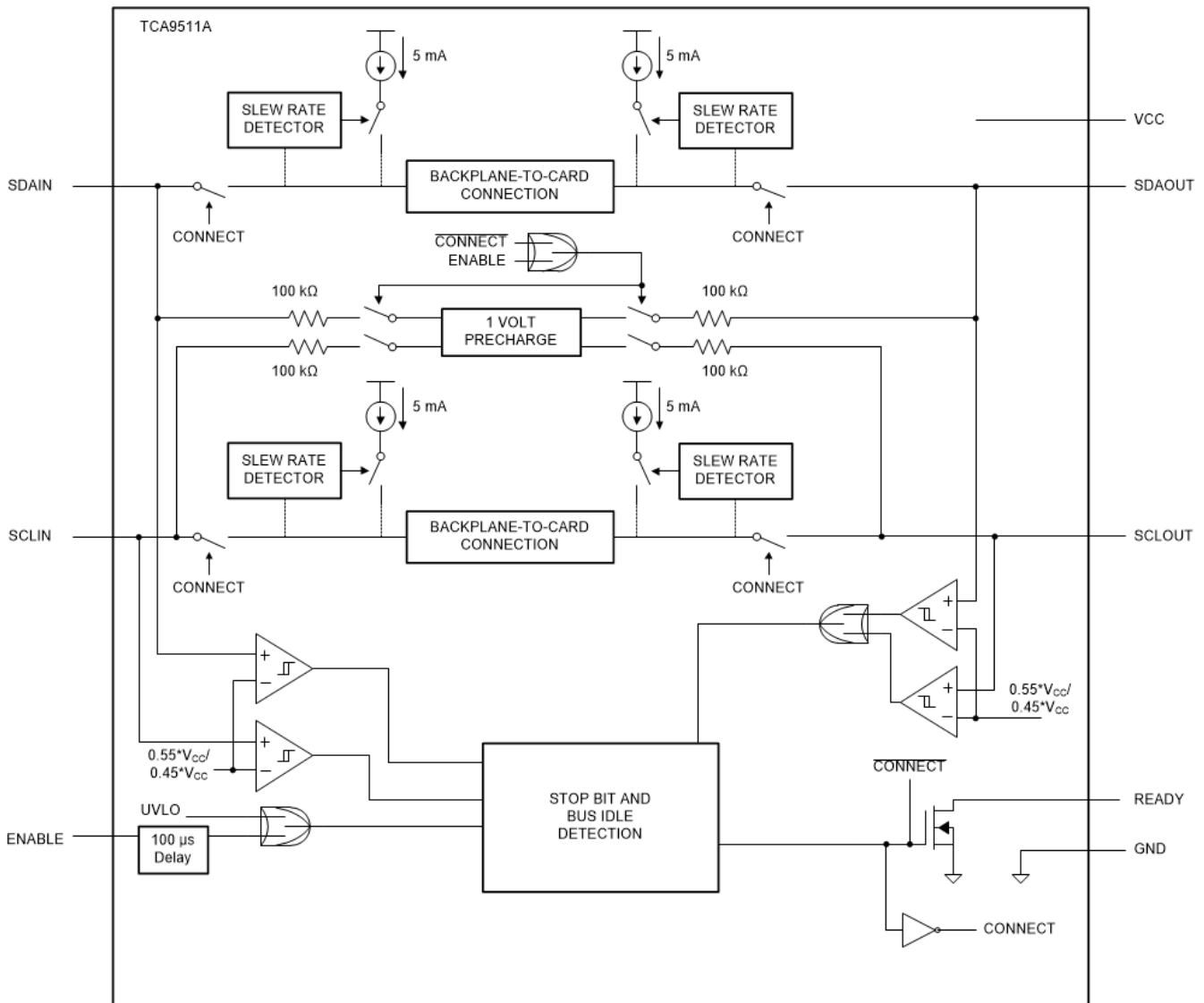
## 8 Detailed Description

### 8.1 Overview

The TCA9511A is a hot-swappable I<sup>2</sup>C bus buffer that supports I/O card insertion into a live backplane without corruption of the data and clock buses. Control circuitry prevents the backplane from being connected to the card until a stop command or bus idle condition occurs on the backplane without bus contention on the card. When the connection is made, this device provides bidirectional buffering, keeping the backplane and card capacitances isolated. During insertion, the SDA and SCL lines are pre-charged to 1 V to minimize the current required to charge the parasitic capacitance of the device.

When the I<sup>2</sup>C bus is idle, the TCA9511A is put into shutdown mode by setting the EN pin low. When EN is high, the TCA9511A resumes normal operation. It also includes an open drain READY output pin, which indicates that the backplane and card sides are connected together. When READY is high, the SDAIN and SCLIN are connected to SDAOUT and SCLOUT. When the two sides are disconnected, READY is low.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Hot bus insertion

During a hot bus insertion event, the TCA9511A keeps the buses disconnected to ensure that no data corruption occurs on either bus. Once the buses are idle or a stop bit on the IN side is detected, the TCA9511A connects the buses and READY goes high.

### 8.3.2 Pre-charge voltage

Both the SDA and SCL pins feature a 1-V pre-charge circuit through an internal 100 k $\Omega$  resistor prior to the pins being connected to an I<sup>2</sup>C bus. This feature helps minimize disruptions as a result of a hot bus insertion event.

### 8.3.3 Rise time accelerators

The TCA9511A features a rise time accelerator (RTA) on all I<sup>2</sup>C pins that during a positive bus transition, switches on a current source to quickly slew the bus pins high. This allows the use of weaker pull-up resistors, which can lower  $V_{OLs}$  and lower power system level power consumption.

### 8.3.4 Bus ready output indicator

The READY pin is an open drain output that provides an indicator to whether the buses are connected and ready for traffic. This pin is pulled low when the connection between IN/OUT is high impedance. Once the bus is idle or a stop condition on the IN side is detected, and the connection between IN/OUT is made, the READY pin is released and pulled high by an external pull-up resistor, signaling that it is ready for traffic.

### 8.3.5 Powered-off high impedance for I<sup>2</sup>C and I/O pins

When the supply voltage is below the UVLO threshold, the I<sup>2</sup>C and digital I/O pins are a high impedance state to prevent leakage currents from flowing through the device. When the EN pin is taken low, the device enters an isolation state, presenting a high impedance on all bus pins and pulling the READY pin low.

### 8.3.6 Supports clock stretching and arbitration

The TCA9511A supports full clock stretching, and arbitration without lock up.

## 8.4 Device Functional Modes

### 8.4.1 Start-up and precharge

When the TCA9511A first receives power on the VCC pin, either during power-up or during live insertion, it starts in an under voltage lockout (UVLO) state, ignoring any activity on the SDA and SCL pins until  $V_{CC}$  rises above UVLO.

Once the ENABLE pin goes high, the 'Stop Bit and Bus Idle' detect circuit is enabled and the device enters the bus idle state.

When  $V_{CC}$  rises above UVLO, the precharge circuitry will activate, which biases the bus pins on both sides to about 1 V through an internal 100 k $\Omega$  resistor.

### 8.4.2 Bus idle

After the Stop Bit and Bus Idle detect circuits are enabled the device enters the bus idle state. The pre-charge circuitry becomes active and forces 1 V through 100 k $\Omega$  nominal resistors to the SCL and SDA pins. The pre-charge circuitry minimizes the voltage differential seen by the SCL/SDA pins during a hot insertion event. This minimizes the amount of disturbance seen by the I/O card.

The device waits for the SDAIN and SCLIN pins to be high for the bus idle time or a STOP condition to be observed on the IN pins. The SDAOUT and SCLOUT pins must be high and the SDAIN and SCLIN pins must meet 1 of the 2 qualifiers (idle timer or a STOP condition) before connecting SDAIN to SDAOUT and SCLIN to SCLOUT. Once the bus connections have been made, the pre-charge circuitry is disabled and the device enters the bus active state.

### 8.4.3 Bus active

In the bus active mode, the I<sup>2</sup>C IN and OUT pins are connected, and the input is passed bi-directionally from IN/OUT side of the bus to the OUT/IN side respectively. The buses remain connected until the EN pin is taken low.

When the bus is connected, the driven-low side of the device is reflected on the opposite side, but with a small offset voltage. For example, if the input is pulled low to 100 mV, the output side will be pulled to roughly 150 mV. This offset allows the device to determine which side is currently being driven and avoid getting stuck low.

## 9 Application Information Disclaimer

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The typical application is to place the TCA9511A on the card that is being inserted or connected to a live bus, rather than being placed on the live bus. The reason for this is to provide maximum benefit by ensuring that the bus stays disconnected until an idle condition or stop condition is seen.

### 9.2 Typical Application

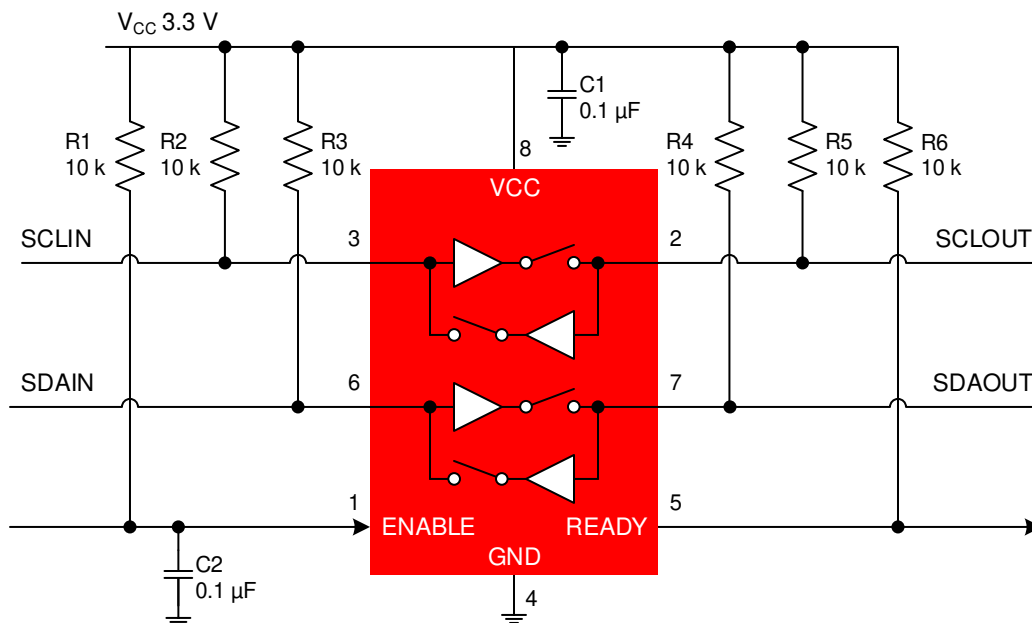


Figure 9-1. General Application Schematic

### 9.2.1 Design Requirements

#### 9.2.1.1 Series connections

It is possible to have multiple buffers in series, but care must be taken when designing a system.

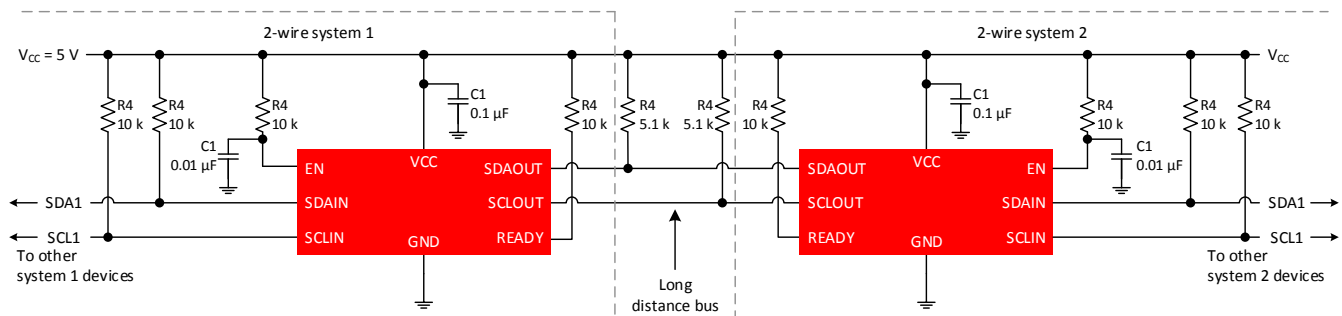


Figure 9-2. Series Buffer Connections

Each buffer adds approximately 60 mV of offset. Maximum offset ( $V_{\text{OFFSET}}$ ) should be considered. The low level at the signal origination end is dependent upon bus load. The I<sup>2</sup>C-bus specification requires that a 3 mA current produces no larger than a 0.4 V  $V_{\text{OL}}$ . As an example, if the  $V_{\text{OL}}$  at the master is 0.1 V, and there are 4 buffers in series (each adding about 60 mV), then the  $V_{\text{OL}}$  at the farthest buffer is approximately 0.34 V. This device has a rise time accelerator (RTA) that activates at 0.6 V. With great care, a system with 4 buffers may work, but as the  $V_{\text{OL}}$  moves up, it may be possible to trigger the RTA, creating a false edge on the clock.

It is recommended to limit the number of buffers in series to two, and to keep the load light to minimize the offset.

Another special consideration of series connections is the effect on round-trip-delay. This is the sum of propagation delays through the buffers and any effects on rise time. It is possible that fast mode speeds (400 kHz) are not possible due to delays and bus loading.

### 9.2.1.2 Multiple connections to a common node

It is possible to have multiple buffers in connect to a common node, but care must be taken when designing a system.

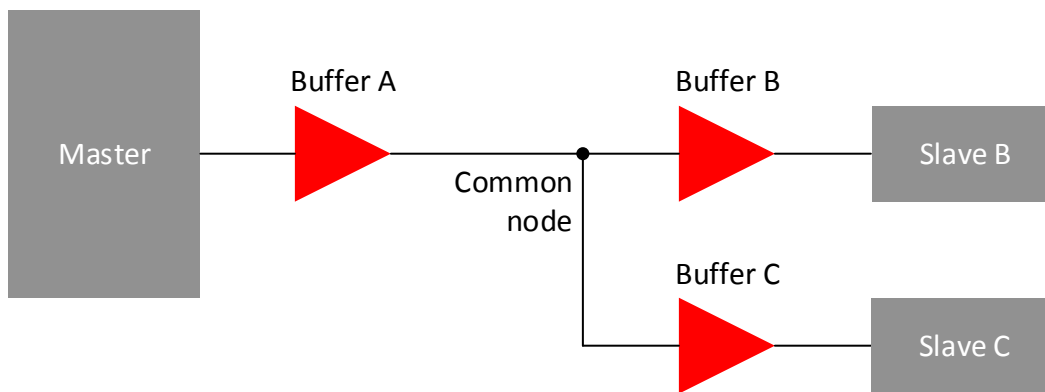


Figure 9-3. Connections to Common Node

It is important to try and avoid common node architectures. The multiple nodes sharing a common node can create glitches if the output voltage from a master slave device plus the offset voltage of the buffer are high enough to trip the RTA. Also keep in mind that the  $V_{\text{OS}}$  must be crossed in order for a device to begin to regulate the other side.

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of buffer A and buffer B in series as shown in Figure 9-3. Consider if the  $V_{\text{OL}}$  at the input of buffer A is 0.3 V and the  $V_{\text{OL}}$  of Slave B (when acknowledging) is 0.36 V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change the user should observe  $V_{\text{IL}}$  at the input of buffer A of 0.3 V and its output, the common node, is ~0.36 V. The output of buffer B and buffer C would be ~0.42 V, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of buffer C is ~0.52 V. When the Master pull-down turns off, the input of buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node rises to ~0.5 V before the buffer B output turns on, if the pull-up is strong the node may bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6 V, the accelerators on both buffer A and buffer C will fire, contending with the output of buffer B. The node on the input of buffer A goes high as will the input node of buffer C. After the common node voltage is stable for a while, the rising edge accelerators turn off, and the common node returns to ~0.5 V because the buffer B is still on. The voltage at both the Master and Slave C nodes then fall to ~0.6 V until Slave B turned off. This does not cause a failure on the data line as long as the return to 0.5 V on the common node (~0.56 V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on buffer A and buffer C would see a false clock rather than a stretched clock, which causes a system error.

### 9.2.1.3 Propagation delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same,

any difference in rise time is directly proportional to the difference in capacitance between the two sides. The  $t_{PLH}$  may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The  $t_{PHL}$  can never be negative because the output does not start to fall until the input is below  $0.7 \times V_{CC}$ , the output turn on has a non-zero delay, and the output has a limited maximum slew rate. Even if the input slew rate is slow enough that the output catches up, it would still lag the falling voltage of the input by the offset voltage. The maximum  $t_{PHL}$  occurs when the input is driven low with a very fast slew rate and the output is still limited by its turn-on delay and the falling edge slew rate.

### 9.2.2 Detailed Design Procedure

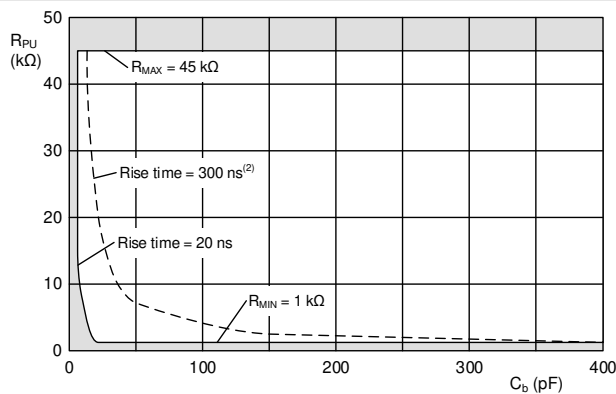
The system pull-up resistors must be strong enough to provide a positive slew rate of  $1.25 \text{ V}/\mu\text{s}$  on the SDA and SCL pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula given in Equation 1.

$$R \leq 800 \times 10^3 \left( \frac{V_{CC(MIN)} - 0.6}{C} \right) \quad (1)$$

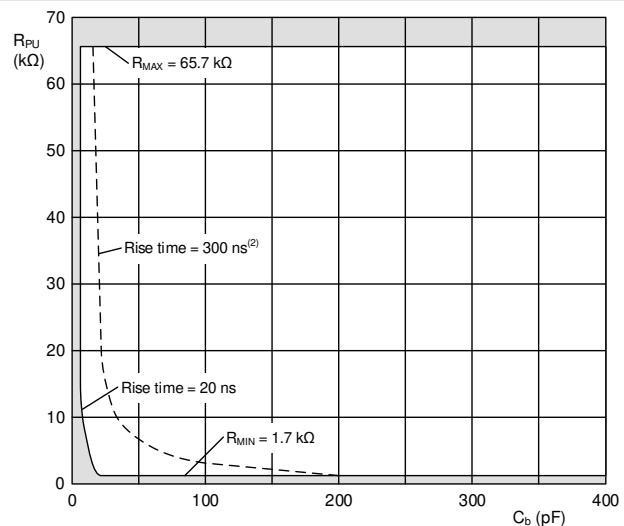
where  $R$  is the pull-up resistor value in  $\Omega$ ,  $V_{CC(MIN)}$  is the minimum  $V_{CC}$  voltage in volts, and  $C$  is the equivalent bus capacitance in picofarads (pF).

In addition, regardless of the bus capacitance, always choose  $R_{PU} \leq 65.7 \text{ k}\Omega$  for  $V_{CC} = 5.5 \text{ V}$ ,  $R_{PU} \leq 45 \text{ k}\Omega$  for  $V_{CC} = 3.3 \text{ V}$ , and  $R_{PU} \leq 33 \text{ k}\Omega$  for  $V_{CC} = 2.5 \text{ V}$ . The start-up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the pre-charge voltage.

### 9.2.3 Application Curves



**Figure 9-4. Example Bus Requirements for 3.3 V Systems**



**Figure 9-5. Example Bus Requirements for 5 V Systems**

### 9.3 Typical Application on a Backplane

As shown in Figure 9-6, the TCA9511A is used in a backplane connection. The TCA9511A is placed on the I/O peripheral card and connects the I<sup>2</sup>C devices on the card to the backplane safely upon a hot insertion event. Note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing a bus buffer on the edge of each card; however, isolates the card capacitance from the backplane. For a given I/O card, the TCA9511A drives the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.

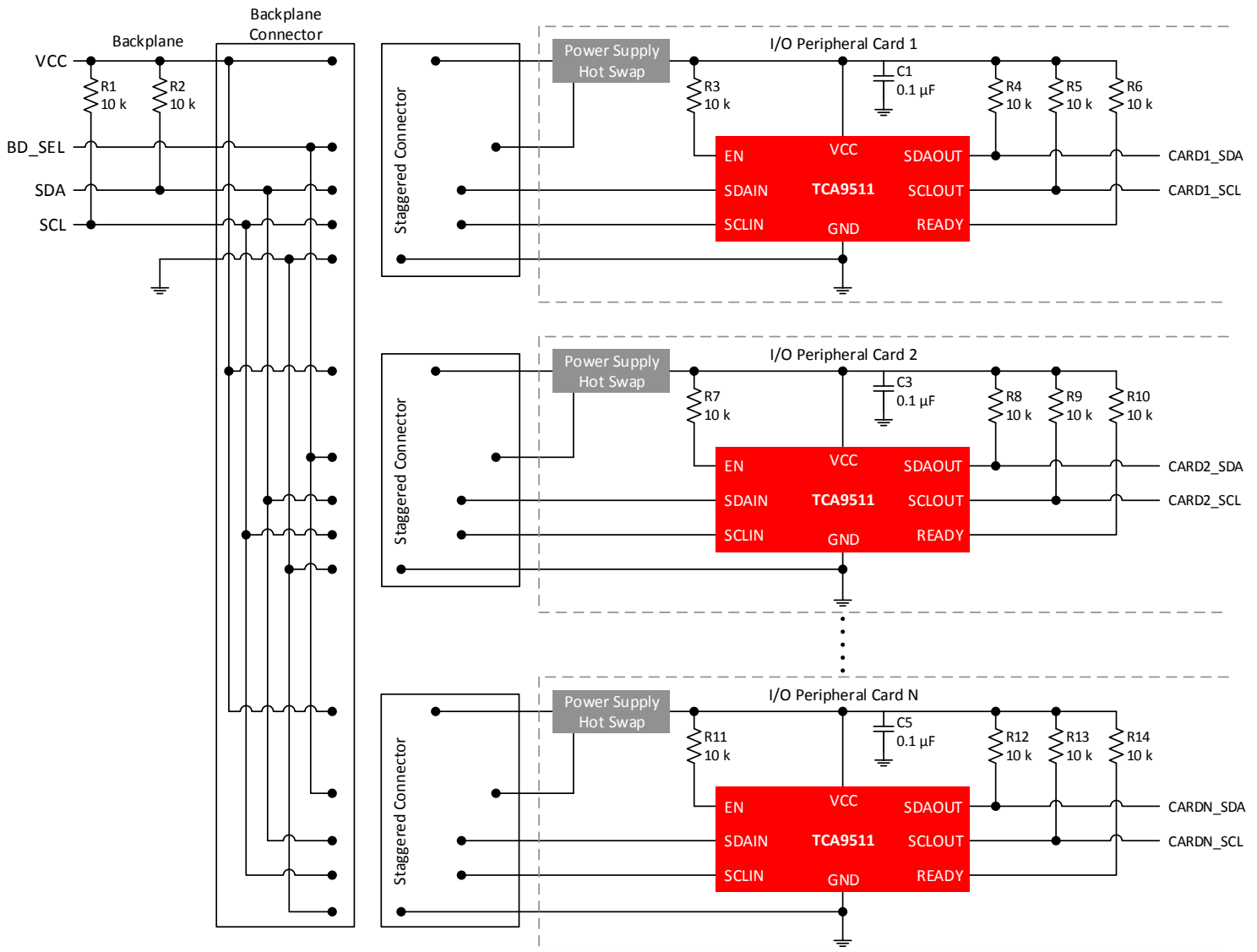


Figure 9-6. Backplane Application Schematic

#### 9.3.1 Design Requirements

There are a few considerations when using these hot swap buffers. It is NOT recommended to place the TCA9511A on the backplane connector as it cannot isolate the cards from one another which will possibly result in disturbing on-going I<sup>2</sup>C transactions. Instead, place the TCA9511A on the I/O peripheral card to maximize benefit.

#### 9.3.2 Detailed Design Procedure

The design procedure is the same as outlined in Section 9.2.2.

## 10 Power Supply Recommendations

### 10.1 Power Supply Best Practices

In order for the pre-charge circuitry to dampen the effect of hot-swap insertion of the TCA9511A into an active I<sup>2</sup>C bus, V<sub>CC</sub> must be applied before the SCL and SDA pins make contact to the main I<sup>2</sup>C bus. This is essential when the TCA9511A is placed on the add-on card circuit board, as in [Section 9.3](#). Although the pre-charge circuitry exists on both the -IN and -OUT side, the example in [Section 9.3](#) shows SCLIN and SDAIN connecting to the main bus. The supply voltage to VCC can be applied early by ensuring that the VCC and GND pin contacts are physically longer than the contacts for the SCLIN and SDAIN pins. If a voltage supervisor will also be used to control the voltage supply on the add-on card, additional delay will exist before the 1 V pre-charge voltage is present on the SCL and SDA pins.

### 10.2 Power-on Reset Requirements

In order to ensure that the part starts up in the correct state, it is recommended that the power supply ramp rates meet the below requirements.

**Table 10-1. Recommended supply ramp rates**

Parameter		MIN	MAX	UNIT
t <sub>RT</sub>	Rise rate	0.1	1000	ms
t <sub>FT</sub>	Fall rate	0.1	1000	ms



## 11 Layout

### 11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9511A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds. In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high frequency ripple. These capacitors should be placed as close to the TCA9511A as possible. These best practices are shown in [Section 11.2](#).

The layout example provided in [Section 11.2](#) shows a 4 layer board, which is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V<sub>CC</sub> or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, shown in the [Section 11.2](#) for the VCC side of the resistor connected to the EN pin; however, this routing and via is not necessary if V<sub>CC</sub> and GND are both full planes as opposed to the partial planes depicted.

## 11.2 Layout Example

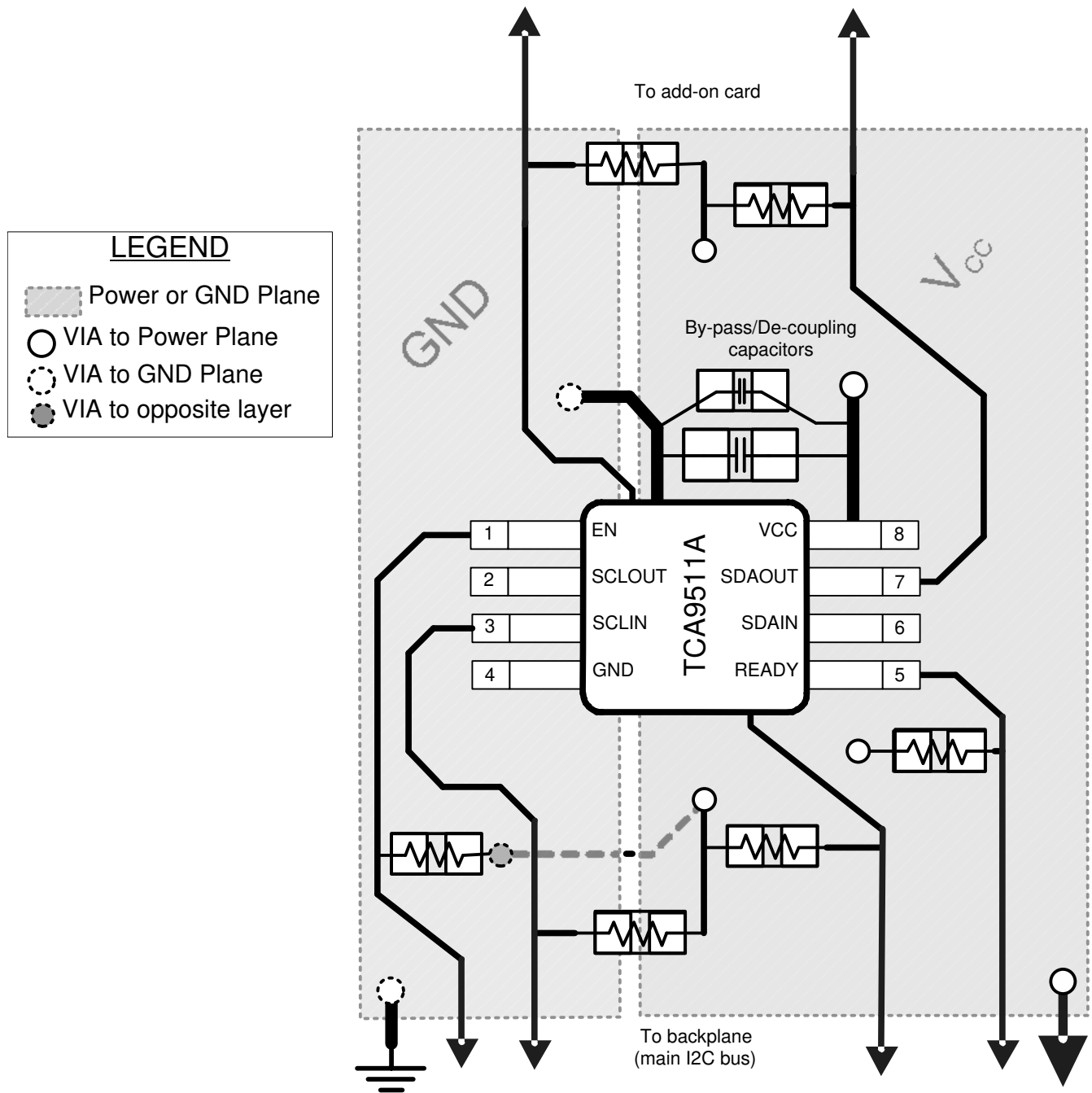


Figure 11-1. Layout example for TCA9511A

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.3 Trademarks

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### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9511ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG   SN	Level-1-260C-UNLIM	-40 to 125	9511A	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9511ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9511ADGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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