

# THVD1406, THVD1426 3.3-V to 5-V RS-485 Transceivers with Auto-direction Control and $\pm 12$ -kV IEC ESD Protection

## 1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard
- 3-V to 5.5-V Supply voltage
- Auto-direction control using the data input pin
- Half-duplex RS-422/RS-485
- Data rates
  - THVD1406: 500 kbps
  - THVD1426: 12 Mbps
- Bus I/O protection
  - $\pm 16$ -kV HBM ESD
  - $\pm 12$ -kV IEC 61000-4-2 Contact discharge
  - $\pm 15$ -kV IEC 61000-4-2 Air gap discharge
  - $\pm 4$ -kV IEC 61000-4-4 Fast transient burst
- $\pm 16$ -V bus fault protection
- Small, space-saving 8-Pin SOT package option (2.1 mm x 1.2 mm)
  - See the [layout example](#) for co-layout with standard SOIC-8 package
- Extended industrial temperature range:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Large receiver hysteresis for noise rejection
- Low power consumption
  - Low standby supply current:  $3\mu\text{A}$  (typ)
  - Quiescent current during operation:  $1.7\text{ mA}$  (typ)
- Glitch-free power-up, power-down for hot plug-in capability
- Open, short, and idle bus fail-safe
- 1/8 Unit load (Up to 256 bus nodes)

## 2 Applications

- [Factory automation and control](#)
- [Building automation](#)
- [HVAC systems](#)
- [Video surveillance](#)
- [Smart meters](#)

## 3 Description

The THVD14x6 (THVD1406 and THVD1426) devices are robust half-duplex RS-485 transceivers for industrial applications. These devices feature auto-direction control using the data input pin that reduces the reliance on separate pins for driver-enable and the receiver-enable functionality. This reduces the number of isolation channels needed or number of the GPIO pins needed for logic control. The bus pins are immune to high levels of IEC ESD events eliminating need of additional system level protection components.

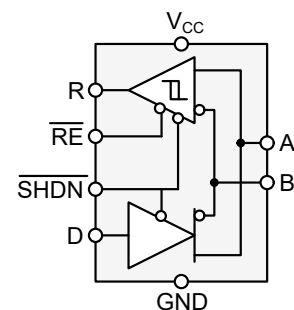
The devices operate from a single 3-V to 5.5-V supply. The wide common-mode voltage range and low input leakage on bus pins make devices suitable for multi-point applications over long cable runs.

The devices are available in industry standard 8-pin SOIC package for drop-in compatibility. The devices are also available in a small, space-saving SOT package. The devices are characterized for ambient temperatures from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
THVD1406	SOIC (8)	4.90 mm x 3.91 mm
THVD1426	SOT (8)	2.10 mm x 1.20 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Schematic**



## Table of Contents

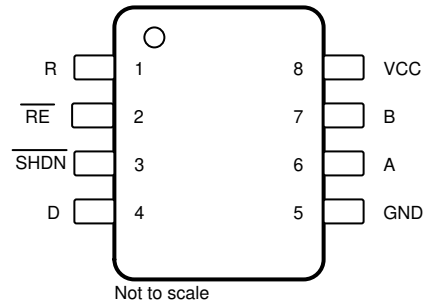
<b>1 Features</b> .....	1	8.2 Functional Block Diagrams.....	12
<b>2 Applications</b> .....	1	8.3 Feature Description.....	12
<b>3 Description</b> .....	1	8.4 Device Functional Modes.....	12
<b>4 Revision History</b> .....	2	<b>9 Application Information Disclaimer</b> .....	14
<b>5 Pin Configuration and Functions</b> .....	3	9.1 Application Information.....	14
<b>6 Specifications</b> .....	4	9.2 Typical Application.....	14
6.1 Absolute Maximum Ratings.....	4	<b>10 Power Supply Recommendations</b> .....	18
6.2 ESD Ratings.....	4	<b>11 Layout</b> .....	19
6.3 ESD Ratings - IEC Specifications.....	4	11.1 Layout Guidelines.....	19
6.4 Recommended Operating Conditions.....	4	11.2 Layout Example.....	19
6.5 Thermal Information.....	5	<b>12 Device and Documentation Support</b> .....	21
6.6 Power Dissipation Characteristics.....	5	12.1 Device Support.....	21
6.7 Electrical Characteristics.....	6	12.2 Receiving Notification of Documentation Updates..	21
6.8 Switching Characteristics (THVD1406).....	7	12.3 Support Resources.....	21
6.9 Switching Characteristics (THVD1426).....	7	12.4 Trademarks.....	21
6.10 Typical Characteristics.....	8	12.5 Electrostatic Discharge Caution.....	21
<b>7 Parameter Measurement Information</b> .....	10	12.6 Glossary.....	21
<b>8 Detailed Description</b> .....	12	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	21
8.1 Overview.....	12		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2021) to Revision A (November 2021)	Page
• Changed document status from <i>Advanced Information</i> to <i>Production</i> data .....	1

## 5 Pin Configuration and Functions



**Figure 5-1. D (8-Pin SOIC) , DRL (8-Pin SOT) Top View**

**Table 5-1. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
R	1	O	Receiver data output
$\overline{\text{RE}}$	2	I	Receiver enable, active low (internal 2-M $\Omega$ pull-up)
$\overline{\text{SHDN}}$	3	I	Shutdown enable, active low (internal 2-M $\Omega$ pull-up)
D	4	I	Driver data input
GND	5	-	Device ground
A	6	I/O	Bus I/O port, A (complementary to B)
B	7	I/O	Bus I/O port, B (complementary to A)
V <sub>CC</sub>	8	P	3-V to 5.5-V supply For the device.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
V <sub>L</sub>	Input voltage at any logic pin (D, SHDN or RE)	-0.3	5.7	V
V <sub>A</sub> , V <sub>B</sub>	Voltage at A or B inputs	-16	16	V
I <sub>O</sub>	Receiver output current	-24	24	mA
T <sub>J</sub>	Junction temperature		170	°C
T <sub>STG</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±16,000	V
		Between bus terminals (A, B) and GND		
		All other pins	±4,000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1,500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND	±12,000	V
		IEC 61000-4-2 ESD (Air-Gap Discharge), bus terminals and GND	±15,000	
		IEC 61000-4-4 EFT (Fast transient or burst), bus terminals and GND	±4,000	

### 6.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		3	5	5.5	V
V <sub>ID</sub>	Differential input voltage		-12		12	V
V <sub>I</sub>	Input voltage at any bus terminal <sup>(1)</sup>		-7		12	V
V <sub>IH</sub>	High-level input voltage (D, SHDN, and RE inputs)		2		5.5	V
V <sub>IL</sub>	Low-level input voltage (D, SHDN, and RE inputs)		0		0.8	V
I <sub>O</sub>	Output current	Driver	-60		60	mA
		Receiver	-8		8	
R <sub>L</sub>	Differential load resistance		54	60		Ω
1/t <sub>UI</sub>	Signaling rate: THVD1406				500	kbps
1/t <sub>UI</sub>	Signaling rate: THVD1426				12	Mbps
T <sub>J</sub>	Junction temperature		-40		150	°C
T <sub>A</sub> <sup>(2)</sup>	Operating ambient temperature		-40		125	°C
T <sub>SHDN</sub>	Thermal shutdown threshold (temperature rising)	Thermal shutdown threshold (temperature rising)	150	170		°C
T <sub>HYS</sub>	Thermal shutdown hysteresis	Thermal shutdown hysteresis		15		°C

- (1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

- (2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

## 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		THVD1406, THVD1426		UNIT
		DRL (SOT)	D (SOIC)	
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	112.2	126.0	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	28.4	66.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	22.1	69.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.2	18.7	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	22.0	68.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS		VALUE	UNIT	
P <sub>D</sub>	Power dissipation, driver and receiver enabled, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = 125°C, 50% duty cycle square-wave signal at maximum signaling rate	Unterminated R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 50 pF	THVD1406	500 kbps	150	mW
			THVD1426	12 Mbps	155	
		RS-422 load R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 50 pF	THVD1406	500 kbps	175	
			THVD1426	12 Mbps	180	
		RS-485 load R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF	THVD1406	500 kbps	220	
			THVD1426	12 Mbps	225	

## 6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT		
<b>Driver</b>									
V <sub>OD</sub>	Driver differential-output voltage magnitude	R <sub>L</sub> = 60 Ω, -7 V ≤ V <sub>test</sub> ≤ 12 V		See Figure 7-1	1.5	2	V		
		R <sub>L</sub> = 60 Ω, -7 V ≤ V <sub>test</sub> ≤ 12 V, 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V			2.1	3			
		R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 50 pF		See Figure 7-2	2	2.5			
		R <sub>L</sub> = 54 Ω, C <sub>L</sub> = 50 pF			1.5	2			
		R <sub>L</sub> = 54 Ω, 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V			2.1	3			
Δ V <sub>OD</sub>	Change in magnitude of driver differential-output voltage			-50		50	mV		
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage	R <sub>L</sub> = 54 Ω or 100 Ω, C <sub>L</sub> = 50 pF		See Figure 7-2	1	V <sub>CC</sub> / 2	3	V	
ΔV <sub>OC</sub>	Change in differential driver common-mode output voltage			-50		50	mV		
V <sub>OC(PP)</sub>	Peak-to-peak driver common-mode output voltage	R <sub>L</sub> = 54 Ω or 100 Ω, C <sub>L</sub> = 50 pF, V <sub>CC</sub> = 3.3 V		See Figure 7-2		200	mV		
I <sub>OS</sub>	Driver short-circuit output current	-7 V ≤ [V <sub>A</sub> or V <sub>B</sub> ] ≤ 12 V, or A pin shorted to B pin					-250	250	mA
<b>Receiver</b>									
I <sub>I</sub>	Bus input current (driver disabled)	V <sub>CC</sub> = 0 V or 5.5 V		V <sub>I</sub> = 12 V		75	100	μA	
				V <sub>I</sub> = -7 V		-97	-70		
V <sub>IT+</sub>	Positive-going receiver differential-input voltage threshold	-7 V ≤ V <sub>CM</sub> ≤ 12 V				-70	-45	mV	
V <sub>IT-</sub>	Negative-going receiver differential-input voltage threshold					-200	-150	mV	
V <sub>HYS</sub> <sup>(1)</sup>	Receiver differential-input voltage threshold hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )					30	50	mV	
V <sub>OH</sub>	Receiver high-level output voltage	I <sub>OH</sub> = -4 mA		V <sub>CC</sub> - 0.4	V <sub>CC</sub> - 0.2			V	
V <sub>OL</sub>	Receiver low-level output voltage	I <sub>OL</sub> = 4 mA				0.2	0.4	V	
I <sub>OZ</sub>	Receiver high-impedance output current	V <sub>O</sub> = 0 V or V <sub>CC</sub> , RE = V <sub>CC</sub>				-1	1	μA	
<b>Logic</b>									
I <sub>IN</sub>	Input current (D, SHDN, RE)					-5	5	μA	
<b>Supply</b>									
I <sub>CC</sub>	Supply current (quiescent)	V <sub>CC</sub> = 3.6 V	Driver and receiver enabled	SHDN = V <sub>CC</sub> , RE = 0, D = 0, no load		1500	1800	μA	
			Driver enabled, receiver disabled	SHDN = V <sub>CC</sub> , RE = V <sub>CC</sub> , D = 0, no load		1000	1500	μA	
			Driver and receiver disabled	SHDN = 0, no load		2	4.1	μA	
I <sub>CC</sub>	Supply current (quiescent)	V <sub>CC</sub> = 5.5 V	Driver and receiver enabled	SHDN = V <sub>CC</sub> , RE = 0, D = 0, no load		1700	3000	μA	
			Driver enabled, receiver disabled	SHDN = V <sub>CC</sub> , RE = V <sub>CC</sub> , D = 0, no load		1300	2500	μA	
			Driver and receiver disabled	SHDN = 0, no load		3	6.9	μA	

(1) Under any specific conditions, V<sub>IT+</sub> is specified to be at least V<sub>HYS</sub> higher than V<sub>IT-</sub>.

## 6.8 Switching Characteristics (THVD1406)

over operating free-air temperature range (unless otherwise noted)

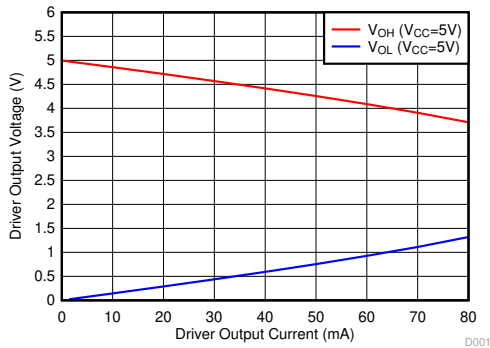
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>Driver</b>							
$t_r, t_f$	Driver differential output rise and fall times		See Figure 7-3	200	300	600	ns
$t_{PHL}, t_{PLH}$	Driver propagation delay				275	500	ns
$t_{SK(P)}$	Driver pulse skew, $ t_{PHL} - t_{PLH} $					10	ns
$t_{PHZ}, t_{PLZ}$	Driver disable time		See Figure 7-4 and Figure 7-5		80	200	ns
$t_{PZH}, t_{PZL}$	Driver enable time	Receiver enabled			200	650	ns
		Receiver disabled		5	10	$\mu$ s	
$t_{device\_auto-dir}$	Driver active time in the auto-direction mode when SHDN is high and D switches from low to high	Driver active time in the auto-direction mode when SHDN is high and D turns from low to high	Figure 7-8	4	8	14	$\mu$ s
<b>Receiver</b>							
$t_r, t_f$	Receiver output rise and fall times		See Figure 7-6		6	20	ns
$t_{PHL}, t_{PLH}$	Receiver propagation delay time				40	110	ns
$t_{SK(P)}$	Receiver pulse skew, $ t_{PHL} - t_{PLH} $					7	ns
$t_{PHZ}, t_{PLZ}$	Receiver disable time	See Figure 7-7			15	60	ns
$t_{PZL(1)}, t_{PZH(1)}$	Receiver enable time	Driver enabled	See Figure 7-7		80	150	ns

## 6.9 Switching Characteristics (THVD1426)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>Driver</b>							
$t_r, t_f$	Driver differential output rise and fall times		See Figure 7-3		8	25	ns
$t_{PHL}, t_{PLH}$	Driver propagation delay				17	35	ns
$t_{SK(P)}$	Driver pulse skew, $ t_{PHL} - t_{PLH} $					3.5	ns
$t_{PHZ}, t_{PLZ}$	Driver disable time		See Figure 7-4 and Figure 7-5		15	38	ns
$t_{PZH}, t_{PZL}$	Driver enable time	Receiver enabled			15	70	ns
		Receiver disabled		5	10	$\mu$ s	
$t_{device\_auto-dir}$	Driver active time in the auto-direction mode when SHDN is high and D turns from low to high	Driver active time in the auto-direction mode when SHDN is high and D switches from low to high	Figure 7-8	0.4	0.8	1.45	$\mu$ s
<b>Receiver</b>							
$t_r, t_f$	Receiver output rise and fall times		See Figure 7-6		4	16	ns
$t_{PHL}, t_{PLH}$	Receiver propagation delay time				40	75	ns
$t_{SK(P)}$	Receiver pulse skew, $ t_{PHL} - t_{PLH} $					5	ns
$t_{PHZ}, t_{PLZ}$	Receiver disable time	See Figure 7-7			15	25	ns
$t_{PZL(1)}, t_{PZH(1)}$	Receiver enable time	Driver enabled	See Figure 7-7		80	170	ns

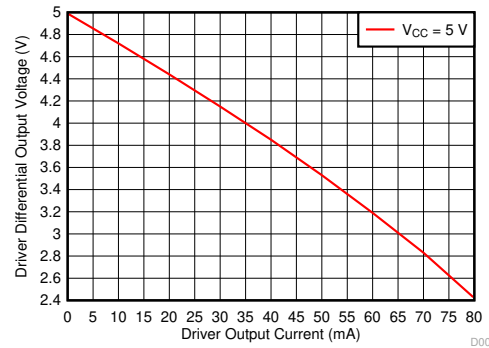
## 6.10 Typical Characteristics



D001\_driver\_vout\_iout.grf

DE = V<sub>CC</sub>      T<sub>A</sub> = 25°C

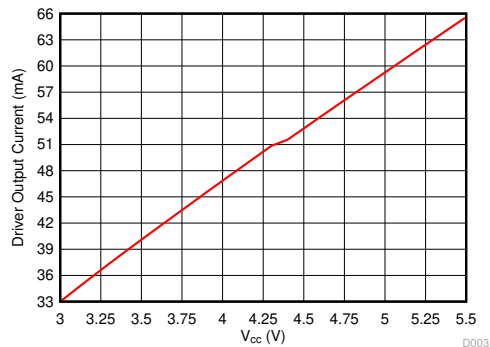
**Figure 6-1. Driver Output voltage vs Driver Output Current**



D002\_driver\_vdiff.grf

D = 0 V      DE = V<sub>CC</sub>      T<sub>A</sub> = 25°C

**Figure 6-2. Driver Differential Output voltage vs Driver Output Current**

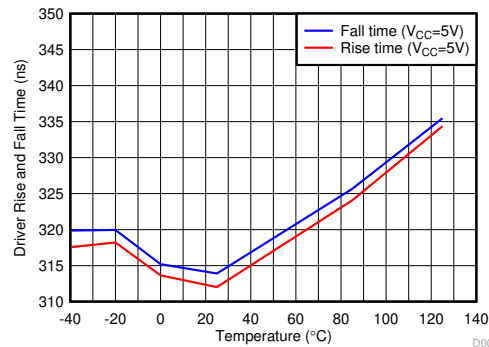


D003

D003\_iout\_vcc.grf

R<sub>L</sub> = 54 Ω      DE = V<sub>CC</sub>      D = V<sub>CC</sub>  
T<sub>A</sub> = 25°C

**Figure 6-3. Driver Output Current vs Supply Voltage**

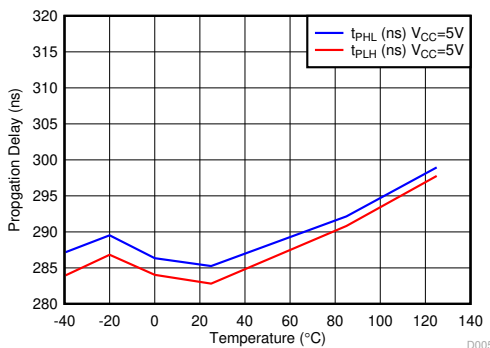


D004

D004\_rise\_fall.grf

R<sub>L</sub> = 54 Ω      C<sub>L</sub> = 50 pF

**Figure 6-4. Driver Rise or Fall Time vs Temperature (THVD1406)**

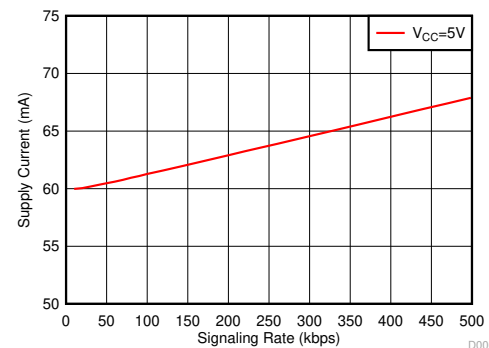


D005

D005\_prop\_delay.grf

R<sub>L</sub> = 54 Ω      C<sub>L</sub> = 50 pF

**Figure 6-5. Driver Propagation Delay vs Temperature (THVD1406)**



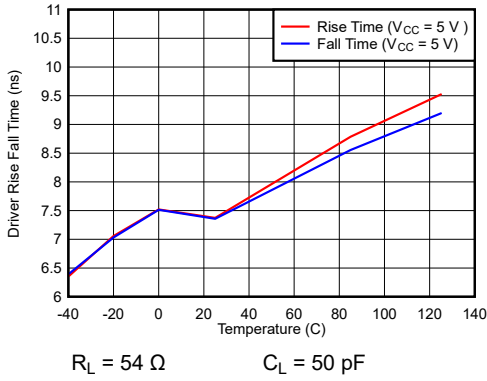
D006

D006\_icc\_datarate.grf

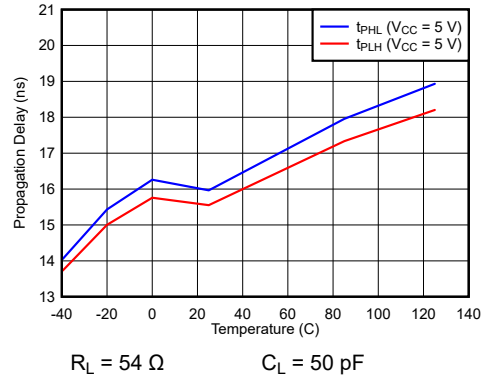
R<sub>L</sub> = 54 Ω      T<sub>A</sub> = 25°C

**Figure 6-6. Supply Current vs Signal Rate (THVD1406)**

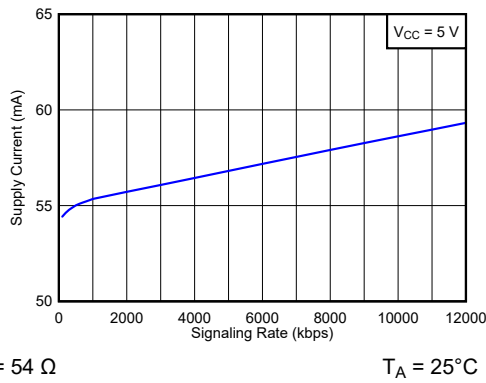




**Figure 6-7. Driver Rise or Fall Time vs Temperature (THVD1426)**



**Figure 6-8. Driver Propagation Delay vs Temperature (THVD1426)**



**Figure 6-9. Supply Current vs Signal Rate (THVD1426)**

## 7 Parameter Measurement Information

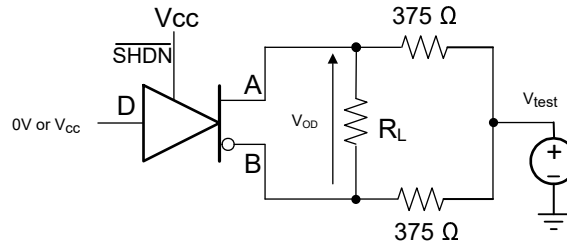


Figure 7-1. Measurement of Driver Differential Output Voltage With Common-Mode Load



Figure 7-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

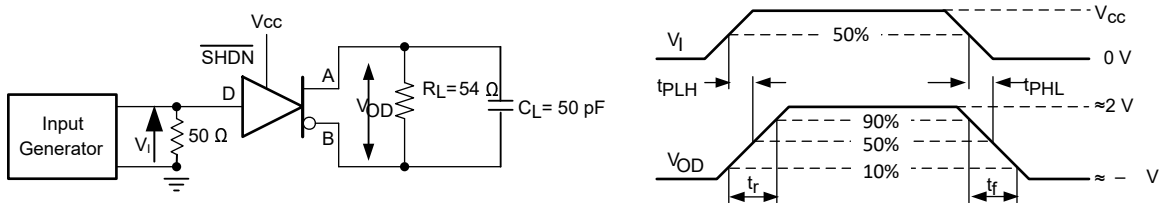


Figure 7-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

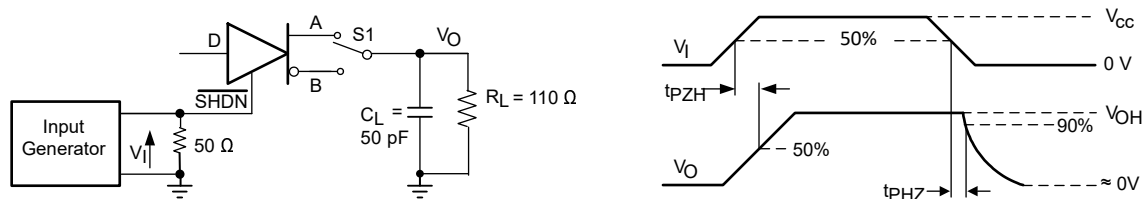


Figure 7-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

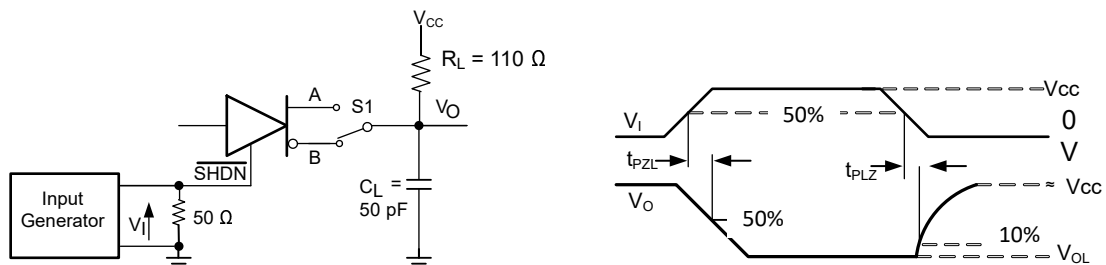
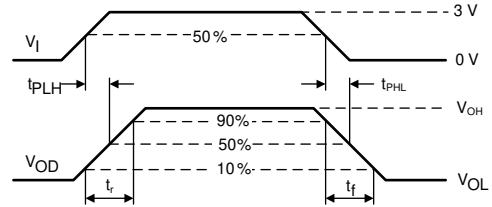
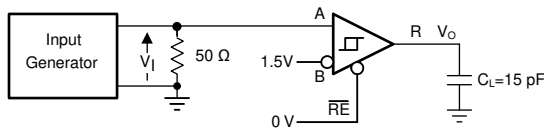
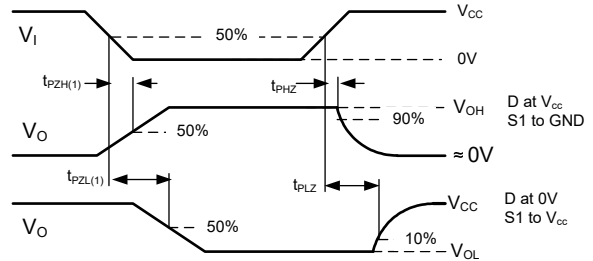
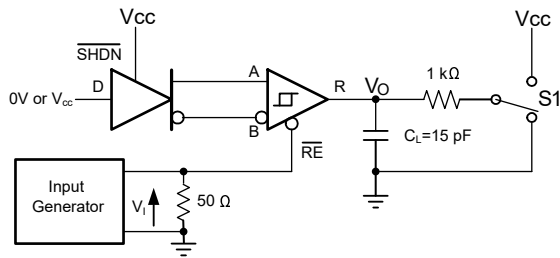


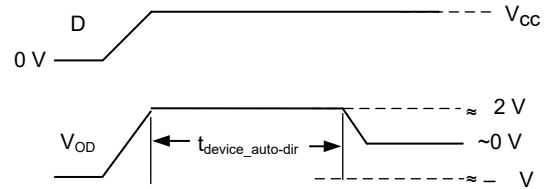
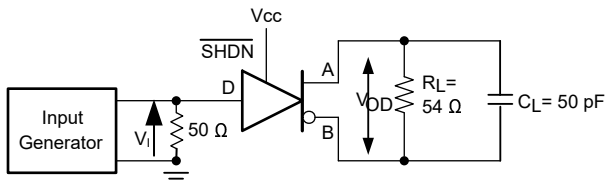
Figure 7-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load



**Figure 7-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays**



**Figure 7-7. Measurement of Receiver Enable/Disable Times With Driver Enabled**



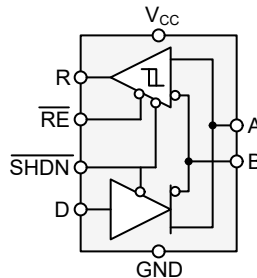
**Figure 7-8. Measurement of Auto-direction Control Timing Parameter ( $t_{\text{device\_auto-dir}}$ )**

## 8 Detailed Description

### 8.1 Overview

The THVD1406 is a low-power, half-duplex RS-485 transceiver suitable for data transmission up to 500 kbps. The THVD1426 is a low-power, half-duplex RS-485 transceiver suitable for data transmission up to 12 Mbps.

### 8.2 Functional Block Diagrams



### 8.3 Feature Description

Internal ESD protection circuits protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to  $\pm 12$  kV (Contact Discharge),  $\pm 15$  kV (Air Gap Discharge) and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to  $\pm 4$  kV.

### 8.4 Device Functional Modes

When the shutdown pin,  $\overline{\text{SHDN}}$ , is logic high, the differential outputs A and B follow the logic states at data input D. When D is low, the output states reverse, B turns high, A becomes low, and  $V_{OD}$  is negative. A logic high at D causes A to turn high and B to turn low for a duration. In this case, the differential output voltage defined as  $V_{OD} = V_A - V_B$  is positive for  $t_{\text{device-auto-dir}}$ . After this duration, the driver turns off and the receiver is enabled. The device can be used in auto-direction mode by tying  $\overline{\text{SHDN}}$  and  $\overline{\text{RE}}$  pins together to logic high and controlling the driver and receiver using the data input pin, D. This enables reducing the number of GPIO pins or the number of isolation channels required to operate the device. Please refer to [Driver Function Table](#) and [Receiver Function Table](#) for further details.

When  $\overline{\text{SHDN}}$  is low, both the driver and the receiver are turned off and the device is in shutdown mode. In this condition, the logic state at D is irrelevant. The  $\overline{\text{SHDN}}$  pin has an internal pull-up resistor to  $V_{CC}$ ; thus, when left open, the driver status is dependent on the status of the D pin. The D pin has an internal pull-up resistor to  $V_{CC}$ , thus, when left open while the driver is enabled for  $t_{\text{device-auto-dir}}$ , before being disabled.

**Table 8-1. Driver Function Table**

INPUT D	ENABLE SHDN	OUTPUTS		FUNCTION
		A	B	
H	H/OPEN	H	L	Actively drive bus high for $t_{\text{device-auto-dir}}$ and then bus is in high impedance
L	H/OPEN	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled. Device in shutdown mode.
OPEN	H/OPEN	H	L	Actively drive bus high for $t_{\text{device-auto-dir}}$ and then bus is in high impedance

When the receiver enable pin,  $\overline{\text{RE}}$ , is logic low, the receiver is enabled. When the differential input voltage defined as  $V_{ID} = V_A - V_B$  is positive and higher than the positive input threshold,  $V_{IT+}$ , the receiver output, R, turns high. When  $V_{ID}$  is negative and lower than the negative input threshold,  $V_{IT-}$ , the receiver output, R, turns low. If  $V_{ID}$  is between  $V_{IT+}$  and  $V_{IT-}$  the output is indeterminate.

When  $\overline{\text{RE}}$  is logic high or left open and D input is logic low, the receiver output is high-impedance and the magnitude and polarity of  $V_{ID}$  are irrelevant. Internal biasing of the receiver inputs causes the output to go

failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

When  $\overline{RE}$  is logic high or left open and D input switches from logic low to logic high, the receiver output is high-impedance for the duration of  $t_{\text{device-auto-dir}}$ . After the duration of  $t_{\text{device-auto-dir}}$ , the receiver turns ON and outputs a logic high or low depending upon the differential bus input voltage.

**Table 8-2. Receiver Function Table**

DIFFERENTIAL INPUT	ENABLE	INPUT	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	D	R	
$V_{IT+} < V_{ID}$	L	X	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	X	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	X	L	Receive valid bus low
X	H/OPEN	L	Z	Receiver disabled
X	H/OPEN	H	Z for $t_{\text{device\_autodir}}$ followed by L or H depending upon bus input voltage	Receiver disabled by for $t_{\text{device\_autodir}}$ after D switches from L to H. Receiver output follows bus input voltage after $t_{\text{device\_autodir}}$
Open-circuit bus	L	X	H	Fail-safe high output
Short-circuit bus	L	X	H	Fail-safe high output
Idle (terminated) bus	L	X	H	Fail-safe high output

## 9 Application Information Disclaimer

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The THVD14x6 devices are half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. The device can be used in auto-direction mode by tying  $\overline{\text{SHDN}}$  and  $\overline{\text{RE}}$  pins together to logic high and controlling the driver and receiver using the data input pin, D. This enables reducing the number of GPIO pins or the number of isolation channels required to operate the device. Please refer to [Driver Function Table](#) and [Receiver Function Table](#) for further details.

### 9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor,  $R_T$ , whose value matches the characteristic impedance,  $Z_0$ , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

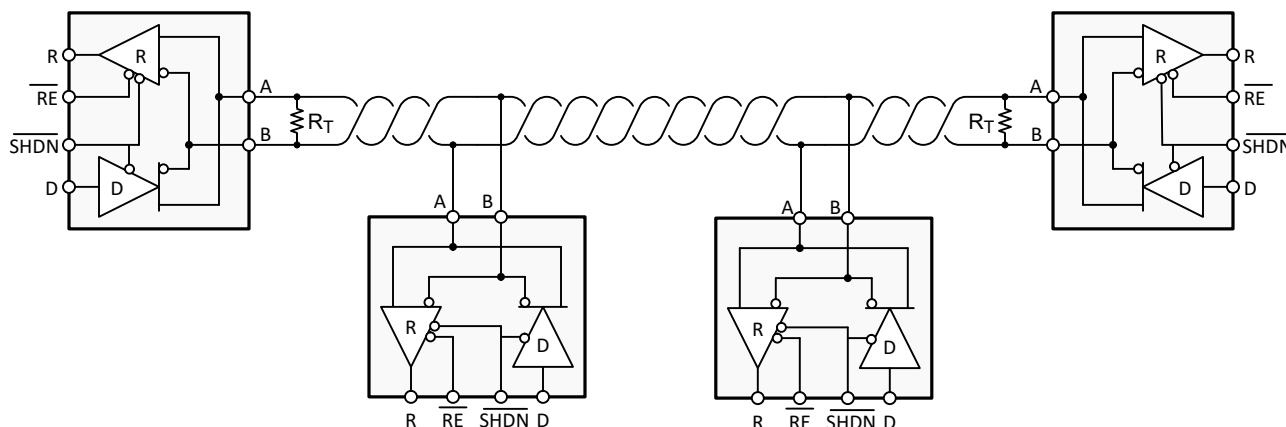


Figure 9-1. Typical RS-485 Network With Half-Duplex Transceivers

#### 9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

##### 9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 300 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

### 9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in [Equation 1](#).

$$L_{(\text{STUB})} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- $t_r$  is the 10/90 rise time of the driver
- $c$  is the speed of light ( $3 \times 10^8$  m/s)
- $v$  is the signal velocity of the cable or trace as a factor of  $c$

### 9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 k $\Omega$ . Because the THVD14x6 devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

### 9.2.1.4 Receiver Failsafe

The differential receivers of the THVD14x6 are *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input  $V_{ID}$  is more positive than 200 mV, and must output a low when  $V_{ID}$  is more negative than  $-200$  mV. The receiver parameters which determine the failsafe performance are  $V_{IT+}$ ,  $V_{IT-}$ , and  $V_{HYS}$  (the separation between  $V_{IT+}$  and  $V_{IT-}$ ). As shown in the [Electrical Characteristics](#) table, differential signals more negative than  $-200$  mV always causes a low receiver output, and differential signals more positive than 200 mV always causes a high receiver output.

When the differential input signal is close to zero, it is still above the  $V_{IT+}$  threshold, and the receiver output is high. Only when the differential input is more than  $V_{HYS}$  below  $V_{IT+}$  does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value,  $V_{HYS}$ , as well as the value of  $V_{IT+}$ .

### 9.2.1.5 Transient Protection

The bus pins of the THVD14x6 transceiver family include on-chip ESD protection against ±16-kV HBM and ±8-kV IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance,  $C_{(S)}$ , and 78% lower discharge resistance,  $R_{(D)}$ , of the IEC model produce significantly higher discharge currents than the HBM model.

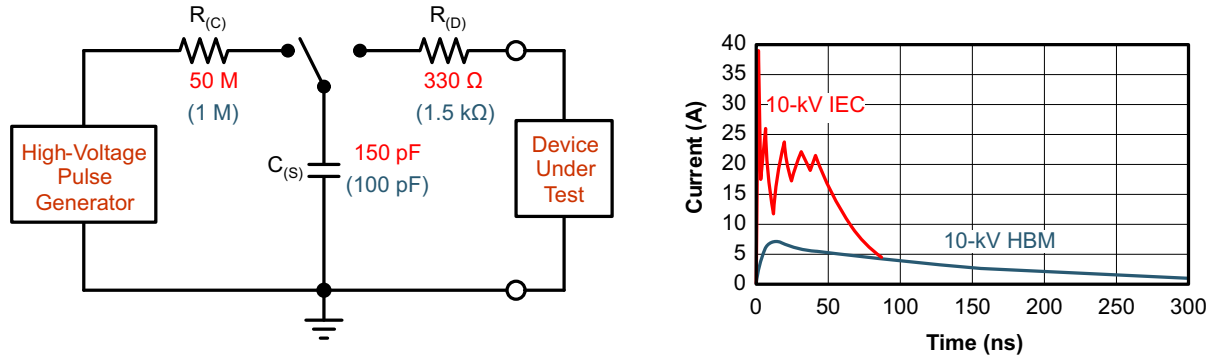


Figure 9-2. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 9-3 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

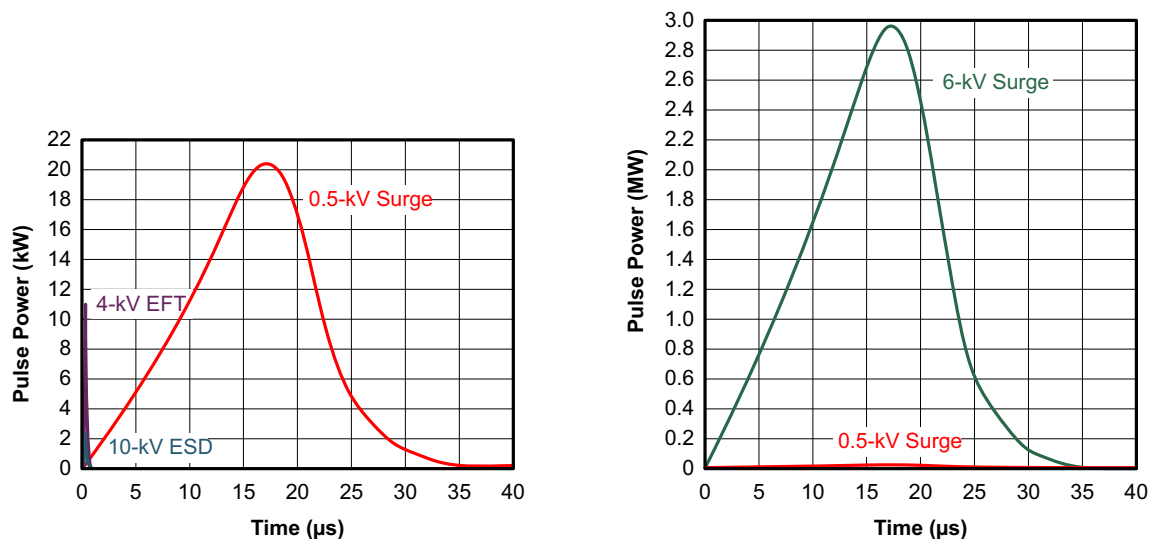
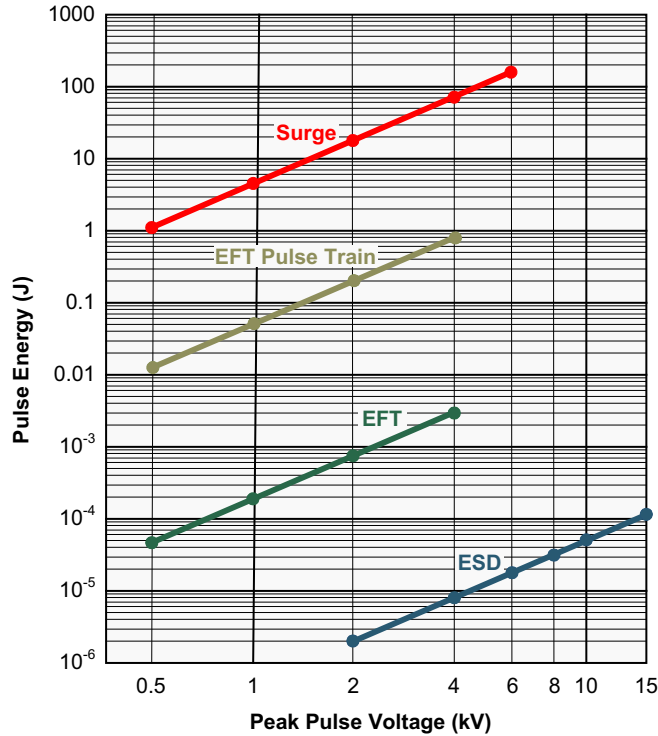


Figure 9-3. Power Comparison of ESD, EFT, and Surge Transients



In the event of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. Figure 9-4 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.



**Figure 9-4. Comparison of Transient Energies**



## 11 Layout

### 11.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use  $V_{CC}$  and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF decoupling capacitors as close as possible to the  $V_{CC}$  pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for  $V_{CC}$  and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1-k $\Omega$  to 10-k $\Omega$  pull-up resistors for  $\overline{RE}$  and  $\overline{SHDN}$  lines to connect them together to  $V_{CC}$  to reduce the number of GPIO lines to MCU or the number of isolation channels.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

### 11.2 Layout Example

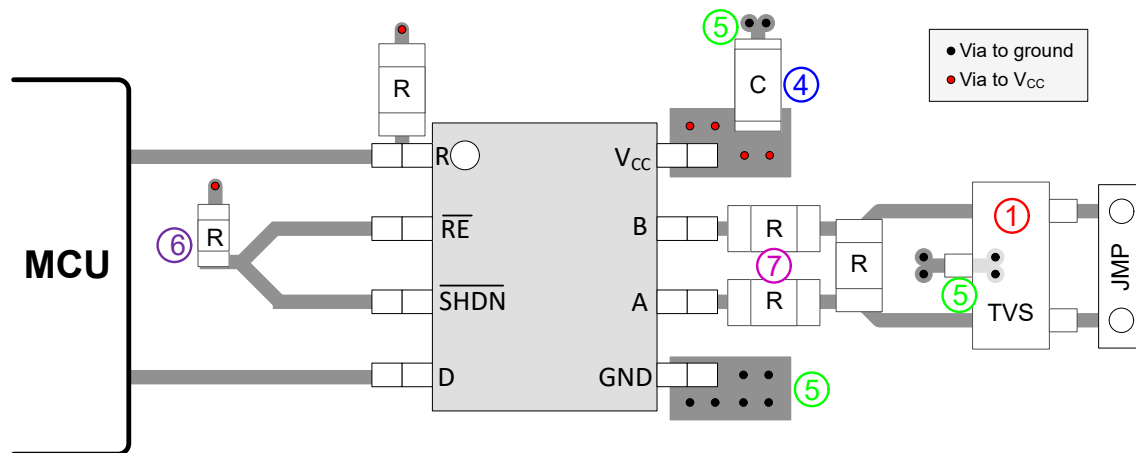


Figure 11-1. Layout Example

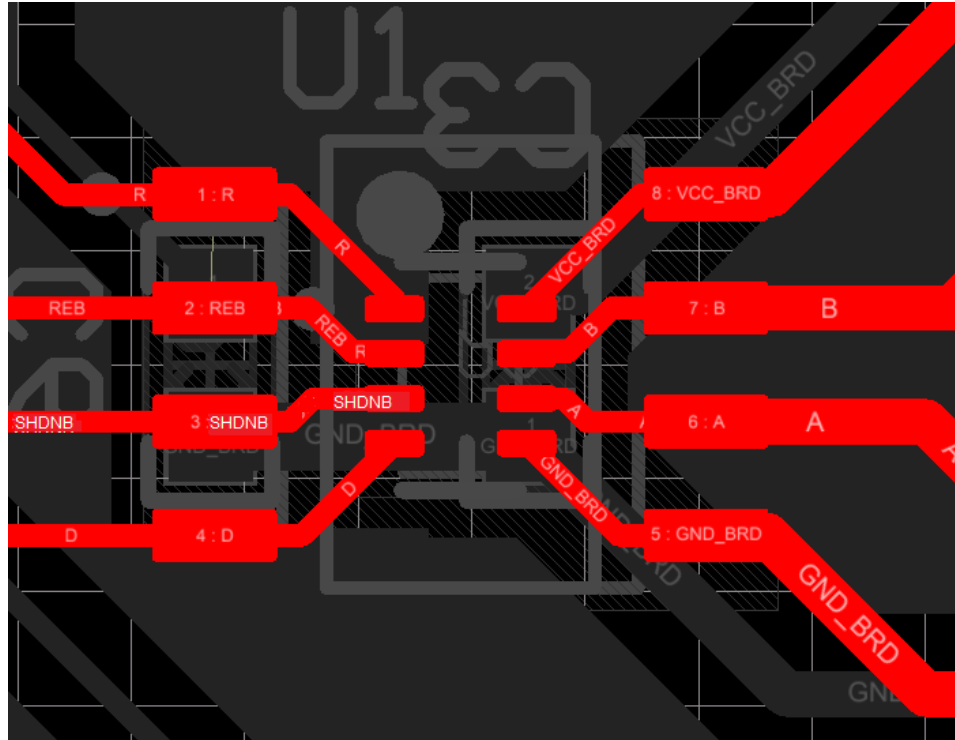


Figure 11-2. Layout Example for Co-layout of SOIC (D) and SOT (DRL) Packages

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

#### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

#### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THVD1406DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1406	<a href="#">Samples</a>
THVD1406DRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI   SN	Level-1-260C-UNLIM	-40 to 125	T406	<a href="#">Samples</a>
THVD1426DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1426	<a href="#">Samples</a>
THVD1426DRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI   SN	Level-1-260C-UNLIM	-40 to 125	T426	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1406DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1406DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
THVD1426DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THVD1426DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1406DR	SOIC	D	8	3000	356.0	356.0	35.0
THVD1406DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
THVD1426DR	SOIC	D	8	3000	356.0	356.0	35.0
THVD1426DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

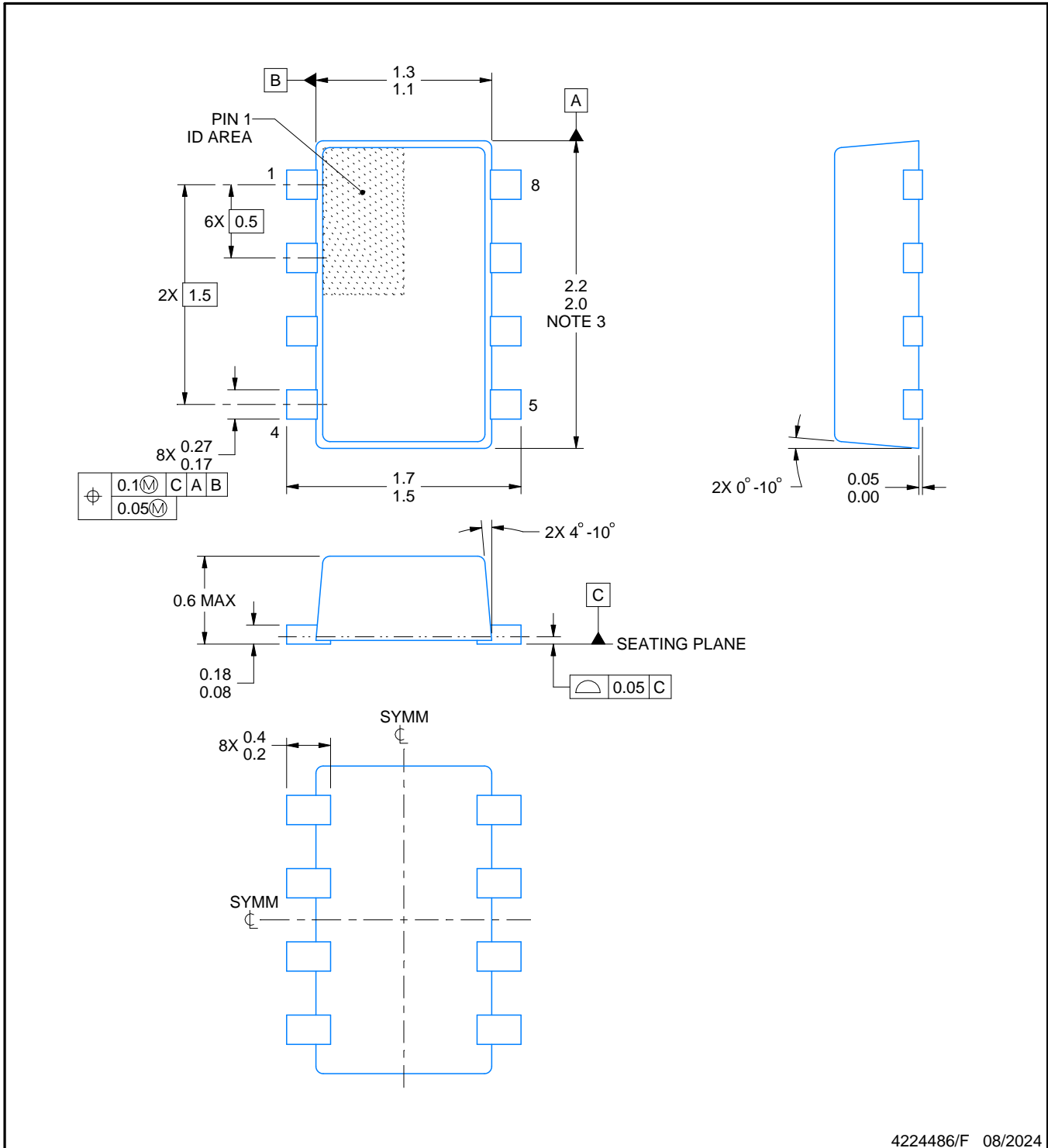


SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4224486/F 08/2024

NOTES:

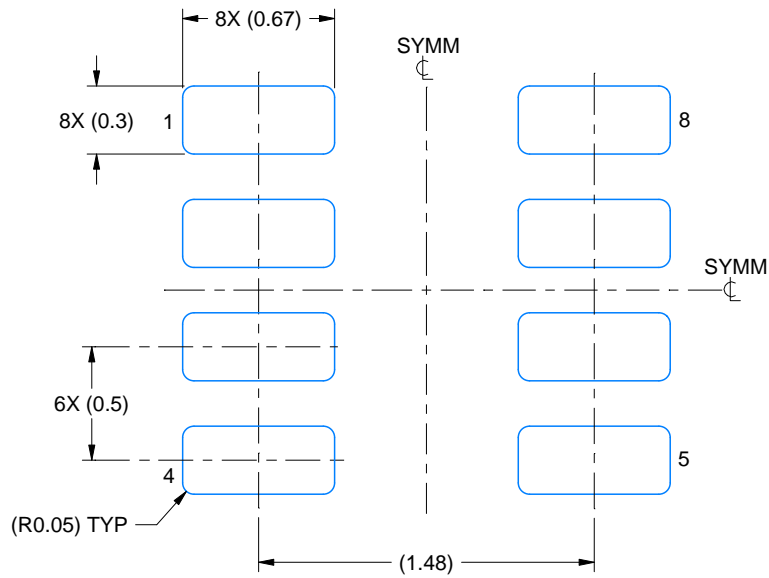
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

# EXAMPLE BOARD LAYOUT

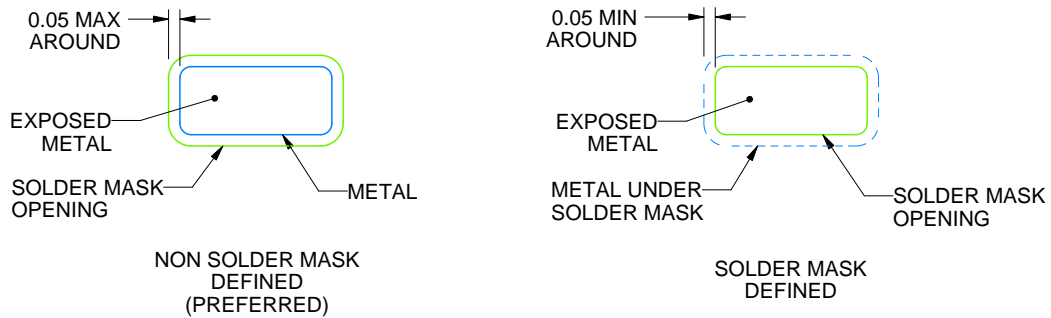
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:30X



SOLDERMASK DETAILS

4224486/F 08/2024

NOTES: (continued)

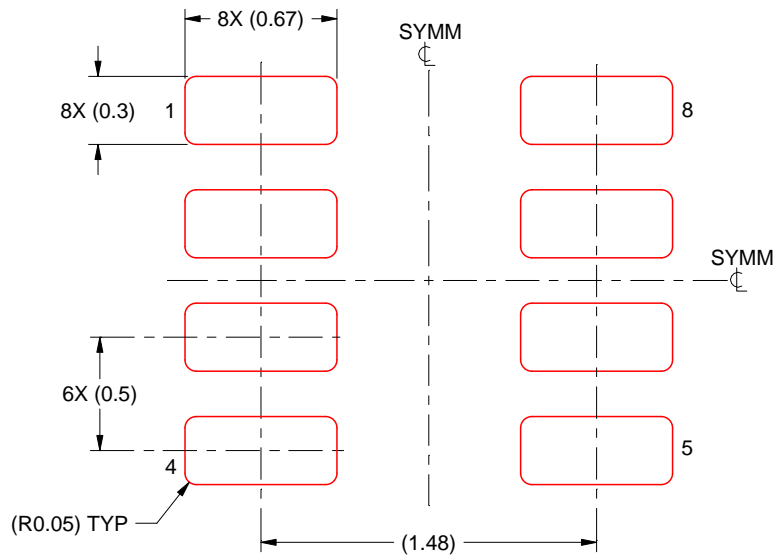
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4224486/F 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated