TEXAS INSTRUMENTS
TPS1685
SLVSHA1 – SEPTEMBER 2024

TPS1685x 9V–80V, 3.65mΩ, 20A Stackable Integrated Hotswap (eFuse) With Accurate and Fast Current Monitor

1 Features

- Input operating voltage range: 9V to 80V
  - 92V absolute maximum
  - Withstands negative voltages up to –5V at output
- Integrated FET with low on-resistance: R_{ON} = 3.65mΩ (typ)
- Active high enable input with adjustable undervoltage lockout (UVLO)
- Adjustable overvoltage protection
- Supports parallel connection of multiple eFuses with device state synchronization and load sharing during start-up and steady state
- Adjustable output slew rate control (dVdt) for inrush current protection
- Precise load current monitoring
  - <3% error for over 50-100% of max current
  - 1MHz bandwidth
- Robust overcurrent protection
  - Circuit-breaker response
  - Adjustable threshold: 2A to 20A
  - Overcurrent protection accuracy: ±3%
  - Adjustable transient overcurrent timer (ITIMER) to support peak currents
- Fast-trip response to short-circuit events
- Overtemperature protection (OTP) with analog die temperature monitor output (TEMP)
- FET health monitoring and reporting
- Fault indication pin ($\overline{FLT}$)
- Power Good indication pin (PGOOD)
- Small footprint: QFN 6mm × 5mm
  - IPC9592B clearance for 60V

2 Applications

- Input hotswap and hotplug
- Server and high performance computing
- Network interface cards
- Graphics and hardware accelerator cards
- Data center switches and routers
- Fire alarm control panel

3 Description

The TPS1685x is an integrated high current circuit protection and power management device. The device provides multiple protection modes using very few external components and is a robust defense against overloads, short-circuits and excessive inrush current. Applications with particular inrush current requirements can set the output slew rate with a single external capacitor. Output current limit level can be set by user as per system needs. A user adjustable overcurrent blanking timer allows systems to support transient peaks in the load current without tripping the eFuse. An integrated fast and accurate sense analog load current monitor facilitates predictive maintenance and advanced dynamic platform power management such as Intel® PSYS and PROCHOT to optimize server and data-center performance.

Multiple TPS1685x devices can be connected in parallel to increase the total current capacity for high power systems. All devices actively synchronize their operating state and share current during start-up as well as steady state to avoid over-stressing some of the devices which can result in premature or partial shutdown of the parallel chain.

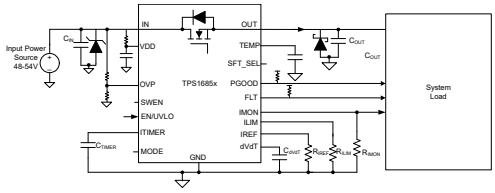
An integrated fast and accurate sense analog load current monitor facilitates predictive maintenance and advanced dynamic platform power management techniques such as Intel® PSYS and PROCHOT# to maximize system throughput and power supply utilization.

The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS16850VMAR TPS16851VMAR	VMA (LQFN, 23)	6.00mm × 5.00mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Device Comparison Table

PART NUMBER	FAULT BEHAVIOR
TPS16850	Auto-retry
TPS16851	Latch-off

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5 Pin Configuration and Functions

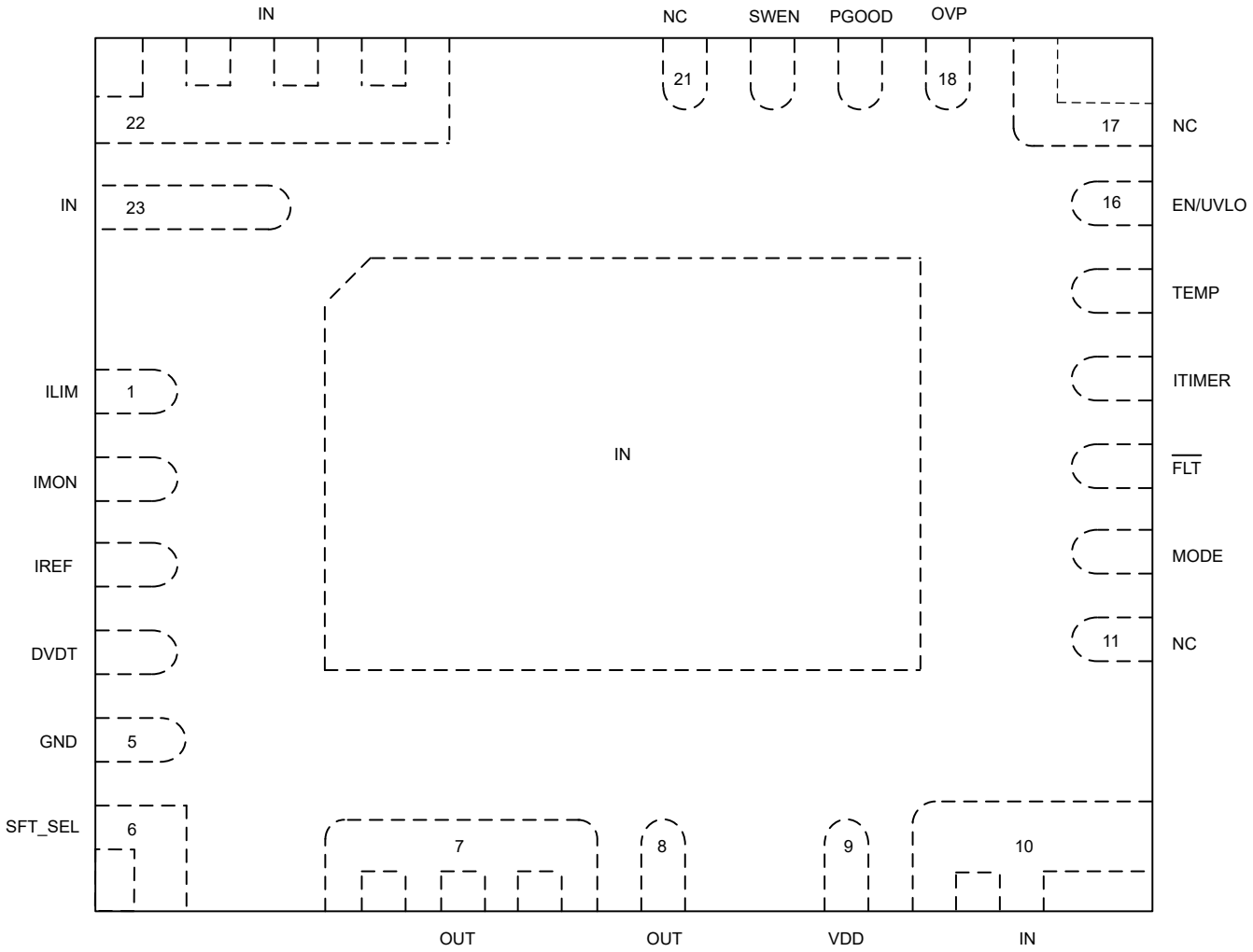

Figure 5-1. TPS1685x VMA Package, QFN 23-Pin (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
ILIM	1	I/O	An external resistor from this pin to GND sets the active current sharing threshold during steady-state. This pin also serves as individual eFuse current monitor output during steady state. *Do not leave floating.*
IMON	2	I/O	An external resistor from this pin to GND sets the overcurrent protection threshold and fast-trip threshold during steady-state. This pin also acts as a fast and accurate analog output load current monitor signal during steady-state. *Do not leave floating.*
IREF	3	I/O	This pin sets the reference voltage for overcurrent, short-circuit protection and active current sharing blocks. The reference voltage can be generated using internal current source and resistor on this pin, or can be driven from external voltage source. *Do not leave floating.*
dVdT	4	I/O	This pin is used to configure the output slew rate during Start-up. Leave this pin open to allow fastest start-up. Connect capacitor to ground to slow down the slew rate to manage inrush current.
GND	5	G	Device ground reference pin. Connect to system ground.
SFT_SEL	6	I/O	This pin selects the scalable fast trip threshold multiplier during steady state. Connect a resistor from this pin to GND to select the SFT multiplier.

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
OUT	7, 8	P	Power output. Must be soldered to the output power plane uniformly for proper heat dissipation.
VDD	9	P	Controller power input pin. Can be used to power the internal control circuitry with a filtered and stable supply which is not affected by system transients. Connect this pin to VIN through a series resistor and add a decoupling capacitor to GND.
IN	10, 22, 23	P	Power input. Must be soldered to the input power plane uniformly for proper heat dissipation.
NC	11, 17, 21	—	Do not connect anything to this pin.
MODE	12	I	This pin is used to configure the device for standalone/primary or secondary mode. Connect the pin to GND to configure device as a secondary to a primary eFuse/controller. Leave the pin floating for standalone/primary mode of operation.
$\overline{FLT}$	13	O	This is an open drain active low pin which is pulled low to indicate a fault. Pull up this pin to external supply voltage with a resistor.
ITIMER	14	I/O	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed the overcurrent threshold (but lower than fast-trip threshold) during steady-state operation before the device overcurrent response takes action.
TEMP	15	I/O	Analog voltage output for junction temperature. Can be tied together with TEMP outputs of multiple devices in a parallel configuration to indicate the peak temperature of the parallel chain.
EN/UVLO	16	I	Active high enable input. Connect resistor divider from input supply to set the undervoltage threshold. Do not leave floating.
OVP	18	I	This pin can be used to set the over-voltage set-point. Connect a resistor divider from VIN to this pin. Do not leave floating.
PGOOD	19	O	This is an open-drain active high power good pin which is asserted high when the device is in steady state. This pin has weak internal pull-up to internal supply voltage.
SWEN	20	I/O	This is an open-drain signal to indicate and control power switch ON/OFF status. This pin facilitates active synchronization between multiple devices in a parallel chain. This pin has weak internal pull-up to internal supply voltage.
IN	PowerPad	P	Power input. Must be soldered to the input power plane uniformly for proper heat dissipation.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{INMAX}, V_{DDMAX}	Maximum Input and Supply Voltage (-40℃ ≤ T_J ≤ 125℃)	IN, VDD	–0.3	90	V
$V_{INMAX,25}$, $V_{DDMAX,25}$	Maximum Input and Supply Voltage (25℃ ≤ T_J ≤ 125℃)	IN, VDD	–0.3	92	V
V_{OUTMAX}	Maximum Output Voltage	OUT	–5(2)	Min(92 V, VIN + 0.3)	
V_{IN} - V_{OUT}	Maximum difference between IN and OUT	IN, OUT	-0.3	90	V
$V_{ILIMMAX}$	Maximum ILIM Pin Voltage	ILIM	–0.3	Internally Limited	V
$V_{IMONMAX}$	Maximum IMON Pin Voltage	IMON	–0.3	Internally Limited	V
V_{SFT_SELMAX}	Maximum SFT_SEL Pin Voltage	SFT_SEL	–0.3	Internally Limited	V
V_{OVP}	Maximum OVP Pin Voltage	OVP	–0.3	6	V
V_{ITIMER}	Maximum ITIMER Pin Voltage	ITIMER	–0.3	Internally Limited	V
$V_{IREFMAX}$	Maximum IREF Pin Voltage	IREF	–0.3	6	V
$V_{DVDTMAX}$	Maximum DVDT Pin Voltage	DVDT	–0.3	6	V
$V_{MODEMAX}$	Maximum MODE Pin Voltage	MODE	–0.3	Internally Limited	V
$V_{SWENMAX}$	Maximum SWEN Pin Voltage	SWEN	–0.3	6	V
$I_{SWENMAX}$	Maximum SWEN Pin Sink	SWEN		10	mA
V_{ENMAX}	Maximum EN/UVLO Pin Voltage	EN/UVLO	–0.3	6	V
$V_{\overline{FLT}MAX}$	Maximum $\overline{FLT}$ Pin Voltage	$\overline{FLT}$	–0.3	6	V
$I_{\overline{FLT}MAX}$	Maximum $\overline{FLT}$ Pin Sink Current	$\overline{FLT}$		10	mA
$V_{PGOODMAX}$	Maximum PGOOD Pin Voltage	PGOOD	–0.3	6	V
$I_{PGOODMAX}$	Maximum PGOOD Pin Sink Current	PGOOD		10	mA
V_{TEMP}	Maximum TEMP Pin Voltage	TEMP	–0.3	6	V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	Internally Limited		A
T_{JMAX}	Junction temperature		Internally Limited		°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) During FET OFF condition for negative transients.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	9	80	V
V_{DD}	Supply Voltage Range	VDD	9	80	V
V_{OUT}	Output Voltage Range	OUT		V_{IN}	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/ UVLO		5	V
dVdT	dVdT Pin Cap Voltage Rating	dVdT	4		V
V_{PGOOD}	PGOOD Pin Pull-up Voltage Range	PGOOD		5	V
$V_{\overline{FLT}}$	$\overline{FLT}$ Pin Pull-up Voltage Range	$\overline{FLT}$		5	V
V_{SWEN}	SWEN Pin Pull-up Voltage Range	SWEN		5	V
V_{TEMP}	TEMP Pin Voltage Rating	TEMP		5	V
V_{IREF}	IREF Pin Voltage Range	IREF	0.3	1.2	V
V_{ILIM}	ILIM Pin Voltage Range	ILIM		0.4	V
V_{IMON}	IMON Pin Voltage Range	IMON		1.2	V
C_{IN}	Capacitance on IN pins	IN	10		nF
C_{OUT}	Capacitance on OUT pins	OUT	10		µF
dV_{IN}/dt	Slew rate on IN pins	IN		500	V/µs
I_{MAX}	RMS Switch Current T_J ≤125°C	IN to OUT		20	A
$I_{MAX, Pulse}$	Peak Output Current for ≤10 ms duration, T_A ≤ 70 °C	IN to OUT		27	A
T_J	Junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1) (2)		TPS1685X LQFN PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a 3 x 4.5" PCB (2s2p) as JESD51-7

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6.5 Electrical Characteristics

–40°C ≤ T_J ≤ +125°C, VIN = V_{DD} = 50 V, OUT = Open, R_{ILIM} = 931 Ω R_{IMON} = 2.55 kΩ, V_{IREF} = 1 V , $\overline{FLT}$ = 33 kΩ pull-up to 3.3 V, PGOOD = 33 kΩ pull-up to 3.3 V, C_{OUT} = 10 µF, C_{IN} = 10 nF, dVdT = Open, ITIMER = Open. , $V_{EN/UVLO}$ = 2 V, TEMP = Open, MODE = Open. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VDD)						
V_{IN}	Input voltage range		9		80	V
V_{DD}	Input voltage range		V_{IN}		80	V
$I_{QON(VDD)}$	V_{DD} ON state quiescent current	V_{DD} > V_{UVPR}, V_{EN} ≥ V_{UVLOR}, V_{OVP} < V_{OVPF}		0.6		mA
V_{UVPR}	V_{DD} Undervoltage Protection Threshold Rising	V_{DD} Rising		8.5		V
V_{UVPF}	V_{DD} Undervoltage Protection Threshold falling	V_{DD} Falling		7.05		V
V_{UVPHYS}	UVP Hysteresis VDD			1450		mV
INPUT SUPPLY (IN)						
$V_{UVPR(VIN)}$	VIN Undervoltage Protection Threshold	V_{IN} Rising		8.5		V
$V_{UVPF(VIN)}$	VIN Undervoltage Protection Threshold	V_{IN} Falling		7.05		V
$I_{QON(VIN)}$	V_{IN} ON state quiescent current	V_{EN} ≥ V_{UVLOR}		1.35		mA
$I_{QOFF(VIN)}$	V_{IN} OFF state current	V_{SDR} < V_{EN} < V_{UVLO}		45		µA
$I_{SD(VIN)}$	V_{IN} shutdown current	V_{EN} < V_{SDF}		44		µA
ENABLE / UNDERVOLTAGE LOCKOUT (EN/UVLO)						
$V_{UVLO(R)}$	EN/UVLO pin voltage threshold for turning on, rising	EN/UVLO Rising		1.2		V
$V_{UVLO(F)}$	EN/UVLO pin voltage threshold for turning off and engaging QOD, falling (primary device)	EN/UVLO Falling		1.12		V
V_{UVLOF}	EN/UVLO pin voltage threshold for turning off and engaging QOD, falling (Secondary device)	EN/UVLO Falling		1		V
$V_{UVLOHYS}$	UVLO Hysteresis			84		mV
V_{SDF}	Shutdown threshold	EN/UVLO Falling		0.45		V
V_{SDR}	Shutdown threshold	EN/UVLO Rising		0.5		V
OVERVOLTAGE PROTECTION (IN)						
$V_{OVP(R)}$	Overvoltage protection threshold (rising)	OVP pin rising		1.16		V
$V_{OVP(F)}$	Overvoltage protection threshold (falling)	OVP pin falling		1.12		V
V_{OVPHYS}	Overvoltage protection threshold (Hysterisis)			41		mV
$V_{OVPR(IN)}$	Internal Overvoltage protection threshold (rising)	VIN Rising		90.75		V
$V_{OVPF(IN)}$	Internal Overvoltage protection threshold (falling)	VIN falling		84.5		V
ON-RESISTANCE (IN - OUT)						
R_{ON}	ON state resistance	I_{OUT} = 12 A		3.65		mΩ
CURRENT LIMIT REFERENCE (IREF)						
V_{IREF}	IREF pin recommended voltage range			1		V
I_{IREF}	IREF internal sourcing current	V_{IREF} = 1 V		25		µA
CURRENT LIMIT (ILIM)						
$G_{ILIM(LIN)}$	Current Monitor Gain (ILIM:IOUT) vs. IOUT.	Device in steady state (PG asserted), I_{OUT} = 12 A		18.26		µA/A

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6.5 Electrical Characteristics (continued)

–40°C ≤ T_J ≤ +125°C, VIN = V_{DD} = 50 V, OUT = Open, R_{ILIM} = 931 Ω R_{IMON} = 2.55 kΩ, V_{IREF} = 1 V , $\overline{FLT}$ = 33 kΩ pull-up to 3.3 V, PGOOD = 33 kΩ pull-up to 3.3 V, C_{OUT} = 10 µF, C_{IN} = 10 nF, dVdT = Open, ITIMER = Open. , $V_{EN/UVLO}$ = 2 V, TEMP = Open, MODE = Open. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{start-up}$	IOUT Start-up Current limit regulation threshold	V_{IN} - V_{OUT} = 350 mV		0.56		A
V_{FB}	Foldback voltage			2		V
OUTPUT CURRENT MONITOR AND OVERCURRENT PROTECTION (IMON)						
G_{IMON}	Current Monitor Gain (IMON:IOUT)	Device in steady state (PG asserted), for 2A ≤ I_{OUT} ≤ 20 A		18.38		µA/A
G_{IMON}	Current Monitor Gain (IMON:IOUT)	Device in steady state (PG asserted), I_{OUT} = 4 A		18.27		µA/A
I_{OCP}	IOUT Current limit trip (Circuit-Breaker) threshold	R_{IMON} = 2.55k Ω, V_{IREF} = 1 V		21.51		A
CURRENT FAULT TIMER (ITIMER)						
I_{ITMR}	ITIMER pin internal discharge current	I_{OUT} > I_{OCP}, ITIMER ↓		2		µA
R_{ITMR}	ITIMER pin internal pull-up resistance			12.66		kΩ
V_{INT}	ITIMER pin internal pull-up voltage	I_{OUT} < I_{OCP}		5		V
ΔV_{ITMR}	ITIMER discharge voltage	I_{OUT} > I_{TRIP}, ITIMER ↓		1.54		V
SHORT-CIRCUIT PROTECTION						
I_{FFT}	Fixed fast-trip threshold in steady state (primary)	PG asserted High (MODE = Open)		87.11		A
I_{FFT}	Fixed fast trip threshold in steady state (secondary)	PG asserted High (MODE = GND)		97.2		A
I_{SFT}	Scalable fast trip current	R_{SFT_SEL} < 95-kΩ, PG asserted High (MODE = Open)		8 × I_{OCP}		A
I_{SFT}	Scalable fast trip current	105-kΩ < R_{SFT_SEL} < 195-kΩ, PG asserted High (MODE = Open)		2.5 × I_{OCP}		A
I_{SFT}	Scalable fast trip current	105-kΩ < R_{SFT_SEL} < 195-kΩ, PG asserted High (MODE = GND)		2.8 × I_{OCP}		A
I_{SFT}	Scalable fast trip current	205-kΩ < R_{SFT_SEL} < 295-kΩ, PG asserted High (MODE = Open)		2 × I_{OCP}		A
I_{SFT}	Scalable fast trip current	205-kΩ < R_{SFT_SEL} < 295-kΩ, PG asserted High (MODE = GND)		2.26 × I_{OCP}		A
I_{SFT}	Scalable fast trip current	305-kΩ < R_{SFT_SEL}, PG asserted High (MODE = Open)		1.5 × I_{OCP}		A
I_{SFT}	Scalable fast trip current	305-kΩ < R_{SFT_SEL},PG asserted High (MODE = GND)		1.71 × I_{OCP}		A
$I_{SFT(SAT)}$	Scalable fast trip Current (inrush)	During Powerup, PGOOD Low		2		A
ACTIVE CURRENT SHARING						
$R_{ON(ACS)}$	R_{ON} during Active current sharing	V_{ILIM} > 1.1 x (1/3)xV_{IREF}		4.67		mΩ
$G_{IMON(ACS)}$	IMON:IOUT ratio during active current limiting	PG asserted High, V_{ILIM} > 1.1 x V_{IREF}		18.67		µA/A
$CL_{REF(ACS)}$	Ratio of active current sharing trigger threshold to steady state circuit-breaker threshold	PG asserted High		36.67		%
INRUSH CURRENT PROTECTION (DVDT)						
I_{DVDT}	dVdt Pin Charging Current (Primary/ Standalone mode)	MODE = Open		2.06		µA

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6.5 Electrical Characteristics (continued)

–40°C ≤ T_J ≤ +125°C, VIN = V_{DD} = 50 V, OUT = Open, R_{ILIM} = 931 Ω R_{IMON} = 2.55 kΩ, V_{IREF} = 1 V , $\overline{FLT}$ = 33 kΩ pull-up to 3.3 V, PGOOD = 33 kΩ pull-up to 3.3 V, C_{OUT} = 10 µF, C_{IN} = 10 nF, dVdT = Open, ITIMER = Open. , $V_{EN/UVLO}$ = 2 V, TEMP = Open, MODE = Open. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{DVDT}	dVdt Gain	0.4 V < V_{dVdt} < 2.4 V		25		V/V
$I_{DVDTLKG}$	dVdt Pin Leakage Current (Secondary mode)	MODE = GND		30		nA
R_{DVDT}	dVdt Pin to GND Discharge Resistance			494		Ω
GHI						
$V_{GS(GHI)}$ Rising	G-S Threshold when GHI/PG is asserted			7		V
$V_{GS(GHI)}$ Falling	G-S Threhold when GHI/PG is de-asserted			3.4		V
$R_{ON(GHI)}$	Ron When GHI/PG is asserted			3.65		mΩ
QUICK OUTPUT DISCHARGE (QOD)						
I_{QOD}	Quick Output Discharge pull-down current	$V_{SD(R)}$ < V_{EN} < V_{UVLO}, 0 < Tj < 125 °C, VIN = 50 V		21.75		mA
I_{QOD}	Quick Output Discharge pull-down current	$V_{SD(R)}$ < V_{EN} < V_{UVLO}, -40 < Tj < 125 °C, VIN = 50 V		21.75		mA
TEMPERATURE SENSOR OUTPUT (TEMP)						
G_{TMP}	TEMP sensor gain	VIN = 51 V		2.75		mV/°C
V_{TMP}	TEMP pin output voltage	T_J = 25 °C, VIN = 51 V		670		mV
I_{TMPSRC}	TEMP pin sourcing current	VIN = 51 V		110		µA
I_{TMPSNK}	TEMP pin sinking current	VIN = 51 V		10.4		µA
OVERTEMPERATURE PROTECTION (OTP)						
TSD	Absolute Thermal Shutdown Rising Threshold	T_J Rising, , VIN = 51 V		150		°C
TSD_{HYS}	Absolute Thermal shutdown hysteresis	T_J Falling, VIN = 51 V		13		°C
FET HEALTH MONITOR						
V_{DSFLT}	FET D-S Fault Threshold	SWEN = L, VIN = 51 V		0.5		V
V_{DSOK}	FET D-S Fault Recovery Threshold	SWEN = L, VIN = 51 V		0.62		V
SINGLE POINT FAILURE (IMON, IREF, ITIMER)						
I_{OC_BKP}	Back-up overcurrent protection threshold	IMON short to GND		39		A
POWER GOOD OUTPUT (PG)						
R_{PG}	Power Good Output Discharge resistance	V_{EN} < $V_{SD(F)}$, VIN = 51 V		60		Ω

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6.6 Logic Interface

–40°C ≤ T_J ≤ +125°C, VIN = V_{DD} = 45 V to 60 V, OUT = Open, R_{ILIM} = 931 Ω R_{IMON} = 2.55 kΩ, V_{IREF} = 1 V , $\overline{FLT}$ = 33 kΩ pull-up to 3.3 V, PGOOD = 33 kΩ pull-up to 3.3 V, C_{OUT} = 10 µF, C_{IN} = 10 nF, dVdT = Open, ITIMER = Open. , $V_{EN/UVLO}$ = 2 V, TEMP = Open, MODE = Open. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWEN						
R_{SWEN}	SWEN pin pull-down resistance	SWEN de-asserted Low		7.5		Ω
$I_{SWENLKG}$	SWEN pin leakage current	SWEN asserted high, pulled up to 5.5 V		0.02		uA
FAULT INDICATION ($\overline{FLT}$)						
$R_{\overline{FLT}}$	$\overline{FLT}$ pin pull-down resistance	$\overline{FLT}$ asserted Low		4.2		Ω
I_{FLTLKG}	$\overline{FLT}$ pin leakage current	$\overline{FLT}$ de-asserted High, pulled up to 3.3 V through 33 kΩ		0.02		µA
POWER GOOD INDICATION (PG)						
R_{PG}	PG pin pull-down resistance	PG de-asserted Low		4.2		Ω
I_{PGKG}	PG pin leakage current	PG asserted High,pulled up to 3.3 V through 33 kΩ		0.02		µA

6.7 Timing Requirements

–40°C ≤ T_J ≤ +125°C, VIN = V_{DD} = 45 V to 60 V, OUT = Open, R_{ILIM} = 931 Ω R_{IMON} = 2.55 kΩ, V_{IREF} = 1 V , $\overline{FLT}$ = 33 kΩ pull-up to 3.3 V, PGOOD = 33 kΩ pull-up to 3.3 V, C_{OUT} = 10 µF, C_{IN} = 10 nF, dVdT = Open, ITIMER = Open. , $V_{EN/UVLO}$ = 2 V, TEMP = Open, MODE = Open. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVP}	Overvoltage protection response time	V_{OVP} > V_{OVPR} V to SWEN↓		1.5		µs
t_{Insdly}	Insertion delay	$V_{EN/UVLO}$ > $V_{UVLO(R)}$ to SWEN↑		10		ms
t_{FFT}	Fixed Fast-Trip response time Hard Short	V_{DS} > V_{DSCOMP} to I_{OUT}↓		195		ns
t_{SFT}	Scalable Fast-Trip response time	I_{OUT} > 3 x I_{OCP} to IOUT↓		400		ns
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.5 x I_{OCP}, C_{ITIMER} = Open		0		ms
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.5 x I_{OCP}, C_{ITIMER} = 4.7nF		3.5		ms
t_{RST}	Auto-Retry Interval	Auto-retry variant, Primary mode (MODE = Open)		285		ms
t_{REC}	Fault Recovery Time	Secondary mode (MODE = GND), SWEN↓ to SWEN↑		12		µs
$t_{EN(DG)}$	EN/UVLO de-glitch time			13		µs
$t_{SWEN(TO)}$	SWEN low interval to disable fast recovery					us
t_{SU_TMR}	Start-up timeout interval	SWEN↑ to FLT↓		5		s
$t_{Discharge}$	QOD discharge time (90% to 10% of V_{OUT})	V_{SD} < $V_{EN/UVLO}$ < V_{UVLO}, C_{OUT} = 0.5 mF, V_{IN} = 51 V.		1300		ms
t_{QOD}	QOD enable timer	V_{SD} < $V_{EN/UVLO}$ < V_{UVLO}		6		ms

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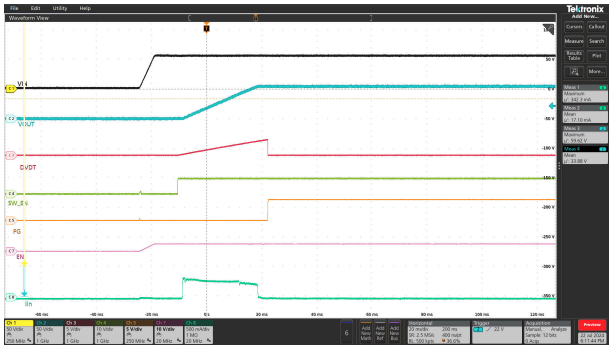
6.8 Typical Characteristics

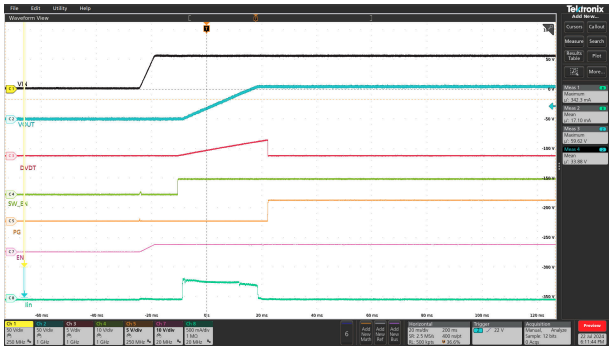


Input supply ramped up

Figure 6-1. Power Up Sequencing Using Input Supply with EN connected to VIN through Resistor

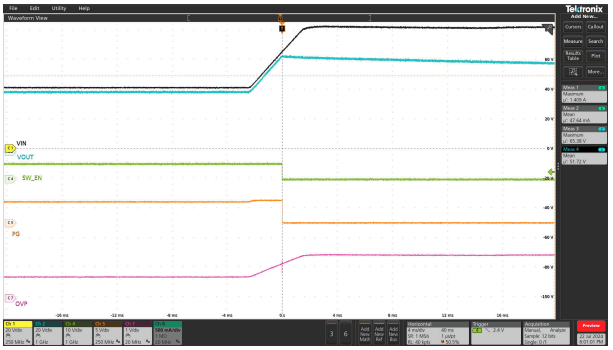
Input supply held steady, EN/UVLO pin toggled high

Figure 6-2. Power Up Using EN/UVLO Pin



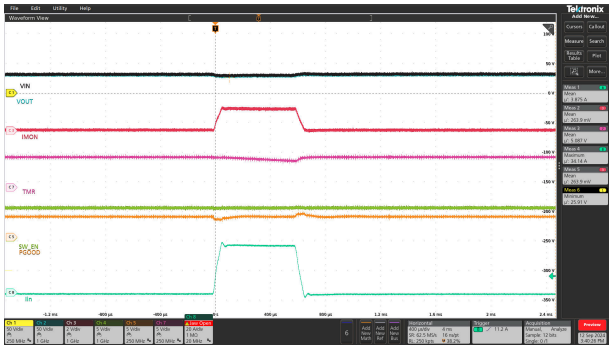
C_{OUT} = 144uF, C_{dVdt} = 22nF

Figure 6-3. Inrush Current Control with Capacitive Load



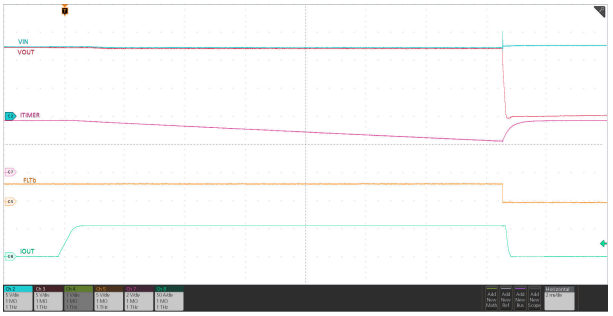
Input supply ramped up above 65V

Figure 6-4. Input Overvoltage Protection Response with OVP threshold= 65V



I_{OCP} = 22A, t_{ITIMER} = 1.4 ms, I_{OUT} pulsed above the I_{OCP} threshold for short duration without triggering circuit-breaker response

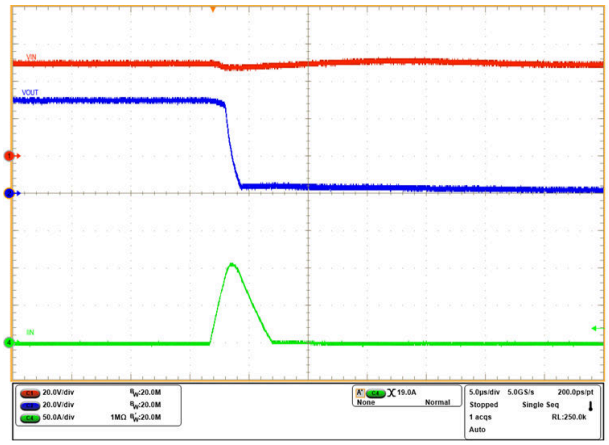
Figure 6-5. Peak Current Support Until Transient Overcurrent Blanking Timer expires



I_{OCP} = 50 A, t_{ITIMER} = 14 ms, I_{OUT} stays above the I_{OCP} threshold persistently to trigger circuit-breaker response

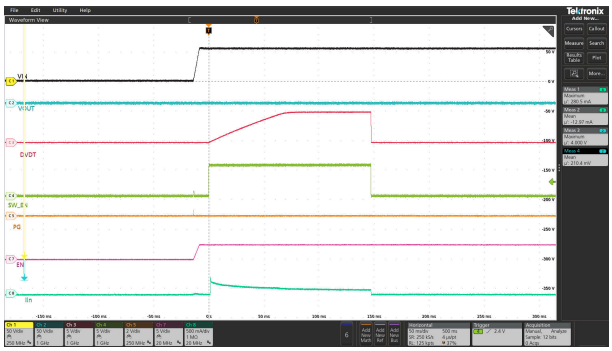
Figure 6-6. Overcurrent Protection Response (Circuit-Breaker)

6.8 Typical Characteristics (continued)



I_{OCP} = 22A, Output hard-short to GND while in steady. I_{OUT} rises above 2 × I_{OCP} triggers fast-trip response

Figure 6-7. Short-Circuit Protection Response



Device turned on using SWEN with output hard-short to GND. Device limits the current with foldback.

Figure 6-8. Power Up into Short-Circuit

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7 Detailed Description

7.1 Overview

The TPS1685x is an eFuse with integrated power switch that is used to manage load voltage and load current. The device starts its operation by monitoring the VDD and IN bus. When V_{DD} and V_{IN} exceed the respective undervoltage protection (UVP) thresholds, the device waits for the insertion delay timer duration to allow the supply to stabilize before starting up. Next, it samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low, the internal MOSFET is turned off.

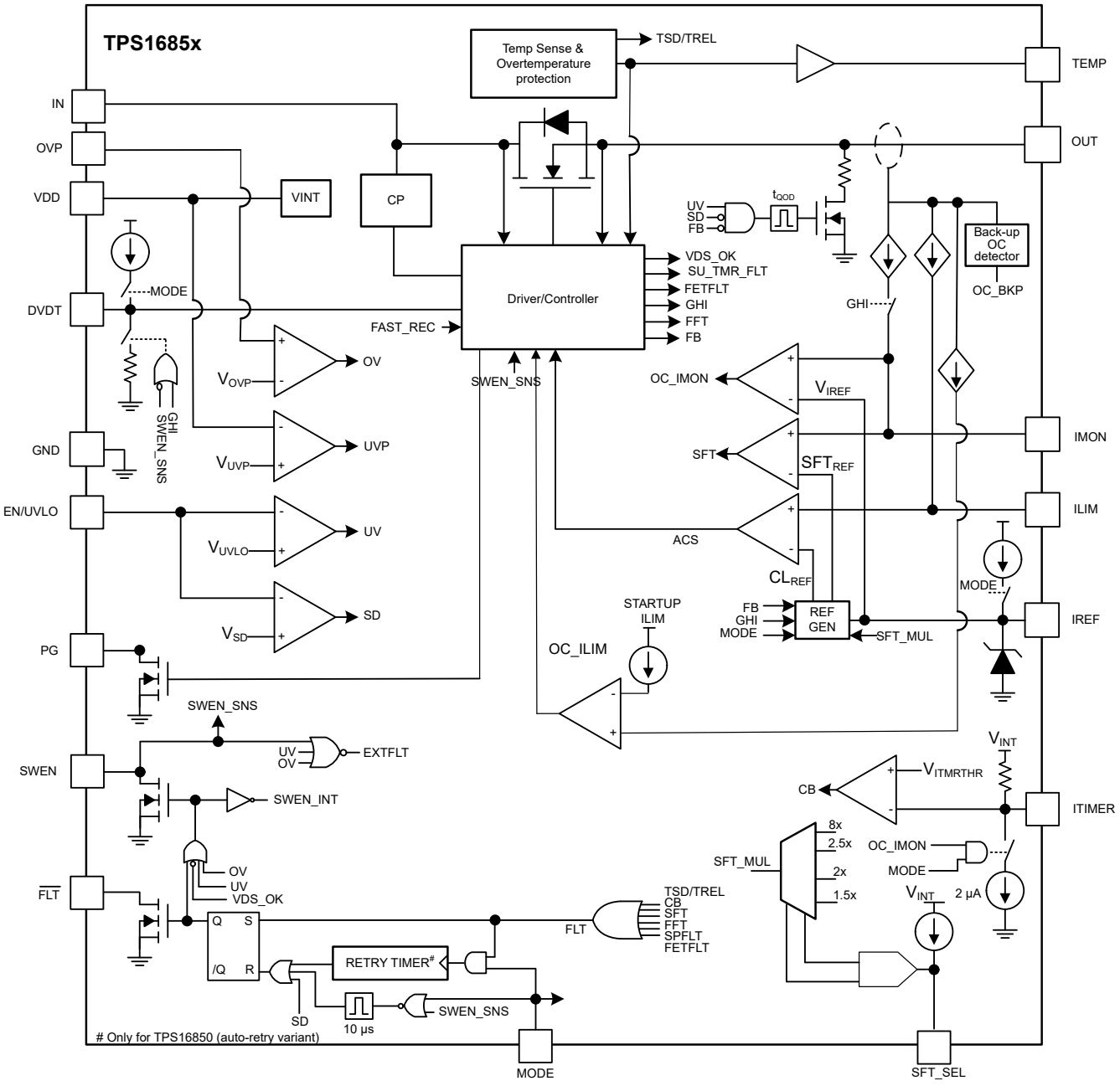
After a successful start-up sequence, the TPS1685x device now actively monitors its load current and input voltage, and controls the internal FET to ensure that the user adjustable overcurrent protection threshold limit I_{LIM} is not exceeded and overvoltage spikes on IN pin are cut-off. This keeps the system safe from harmful levels of voltage and current. At the same time, a user adjustable overcurrent blanking timer allows the system to pass transient peaks in the load current profile without tripping the eFuse. Similarly, voltage transients on the supply line are intelligently masked to prevent nuisance trips. This ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

The device has integrated high accuracy and high bandwidth analog load current monitor, which allows the system to precisely monitor the load current in steady state as well as during transients. This facilitates the implementation of advanced dynamic platform power management techniques to maximize system power utilization and throughput without sacrificing safety and reliability.

For systems needing higher load current support, multiple TPS1685x eFuses can be connected in parallel. All devices share current during start-up as well as steady state to avoid overstressing some of the devices more than others resulting in pre-mature or partial shutdown of the parallel chain. The devices synchronize their operating states to ensure graceful startup, shutdown and response to faults.

The device has integrated protection circuits to ensure device safety and reliability under recommended operating conditions. The internal FET is protected at all time using the thermal shutdown mechanism, which turns off the FET whenever the junction temperature (Tj) becomes too hot.

7.2 Functional Block Diagram



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7.3 Feature Description

The TPS1685x eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

7.3.1 Undervoltage Protection

The TPS1685x implements Undervoltage Lockout on VDD & VIN in case the applied voltage becomes too low for the system or device to properly operate. The Undervoltage lockout has a default lockout threshold of V_{UVP} internally on VDD and V_{UVPIN} on V_{IN}. Also, the UVLO comparator on the EN/UVLO pin allows the Undervoltage Protection threshold to be externally adjusted to a user defined value. The figure and equation below shows how a resistor divider can be used to set the UVLO set point for a given voltage supply.

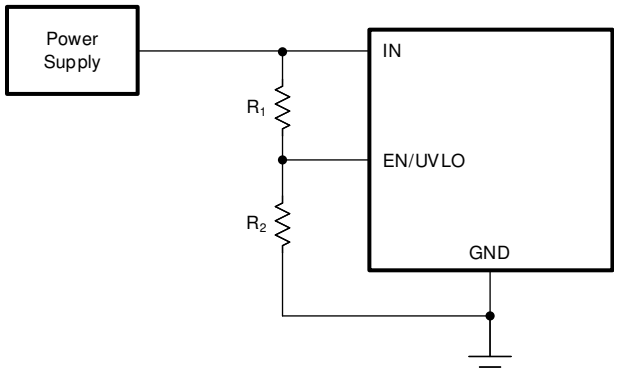

Figure 7-1. Adjustable Undervoltage Protection

$$V_{IN(UV)} = V_{UVLO(R)}\frac{R_1 + R_2}{R_2} \quad (1)$$

The EN/UVLO pin implements a bi-level threshold.

1. $V_{EN} > V_{UVLO(R)}$: Device is fully ON.
2. $V_{SD(F)} < V_{EN} < V_{UVLO(F)}$: The FET along with most of the controller circuitry is turned OFF, except for some critical bias and digital circuitry. Holding the EN/UVLO pin in this state for > t_{QOD} activates the Output Discharge function.
3. $V_{EN} < V_{SD(F)}$: All active circuitry inside the part is turned OFF and it retains no digital state memory. It also resets any latched faults. In this condition, the device quiescent current consumption is minimal.

7.3.2 Insertion Delay

The TPS1685x implements insertion delay at start-up to ensure the supply has stabilized before the device tries to turn on. This is to prevent any unexpected behavior in the system if the device tries to turn on while the card has not made firm contact with the backplane or if there's any supply ringing/oscillation during startup.

The device initially waits for the VDD supply to rise above the UVP threshold and all the internal bias voltages to settle. After that, it remains off for an additional delay of 10 ms irrespective of the EN/UVLO pin condition.

7.3.3 Overvoltage Protection

The TPS1685x implements overvoltage lockout to protect the load from input overvoltage conditions. A resistor divider needs to be connected on OVP pin to set the overvoltage set-point externally.

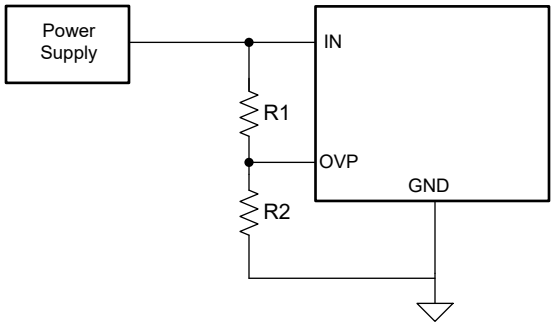

Figure 7-2. Adjustable Overvoltage Protection

$$V_{IN(OVP)} = V_{OVP(R)} \frac{R1 + R2}{R2} \quad (2)$$

When V_{IN} exceeds this value, the device turns off protecting the load from overvoltage.

The device also has a fixed internal OV protection on IN pin at $V_{OVPR(IN)}$.

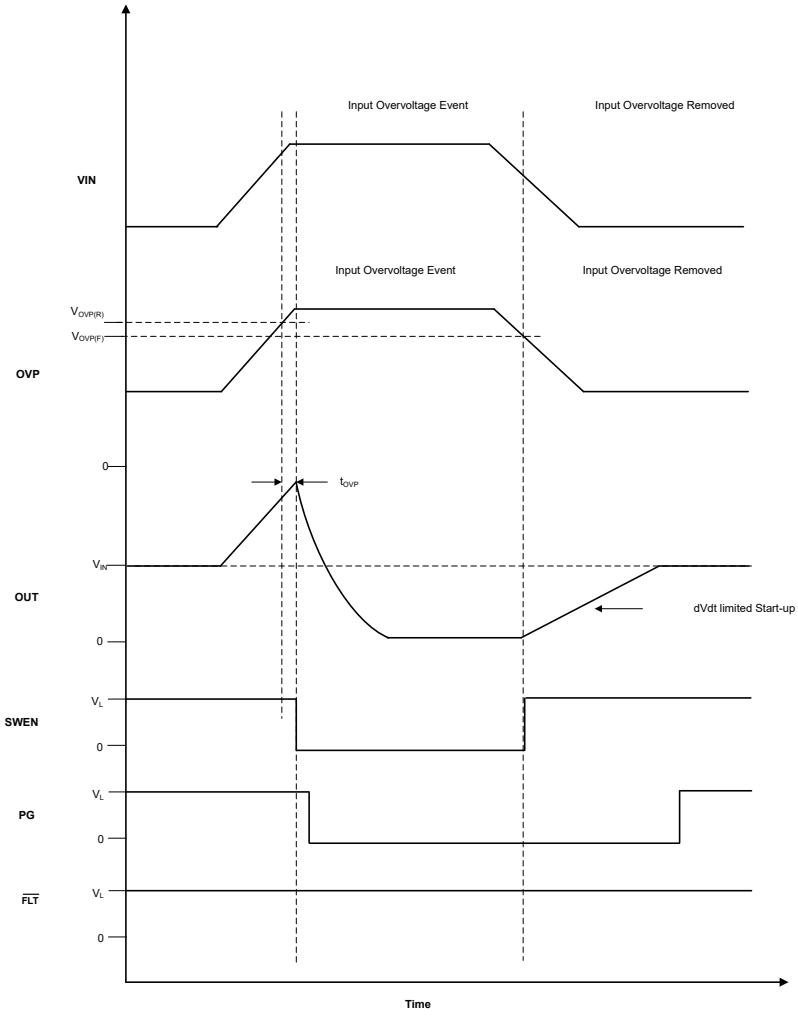

Figure 7-3. Input Overvoltage Protection Response

7.3.4 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS1685x incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Fixed current limit ($I_{start-up}$) for overcurrent protection during start-up
3. Circuit-breaker with an adjustable threshold (I_{OCP}) and blanking timer (t_{ITIMER}) for overcurrent protection during steady-state

7.3.4.1 Slew rate (dVdt) and Inrush Current Control

During hot plug events or while trying to charge a large output capacitance, there can be a large inrush current. If the inrush current is not managed properly, the inrush current can damage the input connectors and cause the system power supply to droop. This action can lead to unexpected restarts elsewhere in the system. The inrush current during turn-on is directly proportional to the load capacitance and rising slew rate. Equation 3 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{LOAD}):

$$SR(V/ms) = \frac{I_{INRUSH}(A)}{C_{LOAD}(mF)} \quad (3)$$

A capacitor can be added to the DVDT pin to control the rising slew rate and lower the inrush current during turn-on. The required CdVdt capacitance to produce a given slew rate can be calculated using Equation 4.

$$C_{DVDT}(nF) = \frac{48}{SR(V/ms)} \quad (4)$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

Note

1. High input slew rates in combination with high input power path inductance can result in oscillations during start-up. This can be mitigated using one or more of the following steps:
   a. Reduce the input inductance.
   b. Increase the capacitance on VIN pin.
   c. Increase the dVdt pin capacitance to reduce the slew rate or increase the start-up time. TI recommends using a minimum start-up time of 8ms.

7.3.4.1.1 Start-Up Time Out

If the start-up is not completed, that is, the FET is not fully turned on within a certain timeout interval (t_{SU_TMR}) after SWEN is asserted, the device registers it as a fault. $\overline{FLT}$ is asserted low and the device goes into latch-off or auto-retry mode depending on the device configuration.

7.3.4.2 Steady-State Overcurrent Protection (Circuit-Breaker)

The TPS1685x responds to output overcurrent conditions during steady-state by performing a circuit-breaker action after a user-adjustable transient fault blanking interval. This action allows the device to support a higher peak current for a short user-defined interval but also ensures robust protection in case of persistent output faults.

The device constantly senses the output load current and provides an analog current output (I_{IMON}) on the IMON pin which is proportional to the load current, which in turn produces a proportional voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) as per Equation 5.

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \quad (5)$$

Where G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT})

The overcurrent condition is detected by comparing this voltage against the voltage on the IREF pin as a reference. The reference voltage (V_{IREF}) can be controlled in two ways, which sets the overcurrent protection threshold (I_{OCP}) accordingly.

- In the standalone or primary mode of operation, the internal current source interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage. It is also possible to drive the IREF pin from an external low impedance reference voltage source as shown in Equation 6.

$$V_{IREF} = I_{IREF} \times R_{IREF} \quad (6)$$

- In a primary and secondary parallel configuration, the primary eFuse or controller drives the voltage on the IREF pin to provide an external reference (V_{IREF}) for all the secondary devices in the chain.

The overcurrent protection threshold during steady-state (I_{OCP}) can be calculated using Equation 7.

$$I_{OCP} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \quad (7)$$

After an overcurrent condition is detected, that is the load current exceeds the user adjustable over current limit threshold (I_{OCP}), but stays lower than the short-circuit threshold (I_{SFT}), the device starts discharging the ITIMER pin capacitor using an internal pulldown current. If the load current drops below the current limit threshold before the ITIMER capacitor discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the circuit-breaker action is not engaged. This action allows short overload transient pulses to pass through the device without tripping the circuit. If the overcurrent condition persists, the ITIMER capacitor continues to discharge and after it falls by ΔV_{ITIMER}, the circuit-breaker action turns off the FET immediately. At the same time, the ITIMER cap is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This action ensures the full blanking timer interval is provided for every overcurrent event. Equation 8 can be used to calculate the R_{IMON} value for the desired overcurrent threshold.

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP}} \quad (8)$$

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The transient overcurrent blanking interval can be calculated using Equation 9.

$$t_{ITIMER}(ms) = \frac{C_{ITIMER}(nF) \times \Delta V_{ITIMER}(V)}{I_{ITIMER}(\mu A)} \quad (9)$$

Note

1. Leave the ITIMER pin open to allow the part to break the circuit with the minimum possible delay. However, this makes the circuit-breaker response extremely sensitive to noise and can cause false tripping during load transients.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the quiescent current – not a recommended mode of operation.
3. Increasing the ITIMER cap value extends the overcurrent blanking interval. However, it also extends the time needed for the ITIMER cap to recharge up to V_{INT} before the next overcurrent event. If the next overcurrent event occurs before the ITIMER cap is recharged fully, it takes less time to discharge to the VITIMER threshold, thereby it provides a shorter blanking interval than intended.

Figure 7-4 illustrates the overcurrent response for TPS1685x eFuse. After the part shuts down due to a circuit-breaker fault, it either stays latched off (TPS16851 variant) or restarts automatically after a fixed delay (TPS16850 variant).

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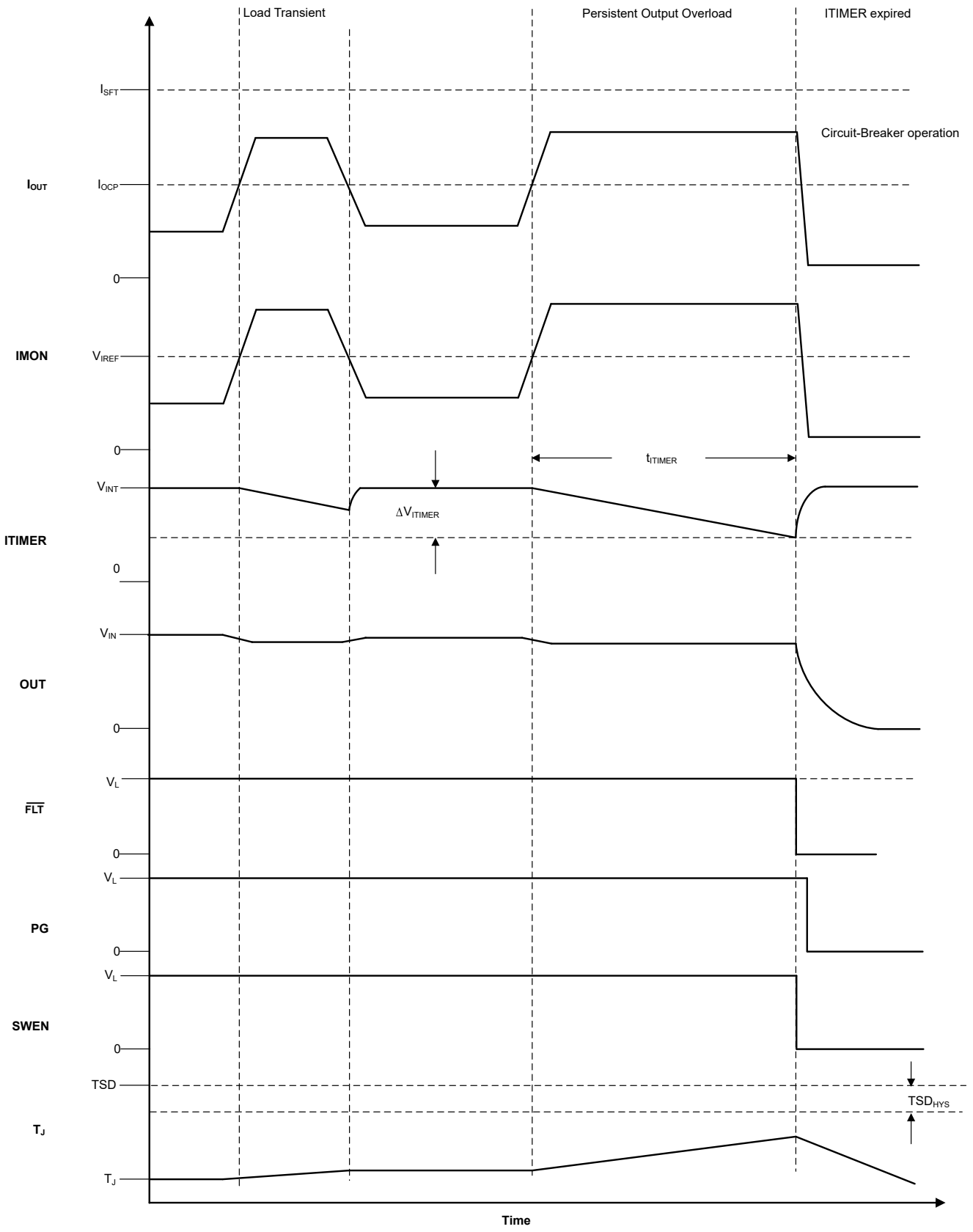

Figure 7-4. Steady-State Overcurrent (Circuit-Breaker) Response

7.3.4.3 Active Current Limiting During Start-Up

The TPS1685x responds to output overcurrent conditions during start-up by actively limiting the current. The startup current limit is internally fixed to $I_{start-up}$.

When the load current during start-up exceeds $I_{Start-up}$, the device tries to regulate and hold the load current at $I_{Start-up}$.

During current regulation, the output voltage drops, resulting in increased device power dissipation across the FET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the FET is turned off. After the part shuts down due to a TSD fault, it either stays latched off (TPS16851 variants) or restarts automatically after a fixed delay (TPS16850 variants). See *Overtemperature protection* section for more details on device response to overtemperature.

Note

The active current limit block employs a foldback mechanism during start-up based on the output voltage (V_{OUT}). When V_{OUT} is below the foldback threshold (V_{FB}), the current limit threshold is further lowered.

7.3.4.4 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When an output short-circuit is detected, the internal fast-trip comparator triggers a fast protection sequence to prevent the current from building up further and causing any damage or excessive input supply droop. The fast-trip comparator employs a scalable threshold (I_{SFT}) during steady-state . I_{SFT} can be selected by resistor on SFT_SEL pin. This enables the user to adjust the fast-trip threshold as per system rating, rather than using a high fixed threshold which can not be suitable for all systems. After the current exceeds the fast-trip threshold, the TPS1685x turns off the FET within t_{SFT}. The device also employs a higher fixed fast-trip threshold (I_{FFT}) to provide fast protection against hard short-circuits during steady-state (FET in linear region). After the current exceeds I_{FFT}, the FET is turned off completely within t_{FFT}.

Table 7-1. Device Functional Modes Based on resistor on SFT_SEL Pin

I_{SFT_SEL}	SFT_SEL pin	MODE pin
8 x I_{OCP}	R_{SFT_SEL} <95kΩ	Open
2.5 x I_{OCP}	105kΩ < R_{SFT_SEL} < 195kΩ	Open
2.8 xI_{OCP}	105kΩ < R_{SFT_SEL} < 195kΩ	Gnd
2 xI_{OCP}	205kΩ < R_{SFT_SEL} < 295kΩ	Open
2.26xI_{OCP}	205kΩ < R_{SFT_SEL} < 295kΩ	Gnd
1.5 xI_{OCP}	305kΩ < R_{SFT_SEL}	Open
1.71xI_{OCP}	305kΩ < R_{SFT_SEL}	Gnd

Figure 7-5 illustrates the short-circuit response for TPS1685x eFuse.

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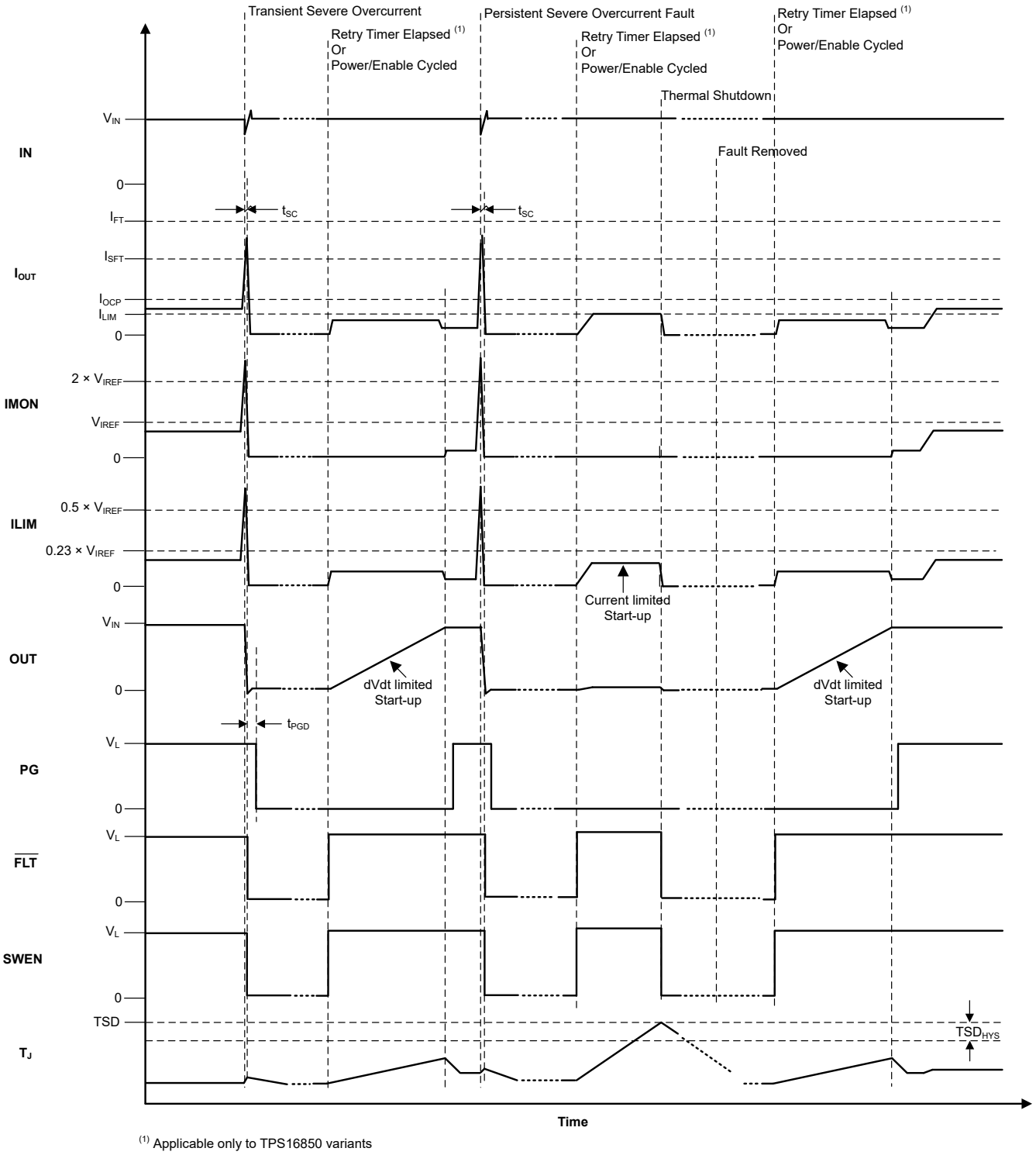

(1) Applicable only to TPS16850 variants

Figure 7-5. Short-Circuit Response

7.3.5 Analog Load Current Monitor (IMON)

The TPS1685x allows the system to monitor the output load current accurately by providing an analog current on the IMON pin which is proportional to the current through the FET. The benefit of having a current output is that the signal can be routed across a board without adding significant errors due to voltage drop or noise

coupling from adjacent traces. The current output also allows the IMON pins of multiple TPS1685x devices to be tied together to get the total current in a parallel configuration. The IMON signal can be converted to a voltage by dropping it across a resistor at the point of monitoring. The user can sense the voltage (V_{IMON}) across the R_{IMON} to get a measure of the output load current using Equation 10.

$$I_{OUT} = \frac{V_{IMON}}{G_{IMON} \times R_{IMON}} \quad (10)$$

The TPS1685x IMON circuit is designed to provide high bandwidth and high accuracy across load and temperature conditions, irrespective of board layout and other system operating conditions. This design allows the IMON signal to be used for advanced dynamic platform power management techniques such as Intel® PSYS or PROCHOT# to maximize system power usage and platform throughput without sacrificing safety or reliability.

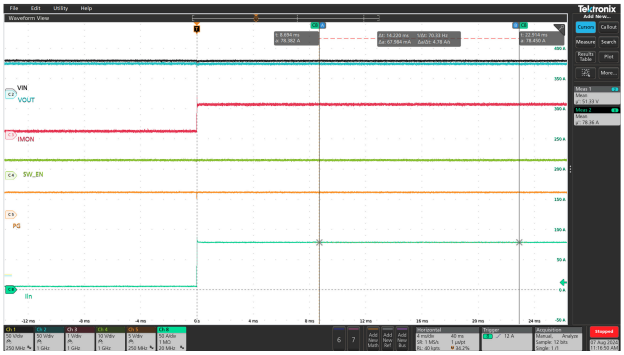

Figure 7-6. Analog Load Current Monitor Response

Note

1. The IMON pin provides load current monitoring information only during steady-state. During inrush, the IMON pin reports zero load current.
2. The ILIM pin reports the individual device load current at all times and can also be used as an analog load current monitor for each individual device.
3. Care must be taken to minimize parasitic capacitance on the IMON and ILIM pins to avoid any impact on the overcurrent and short-circuit protection timing.

7.3.6 Mode Selection (MODE)

This pin can be used to configure the TPS1685x as a primary device in a chain along with other TPS1685x eFuses, designated as secondary devices. This feature allows some of the TPS1685x pin functions to be changed to aid the primary + secondary parallel connection.

This pin is sampled at power up. Leaving the pin open configures it as a primary or standalone device. Connecting this pin to GND configures it as a secondary device.

The following functions are disabled in secondary mode and the device relies on the primary device to provide this functionality:

1. IREF internal current source
2. DVDT internal current source
3. Overcurrent detection in steady-state for circuit-breaker response
4. PG de-assertion (pulldown) after reaching steady-state
5. Latch-off after fault

In secondary mode, the following functions are still active:

1. Overtemperature protection
2. Start-up current limit
3. Active current sharing during inrush as well as steady-state

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4. Analog current monitor (IMON) in steady state
5. Steady-state overcurrent detection based on IMON. This is indicated by pulling ITIMER pin low internally, but does not trigger circuit-breaker action on ITIMER expiry. Rather, it relies on the primary device to start its own ITIMER and then trigger the circuit-breaker action for the whole chain by pulling SWEN low after the ITIMER expiry. However, the secondary devices use an internal overcurrent timer as a backup in case the primary device fails to initiate circuit-breaker action for an extended period of time. Refer to *Single Point Failure Mitigation* section for details.
6. Each device still has individual scalable and fixed fast-trip thresholds to protect itself. The individual short-circuit protection threshold is set to higher values in secondary mode so that the primary device can lower it further for the whole system.
7. Individual OVP is set to maximum in secondary device so that the primary can lower it further for the whole system.
8. $\overline{\text{FLT}}$ assertion based on individual device fault detection (except circuit-breaker).
9. PG de-assertion control during inrush and assertion control after device reaches steady state. However, after that in steady state, the secondary device no longer controls the de-assertion of the PG in case of faults.
10. SWEN assertion or de-assertion based on internal events as well as FET ON and OFF control based on SWEN pin status.

In secondary mode, the device behavior during short-circuit and fast-trip is also altered. More details are available in the *Short-Circuit Protection* section.

7.3.7 Parallel Device Synchronization (SWEN)

The SWEN pin is a signal which is driven high when the FET must be turned ON. When the SWEN pin is driven low (internally or externally), it signals the driver circuit to turn OFF the FET. This pin serves both as a control and handshake signal and allows multiple devices in a parallel configuration to synchronize their FET ON and OFF transitions.

Table 7-2. SWEN Summary

Device State	FET Driver Status	SWEN
Steady-state	ON	H
Inrush	ON	H
Overtemperature shutdown	OFF	L
Auto-retry timer running	OFF	L
Undervoltage (EN/UVLO)	OFF	L
Undervoltage (VDD UVP)	OFF	L
Undervoltage (VIN UVP)	OFF	L
Insertion delay	OFF	L
Overvoltage lockout (VIN OVP)	OFF	L
Transient overcurrent	ON	H
Circuit-breaker (persistent overcurrent followed by ITIMER expiry)	OFF	L
Fast-trip	OFF	L
Fault response mono-shot running (MODE = GND)	OFF	L
Fault response mono-shot expired (MODE = GND)	ON	H
IMON pin open (steady-state)	OFF	L
IMON pin short (steady-state)	OFF	L
FET health fault	OFF	L

Note

1. The SWEN is an open-drain pin but has a weak internal pullup to V_{INT}.
2. The SWEN can also be pulled up to an external supply. TI recommends to use a system standby rail which is derived from the input of the eFuse.

In a primary + secondary parallel configuration, the SWEN pin is used by the primary device to control the on and off transitions of the secondary devices. At the same time, it allows the secondary devices to communicate any faults or other condition which can prevent it from turning on to the primary device. Refer to *Fault Response and Indication ($\overline{FLT}$)* for more details.

To maintain state machine synchronization, the devices rely on SWEN level transitions as well as timing for handshakes. This ensures all the devices turn ON and OFF synchronously and in the same manner (for example, DVDT controlled or current limited start-up). There are also fail-safe mechanisms in the SWEN control and handshake logic to ensure the entire chain is turned off safely even if the primary device is unable to take control in case of a fault.

Note

TI recommends to keep the parasitic loading on the SWEN pin to a minimum to avoid synchronization timing issues.

7.3.8 Stacking Multiple eFuses for Unlimited Scalability

For systems needing higher current than supported by a single TPS1685x, multiple TPS1685x devices can be connected in parallel to deliver the total system current. Conventional eFuses can not share current equally between themselves during steady-state due to mismatches in their path resistances (which includes the individual device R_{DSON} variation from part to part, as well as the parasitic PCB trace resistance). This fact can lead to multiple problems in the system:

1. Some devices always carry higher current as compared to other devices, which can result in accelerated failures in those devices and an overall reduction in system operational lifetime.
2. As a result, thermal hotspots form on the board, devices, traces, and vias carrying higher current, leading to reliability concerns for the PCB. In addition, this problem makes thermal modeling and board thermal management more challenging for designers.
3. The devices carrying higher current can hit their individual circuit-breaker threshold prematurely even while the total system load current is lower than the overall circuit-breaker threshold. This action can lead to false tripping of the eFuse during normal operation. This has the effect of lowering the current-carrying capability of the parallel chain. In other words, the current rating of the parallel eFuse chain must be de-rated as compared to the sum of the current ratings of the individual eFuses. This de-rating factor is a function of the path resistance mismatch, the number of devices in parallel, and the individual eFuse circuit-breaker accuracy.

The need for de-rating has an adverse impact on the system design. The designer is forced to make one of these trade-offs:

1. Limit the operating load current of the system to below the derated current threshold of the eFuse chain. Essentially, it means lower platform capabilities than are supported by the power supply (PSU).
2. Increase the overall circuit-breaker threshold to allow the desired system load current to pass through without tripping. As a consequence, the power supply (PSU) must be oversized to deliver higher currents during faults to account for the de-grading of the overall circuit-breaker accuracy.

In either case, the system suffers from poor power supply utilization, which can mean sub-optimal system throughput or increased installation and operating costs, or both.

The TPS1685x uses a proprietary technique to address these problems and provide unlimited scalability of the solution by paralleling as many eFuses as needed. This is incorporated without unequal current sharing or any degradation in accuracy.

For this scheme to work correctly, the devices must be connected in the following manner:

- The SWEN pins of all the devices are connected together.
- The IMON pins of all the devices must be connected together. The R_{IMON} resistor value on the combined IMON pin can be calculated using Equation 11.

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \quad (11)$$

- The R_{ILIM} for each individual eFuse must be selected based on Equation 12.

$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \quad (12)$$

Where N = number of devices in parallel chain.

Note

The active current sharing scheme is engaged when the current through any eFuse while in steady-state exceeds the individual current sharing threshold set by the R_{ILIM} based on Equation 13.

$$R_{ILIM} = \frac{1.1 \times V_{IREF}}{3 \times G_{ILIM} \times I_{LIM(ACS)}} \quad (13)$$

The active current sharing scheme is disengaged when the total system current exceeds the system overcurrent (circuit-breaker) threshold ($I_{OCP(TOTAL)}$).

7.3.8.1 Current Balancing During Start-Up

The TPS1685x implements a proprietary current balancing mechanism during start-up, which allows multiple TPS1685x devices connected in parallel to share the inrush current and distribute the thermal stress across all the devices. This feature helps to complete a successful start-up with all the devices and avoid a scenario where some of the eFuses hit thermal shutdown prematurely. This in effect increases the inrush current capability of the parallel chain. The improved inrush performance makes it possible to support very large load capacitors on high current platforms without compromising the inrush time or system reliability.

7.3.9 Analog Junction Temperature Monitor (TEMP)

The device allows the system to monitor the junction temperature (T_J) accurately by providing an analog voltage on the TEMP pin which is proportional to the temperature of the die. This voltage can be connected to the ADC input of a host controller or eFuse with digital telemetry. In a multi-device parallel configuration, the TEMP outputs of all devices can be tied together. In this configuration, the TEMP signal reports the temperature of the hottest device in the chain.

7.3.10 Overtemperature Protection

The TPS1685x employs an internal thermal shutdown mechanism to protect itself when the internal FET becomes too hot to operate safely. When the TPS16851 detects thermal overload, it shuts down and remains latched-off until the device is power cycled or re-enabled. When the TPS16850 detects thermal overload, it remains off until it has cooled down sufficiently. Thereafter, the device remains off for an additional delay of t_{RST} after which it automatically retries to turn on if it is still enabled.

Table 7-3. Overtemperature Protection Summary

Device	Enter TSD	Exit TSD
TPS16851 (Latch-Off)	$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} VDD cycled to 0 V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$

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Table 7-3. Overtemperature Protection Summary (continued)

Device	Enter TSD	Exit TSD
TPS16850 (Auto-Retry)	$T_J \geq TSD$	$T_J < TSD - TSD_{HYS}$ t_{RST} timer expired or VDD cycled to 0 V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$

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7.3.11 Fault Response and Indication ($\overline{FLT}$)

Table 7-4 summarizes the device response to various fault conditions.

Table 7-4. Fault Summary

Event or Condition	Device Response	Fault Latched Internally	$\overline{FLT}$ Pin Status	Delay
Steady-state	None	N/A	H	
Inrush	None	N/A	H	
Overtemperature	Shutdown	Y	L	
Undervoltage (EN/UVLO)	Shutdown	N	H	
Undervoltage (VDD UVP)	Shutdown	N	H	
Undervoltage (VIN UVP)	Shutdown	N	H	
Overvoltage (VIN OVP)	Shutdown	N	H	
Transient overcurrent	None	N	H	
Persistent overcurrent (steady-state)	Circuit-Breaker	Y	L	t_{ITIMER}
Persistent overcurrent (start-up)	Current Limit	N	L	
Short-circuit (primary mode)	Fast-trip	Y	L	t_{FT}
Short-circuit (secondary mode)	Fast-trip followed by current limited Start-up	N	H	
ILIM pin open (steady-state)	Active current sharing loop always active	N	H	
ILIM pin short (steady-state)	Active current sharing loop disabled	N	H	
IMON pin open (steady-state)	Shutdown	Y	L	
IMON pin short (steady-state)	Shutdown (If I_{OUT} > I_{OC_BKP})	Y	L	30 µs
IREF pin open (steady-state)	Shutdown (if I_{OUT} > I_{OC_BKP})	Y	L	t_{ITIMER}
IREF pin short (steady-state)	Shutdown	Y	L	
ITIMER pin forced to high voltage	Shutdown (if I_{OUT} > I_{OCP} or I_{OUT} > I_{OC_BKP})	Y	L	t_{SPFAIL_TMR}
Start-up timeout	Shutdown	Y	L	t_{SU_TMR}
FET health fault (G-S)	Shutdown	Y	L	10 µs
FET health fault (G-D)	Shutdown	Y	L	
FET health fault (D-S)	Shutdown	N	L	t_{SU_TMR}
External fault (SWEN pulled low externally while device is not in UV or OV)	Shutdown	Y	L	

$\overline{FLT}$ is an open-drain pin and must be pulled up to an external supply.

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The device response after a fault varies based on the mode of operation:

1. During standalone or primary mode of operation (MODE = OPEN), the device latches a fault and follows the auto-retry or latch-off response as per the device selection. When the device turns on again, it follows the usual DVDT limited start-up sequence.
2. During the secondary mode of operation (MODE = GND), if the device detects any fault, it pulls the SWEN pin low momentarily to signal the event to the primary device and thereafter relies on the primary to take control of the fault response. However, if the primary device fails to register the fault, there i a failsafe mechanism in the secondary device to turn off the entire chain and enter a latch-off condition. Thereafter, the device can be turned on again only by power cycling VDD below $V_{UVP(F)}$ or by cycling EN/UVLO pin below $V_{SD(F)}$.

For faults that are latched internally, power cycling the part or pulling the EN/UVLO pin voltage below $V_{SD(F)}$ clears the fault and the pin is de-asserted. This action also clears the t_{RST} timer (auto-retry variants only). Pulling the EN/UVLO just below the UVLO threshold has no impact on the device in this condition. This is true for both latch-off and auto-retry variants.

7.3.12 Power Good Indication (PG)

Power Good indication is an active high output which is asserted high to indicate when the device is in steady-state and capable of delivering maximum power.

Table 7-5. PG Indication Summary

Event or Condition	FET Status	PG Pin Status	PG Delay
Undervoltage ($V_{EN} < V_{UVLO}$)	OFF	L	t_{PGD}
$V_{IN} < V_{UVP}$	OFF	L	
$V_{DD} < V_{UVP}$	OFF	L	
Overvoltage ($V_{IN} > V_{OVP}$)	OFF	L	t_{PGD}
Steady-state	ON	H	t_{PGA}
Inrush	ON	L	t_{PGA}
Transient overcurrent	ON	H	N/A
Circuit-breaker (persistent overcurrent followed by ITIMER expiry)	OFF	L (MODE = H) H (MODE = L)	t_{PGD} N/A
Fast-trip	OFF	L (MODE = H) H (MODE = L)	t_{PGD} N/A
Overtemperature	Shutdown	L (MODE = H) H (MODE = L)	t_{PGD} N/A

After power up, PG is pulled low initially. The device initiates an inrush sequence in which the gate driver circuit starts charging the gate capacitance from the internal charge pump. When the FET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the device is capable of delivering full power, the PG pin is asserted HIGH after a de-glitch time (t_{PGA}).

The PG is de-asserted if the FET is turned off at any time during normal operation. The PG de-assertion de-glitch time is t_{PGD}.

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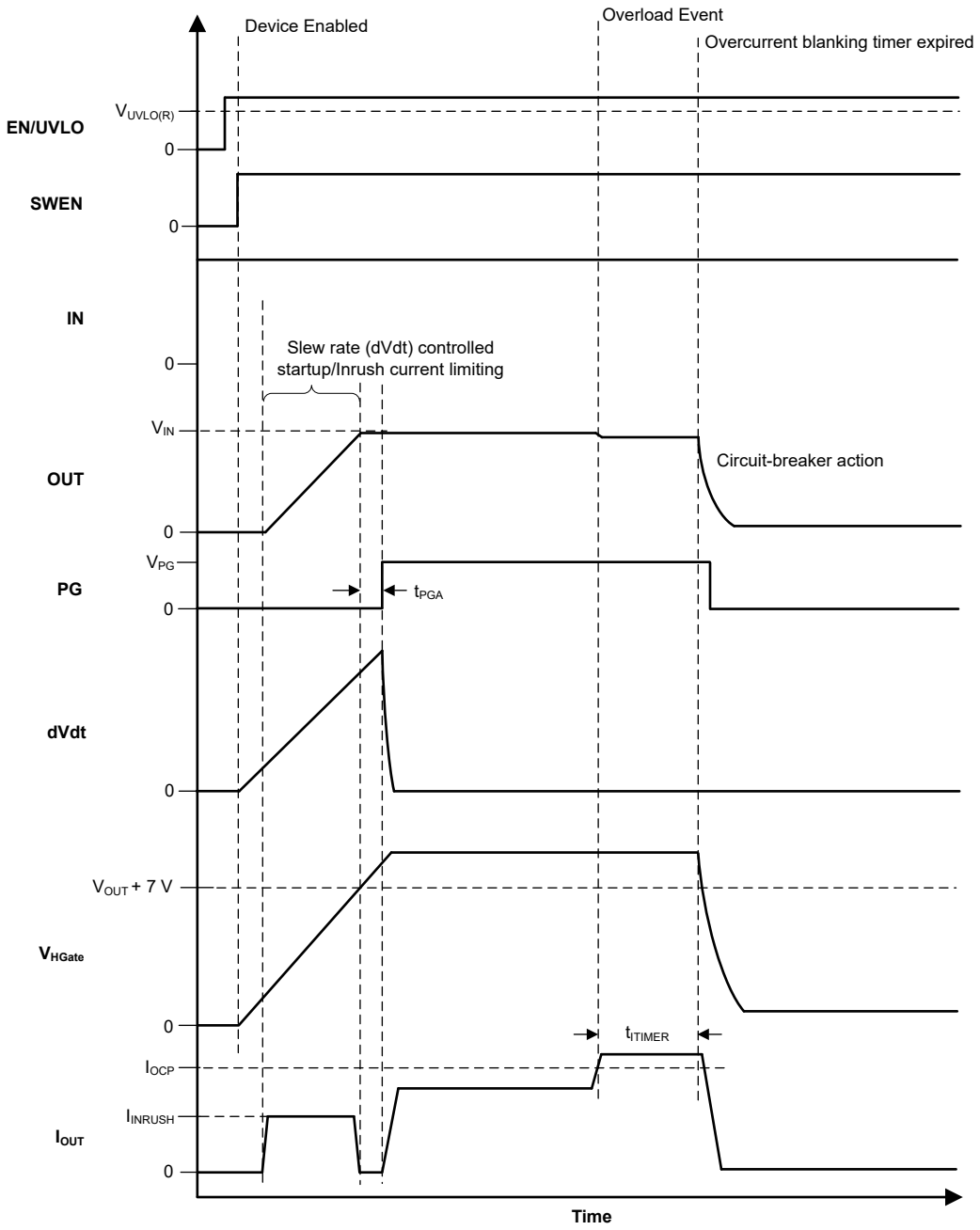

Figure 7-7. TPS1685x PG Timing Diagram

The PG is an open-drain pin and must be pulled up to an external supply.

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

When the device is used in secondary mode (MODE = GND) in conjunction with another TPS1685x device as a primary device in a parallel chain, it controls the PG assertion during start-up, but after the device reaches steady-state, it no longer has control over the PG de-assertion. Refer to the *Mode Selection (MODE)* for more details.

7.3.13 Output Discharge

The device has an integrated output discharge function which discharges the capacitors on the OUT pin using an internal constant current (I_{QOD}) to GND. The output discharge function is activated when the EN/UVLO is held low ($V_{SD(F)} < V_{EN} < V_{UVLO(F)}$) for a minimum interval (t_{QOD}). The output discharge function helps to rapidly remove the residual charge left on large output capacitors and prevents the bus from staying at some undefined voltage for extended periods of time. The output discharge is disengaged when $V_{OUT} < V_{FB}$ or if the device detects a fault.

The output discharge function can result in excessive power dissipation inside the device leading to an increase in junction temperature (T_J). The output discharge is disabled if the junction temperature (T_J) crosses TSD to avoid long-term degradation of the part.

Note

In a primary+secondary parallel configuration, TI recommends to hold EN/UVLO voltage below the $V_{UVLO(F)}$ threshold of the secondary device to activate output discharge for all the devices in the chain.

7.3.14 FET Health Monitoring

The TPS1685x can detect and report certain conditions which are indicative of a failure of the power path FET. If undetected or unreported, these conditions can compromise system performance by not providing power to the load correctly or by not providing the necessary level of protection. After a FET failure is detected, the TPS1685x tries to turn off the internal FET by pulling the gate low and asserts the $\overline{FLT}$ pin.

- **D-S short:** D-S short can result in a constant uncontrolled power delivery path formed from source to load, either due to a board assembly defect or due to internal FET failure. This condition is detected at start-up by checking if $V_{IN-OUT} < V_{DSFLT}$ before the FET is turned ON. If yes, the device engages the internal output discharge to try and discharge the output. If the V_{OUT} does not discharge below V_{FB} within a certain allowed interval, the device asserts the $\overline{FLT}$ pin.
- **G-D short:** The TPS1685x detects this kind of FET failure at all times by checking if the gate voltage is close to V_{IN} even when the internal control logic is trying to hold the FET in OFF condition.
- **G-S short:** The TPS1685x detects this kind of FET failure during start-up by checking if the FET G-S voltage fails to reach the necessary overdrive voltage within a certain timeout period (t_{SU_TMR}) after the gate driver is turned ON. While in steady-state, if the G-S voltage becomes low before the controller logic has signaled to the gate driver to turn off the FET, it is latched as a fault.

7.3.15 Single Point Failure Mitigation

The TPS1685x relies on the proper component connections and biasing on the IMON, IREF, and ITIMER pins to provide overcurrent and short-circuit protection under all circumstances. As an added safety measure, the device uses the following mechanisms to ensure that the device provides some form of overcurrent protection even if any of these pins are not connected correctly in the system or the associated components have a failure in the field.

7.3.15.1 IMON Pin Single Point Failure

- **IMON pin open:** In this case, the IMON pin voltage is internally pulled up to a higher voltage and exceeds the threshold (V_{IREF}), causing the part to perform a circuit-breaker action even if there is no significant current flowing through the device.
- **IMON pin shorted to GND directly or through a very low resistance:** In this case, the IMON pin voltage is held at a low voltage and is not allowed to exceed the threshold (V_{IREF}) even if there is significant current flowing through the device, thereby rendering the primary overcurrent protection mechanism ineffective. The device relies on an internal overcurrent sense mechanism to provide some protection as a backup. If the device detects that the backup current sense threshold (I_{OC_BKP}) is exceeded but at the same time the primary overcurrent detection on IMON pin fails, it triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.

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7.3.15.2 IREF Pin Single Point Failure

- **IREF pin open or forced to higher voltage:** In this case, the IREF pin (V_{IREF}) is pulled up internally or externally to a voltage which is higher than the target value as per the recommended I_{OCP} or I_{LIM} calculations, preventing the primary circuit-breaker, active current limit, and short-circuit protection from getting triggered even if there is significant current flowing through the device. The device relies on an internal overcurrent detection mechanism to provide some protection as a backup. If the device detects that the backup overcurrent threshold is exceeded but at the same the primary overcurrent or short-circuit detection on IMON pin fails, it triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.
- **IREF pin shorted to GND:** In this case, the V_{IREF} threshold is set to 0 V, causing the part to perform active current limit or circuit-breaker action even if there is no significant current flowing through the device.

7.3.15.3 ITIMER Pin Single Point Failure

- **ITIMER pin open or short to GND:** In this case, the ITIMER pin is already discharged below $V_{ITIMERTHR}$ and hence indicates overcurrent blanking timer expiry instantaneously after an overcurrent event and triggers a circuit-breaker action without any delay.
- **ITIMER pin forced to some voltage higher than $V_{ITIMERTHR}$:** In this case, the ITIMER pin is unable to discharge below $V_{ITIMERTHR}$ and hence fails to indicate overcurrent blanking timer expiry, thereby rendering the circuit-breaker mechanism ineffective. The device relies on a backup overcurrent timer mechanism to provide some protection as a backup. If the device detects an overcurrent event on either the IMON pin or the backup overcurrent detection circuit, the device engages the internal backup time and after the timer expires ($t_{SPFLTMR}$), it latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.

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7.4 Device Functional Modes

The features of the device depend on the operating mode. Table 7-6 and Table 7-7 summarize the device functional modes.

Table 7-6. Device Functional Modes Based on EN/UVLO Pin

Pin: EN/UVLO	Device State	Output Discharge
> $V_{UVLO(R)}$	Fully ON	Disabled
> $V_{SD(F)}$, < $V_{UVLO(F)}$ (< t_{QOD})	FET OFF	Disabled
> $V_{SD(F)}$, < $V_{UVLO(F)}$ (> t_{QOD})	FET OFF	Enabled
< $V_{SD(F)}$	Shutdown	Disabled

Table 7-7. Device Functional Modes Based on MODE Pin

Pin: MODE	Device Configuration
Open	Primary or standalone
GND	Secondary

Table 7-8. Device Functional Modes Based on Resistor at SFT_SEL Pin

I_{SFT_SEL}	SFT_SEL pin	MODE pin
8 × I_{OCP}	R_{SFT_SEL} <95kΩ	Open
2.5 × I_{OCP}	105kΩ < R_{SFT_SEL} < 195kΩ	Open
2.8 × I_{OCP}	105kΩ < R_{SFT_SEL} < 195kΩ	GND
2 × I_{OCP}	205kΩ < R_{SFT_SEL} < 295kΩ	Open
2.26 × I_{OCP}	205kΩ < R_{SFT_SEL} < 295kΩ	GND
1.5 × I_{OCP}	305kΩ < R_{SFT_SEL}	Open
1.71 × I_{OCP}	305kΩ < R_{SFT_SEL}	GND

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS1685x is a high voltage and current eFuse that is typically used for power rail protection applications. The device operates from 9 V to 80 V with input overvoltage and adjustable undervoltage protection. The device provides ability to control inrush current and offers protection against overcurrent and short-circuit conditions. The device can be used in a variety of systems such as server motherboards, add-on cards, graphics cards, accelerator cards, enterprise switches, routers, and so forth. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirements. Additionally, a spreadsheet design tool, *TPS1685x Design Calculator* is available in the web product folder.

8.1.1 Single Device, Standalone Operation

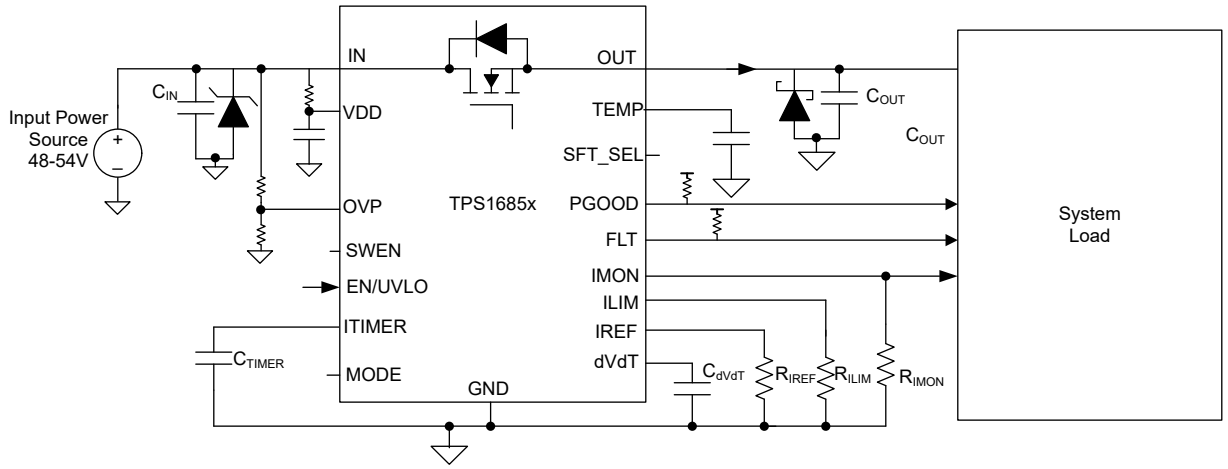

Figure 8-1. Single Device, Standalone Operation

Note

The MODE pin is left OPEN to configure for standalone operation.

Other variations:

1. The IREF pin can be driven from an external reference voltage source.
2. In a host MCU controlled system, EN/UVLO can be connected to a GPIO pin to control the device. IMON pin voltage can be monitored using an ADC. The host MCU can use a DAC to drive IREF to change the current limit threshold dynamically.
3. The device can be used as a simple high current load switch without adjustable overcurrent or fast-trip protection by tying the ILIM and IMON pins to GND and leaving the IREF pin open. The inrush current protection, fixed fast-trip and internal fixed overcurrent protection are still active in this condition.

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8.1.2 Multiple Devices, Parallel Connection

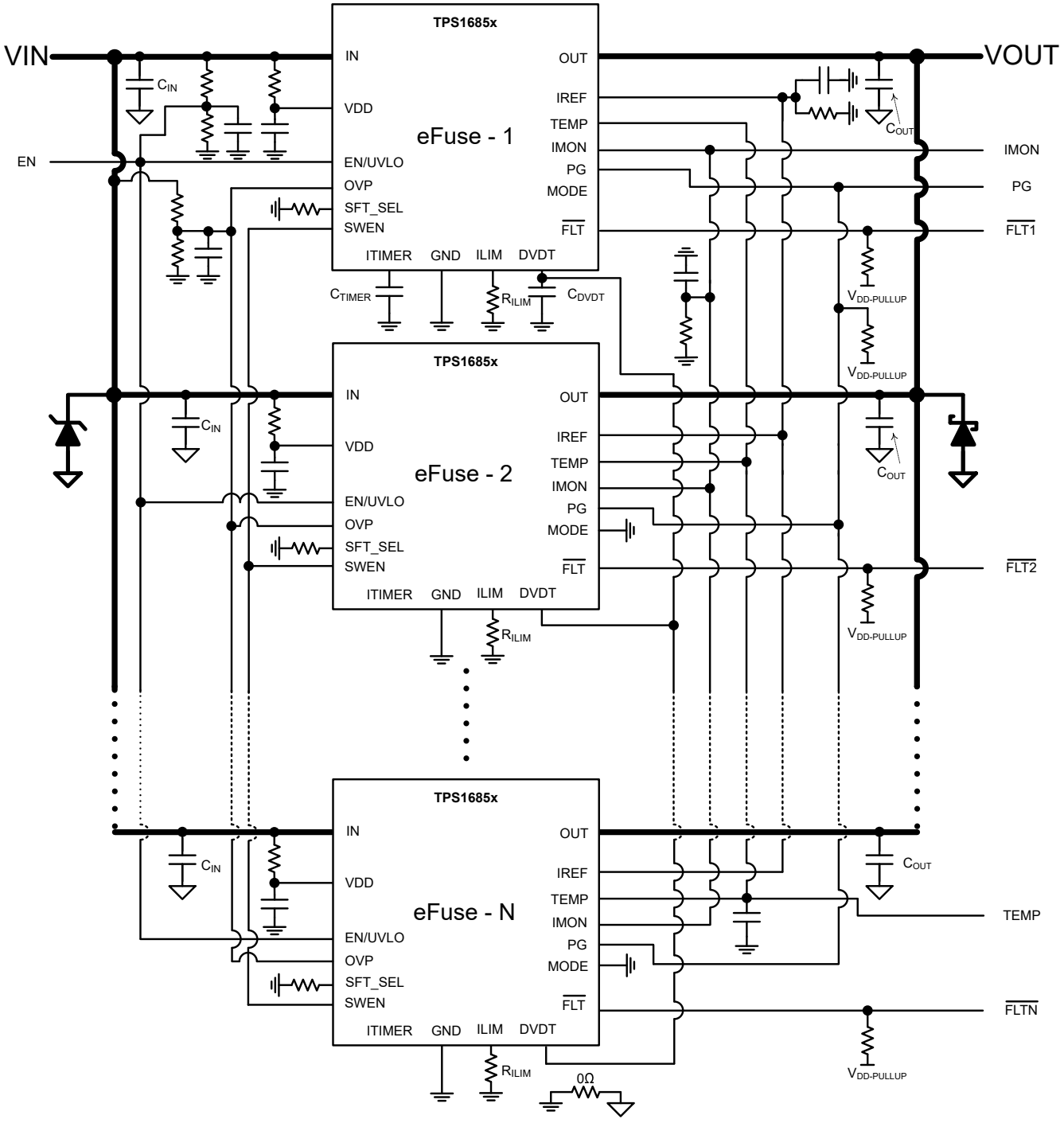

Figure 8-2. Devices Connected in Parallel for Higher Current Capability

In this configuration, one TPS1685x device is designated as the primary device and controls the other TPS1685x devices in the chain which are designated as secondary devices. This configuration is achieved by connecting the primary device as follows:

1. VDD is connected to IN through an R-C filter.
2. MODE pin is left OPEN.
3. ITIMER is connected through capacitor to GND.

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4. DVDT is connected through capacitor to GND.
5. IREF is connected through resistor to GND.
6. IMON is connected through resistor to GND.
7. ILIM is connected through resistor to GND.
8. SWEN is pulled up to a 3.3-V to 5-V standby rail. This rail must be powered up independent of the eFuse.

The secondary devices must be connected in the following manner:

1. VDD is connected to IN through a R-C filter.
2. MODE pin is connected to GND.
3. ITIMER pin is left OPEN.
4. ILIM is connected through resistor to GND.

The following pins of all devices must be connected together:

1. IN
2. OUT
3. EN/UVLO
4. OVP
5. DVDT
6. SWEN
7. PG
8. IMON
9. IREF

In this configuration, all the devices are powered up and enabled simultaneously.

Power up: After power up or enable, all devices initially hold their SWEN low till the internal blocks are biased and initialized correctly. After that, each device releases its own SWEN. After all devices have released their SWEN, the combined SWEN goes high and the devices are ready to turn on their respective FETs at the same time.

Inrush: During inrush, because the DVDT pins are tied together to a single DVDT capacitor all the devices turn on the output with the same slew rate (SR). Choose the common DVDT capacitor (C_{DVDT}) as per the following Equation 14 and Equation 15.

$$SR(V/ms) = \frac{I_{INRUSH}(A)}{C_{LOAD}(mF)} \quad (14)$$

$$C_{DVDT}(nF) = \frac{48}{SR(V/ms)} \quad (15)$$

In this condition, the internal balancing circuit ensures that the load current is shared among all devices during start-up. This action prevents a situation where some devices turn on faster than others and experience more thermal stress as compared to other devices. This can potentially result in premature or partial shutdown of the parallel chain, or even SOA damage to the devices. The current balancing scheme ensures the inrush capability of the chain scales according to the number of devices connected in parallel, thereby ensuring successful start-up with larger output capacitances or higher loading during start-up.

All devices hold their respective PG signals low during start-up. After the output ramps up fully and reaches steady-state, each device releases its own PG pulldown. Because the DVDT pins of all devices are tied together, the internal gate high detection of all devices is synchronized. There can be some threshold or timing mismatches between devices leading to PG assertion in a staggered manner. However, since the PG pins of all devices are tied together, the combined PG signal becomes high only after all devices have released their PG pulldown. This signal is sent to the downstream loads to allow power to be drawn.

Steady-state: During steady-state, all devices share current equally using the active current sharing mechanism which actively regulates the respective device R_{DSON} to evenly distribute current across all the devices in the parallel chain.

Overcurrent during steady-state: The circuit-breaker threshold for the parallel chain is based on the total system current rather than the current flowing through individual devices. This is done by connecting the IMON pins of all the devices together. Similarly, the IREF pins of all devices are tied together and connected to a single R_{IREF} (or an external V_{IREF} source) to generate a common reference for the overcurrent protection block in all the devices. This action helps minimize the contribution of I_{IREF} variation and R_{IREF} tolerance to the overall mismatch in overcurrent threshold between devices. In this case, choose the combined R_{IMON} as per the following Equation 16:

$$R_{IMON} = \frac{I_{IREF} \times R_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \quad (16)$$

The R_{ILIM} value for each individual eFuse must be selected based on the following Equation 17.

$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \quad (17)$$

Where N = number of devices in parallel chain.

Other variations:

The IREF pin can be driven from an external voltage reference (V_{IREF}).

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \quad (18)$$

During an overcurrent event, the overcurrent detection of all the devices is triggered simultaneously. This in turn triggers the overcurrent blanking timer (ITIMER) on each device. However, only the primary device uses the ITIMER expiry event as a trigger to pull the SWEN low for all the devices, thereby initiating the circuit-breaker action for the whole chain. This mechanism ensures that mismatches in the current distribution, overcurrent thresholds and ITIMER intervals among the devices do not degrade the accuracy of the circuit-breaker threshold of the complete parallel chain or the overcurrent blanking interval.

However, the secondary devices also start their backup overcurrent timer and can trigger the shutdown of the whole chain if the primary device fails to do so within a certain interval.

Severe overcurrent (short-circuit): If there is a severe fault at the output (for example, output shorted to ground with a low impedance path) during steady-state operation, the current builds up rapidly to a high value and triggers the fast-trip response in each device. The devices use two thresholds for fast-trip protection – a user-adjustable threshold I_{SFT} as well as a fixed threshold I_{FFT} . After the fast-trip, the devices enter into a latch-off fault condition till the device is power cycled or re-enabled or expires the auto-retry timer (only for auto-retry variants).

8.2 Typical Application: 54V Power Path Protection in Data Center Servers

This design example considers a 54V system operating voltage with a tolerance of ±10%. The maximum steady-state load current is 80A. If the load current exceeds 85A, the eFuse circuit must allow transient overload currents up to a 3ms interval. For persistent overloads lasting longer than that, the eFuse circuit must break the circuit and then latch-off. The eFuse circuit must charge a bulk capacitance of 1mF. Figure 8-3 shows the application schematic for this design example.

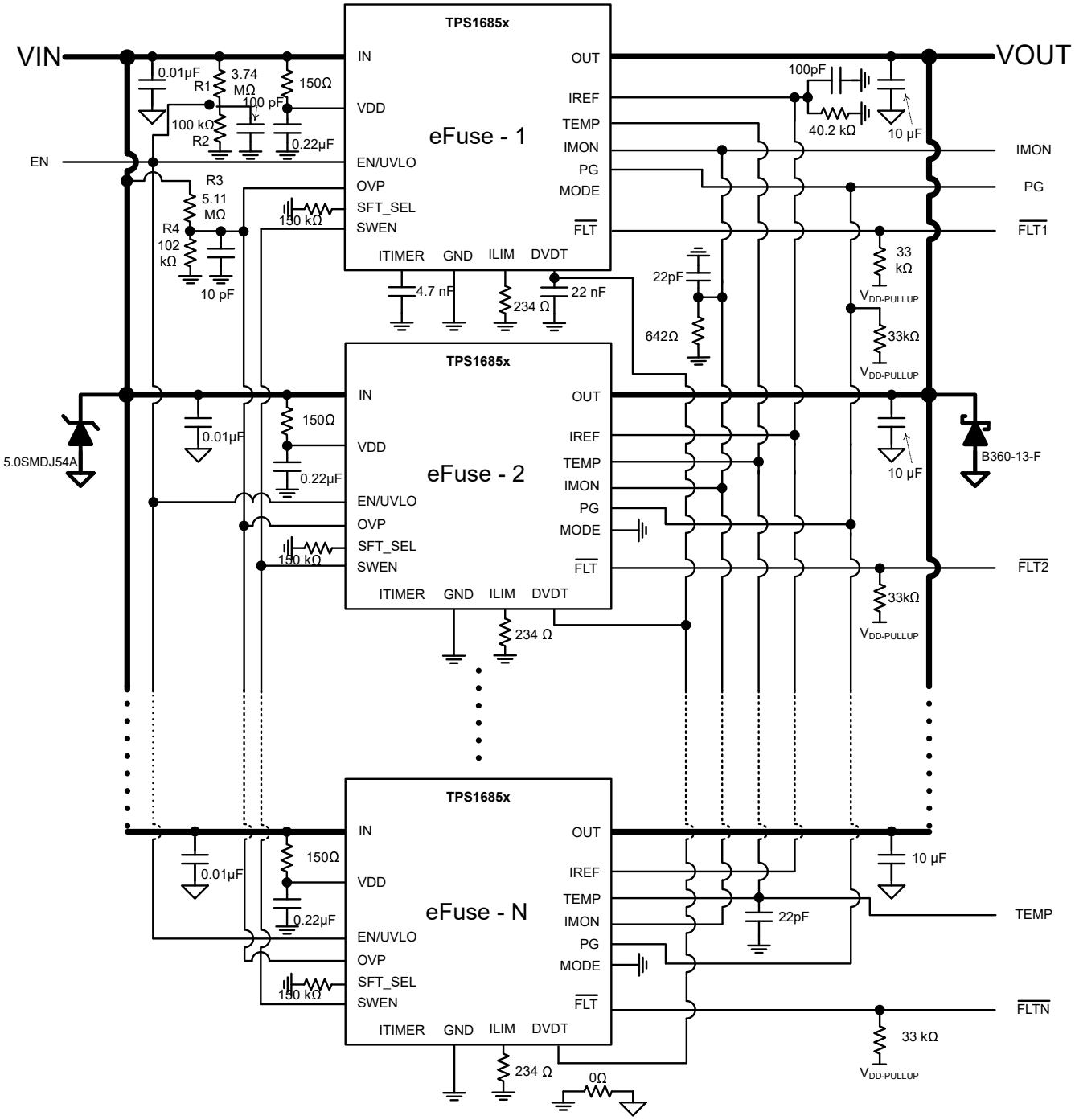

Figure 8-3. Application Schematic for a 54V, 4.3kW Power Path Protection Circuit

8.2.1 Design Requirements

Table 8-1 shows the design parameters for this application example.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range (V_{IN})	48.6V – 59.4V
Maximum DC load current ($I_{OUT(max)}$)	80A
Maximum output capacitance (C_{LOAD})	1mF
Maximum ambient temperature	55°C
Transient overload blanking timer	3ms
Output voltage slew rate	2.2V/ms
Need to survive a “hot-short” on output condition ?	Yes
Need to survive a “power up into short” condition?	Yes
Can a board be hotplugged in or power cycled?	Yes
Load current monitoring needed?	Yes
Fault response	Latch-off

8.2.2 Detailed Design Procedure

- **Determining the number of eFuse devices to be used in parallel**

  By factoring in a small variation in the junction to ambient thermal resistance ($R_{\theta JA}$), a single TPS1685x eFuse is rated at a maximum steady state DC current of 20A with a maximum junction temperature of less than 125°C. Therefore, Equation 19 can be used to calculate the number of devices (N) to be in parallel to support the maximum steady state DC load current ($I_{LOAD(max)}$), for which the solution must be designed.

$$N \geq \frac{I_{OUT(max)}\,(A)}{20\ A} \tag{19}$$

  According to Table 8-1, $I_{OUT(max)}$ is 80A. Therefore, 4 TPS1685 eFuses are connected in parallel.

- **Setting up the primary and secondary devices in a parallel configuration**

  The MODE pin is used to configure one TPS1685x eFuse as the primary device in a parallel chain along with the other TPS1685x eFuses as the secondary devices. As a result, some of the TPS1685 pin functions can be changed to facilitate primary and secondary configuration as described in *Multiple Devices, Parallel Connection*.

  Leaving the pin open configures the corresponding device as the primary one. For the secondary devices, this pin must be connected to GND.

- **Selecting the C_{DVDT} capacitor to control the output slew rate and start-up time**

  A capacitor (C_{DVDT}) must be added at the DVDT pin to GND to set the required value of slew rate. Equation 20 is used to compute the value of C_{DVDT}. The DVDT pins of all the eFuses in a parallel chain must be connected together.

$$C_{DVDT}(nF) = \frac{48}{V_{IN}(V)/T_{ss}(ms)} \tag{20}$$

  To get slew rate of 2.2V/ms , as per above equation we get C_{DVDT} as 21.82nF. We can keep nearby standard value of 22nF.

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- **Selecting the R_{IREF} resistor to set the reference voltage for overcurrent protection and active current sharing**

  In this parallel configuration, the IREF internal current source (I_{IREF}) of the primary eFuse interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage (V_{IREF}) for the overcurrent protection and active current sharing blocks. When the voltage at the IMON pin (V_{IMON}) is used as an input to an ADC to monitor the system current or to implement the Platform Power Control (Intel PSYS) functionality inside the VR controller, V_{IREF} must be set to half of the maximum voltage range of the ISYS_IN input of the controller. This action provides the necessary headroom and dynamic range for the system to accurately monitor the load current up to the fast-trip threshold (2 × I_{OCP}). Equation 21 is used to calculate the value of R_{IREF}.

$$V_{IREF} = I_{IREF} \times R_{IREF} \quad (21)$$

  In this design example, V_{IREF} is set at 1V. With I_{IREF} = 25µA (typical), we can calculate the target R_{IREF} to be 40kΩ. The closest standard value of R_{IREF} is 40.2kΩ with 0.1% tolerance and power rating of 100mW. For improved noise immunity, place a 100pF ceramic capacitor from the IREF pin to GND.

Note

Maintain V_{IREF} within the recommended voltage to ensure proper operation of overcurrent detection circuit.

- **Selecting the R_{IMON} resistor to set the overcurrent (circuit-breaker) and fast-trip thresholds during steady-state**

  TPS1685x eFuse responds to the output overcurrent conditions during steady-state by turning off the output after a user-adjustable transient fault blanking interval. This eFuse continuously senses the total system current (I_{OUT}) and produces a proportional analog current output (I_{IMON}) on the IMON pin. This generates a voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) in response to the load current, which is defined as Equation 22.

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \quad (22)$$

  G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT}), whose typical value is 18.2µA/A. The overcurrent condition is detected by comparing the V_{IMON} against the V_{IREF} as a threshold. The circuit-breaker threshold during steady-state (I_{OCP}) can be calculated using Equation 23.

$$I_{OCP(TOTAL)} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \quad (23)$$

  In this design example, $I_{OCP(TOTAL)}$ is considered as 85A, and R_{IMON} can be calculated to be 646.4Ω with G_{IMON} as 18.2µA/A and V_{IREF} as 1V. The nearest value of R_{IMON} is 642Ω with 0.1% tolerance and power rating of 100mW. For noise reduction, place a 22pF ceramic capacitor across the IMON pin and GND.

Note

System output current (I_{OUT}) must be considered when selecting R_{IMON}, not the current carried by each device.

- **Selecting the R_{ILIM} resistor to set active sharing threshold during steady-state**

  R_{ILIM} is used in setting up the active current sharing threshold during steady-state. Each device continuously monitors the current flowing through it (I_{DEVICE}) and outputs a proportional analog output current on its own ILIM pin. This in turn produces a proportional voltage (V_{ILIM}) across the respective ILIM pin resistor (R_{ILIM}), which is expressed as Equation 24.

$$V_{ILIM} = I_{DEVICE} \times G_{ILIM} \times R_{ILIM} \quad (24)$$

G_{ILIM} is the current monitor gain (I_{ILIM} : I_{DEVICE}), whose typical value is 20µA/A.

– ***Active current sharing during steady-state*:** This mechanism operates only after the device reaches steady-state and acts independently by comparing its own load current information (V_{ILIM}) with the Active Current Sharing reference ($CLREF_{LIN}$) threshold, defined as Equation 25.

$$CLREF_{LIN} = \frac{1.1 \times V_{IREF}}{3} \quad (25)$$

Therefore, R_{ILIM} must be calculated using Equation 26 to define the active current sharing threshold as $I_{OCP(TOTAL)}$/N, where N is the number of devices in parallel. Using N = 4, R_{IMON} = 642Ω, and Equation 26, R_{ILIM} can be calculated to be 235.4Ω. The closest standard value of 234Ω with 0.1% tolerance and power rating of 100mW resistances are selected as R_{ILIM} for each device.

$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \quad (26)$$

Note

To determine the value of R_{ILIM}, Equation 27 must be used if a different threshold for active current sharing ($I_{LIM(ACS)}$) than I_{OCP}/N is desired.

$$R_{ILIM} = \frac{1.1 \times V_{IREF}}{3 \times G_{ILIM} \times I_{LIM(ACS)}} \quad (27)$$

- **Selecting the C_{ITIMER} capacitor to set the overcurrent blanking timer**

An appropriate capacitor must be connected at the ITIMER pin to ground of the primary or standalone device to adjust the duration for which the load transients above the circuit-breaker threshold are allowed. The transient overcurrent blanking interval can be calculated using Equation 28.

$$t_{ITIMER}(ms) = \frac{C_{ITIMER}(nF) \times \Delta V_{ITIMER}(V)}{I_{ITIMER}(\mu A)} \quad (28)$$

Where t_{ITIMER} is the transient overcurrent blanking timer and C_{ITIMER} is the capacitor connected between ITIMER pin of the primary device and GND. I_{ITIMER} = 2µA (typical) and ΔV_{ITIMER} = 1.3V (typical). A 4.7nF capacitor with 10% tolerance and DC voltage rating of 25V is used as the C_{ITIMER} for the primary device in this design, which results in 3ms of t_{ITIMER}. The ITIMER pin for all the secondary devices should be left open.

- **Selecting the resistors to set the undervoltage lockout threshold**

The undervoltage lockout (UVLO) threshold is adjusted by employing the external voltage divider network of R_1 and R_2 connected between IN, EN/UVLO, and GND pins of the device as described in Undervoltage protection section. The resistor values required for setting up the UVLO threshold are calculated using Equation 29.

$$V_{IN(UV)} = V_{UVLO(R)} \frac{R_1 + R_2}{R_2} \quad (29)$$

To minimize the input current drawn from the power supply, TI recommends using higher resistance values for R_1 and R_2. From the device electrical specifications, UVLO rising threshold $V_{UVLO(R)}$ = 1.2V. From the design requirements, V_{INUVLO} = 46V. First choose the value of R_1 = 3.74MΩ and use Equation 29 to calculate R_2 = 100kΩ. Use the closest standard 1 % resistor values: R_1 = 3.74MΩ and R_2 = 100kΩ. For noise reduction, place a 100pF ceramic capacitor across the EN/UVLO pin and GND.

- **Selecting the resistors to set the overvoltage lockout threshold**

The overvoltage lockout (OVLO) threshold is adjusted by employing the external voltage divider network of R_3 and R_4 connected between IN, OVLO, and GND pins of the device as described in overvoltage protection section. The resistor values required for setting up the OVLO threshold are calculated using below equation.

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$$V_{IN(OV)} = V_{OVLO(R)}\frac{R_3 + R_4}{R_4} \quad (30)$$

To minimize the input current drawn from the power supply, TI recommends using higher resistance values for R_3 and R_4. From the device electrical specifications, OVLO rising threshold $V_{OVLO(R)}$ = 1.164V. From the design requirements, V_{INOVLO} = 60V. First choose the value of R_1 = 5.11MΩ and use Equation 29 to calculate R_3 = 101kΩ. Use the closest standard 1% resistor values: R_3 = 5.11MΩ and R_4 = 102kΩ. For noise reduction, place a 10pF ceramic capacitor across the OVLO pin and GND.

- **Selecting the R-C filter between VIN and VDD**

  VDD pin is intended to power the internal control circuitry of the eFuse with a filtered and stable supply, not affected by system transients. Therefore, use an R (150Ω) – C (0.22µF) filter from the input supply (IN pin) to the VDD pin. This helps to filter out the supply noises and to hold up the controller supply during severe faults such as short-circuit at the output. In a parallel chain, this R-C filter must be employed for each device.

- **Selecting the pullup resistors and power supplies for PG, $\overline{FLT}$,**

  $\overline{FLT}$, PG, are the open drain outputs. If these logic signals are used, the corresponding pins must be pulled up to an appropriate supply rail voltage through 33kΩ pullup resistances.

- **Selection of TVS diode at input and Schottky diode at output**

  In the case of a short circuit and overload current limit when the device interrupts a large amount of current instantaneously, the input inductance generates a positive voltage spike on the input, whereas the output inductance creates a negative voltage spike on the output. The peak amplitudes of these voltage spikes (transients) are dependent on the value of inductance in series with the input or output of the device. Such transients can exceed the absolute maximum ratings of the device and eventually lead to failures due to electrical overstress (EOS) if appropriate steps are not taken to address this issue. Typical methods for addressing this issue include:

  1. Minimize lead length and inductance into and out of the device.
  2. Use a large PCB GND plane.
  3. Addition of the Transient Voltage Suppressor (TVS) diodes to clamp the positive transient spike at the input.
  4. Using Schottky diodes across the output to absorb negative spikes.

  Refer to *TVS Clamping in Hot-Swap Circuits* , *Selecting TVS Diodes in Hot-Swap and ORing Applications*, TVS Diode recommendation tool for details on selecting an appropriate TVS diode and the number of TVS diodes to be in parallel to effectively clamp the positive transients at the input below the absolute maximum ratings of the IN pin (20V). These TVS diodes also help to limit the transient voltage at the IN pin during the Hot Plug event. Four (4) SMDJ54A are used in parallel in this design example.

Note

Maximum Clamping Voltage V_C specification of the selected TVS diode at I_{pp} (10/1000µs) (V) must be lower than the absolute maximum rating of the power input (IN) pin for safe operation of the eFuse.

Selection of the Schottky diodes must be based on the following criteria:

– The non-repetitive peak forward surge current (I_{FSM}) of the selected diode must be more than the fast-trip threshold (2 × $I_{OCP(TOTAL)}$). Two or more Schottky diodes in parallel must be used if a single Schottky diode is unable to meet the required I_{FSM} rating. Equation 31 calculates the number of Schottky diodes ($N_{Schottky}$) that must be in parallel.

$$N_{Schottky} > \frac{2 \times I_{OCP(TOTAL)}}{I_{FSM}} \quad (31)$$

– Forward Voltage Drop (V_F) at near to I_{FSM} must be as small as possible. Ideally, the negative transient voltage at the OUT pin must be clamped within the absolute maximum rating of the OUT pin (–5V).

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  - DC Blocking Voltage (V_{RM}) must be more than the maximum input operating voltage.
  - Leakage current (I_R) must be as small as possible.

  4 B360-13-F are used in parallel in this design example.

- **Selecting C_{IN} and C_{OUT}**

  TI recommends to add ceramic bypass capacitors to help stabilize the voltages on the input and output. The value of C_{IN} must be kept small to minimize the current spike during hot-plug events. For each device, 0.01µF of C_{IN} is a reasonable target. Because C_{OUT} does not get charged during hot-plug, a larger value such as 10µF can be used at the OUT pin of each device.

8.2.3 Application Curves

All the waveforms below are captured on an evaluation setup with four TPS1685 eFuses in parallel. All the pullup supplies are derived from a separate standby rail.

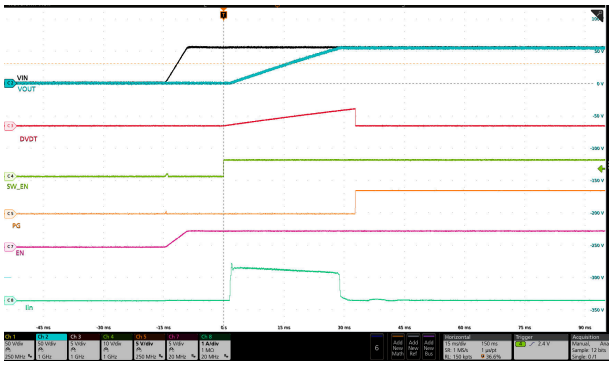

Figure 8-4. V_{IN} Ramped From 0V to 54V

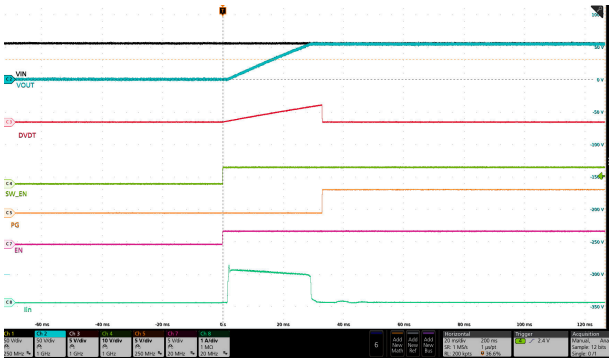

Figure 8-5. Start-Up With EN/UVLO

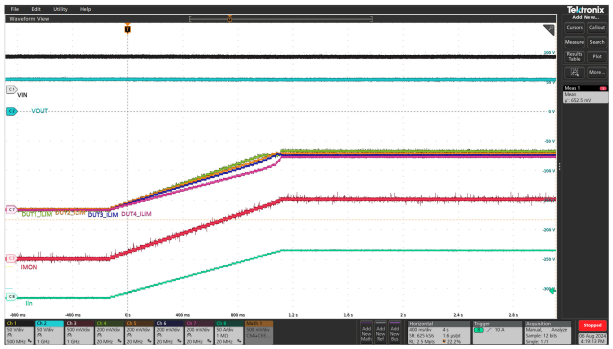

Figure 8-6. Active Current Sharing

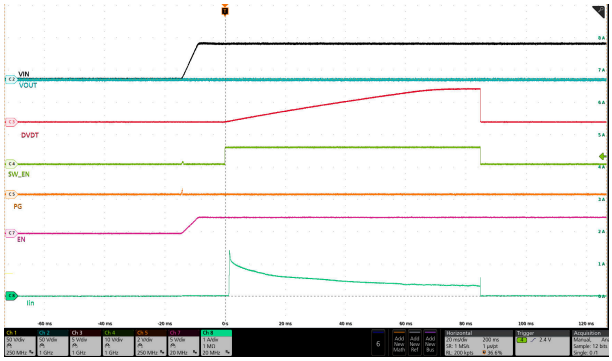

Figure 8-7. Power Up Into Short: V_{IN} = 54V, EN/UVLO Stepped Up From 0V to 3V

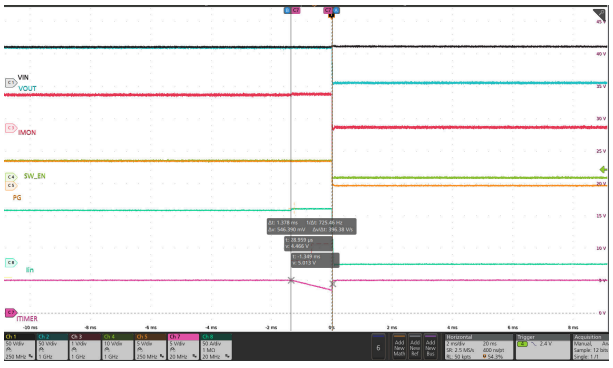

Figure 8-8. Circuit-Breaker Response

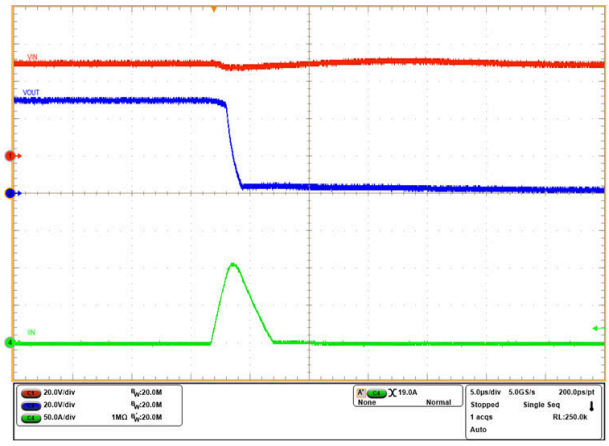

Figure 8-9. Output Hot-Short Response

8.3 Power Supply Recommendations

The TPS1685x devices are designed for a supply voltage in the range of 9V to 80V on the IN and VDD pins. TI recommends using a minimum capacitance of 0.1 µF on the IN pin of each device in parallel chain to avoid coupling of high slew rates during hot plug events. TI also recommends using an R-C filter from the input supply to the VDD pin on each device in parallel chain to filter out supply noise and to hold up the controller supply during severe faults such as short-circuit.

8.3.1 Transient Protection

In the case of a short-circuit or circuit-breaker event when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor of 10µF or higher at the OUT pin very close to the device.
- Connect a ceramic capacitor C_{IN} = 0.1 µF or higher at the IN pin very close to the device to dampen the rise time of input transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

The approximate value of input capacitance can be estimated with Equation 32.

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (32)$$

where

V_{IN} is the nominal supply voltage.

I_{LOAD} is the load current.

L_{IN} equals the effective inductance seen looking into the source.

C_{IN} is the capacitance present at the input.

- Some applications can require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

The circuit implementation with optional protection components is shown in Figure 8-10.

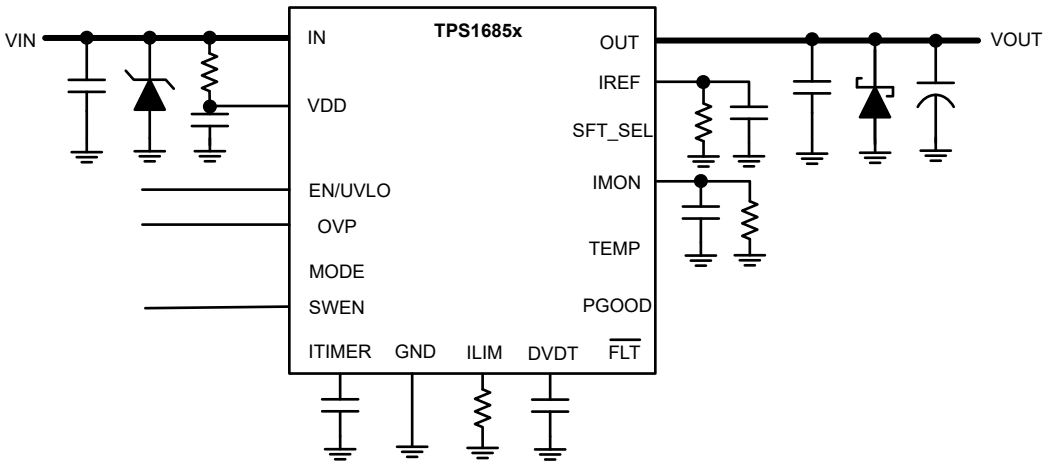

Figure 8-10. Circuit Implementation with Optional Protection Components

8.3.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing

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- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

8.4 Layout

8.4.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- For all applications, TI recommends a ceramic decoupling capacitor of 10µF or greater between the OUT terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure below for a PCB layout example.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- The IN and OUT pins are used for Heat Dissipation. Connect to as much copper area as possible with thermal vias.
- Locate the following support components close to their connection pins:
  - R_{ILIM}
  - R_{IMON}
  - C_{IMON}
  - R_{IREF}
  - C_{IREF}
  - C_{dVdT}
  - C_{ITIMER}
  - C_{IN}
  - C_{OUT}
  - C_{VDD}
  - Resistors for the EN/UVLO pin and OVP pin
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the C_{IN}, C_{OUT}, C_{VDD}, R_{IREF}, C_{IREF}, R_{ILIM}, R_{IMON}, C_{IMON}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit, overcurrent blanking interval and soft-start timing. These traces must not have any coupling to switching signals on the board.
- Because the IMON, ILIM, IREF and ITIMER pins directly control the overcurrent protection behavior of the device, the PCB routing of these nodes must be kept away from any noisy (switching) signals.
- TI recommends to keep the parasitic loading on SWEN pin to a minimum to avoid synchronization issues.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.

8.4.2 Layout Example

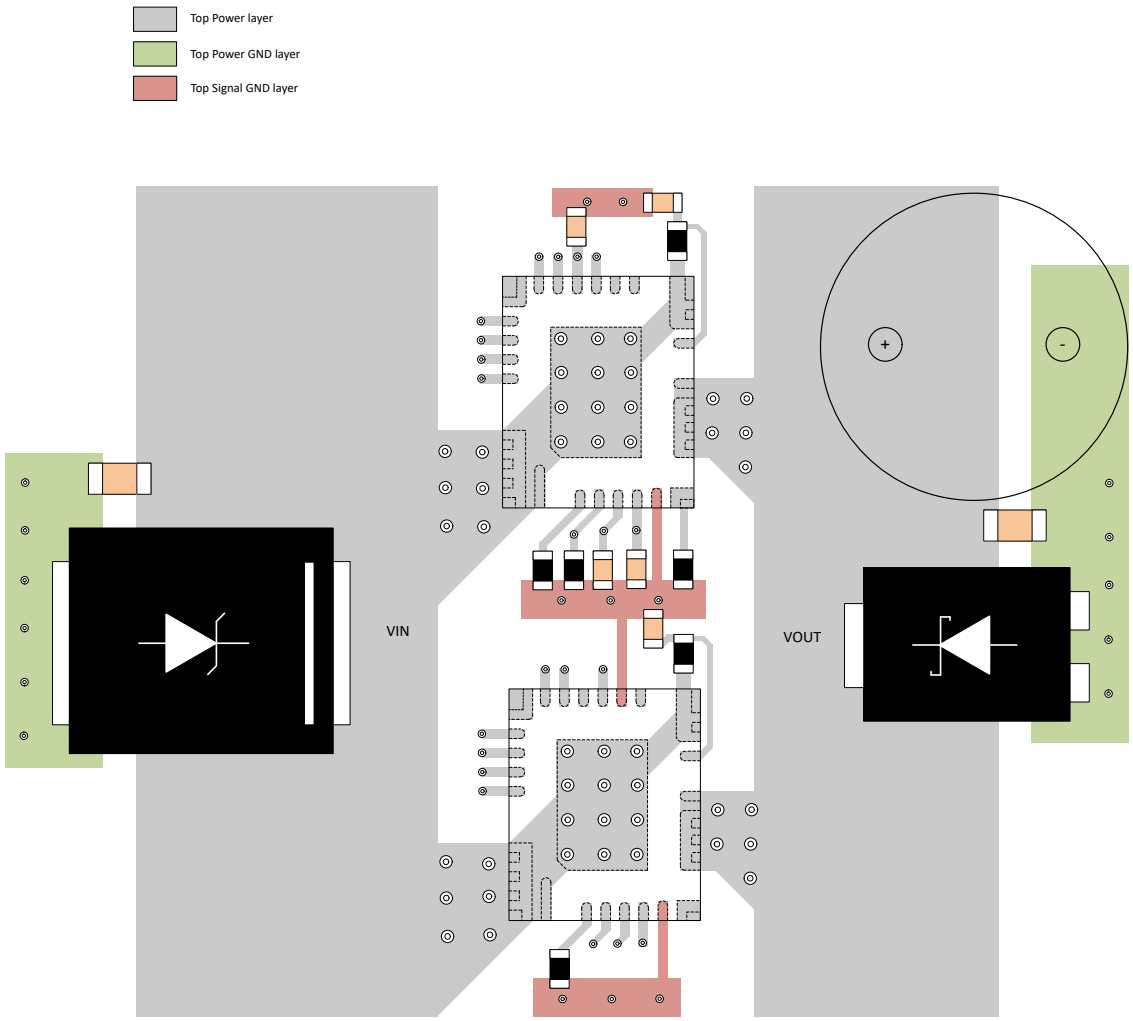

Figure 8-11. TPS1685x Two Parallel Devices Layout Example

ADVANCE INFORMATION

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS1685EVM eFuse Evaluation Board*
- Texas Instruments, *TPS1685x Design Calculator*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Intel® is a registered trademark of Intel.
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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

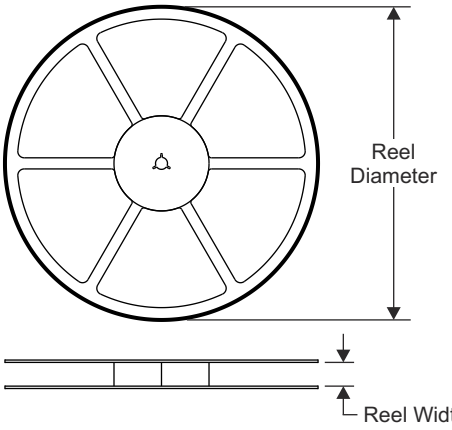
DATE	REVISION	NOTES
September 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

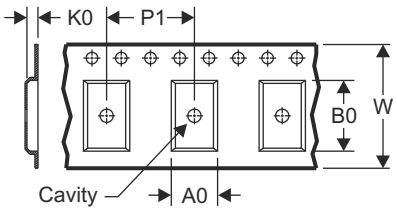
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

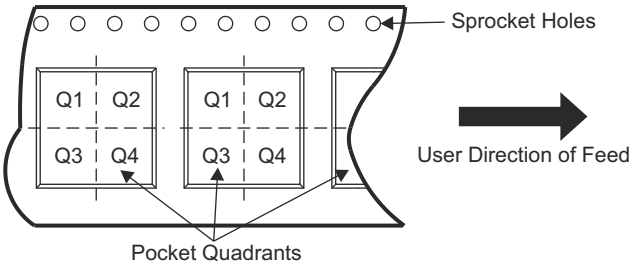


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

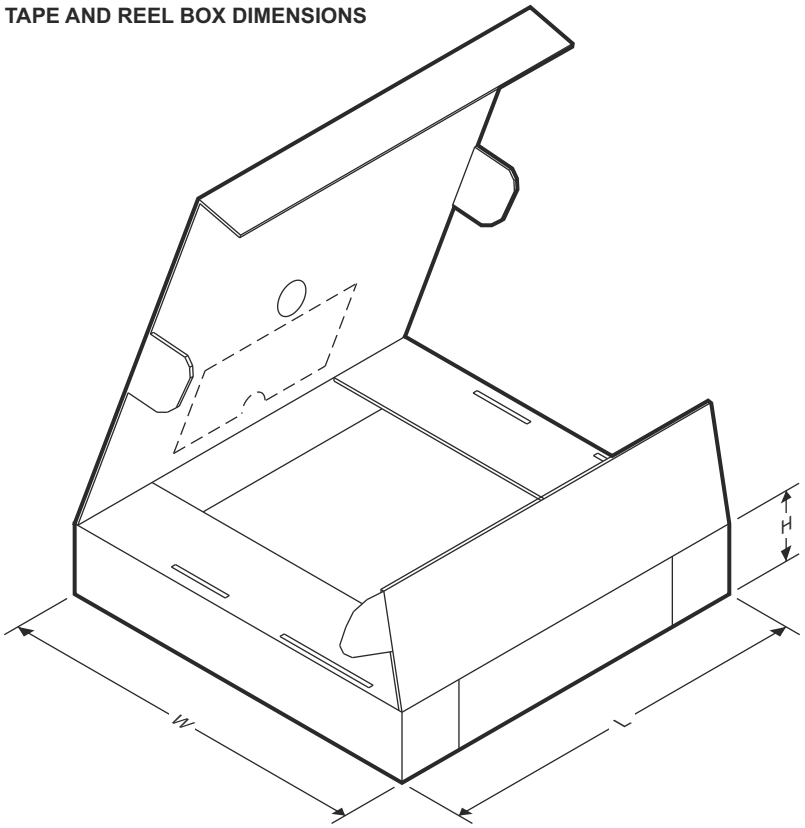


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS16850VMAR	LQFN	VMA	23	2500	330	16.4	6.3	5.3	1.75	8	16	Q1
PTPS16851VMAR	LQFN	VMA	23	2500	330	16.4	6.3	5.3	1.75	8	16	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

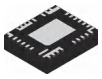
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS16850VMAR	LQFN	VMA	23	2500	367	367	38
PTPS16851VMAR	LQFN	VMA	23	2500	367	367	38

11.2 Mechanical Data

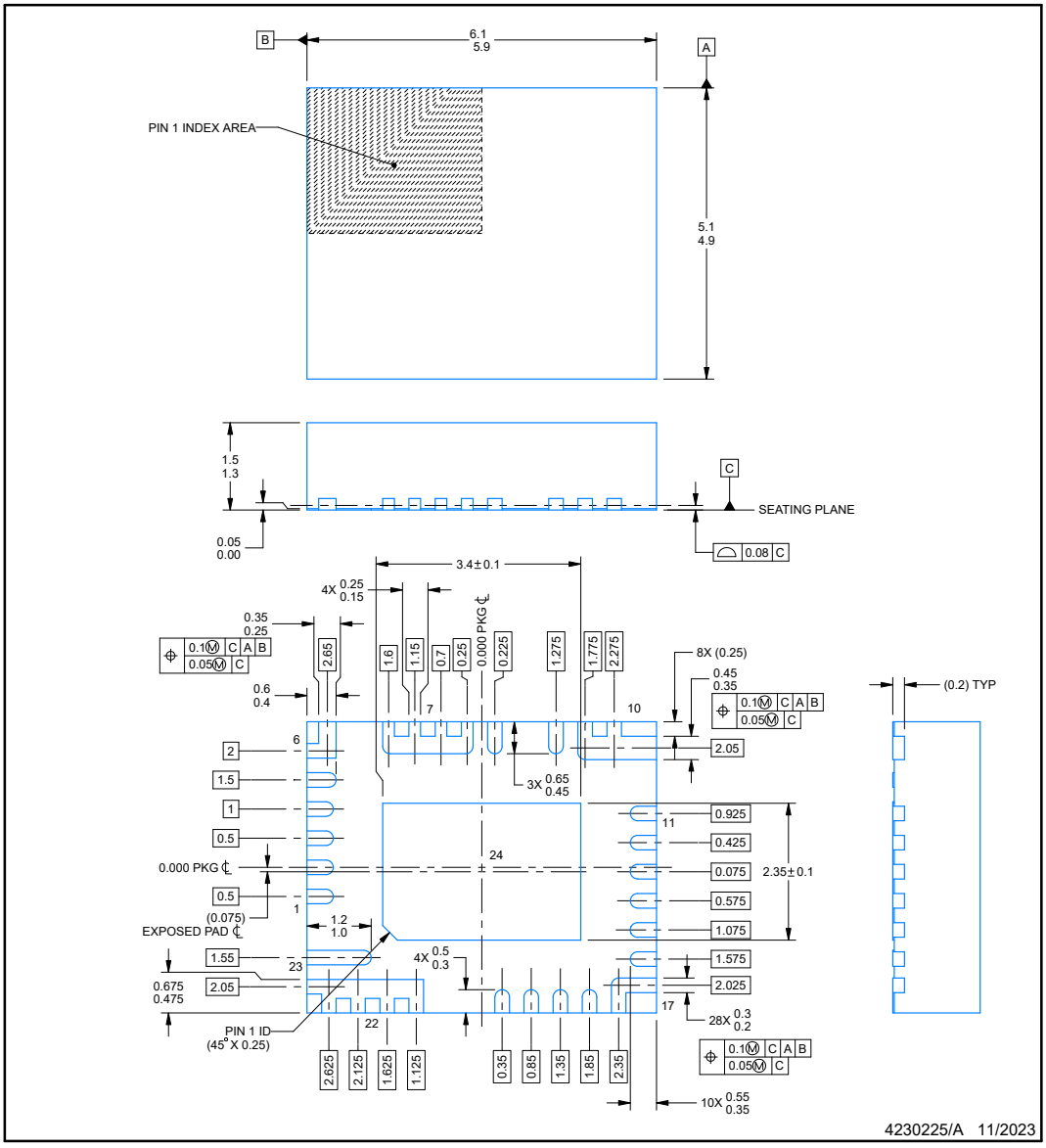
VMA0023A



PACKAGE OUTLINE

LQFN-CLIP - 1.5 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

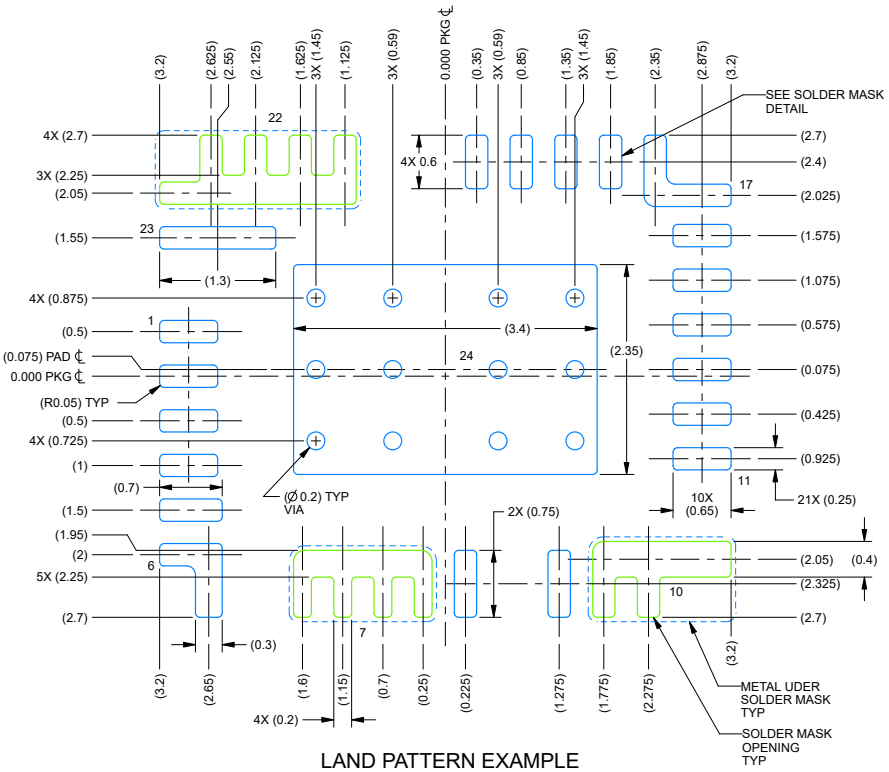
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

VMA0023A

LQFN-CLIP - 1.5 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

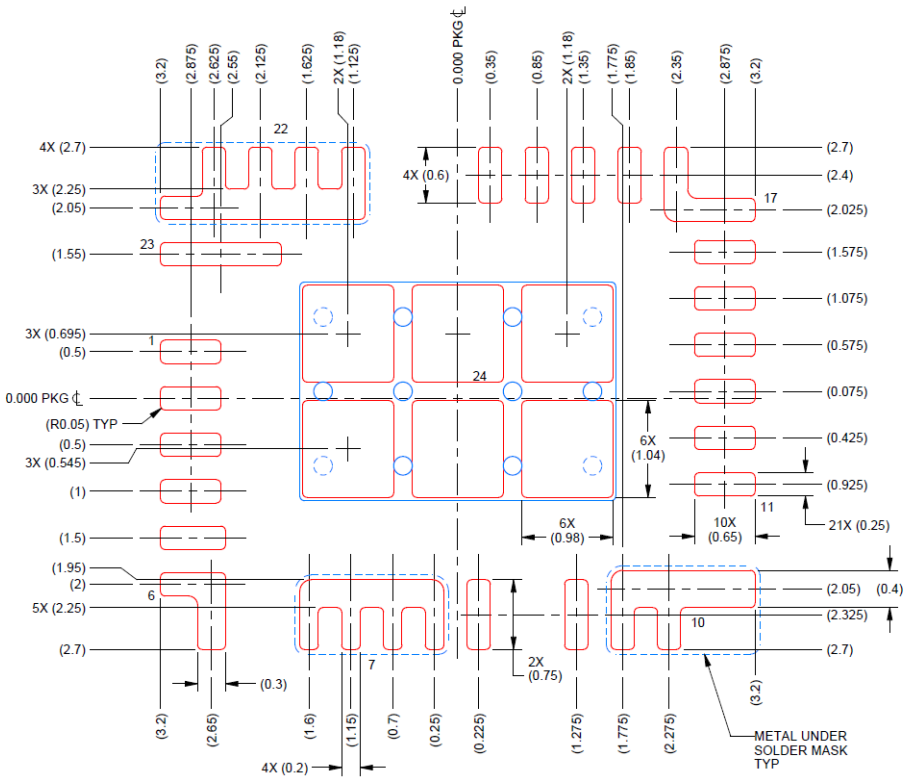
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VMA0023A

LQFN-CLIP - 1.5 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 28
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS16850VMAR	ACTIVE	LQFN-CLIP	VMA	23	2500	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS16851VMAR	ACTIVE	LQFN-CLIP	VMA	23	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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