TPS22860 Ultra-Low Leakage Load Switch

1 Features

- Integrated Single Channel Load Switch
- Bias Voltage Range (V_{BIAS}): 1.65 V to 5.5 V
- Input Voltage Range: 0 V to V_{BIAS}
- ON-Resistance (R_{ON})
  - R_{ON} = 0.73 Ω at VIN = 5 V (V_{BIAS} = 5 V)
  - R_{ON} = 0.68 Ω at VIN = 3.3 V (V_{BIAS} = 5 V)
  - R_{ON} = 0.63 Ω at VIN = 1.8 V (V_{BIAS} = 5 V)
- 200 mA Maximum Continuous Switch Current
- Ultra-Low Leakage Current
  - V_{IN} Leakage Current = 2 nA
  - V_{BIAS} Leakage Current at 5.5 V = 10 nA
- 6-pin SOT-23 or SC70 Package
- ESD Performance Tested per JESD 22
  - 2 kV HBM and 1 kV CDM

2 Applications

- Wearables
- Internet of Things
- Wireless Sensor Networks

3 Description

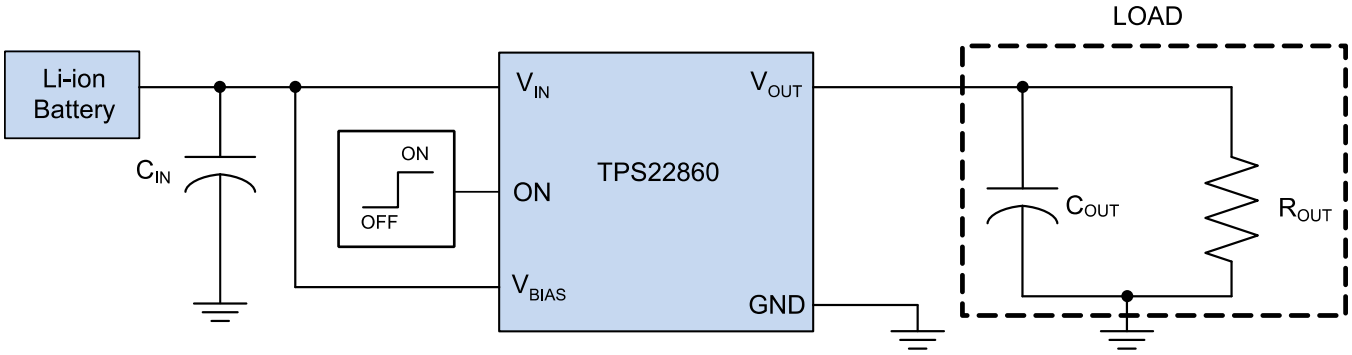
The TPS22860 is a small, ultra-low leakage current, single channel load switch. The device requires a V_{BIAS} voltage and can operate over an input voltage range of 0 V to V_{BIAS}. It can support a maximum continuous current of 200 mA. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. The TPS22860 is available in two small, space-saving 6-pin SOT-23 and SC70 packages. The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22860	SOT-23	2.80 x 2.90 mm
	SC-70	2.10 x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Common Application Schematic



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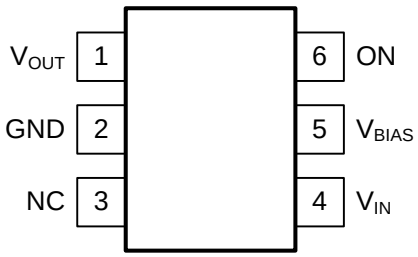
5 Revision History

DATE	REVISION	NOTES
April 2015	*	Initial release.

6 Pin Configuration and Functions

Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{OUT}	1	O	Switch output.
GND	2	—	Ground
NC	3	—	No connect
V_{IN}	4	I	Switch input. Connect a ceramic capacitor from V_{IN} to GND.
V_{BIAS}	5	I	Bias voltage. Power supply to the device.
ON	6	I	Active high switch control input. Do not leave floating.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT(2)
V_{BIAS}	BIAS voltage range	–0.5	6.5	V
V_{IN}	Input voltage range	–0.5	V_{BIAS} + 0.5	V
V_{OUT}	Output voltage range	–0.5	V_{BIAS} + 0.5	V
V_{ON}	Input voltage range	–0.5	6.5	V
I_{MAX}	Maximum Continuous Switch Current		200	mA
I_{PLS}	Maximum Pulsed Switch Current, pulse <300us, 2% duty cycle		400	mA
T_A	Operating free-air temperature range(3)	–40	85	°C
T_J	Maximum junction temperature		125	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Inapplications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (M JA \times P_{D(max)})$

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range		0		V_{BIAS}	V
V_{BIAS}	Supply voltage range		1.65		5.5	V
V_{ON}	Control input voltage range		0		5.5	V
V_{OUT}	Output voltage range		0		V_{BIAS}	V
$V_{IH, ON}$	High-level input voltage, ON	V_{BIAS} = 5 V	2.4		5.5	V
$V_{IL, ON}$	Low-level input voltage, ON	V_{BIAS} = 5 V	0		0.8	V
C_{IN}	Input Capacitor		1			µF

7.4 Thermal Information

THERMAL METRIC(1)(2)		TPS22860		UNIT
		DBV	DCK	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	235.2	249.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	164.8	107.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	82,.5	95.8	
ψ_{JT}	Junction-to-top characterization parameter	52.9	6.2	
ψ_{JB}	Junction-to-board characterization parameter	82.0	93.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

7.5 Electrical Characteristics

over operating free-air temperature range(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = V_{BIAS} = 3.3 V				10	100	nA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	V_{ON} = 0 V				10	100	
$I_{SD, VIN}$	V_{IN} shutdown current	V_{ON} = 0 V, V_{OUT} = 1 V	V_{IN} = 3.0 V			2	50	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V					100	
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –100 mA, V_{BIAS} = 3.3 V	V_{IN} = 3.3 V	T_A = 25°C		0.92	1.15	Ω
				Full T_A			1.31	
			V_{IN} = 2 V	T_A = 25°C		1.2	1.5	
				Full T_A			1.7	
			V_{IN} = 1.8 V	T_A = 25°C		0.95	1.2	
				Full T_A			1.35	

(1) Over the operating ambient temp –40°C ≤ TA ≤ 85°C (full) and VBIAS = 3.3V. Typical values are for TA = 25°C. (unless otherwise noted)

7.6 Switching Characteristics

over operating free-air temperature range(1) (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time	V_{OUT} = V_{BIAS}, R_L = 50 Ω C_L = 35 pF	T_A = 25°C	V_{BIAS} = 3.3 V	2	4.5	13	ns
			Full T_A	V_{BIAS} = 3 V to 3.6 V	1		15	
t_{OFF}	Turn-off time	V_{OUT} = V_{BIAS}, R_L = 50 Ω C_L = 35 pF	T_A = 25°C	V_{BIAS} = 3.3 V	3	9	15	ns
			Full T_A	V_{BIAS} = 3 V to 3.6 V	2		20	
$t_{ON/OFF}$	ON/OFF delay time				See Figure 9			

(1) V_{IN} = V_{ON} = V_{BIAS} = 5V, TA = 25ºC

7.7 Typical Characteristics

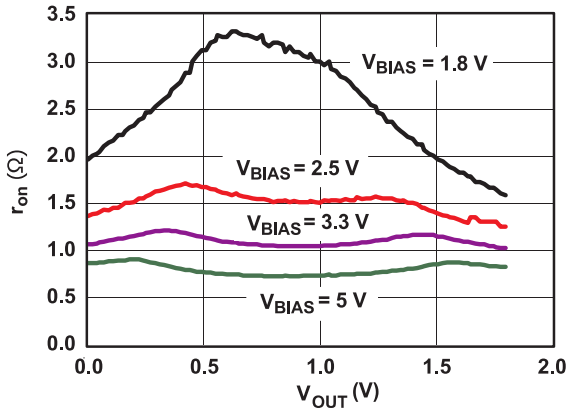


Figure 1. r_{on} vs V_{OUT}

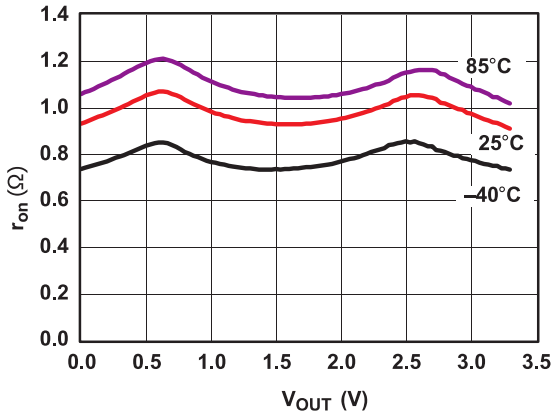


Figure 2. r_{on} vs V_{OUT} (V_{BIAS} = 3.3 V)

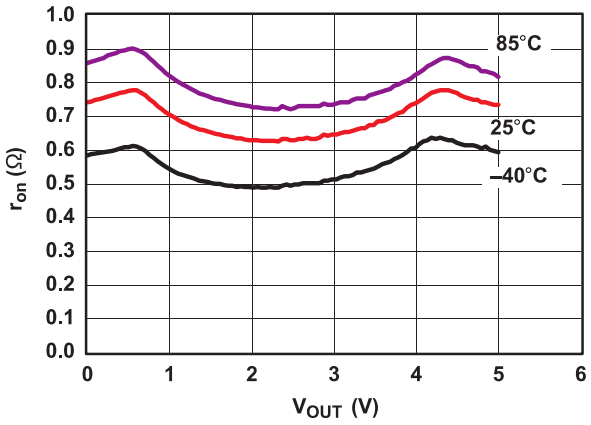


Figure 3. r_{on} vs V_{OUT} (V_{BIAS} = 5 V)

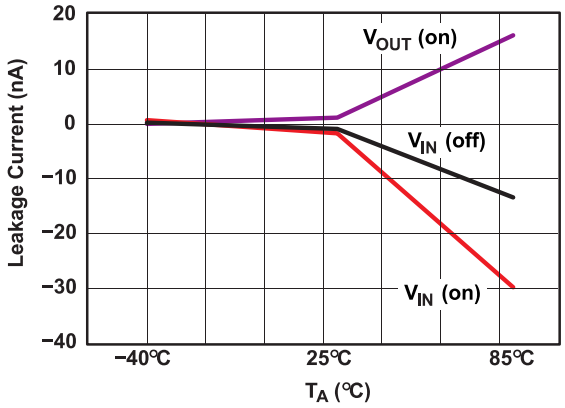


Figure 4. Leakage Current vs Temperature (V_{BIAS} = 5.5 V)

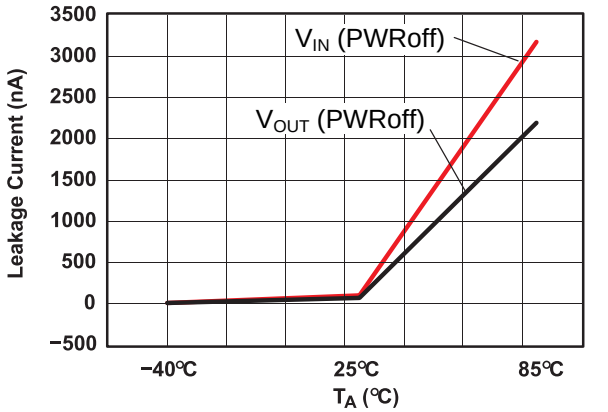


Figure 5. Leakage Current vs Temperature (V_{BIAS} = 5 V)

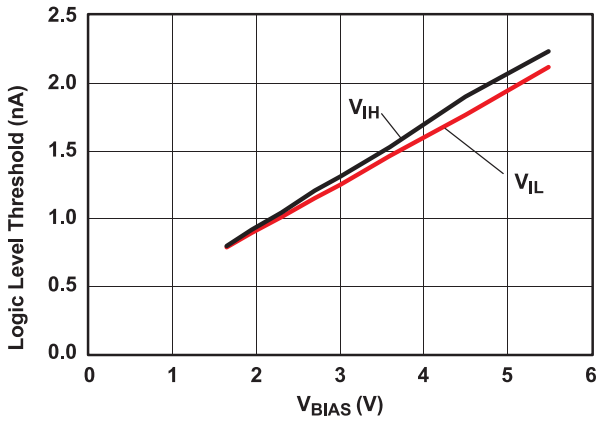


Figure 6. Logic-Level Threshold vs V_{BIAS}

Typical Characteristics (continued)

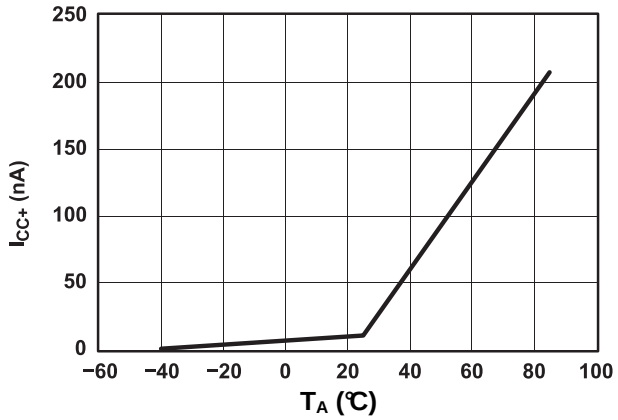


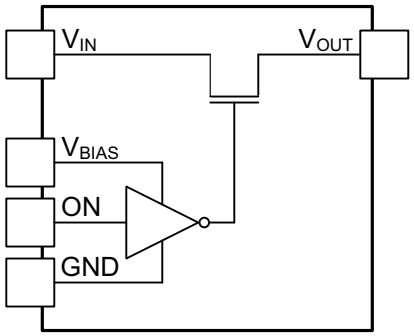
Figure 7. Power-Supply Current vs Temperature (V_{BIAS} = 5 V)

8 Detailed Description

8.1 Overview

The TPS22860 is a small, ultra-low leakage current, single channel bi-driectional load switch. The device requires a V_{BIAS} voltage and can operate over an input voltage range of 0 V to V_{BIAS}. It can support a maximum continuous current of 200 mA. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. The TPS22860 is available in two small, space-saving 6-pin SOT-23 and SC70 packages. The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ON/OFF Control

The ON input controls the load switch with positive logic.

8.3.2 Pass Transistor

The TPS22860 supports up to 200-mA current flow in either direction. R_{ON} is dependent on V_{BIAS} as shown in Figure 1, Figure 2, and Figure 3.

8.4 Device Functional Modes

Table 1. Functional Table

ON	V_{IN} to V_{OUT}
L	Off
H	On

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section will highlight some of the design considerations when implementing this device in a common application.

9.2 Typical Application

The TPS22860 IC is a high side load switch. The TPS22860 internal components are rated for 1.65-V to 5.5-V supply and support up to 200 mA of load current. The TPS22860 can be used in a variety of applications. Figure 8 below shows a general application of TPS22860 to control the load inrush current.

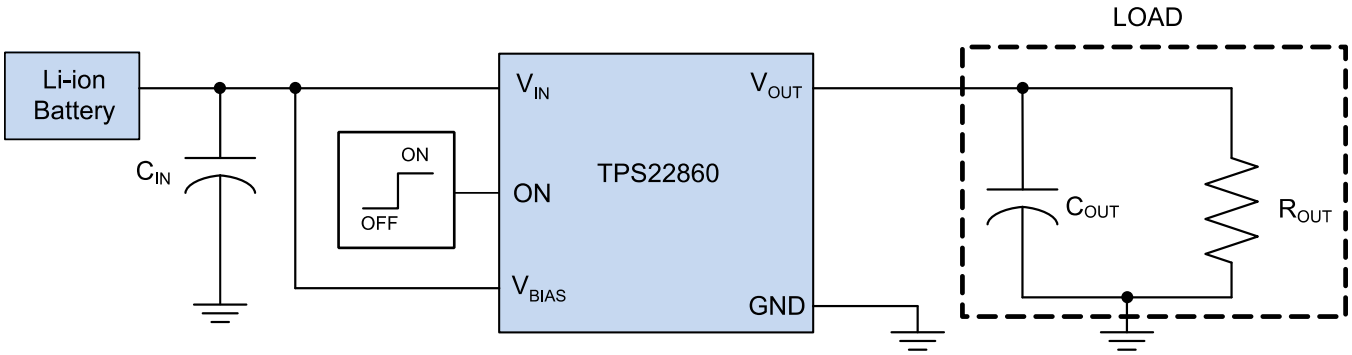


Figure 8. Standard Load Switching Application

9.2.1 Design Requirements

Table 2. Component Table

COMPONENT	DESCRIPTION
C_{IN}	Input capacitance (1)
LOAD	Load resistance and capacitance will affect the output rise time

(1) Required for load inrush current (slew rate) control

9.2.2 Detailed Design Procedure

9.2.2.1 Inrush Current

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor must be placed between V_{IN} and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current applications. When switching heavy loads, TI recommends to have an input capacitor about 10× higher than the output capacitor to avoid excessive voltage drop. Do not float the ON pin.

9.2.2.2 ON/OFF Interface

The load switch is controlled by the voltage at the ON pin. To turn ON, the input voltage must be larger than V_{IH} and to turn off the voltage must be below V_{IL}.

In applications where an ON/OFF signal is not available, connect ON pin to V_{IN}. The TPS22860 will turn ON/OFF in sync with the input supply connected to V_{IN}.

NOTE

Connect a pull down resistor from the ON pin to GND when the ON/OFF signal is driven by a high-impedance (tri-state) driver.

9.2.3 Application Curves

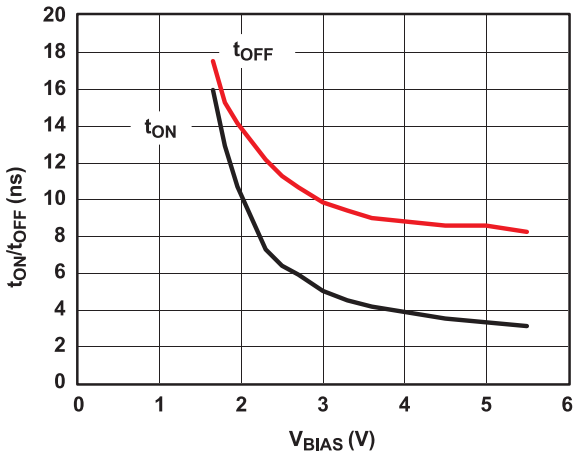


Figure 9. t_{ON} and t_{OFF} vs V_{BIAS}

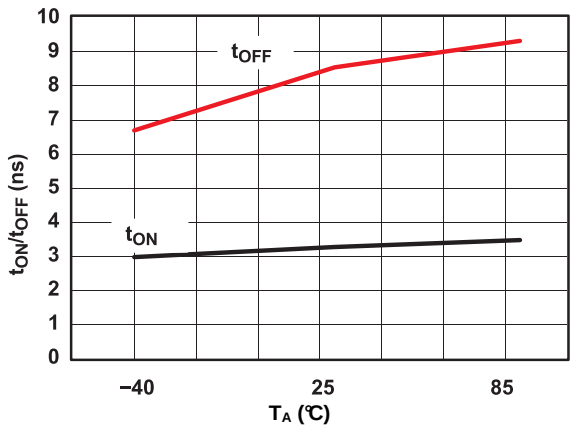


Figure 10. t_{ON} and t_{OFF} vs Temperature (V_{BIAS} = 5 V)

10 Power Supply Recommendations

The device is designed to operate from a VIN range of 1.65 V to 5.5 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1-µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 µF may be sufficient.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- V_{IN} and V_{OUT} traces should be as short and wide as possible to accommodate for high current.
- The V_{IN} pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- The VOUT pin should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the V_{IN} bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.

11.2 Thermal Reliability

For higher reliability it is recommended to limit TPS22860 IC's die junction temperature to less than 105°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate maximum on-chip power dissipation to achieve the maximum die junction temperature target:

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) \Big/ \theta_{JA} \quad (1)$$

Where:

$T_{J(MAX)}$ is the target maximum junction temperature.

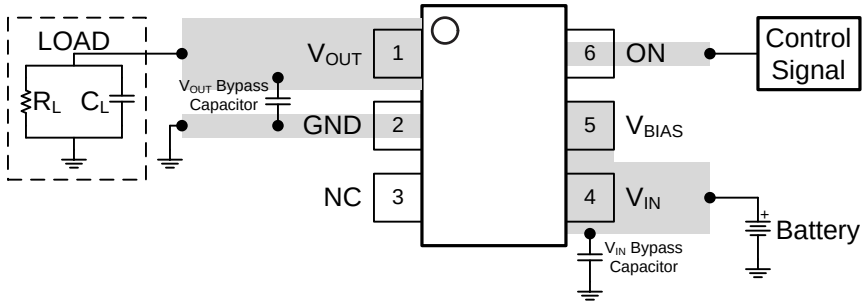
T_A is the operating ambient temperature.

$R_{\theta JA}$ is the package junction to ambient thermal resistance.

11.3 Improving Package Thermal Performance

The package $R_{\theta JA}$ value under standard conditions on a High-K board is listed in the *Thermal Information* table. $R_{\theta JA}$ value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce $R_{\theta JA}$ and thus improve device thermal capabilities. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

11.4 Layout Example



⏚ Indicates connection to ground plane

Figure 11. Basic PCB Layout

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22860DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZFNR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

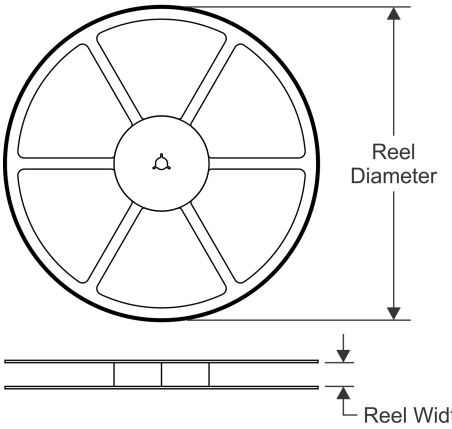
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

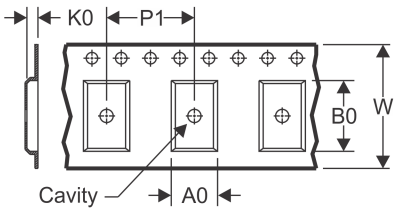
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

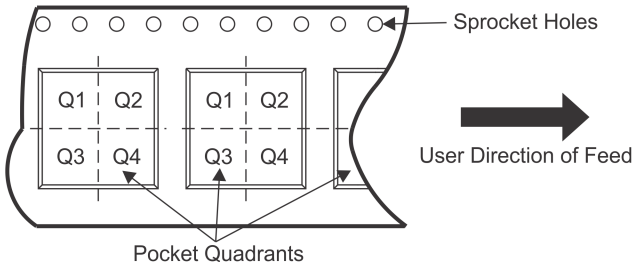


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

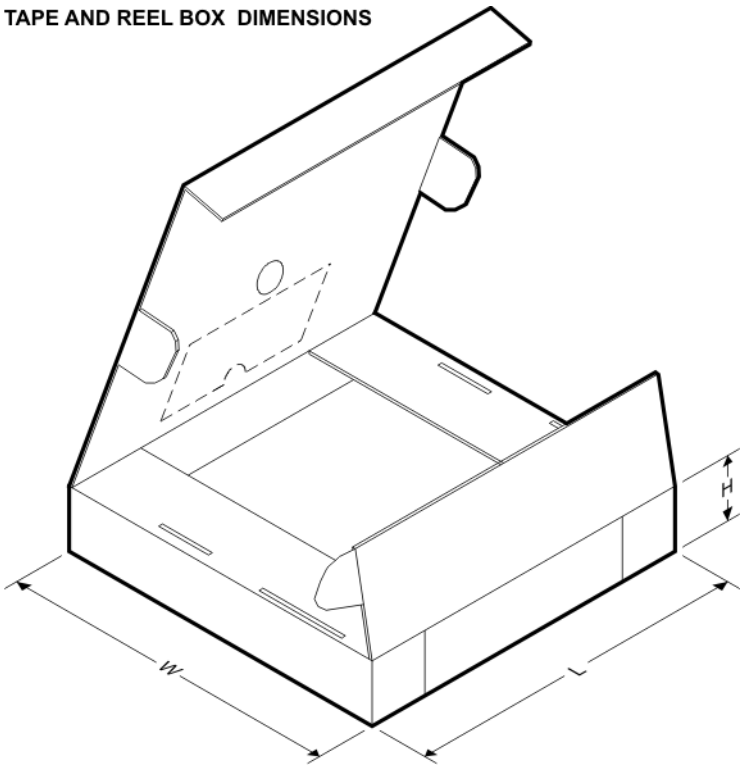
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22860DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

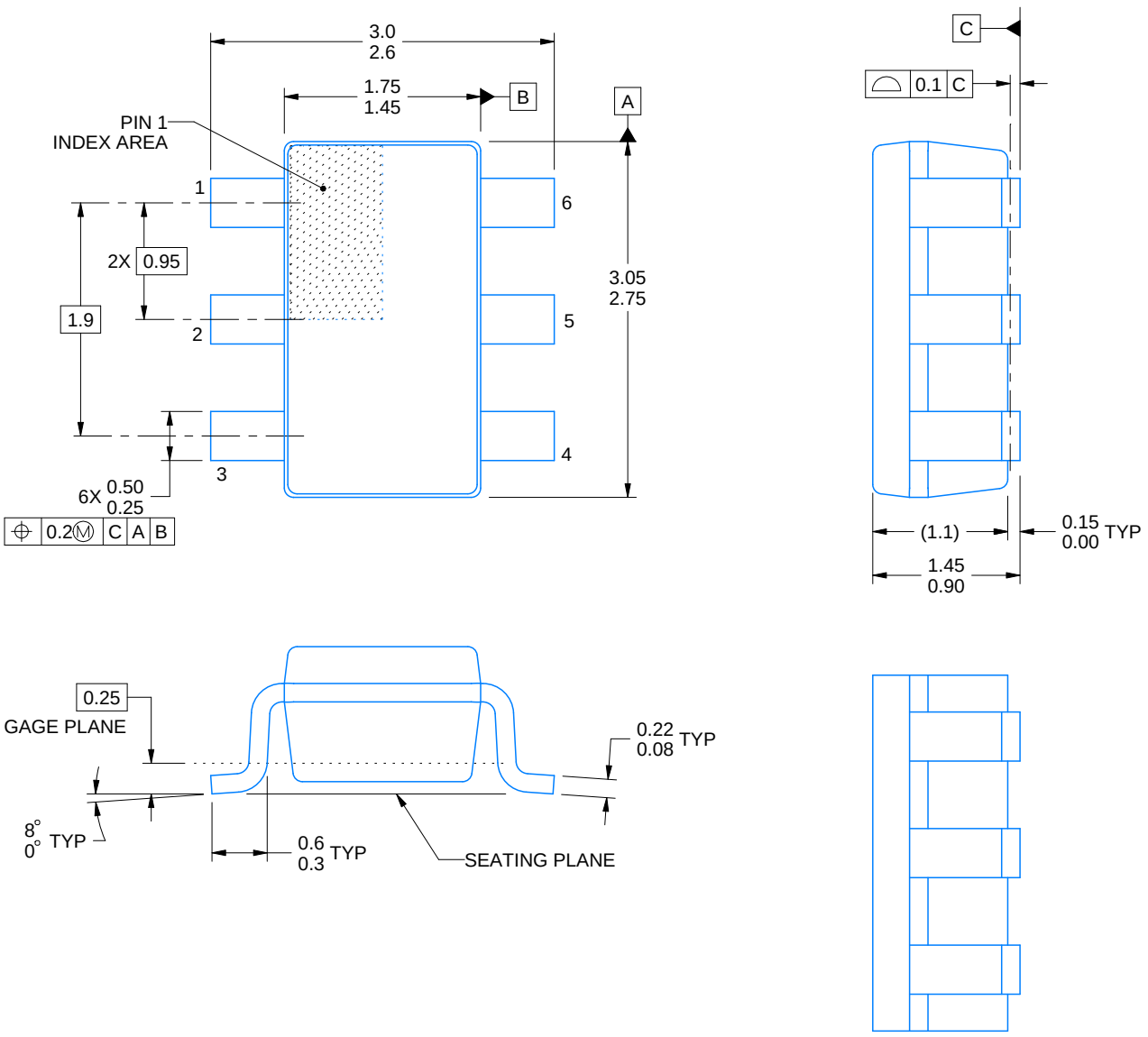
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22860DBVR	SOT-23	DBV	6	3000	183.0	183.0	20.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

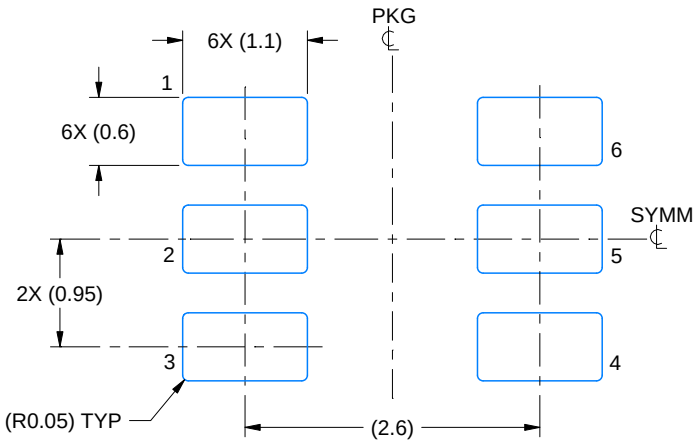


ALTERNATIVE PACKAGE SINGULATION VIEW

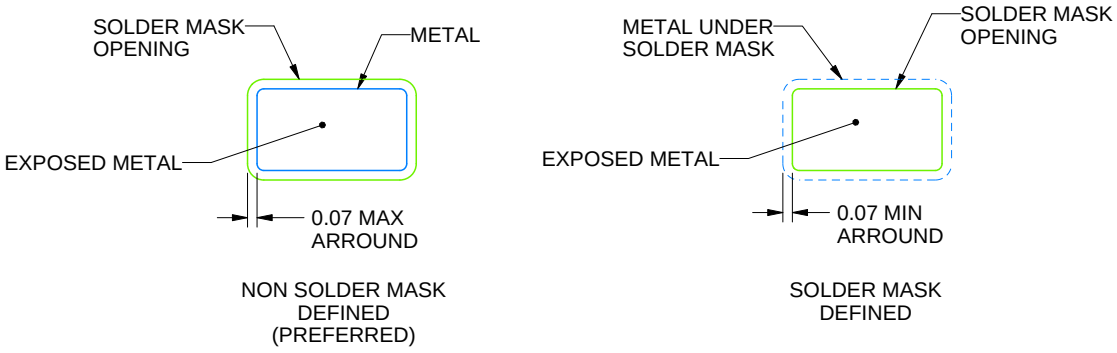
4214840/F 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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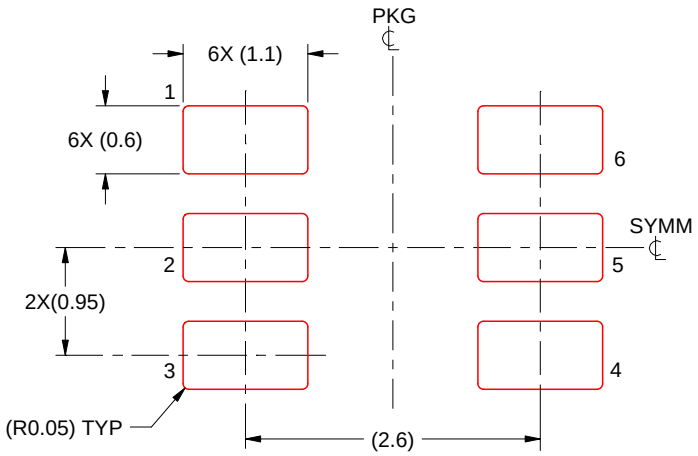
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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