XTR305 Industrial Analog Current or Voltage Output Driver

1 Features

- User-Selectable: Current or Voltage Output
- V_{OUT}: ±10 V (up to ±17.5 V at ±20-V supply)
- I_{OUT}: ±20 mA (Linear up to ±24 mA)
- 40-V Supply Voltage
- Diagnostic Features:
  - Short- or Open-Circuit Fault Indicator Pin
  - Thermal Protection
  - Overcurrent Protection
- No Current Shunt Required
- Output Disable for Single Input Mode
- Separate Driver and Receiver Channels
- Designed For Testability

2 Applications

- Motor Drives Analog Outputs: 4-20 mA and ±10 V
- PLC Output Programmable Driver
- Industrial Cross-Connectors
- Industrial High-Voltage I/O
- Three-Wire Sensor Current or Voltage Output
- ±10-V Two- and Four-Wire Voltage Output

U.S. Patent Nos. 7,427,898, 7,425,848, and 7,449,873

3 Description

The XTR305 is a complete output driver for cost-sensitive industrial and process control applications. The output can be configured as current or voltage by the digital I/V select pin. No external shunt resistor is required. Only external gain-setting resistors and a loop compensation capacitor are required.

The separate driver and receiver channels provide flexibility. The instrumentation amplifier (IA) can be used for remote voltage sense or as a high-voltage, high-impedance measurement channel. In voltage-output mode, a copy of the output current is provided, allowing calculation of load resistance.

The digital output-selection capability, together with the error flags and monitor pins, makes remote configuration and troubleshooting possible. Fault conditions on the output and on the IA input, as well as overtemperature conditions, are indicated by the error flags. The monitoring pins provide continuous feedback about load power or impedance. For additional protection, the maximum output current is limited, and thermal protection is provided.

The XTR305 is specified over the −40°C to +85°C industrial temperature range and for supply voltages up to 40 V, and is operational over the extended industrial temperature range (−55°C to +125°C).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
XTR305	VQFN (20)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

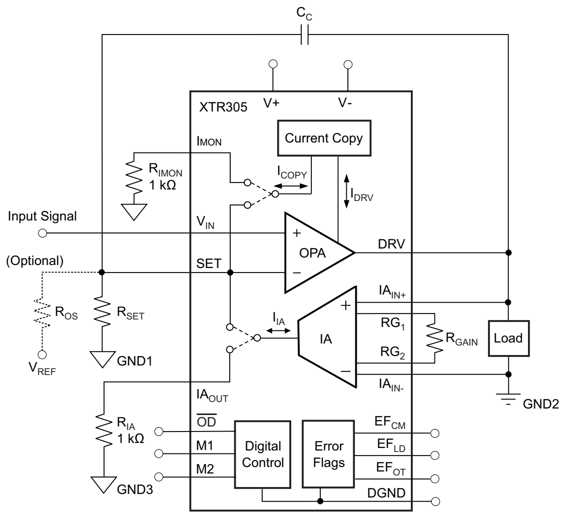


Table of Contents

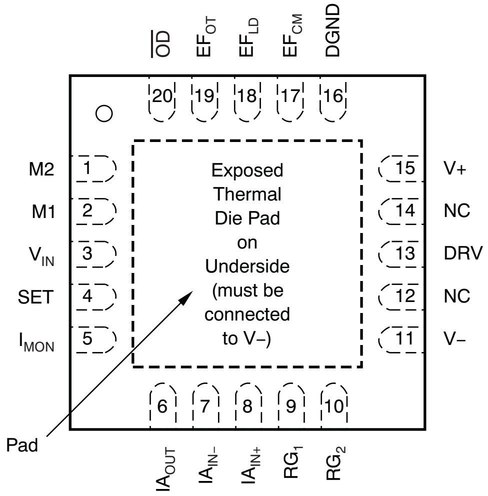
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2018	*	Initial release

5 Pin Configuration and Functions

RGW Package
20-Pin VQFN With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	M2	I	Mode input
2	M1	I	Mode input
3	V_{IN}	I	Noninverting signal input
4	SET	I	Input for gain setting; inverting input
5	I_{MON}	O	Current monitor output
6	IA_{OUT}	O	Instrumentation amplifier signal output
7	IA_{IN-}	I	Instrumentation amplifier inverting input
8	IA_{IN+}	I	Instrumentation amplifier noninverting input
9	RG1	I	Instrumentation amplifier gain resistor
10	RG2	I	Instrumentation amplifier gain resistor
11	V–	-	Negative power supply
12	NC	-	No internal connection
13	DRV	O	Operational amplifier output
14	NC	-	No internal connection
15	V+	-	Positive power supply
16	DGND	-	Ground for digital I/O
17	EF_{CM}	O	Error flag for common mode over range, active low
18	EF_{LD}	O	Error flag for load error, active low
19	EF_{OT}	O	Error flag for over temperature, active low
20	$\overline{OD}$	I	Output disable, disabled low
Pad	Exposed Pad	-	Exposed thermal pad must be connected to V−

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{VSP}			+44	V
Signal input terminals	Voltage(2)	(V−) − 0.5	(V+) + 0.5	V
	Current(2)		±25	mA
DGND			±25	mA
Output short circuit(3)		Continuous		
Operating temperature		–55	125	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited. DRV pin allows a peak current of 50 mA. See the *Output Protection* section in *Application and Implementation*.

(3) See *Driver Output Disable* in *Application and Implementation* for thermal protection.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Specified temperature range	−40		85	°C
Operating temperature range	−55		125(1)	°C

(1) EF_{OT} not connected with $\overline{OD}$.

6.4 Thermal Information

THERMAL METRIC(1)		XTR305	UNIT
		RGW (VQFN)	
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: Voltage Output Mode

All specifications at T_A = 25°C, V_S = ±20 V, R_{LOAD} = 800 Ω, R_{SET} = 2 kΩ, R_{OS} = 2 kΩ, V_{REF} = 4 V, R_{GAIN} = 10 kΩ, input signal span 0 V to 4 V, and C_C = 100 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Offset voltage, RTI			±0.4	±2.5	mV
dV_{OS}/dT	Offset voltage vs temperature	T_A = –40°C to 85°C		±1.6	±10	µV/°C
PSRR	Offset voltage vs power supply	V_S = ±5 V to ±22 V		±0.2	±10	µV/V
INPUT VOLTAGE RANGE						
	Nominal setup for ±10-V output	See Figure 35				
	Input voltage for linear operation		(V−) + 3		(V+) − 3	V
NOISE						
	Voltage noise, f = 0.1 Hz to 10 Hz, RTI			3		μV_{PP}
e_n	Voltage noise density, f = 1 kHz, RTI			40		nV/√Hz
OUTPUT						
	Voltage output swing from rail	I_{DRV} ≤ 15 mA, T_A = –40°C to 85°C	(V−) +3		(V+) − 3	V
	Gain nonlinearity			±0.01	±0.2	%FS
	Gain nonlinearity vs temperature	T_A = –40°C to 85°C		±0.1	±1	ppm/°C
I_B	Gain error			±0.04	±0.2	%FS
	Gain error vs temperature	T_A = –40°C to 85°C		±0.2	±1	ppm/°C
	Output impedance, dV_{DRV}/dI_{DRV}			7		mΩ
	Output leakage current while output disabled	$\overline{OD}$ pin = L (1), T_A = –40°C to 85°C		30		nA
I_{SC}	Short-circuit current	T_A = –40°C to 85°C	±15	±20	±24	mA
C_{LOAD}	Capacitive load drive	C_C = 10 nF, R_C = 15 (2)		1		µF
	Rejection of voltage difference between GND1 and GND2, RTO			130		dB
FREQUENCY RESPONSE						
	Bandwidth (3)	−3 dB, G = 5		300		kHz
SR	Slew rate (2)			1		V/µs
		C_C = 10 nF, C_{LOAD} = 1 µF, R_C = 15 Ω		0.015		
	Settling time (2) (4), 0.1%, small signal	V_{DRV} = ±1 V		8		µs
	Overload recovery time	50% overdrive		12		µs

(1) Output leakage includes input bias current of INA.
(2) Refer to *Driving Capacitive Loads and Loop Compensation* section in *Application and Implementation*.
(3) Small signal with no capacitive load.
(4) 8 µs plus number of chopping periods. See *Application and Implementation*, *Internal Current Sources, Switching Noise, and Settling Time* section.

6.6 Electrical Characteristics: Current Output Mode

All specifications at T_A = 25°C, V_S = ±20 V, R_{LOAD} = 800 Ω, R_{SET} = 2 kΩ, R_{OS} = 2 kΩ, V_{REF} = 4 V, input signal span 0 V to 4 V, and C_C = 100 pF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	Output current < 1 µA		±0.4	±2.5	mV
dV_{OS}/dT	Input offset voltage vs temperature			±1.5	±10	µV/°C
PSRR	Input offset voltage vs power supply	V_S = ±5 V to ±22 V		±0.2	±10	µV/V
INPUT VOLTAGE RANGE						
	Nominal setup for ±20-mA output	See Figure 36				
	Maximum input voltage for linear operation		(V−) + 3		(V+) − 3	V
NOISE						
	Voltage noise, f = 0.1Hz to 10Hz, RTI			3		μV_{PP}
e_n	Voltage noise density, f = 1kHz, RTI			33		nV/√Hz
OUTPUT						
	Compliance voltage swing from rail	I_{DRV} = ±24 mA	(V−) +3		(V+) − 3	V
	Output conductance (dI_{DRV}/dV_{DRV})	dV_{DRV} = ±15 V, dI_{DRV} = ±24 mA		0.7		µA/V
	Transconductance	See transfer function in Figure 36				
	Gain error	I_{DRV} = ±24 mA		±0.04	±0.2	%FS
	Gain error vs temperature	I_{DRV} = ±24 mA		±3.6	±10	ppm/°C
I_B	Linearity error	I_{DRV} = ±24 mA		±0.01	±0.2	%FS
	Linearity error vs temperature	I_{DRV} = ±24 mA		±1.5	±10	ppm/°C
	Output leakage current while output disabled	$\overline{OD}$ pin = L		0.6		nA
I_{SC}	Short-circuit current		±24.5	±32	±38.5	mA
C_{LOAD}	Capacitive load drive (1)(2)			1		µF
FREQUENCY RESPONSE						
	Bandwidth	−3 dB		160		kHz
SR	Slew rate (2)			1.3		mA/µs
	Settling time (2)(3), 0.1%, Small Signal	I_{DRV} = ±2 mA		8		µs
	Overload recovery time	C_{LOAD} = 0, 50% overdrive		1		µs

(1) Refer to *Driving Capacitive Loads and Loop Compensation* section in *Application and Implementation*.
(2) With capacitive load, the slew rate can be limited by the short circuit current and the load error flag can trigger during slewing.
(3) 8 µs plus number of chopping periods. See *Application and Implementation*, *Internal Current Sources, Switching Noise, and Settling Time* section.

6.7 Electrical Characteristics: Operational Amplifier (OPA)

All specifications at T_A = 25°C, V_S = ±20 V, and R_{LOAD} = 800 Ω, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Offset voltage, RTI	I_{DRV} = 0 A		±0.4	±2.5	mV
dV_{OS}/dT	Offset voltage drift	T_A = –40°C to 85°C		±1.5		µV/°C
PSRR	Offset voltage vs power supply	V_S = ±5 V to ±22 V		±0.2	±10	µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V−) + 3		(V+) − 3	V
CMRR	Common-mode rejection ratio	(V−) + 3 V < V_{CM} < (V+) − 3 V	95	126		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±20	±35	nA
I_{OS}	Input offset current			±0.3	±10	nA
INPUT IMPEDANCE						
	Differential			10^8 || 5		Ω || pF
	Common-mode			10^8 || 5		Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V−) + 3 V < V_{DRV} < (V+) − 3 V, I_{DRV} = ±24 mA	95	126		dB
OUTPUT						
	Voltage output swing from rail	I_{DRV} = ±24 mA	(V−) + 3		(V+) − 3	V
I_{LIMIT}	Short-circuit current	M2 = high	±25.5	±32	±38.5	mA
I_{LIMIT}		M2 = low	±16	±20	±24	mA
I_{LEAK_DRV}	Output leakage current while output disabled	$\overline{OD}$ pin = L		10		pA
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 1		2		MHz
SR	Slew rate			1		V/µs

6.8 Electrical Characteristics: Instrumentation Amplifier (IA)

All specifications at T_A = 25°C, V_S = ±20 V, R_{IA} = 2 kΩ, and R_{GAIN} = 2 kΩ, unless otherwise noted. See Figure 37.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Offset voltage, RTI	I_{DRV} = 0 A		±0.7	±2.7	mV
dV_{OS}/dT	Offset voltage vs temperature	T_A = –40°C to 85°C		±2.4	±10	µV/°C
PSRR	Offset voltage vs power supply	V_S = ±5 V to ±22 V		±0.8	±10	µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Input voltage range		(V−) + 3		(V+) − 3	V
CMRR	Common-mode rejection ratio	RTI	100	130		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±20	±35	nA
I_{OS}	Input offset current			±1	±10	nA
INPUT IMPEDANCE						
	Differential			10^5 || 5		Ω || pF
	Common-mode			10^5 || 5		Ω || pF
TRANSCONDUCTANCE (Gain)(1)						
	Transconductance error	IA_{OUT} = ±2.4 mA, (V−) + 3 V < V_{IAOUT} < (V+) − 3 V		±0.04	±0.1	%FS
	Transconductance error vs temperature	T_A = –40°C to 85°C		±0.2		ppm/°C
	Linearity error	(V−) + 3 V < V_{IAOUT} < (V+) − 3 V		±0.01	±0.1	%FS
	Input bias current to G1, G2			±20		nA
	Input offset current to G1, G2(2)			±1		nA
OUTPUT						
	Output swing to the rail	IA_{OUT} = ±2.4 mA	(V−) + 3		(V+) − 3	V
	Output impedance	IA_{OUT} = ±2.4 mA		600		mΩ
I_{LIMIT}	Short-circuit current	M2 = High		±7.2		mA
		M2 = Low		±4.5		mA
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	G = 1, R_{GAIN} = 10 kΩ, R_{IA} = 5 kΩ		1		MHz
SR	Slew rate	G = 1, R_{GAIN} = 10 kΩ, R_{IA} = 5 kΩ		1		V/µs
	Settling time(3), 0.1%	IA_{OUT} = ±40 µA, R_{GAIN} = 10 kΩ, R_{IA} = 5 kΩ, C_L = 100 pF		6		µs
	Overload recovery time, 50%	R_{GAIN} = 10 kΩ, R_{IA} = 15 kΩ, C_L = 100 pF		10		µs

(1) Use equation: $IA_{OUT} = 2\ (IA_{IN+} - IA_{IN-})\ /\ R_{GAIN}$

(2) See typical characteristics curve (Figure 3).

(3) 6 µs plus number of chopping periods. See *Application and Implementation*, *Internal Current Sources, Switching Noise, and Settling Time*.

6.9 Electrical Characteristics: Current Monitor

All specifications at T_A = 25°C and V_S = ±20 V, unless otherwise noted. See Figure 37.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
I_{OS}	Offset current	I_{DRV} = 0 A		±30	±100	nA
dI_{OS}/dT	Offset current drift	T_A = –40°C to 85°C		±0.05		nA/°C
PSRR	Offset current vs power supply	V_S = ±5 V to ±22 V		±0.1	±10	nA/V
	Monitor output swing to the rail	I_{MON} = ±2.4 mA	(V−) + 3		(V+) − 3	V
	Monitor output impedance	I_{MON} = ±2.4 mA		200		MΩ
MONITOR CURRENT GAIN(1)						
	Current gain error	I_{DRV} = ±24 mA		±0.04	±0.12	%FS
	Current gain error vs temperature	I_{DRV} = ±24 mA, T_A = –40°C to 85°C		±3.6		ppm/°C
	Linearity error	I_{DRV} = ±24 mA		±0.01	±0.1	%FS
	Linearity error vs temperature	I_{DRV} = ±24 mA, T_A = –40°C to 85°C		±1.5		ppm/°C

(1) Use equation: $I_{MON} = I_{DRV} / 10$

6.10 Electrical Characteristics: Power and Digital

All specifications at T_A = 25°C and V_S = ±20 V, unless otherwise noted. See Figure 37.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Specified voltage range		±5		±20	V
	Operating voltage range		±5		±22	V
I_Q	Quiescent current	$I_{DRV} = IA_{OUT}$ = 0 A		1.8	2.3	mA
	Quiescent current over temperature	T_A = –40°C to 85°C			2.8	mA
THERMAL FLAG (EF_{OT}) OUTPUT						
	Alarm (EF_{OT} pin LOW)			140		°C
	Return to normal operation (EF_{OT} pin HIGH)			125		°C
DIGITAL INPUTS (M1, M2, $\overline{OD}$)						
	V_{IL} low-level input voltage			≤ 0.8		V
	V_{IH} high-level input voltage			> 1.4		V
	Input current			±1		µA
DIGITAL OUTPUTS (EF_{LD}, EF_{CM}, EF_{OT})						
	I_{OH} high-level leakage current (open-drain)			−1.2		µA
	V_{OL} low-level output voltage	I_{OL} = 5 mA		0.8		V
	V_{OL} low-level output voltage	I_{OL} = 2.8 mA		0.4		V
DIGITAL GROUND PIN(1)						
	Current input	M1 = M2 = L, $\overline{OD}$ = H, all digital outputs H		−25		µA

(1) Use equation: (V−) ≤ DGND ≤ (V+) − 7 V

6.11 Typical Characteristics

at T_A = 25°C and V+ = ±20 V, unless otherwise noted

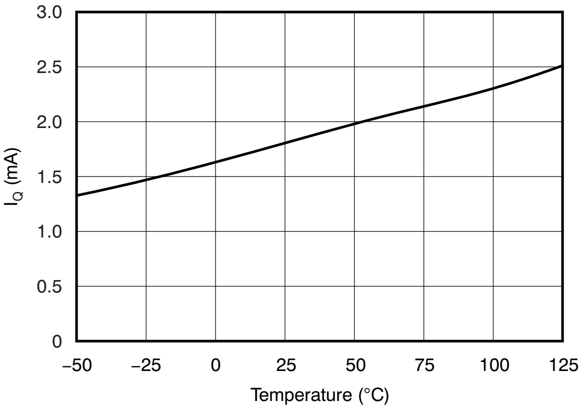


Figure 1. Quiescent Current vs Temperature

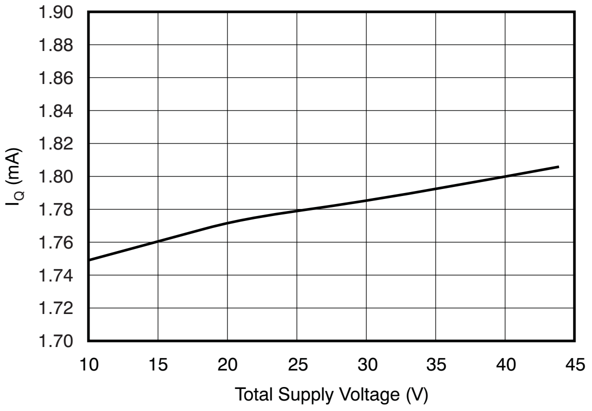
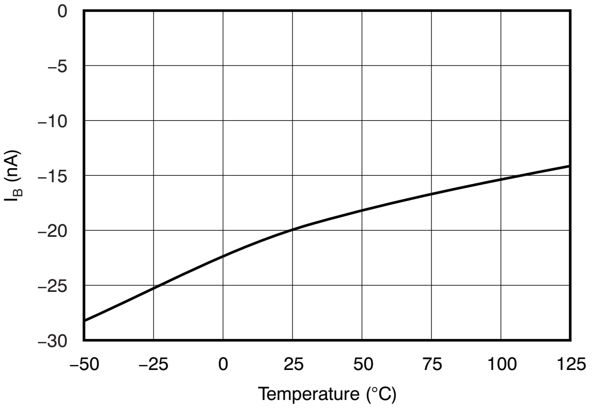


Figure 2. Quiescent Current vs Supply Voltage



(V_{IN}, SET, IA_{IN+}, IA_{IN-}, RG1, RG2)

Figure 3. Input Bias Current vs Temperature

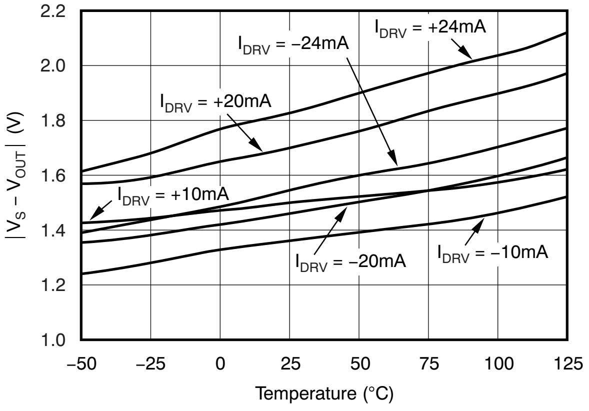


Figure 4. OPA Output Swing to Rail vs Temperature

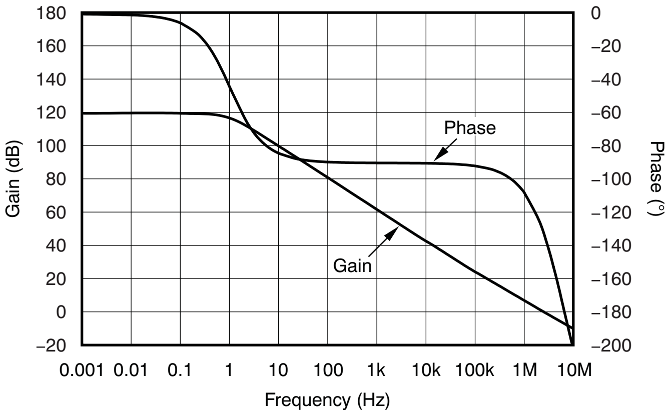


Figure 5. OPA Gain and Phase vs Frequency

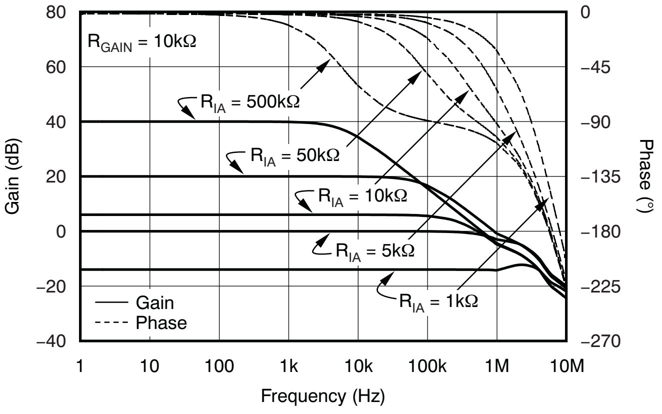


Figure 6. IA Gain and Phase vs Frequency

Typical Characteristics (continued)

at T_A = 25°C and V+ = ±20 V, unless otherwise noted

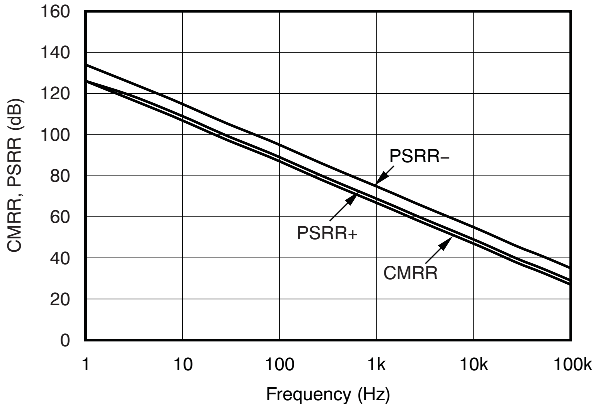


Figure 7. OPA CMRR and PSRR vs Frequency

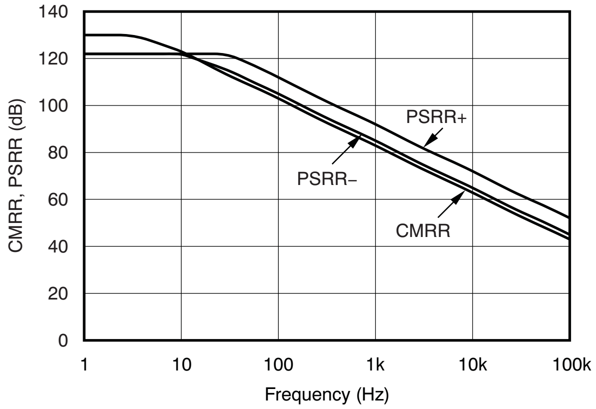
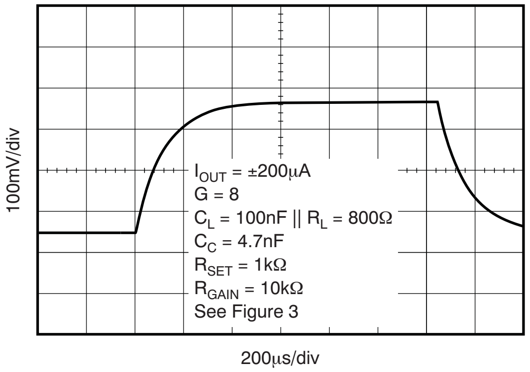
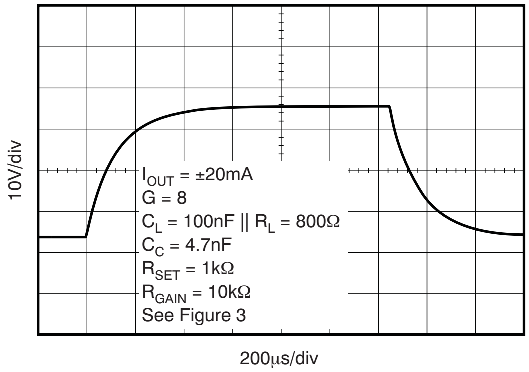


Figure 8. IA CMRR and PSRR vs Frequency



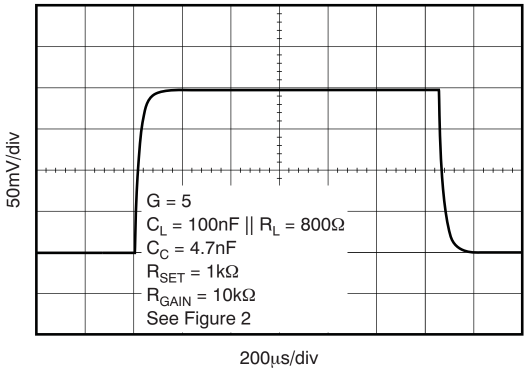
I_{OUT} = ±200μA
G = 8
C_L = 100nF || R_L = 800Ω
C_C = 4.7nF
R_{SET} = 1kΩ
R_{GAIN} = 10kΩ
See Figure 3

Figure 9. Small-Signal Step Response Current Mode



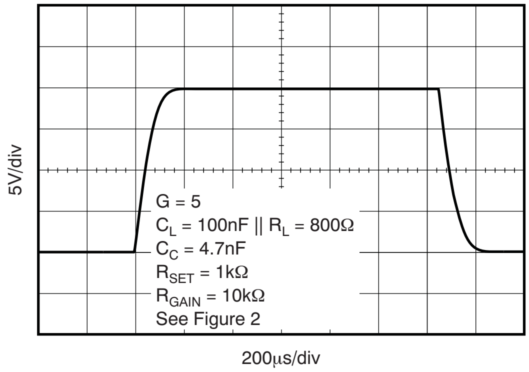
I_{OUT} = ±20mA
G = 8
C_L = 100nF || R_L = 800Ω
C_C = 4.7nF
R_{SET} = 1kΩ
R_{GAIN} = 10kΩ
See Figure 3

Figure 10. Large-Signal Step Response Current Mode



G = 5
C_L = 100nF || R_L = 800Ω
C_C = 4.7nF
R_{SET} = 1kΩ
R_{GAIN} = 10kΩ
See Figure 2

Figure 11. Small-Signal Step Response Voltage Mode



G = 5
C_L = 100nF || R_L = 800Ω
C_C = 4.7nF
R_{SET} = 1kΩ
R_{GAIN} = 10kΩ
See Figure 2

Figure 12. Large-Signal Step Response Voltage Mode

Typical Characteristics (continued)

at T_A = 25°C and V+ = ±20 V, unless otherwise noted

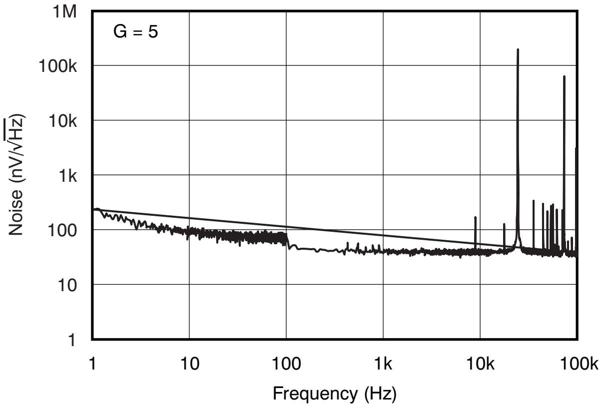


Figure 13. Input-Referred Noise Spectrum Voltage Output Mode

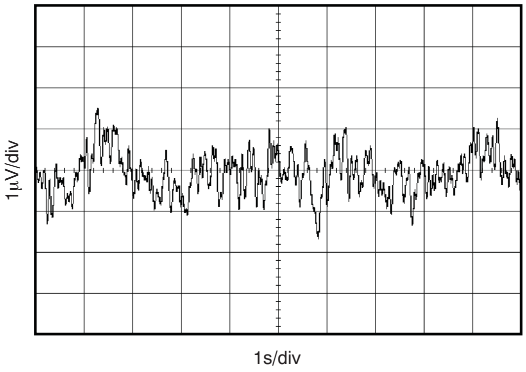


Figure 14. Input-Referred 0.1-Hz to 10-Hz Noise Voltage Output Mode

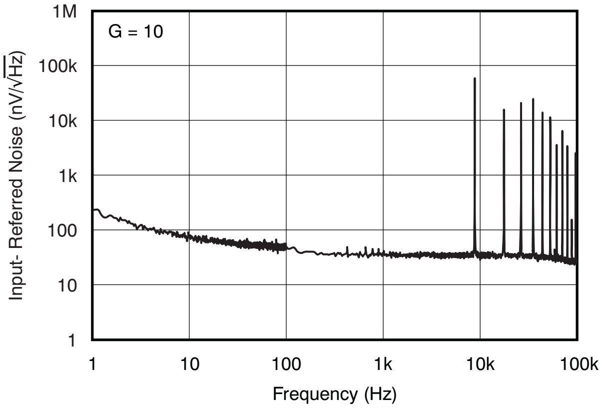


Figure 15. Input-Referred Noise Spectrum Current Output Mode

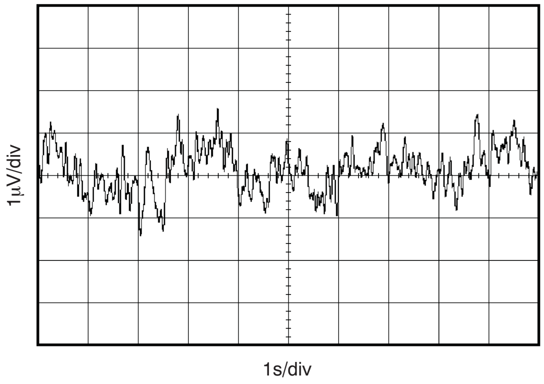


Figure 16. Input-Referred 0.1-Hz to 10-Hz Noise Current Output Mode

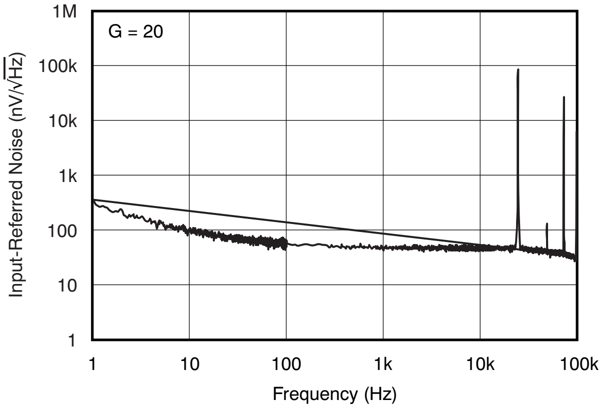


Figure 17. IA Input-Referred Noise Spectrum

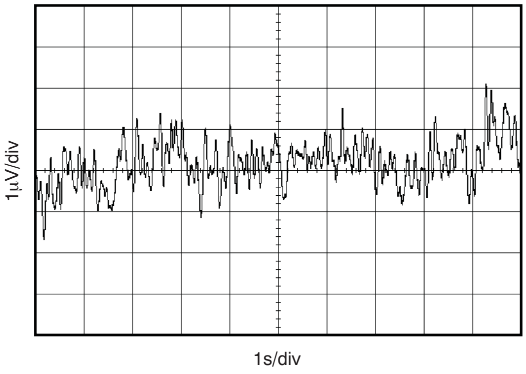


Figure 18. IA Input-Referred 0.1-Hz to 10-Hz Noise

Typical Characteristics (continued)

at T_A = 25°C and V+ = ±20 V, unless otherwise noted

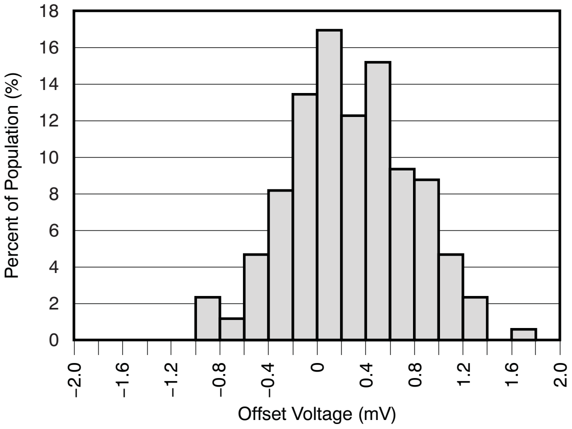


Figure 19. OPA Offset Voltage Distribution

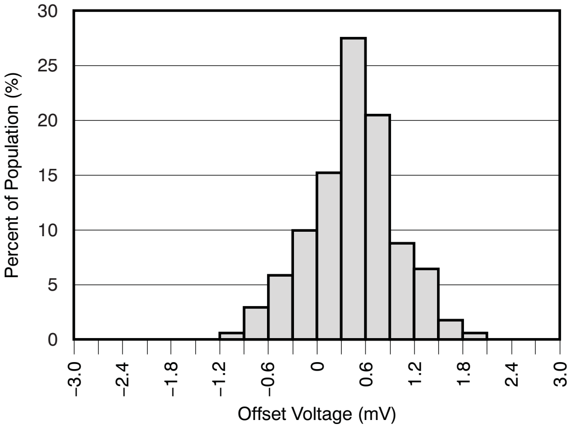


Figure 20. IA Offset Voltage Distribution

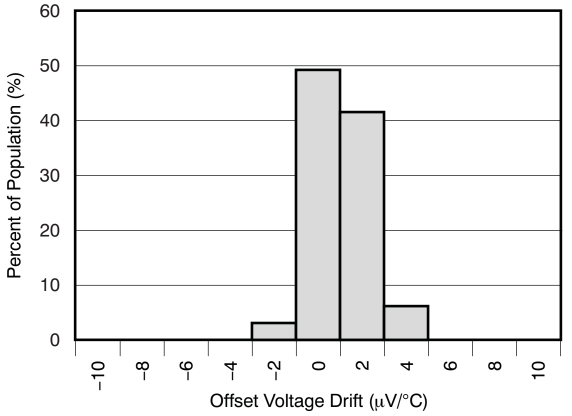


Figure 21. OPA Offset Voltage Drift Distribution

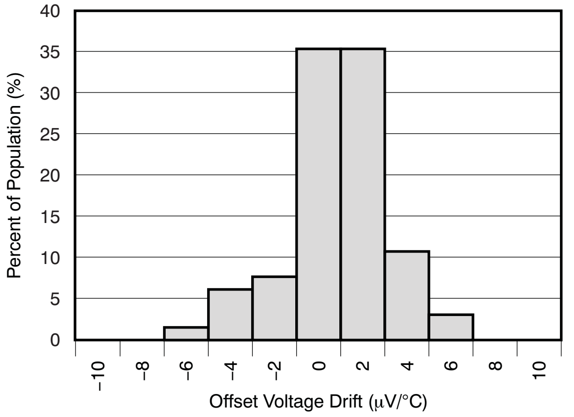


Figure 22. IA Offset Voltage Drift Distribution

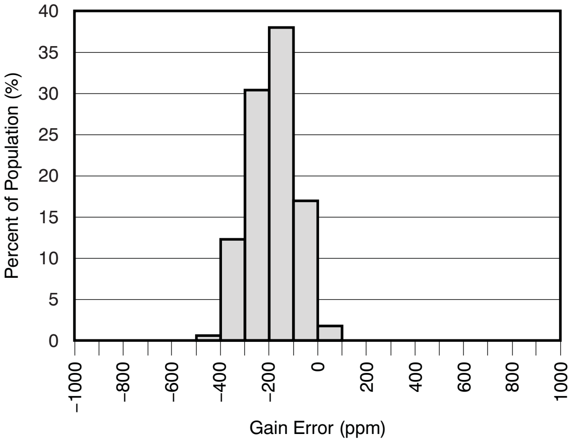


Figure 23. Voltage Mode Gain Error Distribution

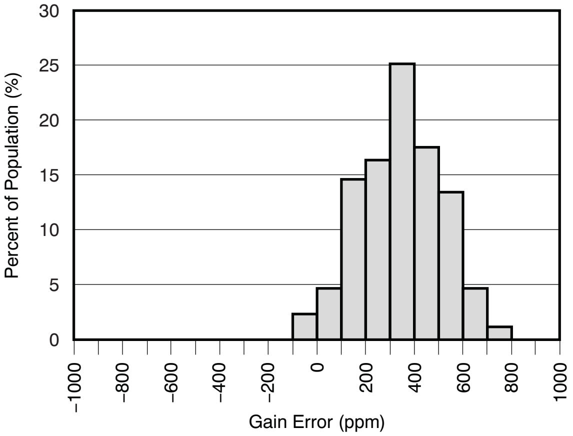


Figure 24. Current Mode Gain Error Distribution

Typical Characteristics (continued)

at T_A = 25°C and V+ = ±20 V, unless otherwise noted

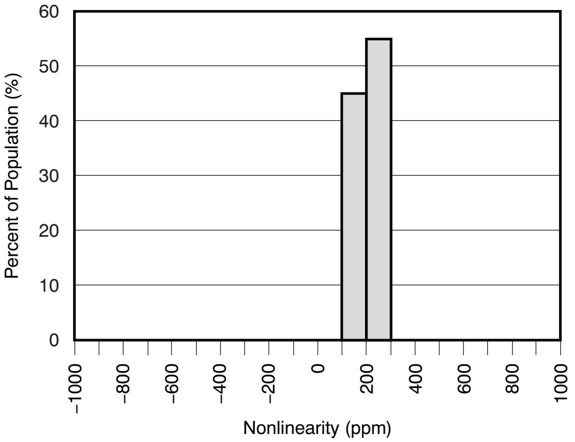


Figure 25. Voltage Mode Nonlinearity Distribution

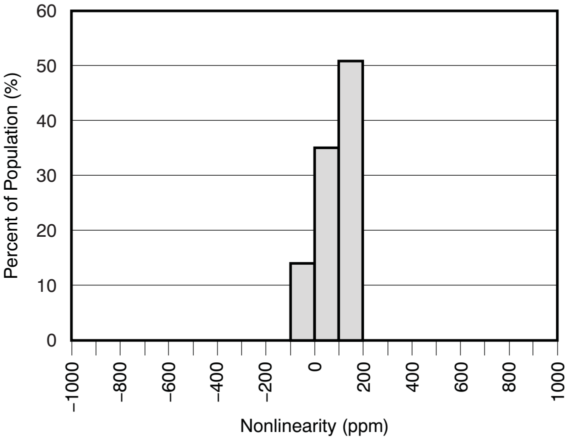


Figure 26. Current Mode Nonlinearity Distribution

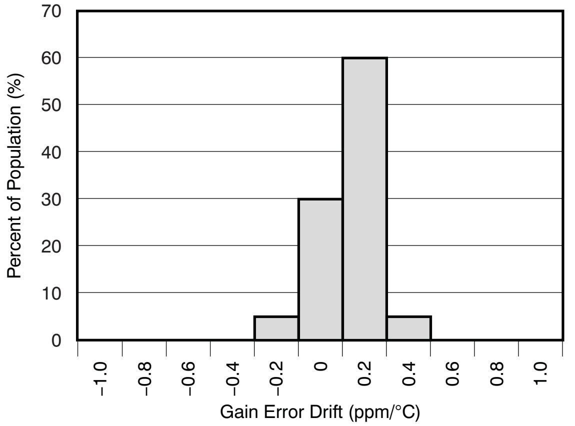


Figure 27. Voltage Mode Gain Error Drift Distribution

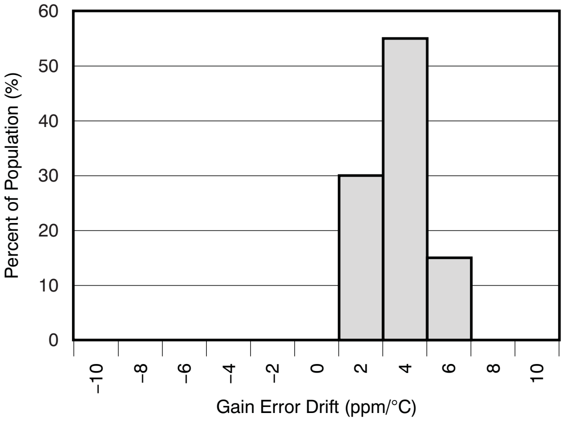


Figure 28. Current Mode Gain Error Drift Distribution

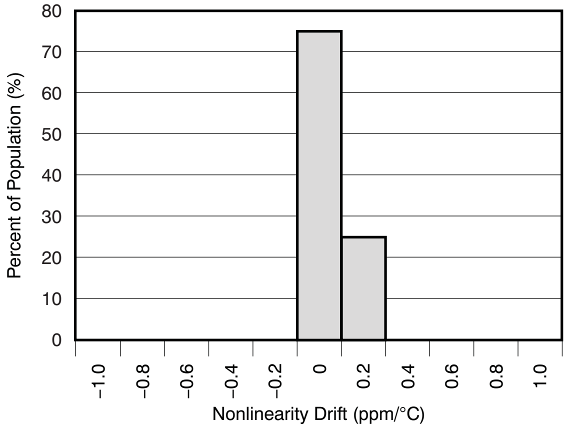


Figure 29. Voltage Mode Nonlinearity Drift Distribution

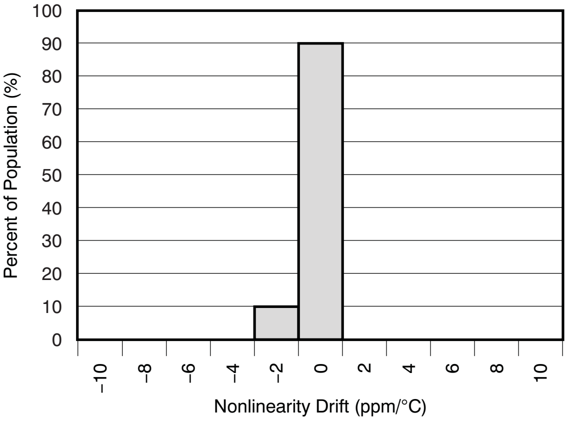


Figure 30. Current Mode Nonlinearity Drift Distribution

Typical Characteristics (continued)

at T_A = 25°C and V+ = ±20 V, unless otherwise noted

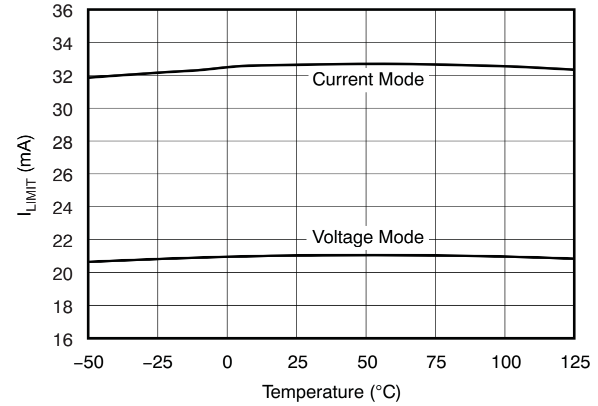


Figure 31. Positive Current Limit vs Temperature

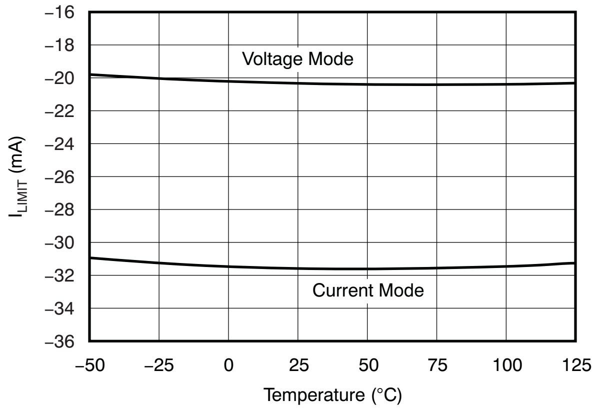
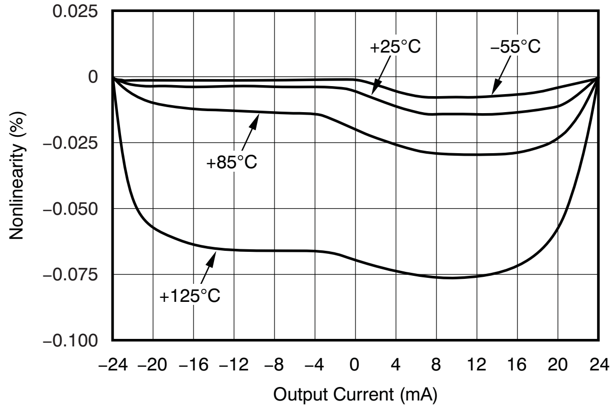
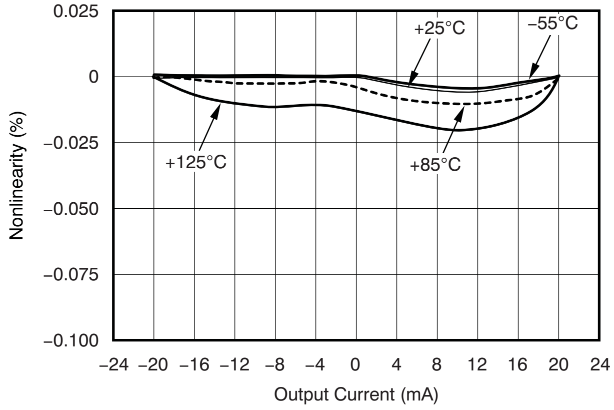


Figure 32. Negative Current Limit vs Temperature



(±24-mA End Point Calibration)

Figure 33. Nonlinearity vs Output Current



(±20-mA End Point Calibration)

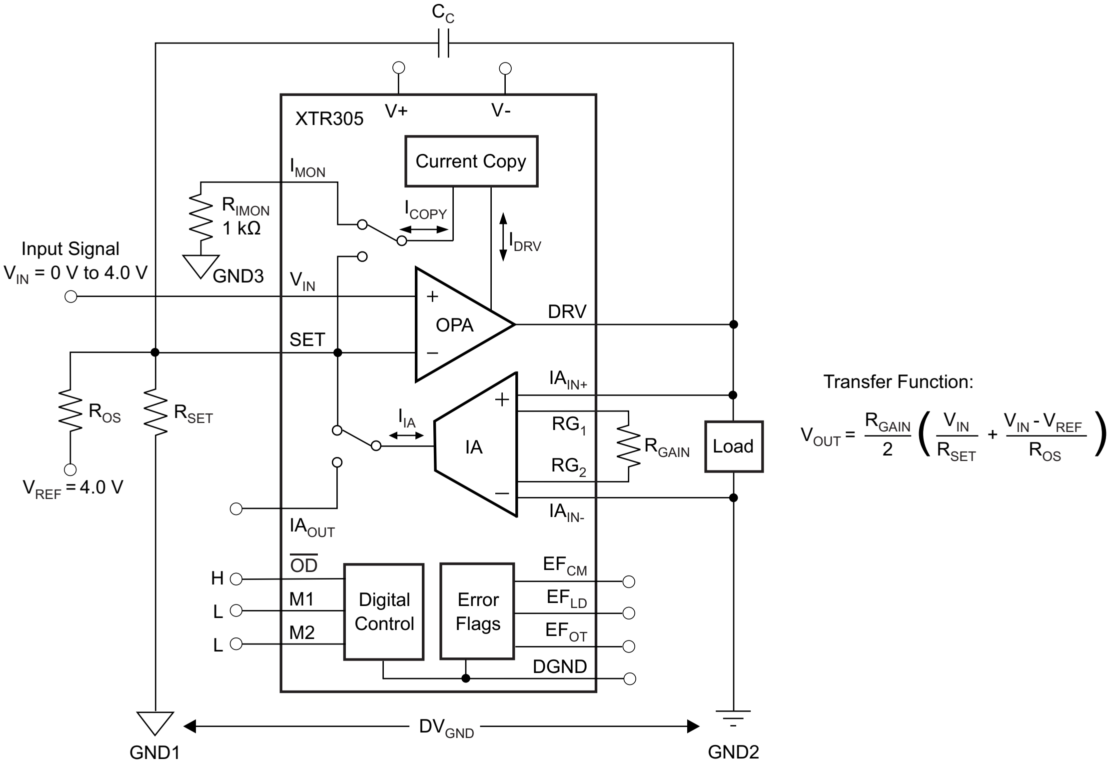
Figure 34. Nonlinearity vs Output Current

7 Detailed Description

7.1 Overview

Built on a robust high-voltage BiCMOS process, the XTR305 is designed to interface the 5-V or 3-V supply domain used for processors, signal converters, and amplifiers to the high-voltage and high-current industrial signal environment. The device is specified for up to ±20-V supply, but can also be powered asymmetrically (for example, +24 V and −5 V). It is designed to allow insertion of external circuit protection elements and drive large capacitive loads.

7.2 Functional Block Diagrams



Copyright © 2017, Texas Instruments Incorporated

Figure 35. Standard Circuit for Voltage Output Mode

Functional Block Diagrams (continued)

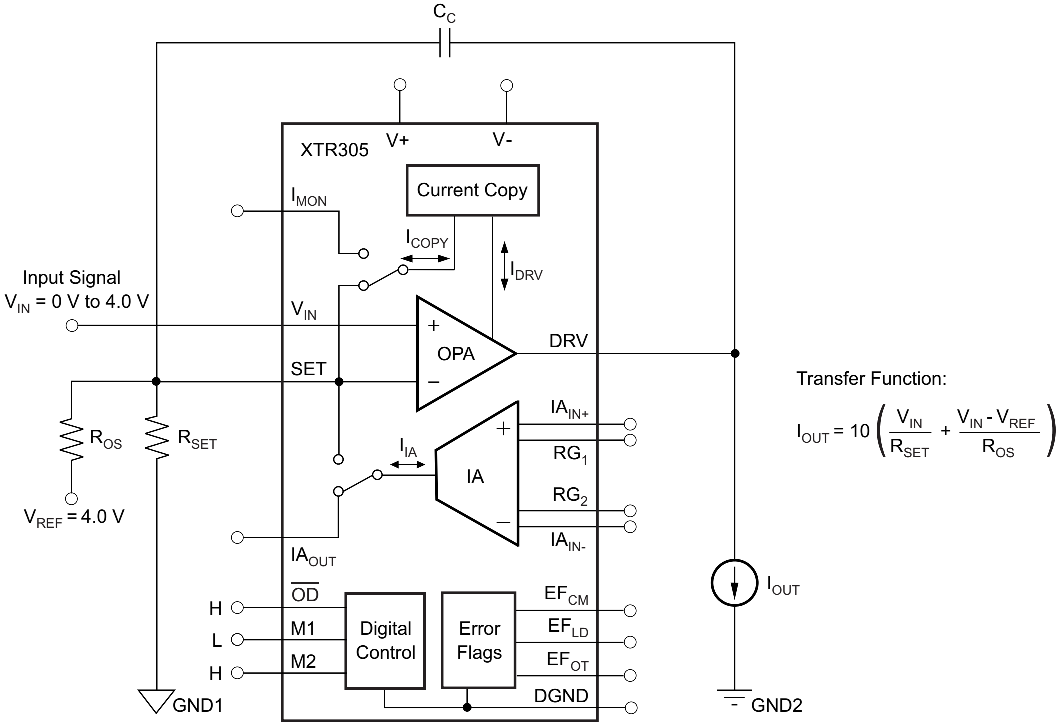


Figure 36. Standard Circuit for Current Output Mode

Functional Block Diagrams (continued)

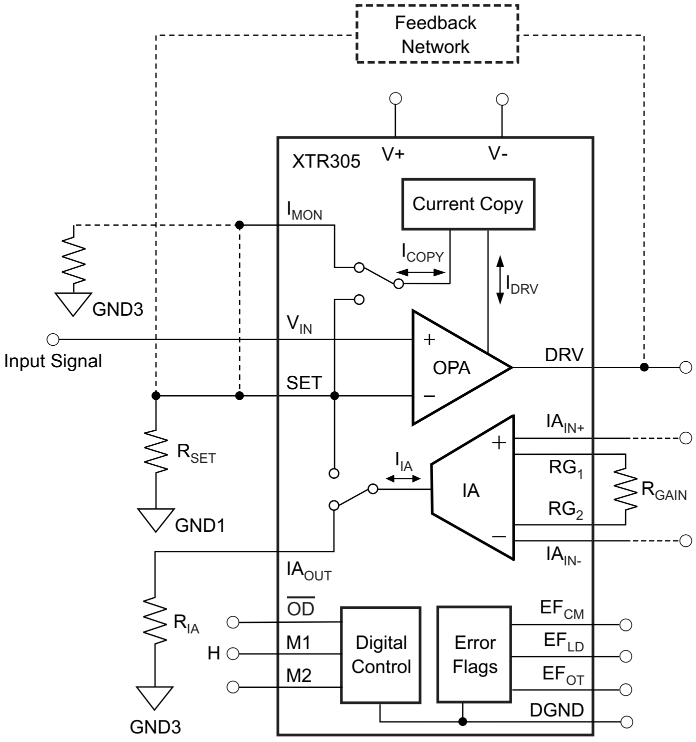


Figure 37. Standard Circuit for Externally Configured Mode

7.3 Feature Description

7.3.1 Functional Features

The XTR305 provides two basic functional blocks: an instrumentation amplifier (IA) and a driver that is a unique operational amplifier (OPA) for current or voltage output. This combination represents an analog output stage which can be digitally configured to provide either current or voltage output to the same terminal pin. Alternatively, it can be configured for independent measurement channels.

Three open collector error signals are provided to indicate output related errors such as overcurrent or open-load (EF_{LD}) or exceeding the common-mode input range at the IA inputs (EF_{CM}). An overtemperature flag (EF_{OT}) can be used to control output disable to protect the circuit. The monitor outputs (I_{MON} and IA_{OUT}) and the error flags offer optimal testability during operation and configuration. The I_{MON} output represents the current flowing into the load in voltage output mode, while the IA_{OUT} represents the voltage across the connectors in current output mode. Both monitor outputs can be connected together when used in current or voltage output mode because the monitor signals are multiplexed accordingly.

7.3.2 Current Monitor

In current output mode (M2 = high), the XTR305 provides high output impedance. A precision current mirror generates an exact 1/10th copy of the output current and this current is either routed to the summing junction of the OPA to close the feedback loop (in the current output mode) or to the I_{MON} pin for output current monitoring in other operating modes.

The high accuracy and stability of this current split results from a cycling chopper technique. This design eliminates the need for a precise shunt resistor or a precise shunt voltage measurement, which would require high common-mode rejection performance.

Feature Description (continued)

During a saturation condition of the DRV output (the error flag is active), the monitor output (I_{MON}) shows a current peak because the loop opens. Glitches from the current mirror chopper appear during this time in the monitor signal. This part of the signal cannot be used for measurement.

7.3.3 Error Flags

The XTR305 is designed for testability of its proper function and allows observation of the conditions at the load connection without disrupting service.

If the output signal is not in accordance to the transfer function, an error flag is activated (limited by the dynamic response capabilities). These error flags are in addition to the monitor outputs, I_{MON} and IA_{OUT}, which allow the momentary output current (in voltage mode) or output voltage (in current mode) to be read back.

This combination of error flag and monitor signal allows easy observation of the XTR305 for function and working condition, providing the basis for not only remote control, but also for remote diagnosis.

All error flags of the XTR305 have open collector outputs with a weak pullup of approximately 1 µA to an internal 5 V. External pullup resistors to the logic voltage are required when driving 3-V or 5-V logic.

The output sink current should not exceed 5 mA. This is just enough to directly drive optical-couplers, but a current-limiting resistor is required.

There are three error flags:

1. **IA Common-Mode Over Range (EF_{CM})**: goes low as soon as the inputs of the IA reach the limits of the linear operation for the input voltage. This flag shows noise from the saturated current mirrors which can be filtered with a capacitor to GND.
2. **Load Error (EF_{LD})**: indicates fault conditions driving voltage or current into the load. In voltage output mode it monitors the voltage limits of the output swing and the current limit condition caused from short or low load resistance. In current output mode it indicates a saturation into the supply rails from a high load resistance or open load.
3. **Overtemperature Flag (EF_{OT})**: a digital output that goes low if the chip temperature reaches a temperature of 140°C and resets as soon as it cools down to 125°C. It does not automatically shut down the output; it allows the user system to take action on the situation. If desired, this output can be connected to output disable ($\overline{OD}$) which disables the output and therefore removes the source of power. This connection acts like an automatic shut down, but requires a 2.2-kΩ external pullup resistor to safely override the internal current sources. The IA channel is not affected, which allows continuous observation of the voltage at the output.

7.3.4 Power On/Off Glitch

When power is turned on or off, most analog amplifiers generate some glitching of the output because of internal circuit thresholds and capacitive charges. Characteristics of the supply voltage, as well as its rise and fall time, directly influence output glitches. Load resistance and capacitive load also affect the amplitude.

The output disable control ($\overline{OD}$) cannot fully suppress glitches during power-on and power-off, but reduces the energy significantly. The glitch consists of a small amount of current and capacitive charge (voltage) that reacts with the resistive and capacitive load. The bias current of the IA inputs that are normally connected to the output also generate a voltage across the load.

Feature Description (continued)

Figure 38 indicates no glitches when transitioning between disable and enable. This measurement is made with a load resistance of 1 kΩ and tested in the circuit configuration of Figure 40.

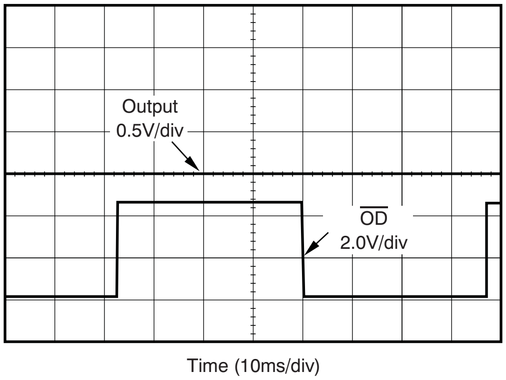


Figure 38. Output Signal During Toggle of $\overline{\text{OD}}$

When the power is off or with low supply, the output is diode clamped to the momentary supply voltage, but can float while output disabled within those limits unless terminated. Only an external switch (relays or opto-relays) can isolate the output under such conditions. Refer to Figure 39 for an illustration of this configuration. The same consideration applies if low impedance zero output is required, even during power off.

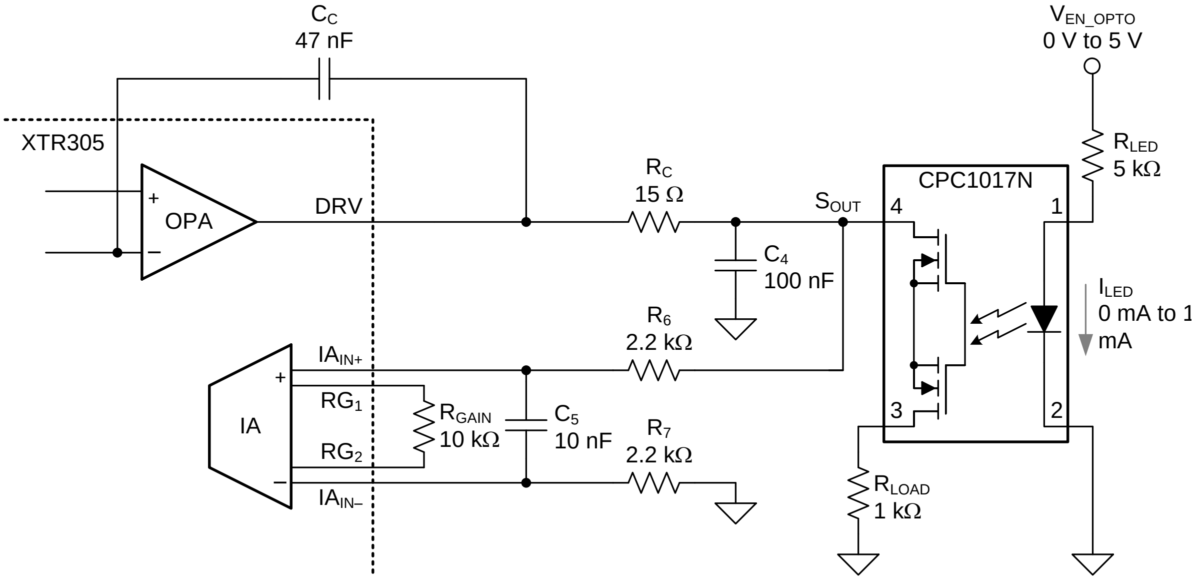


Figure 39. Example for Opto-Relay Output Isolation

7.4 Device Functional Modes

The XTR305 has a three functional modes: voltage output mode as shown in Figure 35, current output mode as shown in Figure 36, and externally configured mode as shown in Figure 37.

8 Application and Implementation

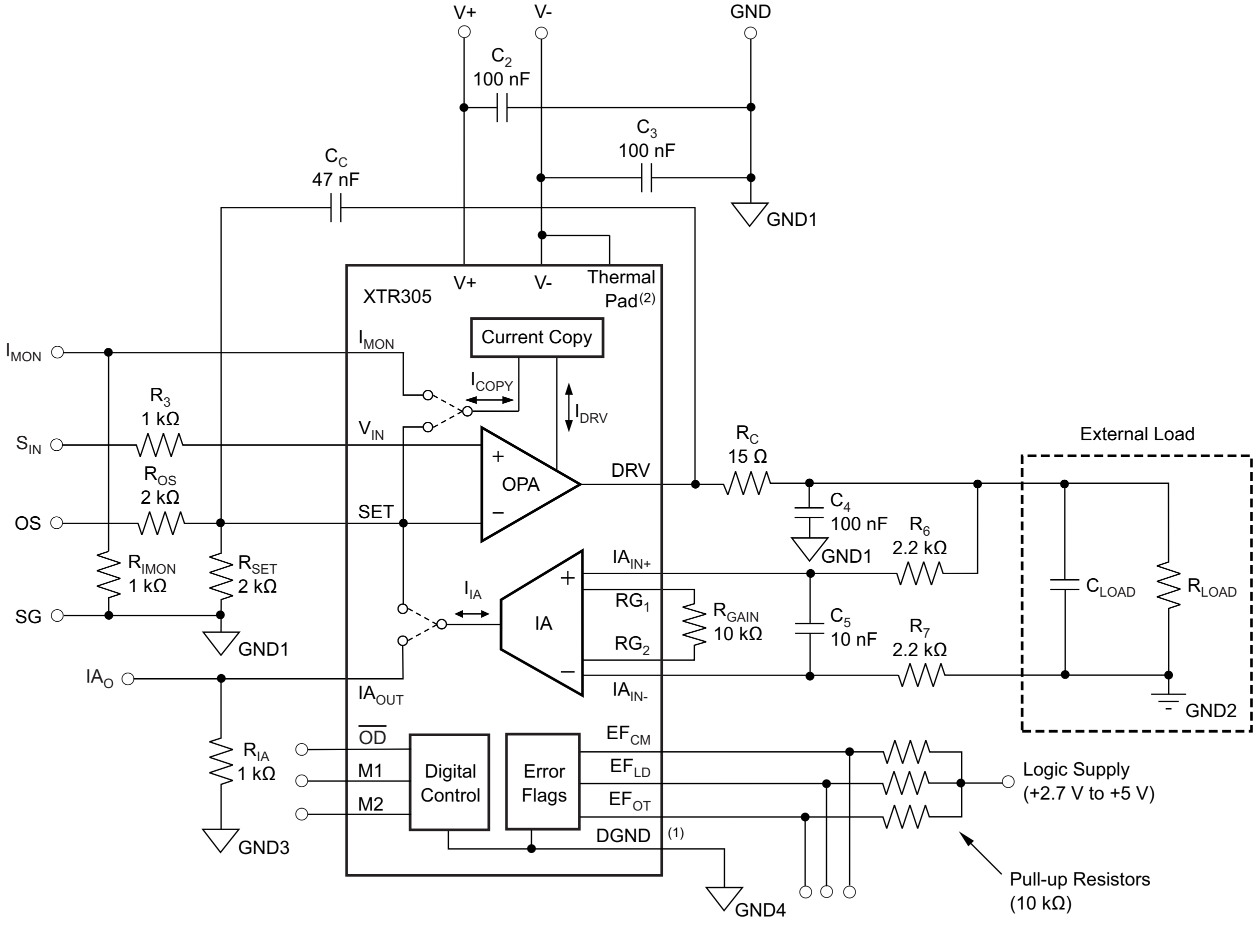
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following sections provide details regarding the typical application of the XTR305 using three different functional modes: voltage output mode as shown in Figure 35, current output mode as shown in Figure 36, and externally configured mode as shown in Figure 37.

8.2 Typical Application



(1) See the *Electrical Characteristics: Power and Digital* and *Digital I/O and Ground Considerations* section for operating limits of DGND.

(2) Connect thermal pad to V−.

Figure 40. Standard Circuit Configuration

8.2.1 Design Requirements

Consider the following information during XTR305 circuit configuration:

- Recommended bypassing: 100 nF or more for supply bypassing at each supply.
- R_{IMON} can be in the kΩ range or short-circuited if not used. Do not leave this current output unconnected — it would saturate the internal current source. The current at this I_{MON} output is I_{DRV} / 10. Therefore, V_{IMON} = R_{IMON} (I_{DRV} /1 0).
- R_3 is not required but can match R_{SET} (or $R_{SET}||R_{OS}$) to compensate for the bias current.
- R_{IA} can be short-circuited if not used. Do not leave this current output unconnected. R_{GAIN} is selected to 10 kΩ to match the output of 10 V with 20 mA for the equal input signal.
- R_C ensures stability for unknown load conditions and limits the current into the internal protection diodes. C_4 helps protect the device. Overvoltage clamp diodes (standard 1N4002) might be necessary to protect the output.
- R_6, R_7, and C_5 protect the IA.
- R_{LOAD} and C_{LOAD} represent the load resistance and load capacitance.
- R_{SET} defines the transfer gain. It can be split to allow a signal offset and, therefore, allow a 5-V single-supply digital-to-analog converter (DAC) to control a ±10-V or ±20-mA output signal.

The XTR305 can be used with asymmetric supply voltages; however, the minimum negative supply voltage must be equal to or more negative than −3 V (typically −5 V). This supply value ensures proper control of 0 V and 0 mA with wire resistance, ground offsets, and noise added to the output. For positive output signals, the current requirement from this negative voltage source is less than 5 mA.

GND1 through GND4 must be selected to fulfill specified operating ranges. DGND must be in the range of (V−) ≤ DGND ≤ (V+) −7 V.

8.2.2 Detailed Design Procedure

8.2.2.1 Voltage Output Mode

In voltage output mode (M1 and M2 are connected low or left unconnected), the feedback loop through the IA provides high impedance remote sensing of the voltage at the destination, compensating the resistance of a protection circuit, switches, wiring, and connector resistance. The output of the IA is a current that is proportional to the input voltage. This current is internally routed to the OPA summing junction through a multiplexer, as shown in Figure 41.

A 1:10 copy of the output current of the OPA can be monitored at the I_{MON} pin. This output current and the known output voltage can be used to calculate the load resistance or load power.

During an output short-circuit or an overcurrent condition the XTR305 output current is limited and EF_{LD} (load error, active low) flag is activated.

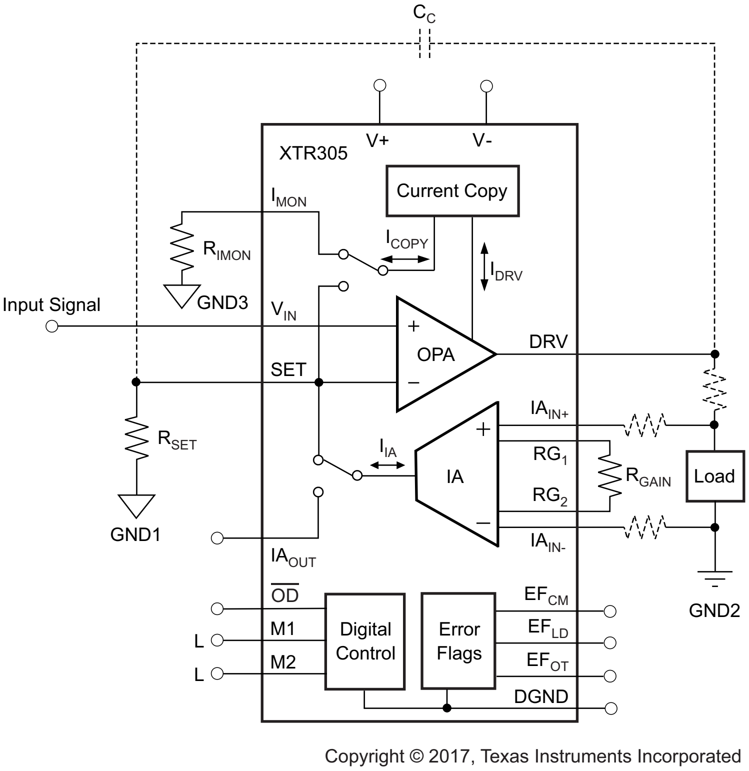


Figure 41. Simplified Voltage Output Mode Configuration

Applications not requiring the remote sense feature can use the OPA in stand-alone operation (M1 = high). In this case, the IA is available as a separate input channel.

The IA gain can be set by two resistors, R_{GAIN} and R_{SET} (Equation 1):

$$V_{OUT} = \frac{R_{GAIN}}{2R_{SET}} V_{IN} \tag{1}$$

or when adding an offset, V_{REF}, to get bidirectional output with a single-ended input shown in Equation 2:

$$V_{OUT} = \frac{R_{GAIN}}{2} \left(\frac{V_{IN}}{R_{SET}} + \frac{V_{IN} - V_{REF}}{R_{OS}} \right) \tag{2}$$

The R_{SET} resistor is also used in current output mode. Therefore, it is useful to define R_{SET} for the current mode, then set the ratio between current and voltage span with R_{GAIN}.

8.2.2.2 Current Output Mode

The XTR305 does not require a shunt resistor for current control because it uses a precise current mirror arrangement.

In current output mode (M1 connected low, or left unconnected and M2 connected high), a precise copy of 1/10th of the output is internally routed back to the summing junction of the OPA through a multiplexer, closing the control loop for the output current.

The OPA driver can deliver more than ±24 mA within a wide output voltage range. An open-output condition or high-impedance load that prevents the flow of the required current activates the EF_{LD} flag and the IA can become overloaded and draw greater than 7-mA saturation current.

While in current output mode, a current (I_{IA}) that is proportional to the voltage at the IA input is routed to IA_{OUT} and can be used to monitor the load voltage. A resistor converts this current into voltage. This arrangement makes level shifting easy.

Alternatively, the IA can be used as an independent monitoring channel. If this output is not used, connect it to GND to maintain proper function of the monitor stage, as shown in Figure 42.

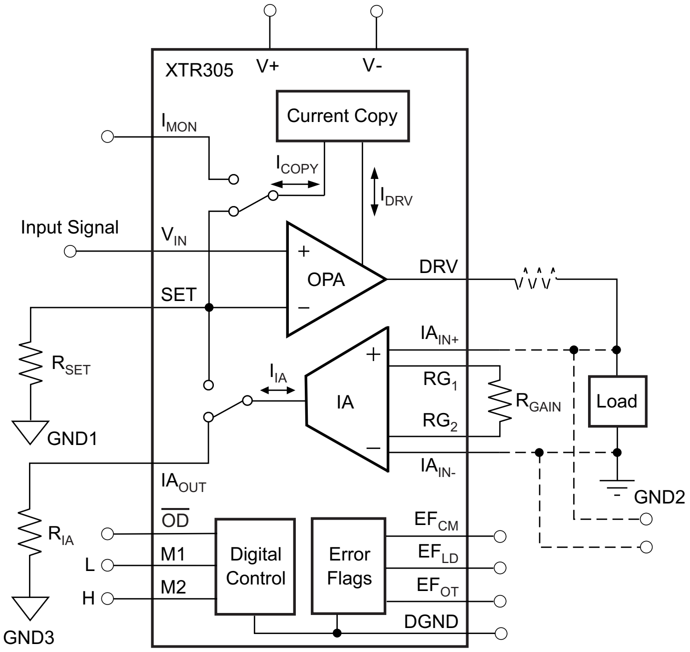


Figure 42. Simplified Current Output Mode Configuration

The transconductance (gain) can be set by the resistor, R_{SET}, according to Equation 3:

$$I_{OUT} = \frac{10}{R_{SET}} V_{IN} \tag{3}$$

or when adding an offset V_{REF} to get bidirectional output with a single-ended input shown in Equation 4:

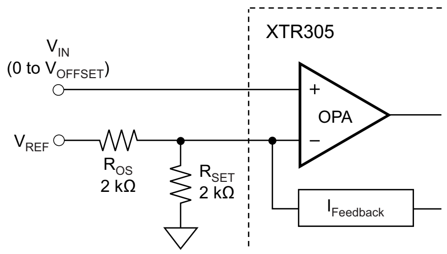
$$I_{OUT} = 10\left(\frac{V_{IN}}{R_{SET}} + \frac{V_{IN} - V_{REF}}{R_{OS}}\right) \tag{4}$$

8.2.2.3 Input Signal Connection

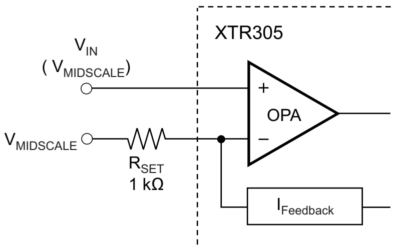
It is possible to drive the XTR305 with a unidirectional input signal and still get a bidirectional output by adding an additional resistor, R_{OS}, and an offset voltage signal, V_{REF}. It can be a mid-point voltage or a signal to shift the output voltage to a desired value.

This design is illustrated in Figure 43a, Figure 43b, and Figure 43c. As with a normal operational amplifier, there are several options for offset-shift circuits. The input can be connected for inverting or noninverting gain. Unlike many op amp input circuits, however, this configuration uses current feedback, which removes the voltage relationship between the noninverting input and output potential because there is no feedback resistor.

a) Noninverting Input



b) Noninverting Input



c) Inverting Input (V_{REF} = V_{OFFSET})

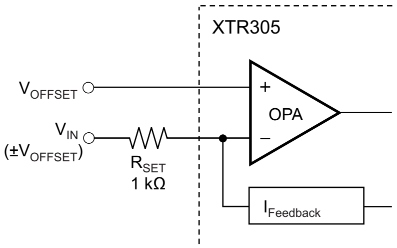


Figure 43. Circuit Options for Op Amp Output Level Shifting

The input bias current effect on the offset voltage can be reduced by connecting a resistor in series with the positive input that matches the approximate resistance at the negative input. This resistor placed close to the input pin acts as a damping element and makes the design less sensitive to RF noise. See R_3 in Figure 40.

8.2.2.4 Externally-Configured Mode: OPA and IA

It is possible to use the precision of the operational amplifier (OPA) and instrumentation amplifier (IA) independently from each other by configuring the digital control pins (M1 high). In this mode, the IA output current is routed to IA_{OUT} and the copy of the OPA output current is routed to I_{MON}, as shown in Figure 37.

This mode allows external configuration of the analog signal routing and feedback loop.

The current output IA has high input impedance, low offset voltage and drift, and very high common-mode rejection ratio. An external resistor (R_{IA}) can be used to convert the output current of the IA (I_{IA}) to an output voltage. The gain is given by Equation 5:

$$I_{IA} = \frac{2}{R_{GAIN}} V_{IN} \text{ or } V_{IA} = \frac{2R_{IA}}{R_{GAIN}} V_{IN} \quad (5)$$

The OPA provides low drift and high voltage output swing that can be used like a common operational amplifier by connecting a feedback network around it. In this mode, the copy of the output current is available at the I_{MON} pin (it includes the current into the feedback network). It provides an output current limit for protection, which can be set between two ranges by M2. The error flag indicates an overcurrent condition, as well as indicating driving the output into the supply rails.

Alternatively, the feedback can be closed through the I_{MON} pin to create a precise voltage-to-current converter.

8.2.2.5 Driver Output Disable

The OPA output (DRV) can be switched to a high-impedance mode by driving the $\overline{OD}$ control pin low. This input can be connected to the overtemperature flag, EF_{OT}, and a pullup resistor to protect the IC from over-temperature by disconnecting the load.

The output disable mode can be used to sense and measure the voltage at the IA input pins without loading from the DRV output. This mode allows testing of any voltage present at the I/O connector. However, consider the bias current of the IA input pins.

The digital control inputs, M1 and M2, set the four operation modes of the XTR305 as shown in Table 1. When M1 is asserted low, M2 determines voltage or current mode and the corresponding appropriate current limit (I_{SC}) setting. When M1 is high, the internal feedback connections are opened; IA_{OUT} and I_{MON} are both connected to the output pins; and M2 only determines the current limit (I_{SC}) setting.

M1 and M2 are pulled low internally with 1 μA. Terminate these two pins to avoid noise coupling. Output disable ($\overline{OD}$) is internally pulled high with approximately 1 μA. When connecting $\overline{OD}$ to EF_{OT}, a 2.2-kΩ pullup resistor is recommended.

Table 1. Summary of Configuration Modes[1]

M1	M2	MODE	DESCRIPTION
L	L	V_{OUT}	Voltage output mode, I_{SC} = 20 mA
L	H	I_{OUT}	Current output mode, I_{SC} = 32 mA
H	L	Ext	IA and I_{MON} on external pins, I_{SC} = 20 A
H	H	Ext	IA and I_{MON} on external pins, I_{SC} = 32 mA

(1) $\overline{OD}$ is a control pin independent of M1 or M2.

8.2.2.6 Driving Capacitive Loads and Loop Compensation

For normal operation, the driver OPA and the IA are connected in a closed loop for voltage output. In current output mode, the current copy closes the loop directly.

In current output mode, loop compensation is not critical, even for large capacitive loads. However, in voltage output mode, the capacitive load, together with the source impedance and the impedance of the protection circuit, generates additional phase lag. The IA input might also be protected by a low-pass filter that influences phase in the closed loop.

The loop compensation low-pass filter consists of C_C and the parallel resistance of R_{OS} and R_{SET}. For loop stability with large capacitive load, the external phase shift has to be added to the OPA phase. With C_C, the voltage gain of the OPA has to approach zero at the frequency where the total phase approaches 180° + 135°.

The best stability for large capacitive loads is provided by adding a small resistor, R_C (15 Ω). See the *Output Protection* section.

An empirical method of evaluation is using a square wave input signal and observing the settling after transients. Use small signal amplitudes only—steep signal edges cause excessive current to flow into the capacitive load and may activate the current limit, which hides or prevents oscillation. A small-signal oscillation can be hidden from large capacitive loads, but observing the I_{MON} output on an appropriate resistor (use a similar value like $R_{SET}||R_{OS}$) would indicate stability issues. Note that noise pulses at I_{MON} during overload (EF_{LD} active) are normal and are caused by cycling of the current mirror.

The voltage output mode includes the IA in the loop. An additional low-pass filter in the input reverses the phase and therefore increases the signal bandwidth of the loop, but also increases the delay. Again, loop stability has to be observed. Overloading the IA disconnects the closed loop and the output voltage rails.

8.2.2.7 Internal Current Sources, Switching Noise, and Settling Time

The accuracy of the current output mode and the DC performance of the IA rely on dynamically-matched current mirrors.

Identical current sources are rotated to average out mismatch errors. It can take several clock cycles of the internal 100-kHz oscillator (or a submultiple of that frequency) to reach full accuracy. This may dominate the settling time to the 0.1% accuracy level and can be as much as 100 µs in current output mode or 40 µs in voltage output mode.

A small portion of the switching glitches appear at the DRV output, and also at the I_{MON} and IA_{MON} outputs. The standard circuit configuration, with R_C, C_4, and C_C, which are required for loop compensation and output protection, also helps reduce the noise to negligible levels at the signal output. If necessary, the monitor outputs can be filtered with a shunt capacitor.

8.2.2.8 IA Structure, Voltage Monitor

The instrumentation amplifier has high-impedance NPN transistor inputs that do not load the output signal, which is especially important in current output mode. The output signal is a controlled current that is multiplexed either to the SET pin (to close the voltage output loop) or to IA_{OUT} (for external access).

The principal circuit is shown in Figure 44. The two input buffer amplifiers reproduce the input difference voltage across R_{GAIN}. The resulting current through this resistor is bidirectionally mirrored to the output. That mirroring results in the transfer function of Equation 6:

$$I_{IA} = IA_{OUT} = 2\,\frac{(IA_{IN+} - IA_{IN-})}{R_{GAIN}} \qquad (6)$$

The accuracy and drift of R_{GAIN} defines the accuracy of the voltage to current conversion. The high accuracy and stability of the current mirrors result from a cycling chopper technique.

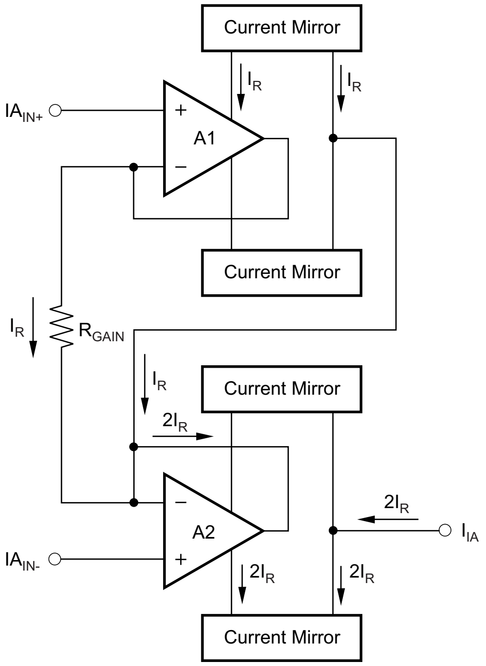


Figure 44. IA Block Diagram

The output current, IA_{OUT}, of the instrumentation amplifier is limited to protect the internal circuitry. This current limit has two settings controlled by the state of M2 (see *Electrical Characteristics: Instrumentation Amplifier (IA)*, Short-Circuit Current specification).

NOTE

If R_{SET} is too small, the current output limitation of the instrumentation amplifier can disrupt the closed loop of the XTR305 in voltage output mode.

With M2 = low, the nominal R_{GAIN} of 10 kΩ allows an input voltage of 20 V_{PP}, which produces an output current of 4 mA_{PP}. When using lower resistors for R_{GAIN} that can allow higher currents, the IA output current limitation must be taken into account.

8.2.2.9 Digital I/O and Ground Considerations

The XTR305 offers voltage output mode, current output mode, external configuration, and instrumentation mode (voltage input). In addition, the internal feedback mode can be disconnected and external loop connections can be made. These modes are controlled by M1 and M2 (see Table 1). The $\overline{OD}$ input pin controls enable or disable of the output stage ($\overline{OD}$ is active low).

The digital I/O is referenced to DGND and signals on this pin must remain within 5 V of the DGND potential. This DGND pin carries the output low-current (sink current) of the logic outputs. DGND can be connected to a potential within the supply voltage but needs to be 8 V below the positive supply. Proper connection avoids current from the digital outputs flowing into the analog ground.

CAUTION

The DGND has normally reverse-biased diodes connected to the supply. Therefore, high and destructive currents could flow if DGND is driven beyond the supply rails by more than a diode forward voltage. *Avoid this condition during power on and power off.*

8.2.2.10 Output Protection

The XTR305 is intended to operate in a harsh industrial environment. Therefore, a robust semiconductor process was chosen for this design. However, some external protection is still required.

The instrumentation amplifier inputs can be protected by external resistors that limit current into the protection cell behind the IC pins, as shown in Figure 45. This cell conducts to the power-supply connection through a diode as soon as the input voltage exceeds the supply voltage. The circuit configuration example shows how to arrange these two external resistors.

The bias current is best cancelled if both resistors are equal. The additional capacitor reduces RF noise in the input signal to the IA.

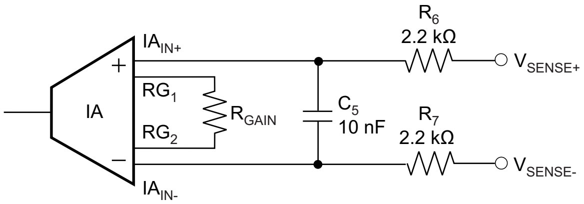


Figure 45. Current-Limiting Resistors

The load connection to the DRV output must be low impedance; therefore, external protection diodes may be necessary to handle excessive currents, as shown in Figure 46. The internal protection diodes start to conduct earlier than a normal external PN-type diode because they are affected by the higher die temperature. Therefore, either Schottky diodes are required, or an additional resistor (R_C) can be placed in series with the input. An example of this protection is shown in Figure 46. Assuming the standard diodes limit the voltage to 1.4 V and the internal diodes clamp at 0.7 V, this resistor can limit the current into the internal protection diodes to 50 mA shown in Equation 7:

$$\frac{(1.4V - 0.7V)}{15\Omega} = 47mA \tag{7}$$

R_C is also part of the recommended loop compensation. C_4 helps protect the output against RFI and high-voltage spikes.

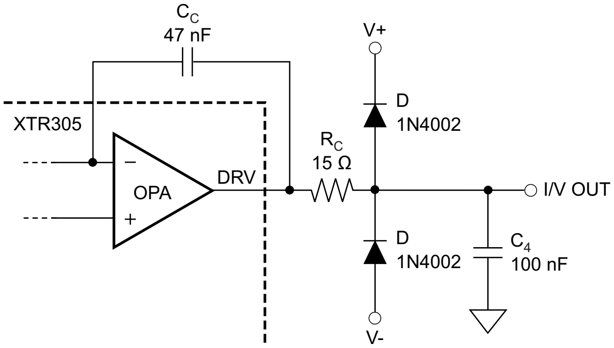
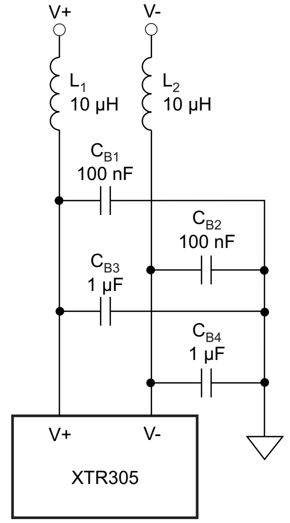


Figure 46. Example for DRV Output Protection

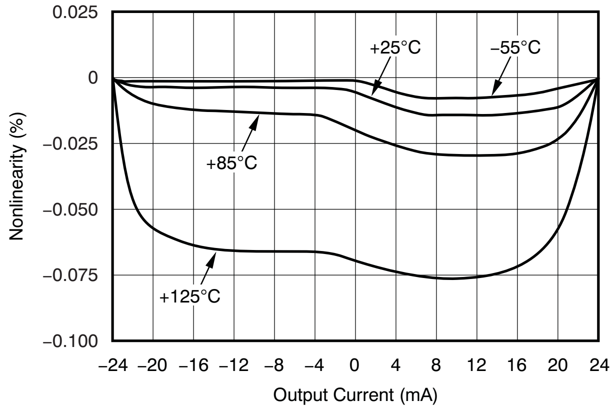
8.2.3 Application Curves

The nonlinearity of the XTR305 when operating in current output mode is shown in Figure 47 and Figure 48.



(±20-mA End Point Calibration)

Figure 47. Nonlinearity vs Output Current



(±24-mA End Point Calibration)

Figure 48. Nonlinearity vs Output Current

9 Power Supply Recommendations

Built on a robust high-voltage BiCMOS process, the XTR305 is designed to interface the 5-V or 3-V supply domain used for processors, signal converters, and amplifiers to the high-voltage and high-current industrial signal environment. The device is specified for up to ±20-V supply, but can also be powered asymmetrically (for example, +24 V and −5 V). XTR305 is designed to allow insertion of external circuit protection elements and drive large capacitive loads.

10 Layout

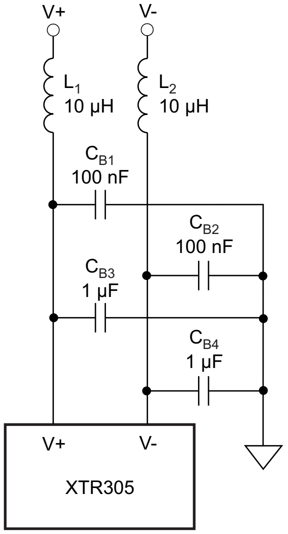
10.1 Layout Guidelines

Supply bypass capacitors must be close to the package and connected with low-impedance conductors. Avoid noise coupled into R_{GAIN}, and observe wiring resistance. For thermal management, see the *VQFN Package and Heat Sinking* section.

Layout for the XTR305 is not critical; however, its internal current chopping works best with good (low dynamic impedance) supply decoupling. Therefore, avoid through-hole contacts in the connection to the bypass capacitors or use multiple through-hole contacts. Switching noise from power supplies should be filtered enough to reduce influence on the circuit. Small resistors (2-Ω, for example) or damping inductors in series with the supply connection (between the DC-DC converter and the XTR circuit) act as a decoupling filter together with the bypass capacitor as shown in Figure 49.

Resistors connected close to the input pins help dampen environmental noise coupled into conductor traces. Therefore, place the OPA input- and IA input-related resistors close to the package. Also, avoid additional wire resistance in series to R_{SET}, R_{OS}, and R_{GAIN} (observe the reliability of the through-hole contacts), because this resistance could produce gain and offset error as well as drift; 1 Ω is already 0.1% of the 1-kΩ resistor.

The exposed lead-frame die pad on the bottom of the package must be connected to V−, pin 11 (see the *VQFN Package and Heat Sinking* section for more details).



Copyright © 2017, Texas Instruments Incorporated

Figure 49. Suggested Supply Decoupling for Noisy Chopper-Type Supplies

10.2 Layout Example

A detailed layout example can be found in the technical document *XTR300EVM*. This document is available for download at www.ti.com. The example layout is also shown in Figure 50.

Layout Example (continued)

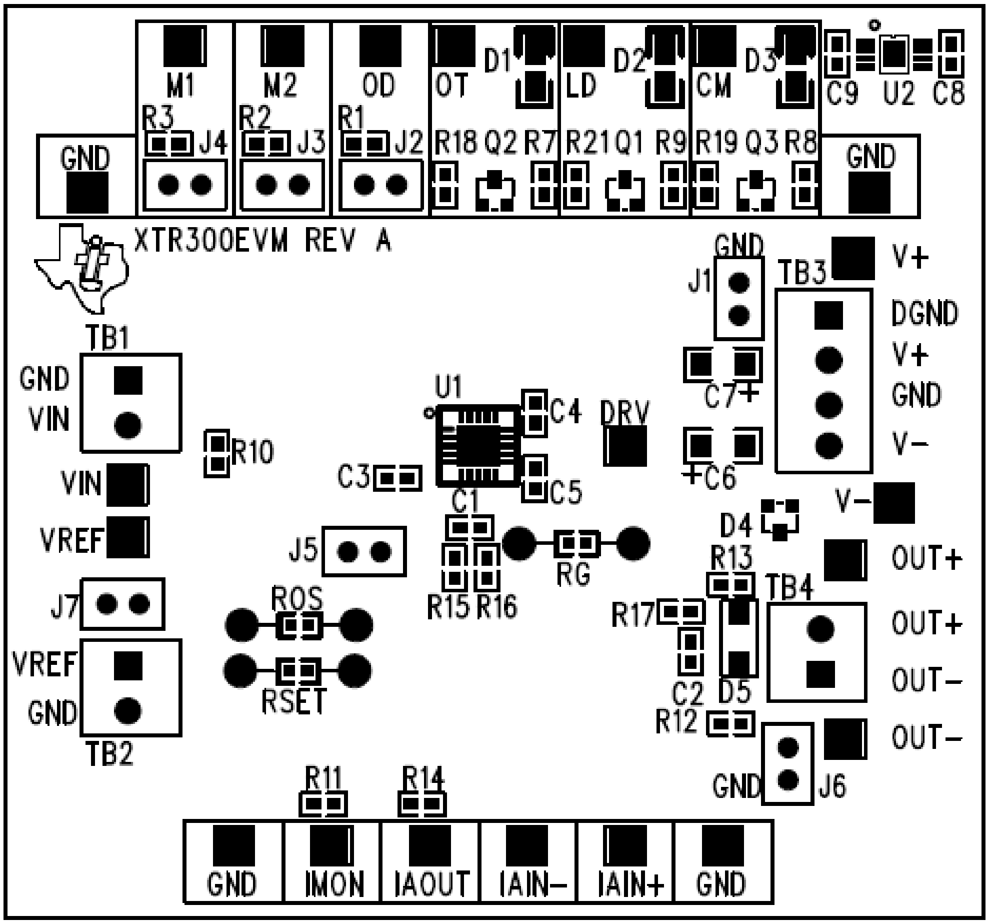


Figure 50. Layout Example

10.3 VQFN Package and Heat Sinking

The XTR305 is available in a VQFN package. This leadless, near-chip-scale package maximizes board space and enhances thermal and electrical characteristics of the device through an exposed thermal pad.

Packages with an exposed thermal pad are specifically designed to provide excellent power dissipation, but printed circuit board (PCB) layout greatly influences overall heat dissipation. The thermal resistance from junction-to-ambient (θ_{JA}) is specified for the packages with the exposed thermal pad soldered to a normalized PCB, as described in the technical brief *PowerPAD™ Thermally-Enhanced Package*. See also *EIA/JEDEC Specifications JESD51-0 to 7*, *VQFN/SON PCB Attachment*, and *Quad Flatpack No-Lead Logic Packages*. These documents are available for download at www.ti.com.

NOTE

All thermal models have an accuracy variation of ±20%.

Component population, layout of traces, layers, and air flow strongly influence heat dissipation. Worst-case load conditions should be tested in the real environment to ensure proper thermal conditions. Minimize thermal stress for proper long-term operation with a junction temperature well below +125°C.

The exposed lead-frame die pad on the bottom of the package must be connected to the V− pin.

10.4 Power Dissipation

Power dissipation depends on power supply, signal, and load conditions. It is dominated by the power dissipation of the output transistors of the OPA. For DC signals, power dissipation is equal to the product of output current, I_{OUT} and the output voltage across the conducting output transistor (V_S – V_{OUT}).

It is very important to note that the temperature protection does not shut the device down in overtemperature conditions, unless the EF_{OT} pin is connected to the output enable pin $\overline{OD}$; see the *Driver Output Disable* section.

The power that can be safely dissipated in the package is related to the ambient temperature and the heat sink design and conditions. The VQFN package with an exposed thermal pad is specifically designed to provide excellent power dissipation, but board layout greatly influences the heat dissipation.

To appropriately determine the required heat sink area, calculate required power dissipation; also consider the relationship between power dissipation and thermal resistance to minimize overheat conditions and allow for reliable long-term operation.

The heat-sinking efficiency can be tested using the EF_{OT} output signal. This output goes low at nominally 140°C junction temperature (assume 6% tolerance). With full power dissipation (for example, maximum current into a 0-Ω load), the ambient temperature can be slowly raised until the OT flag goes low. This flag would indicate the minimum heat sinking for the usable operation condition.

The recommended landing pattern for the VQFN package is shown at the end of this data sheet.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:
- *PowerPAD™ Thermally-Enhanced Package*
- *EIA/JEDEC Specifications JESD51-0 to 7, VQFN/SON PCB Attachment*
- *Quad Flatpack No-Lead Logic Packages*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTR305IRGWR	ACTIVE	VQFN	RGW	20	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	XTR 305	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

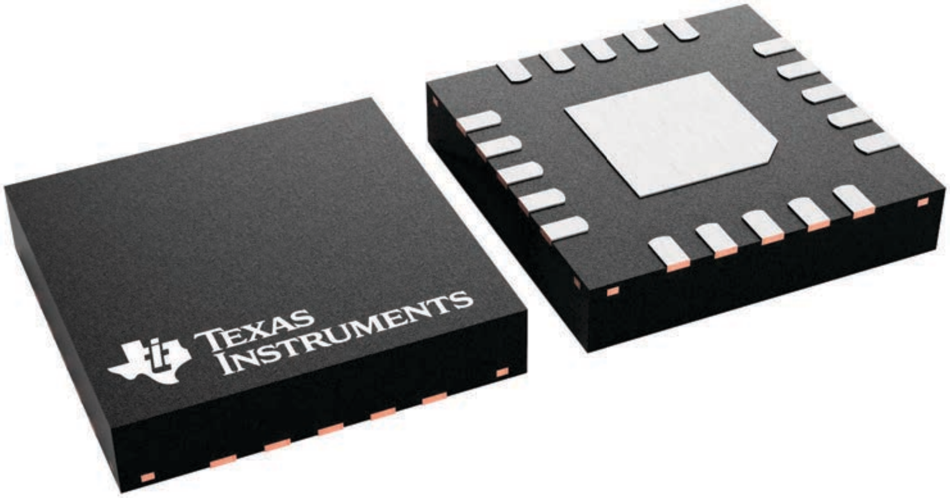
RGW 20

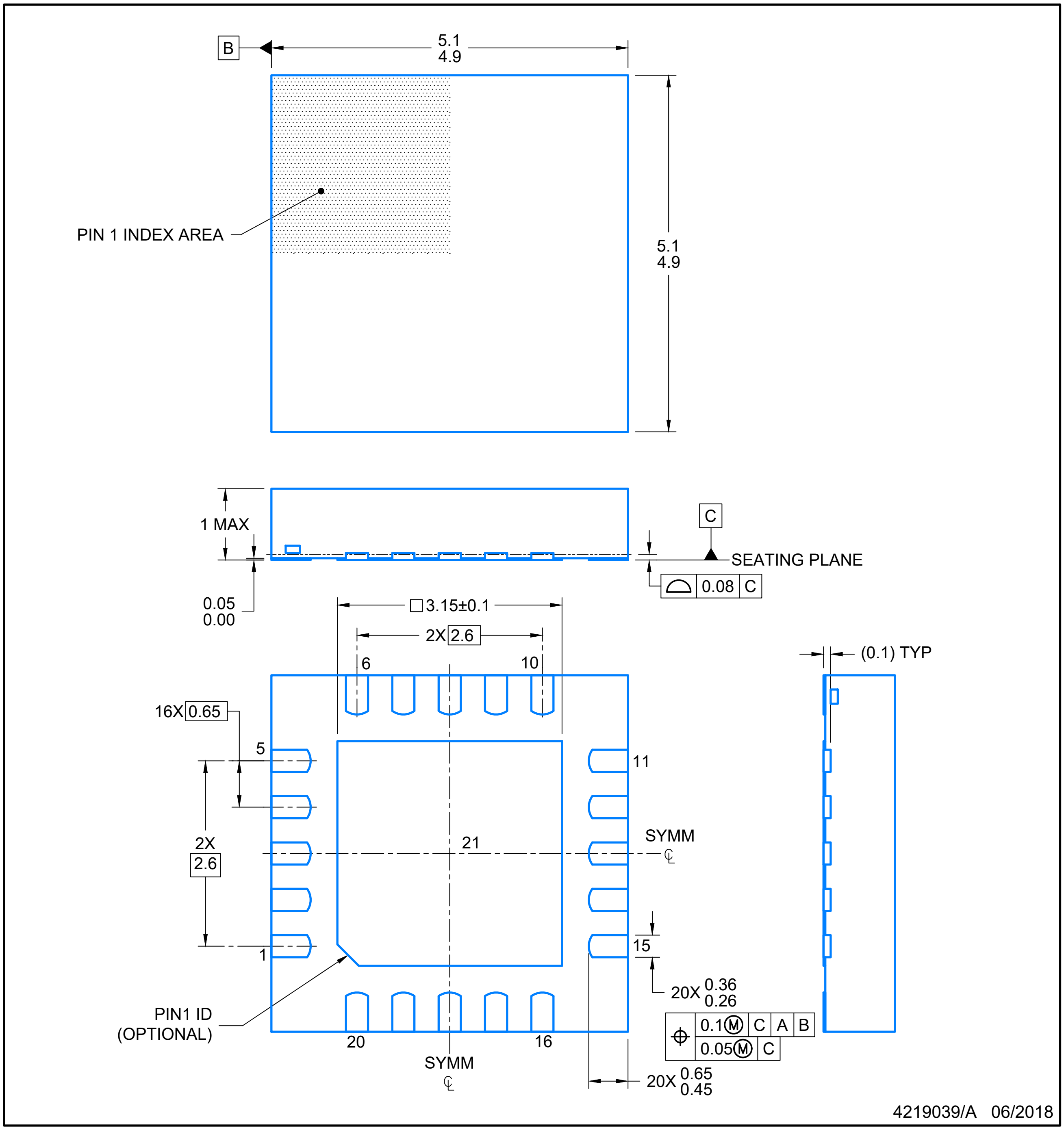
VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

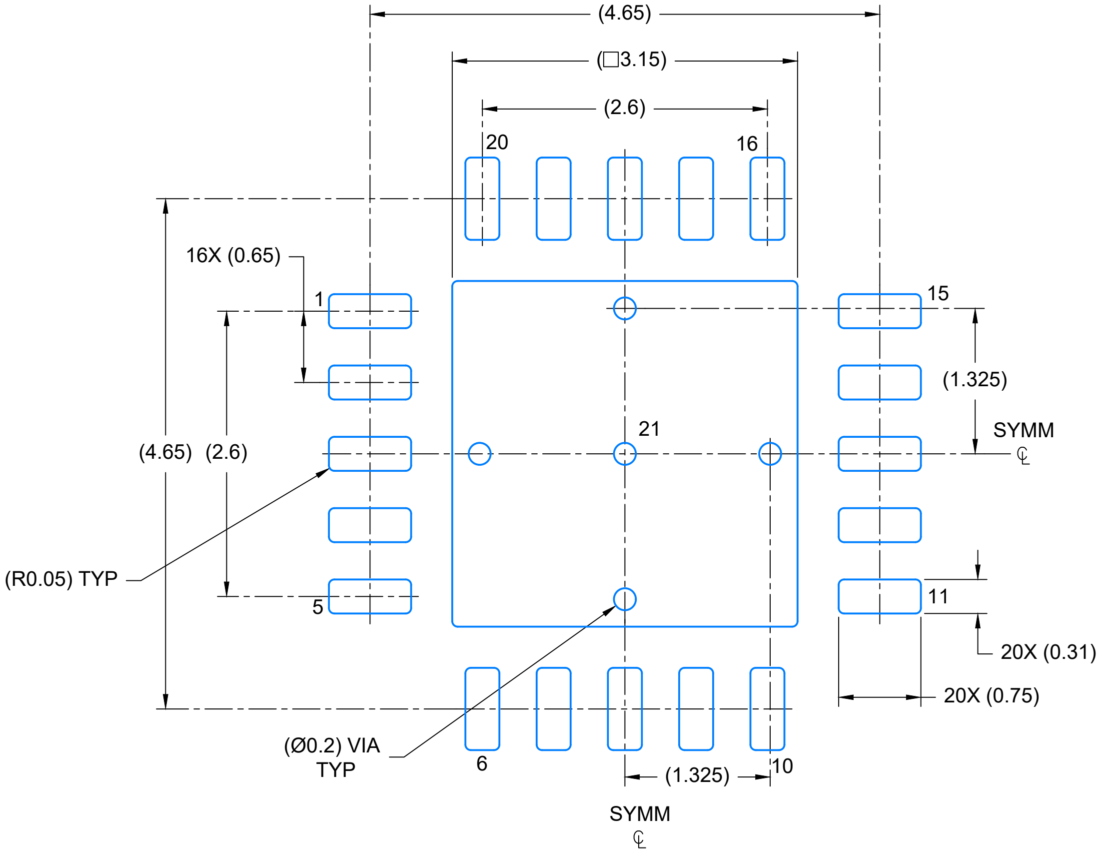
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



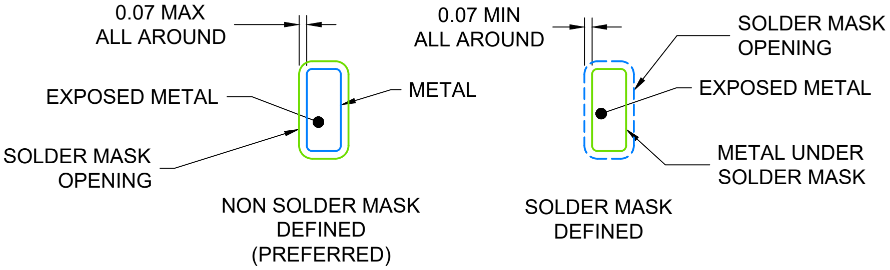


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 15X

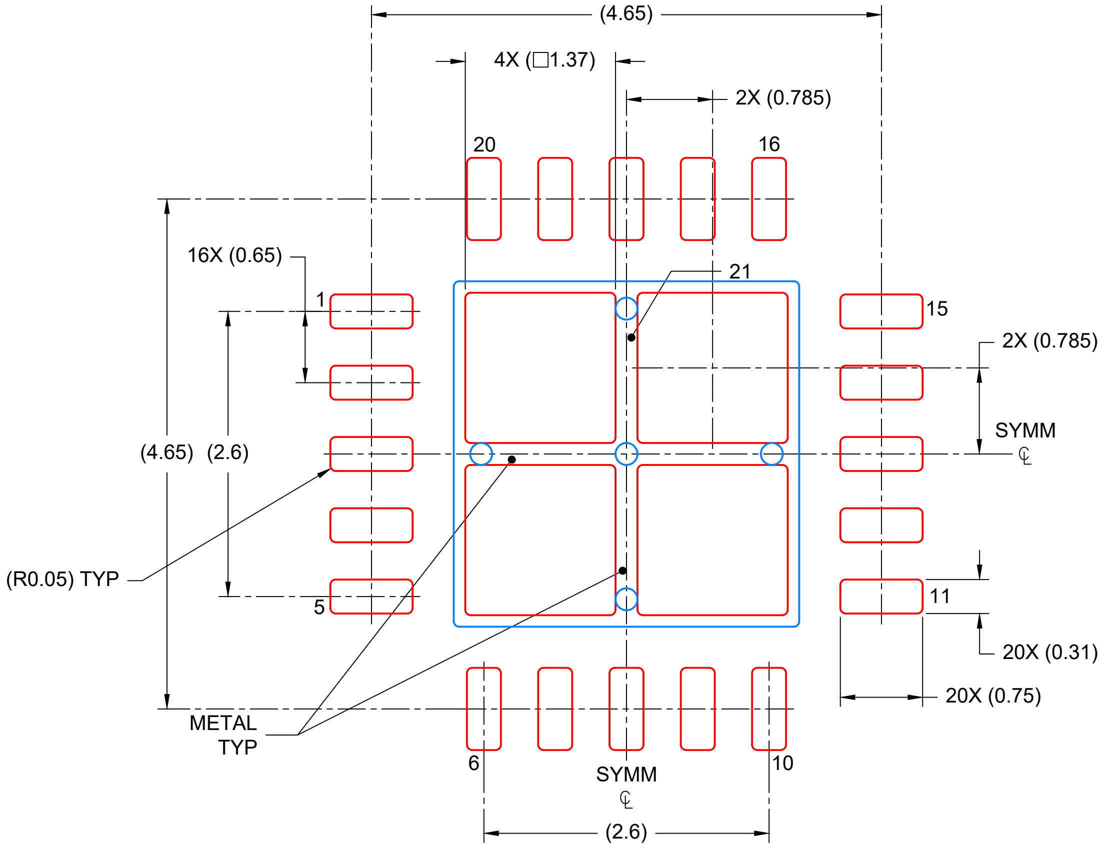


SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated