An Engineer's Guide to Isolated Signal Chain Solutions

Texas Instruments

Introduction

Designers have many options when addressing the challenges associated with designing an accurate isolated current and voltage measurement circuit. Approaches range from using from discrete implementations, through isolated amplifiers and modulators, to magnetic sensing technologies. Technology of choose varies based on the system, regulations, and flexibility a designer has for their of current sensing or voltage sensing applications – the different types of technologies allows the designer to specifically address their unique design challenges.

This e-book was created to further simplify the current and voltage sensing design process by helping you quickly and efficiently narrow down the list of potential devices that align best with your particular system's requirements.

The current and voltage sensing information featured in this e-book address specific current sensing and voltage sensing use-cases, applications, focusing on identifying the most optimized device to best serve the challenges faced in that particular application and offer alternative solutions that may be beneficial for other circuit optimizations.

Although this e-book is not an exhaustive collection of current and voltage-sensing challenges, it does address many of the more common and challenging functional circuits seen today. If you have any questions about the topics covered here or any other current and voltage sensing questions, submit them to the TI E2E™ design support forums Amplifiers forum.

Table of Contents

Introduction to Isolated Signal Chain

- Comparing Isolated Amplifiers and Isolated Modulators
- TI's First Isolated Amplifiers With Ultra-Wide Creepage and Clearance

Comparing Isolated Amplifiers and Isolated Modulators

Abstract

Industrial applications such as motor drives, photo voltaic inverters, and uninterruptible power supplies (UPS) and automotive applications such as onboard chargers (OBCs), traction inverters, and DC/DC converters operate at high voltage and current levels to optimize overall efficiency and power throughput. These systems are subjected to hostile environments such as electrical noise, vibration, mechanical shock, extreme temperatures, ingress of contaminants, and so forth. Such systems demand robust, reliable, galvanic isolation to isolate high voltages from low-voltage circuits. The feedback signals measured on these high voltages are galvanically isolated from the low-voltage controllers by isolated amplifiers or isolated modulators.

This document compares isolated amplifiers and isolated-modulator-based designs and explains some unique advantages of isolated-modulator-based designs.

Introduction to Isolated Amplifiers

Figure 1 shows the implementation of an isolated-amplifier-based measurement design.

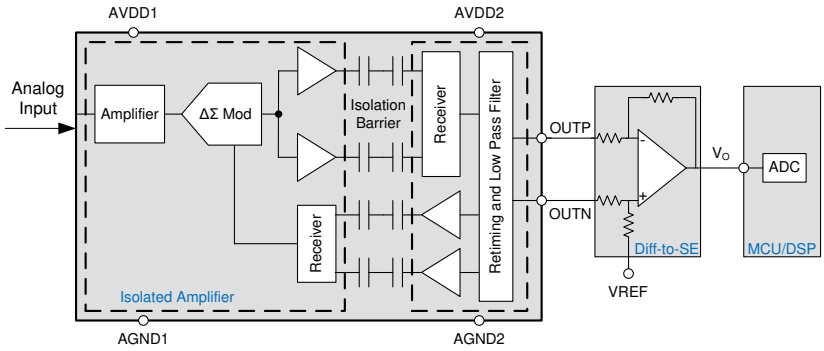


Figure 1. *Isolated Amplifier Implementation*

The input stage of an isolated amplifier consists of an input amplifier that drives a delta-sigma (ΔΣ) modulator. The gain of the input amplifier is fixed and set by internal precision resistors. The ΔΣ modulator uses the internal reference voltage and clock generator to convert the analog input signal to a digital bit stream. The drivers transfer the output of the modulator across an isolation barrier that separates the high and low voltage domains. The received bitstream and clock are synchronized and processed by an analog low-pass filter on the low voltage side and presented as an analog output signal.

The differential output of the isolated amplifier is often converted to a single-ended analog output with an op-amp-based circuit. This op-amp-based circuit can also implement a low-pass filter to further reduce the signal bandwidth to a bandwidth of interest and thereby improve the system noise performance.

The analog-to-digital converter (ADC), either external or internal to the microcontroller (MCU) or digital signal processor (DSP), receives this feedback analog output and converts this output back to the digital domain.

Introduction to Isolated Modulators

Figure 2 shows the implementation of an isolated-modulator-based measurement design.

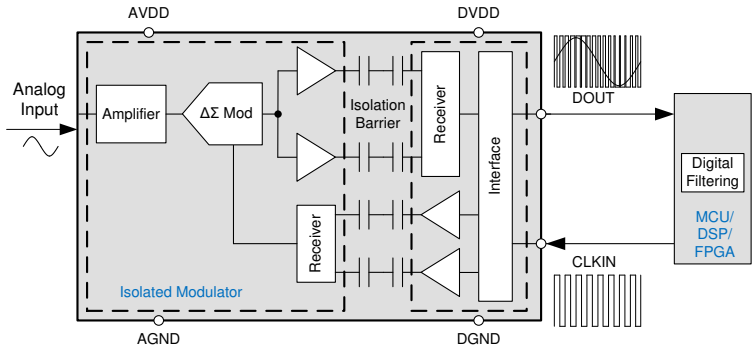


Figure 2. *Isolated Modulator Implementation*

The input stage of an isolated modulator is similar to that of an isolated amplifier. The drivers transfer the modulator output across the isolation barrier. The isolated data output DOUT provides a digital bit stream of 1's and 0's at a much higher frequency (up to 20 MHz). The time average of this bit stream output is proportional to the analog input voltage. The measured signal is reconstructed with a digital filter inside the microcontroller families such as the **TMS320F2807x** and **TMS320F2837x**, a DSP, or a field programmable gate array (FPGA).

Performance Comparison Between Isolated Amplifiers and Isolated Modulators

Table 1 shows the basic difference in performance between isolated amplifiers and isolated modulators.

Table 1. Performance Comparison Between Isolated Amplifiers and Isolated Modulators

CATEGORY	ISOLATED AMPLIFIER	ISOLATED MODULATOR
Sample resolution	11 bits (bandwidth = 100kHz)	> 14 bits achievable, trade-off between resolution and bandwidth or latency
Latency	2µs to 3µs (fixed)	< 1µs achievable, trade-off between resolution and bandwidth or latency
Bandwidth	up to 300kHz	> 1MHz achievable, trade-off between resolution and bandwidth or latency
Accuracy and drift performance	High	Very high
No. of components needed	More	Less

In an *isolated-amplifier-based design*, the measured analog signal undergoes several analog-to-digital and digital-to-analog conversions. The stages within the isolated amplifier, the differential-to-single-ended stage, and the ADC either external or internal to the MCU or DSP reduce overall accuracy and noise performance and increase latency. The fixed low-pass filter implementation in the output stage of the isolated amplifier limits the signal bandwidth. An external op-amp-based circuit used for differential-to-single-ended conversions can be used to create an active low-pass filter to further limit the signal bandwidth and thereby improve noise performance. The isolated amplifier has a fixed latency. Isolated-amplifier-based designs are widely used because of familiarity and relative ease of implementation.

As shown in **Figure 2**, the measured analog signal in an *isolated-modulator-based design* undergoes only one analog-to-digital conversion. This design eliminates the need for a differential-to-single-ended stage, thereby reducing the number of components and design size. The ADC used in an isolated-amplifier-based design, which in many situations limits the maximum achievable sample resolution and accuracy, is not needed anymore. This isolated-modulator-based approach has improved signal noise performance, overall accuracy, and can achieve higher signal bandwidth and lower latency than an isolated-amplifier-based design. Isolated modulators provide a much faster digital bitstream output, typically up

to 20 MHz. The sigma-delta filter module (SDFM) module inside the microcontroller families (such as the **TMS320F2807x** and **TMS320F2837x**) provides an easy way to tune the noise performance and signal bandwidth or latency. As shown in **Table 2**, a higher oversampling ratio (OSR) implementation leads to better accuracy and higher sample resolution but less signal bandwidth and higher latency. Similarly, lowering OSR reduces accuracy and sample resolution but increases bandwidth and reduces latency. A similar DSP or an FPGA can also implement such a digital filter.

*Table 2. Performance Trade-Off Between ENOB and Settling, Latency or Bandwidth for the **AMC1306** at CLKIN = 20 MHz Using a Sinc^3 Filter*

OSR	ENOB (Bits)	SETTLING (µs)	LATENCY (µs)	BANDWIDTH (kHz)
8	4.65	1.2	0.6	1250
16	7.57	2.4	1.2	625
32	10.02	4.8	2.4	312.5
64	12.3	9.6	4.8	156.25
128	13.51	19.2	9.6	78.13
256	14.11	38.4	19.2	39.06
512	14.39	76.8	38.4	19.53

Additionally, as shown in **Figure 3**, multiple digital filters can be implemented in parallel to achieve higher sample resolution, lower latency, and higher bandwidth, all at the same time. One of the digital filters can implement a high OSR digital filter for better noise performance and another one can implement a low-latency digital filter.

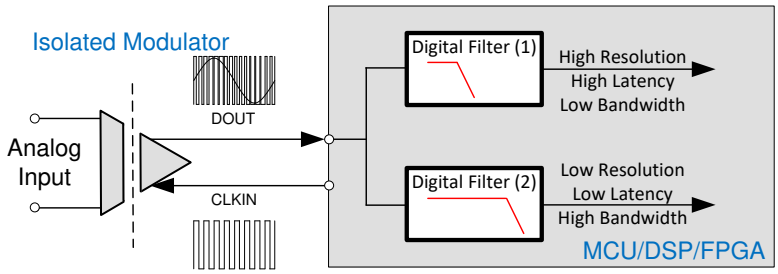


Figure 3. *Implementation of Two Digital Filter in Parallel*

With the system advantages offered by an isolated-modulator-based design, there is a resulting trend to move to an isolated-modulator-based design in high-performance systems.

Isolated Modulators in Traction Inverters

Figure 4 shows an implementation of an isolated-modulator-based design in automotive traction inverters.

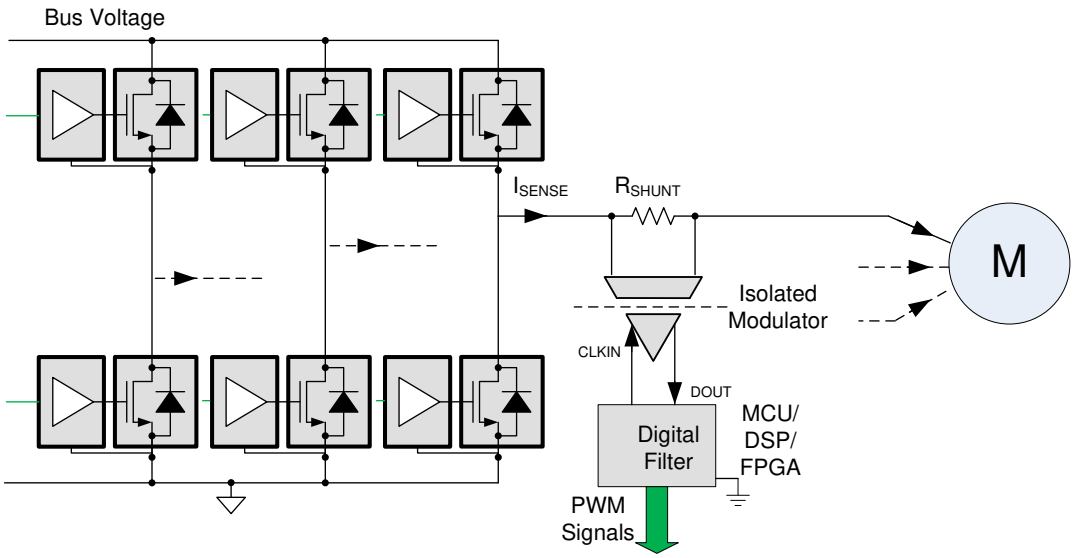


Figure 4. *Current Measurement Using an Isolated Modulator*

Traction inverters have a direct influence on the driving experience and require precise control of speed and torque of the traction motor. A shunt coupled with an isolated delta-sigma modulator provides the highest-quality feedback signals to the controller to establish the pulse-width modulation (PWM) pattern for bridge transistors. The digital filter implementation allows the engineer to tune the quality of traction motor controls.

As shown in **Figure 3**, the FPGA, MCU, and DSP can have multiple digital filters running in parallel. One of the digital filters can be a high-performance digital filter that provides accurate feedback signals to control the bridge transistors. Another digital filter can be a low-latency digital filter for detecting overload or overcurrent conditions. A third-order ($sinc^3$) filter with a different OSR can be used for both digital filters.

Isolated Amplifier and Modulator Recommendations

Table 3 lists the recommended devices for use with the isolated amplifier and modulator.

Table 3. Recommended Devices

DEVICE	ISOLATION	DESCRIPTION
AMC1306	Reinforced	±50-mV, ±250-mV small isolated modulators
AMC1305, AMC1305-Q1	Reinforced	±50-mV, ±250-mV isolated modulators
AMC1301, AMC1301-Q1	Reinforced	±250-mV isolated amplifiers
AMC1302, AMC1302-Q1	Reinforced	±50-mV isolated amplifiers
AMC1311, AMC1311-Q1	Reinforced	0-V to 2-V isolated amplifiers

Conclusion

Isolated modulators offer higher sample resolution and accuracy compared to isolated amplifiers. With the combination of isolated modulators and custom digital filters, the engineer can trade system latency and bandwidth with sample resolution. Isolated-modulator-based designs require fewer components and enable a smaller design size at a reasonable cost. Isolated modulators are strongly recommended in isolated measurement applications wherein high sample resolution or low latency is required.

TI's First Isolated Amplifiers With Ultra-Wide Creepage and Clearance

Application Brief

Several industrial systems such as motor drives, solar and wind power inverters, and automotive systems such as traction inverters require accurate voltage and current measurements at high common-mode voltages. The operating working voltages in these systems are going increasingly higher to increase output power, overall efficiency and reduce cost. Higher DC bus voltages enable higher power ratings without increasing current levels, which keeps copper costs the same. This helps reduce the per-unit cost of energy generated. Another bonus of higher voltage is increased efficiency because the total power output can increase with higher voltage, but when current does not change, the conduction losses also remain the same.

In photovoltaic systems (PV), there is a trend in upgrading designs from 1000 V DC voltages to 1500 V DC voltages to reap the benefits elaborated by increased operating voltages. There are regulatory safety standards such as IEC 62109-2 in photovoltaic systems to address potential electrical hazards associated with the increased voltage.

In motor drive (MD) systems, IEC61800-5-1 is used to address the potential electrical hazards. Higher voltage grids such as 690 V_{AC} are more cost effective to install and operate for high-power applications, therefore, they are commonly found in high-power industrial environments.

In welding equipments for industrial and professional use, IEC 60974-1 specifies the safety and performance requirements of the supply and welding circuit to protect against electric shock.

In electric vehicles (EVs), there is a strong trend to increase electric vehicle battery voltage to lower system weight, reduce charging time and increase range.

Need for High-Creepage and High-Clearance Products

While designing these systems, the engineers need to consider the relevant regulatory safety standards and several requirements such as working and transient voltages, pollution degree, and altitudes to define the minimum creepage and clearance requirements.

Most reinforced isolated amplifiers come in a SOIC package with less than 9 mm of clearance and creepage specification. Improved and wider packages prevent degradation along the package surface and arcing through the air between pins, which ensures isolation quality. Systems with working voltages greater than 1000 V_{RMS}, impulse voltage requirements greater than 8000 V, or systems designed for altitudes greater than 2000 m or for a pollution degree 2 or higher, may require clearance and creepage distances greater than 9 mm depending on the overvoltage category of the designed system.

Introducing AMC1411 and AMC1400 in Stretched SOIC (DWL) Package

To address the requirements for higher creepage and clearances, Texas Instrument's released a family of high-performance reinforced isolated amplifiers, **AMC1411** (**Figure 5**) and **AMC1400** (**Figure 6**).

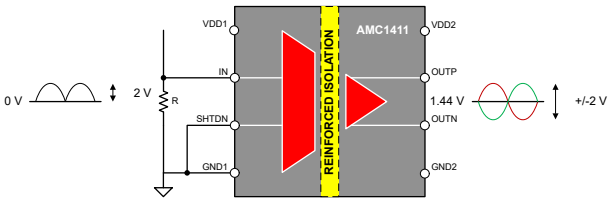


Figure 5. *Isolated Voltage Sensing With AMC1411*

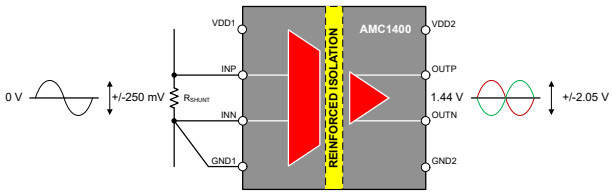


Figure 6. *Isolated Current Sensing With AMC1400*

These products come in a stretched SOIC (DWL) package (**Figure 7**) with clearance of ≥14.7 mm and creepage of ≥15.7 mm and are specifically designed for use in high-voltage, high-altitude and high-pollution degree environments.

Figure 7. *DWL Package, 8-Pin SOIC*

AMC1411 and AMC1400 offer 10600-VPK reinforced isolation per DIN VDE V 0884-11 (VIOTM) and 7500-VRMS isolation for 1 minute per UL1577 (VISO). The high isolation voltage rating and high common-mode transient immunity (CMTI) of 100 kV/µs ensure reliable and accurate operation even in harsh industrial and automotive environments.

The 0-2 V input voltage range, high input impedance, low input bias current, excellent accuracy, and low temperature drift make the AMC1411 a high-performance solution for isolated voltage sensing.

The ±250 mV input voltage range, very low nonlinearity, and temperature drift make the AMC1400 a high-performance solution for isolated shunt-based current sensing.

AMC1411 and AMC1400 in Motor Drives

Figure 8 shows a 3-phase motor-drive application that uses the AMC1411 to monitor DC-link voltage and AMC1400 to monitor the in-phase motor current per phase.

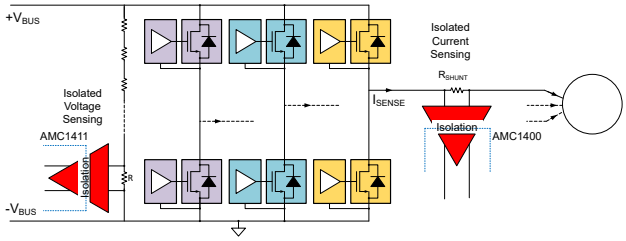


Figure 8. *AMC1411 and AMC1400 in Motor Drives*

AMC1411 is used to measure the DC-link voltage divided down to an approximate 2 V level across the bottom resistor of a high-impedance resistive divider. The output of the AMC1411 is a differential analog output voltage of the same value as the input voltage but is galvanically isolated from the high-side by a reinforced isolation barrier.

AMC1400 is used to measure the in-phase motor current by sensing the voltage drop across the in-phase shunt to the motor.

Additional Resources

- Learn more about isolated amplifiers and modulators in our video **training series**.
- Read these white papers:
  - **"High-Voltage Isolation Quality and Reliability for AMC130x."**
  - **"Comparing Isolated Amplifiers and Isolated Modulators."**
  - **"Comparing Shunt- and Hall-Based Current-Sensing Solutions in Onboard Chargers and DC/DC Converters."**
- Read the application brief, **Accuracy Comparison of Isolated Shunt and Closed-Loop Current Sensing.**

Selection Trees

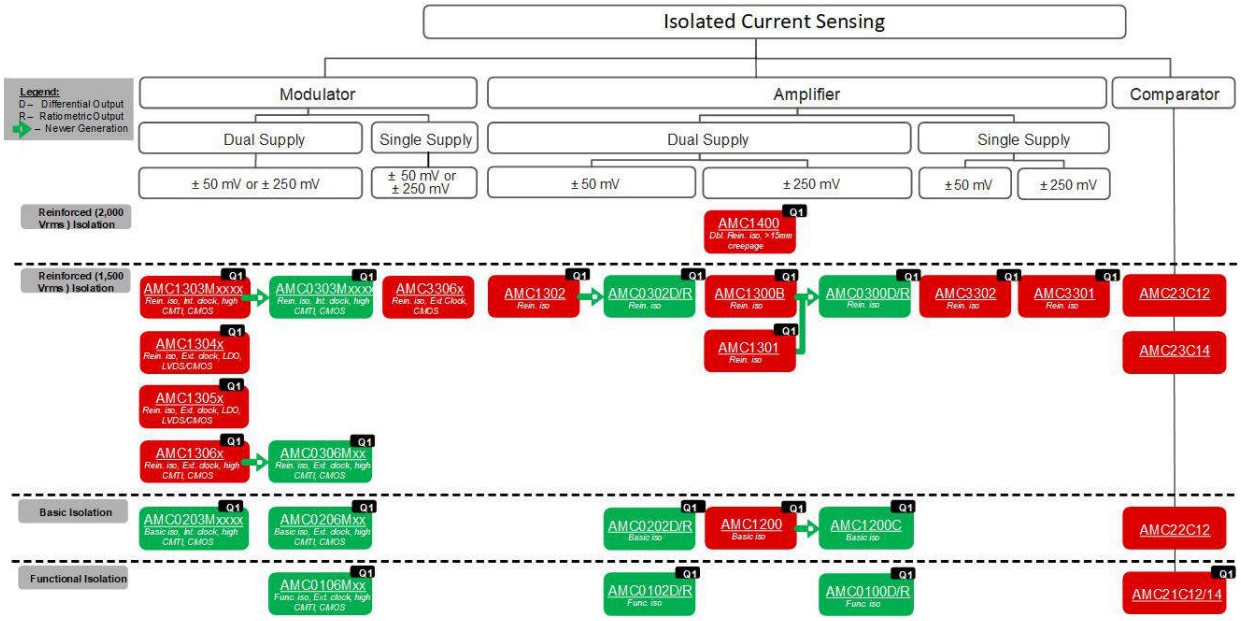


Figure 9. *Isolated Current Sensing: Selection Tree*

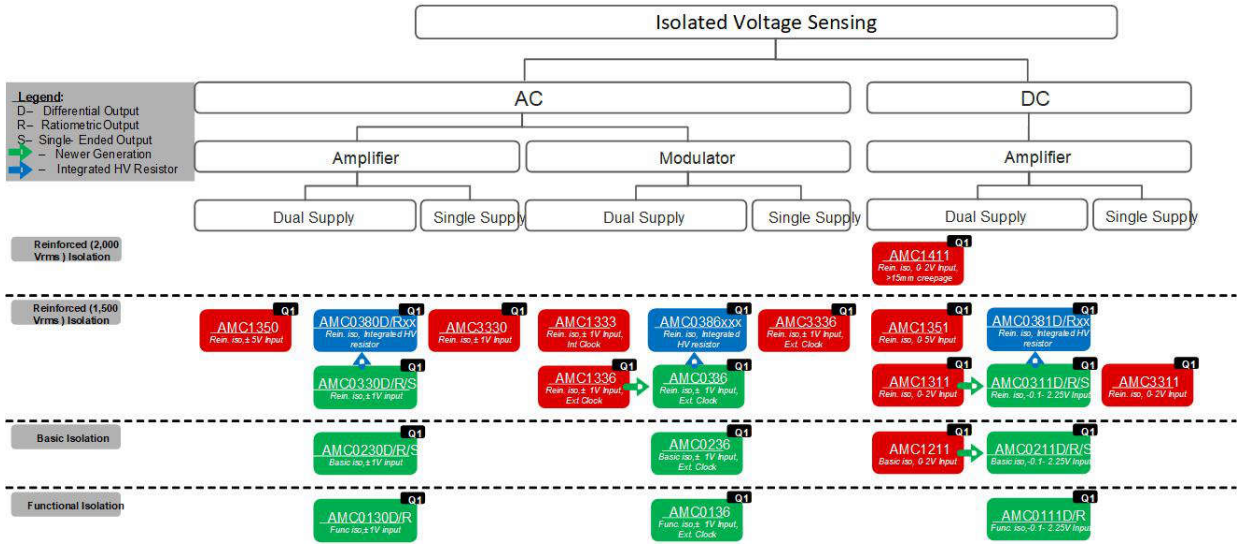


Figure 10. *Isolated Voltage Sensing: Selection Tree*

Current Sensing

- Shunt Resistor Selection for Isolated Data Converters
- Design considerations for isolated current sensing
- Isolated Current-Sensing Circuit With ±50-mV Input and Single-Ended Output
- Isolated Current-Sensing Circuit With ±50-mV Input and Differential Output
- Isolated Current-Sensing Circuit With ±250-mV Input Range and Single-Ended Output Voltage
- Isolated current-measurement circuit with ±250-mV input and differential output
- Isolated Overcurrent Protection Circuit
- Interfacing a Differential-Output (Isolated) Amp to a Single-Ended Input ADC
- Utilizing AMC3311 to Power AMC23C11 for Isolated Sensing and Fault Detection
- Isolated Current-Sensing Circuit With Front-End Gain Stage
- Accuracy Comparison of Isolated Shunt and Closed-Loop Current Sensing

Shunt Resistor Selection for Isolated Data Converters

Introduction

A low-ohmic, precise, in-line resistor is known as a shunt resistor. In high-voltage automotive and industrial applications such as **Hybrid, electric and powertrain systems**, **EV charging infrastructure**, **Motor drives**, and shunt resistors are often paired with an isolated data converter to measure a current whose magnitude drives the feedback algorithm of a control loop while protecting the digital circuitry from the high-voltage circuit performing a function. Texas Instruments has an extensive portfolio of **isolated amplifiers**, **isolated ADCs**, and **isolated comparators** featuring a capacitive isolation barrier to help customers address isolated data conversion needs. Texas Instruments' capacitive isolation barrier often allows for over 100 years of operation. For more information on TI's capacitive isolation barrier, see the **Isolation** link.

As the **Accuracy Comparison of Isolated Shunt and Closed-Loop Current Sensing Application Brief** shows, shunt-based current sensing allows for industry-leading accuracy, immunity to magnetic interference, long-term stability, high linearity, low offset drift, scalability to multiple projects, and a reduced price. Shunts can be chassis mounted, surface mounted, or leaded for through-hole connections to the printed circuit board (PCB). Many shunt resistors are available to choose from and selecting the correct shunt resistor for a given application is not always straightforward. This application brief discusses shunt resistors that are often used for isolated current sensing and the associated tradeoffs.

Calculating Resistance and Power Dissipation Requirements

To select a shunt resistor, the first step is to calculate the required resistance and power-dissipation rating based on the continuous and maximum current magnitudes and the linear full-scale input voltage range of the isolated data converter as discussed in the **Design considerations for isolated current sensing** article. However, care must be taken to maintain that the shunt resistors maximum temperature does not exceed the rating listed in the data sheet due to self-heating. Under normal conditions, shunt resistors cannot operate continuously beyond two-thirds of the rated current, assuming that the design allows for adequate heat dissipation. Heat dissipation techniques vary by application and can be accomplished in multiple ways: an increased weight or size of the current carrying PCB trace or primary conductor, heat sinks, or fans for forced air cooling. If the application does not allow for adequate heat dissipation, then the shunt resistor is not necessarily able to operate beyond as low as one-fourth rated current. Beyond this current, further decreasing the resistance or increasing the power dissipation rating of the selected shunt resistor can be necessary.

For surface mount resistors, roughly 90% of the self-generated heat is dissipated by conduction to the PCB trace. **Figure 11** demonstrates that increasing the size of the current carrying PCB trace is an effective heat dissipation technique. The simulated thermal performance of surface mounted, metal element, 1mΩ, 2512 (5W) and 3920 (8W) package shunt resistors are shown with natural and forced air cooling. The results are presented as Shunt Rated Current (%) vs PCB Size (mm^2); where the maximum temperature of the selected shunt resistor (170°C) was reached.

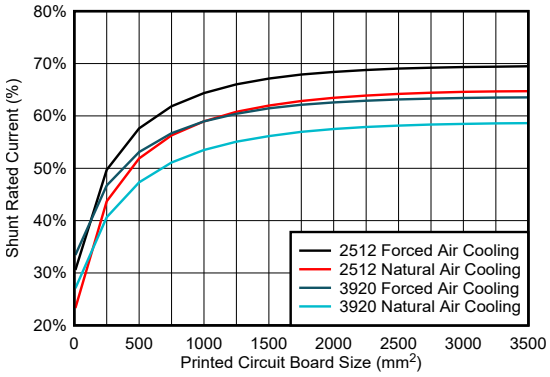


Figure 11. *Shunt Rated Current vs PCB Size*

To verify the performance of the shunt resistor in an application, measure the terminal temperature of the shunt resistor during maximum nominal operation and consult the power derating curve in the data sheet of the shunt resistor to verify that operation is within the specified range. This practice not only maintains that the resistive material does not exceed the specified maximum temperature, but also that the specified temperature drift coefficient is valid.

When calculating expected output voltage and power dissipation, consider transient and short-circuit current magnitudes. The short-term overload power dissipation specification of the shunt resistor, as specified in the data sheet, must not be violated because there is risk of permanently altering the physical properties of the shunt resistor or creating an open circuit. Additionally, verify that the isolated data converter absolute maximum input voltage specification is not violated for either condition as shown in the Absolute Maximum Ratings table of the data sheet. The input pins of isolated data converters from Texas Instruments are typically rated to withstand voltages between –6V and up to the high-side supply voltage +500mV with respect to the high-side ground without risk of being damaged.

Mounting, Construction, and Material Types

Once an approximate resistance and power dissipation requirement is calculated, additional selection criteria must be considered as summarized in **Table 4**.

Table 4. Shunt Selection Summary

Technology	Metal Element	Metal Foil	Metal Element	Wire-Wound
Installation Method	Surface Mount	Surface Mount	Chassis Mount	Chassis Mount or Leaded
Resistance Range (Ω)	0.1m – 1	0.5m – 0.7	25µ – 0.1	R > 5m
Wattage Range (W)	1/16 – 20	1/80 – 10	¼ – 100	½ – 1k
Tolerance Range (%)	0.1 – 5	0.01 – 10	0.1 – 1	0.1 – 10
Drift Range (ppm/C°)	15 – 750	0.2 – 1k	20 – 100	20 – 400
Pulse Capability (C°)	Up to 275	Up to 225	Up to 175	275+
Cost	+	++	+++	+++/+

Surface mount, metal element shunt resistors are the most popular choice for isolated current sensing because these offer low resistances, high wattage capability, fair initial accuracy, and low cost. Shunt resistor series such as CSS2H from Bourns® and WSLP from Vishay® are well equipped for isolated current sensing. Applications requiring a higher initial accuracy, or lower drift over temperature than what metal element can provide, can consider metal foil such as FC4L from Ohmite®; however, power dissipation ratings are typically lower and the cost is higher compared to the metal element. Layout considerations for surface mount resistors include placement close to the isolated data converter with short and evenly matched sensing connections to the inputs as explained in this **Current Sense Amplifiers Shunt**

Resistor Layout video from TI precision labs. Additionally, take care when designing the PCB pads for surface mount resistors with low resistance (< 500µΩ) as discussed in this **TI E2E™ blog**. Lastly, verify establishment of the correct soldering reflow process when working with the PCB manufacturer because incorrect installation can lead to a high initial error due to solder contact resistance on the pads, imbalanced heat dissipation during operation, or an open circuit.

Chassis mounted resistors are often used in applications that require high currents since these resistors allow for in-line conductor installation and do not dissipate the self-generated heat to the PCB. Metal element chassis mounted resistors allow for resistances as low as 25µΩ and wattage up to 100W, whereas chassis mounted wire-wound resistors have exceptional pulse-power capability. When installing, take special care to not over- or under-torque bolts, rivets, or crimp joints of the primary connections because additional resistance can be added to the primary conductor line resulting in unnecessary or imbalanced power dissipation and analog errors. Consult the chassis mount resistor manufacturer for additional guidance.

For applications that require the highest accuracy, consider four terminal shunt resistors with differential sensing connections independent of the primary current carrying leads (Kelvin connections). Kelvin connections offer higher accuracy compared to two terminal shunts due to reduced temperature drift in the sensing element leads; however, cost is typically higher and there is additional risk because improper installation allows for the primary current to flow through the sensing connections, potentially damaging the isolated data converter. Temperature measurements local to the shunt resistor can also be made to periodically update a calibration table because most shunt resistors offer a relatively predictable change in resistance over temperature allowing for exceptional accuracy in spite of changes in ambient temperature or self-heating due to power dissipation.

Conclusion

Pairing the correct shunt resistor with an **isolated amplifier**, **isolated ADC**, or **isolated comparator** from TI, can achieve a measurement that features industry leading accuracy, immunity to magnetic interference, long-term stability, high linearity, low drift, scalability to multiple projects, and low price.

Design considerations for isolated current sensing

Industrial and automotive applications such as on-board chargers, string inverters and motor drives require some type of isolated current measurement to drive the feed- back algorithm for the current control loop while protecting the digital circuitry from the high-voltage circuit performing a function.

Given their high performance, isolated amplifiers are excellent devices for transferring current-measurement data across the isolation barrier. However, selecting the correct isolated amplifier is not always a straightforward process. There are many decisions to consider when selecting an isolated amplifier, such as isolation specifications, how to power the high side and selection of the input voltage range. This article covers each of these decisions in detail to help select an isolated amplifier best suited to a specific system.

The first decision when selecting a device for isolated current measurement is to determine the level of isolation required. There are two levels of isolation, basic and rein- forced. System architecture and end-equipment standards such as International Electrotechnical Commission (IEC) 61800 for motor drives and IEC 60601 for medical equipment will specify the required isolation level.

Here are the main specifications that quantify the performance of the isolation barrier:

- The isolation working voltage is the maximum voltage defined in the root-mean-square voltage that the isolated amplifier can handle continuously throughout its operating life.
- Common-mode transient immunity describes the maxi- mum rate of change in ground potential difference that the isolated amplifier can withstand without errors.
- The isolation transient overvoltage is the voltage defined in the peak-to-peak voltage that the isolated amplifier can tolerate for 60 s.
- The surge rating (impulse voltage rating) according to IEC 60065 is the 1.2-/50-µs voltage magnitude that the isolated amplifier can tolerate without failure.

Some end-equipment manufacturers have their products certified by third parties to verify that they meet isolation specifications. Isolated amplifiers are not measured to these specifications themselves, since they are components inside end equipment, and end-equipment standards apply only indirectly to them. Instead, components are measured against device-level certifications such as Deutsches Institut für Normung e.V. (DIN) Verband Deutscher Elektrotechniker (VDE) V 0884-11 and Underwriters Laboratories (UL) 1577. As stated in the IEC standards, devices complying with component-level standards that have equivalent requirements do not require separate evaluation. This applies to Comité International Spécial des Perturbations Radio (CISPR) radiated emissions electromagnetic interference (EMI) standards as well. See [1] for radiated emissions performance for isolated amplifiers from Texas Instruments (TI).

For the best performance, the layout and application practices shown in the device-specific data sheet are recommended; [2] lists the TI isolated amplifier device-level certifications.

The next decision when selecting an isolated amplifier is how to power it on the high side of the isolation barrier.

When designing this portion of the circuit, remember that the high-side supply voltage must float with the common-mode input voltage of the current being measured. This means that for multiple-phase current measurements, each phase requires one isolated amplifier with its own high-side power supply. Incorrectly designing the high- side power-

supply circuit can lead to exceeding the absolute maximum analog input-voltage ratings, which can cause permanent damage to the device.

There are three main design options to power the high side of an isolated amplifier.

The first design option is to design a discrete isolated transformer circuit that can supply voltage to the high side of the isolated amplifier from the low side. This method will require selecting an isolated transformer, a trans- former driver such as TI's SN6501 and a low-dropout regulator such as TI's TLV704. Although easy to design, this approach requires a large board area and several components. **Figure 12** illustrates an example implementation on the top portion of the AMC1300 evaluation module (EVM).

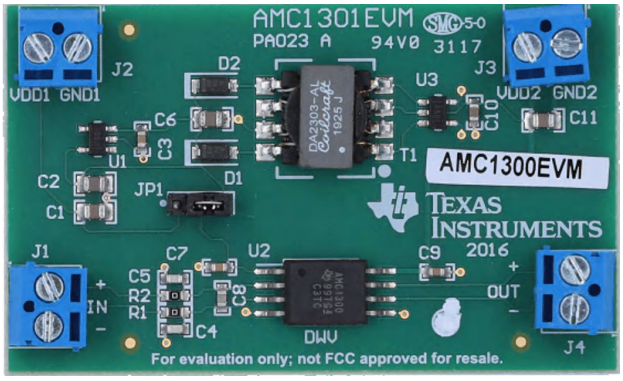


Figure 12. *The AMC1300 EVM with an isolate transformer.*

The second design option, shown in **Figure 13**, uses the floating high-side gate driver supply (typically 15 V) and a shunt regulator such as a Zener diode to regulate the voltage down to 5 V. Examples of this design are in the device data sheets, such as the AMC1300B-Q1 reinforced isolated amplifier. While this design option is economical and effective, layout restrictions and parasitic impedances between the gate-driver-supply ground reference and the amplifier ground reference can lead to common-mode input voltage violations and transient errors.

The third and simplest design option, shown in **Figure 14**, uses a device with an integrated DC/DC converter. Isolated amplifiers with integrated DC/DC converters such as TI's AMC3302 greatly reduce solution size and complexity, lower system costs, provide excellent conversion efficiency, and enable flexible placement of the shunt resistor.[4]

The last decision when selecting an isolation amplifier is toselect the input voltage range of the device. Most isolated amplifiers optimized for current sensing have options for either a ±50-mV or ±250-mV linear-input voltage range. Determining which input voltage range is right for the application will depend on the magnitude of current being measured and the size of the shunt resistor. In general, systems with high current magnitudes typically require an isolated amplifier with a smaller input range, such as ±50 mV. Systems with relatively low current magnitudes may benefit from the slightly larger input voltage range of ±250 mV, which allows for higher signal- to-noise ratios

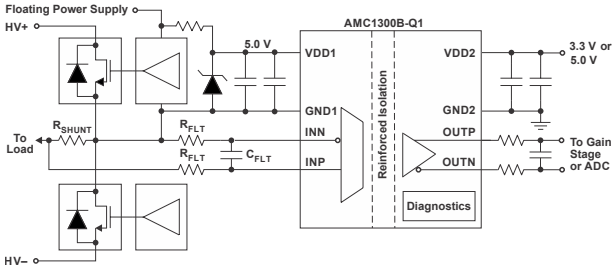


Figure 13. *The AMC1300B-Q1 and a floating power supply.*

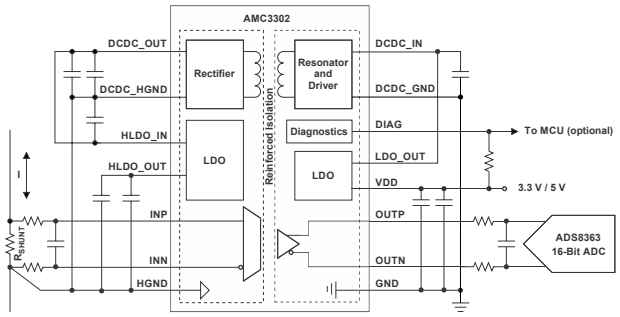


Figure 14. *The AMC3302 isolated amplifier with an internal DC/DC converter.*

There are two equations to consider when selecting the input voltage range: Ohm's law (see **Equation 1**), and the power dissipated in a resistor (see **Equation 2**):

$$V = I \times R \tag{1}$$

$$P = I^2 \times R \tag{2}$$

These two equations govern the trade-off between maximizing the full-scale input range of the isolated amplifier and the amount of power dissipated in the shunt resistor. When supplied with current and resistance values, **Equation 1** calculates the voltage drop across the shunt resistor. Try to match this voltage range as closely as possible to the full-scale input voltage range of the isolated amplifier, as an mismatch between the two values will result in a direct loss of resolution.

Equation 2 quantifies the power dissipated in the shunt resistor. This is important, since shunt resistors will begin to drift (according to their temperature drift specification) from self-heating once the power dissipated through the resistor reaches one-half the rated power dissipation, resulting in a gain error. In order to avoid excessive shunt drift caused by self-heating, it is often best to limit the shunt resistor's nominal power dissipation to be equal to or less than one-eighth the rated power dissipation.

For example, if the current requirement is for a nominal current of 18 A and a maximum current of 52 A. Knowing that there are two options for the linear-input voltage range (±50 mV and ±250 mV), as well as the maximum current, it is possible to calculate ideal shunt resistance values to meet the full-scale input range for both choices:

$$\pm 50\ \text{mV: } R_{Ideal} = 0.96\ \text{m}\Omega$$
$$\pm 250\ \text{mV: } R_{Ideal} = 4.8\ \text{m}\Omega \tag{3}$$

Finding the closest standard shunt resistor values:

For ±50 mV: R = 1 mΩ, or
for ±250 mV: R = 5 mΩ (4)

Plugging these values into **Equation 1** enables the resulting full-scale voltage drop across the shunt resistor to be calculated:

For ±50 mV: V = I × R = (52 A) × (1 mΩ) = 52 mV, or
for ±250 mV: V = I × R = (52 A) × (5 mΩ) = 260 mV (5)

Notice that the resistance value from the ideal calculation to the closest standard value increased slightly, which results in a full-scale input voltage range that is larger than the linear full-scale input range of the isolated amplifier. This means that for full-scale current magnitudes, the resulting voltage magnitude will no longer be within the linear region of the isolated amplifier's input. Isolated amplifiers often have an additional input voltage range beyond the linear input voltage range before they begin to clip. Within this region—typically as high as ±280 mV for ±250-mV devices and ±56 mV for ±50-mV devices—the accuracy of the isolated amplifier is not specified in the data sheet; however, the isolated amplifier will continue to output a voltage with accuracy similar to the linear region. This may be acceptable for some applications if the accuracy requirement of the maximum current magnitude is relaxed compared to the nominal measurements.

Next, use the standard resistance values and nominal current magnitudes to calculate the power dissipated in the shunt resistor, assuming that the power dissipation rating in the shunt resistor is 3 W.

$$\text{For } \pm 50\,\text{mV: } P = I_{max}^2 \times R = (18\,\text{A})^2 \times \left(1\,\text{m}\Omega\right) = 0.32\,\text{W},$$
$$\text{For } \pm 250\,\text{mV: } P = I_{nom}^2 \times R = (18\,\text{A})^2 \times \left(5\,\text{m}\Omega\right) = 1.62\,\text{W} \quad (6)$$

For the ±50-mV calculation, the nominal power dissipation is less than one-eighth the rated power dissipation. This shunt resistor should not drift significantly from self- heating when measuring the nominal current. The ±250-mV calculation results in power dissipation that is over one-half the rated power dissipation, meaning that there could be significant temperature drift when measuring the nominal current range.

Additional measures can be taken to reduce the heat dissipated in the shunt resistor, such as forming large printed-circuit-board planes, or using heat sinks or fans. For very-high current applications, it is possible to maximize the input range by using an operational amplifier to gain the input signal to match the full-scale input range of the isolated amplifier, a method used in [5].

For most applications that measure high nominal current magnitudes, it's a good idea to choose an isolated amplifier such as TI's AMC1302 or AMC3302 with the smaller ±50-mV input voltage range.

The last step is to verify that power dissipation at the maximum current magnitude does not exceed the rated power dissipation of the shunt resistor, as exceeding the rated power dissipation could damage the shunt resistor permanently.

$$\text{For } \pm 50\,\text{mV: } P = I_{max}^2 \times R = (52\,\text{A})^2 \times \left(1\,\text{m}\Omega\right) = 2.70\,\text{W} \quad (7)$$

To see measured results similar to the example, see [6].

Conclusion

When designing an isolated current-sensing circuit in end equipment such as on-board chargers, string inverters and motor drives, there are many decisions to consider when selecting an isolated amplifier. Key elements for consider- ation

are the isolation specifications, the high-side power source and the input voltage range. With the right isolated amplifier that suits system requirements, a design can be achieved without the worry of passing the end-equipment certification, exceeding the absolute maximum analog input voltage ratings or causing excessive self-heating of the shunt resistor.

References

1. Alex Smith, **"Best in Class Radiated Emissions EMI Performance with the AMC1300B-Q1 Isolated Amplifier"** Application Report, June 2020.
2. **"Isolated amplifiers – Certifications," for products from Texas Instruments**
3. **AMC1300 evaluation module (EVM), Texas Instruments**
4. Ravi Kiran Raghavendra, **"Simplify your isolated current and voltage sensing designs with single-supply isolated amplifiers and ADCs."** TI E2E™ support forums technical article, October 26, 2020.
5. **"Shunt-Based, 200A Peak Current Measurement Reference Design Using Isolation Amplifier,"** Texas Instruments (TIDA-00445), March 2016.
6. Smith, Alex.**"Accuracy Comparison of Isolated Shunt and Closed-Loop Current Sensing,"**, Application Brief, September, 2020.

Related Websites

Reference designs:

- **On-board(OBC) & wireless charger integrated circuits and reference designs**
- **Solar string inverter integrated circuits and reference designs**
- **Motor drives system block diagrams, reference designs and products**

Product information:

- **Isolation solutions from Texas Instruments**
- **AMC1300B-Q1**
- **AMC1302-Q1**
- **AMC3302**
- **SN6501-Q1**
- **TLV704**

Isolated Current-Sensing Circuit With ±50-mV Input and Single-Ended Output

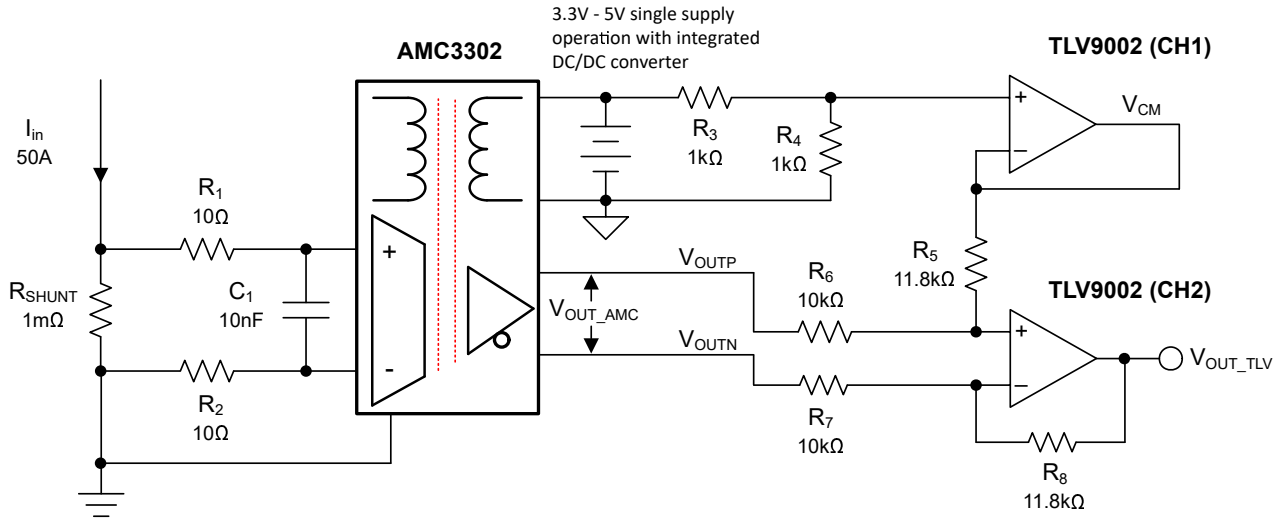
Design Goals

Current Source		Input Voltage		Output Voltage	Single Power Supply
$I_{IN\ MIN}$	$I_{IN\ MAX}$	$V_{IN\ DIFF,\ MIN}$	$V_{IN\ DIFF,\ MAX}$	$V_{OUT\ SE}$	V_{DD}
–50A	50A	–50mV	50mV	55mV to 4.945V	5V

Design Description

This isolated single-supply bidirectional current sensing circuit can accurately measure load currents from –50 A to 50 A. The linear range of the input is from –50 mV to 50 mV with a differential output swing of –2.05 V to 2.05 V and an output common-mode voltage (V_{CM}) of 1.44 V. The gain of the isolated amplifier circuit is fixed at 41 V/V. A secondary amplifier stage, using **TLV9002**, converts the differential output voltage to a single-ended output voltage of 55 mV to 4.945 V. The entire signal chain operates on a single 5.0 V rail.

This circuit is applicable to many high-voltage industrial applications such as **Solar Inverters**, **Motor Drives** and **Protection Relays**. The equations and explanation of component selection in this design can be customized based on the needs and system specification of the end equipment.



Design Notes

1. The AMC3302 was selected due to its accuracy, input voltage range, and the single low-side power requirements of the device.
2. The TLV9002 was selected for its low cost, low offset, small size, and dual channel.
3. Select a low impedance, low-noise source for AVDD which supplies the TLV9002 and AMC3302 as well as provides the common-mode voltage for the single-ended output.
4. For highest accuracy, use a precision shunt resistor with low temperature coefficient.
5. Select the current shunt for expected peak input current levels.
6. For continuous operation, do not run the shunt resistors at more than two-thirds the rated current under normal conditions as per IEEE standards. Further reducing the shunt resistance or increasing the rated wattage may be necessary for applications with stringent power-dissipation requirements.
7. Use the proper resistor divider values to set the common-mode voltage appropriately.
8. Select the proper values for the gain setting resistors on channel 2 of the TLV9002 so that the single-ended output has an appropriate output swing.

Design Steps

1. Determine the transfer equation given the input current range and the fixed gain of the isolation amplifier.

$$V_{OUT} = I_{in} \times R_{shunt} \times 41$$

2. Determine the maximum shunt resistor value.

$$R_{shunt} = \frac{V_{inMax}}{I_{inMax}} = \frac{50\ mV}{50\ A} = 1\ m\Omega$$

3. Determine the minimum shunt resistor power dissipation.

$$Power\ R_{shunt} = {I_{inMax}}^2 \times R_{shunt} = 2500\ A \times 0.001\ \Omega = 2.5\ \text{W}$$

4. To interface with a 5 V ADC, the AMC3302 and TLV9002 can both operate at 5 V so a single-supply can be used.
5. Channel 1 of the TLV9002 is used to set the 2.5 V common-mode voltage of the single-ended output of channel 2. With a 5 V supply, a simple resistor divider can be used to divide 5 V down to 2.5 V. Using 1 kΩ for R_4, R_3 can be calculated using the following equation.

$$R_3 = \frac{V_{DD} \times R_4}{V_{CM}} - R_4 = \frac{5\ V \times 1000\ \Omega}{2.5\ V} - 1000\ \Omega = 1000\ \Omega$$

6. The TLV9002 is a rail-to-rail operational amplifier. However, the output of the TLV9002 can swing a maximum of 55 mV from its supply rails. Because of this, the single-ended output should swing from 55 mV to 4.945 V (4.89 Vpk-pk).
7. The V_{OUTP} and V_{OUTN} outputs of the AMC3302 are 2.05 Vpk-pk, 180 degrees out of phase, and have a common-mode voltage of 1.44 V. Therefore, the differential output is ±2.05 V or 4.1 Vpk-pk. To stay within the output limitations of the TLV9002, the output of the AMC3302 needs to be amplified by a factor of 4.89 / 4.1. When $R_6 = R_7$ and $R_5 = R_8$, the following transfer function can be used to calculate R_5 and R_8.

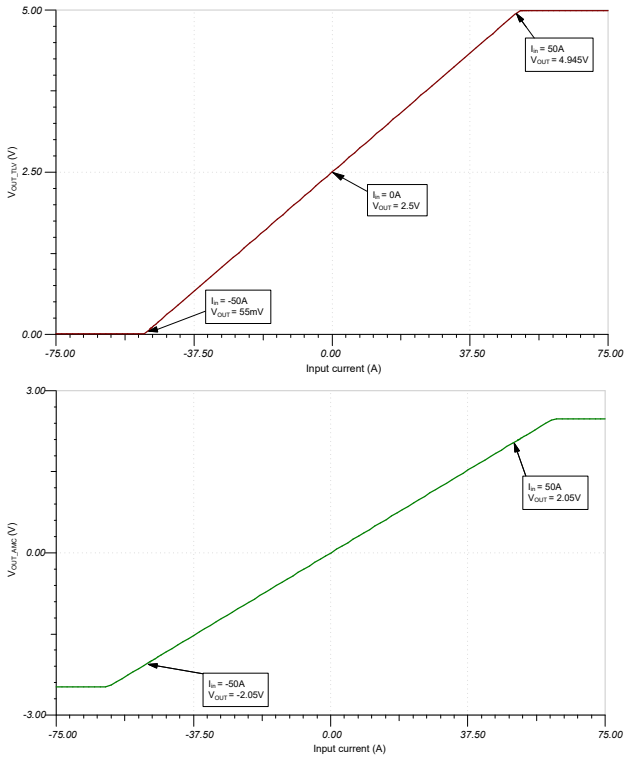
$$V_{OUT} = (V_{OUTP} - V_{OUTN}) \times \left(\frac{R_{5,8}}{R_{6,7}}\right) + V_{CM}$$

8. Using the previously calculated output swing of the TLV9002 and choosing R_6 and R_7 to be 10 kΩ, R_5 and R_8 can be calculated to be 11.93 kΩ using the following equation. To account for standard resistor values, use 11.8 kΩ resistors instead.

$$4.945 = (2.465\ V - 415\ mV) \times \left(\frac{R_{5,8}}{10\ k\Omega}\right) + 2.5$$

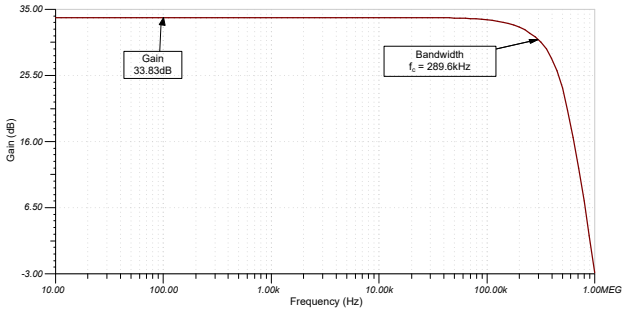
DC Transfer Characteristics

The following plots show the simulated DC characteristics of the single-ended output of the TLV9002 amplifier and the AMC3302 differential output. Both plots show that the outputs are linear at ±50 A.



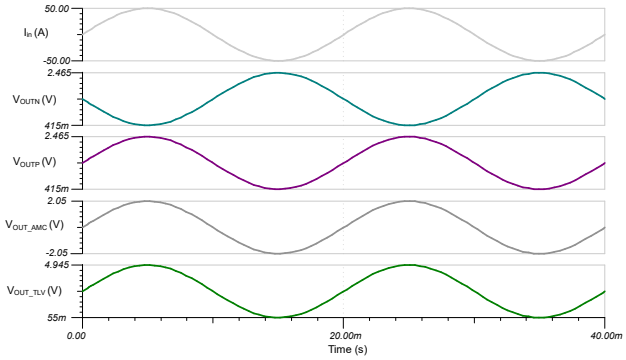
Closed-Loop AC Simulation Results

The following AC sweep shows the AC transfer characteristics of the single-ended output. Since the AMC3302 has a gain of 41 V/V and a gain of 1.2 V/V is applied with the differential to single-ended conversion, the gain of 33.83 dB shown in the following is expected.



Transient Simulation Results

The following transient simulation shows the output signals of both the AMC3302 and TLV9002 from –50 A to 50 A. The differential output of the AMC3302 is ±2.05 Vpk-pk as expected and the single-ended output is 4.89 Vpk-pk and swings from 55 mV to 4.945 V.



Design References

See ***Analog Engineer's Circuit Cookbooks*** for TI's comprehensive circuit library.

Texas Instruments, ***Interfacing a Differential-Output (Isolated) Amp to a Single-Ended Input ADC*** application brief.

Design Featured Isolation Amplifier

AMC3302	
Working voltage	1200 V_{RMS}
Gain	41 V/V
Bandwidth	340 kHz TYP
Linear input voltage range	±50 mV
AMC3302	

Design Differential to Single-Ended Amplifier

TLV9002	
V_{CC}	1.8 V to 5.5 V
V_{inCM}, V_{out}	Rail-to-Rail
V_{os}	400 µV
I_q	60 µA
UGBW	1 MHz
SR	2 V/µs
TLV9002	

Design Alternate Isolation Amplifier

AMC3301	
Working voltage	1200 V_{RMS}
Gain	8.2 V/V
Bandwidth	334 kHz TYP
Linear input voltage range	±250 mV
AMC3301	

Design Alternate Differential to Single-Ended Amplifier

TLV6002	
V_{CC}	1.8 V to 5.5 V
V_{inCM}, V_{out}	Rail-to-Rail
V_{os}	750 µV
I_q	75 µA
UGBW	1 MHz
SR	0.5 V/µs
TLV6002	

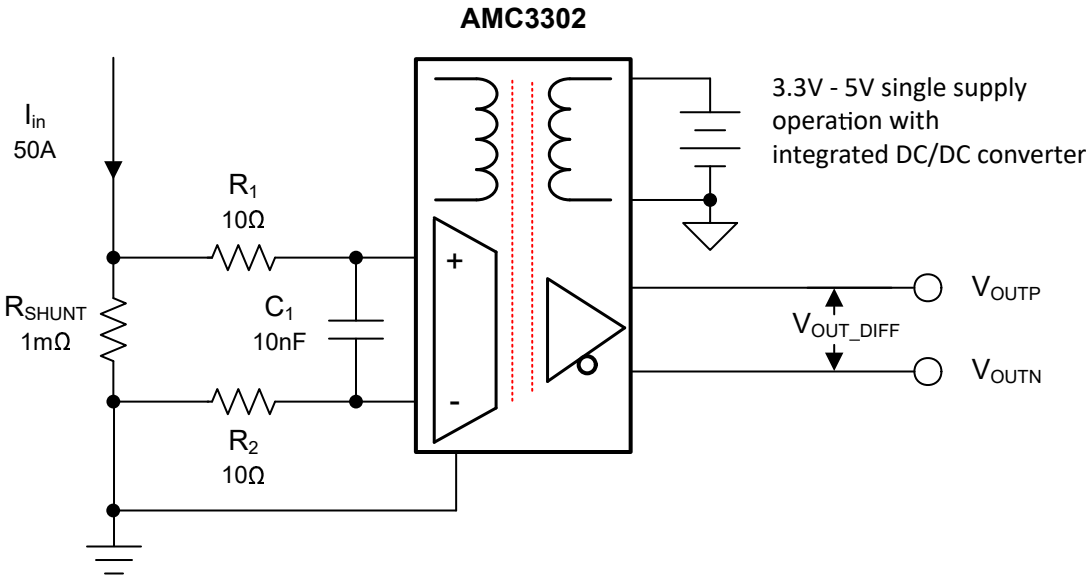
Isolated Current-Sensing Circuit With ±50-mV Input and Differential Output

Design Goals

Current Source		Input Voltage		Output Voltage		Single Power Supply
$I_{IN\ MIN}$	$I_{IN\ MAX}$	$V_{IN\ DIFF,\ MIN}$	$V_{IN\ DIFF,\ MAX}$	$V_{OUT\ DIFF,\ MIN}$	$V_{OUT\ DIFF,\ MAX}$	V_{DD}
–50 A	50 A	–50 mV	50 mV	-2.05 V	2.05 V	5 V

Design Description

This isolated single-supply bidirectional current sensing circuit can accurately measure load currents from –50 A to 50 A. The linear range of the input is from –50 mV to 50 mV with a differential output swing of –2.05 V to 2.05 V and an output common-mode voltage (V_{CM}) of 1.44 V. The gain of the isolated amplifier circuit is fixed at 41 V/V. The design requires 1200-V working voltage to ensure operator safety in a high-voltage application.



Design Notes

1. The AMC3302 was selected due to its high accuracy, small input voltage range and the single, low-side power supply requirement of the application.
2. Select a low impedance, low-noise source for VDD which supplies the AMC3302.
3. For highest accuracy measurements, select a precision shunt resistor with a low temperature coefficient.
4. Select the current shunt resistor based on expected peak input current levels.
5. For continuous operation, do not run shunt resistors at more than two-thirds of the rated current under normal conditions as per IEEE standards. Further reducing the shunt resistance or increasing the rated wattage may be necessary for applications with stringent power dissipation requirements.

Design Steps

1. Determine the transfer equation given the input current range and the fixed gain of the isolation amplifier.

$$V_{OUT} = I_{in} \times R_{shunt} \times 41$$

2. Determine the maximum shunt resistor value.

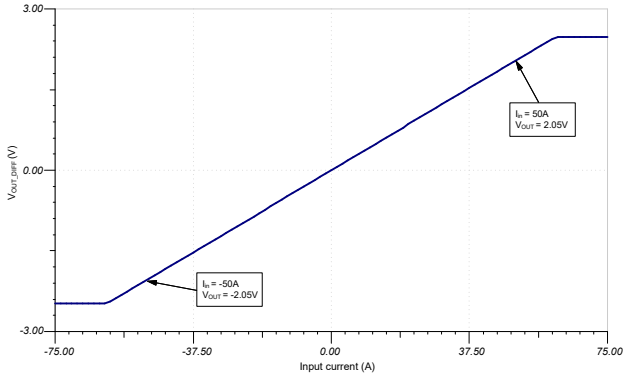
$$R_{shunt} = \frac{V_{inMax}}{I_{inMax}} = \frac{50\ mV}{50\ A} = 1\ m\Omega$$

3. Determine the minimum shunt resistor power dissipation.

$$Power\ R_{shunt} = {I_{inMax}}^2 \times R_{shunt} = 2500\ A \times 0.001\ \Omega = 2.5\ \text{W}$$

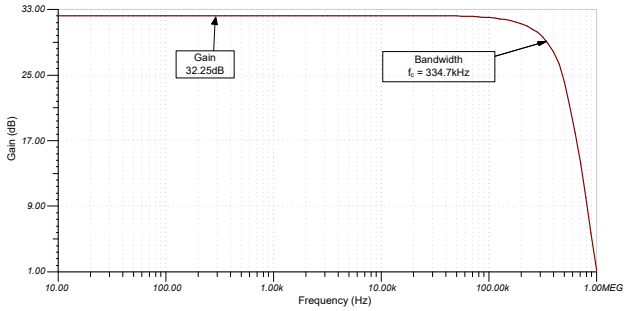
DC Transfer Characteristics

The following plots show the simulated DC characteristics of the AMC3302 differential output. The plot shows that the output is linear with a ±50 A input.



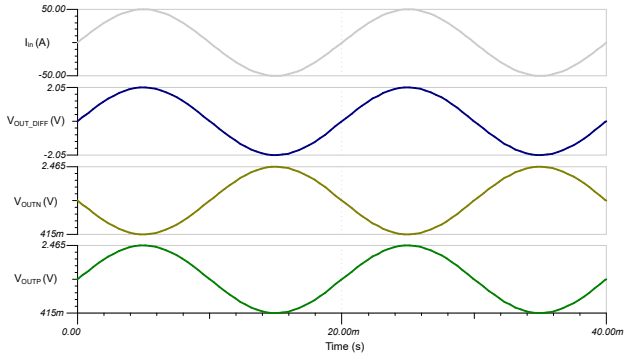
Closed Loop AC Simulation Results

The AC sweep shows the AC transfer characteristics of the differential output. Since the AMC3302 has a gain of 41 V/V, the gain of 33.25-dB shown in the following image is expected.



Transient Simulation Results

The following transient simulation shows the output signals of the AMC3302 from –50 A to 50 A. The differential output of the AMC3302 is ±2.05 Vpk-pk as expected.



Design References

See ***Analog Engineer's Circuit Cookbooks*** for TI's comprehensive circuit library.

Design Featured Isolation Amplifier

AMC3302	
Working voltage	1200 V_{RMS}
Gain	41 V/V
Bandwidth	340 kHz TYP
Linear input voltage range	±50 mV
AMC3302	

Design Alternate Isolation Amplifier

AMC3301	
Working voltage	1200 V_{RMS}
Gain	8.2 V/V
Bandwidth	334 kHz TYP
Linear input voltage range	±250 mV
AMC3301	

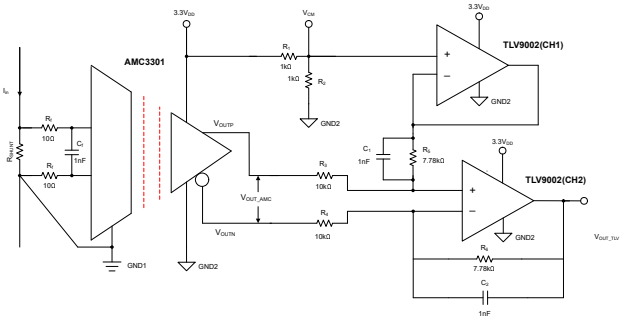
Isolated Current-Sensing Circuit With ±250-mV Input Range and Single-Ended Output Voltage

Design Goals

Current Source		Input Voltage		Output Voltage	Single Power Supply
$I_{IN\ MIN}$	$I_{IN\ MAX}$	$V_{IN\ DIFF,\ MIN}$	$V_{IN\ DIFF,\ MAX}$	$V_{OUT\ SE}$	V_{DD}
–10 A	10 A	–250 mV	250 mV	55 mV to 3.245 V	3.3 V

Design Description

This isolated current sensing circuit can accurately measure load currents from, but not limited to, –10 A to 10 A with a nominal power dissipation of 2.5 W across a 25-mΩ shunt resistor. The linear range of the isolated amplifier input is from –250 mV to 250 mV with a differential output swing of –2.05 V to 2.05 V and an output common-mode voltage (V_{CM}) of 1.44 V. The gain of the isolated amplifier circuit is fixed at 8.2 V/V. A TLV9002 is used to transform the differential output signal to a single-ended signal that can be used with a single-ended ADC such as the ADS8326 as well as buffer the V_{CM} derived from a voltage divider. A 1.65-V reference voltage is used to set the final output voltage range and the common-mode voltage level.



Design Notes

1. The AMC3301 was selected due to its accuracy, input voltage range, and the single low-side power requirements of the device.
2. The TLV9002 was selected for its low cost, low offset, small size, and dual channel package.
3. Select a low impedance, low-noise source for AVDD which supplies the TLV9002 and AMC3301 as well as provides the common-mode voltage for the single-ended output.
4. For highest accuracy, use a precision shunt resistor with a low temperature coefficient.
5. Select the current shunt for expected peak input current levels.
6. For continuous operation, it is recommended that the shunt resistors are not run at more than two-thirds the rated current under normal conditions as per IEEE standards. Further reducing the shunt resistance or increasing the rated wattage may be necessary for applications with stringent power dissipation requirements.
7. Use the proper resistor divider values to set the common-mode voltage on channel 1 of the TLV9002.
8. Select the proper values for the gain setting resistors on channel 2 of the TLV9002 so that the single-ended output has an appropriate output swing.

Design Steps

1. Determine the transfer equation given the input current range and the fixed gain of the isolation amplifier.

$$V_{OUT} = I_{in} \times R_{shunt} \times 8.2$$

2. Determine the maximum shunt resistor value.

$$R_{SHUNT} = \frac{V_{inMax}}{I_{inMax}} = \frac{250mV}{10A} = 25m\Omega$$

3. Determine the minimum shunt resistor power dissipation.

$$\text{Power } R_{SHUNT} = I_{inMax}^{2} \times R_{SHUNT} = 100A \times .025\Omega = 2.5W$$

4. To interface with a 3.3V ADC, the AMC3301 and TLV9002 can both operate at 3.3-V supply voltages so a single-supply can be used.
5. Channel 1 of the TLV9002 is used to set the 1.65-V common-mode voltage of the single-ended output of channel 2. With a 3.3-V supply, a simple resistor divider can be used to divide 3.3 V down to 1.65 V. Using 1 kΩ for R2, R1 can be calculated using the following equation.

$$R_1 = \frac{V_{DD} \times R_2}{V_{CM}} - R_2 = \frac{5V \times 1000\Omega}{2.5V} - 1000\Omega = 1000\Omega$$

6. The TLV9002 is a rail to rail operational amplifier. However, the output of the TLV9002 can swing a maximum of 55 mV from its supply rails. To meet this requirement, the single-ended output of the TLV9002 should swing from 55 mV to 3.245 V (3.19 Vpk-pk) .
7. The V_{OUTP} and V_{OUTN} outputs of the AMC3301 are 2.05 Vpk-pk, 180 degrees out of phase, and have a common-mode voltage of 1.44V. Therefore, the differential output is ±2.05 V or 4.1 Vpk-pk.

   In order to stay within the output limitations of the TLV9002, the output of the AMC3301 needs to be attenuated by a factor of 3.19/4.1. When $R_3 = R_4$ and $R_5 = R_6$, the following transfer function for the differential to single-ended stage can be used to calculate R_5 and R_6.

$$V_{OUT\_TLV} = (V_{OUTP} - V_{OUTN}) \times \left(\frac{R_{5,6}}{R_{3,4}}\right) + V_{CM}$$

8. Using our previously calculated output swing of the TLV9002 and choosing R_3 and R_4 to be 10kΩ, R_5 and R_6 can be calculated to be 7.78kΩ using the equation below.

$$3.245 = (2.465V - 415mV) \times \left(\frac{R_{5,6}}{10k\Omega}\right) + 1.65$$

   Using standard 0.1% resistor values, a 7.77 kΩ can be used. This will provide a maximum output swing within the limitations of the TLV9002.
9. Capacitors C1 and C2 are placed in parallel to resistors R5 and R6 to limit high frequency content. When $R_5 = R_6$ and $C_1 = C_2$, the cutoff frequency can be calculated using the following equation.

$$f_c = \frac{1}{2 \times \pi \times R_{5,6} \times C_{1,2}}$$

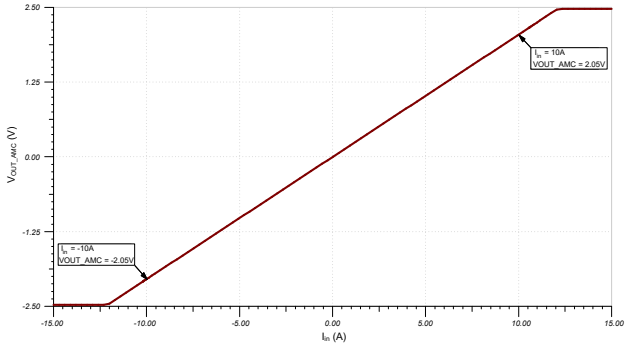
When the C1 = C2 = 1 nF and R5 = R6 = 7780 Ω, the cutoff frequency can be calculated to be 20.45 kHz.

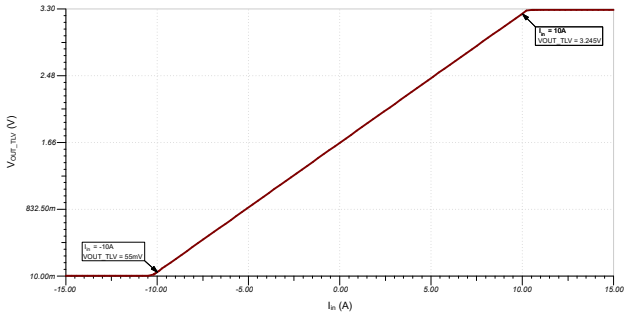
$$f_c = \frac{1}{2 \times \pi \times 7780\Omega \times 1nF} = 20.45kHz$$

Design Simulations

DC Simulation Results

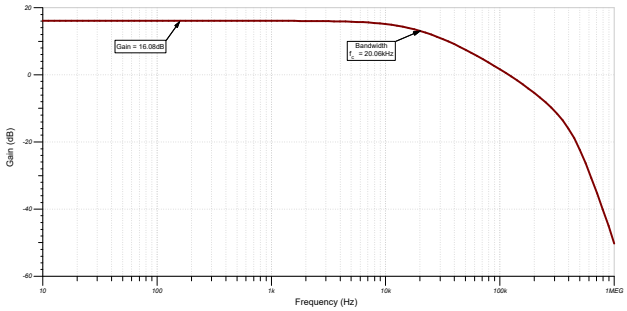
The following plots show the simulated DC characteristics of the AMC3301 differential output and single-ended output of the TLV9002 amplifier. Both plots show that the outputs are linear at ±10 A.





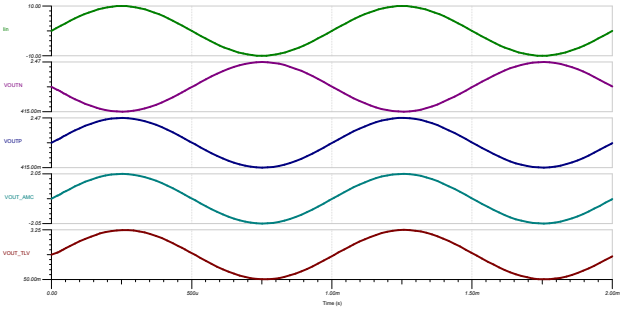
Closed-Loop AC Simulation Results

The following AC sweep shows the AC transfer characteristics of the single-ended output. Using the previously-calculated cutoff frequency illustrated in **the last equation**, shows that the simulation closely matches the simulation. Since the AMC3301 has a gain of 8.2 V/V and a gain of 0.778 V/V is applied with the differential to single-ended conversion, the gain of 16.11 dB shown in the following image is expected.



Transient Simulation Results

The following transient simulation shows the output signals of both the AMC3301 and TLV9002 from –10 A to 10 A. The differential output of the AMC3301 is ±2.05 Vpk-pk as expected and the single-ended output is 3.19 Vpk-pk and swings from 55 mV to 3.245 V.



Design References

See ***Analog Engineer's Circuit Cookbooks*** for TI's comprehensive circuit library and the ***Interfacing a Differential-Output (Isolated) Amp to a Single-Ended Input ADC*** application brief for more information on the differential to single-ended output conversion.

Design Featured Isolated Amplifier

AMC3301	
Working voltage	1200 V_{RMS}
Gain	8.2 V/V
Bandwidth	300 kHz TYP
Linear input voltage range	±250 mV
AMC3301	

Design Alternate Isolated Amplifier

AMC3330	
Working voltage	1200 V_{RMS}
Gain	2 V/V
Bandwidth	310 kHz TYP
Linear input voltage range	±1000 mV
AMC3330	

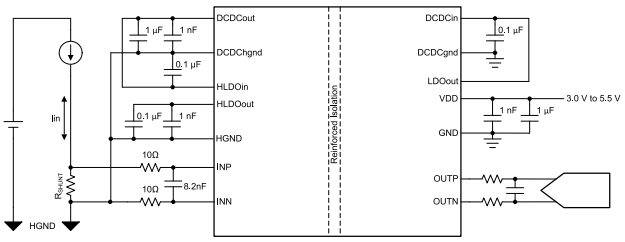
Isolated current-measurement circuit with ±250-mV input and differential output

Design Goals

Current Source		Input Voltage		Output Voltage		Single Power Supply
I_{inMin}	I_{inMax}	Dif V_{INMin}	Dif V_{INMax}	Dif V_{OUTMin}	Dif V_{OUTMax}	V_{DD}
–50A	50A	–250mV	250mV	–2.05V	2.05V	3.0V to 5.5V

Design Description

This isolated single-supply bidirectional current sensing circuit can accurately measure load currents from –50A to 50A. The linear range of the input is from –250mV to 250mV with a differential output range of –2.05V to 2.05V. The gain of the circuit is fixed at 8.2V/V. The design requires 1000-V working voltage to maintain operator safety in a high-voltage application.



Design Notes

1. Select an amplifier with at least 1000-V working voltage across the isolation barrier.
2. Select input filter components to minimize voltage drop from internal bias currents and maintain a –3-dB cutoff frequency of approximately 1MHz.
3. For highest accuracy, use a precision shunt resistor with low temperature coefficient.
4. Select the current shunt for expected peak input current levels.
5. Shunt resistor power should be three to eight times larger than the expected continuous power rating of the system.

Design Steps

1. Determine the transfer equation given the input current range and the fixed gain of the isolation amplifier.

$$V_{OUT} = I_{in} \times Rshunt \times 8.2V$$

2. Determine the maximum shunt resistor.

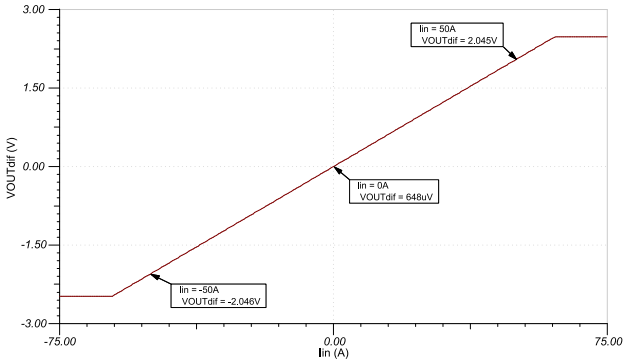
$$Rshunt = \frac{Vshunt}{I_{inMax}} = \frac{250mV}{50A} = 5m\Omega$$

3. Determine the minimum shunt resistor power needed.

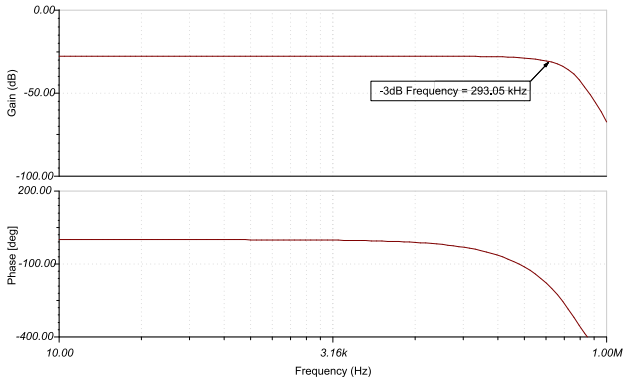
$$Power\ Rshunt = I_{inMax^2} \times Rshunt = 2500 \times 0.005 = 12.5W$$

Design Simulations

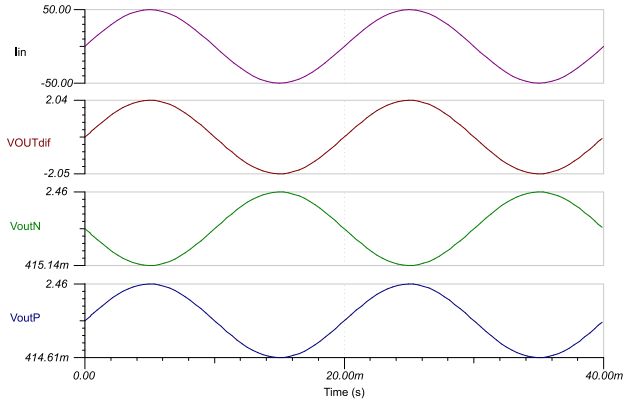
DC Simulation Results



Closed Loop AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files (TINA)

Design files for this circuit – **AMC3301 TINA-TI Reference Design**

Design Featured Op Amp

AMC3301	
Working voltage	$1000V_{RMS}$
Gain	8.2V/V
Bandwidth	300kHz TYP
Linear input voltage range	±250mV
www.ti.com/product/AMC3301	

Design Alternate Op Amp

AMC3330	
Working voltage	$1000V_{RMS}$
Gain	2V/V
Bandwidth	310kHz TYP
Linear input voltage range	±1000mV
www.ti.com/product/AMC3330-Q1	

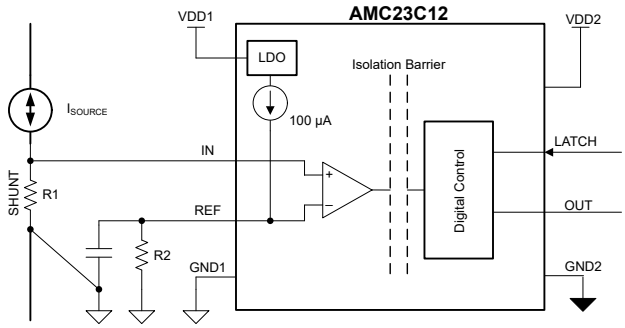
Isolated Overcurrent Protection Circuit

Design Goals

Nominal Current	Overcurrent Level	High-Side Supply	Low-Side Supply	Transient Response Time
50 A	55 A	3 V–27 V	2.7 V–5.5 V	≤ 1000 ns

Design Description

This high-speed, isolated bidirectional overcurrent detection circuit is implemented with the AMC23C12. The AMC23C12 features an isolated window comparator and an adjustable threshold level via a fixed internal precision current source and user-selectable resistor. This circuit is designed for fast detection of overcurrent situations allowing the controller to disable pulse width modulation (PWM) control of high-speed switches used in motor control, traction inverter, and other industrial control systems.



Overcurrent Protection Circuit Schematic

Design Notes

1. To minimize errors, choose a precision shunt resistor (R_1) and the threshold-setting resistor (R_2).
2. The AMC23C12 is powered from the gate-drive supply or high-side auxiliary source up to 27 V.
3. Select the shunt resistor and threshold-setting resistors to match the nominal current and overcurrent limits using the window comparator mode of operation.

Design Steps

1. Determine the size of the shunt resistor based on the nominal current level. The shunt resistor is sized to allow 50 mV at the input pin.

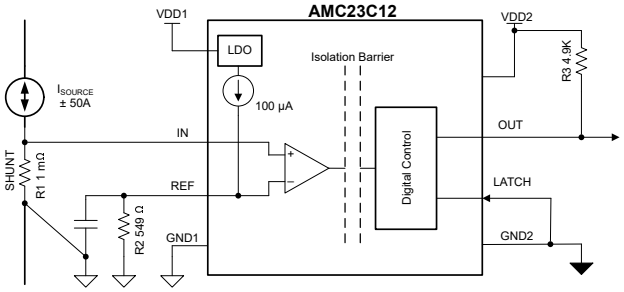
$$R_1 = \left(\frac{50 \ \ mV}{50 \ \ A}\right) = 1.0 \ \ m\Omega$$

2. Determine the value of R2 based on the desired current trip level using the internal 100-µA source and the desired trip level of 55 A with a 1-mΩ shunt for 55 mV at the input to the window comparator.

$$R_2 = \left(\frac{55 \ \ mV}{100 \ \ \mu A}\right) = 550 \ \ \Omega$$

   - Using the **Analog Engineers Calculator**, the closest E96 resister value to 550 Ω is 549 Ω.

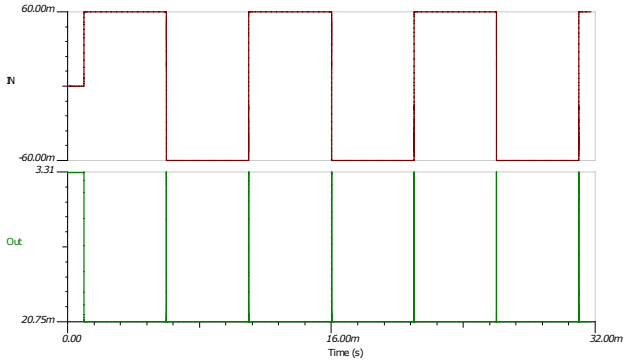
3. Optional - select a 27-V Zener diode to protect the AMC23C12 from voltages greater than the recommended operating supply voltage.



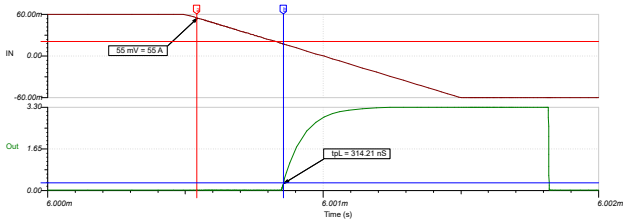
Revised Overcurrent Protection Schematic

Design Simulations

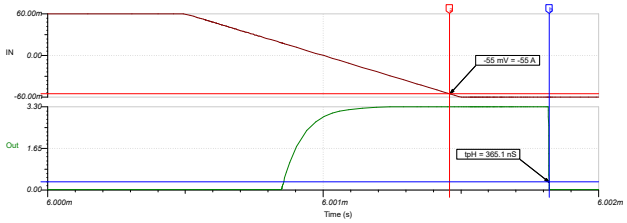
The following images are SPICE simulations of the overcurrent protection circuit. The simulations show the time until the edges trigger which is approximately 360 ns.



Transient Response of Overcurrent Protection Simulation



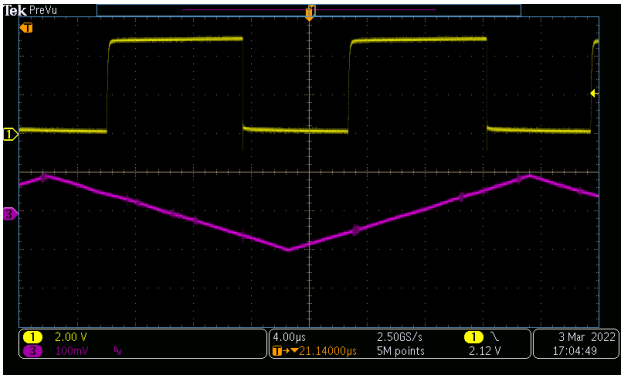
Transient Response of Overcurrent Protection Simulation - Rising



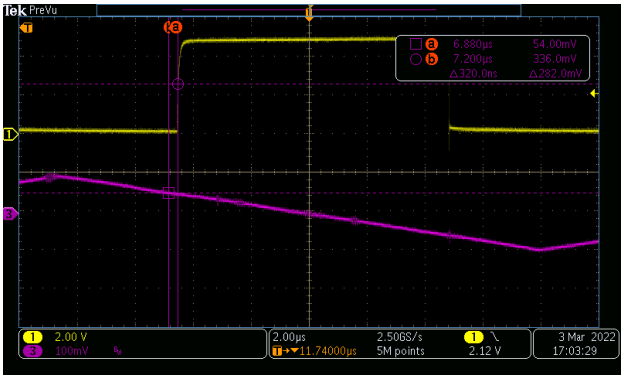
Transient Response of Overcurrent Protection Simulation - Falling

Design Results

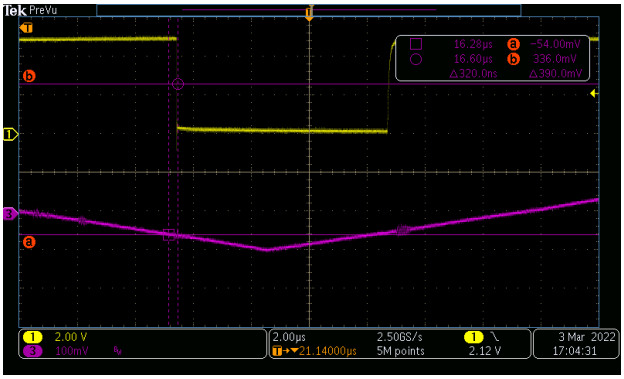
The following images are the waveform captures of the physical circuit. **Overcurrent Protection Circuit Waveform** shows the output on line 1 with relation to input on line 3. **Overcurrent Protection Circuit Waveform - Rising** shows the rising edge of the output line 1 and the time delay from the triggered current to the output. **Overcurrent Protection Circuit Waveform - Falling** shows the falling edge of the output line 1 and the time delay from the triggered current to the output.



Overcurrent Protection Circuit Waveform



Overcurrent Protection Circuit Waveform - Rising



Overcurrent Protection Circuit Waveform - Falling

Design Featured Devices

Device	Key Features	Device Link
AMC23C12	• Wide high-side supply range: 3 V to 27 V • Low-side supply range: 2.7 V to 5.5 V • Adjustable threshold: – Window-comparator mode: ±20 mV to ±300 mV – Positive-comparator mode: 600 mV to 2.7 V • Reference for threshold adjustment: 100 µA, ±2% • Trip threshold error: ±1% (max) at 250 mV • Propagation delay: 290 ns (typ) • High CMTI: 55 kV/µs (min) • Open-drain output with optional latch mode • Safety-related certifications: – 7000-V_{PK} reinforced isolation per DIN VDE V 0884-11 – 5000-V_{RMS} isolation for 1 minute per UL1577 • Fully specified over the extended industrial temperature range: –40°C to +125°C	Device: **AMC23C12** Similar Devices: **Isolated amplifiers**

Design References

See **Analog Engineer's Circuit Cookbooks** for TI's comprehensive circuit library.

Texas Instruments, ***AMC23C12 Fast Response, Reinforced Isolated Window Comparator With Adjustable Threshold and Latch Function*** data sheet

Interfacing a Differential-Output (Isolated) Amp to a Single-Ended Input ADC

Introduction

Whether you are sensing current in an industrial 3-phase servo motor system, a battery management system for an electric vehicle, or a photo voltaic inverter, it is often necessary to include some sort of safety isolation scheme. Safety-related standards define the specific isolation requirements for the end equipment associated with the particular design. Various factors come into play when determining what level of safety insulation (basic, supplemental, or reinforced) is required depending on the type of equipment, the voltage levels involved, and the environment that the equipment is to be installed.

Texas Instruments offers a variety of isolated current shunt amplifiers that are used in the previously-mentioned applications for voltage and current shunt sensing that meet either basic or reinforced insulation requirements. For applications requiring reinforced insulation, one such device is the AMC1301. The output of the AMC1301 is a fully differential signal centered around a common-mode voltage of 1.44 V that can be fed directly to a stand-alone analog-to-digital converter (ADC) as shown in **Figure 15**, or to the on-board ADC found in the MSP430 and C2000 family of microcontroller devices.

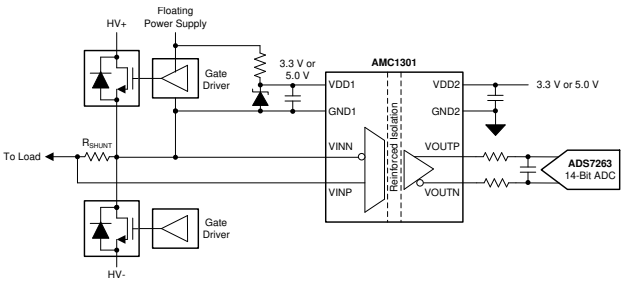


Figure 15. *AMC1301 Functional Block Diagram*

Embedded ADCs

Both the MSP430 and C2000 family of processors have embedded single-ended input ADCs so the question becomes: *How do I get this differential signal into my single-ended data converter?*

The simplest way to achieve this is to use only one output of the AMC1301 leaving the second output floating. The down side to this design is that only half the output voltage swing is available to the data converter, reducing the dynamic range of the measurement. The analog input range to the AMC1301 is ±250 mV. With a fixed gain of 8.2, the VOUTN and VOUTP voltages are ±1.025 V centered around the 1.44-V common-mode output as shown in **Figure 16**. Differentially, the output voltage is ±2.05 V.

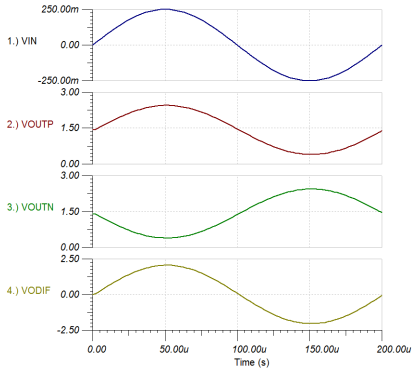


Figure 16. *Differential Output Voltage*

The addition of a differential to single-ended amplifier output stage, shown in **Figure 17**, allows the full output range of the AMC1301 to be provided to the ADC.

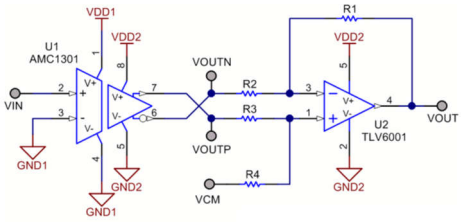


Figure 17. *Differential to Single-Ended Output*

Assuming a full scale sine wave of ±250 mV is applied at VIN; the internal gain of the AMC1301 provides 2.05 Vpk-pk outputs at points VOUTP and VOUTN which are 180° out of phase. The difference between these signals, VODIF, is 4.1 Vpk-pk. When R1 = R4 and R2 = R3, **Equation 8** shows the transfer function of the output stage.

$$\mathrm{VOUT} = \mathrm{VOUTP} \times \left(\frac{\mathrm{R4}}{\mathrm{R3}}\right) - \mathrm{VOUTN} \times \left(\frac{\mathrm{R1}}{\mathrm{R2}}\right) + \mathrm{VCM} \tag{8}$$

With equal value resistors for R1 through R4 in **Equation 8** and VCM set to 2.5 V,**Equation 9** reduces to:

$$\mathrm{VOUT} = (\mathrm{VOUTP} - \mathrm{VOUTN}) + \mathrm{VCM} \tag{9}$$

The plots of **Figure 18** show the input voltage and output voltages of the AMC1301 along with the output voltage of the final differential to single-ended output stage. Note that the differential voltage of ±2.05 V is transposed to a single-ended signal from 0.5 to 4.5 V.

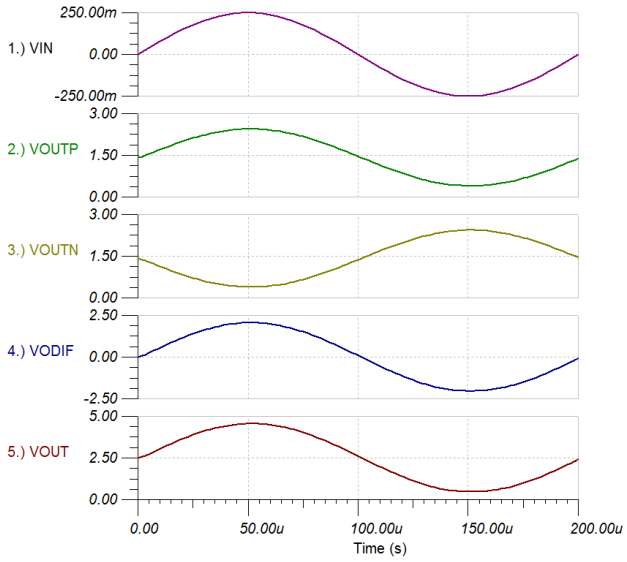


Figure 18. *Single-Ended Output Voltage*

Depending on the input voltage range of the ADC, gain or attenuation can be incorporated into the differential to single-ended stage to adjust the output swing. The output common-mode voltage can be adjusted to fit the input needs of the ADC as well.

Design Example

The ADC12 found on the MSP430 devices have an input voltage range of 0–2.5 V when using the internal voltage reference. Using the VOUTP from the AMC1301 can provide the ADC12 with an input signal ranging from 0.415 V to 2.465 V, well within the input range of the converter while only using half the input range of the AMC1301. As **Figure 19** shows, using a differential to single-ended amplifier configuration with a gain of 0.5 and common mode voltage of 1.25 V, the entire voltage range of the AMC1301 can be applied to the ADC12.

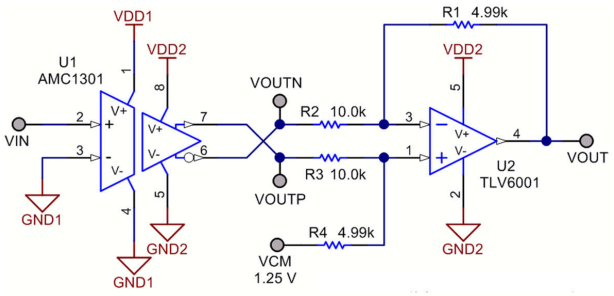


Figure 19. *Scaled Differential to Single-Ended Output*

Alternative Device Recommendations

The AMC1100 or AMC1200 provide basic isolation with similar performance to the AMC1301 at a lower price point. Forthe TLV170 provides this option for applications that require a bipolar output.

Table 5. Alternative Device Recommendations

Device	Optimized Parameter	Performance Trade-Off
AMC1100	Galvanic Isolation up to 4250 V_{PEAK}	Lower Transient Immunity
AMC1200	Galvanic Isolation up to 4250 V_{PEAK}	Basic Isolation versus Reinforced
TLV170	Bi-polar operation to ±18 V	Higher input bias current

Conclusion

While it is possible to use a single output of the AMC1301 to drive a single-ended ADC, adding a differential to single-ended op-amp stage at the output ensures the target application has the largest possible dynamic range.

Related Documentation

1. **Low-Drift, Low-Side Current Measurements for Three-Phase Systems**
2. **Precision Current Measurements on High Voltage Power Supply Rails**

Utilizing AMC3311 to Power AMC23C11 for Isolated Sensing and Fault Detection

Application Brief

Introduction

Fault-detection is essential in applications including **motor drives** , **servo drives** , **onboard chargers (OBCs)**, **string inverters** , and **micro inverters** . Separating the high voltage domain and the low voltage domain across an isolation barrier allows the system to operate at different common-mode voltages. The high voltage domain performs a function while the low voltage domain controls equipment. This prevents both electrical damage to the low voltage circuitry and harm to users. Detecting faults such as overvoltage is required when operating at high common-mode voltages. This document highlights how the AMC3311 can offer high-side supply current from HLDO_OUT to power the high voltage domain of the AMC23C11 isolated comparator for a compact fault detection design.

The AMC3311 is a precision, reinforced, isolated amplifier. This device has a 0-2 V input voltage range, which is an option for precision isolated DC voltage measurements that drive the control loop. This device features an integrated DC/DC converter that supports high-side supply current for auxiliary circuitry of 4 mA. This allows for single-supply operation from the low-side to high-side of the device for both the feedback measurement of the AMC3311 and the overvoltage fault detection of the AMC23C11. The AMC23C11 is a fast response, reinforced, isolated comparator. The device can be used for rapid overcurrent or overvoltage sensing with an adjustable trip threshold. The device requires a high-side supply current of 2.7 mA. The AMC3311 is the first isolated amplifier with an integrated DC/DC converter to enable the two devices to work as a pair for applications that require a precision isolated amplifier for control functions and a fast-acting comparator for overcurrent or overvoltage protection.

AMC3311 used to power AMC23C11

The AMC3311 offers an isolated power supply capable of providing up to 4 mA through the HLDO_OUT pin for connected components that require a high-side supply. This feature directly allows the use of higher performance isolated comparators such as the AMC23C11.

The available supply current from the AMC3311 allows a wider range of companion devices to be used with the isolated amplifier. **Figure 20** shows an example schematic of how to use the AMC3311 to power the high side of the AMC23C11. In the schematic, HLDO_OUT at pin five on the AMC3311 shows a trace that extends to VDD1 at pin one of the AMC23C11. The isolated comparator compares the input voltage to the reference voltage at pin three. The device pulls down the open-drain output if the input voltage exceeds the threshold established as the reference voltage. The threshold voltage can be adjusted by modifying the value of the reference resistor in relation to the internal 100-µA current source.

Additionally, the AMC23C11 has a 1.4-V margin overhead voltage. The threshold voltage cannot be higher than the difference of the 3.2-V input and 1.4-V margin (1.8 V.) A resistor is placed between REF and GND1 to define the trip voltage as 1.07 V. As a result, this overhead requirement limits the threshold voltage on the isolated comparator to be lower than the true cutoff voltage seen on the amplifier. For example, when the true cutoff voltage is 2.14 V on the amplifier, the isolated comparator cannot monitor the voltage because the voltage exceeds the bounds set by the margin overhead voltage. As a result, RSNS is separated into two equal resistors (RSNS1 and RSNS2) to define the cutoff

voltage to be proportionately half of the voltage that the AMC3311 requires. Instead, the AMC23C11 reads 1.07 V as the reference voltage.

Figure 21 shows an example of a PCB layout example that routes the devices in combination.

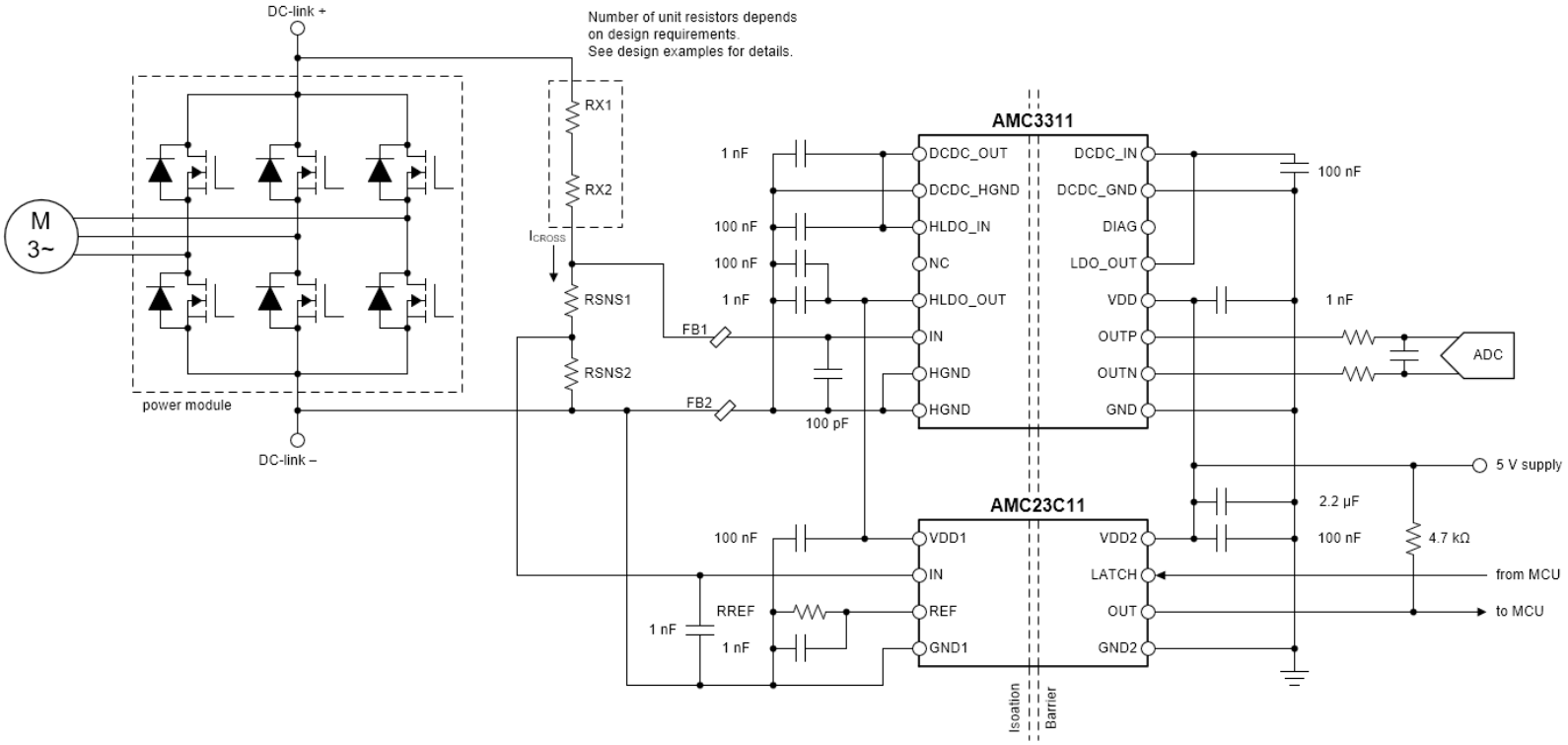


Figure 20. *AMC3311 and AMC23C11 Schematic*

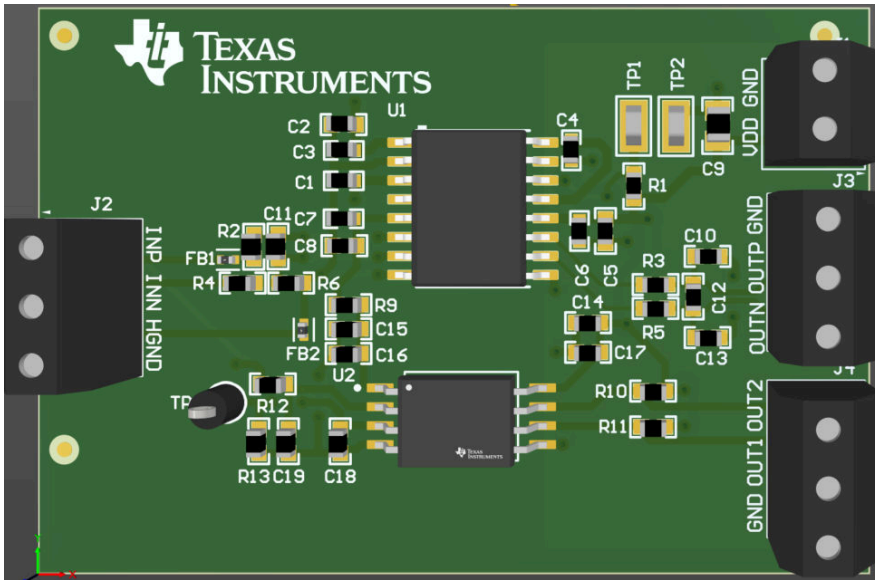


Figure 21. *AMC3311 and AMC23C11 PCB Layout*

AMC23C11 used for overvoltage detection

Figure 22 and **Figure 23** show the overvoltage response times in the AMC3311 and the AMC23C11, respectively. Using a 3.2-V power supply, the input signal (CH4) shows the voltage rise above the 1.07 V overvoltage threshold.

The response time on the AMC3311, VOUTP (CH2), and VOUTN channels (CH1) is 2.906 µs, while the response time on the AMC23C11, OUT (CH3), is 314.015 ns. The amplifier takes greater than nine times the length the isolated comparator takes to detect overvoltage. This time delay can be too long for low latency applications. To supplement the AMC3311 amplifier, the isolated comparator can be used to prevent an overvoltage, as the comparator quickly detects voltages higher than the set threshold. This notifies the controller to shut down all affected electronics, which offers increased safety and reliability in high voltage applications.

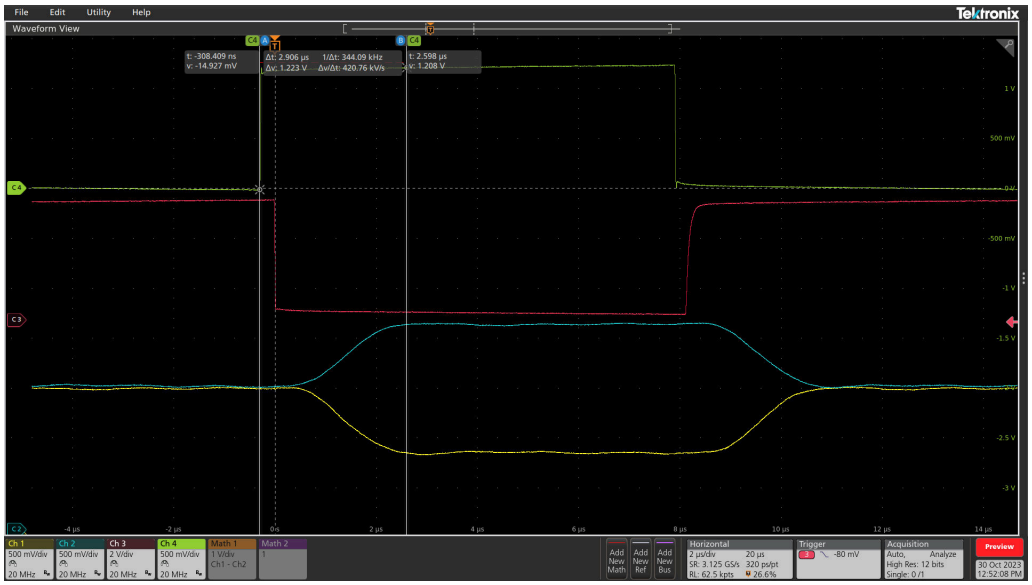


Figure 22. *AMC3311 Overvoltage Response Timing Waveform*

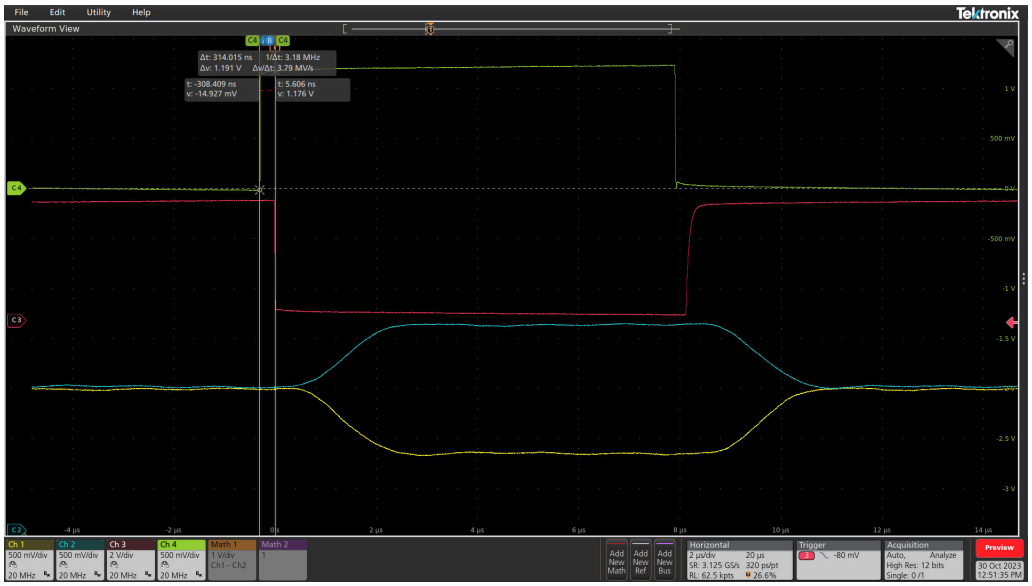


Figure 23. *AMC23C11 Overvoltage Response Timing Waveform*

Conclusion

The AMC3311 is an isolated amplifier with a high-side current supply that can be leveraged to power auxiliary sensing circuits. The device can power external devices up to 4 mA on the high-side, and is compatible with high-speed isolated comparators such as the AMC23C11. This comparator offers the advantage of a significantly faster response time to enable overvoltage protection. Using the AMC3311 and AMC23C11 together can be a useful option for voltage and current sensing applications.

Additional Resources

- Texas Instruments, **Precision labs series: Introduction to isolation**, video series.
- Texas Instruments, ***AMC3311-Q1 Automotive, Precision, 2-V Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter***, data sheet.
- Texas Instruments, ***AMC23C11 Fast Response, Reinforced Isolated Comparator With Adjustable Threshold and Latch Function***, data sheet.
- Texas Instruments, ***Isolation Glossary***
- Texas Instruments, ***Isolated Amplifier Voltage Sensing Excel Calculator***, design resource.

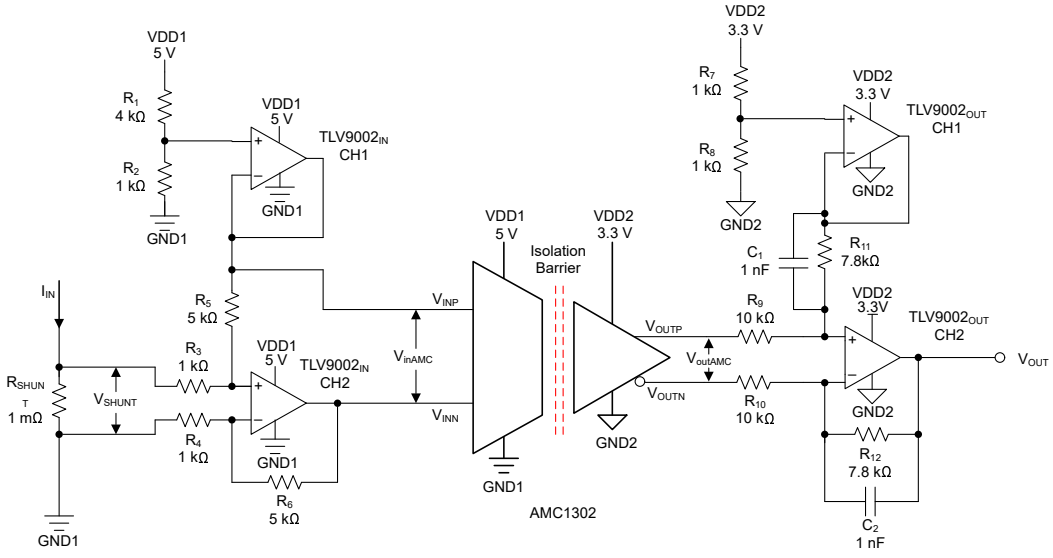
Isolated Current-Sensing Circuit With Front-End Gain Stage

Design Goals

Current Source (Nominal)		Current Source (Short)	Input Voltage		Output Voltage	Power Supplies	
$I_{IN\ MIN}$	$I_{IN\ MAX}$	I_{SHORT}	$V_{SHUNT,\ MIN}$	$V_{SHUNT,\ MAX}$	V_{OUT}	V_{DD1}	V_{DD2}
±10 mA	±10 A	±200 A	±10 µV	±10 mV	55 mV – 3.245 V	5 V	3.3 V

Design Description

Some applications require a circuit to measure small nominal currents while withstanding a high short-circuit current, such as a circuit breaker. This circuit design document describes an isolated current-sensing circuit that can accurately measure nominal load currents from ±10 mA to ±10 A, while withstanding a short-circuit current up to ±200 A. For the purposes of this circuit, assume the output is used with a 3.3-V single-ended ADC, such as one that can be found integrated into an MSP430. The isolation between the line current being measured and the ADC is achieved using an isolated amplifier (AMC1302). With a 1-mΩ shunt resistor, the expected minimum nominal current produces a ±10-µV signal, a signal which is too small to resolve accurately near a zero voltage input due to the delta-sigma modulator dead zone. To remedy this, the circuit uses a 2-channel operational amplifier (TLV9002) to both amplify the signal by a gain of 5 V/V and set the common-mode voltage to 1 V; this not only brings the minimum nominal current out of the dead zone, but also brings the maximum nominal current up to match the full-scale linear input range of the isolated amplifier. The full-scale linear input range of the isolated amplifier is ±50 mV, with a differential output swing of ±2.05 V, on an output common-mode voltage of 1.44 V and a fixed internal gain of 41 V/V. On the output side of the isolated amplifier, a second 2-channel operational amplifier (TLV9002) is used, where: the first channel is used to set the single-ended common-mode voltage to 1.65 V and the second channel transforms the differential output signal from the isolated amplifier into a single-ended that can be used with a 3.3-V single-ended ADC.



Design Notes

1. The AMC1302 was selected as the isolated amplifier due to the low power consumption, resolution, and ±50-mV full-scale input voltage range of the amplifier.
2. The TLV9002 was selected as the operational amplifier for the low cost, low offset, small size, and dual-channel package.
3. Select a low impedance, low-noise source for both VDD1 and VDD2 which provide supply for the $TLV9002_{IN}$, $TLV9002_{OUT}$, and AMC1302; while also being used to set the common-mode voltage for the single-ended output.
   - VDD1 is referenced to GND1 and VDD2 is referenced to GND2.
4. For the highest accuracy, use a precision shunt resistor with a low temperature coefficient.
5. Select the shunt resistor for expected nominal and short-circuit input current levels.
   a. For continuous operation, do not run the shunt resistors at more than two-thirds the rated current under normal conditions as per IEEE standards. Further reducing the shunt resistance or increasing the rated wattage can be necessary for applications with stringent power dissipation requirements.
   b. For short-circuit current, check the short-term overload specification in the shunt resistor data sheet. The current is often 5 × the nominal power dissipation.
   c. For assistance with calculating the power dissipation, see the **Isolated Amplifier Current Sensing Excel Calculator**.
6. Use the proper resistor divider values to set the common-mode voltage on channel 1 of both the $TLV9002_{IN}$ and $TLV9002_{OUT}$. Make sure the input common-mode specification of the isolated amplifier is not violated.
7. Select the proper values for the gain setting resistors on channel 2 of the $TLV9002_{OUT}$ so that the single-ended output has an appropriate output swing.

Design Steps

1. Determine the appropriate shunt resistor value based on the maximum nominal current.

$$R_{SHUNT} = \frac{V_{inMax}}{I_{inMax}} = \frac{50\ mV}{10\ A} = 5\ m\Omega$$

2. Since this shunt resistor must be able to withstand a 200-A short-circuit current, further reduce the shunt resistor resistance by a factor of 5 which is compensated for in **step 6**. Determine the shunt resistor power dissipation during maximum nominal current operation.

$$Power\ R_{SHUNT} = {I_{inMax}}^2 \times R_{SHUNT} = 100\ A^2 \times 1\ m\Omega = 0.1\ W$$

   Determine the shunt resistor power dissipation during minimum nominal current operation.

$$Power\ R_{SHUNT} = {I_{inMin}}^2 \times R_{SHUNT} = 0.1\ mA^2 \times 1\ m\Omega = 0.1\ \mu W$$

3. Determine the shunt resistor power dissipation during short circuit. Be sure to verify that the selected short-term overload specification (typically 5 × nominal) is capable of withstanding the power dissipated by the short circuit.

$$Power\ R_{SHUNT} = {I_{inShort}}^2 \times R_{SHUNT} = 40{,}000\ A^2 \times 1\ m\Omega = 40\ W$$

Select a shunt resistor with power dissipation reduced by a factor of 5. So, if the short-term overload requirement is 40 W, shunt $P_{dissipation}$ = 8 W. For more details, see the ***Design considerations for isolated current sensing*** analog design journal.

4. Channel 1 of the $TLV9002_{IN}$ is used to set the 1-V common-mode voltage of the single-ended output of channel 2 of the $TLV9002_{IN}$. The 1-V output of channel 1 is also sent to the positive input of the AMC1302. With a 5-V supply, a simple resistor divider can be used to divide 5 V down to 1 V. Using 4 kΩ for R_1, R_2 can be calculated using the following equation.

$$R_2 = \frac{V_{CM} \times R_1}{V_{DD} - V_{CM}} = \frac{1.00\,V \times 4000\,\Omega}{5.00\,V - 1.00\,V} = 1000\,\Omega$$

5. Channel 2 of the $TLV9002_{IN}$ is used to amplify the voltage from the shunt resistor such that the full-scale input voltage range of the AMC1302 is utilized when measuring the maximum nominal current range. With a shunt resistor of 1 mΩ and a maximum nominal current of ±10 A, the output voltage from the shunt resistor is ±10 mV. Since the maximum input voltage of the AMC1302 is ±50 mV, the output of the shunt resistor must be amplified by 5 V/V. While keeping R3|R4 at 1 kΩ, the resistor value of R5|R6 can be found with the following equation.

$$Gain\left(V/V\right) = \frac{R_{5,6}}{R_{3,4}};\ R_{5,6} = Gain\left(V/V\right) \times R_{3,4} = 5\ V/V \times 1\ k\Omega = 5\ k\Omega$$

6. Verify the absolute maximum voltage limits of the input of the AMC1302 are not violated during a short-circuit based on the chosen shunt resistor. A 200-A short-circuit current results in a 1-V differential voltage being applied to the AMC1302. Since the input common mode is set to 1 V, a maximum of 2 V is applied to the negative input of the AMC1302 with respect to GND1.

$$V_{inAMC} = 200\,A \times 0.001\,\Omega \times 5\ V/V = 1\,V$$

The absolute maximum input voltage for the AMC1302 is 500 mV greater than the high-side supply voltage (as stated in the ***AMC1302 Precision, ±50-mV Input, Reinforced Isolated Amplifier*** data sheet). With a 5-V high-side supply voltage, the absolute maximum input voltage rating is not violated.

7. Channel 1 of the $TLV9002_{OUT}$ is used to set the 1.65-V common-mode voltage of the single-ended output of channel 2 of $TLV9002_{OUT}$. With a 3.3-V supply, a simple resistor divider can be used to divide 3.3 V down to 1.65 V. Using 1 kΩ for R_7, R_8 can be calculated using the following equation.

$$R_8 = \frac{V_{CM} \times R_7}{V_{DD} - V_{CM}} = \frac{1.65\,V \times 1000\,\Omega}{3.3\,V - 1.65\,V} = 1000\,\Omega$$

8. While the TLV9002 is a rail-to-rail operational amplifier, the output of a TLV9002 can only swing a maximum of 55 mV from the supply rails. Due to this, the single-ended output of $TLV9002_{OUT}$ can swing from 55 mV to 3.245 V (3.19 $V_{pk\text{-}pk}$).
9. The V_{OUTP} and V_{OUTN} outputs of the AMC1302 are 2.05 $V_{pk\text{-}pk}$, 180 degrees out of phase, and have a common-mode voltage of 1.44 V. Therefore, the differential output is ±2.05 V or 4.1 $V_{pk\text{-}pk}$.

To stay within the output limitations of $TLV9002_{OUT}$, the output of the AMC1302 needs to be attenuated by a factor of 3.2 / 4.1. When $R_9 = R_{10}$ and $R_{11} = R_{12}$, the following transfer function for the differential to single-ended stage can be used to calculate R_{11} and R_{12}.

$$V_{OUT} = (V_{OUTP} - V_{OUTN}) \times \left(\frac{R_{11,12}}{R_{9,10}}\right) + V_{CM}$$

10. Using the previously-calculated output swing of the $TLV9002_{OUT}$ and setting R_9 and R_{10} to be 10 kΩ, R_{11} and R_{12} can be calculated to be 7.8 kΩ using the following equation.

$$3.2 = (2.465\ \text{V} - 415\ \text{mV}) \times \left(\frac{R_{11,12}}{10\ k\Omega}\right) + 1.65$$

Using standard 0.1% resistor values, a 7.8 kΩ resistor can be used. This provides the maximum output swing within the limitations of the TLV9002.

11. Capacitors C_1 and C_2 are placed in parallel to resistors R_{11} and R_{12} to limit high-frequency signals. When $R_{11} = R_{12}$ and $C_1 = C_2$, the cutoff frequency can be calculated using the following equation.

$$f_c = \frac{1}{2 \times \pi \times R_{11,12} \times C_{1,2}}$$

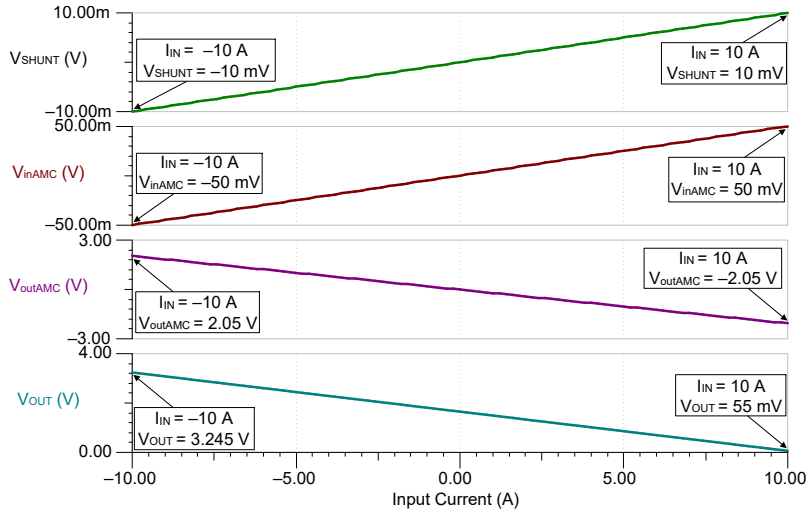
When the $C_1 = C_2 = 1$ nF and $R_{11} = R_{12} = 7800\ \Omega$, the cutoff frequency can be calculated to be 20.414 kHz.

$$f_c = \frac{1}{2 \times \pi \times 7800\ \Omega \times 1\ \text{nF}} = 20.414\ \text{kHz}$$

Design Simulations

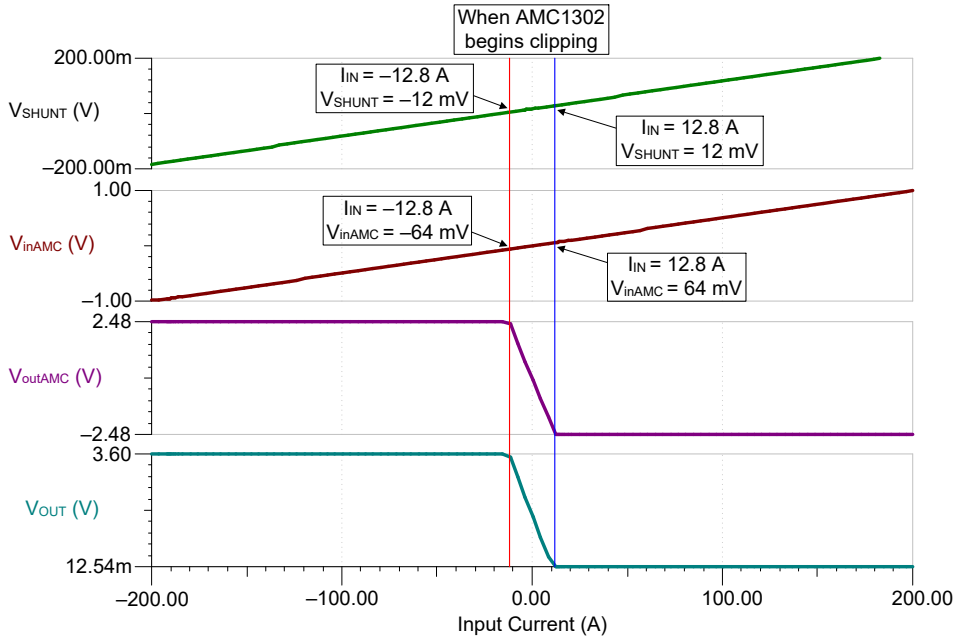
DC Simulation Results

Simulation Results shows the simulated DC characteristics of the voltage across the shunt, the differential input/output of the AMC1302, and the single-ended output of the TLV9002 amplifier from –10 A to 10 A.



Simulation Results

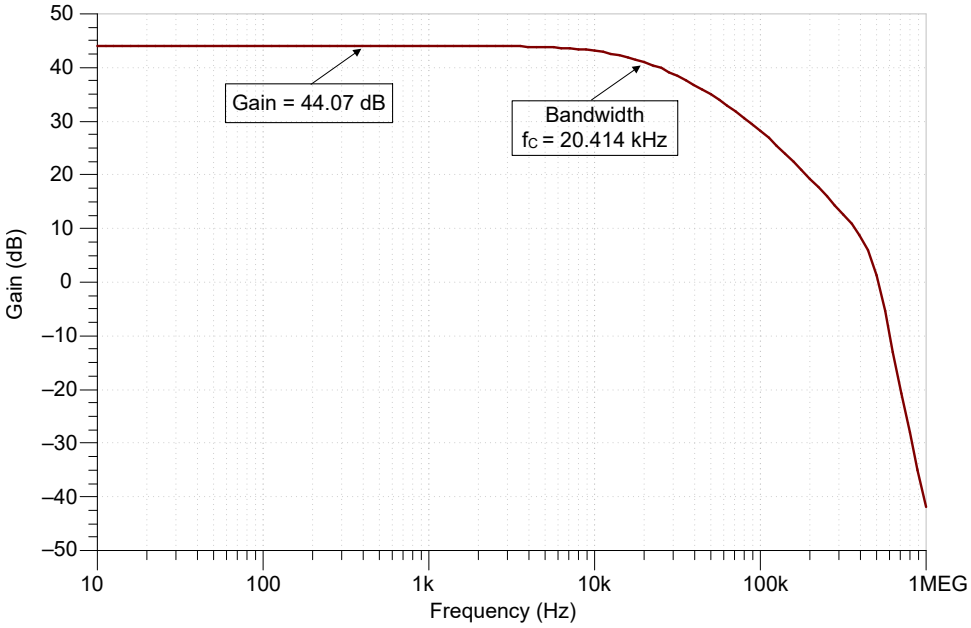
Short-Circuit Event Simulation shows a simulation of the circuit during a short-circuit event by demonstrating how the inputs and outputs react at ±200 A. The red and blue lines going through the graphs mark the points where the output of the AMC1302 begins clipping. From that point on, the purpose of the circuit is to continue operating after the short-circuit event. In the **Design Steps** section, the values of the gain and shunt-resistance on the high-side of the AMC1302 were chosen to avoid damage during this event. The following simulation validates those choices: the maximum input voltage entering the AMC1302 at the short-circuit event is ±1 V, which is lower than the absolute maximum ratings of the part. Therefore, the simulation confirms that the circuit continues operation after the short-circuit event passes.



Short-Circuit Event Simulation

Closed-Loop AC Simulation Results

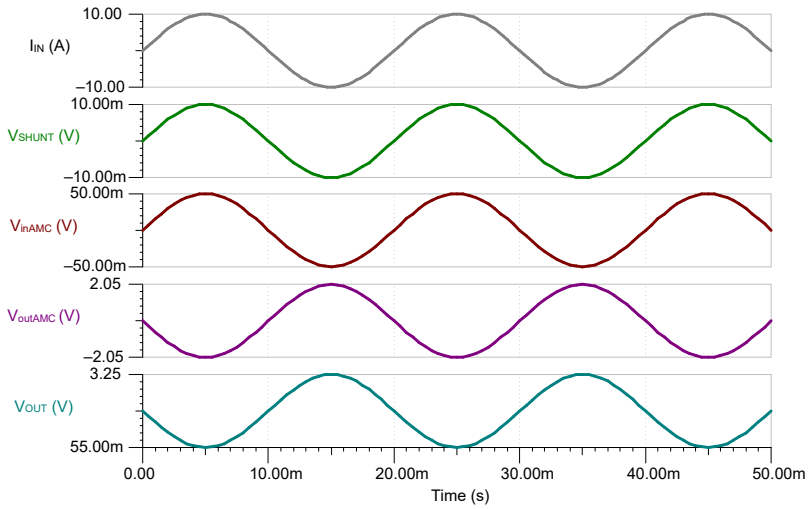
AC Simulation shows the AC transfer characteristics of the single-ended output. This simulation shows what gain (dB) to expect as the frequency approaches and surpasses the cutoff that is calculated with the second equation in **11**. The analog front end has a gain of 5 V/V, the AMC1302 has a gain of 41 V/V, and the differential-to-single-ended conversion has a gain of 0.78 V/V; thus a gain of 44.07 dB is expected, which is illustrated in the following figure.



AC Simulation

Sine-Wave Simulation Results

Sine-Wave Simulation shows the output of the shunt, the differential input and output of the AMC1302, and the single-ended output of the TLV9002 in response to a sine wave with an amplitude from –10 A to 10 A. The differential output of the AMC1302 is ±2.05 V_{pk-pk} as expected, and the single-ended output is 3.19 V_{pk-pk} and swings from 55 mV to 3.245 V.



Sine-Wave Simulation

Design References

See the ***Analog Engineer's Circuit Cookbooks*** for TI's comprehensive circuit library and the ***Interfacing a Differential-Output (Isolated) Amp to a Single-Ended Input ADC*** application brief for more information on the differential to single-ended output conversion.

Design Featured Isolated Amplifier

Working Voltage	1500 V_{RMS}
Gain	41 V/V
Bandwidth	280 kHz TYP
Linear Input Voltage Range	±50 mV
Input Resistance	4.9 kΩ (typ)
Input Offset Voltage and Drift	±50 µV (max), ±0.8 µV/°C (max)
Gain Error and Drift	±0.2% (max), ±35 ppm/°C (max)
Nonlinearity and Drift	0.03% (max), 1 ppm/°C (typ)
Isolation Transient Overvoltage	7071 V_{PEAK}
Common-Mode Transient Immunity, CMTI	100 kV/µs (min)

Design Alternate Isolated Amplifier

Working Voltage	1200 V_{RMS}
Gain	41 V/V
Bandwidth	334 kHz TYP
Linear Input Voltage Range	±50 mV
Input Resistance	4.9 kΩ (typ)
Input Offset Voltage and Drift	±50 µV (max), ±0.5 µV/°C (max)
Gain Error and Drift	±0.2% (max), ±35 ppm/°C (max)
Nonlinearity and Drift	±0.03% (max), 1 ppm/°C (typ)
Isolation Transient Overvoltage	6000 V_{PEAK}
Common-Mode Transient Immunity, CMTI	95 kV/us (min)

Working Voltage	1000 V_{RMS}
Gain	41 V/V
Bandwidth	280 kHz TYP
Linear Input Voltage Range	±50 mV
Input Resistance	4.9 kΩ (typ)
Input Offset Voltage and Drift	±50 µV (max), ±0.8 µV/°C (max)
Gain Error and Drift	±0.2% (max), ±35 ppm/°C (max)
Nonlinearity and Drift	±0.03% (max), 1 ppm/°C (typ)
Isolation Transient Overvoltage	4250 V_{PEAK}
Common-Mode Transient Immunity, CMTI	100 kV/µs (min)

Accuracy Comparison of Isolated Shunt and Closed-Loop Current Sensing

Introduction

Several industrial and automotive applications such as **on board chargers**, **solar inverters**, **DC charging (pile) stations**, **power conversion systems**, and **motor drives** require isolation to protect the digital circuitry from the high-voltage circuit performing a measurement. Two ways to accomplish the isolated current sensing for these applications are isolated shunt based sensing and magnetic (Hall or flux-gate) based sensing. This document compares Texas Instruments **AMC3302** a single-supply, **isolated amplifier** to a popular closed-loop current sensor (CLCS).

Technologies Overview

Isolated shunt based current sensing relies on measuring a voltage across a precise in-line resistor, known as a shunt resistor.

Figure 24. *Isolated Shunt Based Current Sensing*

The shunt resistance must be very accurate in order to produce the expected voltage for the supplied current, as any variation in expected resistance will contribute directly to a gain error. The benefit of shunt based current sensing is that it allows for industry leading accuracy, immunity to magnetic interference, scalability and small size.

CLCS uses a magnetic core to sense the magnetic field created by the current passing through the primary conductor. The magnetic field sensing element included in the CLCS is used to provide a compensation current that is applied to the magnetic core. This compensation current creates a flux that is equal in magnitude, but in the opposite direction of the flux created by the primary conductor; producing a zero-flux measurement. Magnetic based current sensing is vulnerable to magnetic interference which can affect the offset and linearity performance of the device.

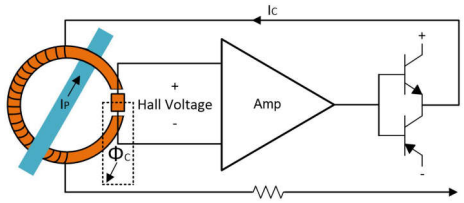


Figure 25. *Hall Based Closed-Loop Sensor*

Additional information comparing the two technologies can be found **here**.

Test Setup

A test setup was created in order to directly compare the performance of these two technologies. A DC current source, electronic load and digital multi-meters were used to capture data for a +/-85A primary current sweep at three different temperatures; -40C, 25C and 85C. All measurements were automated according to IEEE488.

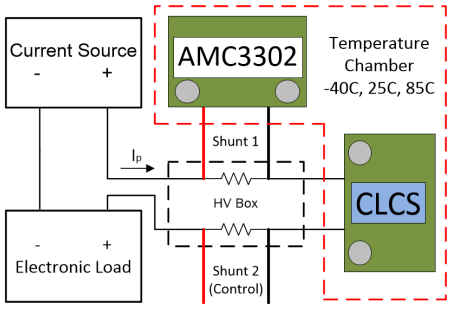


Figure 26. *AMC3302 Circuit and CLCS Test Setup Block Diagram*

Please note that the 500µΩ Shunt 1 used for the AMC3302 circuit measurement and 500µΩ Shunt 2 used for the control measurement were not subjected to changes in ambient temperature, therefor the shunt temperature drift error is not included in this analysis. Both shunts are rated for ±0.25% tolerance, ±15ppm/°C temperature coefficient and 20W power dissipation.

The circuit diagram below shows the **AMC3302** and **TLV6002** circuit used for the accuracy comparison. Channel 1 of the TLV6002 was used to buffer a reference voltage generated via resistor divider while the differential output of the AMC3302 was converted from differential to single-ended via channel 2. Thus the AMC3302 circuit has an identical interface as the CLCS; VDD, GND, VREF and VOUT.

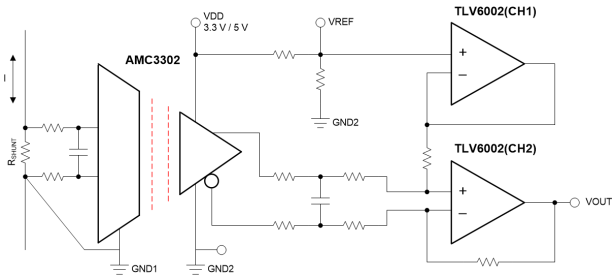


Figure 27. *AMC3302 Circuit Diagram*

Below is the AMC3302 Printed Circuit Board (PCB). The PCB was designed such that the AMC3302 circuit fits within the same x, y footprint as the CLCS, 13.4mm x 21.9mm. The AMC3302 PCB is much smaller in terms of height; 2.6mm compared to 16mm for the CLCS, a reduction in height of 84%.

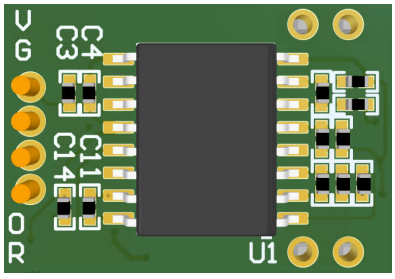


Figure 28. *AMC3302 Circuit Printed Circuit Board*

Accuracy Comparison

Figure 6. shows the accuracy results for the +/-85A primary current sweep over temperature in terms of error as a percentage of full-scale output after a 25C offset calibration. The AMC3302 circuit results are shown in shades of red and the CLCS in blue. The AMC3302 circuit is very accurate over the full current and temperature range without gain calibration, better than 0.1%. The CLCS shows worse gain error drift and linearity performance compared to the AMC3302 circuit, resulting in an overall error greater than 0.5%. The AMC3302 circuit offers an accuracy improvement of more than 5x compared to the CLCS over the full current and temperature range.

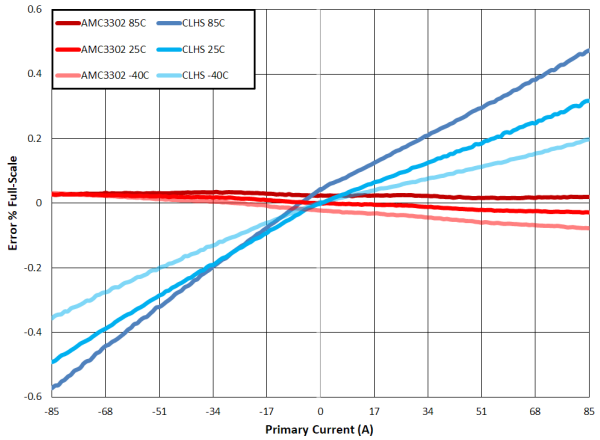


Figure 29. *Accuracy Comparison for AMC3302 Circuit and Closed-loop Current Sensor After Offset Calibration*

Below shows an accuracy comparison table of absolute maximum error.

Temperature	-40C	25C	85C
AMC3302 Circuit	-0.077%	-0.029%	0.035%
CLCS	-0.356%	-0.492%	-0.573%

Conclusion

The table below summarizes the comparison of the AMC3302 circuit and the CLCS. For systems requiring industry leading accuracy, the AMC3302 circuit shows a clear advantage compared to the CLCS. The size of the AMC3302 circuit used for this comparison is equal size in terms of x and y dimensions, while showing a clear advantage in terms of height, z. The AMC3302 circuit also offers immunity to magnetic interference, as well as scalability.

	AMC3302 Circuit	CLCS
Accuracy	++	+
Size	+	-
Magnetic Immunity	++	--
Scalability	++	-
Ease of Design	+	++

Voltage Sensing

- Maximizing Power Conversion and Motor Control Efficiency With Isolated Voltage Sensing
- Increased Accuracy and Performance with Integrated High Voltage Resistor Isolated Amplifiers and Modulators
- Isolated Amplifiers With Differential, Single-Ended Fixed Gain and Ratiometric Outputs for Voltage Sensing Applications
- Isolated Voltage-Measurement Circuit With ±250-mV Input and Differential Output
- Split-Tap Connection for Line-to-Line Isolated Voltage Measurement Using AMC3330
- ±12V Voltage Sensing Circuit With an Isolated Amplifier and Pseudo-Differential Input SAR ADC
- ±12-V voltage sensing circuit with an isolated amplifier and differential input SAR ADC
- Isolated Undervoltage and Overvoltage Detection Circuit
- Isolated Zero-Cross Detection Circuit
- ±480V Isolated Voltage-Sensing Circuit With Differential Output

Maximizing Power Conversion and Motor Control Efficiency With Isolated Voltage Sensing

With growing demand to harvest more renewable energy sources expanding across automotive and industrial applications, the need for small, efficient, accurate and cost-effective power converters and motor controllers is increasing at an unprecedented rate.

Accurate, isolated voltage sensing to measure high voltages presents a significant electrical engineering challenge – and the voltages are only getting higher. DC voltages are increasing from $400V_{DC}$ to $800V_{DC}$ and even as high as $1,500V_{DC}$. Affordability for consumers is also becoming increasingly important, and size optimization is pushing for greater innovation. Thus, a precise, size-optimized, galvanically isolated voltage-sensing device that meets today's requirements is becoming mandatory.

Automakers annually state goals to develop electric vehicles (EVs) that support a longer driving range (>400 miles) and provide better operational safety, while maintaining affordability. Integrated, isolated DC voltage-sensing devices can maximize DC voltage measurements and enable longer driving ranges by providing less than 1% accuracy error of the DC battery voltage in onboard chargers, DC/DC converters and battery-management systems. Integrated, isolated AC voltage-sensing devices can accurately measure single- or three-phase AC grid voltages in a compact integrated circuit (IC), maximizing grid use of the voltage levels. Both AC and DC isolated voltage sensing devices can provide operational safety by detecting functional failures and notifying drivers. AC and DC isolated voltage sensing devices can also enable affordability by integrating external components into a single IC, helping designers accelerate time to market with more energy-efficient designs.

In a smart energy infrastructure, isolated voltage-sensing devices with advanced integration can enable cost reduction and increased power density in DC and AC chargers, energy storage systems, and solar inverters. These isolated voltage-sensing devices can also enable high-accuracy voltage measurements with less than 1% accuracy error for more precise power delivery and lower power dissipation. The improved efficiency then makes it possible to pass the cost savings on to consumers.

Energy infrastructure applications require both AC and DC voltage measurements.

For AC voltage sensing, an accurate isolated voltage sensor allows for a more precise measurement of the grid voltage, which is important for power converters because you need to know the phase difference between each voltage in order to perform power factor correction. In inverter mode, isolated voltage sensors provide precise voltage levels to the load, grid, or both.

For DC voltage sensing, an accurate isolated voltage sensor helps facilitate faster charge during the constant voltage phase when charging the battery to the final voltage, without damaging the battery.

Figure 30 shows an example of where isolated voltage sensing occurs in electric vehicles and energy infrastructure.

Figure 30. *Isolated voltage sensing in EVs and energy infrastructure systems.*

In today's motor-control applications, including industrial motor drives and automotive traction inverters, there is a growing need for more accurate measurements of the DC voltage. A highly accurate and compact IC can enable more efficient DC measurements and not take up much space on the printed circuit board (PCB), which are both challenges in motor-control applications.

Solutions for high-voltage sensing

At TI, there is a strong emphasis on developing products to help solve market challenges and enable more efficient, cost-effective and accurate power-conversion and motor-control systems. We have developed two new isolated voltage-sensing technologies, including integrated high-voltage resistor and single-ended output devices.

Integrated resistor devices

The **AMC0380D04-Q1**, **AMC0381D10-Q1** and **AMC0386M10-Q1** family of galvanically isolated voltage sensing amplifiers and modulators integrate high-voltage resistive dividers and eliminate the need for large and expensive external resistors to step down the voltage to a ±1V or 0V to 2V level. Stand-alone high-voltage resistors can take up a lot of space on PCBs, given that you may need as many as 15 high-voltage resistors to step down the voltage and maintain the system's isolation ratings. Stand-alone high-voltage resistors are also a significant source of measurement error, lifetime drift and temperature drift, and require end-of-line calibration.

When it comes to conserving board space, the AMC0380D04-Q1 ±400V_{AC} input isolated amplifier, AMC0381D10-Q1 1,000V_{DC} input isolated amplifier and AMC0386M10-Q1 ±1,000V_{AC} input isolated modulator save system-level costs and reduce solution size as much as 50% by removing the need for external high-voltage resistors, as shown in **Figure 31**.

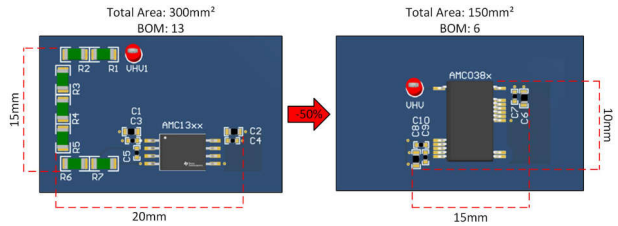


Figure 31. *Integration benefits of the integrated resistor family.*

Integrating the high-voltage resistors into our isolated voltage-sensing devices eliminates the need for a large resistor ladder. We've also eliminated the need for system-level calibration by calibrating out the gain error of the internal resistor

for the AMC0380D04-Q1, AMC0381D10-Q1 and AMC038610-Q1 in our factories, which can save you manufacturing time and costs.

These devices can also help increase system efficiency through improved accuracy. The integrated divider features very low temperature and lifetime drift compared to discrete resistors, enabling voltage measurements with an accuracy <1%.

For more information on integrated resistor devices, see the application note, **Increased Accuracy and Performance with Integrated High Voltage Resistor Isolated Amplifiers and Modulators**.

Single-ended output devices

When designing isolated voltage-sensing circuits with industry-standard isolated amplifiers such as the AMC1311, a common challenge is converting the differential output of the isolated amplifier to single ended in order to interface directly with the analog-to-digital converter (ADC) inside the microcontroller (MCU). This can be costly and consume extra PCB space.

To conserve board space, the **AMC0311R-Q1**, **AMC0311S-Q1**, **AMC0330R-Q1** and **AMC0330S-Q1** devices help save system-level costs and reduce solution size by removing the need for a differential- to single-ended conversion circuit, which typically consists of an operational amplifier and a reference voltage (see **Figure 32**).

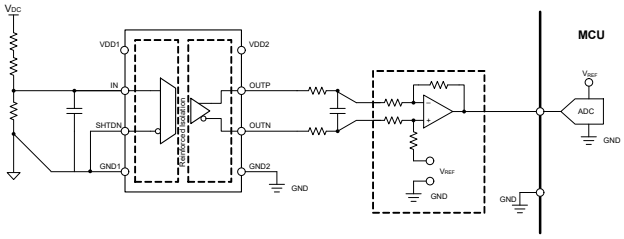


Figure 32. *Traditional isolated voltage-sensing topology.*

Figure 33 shows the pinout of these single-ended devices.

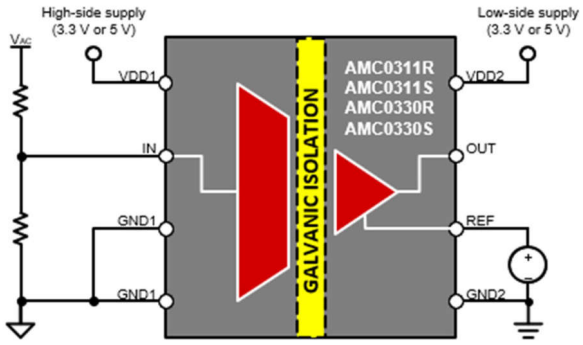


Figure 33. *Integration of the differential- to single-ended operational amplifier.*

Along with the board space savings that come with the AMC0311R-Q1 and AMC0330R-Q1 devices, their ratiometric output enables a variable output gain, providing an output swing from the isolated voltage-sensing device that follows the reference voltage of the ADC inside the MCU, as shown in **Figure 34**. This enables the use of the ADC's full dynamic range for improved resolution measurements.

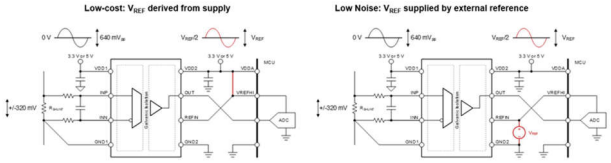


Figure 34. *Ratiometric output isolated voltage sensing.*

For more information on integrated resistor devices, see the application note, **Isolated Amplifiers with Differential, Single-Ended Fixed Gain and Ratiometric Outputs for Voltage Sensing Applications**.

Integrated isolated voltage-sensing use cases

Figure 35 shows the standard topology of a power-conversion system. For AC voltage sensing, you can use the AMC0380D04-Q1 without external high-voltage resistors (the green rectangle) or the AMC0330D-Q1, AMC0330S-Q1 or AMC0330R-Q1 with external high-voltage resistors (the yellow rectangle).

For DC voltage sensing, you can use the AMC0381D10-Q1 and AMC0386M10-Q1 without external high-voltage resistors (the blue rectangles) or the AMC0311D-Q1, AMC0311S-Q1 or AMC0311R-Q1 with external high-voltage resistors (the red rectangles).

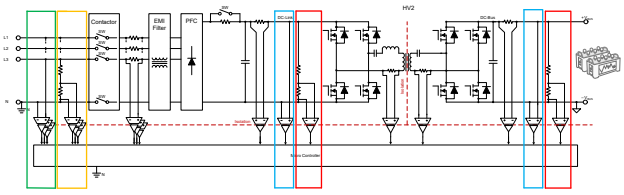


Figure 35. *Isolated voltage sensing in power-conversion applications.*

Figure 36 shows the standard topology of a motor-control system. For AC voltage sensing, you can use the AMC0380D04-Q1 without external high-voltage resistors (the green rectangle) or the AMC0330D-Q1, AMC0330S-Q1 or AMC0330R-Q1 with external high voltage resistors (the yellow rectangle).

For DC voltage sensing, you can use the AMC0381D10-Q1 and AMC0386M10-Q1 without external high-voltage resistors (the blue rectangle) or the AMC0311D-Q1, AMC0311S-Q1 or AMC0311R-Q1 with external high-voltage resistors (the red rectangle).

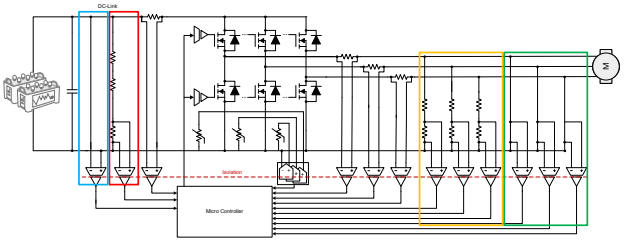


Figure 36. *Isolated voltage sensing in motor-control applications.*

Conclusion

Small, efficient, accurate and cost-effective power converters and motor controllers are a necessity in today's market. The AMC0380D04-Q1, AMC0386M10-Q1, AMC0330D-Q1, AMC0330S-Q1 and AMC0330R-Q1 devices for AC voltage sensing and the AMC0381D-Q1, AMC038610-Q1, AMC0311D-Q1, AMC0311S-Q1 and AMC0311R-Q1 devices for DC voltage sensing address design challenges to help realize the goal of a net-zero emissions future.

Additional resources

- Check out the updated reference designs with high-voltage sensing products:
  - 800V, 300kW SiC-based traction inverter system reference design (download the **TIDM-02014**)
  - 10-kW, bidirectional three-phase three-level (T-type) inverter and PFC reference design (download the **TIDA-01606**)
- Get started designing by ordering the **AMC038XEVM** evaluation module and **DIYAMC-0-EVM** evaluation modules.
- Learn more about TI's **voltage sensing solutions**.

Increased Accuracy and Performance with Integrated High Voltage Resistor Isolated Amplifiers and Modulators

Abstract

This application note introduces the new AMC038x devices, galvanically isolated amplifiers and modulators with integrated resistive dividers for high-voltage sensing, and highlights the benefits and common use cases.

Introduction

As high voltage automotive and industrial designs evolve, the need for precise, safe, and power-efficient galvanically isolated voltage sensing designs intensify. The AMC038x product family is a group of isolated amplifiers and modulators with increased accuracy, enhanced integration, and greater functionality that can meet these requirements. Designed with integrated high voltage (HV) resistors, these devices are a significantly reduced design size contrasted to the conventional design using an external resistive divider. External high voltage resistive dividers can be large and costly to step the voltage down to a 1V or 2V level. Furthermore, the integrated resistors have very low temperature and lifetime drift in comparison to discrete resistors. This allows the AMC038x products to achieve better than 1% accuracy over temperature and lifetime without the need for calibration.

High Voltage Resistor Isolated Amplifiers and Modulators Advantages

The AMC038x product family provides many benefits over the standard 2V input with external resistor divider voltage sensing devices, including improved accuracy and reduced board space.

Space Savings

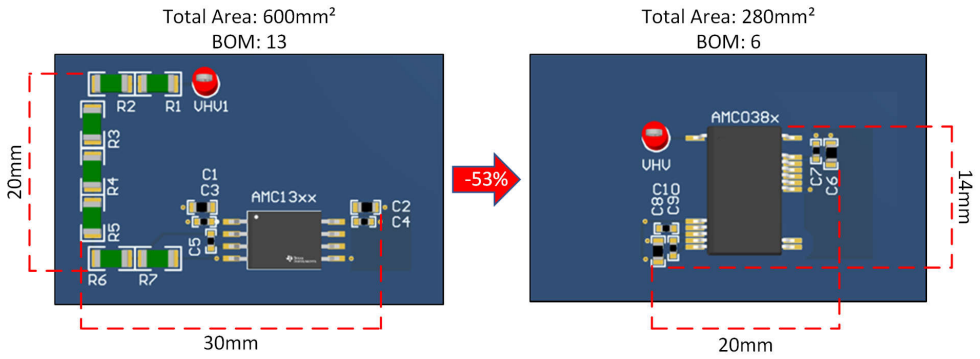


Figure 37. *Board Space Savings*

Current discrete high voltage resistors can consume a significant portion of space on PCB. Typically, voltage drops across a single resistor are limited by manufacturers and customers prefer using smaller footprint resistors due to board-level reliability concerns. Given this, a system can need as many as 15 HV resistors to step down the voltage and maintain the system's isolation ratings. By contrast, the AMC038x product family integrates HV resistors into the device which equates to a simpler, smaller design. This offers 8mm creepage and clearance distance between the HV input and the next closest pin. As demonstrated in **Figure 37**, this is a design size reduction of over 50% and decreases the BOM count significantly.

Improved Temperature and Lifetime Drift of Integrated HV Resistors

Along with space saving benefits, the integration of the HV resistive divider also increases accuracy. Previous designs with external resistors have higher temperature and lifetime drifts; the elimination of external resistors eliminates a

majority of the total error. More specifically, the temperature drifts of external resistors can drift apart, compounding over time. Ordinarily, external resistor dividers use HV resistors in the upper part of the divider and low voltage (LV) resistors in the lower part of the divider. These LV resistors are frequently of a different type, construction, or material. An integrated resistive divider uses the same material for both the upper and lower resistors, which results in a very low temperature coefficient. Any remaining error of the resistive divider is then calibrated out at production, practically eliminating the resistive divider error entirely. Consider the following example:

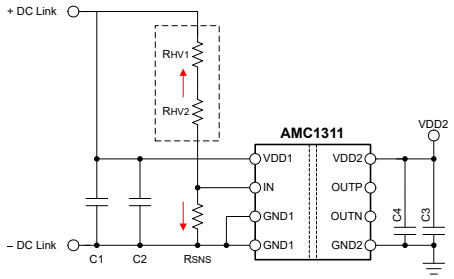


Figure 38. *External Resistor Design*

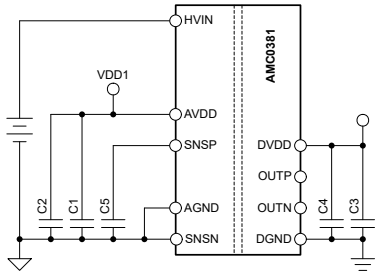


Figure 39. *Integrated Resistor Design*

External Resistor Worst Case Drift Error:

$$50ppm/°C(R_{HV1}/R_{HV2}) - (-50ppm/°C)(R_{SNS}) + 40ppm/°C(AMC1311\,Gain\,Error\,Drift) = 140ppm/°C \quad (10)$$

$$Drift\ Error\ over\ Temperature\ \% = 140ppm/°C \times 100°C = 1.4\,\% \quad (11)$$

Integrated Resistor Worst Case Drift Error:

$$40ppm/°C(AMC0381\,Gain\,Error\,Drift) \quad (12)$$

$$Drift\ Error\ over\ Temperature\ \% = 40ppm/°C \times 100°C = 0.4\,\% \quad (13)$$

As the external resistors can shift in opposite directions, this amounts to over 2/3 of the total signal chain error; an additional 1%. This makes it challenging for external resistor designs to achieve <1% accuracy over temperature and lifetime unlike the HV integrated resistor products.

Accuracy Results

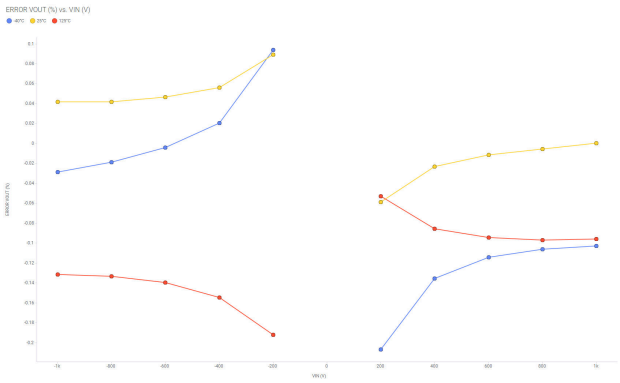


Figure 40. *Total Output Referred Error Percentage vs. Input Voltage*

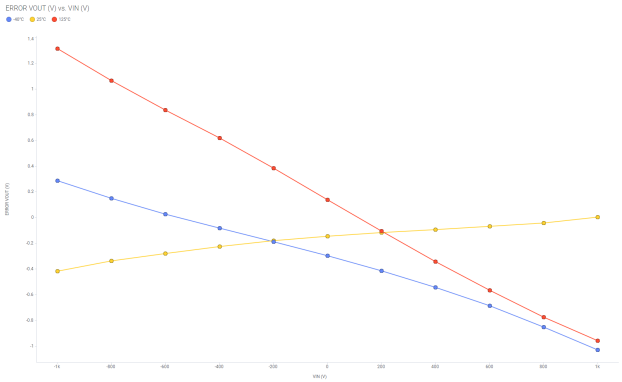


Figure 41. *Total Output Referred Error Voltage vs. Input Voltage*

To illustrate, **Figure 40** and **Figure 41** show the typical accuracy of the AMC038x devices over temperature. The figures show that the AMC038x delivers better than 0.4% accuracy above 100V and that 0.5V absolute error below 100V input can be achieved over temperature without system level calibration. Saving the calibration routine reduces production cost in implementing precise voltage measuring applications.

Figure 42. *AMC038x Thermal Results: 12.5MΩ*

Additionally, the AMC0381D10 thermal results demonstrate the steady performance of the device family at very high voltages. At 1000V, the θ JA thermal resistance of the package is 107°C/W and expects a temperature increase of 8°C which matches well with lab measurements. This is more than tolerable and confirms safe performance also at elevated ambient temperatures.

Fully Integrated Resistors vs. Additional External Resistor Example

Accurate voltage measurement and performance over temperature is crucial in **onboard charger** (OBC) applications. Achieving full state of charge on the battery is necessary for the battery to fully charge after years of use. Ergo, increased accuracy and low lifetime drift directly contribute to the continued success of these systems. These principles can extend to other **HEV**, **Energy Infrastructure**, and **Motor Drive** applications as well.

Some applications can alternatively consider including an external resistor to manually adjust the gain of the internal resistor divider. This is feasible; however, the caveat is reintroducing temperature drift and gain error that is virtually foregone when using integrated resistor devices. With integrated resistors, the gain drift of the HV and LV resistors can drift in the same direction and remain stable over temperature, effectively going unmeasured. When introducing an external resistor, R_{EXT}, the gain drift of the internal resistors and R_{EXT} can shift in opposite directions in the worst case and add secondary error to the system. For example, if a user wanted to sense 1200V on a 1000V device, the user can consider the following demonstration:

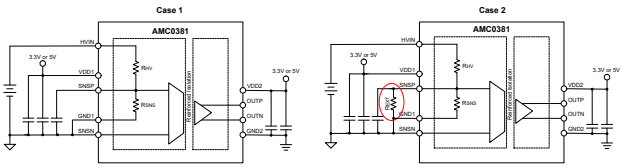


Figure 43. *Gain Error Resistor Divider Variation Schematics*

Case 1: Sensing 1000V on a 1000V Device (AMC0381R10):

For 1000V Devices: R_{HV} = 12.5MΩ; R_{SNS} = 12.5kΩ

Integrated resistors have a tolerance of ±20%. Both the HV and LV resistors, R_{HV} and R_{SNS}, drift in the same direction.

Nominal Resistor Divider Voltage at SNSP Pin:

$$V_{NOM} = V_{PEAK} \times \frac{R_{SNS}}{R_{HV} + R_{SNS}} \quad (14)$$

$$V_{NOM} = 1000V \times \frac{12.5k\Omega}{12.5M\Omega + 12.5k\Omega} = 0.999V \quad (15)$$

Maximum Resistor Divider Voltage at SNSP Pin:

$$V_{MAX} = V_{PEAK} \times \frac{R_{SNS} + 20\,\%}{R_{HV} + 20\,\% + R_{SNS} + 20\,\%} \quad (16)$$

$$V_{MAX} = 1000V \times \frac{15.0k\Omega}{15.0M\Omega + 15.0k\Omega} = 0.999V \quad (17)$$

Gain Error Output Referred:

$$V_{GAIN\ ERROR\ OUTPUT} = (V_{MAX} - V_{NOM}) \times V_{OUTPUT} \quad (18)$$

$$V_{GAIN\ ERROR\ OUTPUT} = (0.999V - 0.999V) \times 2V = 0V \quad (19)$$

$$Gain\ \ Error\ \ \% = \frac{V_{MAX} - V_{NOM}}{V_{NOM}} \times 100 \quad (20)$$

$$Gain\ \ Error\ \ \% = \frac{0.999V - 0.999V}{0.999V} \times 100 = \mathbf{0\,\%} \quad (21)$$

Not maximizing full scale input range can result in the offset error contributing to a larger portion of the full scale error. Please refer to the **isolated voltage sensing calculator** for more information.

Case 2: Sensing 1200V using a 1000V Device (AMC0381R10):

For 1000V Devices: R_{HV} = 12.5MΩ; R_{SNS} = 12.5kΩ

This design requires including an external resistor, R_{EXT}, from SNSP to AGND. This can introduce secondary error to the system and is unadvised. The absolute maximum ratings of the device must not be exceeded.

$$\frac{R_{EXT} \parallel 12.5k\Omega}{12.5M\Omega + R_{EXT} \parallel 12.5k\Omega} = \frac{1}{1200} \quad (22)$$

$$R_{EXT} = 62.8k\Omega \quad (23)$$

Integrated resistors have a tolerance of ±20% and external resistors have a tolerance of 0.1%. In the worst case scenario, R_{EXT} can drift in the opposite direction of R_{HV} and R_{SNS}.

Nominal Resistor Divider Voltage with External Resistor at SNSP Pin:

$$V_{NOM} = V_{PEAK} \times \frac{R_{SNS} \parallel R_{EXT}}{R_{HV} + R_{SNS} \parallel R_{EXT}} \quad (24)$$

$$R_{SNS} \parallel R_{EXT} = \frac{12.5k\Omega \times 62.8k\Omega}{12.5k\Omega + 62.8k\Omega} = 10.4k\Omega \quad (25)$$

$$V_{NOM} = 1200V \times \frac{10.4k\Omega}{12.5M\Omega + 10.4k\Omega} = 1.00V \quad (26)$$

Maximum Resistor Divider Voltage with External Resistor at SNSP Pin:

$$V_{MAX} = V_{PEAK} \times \frac{R_{SNS-20\,\%} \parallel R_{EXT+0.1\,\%}}{R_{HV-20\,\%} + R_{SNS-20\,\%} \parallel R_{EXT+0.1\,\%}} \quad (27)$$

$$R_{SNS-20\,\%} \parallel R_{EXT+0.1\,\%} = \frac{10.0k\Omega \times 62.9k\Omega}{10.0k\Omega + 62.9k\Omega} = 8.63k\Omega \quad (28)$$

$$V_{MAX} = 1200V \times \frac{8.63k\Omega}{10.0M\Omega + 8.63k\Omega} = 1.03V \quad (29)$$

Gain Error Output Referred:

$$V_{GAIN\ ERROR\ OUTPUT} = (1.03V - 1.00V) \times 2V = 0.069V \quad (30)$$

$$Gain\ \ Error\ \ \% = \frac{1.03V - 1.00V}{1.00V} \times 100 = \mathbf{3.44\,\%} \quad (31)$$

Using the integrated resistor devices as is does not incorporate any measurable gain drift. Adding an external resistor to manually adjust the gain of these devices can introduce an additional worst case scenario gain drift error of 3.44% to the total system error and is therefore not recommended.

Device Selection Tree and AC/DC Common Use Cases

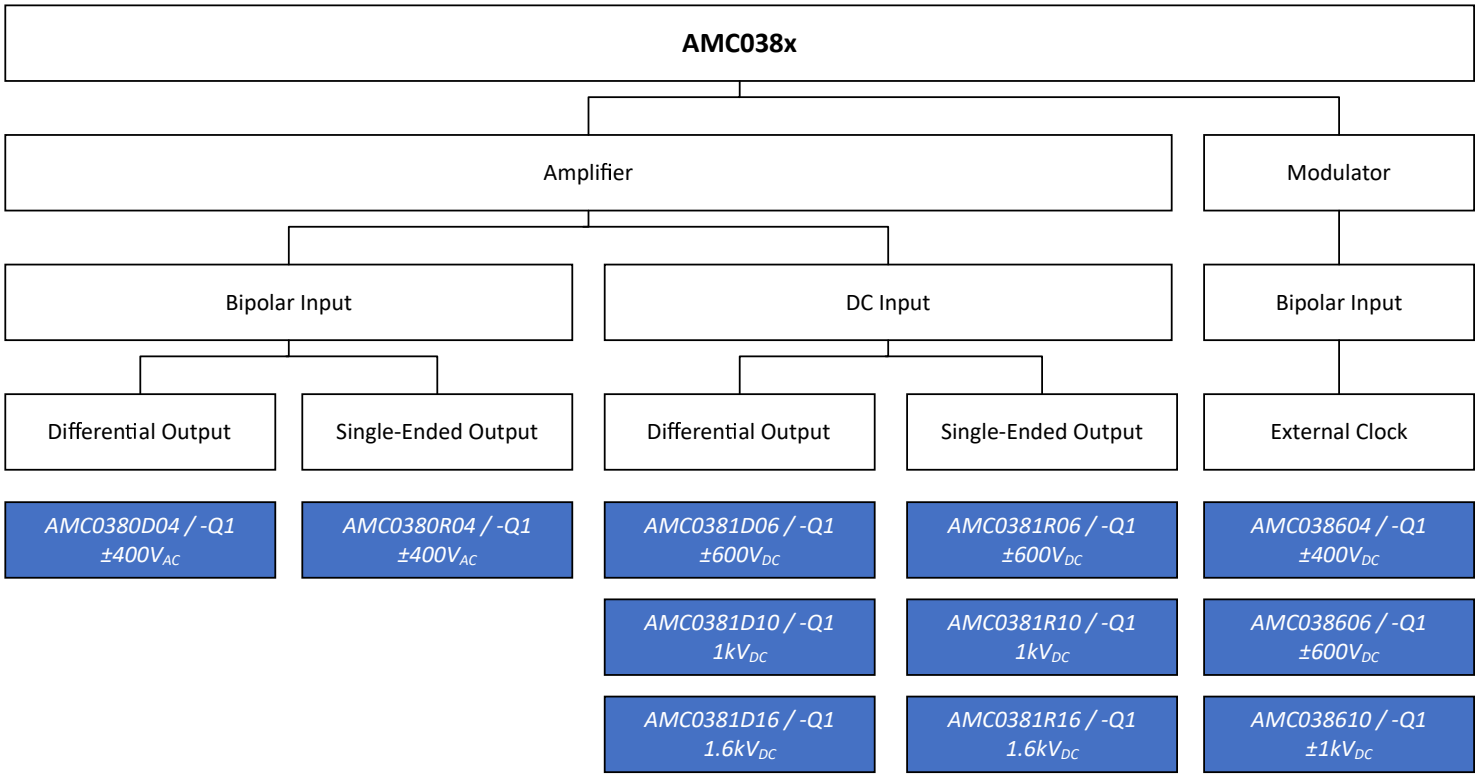


Figure 44. *AMC038x Selection Tree*

Table 6. AC Voltage Sensing Use Cases

Use Case	Nominal Voltage Range	Recommended Divider Ratio
Phase-to-Neutral AC Line Voltage Sensing	$120V_{RMS}$ (±10%) / $190V_{PK}$	400:1
	$230V_{RMS}$ (±10%) / $360V_{PK}$	400:1
Phase-to-Phase AC Line Voltage Sensing	$400V_{RMS}$ (±10%) / $620V_{PK}$	600:1
	$690V_{RMS}$ (±10%) / $1070V_{PK}$	1000:1

Table 7. DC Voltage Sensing Use Cases

Use Case	Nominal Voltage Range	Recommended Divider Ratio
DC Link derived from Single Phase $120V_{AC}$	Up to 400V + 10%	400:1
DC Link derived from Single Phase $230V_{AC}$	Up to 600V + 10%	600:1
DC Link derived from 3-Phase $230/400V_{AC}$	Up to 1000V + 10%	1000:1
ESS / Solar Applications with 1500V+ String Voltage	Up to 1600V + 10%	1600:1

The AM038x devices come with four fixed ratio options allowing for four different input voltage ranges: 400V, 600V, 1000V, and 1600V. These devices also come with three different output types: differential analog output, single-ended analog output, and digital bit stream modulator output. The devices support AC voltage sensing with the bipolar input option and DC voltage sensing with the DC input option. For more information on specific application cases, please see ***Maximizing Power Conversion and Motor Control Efficiency With Isolated Voltage Sensing***, marketing white paper.

Summary

With reduced size, increased accuracy, and easy integration, the AMC038x product family is a potent design for a variety of applications. The integrated high voltage resistor enables industry leading accuracy of <1%, a 50% smaller PCB design size, and removes the need for end of line calibrations. Such improvements bolster the ability of these isolated amplifiers and modulators to be well suited for HEV, energy infrastructure, and motor drive applications.

References

- Texas Instruments, ***AMC038XEVM Evaluation board***.
- Texas Instruments, ***Maximizing Power Conversion and Motor Control Efficiency With Isolated Voltage Sensing***, marketing white paper.
- Texas Instruments, ***Addressing High-Volt Design Challenges w/ Reliable and Affordable Isolation Tech (Rev. C)***, marketing white paper.
- Texas Instruments, ***Isolated Voltage Sensing in AC Motor Drives***, analog design journal.
- Texas Instruments, ***SBAR013 Isolated Amplifier Voltage Sensing Excel Calculator***.

Isolated Amplifiers With Differential, Single-Ended Fixed Gain and Ratiometric Outputs for Voltage Sensing Applications

Abstract

Texas Instruments introduces the AMC0xxxD/S/R product family, a new portfolio of isolated AC and DC voltage sensing amplifiers with options of a differential output, single-ended fixed gain output, and single-ended ratiometric output.

Introduction

Several automotive systems and industrial systems operate at high voltages in harsh environments, making high-performance isolated voltage sensing designs critical for maintaining system efficiency and long-term reliability. Selecting the correct isolated amplifier requires many considerations, such as system accuracy, PCB space, and cost for the system that the device is being implemented into. To design systems with improved accuracy at a reduced design size and cost, while still meeting performance requirements, Texas Instruments introduces the AMC0xxxD/S/R product family, a new portfolio of isolated AC and DC voltage sensing amplifiers with options of a differential output, single-ended fixed gain and ratiometric output.

Overview of Differential, Single-Ended Fixed Gain and Ratiometric Outputs

Isolated Amplifiers with Differential Output

Differential output amplifiers are widely desired in systems requiring high accuracy, noise immunity, and designed for signal integrity. The differential output amplifier provides two outputs: a positive and a negative output that are equal in magnitudes but opposite in phase. With two equally balanced output signals, the differential output amplifier has the ability to handle ground shifts without signal degradation, making the differential output amplifier designed for high-precision and performance applications. Because of the amplifier's insensitivity to ground shifts, these devices enable routing for the output signal over long distances while still maintaining signal integrity.

There are a few design considerations with a differential output amplifier. One of these considerations is PCB layout. Having poor PCB layout can compromise the amplifier’s ability to maintain an accurate common-mode output voltage. Since differential amplifiers rely on both the inverting and non-inverting paths, maintaining symmetry by making sure equal PCB trace lengths for both output lines is essential for minimizing output errors. There are different design options for configuring the differential output amplifier to an analog-to-digital converter (ADC). Option one, as shown in **Figure 45**, is a configuration that directly interfaces the differential output amplifier to a differential input ADC. However, processors such as the MSP430 and the C2000 have embedded single-ended input ADC. This consideration creates the need to convert from the differential signal to a single-ended signal to interface directly with the ADC. The best design for outputting to single-ended input ADC has been the conversion of the differential to single-ended output, as shown as Option 2 in **Figure 45**.

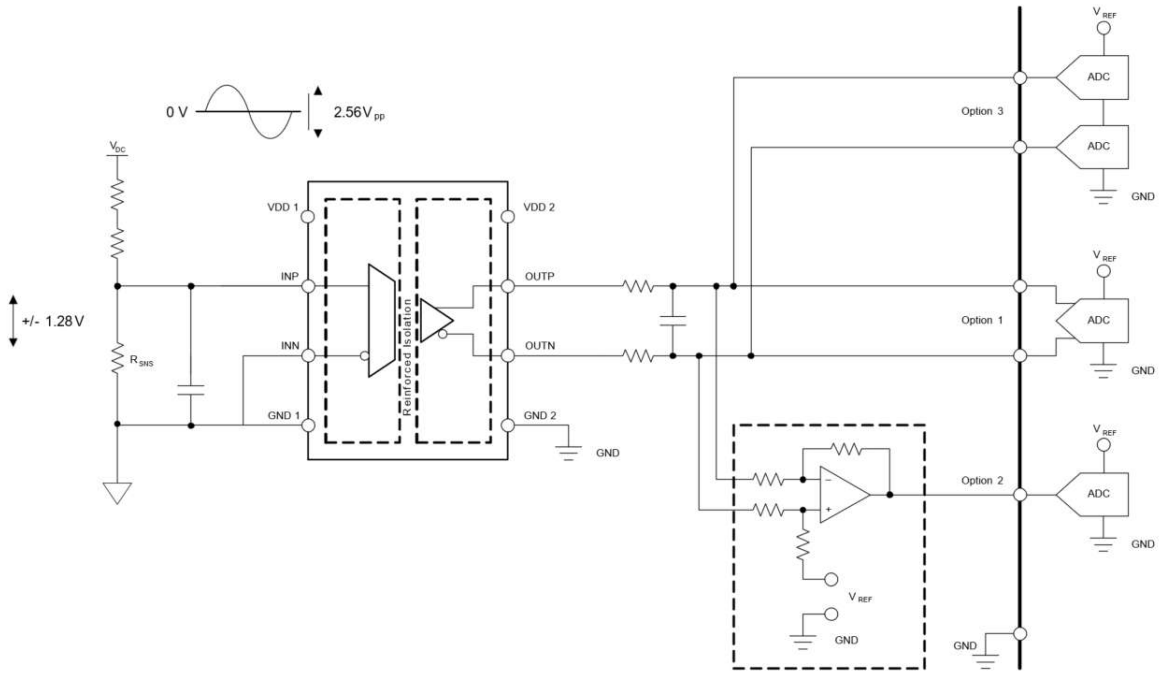


Figure 45. *Differential Output Configuration*

This configuration introduces an additional amplifier, which allows for the conversion of a differential signal to a single-ended signal that outputs directly to the ADC. For more information about interfacing a differential to single-ended output stage, see, ***Isolated Current-Sensing Circuit With ±250-mV Input Range and Single-Ended Output Voltage***, analog engineer's circuit. Another design is using two single-ended input ADC and subtracting the values in the MCU, as shown as Option 3 in **Figure 45**. However, Option 3 has the drawback of compound error and the need for an extra ADC, which makes this option less attractive.

Isolated Amplifiers With Single-Ended, Fixed-Gain Output

The new product family offers alternative devices for compact designs that do not benefit from the differential output. The differences between a differential and single-ended output amplifier can be summarized primarily by how these amplifiers handle noise, output signals, and the design characteristics. The new device family introduces two options of single-ended amplifiers: the single-ended amplifier with fixed gain and the single-ended amplifier with ratiometric gain.

The single-ended fixed gain amplifier is widely desired due to the ease of use and cost-effectiveness. The single ended fixed gain amplifier can output a single-ended signal that is proportional to the input voltage of the amplifier. As this device was designed to interface directly with a single-ended input ADC, the additional differential to single-ended amplifier conversion stage, as previously referenced in **Figure 45**, is no longer necessary. Therefore, this design requires less components which enables a smaller design size and lower BOM cost, making this device designed for compact systems.

One design consideration for the single-ended fixed gain devices is the device's ground noise sensitivity. Fluctuations to the ground potential can bring distortions to the output signal by introducing noise or error to the signal, which can be eliminated with proper grounding and component selection. If not considered, this can potentially decrease your signal to noise ratio and decrease overall performance. Another design consideration is the voltage applied to the reference (REFIN) pin of the device - the pinout of the device is shown in **Figure 48** . **Figure 46** shows the input-to-output transfer

characteristic for the AMC0x11S device, which is the single-ended fixed gain output device that has an input voltage range of 0-2.25V.

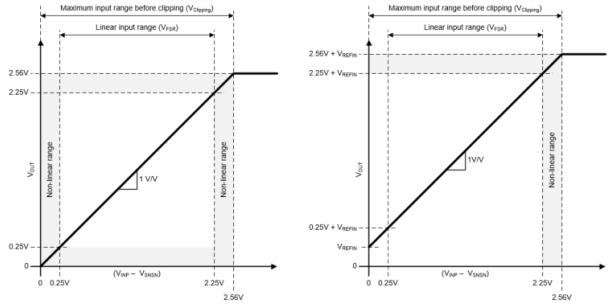


Figure 46. *Input-to-output Transfer Characteristic for AMC0x11S*

The left image shows the case in which REFIN is shorted to GND2. The right image shows when V_{REFIN} = 250mV. Supplying a voltage to REFIN that is ≥250mV extends the linear input voltage range to 0V. The output buffer requires a minimum headroom of 250mV for linear operation. Therefore, with REFIN shorted to GND2, the device shows non-linear behavior for input voltages near 0V. The equation for the output voltage of AMC0x11S device is:

Output Voltage of AMC0x11S:

$$V_{OUT} = (V_{INP} - V_{SNSN}) + V_{REFIN}. \quad (32)$$

For the AMC0x30S device, which is the single-ended, fixed gain device that has an input voltage range of ±1V, the output is directly proportional to the input voltage (V_{IN}), where REFIN is referred to GND2. The output can be defined by the following equation:

Output Voltage of AMC0x30S:

$$V_{OUT} = (V_{INP} - V_{SNSN}) + V_{REFIN}. \quad (33)$$

Figure 47 shows the input-to-output transfer characteristic for the AMC0x30S device. For input voltages below –1V and above +1V, the output of the device continues to follow the input but with reduced linearity performance.

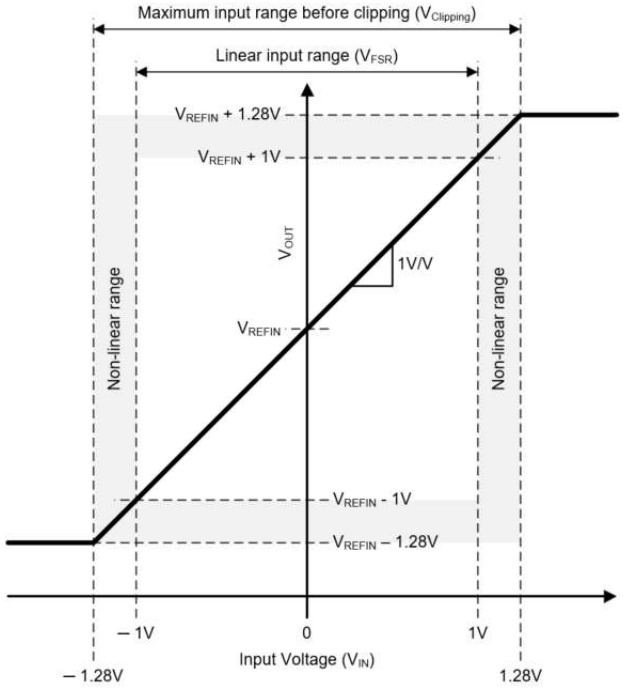


Figure 47. *Input-to-output Transfer Characteristic for AMC0x30S*

Isolated Amplifiers With Single-Ended, Ratiometric Output

To provide a comprehensive portfolio of devices that covers the need for high performance, cost-efficient, and smaller system sizes, the new product family includes options of single-ended devices with a ratiometric output. The single-ended ratiometric output devices of the new product family are designed to adjust the gain in proportion to the reference voltage of the ADC. One disadvantage of the fixed gain output is that the fixed gain can only provide a 2V output swing. Systems with a 5V analog IO can only use 50% of the ADC input range, therefore losing 1 bit of resolution on the measurement. The ratiometric output makes sure that the amplifier fully utilizes the ADC dynamic range, thereby maximizing the resolution of the measurement. **Figure 48** and **Figure 49** refer to two different configurations for the ratiometric devices:

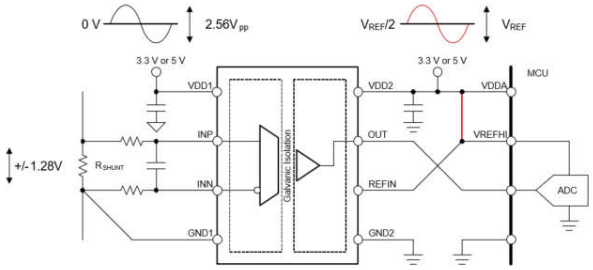


Figure 48. *REF Derived from Supply*

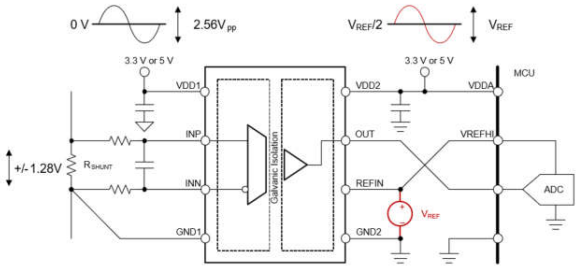


Figure 49. *REF Supplied by External Reference*

Having the reference voltage derived from the power supply rail can contribute to lower costs, as there can be less components involved. However, having the reference voltage derived from an external reference can lead to lower noise.

The design of the single-ended ratiometric output device makes the device insensitive to the value of the reference voltage and tolerant of inaccuracy and AC disturbance. Because of the device's ability to achieve increased resolution, accuracy and stability while eliminating the need for the additional differential to single-ended amplifier stage, the ratiometric option is desired greatly for the cost savings and ability to take up less PCB space and contribute to lower BOM cost, all while meeting performance specifications.

One design consideration for the single-ended, ratiometric device is the input voltage range of the ADC. Because the ratiometric devices can support 2.75-5.5V reference voltages, the ratiometric devices are best designed for ADC with an input voltage range of 3.3V and 5V. Another design consideration for this device is routing. Because the reference

voltage of both the ADC and the amplifier are proportional, the reference voltage of the ADC needs to be routed to the ratiometric device.

Figure 50 shows the input-to-output transfer characteristics for the AMC0x30R, which is the single-ended, ratiometric gain device that has an input voltage range of ±1V. The bipolar input device can output 50% of V_{REF} at V_{IN} = 0 due to the amplifier being biased around the midpoint of the reference voltage

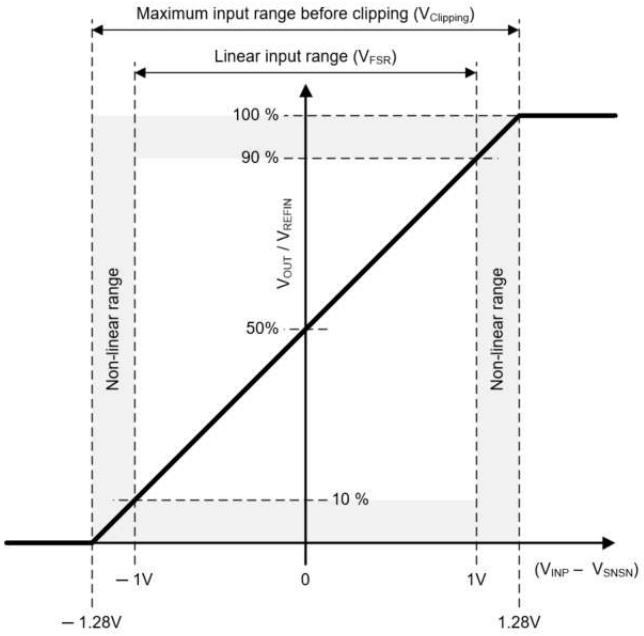


Figure 50. *Input-to-Output Transfer Characteristic for AMC0x30R*

For any input voltage within the specified linear input range, the device outputs a voltage can be defined by the following equation:

Output Voltage of AMC0x30R:

$$V_{OUT} = ((V_{INP}-V_{SNSN}) / V_{Clipping}) \times V_{REFIN} / 2 + V_{REFIN} / 2. \quad (34)$$

For input voltages below –1V and above +1V, the output of device continues to follow the input but with reduced linearity performance.

The AMC0x11R, which is the single-ended, ratiometric device that has an input voltage range of 0.13-2.25V, has an output voltage that is defined by the following equation:

Output Voltage of AMC0x11R:

$$V_{OUT} = ((V_{INP}-V_{SNSN}) / V_{Clipping}) \times V_{REFIN}. \quad (35)$$

Similar to the AMC0x11S, the AMC0x11R device shows non-linear behavior for input voltages near 0V, is shown in **Figure 51**.

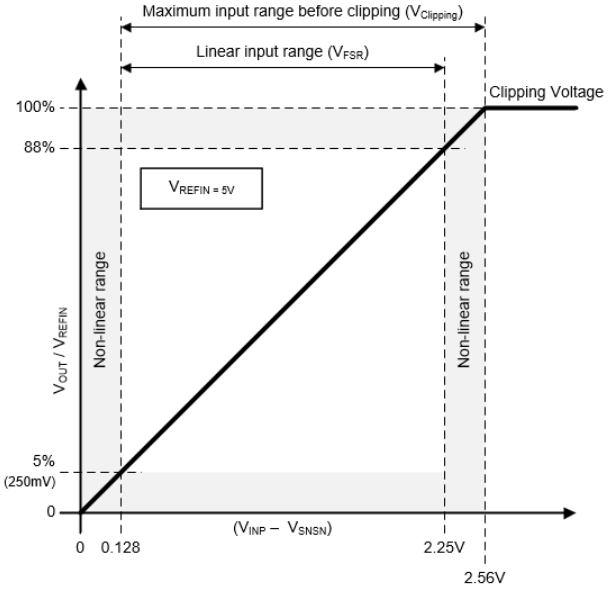


Figure 51. *Input-to-Output Transfer Characteristic for AMC0x11R*

At V_{REFIN}=5V, the minimum input voltage for linear operation is 128mV. The output is 5% of the reference, or 250mV.

The minimum input voltage for linear operation can be calculated using the following equation:

Minimum Input Voltage for Linear Operation for AMC0x11R:

$$V_{INP, MIN} = (250mV \times V_{Clipping}) / V_{REFIN}. \quad (36)$$

Application Examples

Product Selection Tree

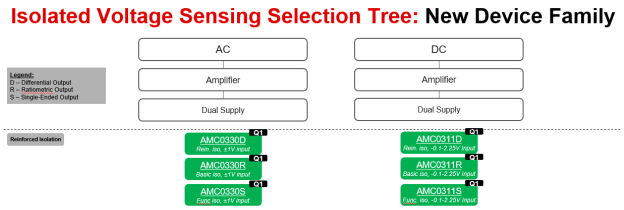


Figure 52. *Product Selection Tree*

The new product family of devices come with six options of reinforced isolated voltage sensing amplifiers, allowing for 0-2V input voltages range for DC applications and ±1V input voltage ranges for AC applications. The AMC0311D, AMC0311R, and AMC0311S devices support DC voltage sensing with the unipolar input option and the AMC0330D, AMC0330R, and AMC0330S devices support AC voltage sensing with the bipolar input option, as showcased in **Figure 52**. For more information on specific application cases, including use cases for the AC and DC voltage sensing amplifiers in power conversion and motor control topologies, please see ***Maximizing Power Conversion and Motor Control Efficiency With Isolated Voltage Sensing***, marketing white paper.

Summary

There are many decisions to consider when selecting an isolated amplifier for voltage sensing applications. The devices in the new product family are designed to improve accuracy at a reduced design size and cost with the options of a differential output and single-ended output amplifiers.

References

- Texas Instruments, ***DIYAMC-0-EVM Universal do-it-yourself (DIY) isolated amplifier and modulator evaluation module***.
- Texas Instruments, ***Isolated Current-Sensing Circuit With ±250-mV Input Range and Single-Ended Output Voltage***, analog engineer's circuit.
- Texas Instruments, **Maximizing Power Conversion and Motor Control Efficiency With Isolated Voltage Sensing**, marketing white paper.
- Texas Instruments, ***Addressing High-Voltage Design Challenges With Reliable and Affordable Isolation Technologies***, marketing white paper.

Isolated Voltage-Measurement Circuit With ±250-mV Input and Differential Output

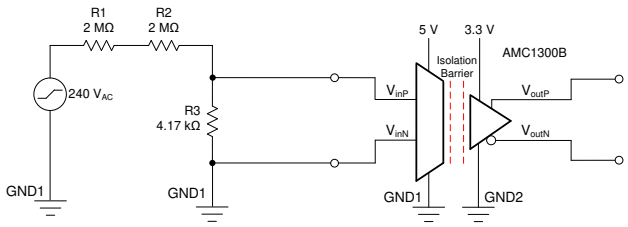
Design Goals

Voltage Source		AMC1300B Input Voltage		AMC1300B Output Voltage (1.44V_{CM})		Power Supplies	
V_{MAX}	V_{MIN}	$V_{IN\ DIFF,\ MAX}$	$V_{IN\ DIFF,\ MIN}$	$V_{OUT\ DIFF,\ MAX}$	$V_{OUT\ DIFF,\ MIN}$	VDD1	VDD2
+240V	–240V	+250mV	–250mV	+2.05V	–2.05V	3.0V–5.5V	3.0V–5.5V

Design Description I

This circuit performs a high-voltage, differential measurement using a voltage divider and a ±250-mV differential input, differential output, **AMC1300B** isolated amplifier. Because it is a low-input impedance device, the **AMC1300B** is better suited for current sensing applications. The interaction of the input impedance of the isolated amplifier and the input voltage divider introduces a gain error. Additionally, bias current passing out of the low-impedance inputs and through the voltage sense resistor causes a significant offset error. We will first design without compensating for these errors. Then, we will observe their effects and describe them mathematically. Finally, we will redesign to limit their effects and observe the improved results.

The voltage-divider circuit reduces the input voltage from ±240V to ±250mV so as to match the input range of the isolation amplifier. The **AMC1300B** requires both high- and low-side power supplies. The high-side supply will often be generated using a floating supply or from the low side using an isolated transformer or isolated DC/DC converter. The **AMC1300B** can measure differential signals of ±250mV with a fixed gain of 8.2V/V and output an isolated differential output voltage of ±2.05V with an output common-mode voltage of 1.44V. The differential output voltage can be scaled as necessary using an additional operational amplifier, as shown in ***Interfacing a Differential-Output (Isolated) Amplifier to a Single-Ended Input ADC Tech Note*** with the TLV6001 device, to interface with an ADC.



Design Notes I

1. Verify that the isolation amplifier will remain in its linear region of operation for the desired input signal range. This can be achieved using a DC sweep simulation as demonstrated in the ***DC Transfer Characteristics I*** section.
2. Ensure the resistors used in the resistor divider circuit (R1–R3) are capable of dissipating the power supplied from the voltage source.
3. Check that the input voltage applied to the device will remain within the range specified by the data sheet. Should the input range be violated, ensure that the input current remains below 10 mA to avoid damaging the part. If the system is susceptible to transient events, consider adding TVS diodes to the inputs.

Design Steps I

1. Calculate the required voltage divider attenuation based on the ratio of the input voltage source (V_{source}) to the full-scale input voltage of the **AMC1300B** ($V_{IN\_AMC\_FSR}$).

$$\mathrm{GaIn} = \frac{\mathrm{V_{IN\_AMC\_FSR}}}{\mathrm{V_{source}}} = \frac{250\mathrm{mV}}{240\mathrm{V}} = \frac{1}{960}\mathrm{V/V}$$

2. Select a resistance for the top portion of the voltage divider (R1 and R2). Note that power consumption is equal to I^2R and by Ohm's law, current and resistivity are inversely proportional. A linear increase in resistivity will lead to a linear decrease in power. For this reason, choosing large resistance values will minimize overall power consumption. These components dominate the power consumption of the voltage divider. So, select the value of Rtop to meet a peak power specification for the voltage divider.

$$\mathrm{Rtop} = \mathrm{R1} + \mathrm{R2}$$

$$\mathrm{P_{peak}} \leq 15\mathrm{mW}$$

$$P = I^2R = \frac{V^2}{R}, \quad P_{peak} = \frac{{V_{peak}}^2}{R}$$

$$\mathrm{Rtop} \geq \frac{{\mathrm{V_{peak}}}^2}{\mathrm{P_{peak}}} = \frac{(240)^2}{0.015} = 3.86\mathrm{M\Omega}$$

$$Rtop = 4M\Omega$$

3. Split the Rtop resistance value into multiple resistors to minimize the power rating required of each resistor.

$$\mathrm{R1} = \mathrm{R2} = 2\mathrm{M\Omega}$$

4. Next, assume the input resistance of the isolation amplifier is large. The input voltage seen by the part from the voltage source will be determined by the voltage divider effect created by Rtop with R3. Solve for R3.

$$\mathrm{V_{In}} = \mathrm{V_{source}}\left(\frac{\mathrm{R3}}{\mathrm{R3} + \mathrm{Rtop}}\right)$$

$$\frac{V_{In}}{V_{source}} = \frac{R3}{R3 + Rtop}$$

$$R3V_{In} + RtopV_{In} = R3V_{source}$$

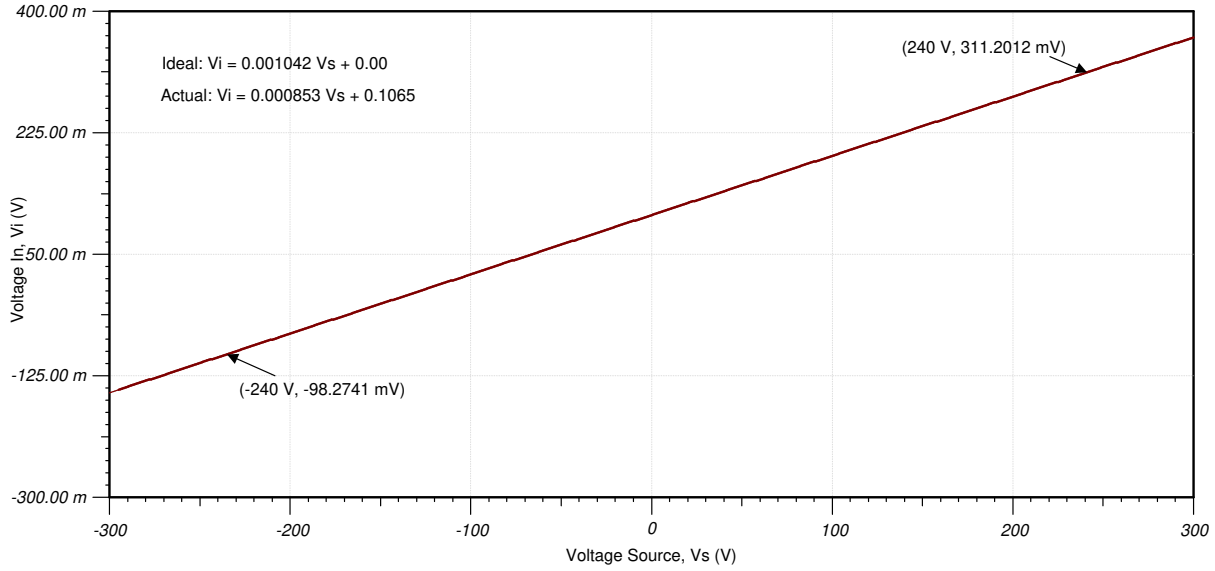
$$R_{top}V_{In} = R_3(V_{source} - V_{In})$$

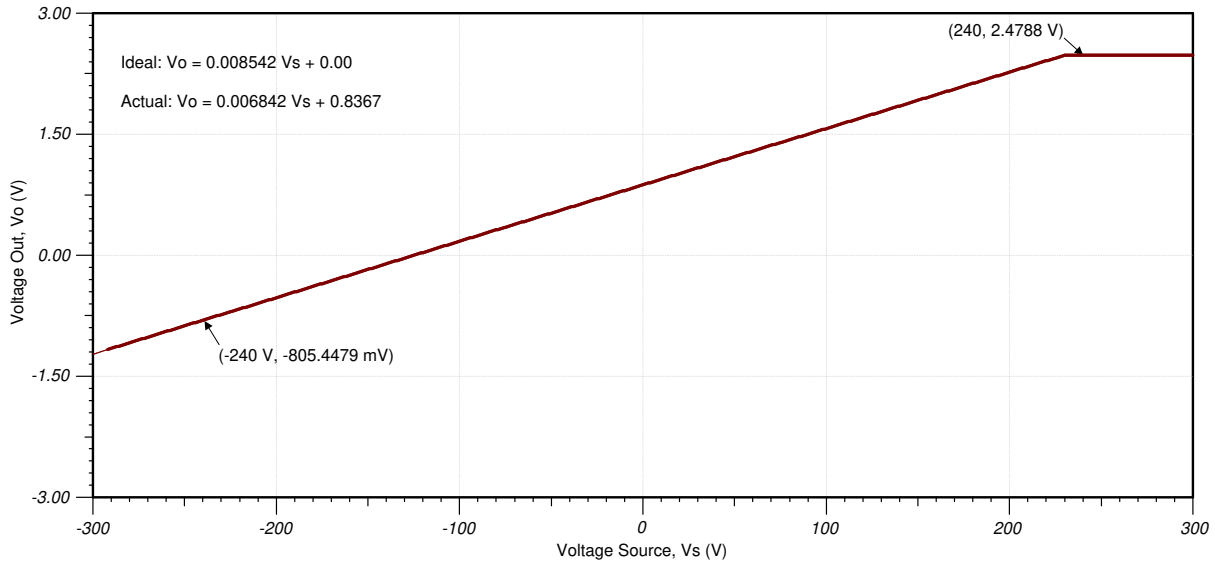
$$R3 = \frac{V_{In}Rtop}{V_{source} - V_{In}} = \frac{(250mV)(4M\Omega)}{240V - 250mV} \approx 4.17k\Omega$$

DC Transfer Characteristics I

The following graphs show the simulated output for a ±240V source. The source is swept from –300V to +300V and the input and output voltages of the amplifier are observed. The desired linear ranges are ±250mV at the input of the amplifier and ±2.05V at the output of the amplifier. At the input of the amplifier, we expect to see an offset error of 0 and a gain of about 1.042mV/V due to the voltage division of the voltage divider. At the output of the amplifier, we again expect to see an offset error of 0 and a gain of 8.542mV/V due to the attenuation of the voltage source of the voltage divider followed by the fixed 8.2V/V gain of the **AMC1300B**.

As can be seen in the following graphs , the simulated results do not match the desired, ideal output. At the input of the amplifier, an offset voltage error of 107mV is present. This is significant when compared to the ±250-mV input range of the part. This offset error is carried over to the output of the amplifier, where an 837-mV offset takes up a large portion of the ±2.05-V output range of the amplifier. The circuit also demonstrates a significant gain error. Despite expecting a gain of 1.042mV/V at the input from the voltage divider and 8.540mV/V at the output of the device, we instead observe gains of 0.853mV/V and 6.842mV/V, respectively, yielding large gain errors of approximately 18.1% and 19.9%. The following section will define better design practices.





Design Description II

The previous method is appropriate for voltage sensing applications when using devices with large input resistances, such as 1MΩ or greater. The **AMC1300B** device has a differential input impedance of 22kΩ which leads to the offset and gain errors shown previously. Gain and offset errors when using a low-input impedance amp for voltage sensing in this circuit configuration can be estimated using the following formulas.

$$\text{Gain Error } (\%) = \frac{R3}{R_{ind}} \times 100$$

$$\text{Offset Error } (V) = I_{bias} \times R3$$

The gain error is a result of a non-ideal voltage division by R3. Because the input resistance of the amplifier is comparable in size to R3, some of the current passing out of R1 and R2 will not pass through R3, but instead pass through the input of the amplifier. The result will be an unexpected voltage drop at the input of the amplifier. Consequently, the formula presented in **4** of the ***Design Steps I*** section will not be valid and a more complete formula that considers the input impedance of the amplifier being parallel to R3 must be considered. The offset error is the product of the bias current flowing out of the positive input pin of the isolated amplifier, through the shunt resistor, R3. This bias current across R3 can lead to significant offset voltages at the input that are then amplified and passed to the output.

Using the previous formulas allows one to estimate the errors of the circuit in the ***Design Steps I*** section. Using the typical data sheet values, the differential input resistance is 22kΩ and the input bias current is 30µA. Our designed value for R3 is 4.17kΩ and as a result one would expect to see a gain error of 18.7% and an offset error of 125mV at the input of the amplifier. In comparison, the simulated errors had a gain error of 19.9% at the output of the amplifier and 107mV of offset at the input. These error formulas serve as valuable tools to get a quick idea of the expected magnitude of the errors. Without needing to perform simulations, one can get an idea of whether or not the expected errors will be acceptable for the end use case.

As noted in the ***AMC1300 Precision, ±250-mV Input, Reinforced Isolated Amplifier Data Sheet***, for voltage sensing applications the introduction of R3' in series with the inverting terminal of the amplifier can reduce the offset and gain errors. The bias current of the amplifier will generate a similar offset at the negative input pin as at the positive input pin. This will greatly

reduce the magnitude of the overall offset voltage. Additionally, the effects of the input resistance of the amplifier and R3' will be taken into account when selecting the value of R3. This will provide a more ideal voltage division of the 240-V source and will improve the overall gain error.

Design Steps II - Consideration of R3'

As in ***Design Steps I*** , the Gain and Rtop resistance calculations are exactly the same, we are more interested in calculating R3 and R3' to provide the best circuit performance.

1. Note that the bottom portion of the resistor divider will set the input voltage range for the isolation amplifier. The ideal value for R3 is dependent on the gain, Rtop and Rind, where Rind is the differential input impedance of the amplifier. As a reminder, Rtop is the combination of R1 + R2.

$$\mathrm{R3} = \frac{\mathrm{Gain} \times \mathrm{Rtop}}{1 - \mathrm{Gain} - \left(\mathrm{Gain} \times \frac{2 \times \mathrm{Rtop}}{\mathrm{RInd}}\right)}$$

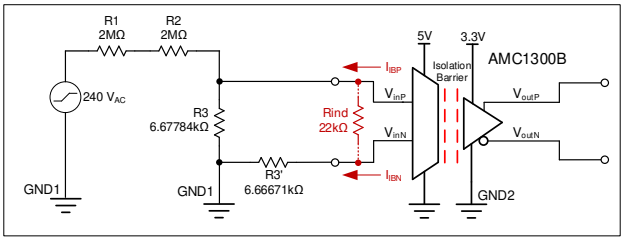
$$\mathrm{R3} = \frac{0.001042 \times 4\mathrm{M\Omega}}{1 - 0.001042 - \left(0.001042 \times \frac{8\mathrm{M\Omega}}{22.22\mathrm{k\Omega}}\right)} = 6.67784 \ \mathrm{k\Omega}$$

2. The purpose of R3’ is to cancel out the gain error introduced by the bias current flowing through R3. The ideal R3’ would be the parallel combination of Rtop and R3. Use the following equation to calculate R3’.

$$\mathrm{R3'} = \frac{\mathrm{Rtop} \times \mathrm{R3}}{\mathrm{Rtop} + \mathrm{R3}}$$

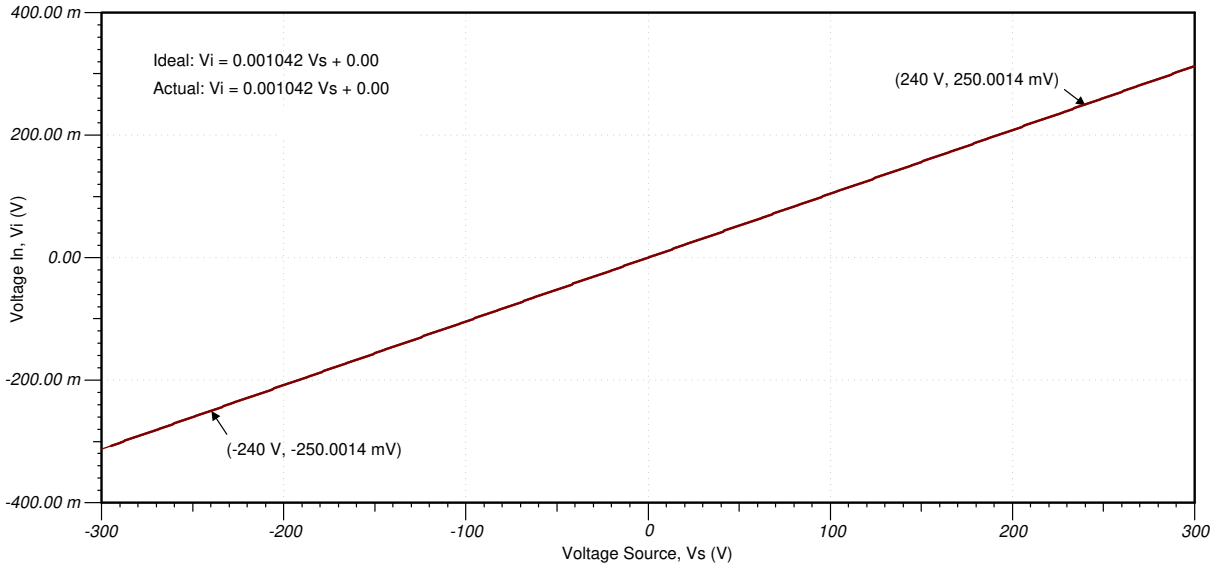
$$\mathrm{R3'} = \frac{4\mathrm{M\Omega} \times 6.67784\mathrm{k\Omega}}{4\mathrm{M\Omega} + 6.67784\mathrm{k\Omega}} = 6.66671 \ \mathrm{k\Omega}$$

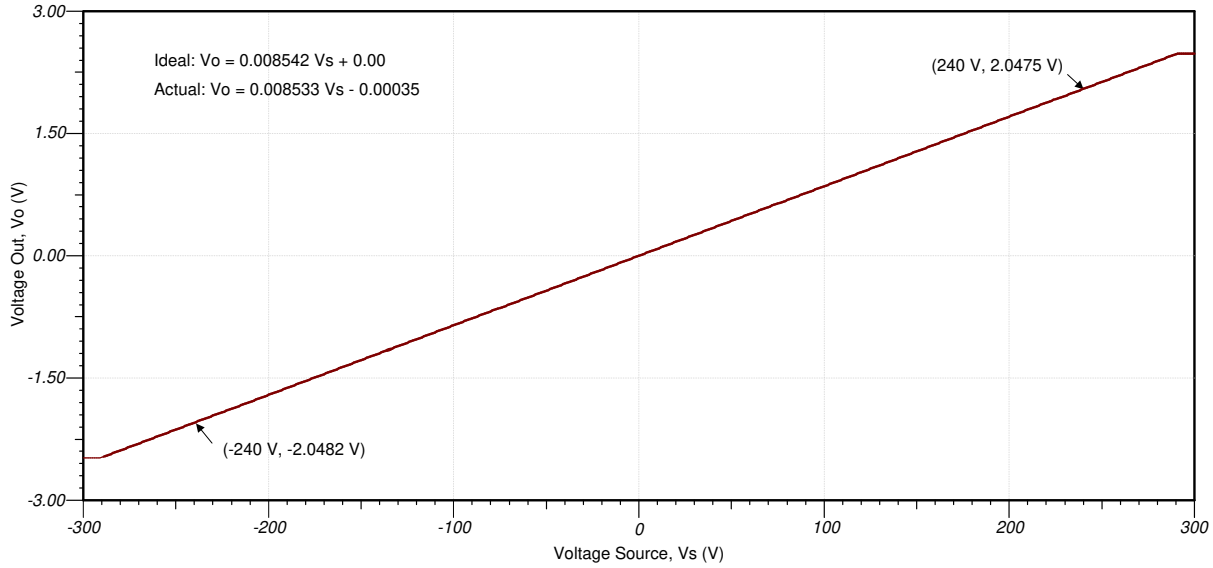
This is the resulting ideal circuit configuration. Note that Rind, shown in red, is shown to represent the differential input resistance of the **AMC1300B** and should not be added to the schematic.



DC Transfer Characteristics II

The following graphs show the simulated output for a ±240-V source using the new design. Recall that the desired linear ranges are ±250mV at the input of the amplifier and ±2.05V at the output of the amplifier.

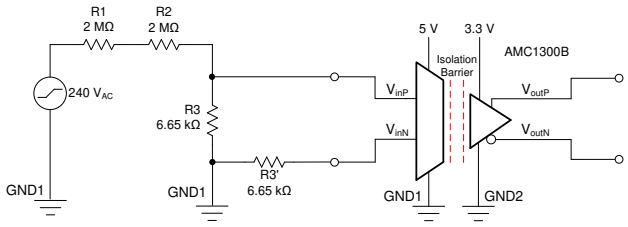




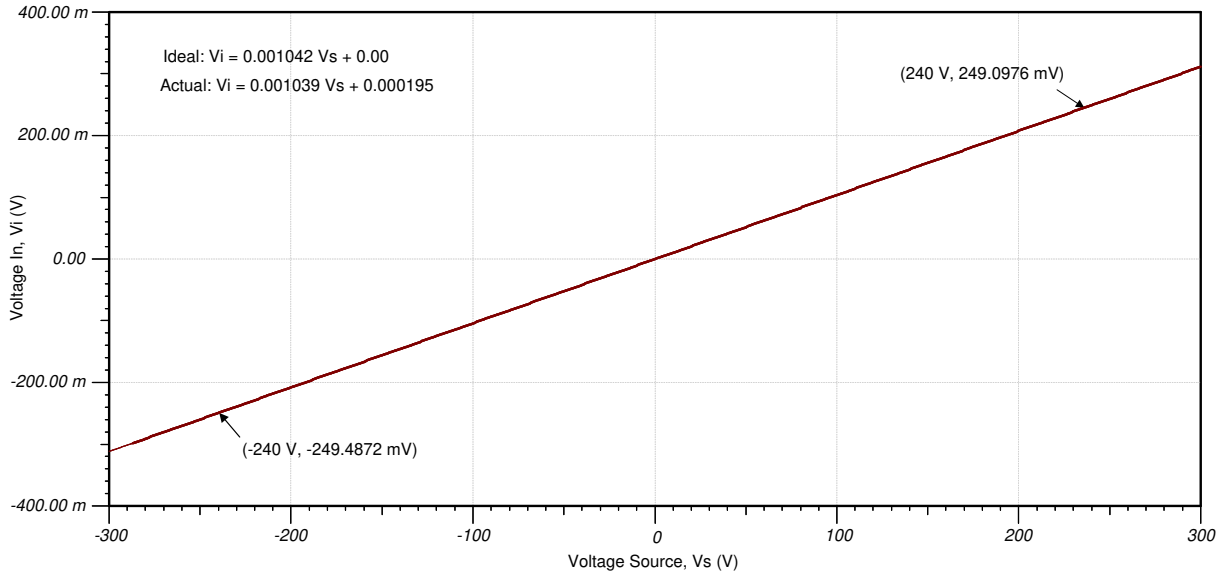
Clearly, the new design offers a dramatically improved offset error. The input offset voltage and gain error have been reduced to zero. The revised circuit also demonstrates better gain error performance due to the more accurate calculation used to find the desired value of R3 for the input voltage divider and the ideal value for R3'.

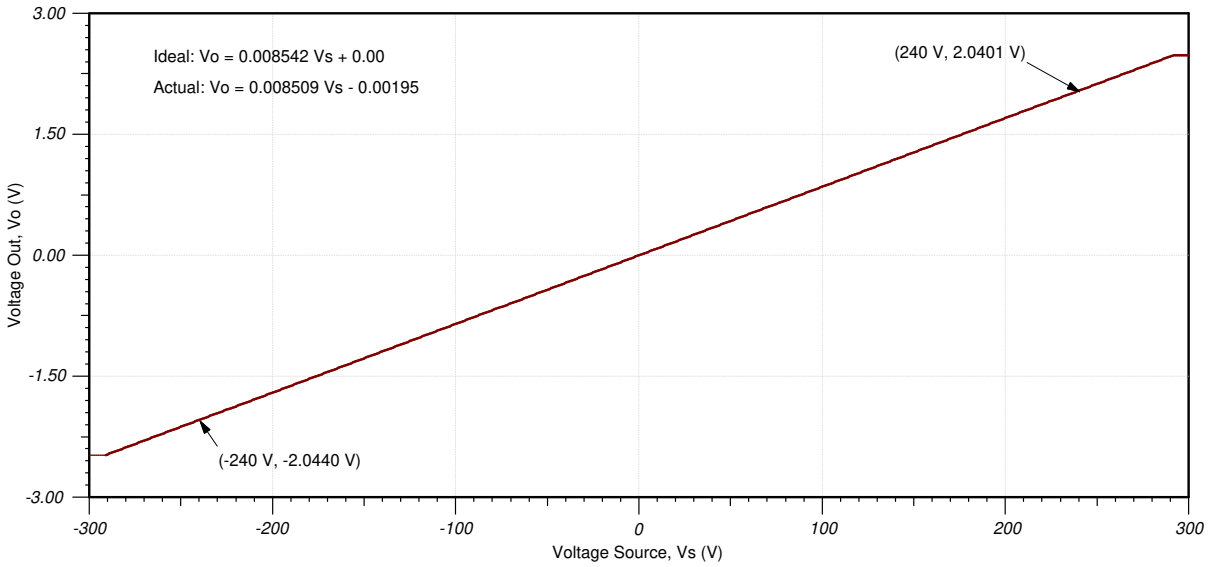
This positive outcome is a consequence of the addition of R3' to cancel the offset voltage introduced in the original design by the bias current of the **AMC1300B** device through R3. The drawback is that the ideal values for R3 and R3' are not commercially available, and in reality it would not be practical to use two different resistor values which are so close together.

Using the ***Analog Engineers Calculator***, it is possible to find the nearest E189 series resistor values that are readily available. In both cases, the nearest 0.1% resistor value to the calculated ideal values for R3 and R3' are 6.65kΩ. The final circuit diagram follows.



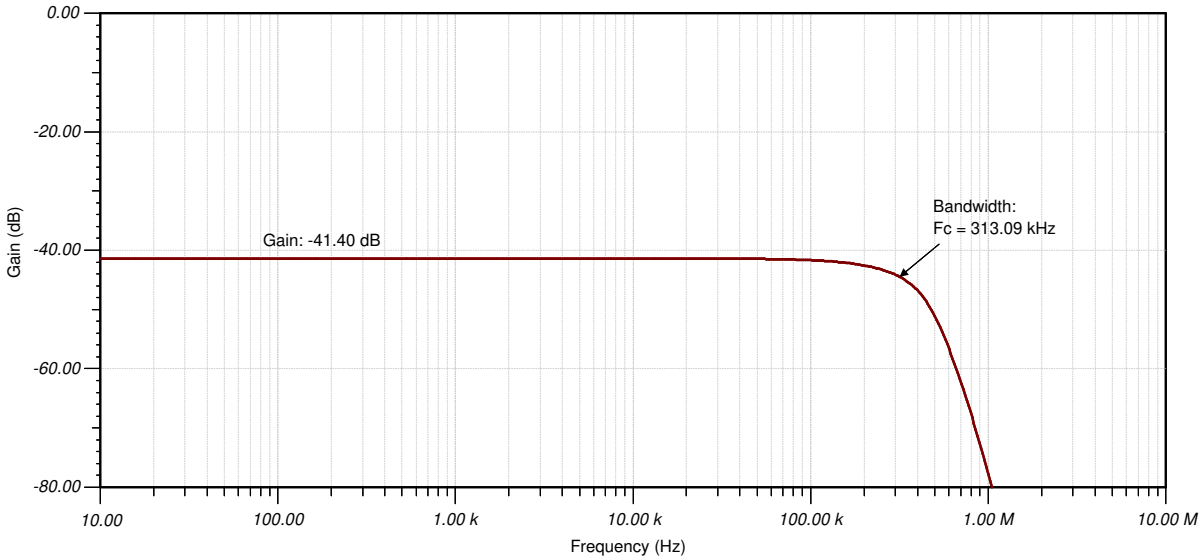
With readily available resistors used for R3 and R3', the circuit performance is still quite good as can be seen in the following graphs. The gain error on the input has been reduced from 18.2% to 0.3%. The gain error at the output has been reduced from 19.9% to 0.4%. The offset errors are also reduced to 195µV on the input and 2mV at the output.




Ideal: Vo = 0.008542 Vs + 0.00
Actual: Vo = 0.008509 Vs - 0.00195
(240 V, 2.0401 V)
(-240 V, -2.0440 V)
3.00
1.50
0.00
-1.50
-3.00
Voltage Out, Vo (V)
-300
-200
-100
0
100
200
300
Voltage Source, Vs (V)

AC Transfer Characteristics II

An AC sweep validates the frequency range across which one can expect to see the desired output. From the following simulation plot, the simulated gain of –41.40 dB, or 8.51mV/V, matches the gain result from the DC output plot. This is relatively close to the desired output gain of –41.37dB, or 8.54mV/V, as discussed in the previous section. The simulated bandwidth of the design, 313.1kHz, slightly exceeds the expectation set by the typical bandwidth specification of 310kHz in the data sheet.



References

1. **Analog Engineer's Circuit Cookbooks**
2. **Analog Engineer's Calculator**
3. **TI Precision Labs**

Design Featured Isolated Op Amp

AMC1300B	
VDD1	3.0V–5.5V
VDD2	3V–5.5V
Input Voltage range	±250mV
Nominal Gain	8.2
V_{OUT}	Differential ±2.05V on output common-mode of 1.44V
Input Resistance	19kΩ (typ, single-ended), 22kΩ (typ, differential)
Small Signal Bandwidth	310kHz
Input Offset Voltage and Drift	±0.2mV (max), ±3µV/°C (max)
Gain Error and Drift	±0.3% (max), ±15 ppm/°C (typ)
Nonlinearity and Drift	±0.03% (max), ±1 ppm/°C (typ)
Isolation Transient Overvoltage	$7.071kV_{PEAK}$
Working Voltage	$1.5kV_{RMS}$, $2.121kV_{DC}$
Common-mode transient immunity, CMTI	75 kV/µs (min), 140 kV/µs (typ)
AMC1300	

Design Alternate Isolated Op Amp

AMC1200	
VDD1	4.5V–5.5V
VDD2	2.7V–5.5V
Input Voltage range	±250mV
Nominal Gain	8
V_{OUT}	Differential ±2V, common-mode varies with supply range
Input Resistance	28kΩ (typ, differential)
Small Signal Bandwidth	100kHz
Input Offset Voltage and Drift	±1.5mV (max), ±10µV/°C (max)
Gain Error and Drift	±1% (max), ±56 ppm/°C (typ)
Nonlinearity and Drift	±0.1% (max), ±2.4 ppm/°C (typ)
Isolation Transient Overvoltage	$4kV_{PEAK}$
Working Voltage	$1.2kV_{peak}$
Common-mode transient immunity, CMTI	10kV/µs (min), 15kV/µs (typ)
AMC1200	

Split-Tap Connection for Line-to-Line Isolated Voltage Measurement Using AMC3330

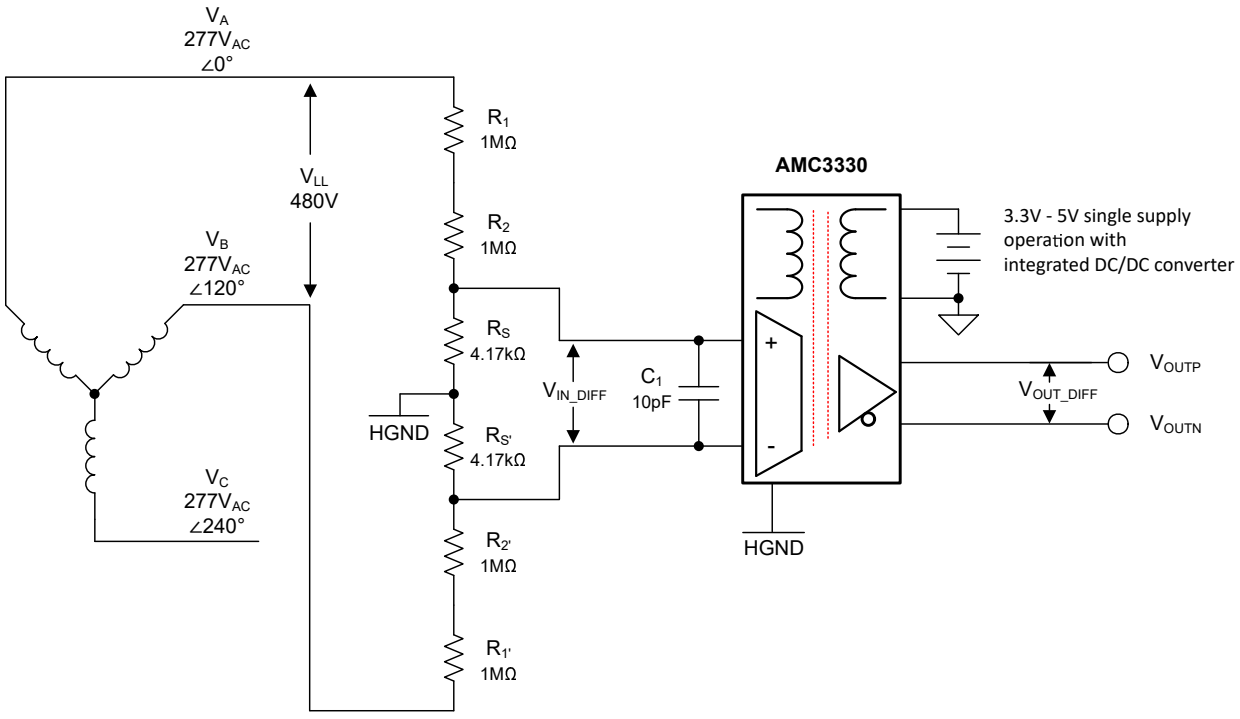
Design Goals

Voltage Source			AMC3330 Input Voltage		AMC3330 Output Voltage	
V_A	V_B	Resulting V_{LL}	$V_{IN\ DIFF,\ MIN}$	$V_{IN\ DIFF,\ MAX}$	$V_{OUT\ DIFF,\ MIN}$	$V_{OUT\ DIFF,\ MAX}$
277 V_{AC} ∠0°	277 V_{AC} ∠120°	±480 V	–1 V	+1 V	–2 V	+2 V

Design Description

This circuit performs a split-tap line-to-line isolated voltage-sensing measurement utilizing the **AMC3330** isolated amplifier and a voltage-divider circuit. The line-to-line measurement is taken between two 277 V_{AC} sources that are 120° out of phase. The voltage-divider circuit reduces the line-to-line voltage from ±480 V to ±1 V which matches the input voltage range of the **AMC3330**. The **AMC3330** can measure differential signals of ±1 V with a fixed gain of 2 V/V. The **AMC3330** has a differential input impedance of 1.2 GΩ and a low input bias current of 2.5 nA, which support low gain-error and low offset-error signal-sensing in high-voltage applications.

By using the split-tap configuration on a balanced three-phase AC voltage system, two line-to-line voltage measurements are sufficient to measure all three line-to-neutral voltages through derivation.



Design Notes

1. The AMC3330 is optimal for voltage-sensing applications due to its high input impedance and low input bias current, both of which minimize the DC errors. The integrated isolated power supply and bipolar input voltage range make the AMC3330 ideal for AC line-to-line voltage sensing.
2. Verify the linear operation of the system for the desired input signal range. This is verified using simulation in the **DC Transfer Characteristics** section.
3. Ensure the resistors used in the resistor divider circuit are capable of reducing the source input voltage to the AMC3330 input voltage range of ±1 V.
4. Ensure the resistors used in the resistor divider circuit have sufficient operating current and voltage ratings.
5. Verify that the AMC3330 input current is less than ±10 mA as stated in the absolute maximum ratings table of the data sheet.

Design Steps

1. Calculate the total line-to-line voltage (V_{LL}) between the two 277 V_{AC} sources that are 120° apart.

$$V_{LL} = \sqrt{3} \times 277\ V = 480\ V$$

2. Calculate the ratio of the line-to-line voltage to the input voltage of the AMC3330 for the voltage-divider circuit.

$$Ratio = \frac{1\ V_{AMC330,\,input}}{480\ V} = 0.0020833$$

4. Choose 1-MΩ resistors for R_1, R_2, $R_{1'}$, and $R_{2'}$. Using the ratio from the previous step and the following voltage-divider equation, solve for the equivalent sensing resistance, R_{sense}, required to reduce the AMC3330 input voltage to ±1 V.

$$0.0020833 = \frac{R_{sense}}{R_1 + R_2 + R_{1'} + R_{2'} + R_{sense}} = \frac{R_{sense}}{4\ M\Omega + R_{sense}}$$

$$R_{sense} = \frac{8333.2\ \Omega}{1 - 0.0020833} = 8350.6\ \Omega$$

5. The split-tap configuration requires two equivalent sensing-resistors, R_S and $R_{S'}$. Use the **analog engineer's calculator** to determine the closest standard value for R_S and $R_{S'}$.

$$R_S = R_{S'} = \frac{R_{sense}}{2} = \frac{8350.6\ \Omega}{2} = 4175.3\ \Omega = 4.17\ k\Omega$$

6. Calculate the current flowing through the voltage-divider circuit from the voltage source to ensure that the power dissipation does not exceed the ratings of the resistor. For additional details, see **Considerations for High Voltage Measurements**.

$$I_{AMC330,\,input} = \frac{V}{R} = \frac{480\ V}{4 \times 1\ M\Omega + 2 \times 4.17\ k\Omega} = 0.039\ mA$$

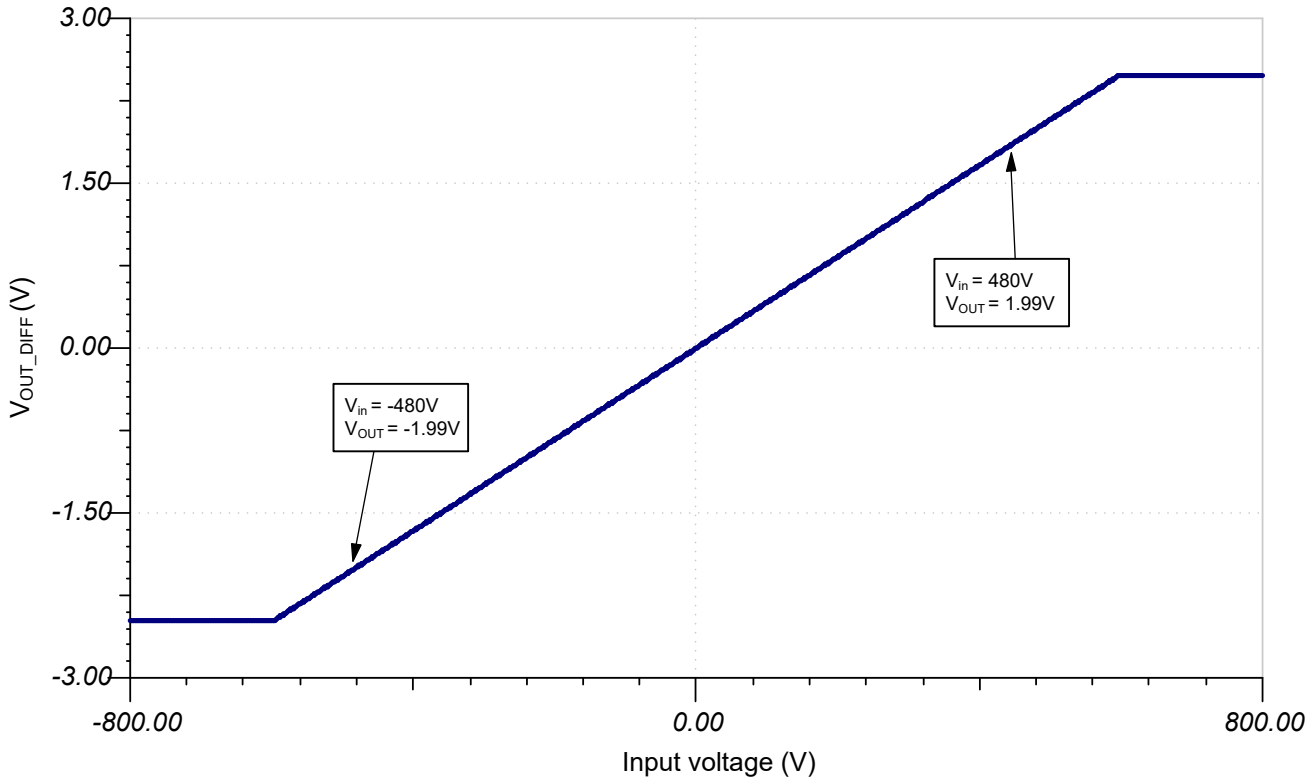
7. Since the gain of the voltage divider is $\frac{1}{480}$ and the gain of the AMC3330 is 2, the output voltage can be calculated for an input voltage of 480 V using the transfer function equation,

$$V_{OUT} = Gain \times V_{IN} \quad (37)$$

$$V_{OUT} = \frac{1}{480} \times 2 \times 480\,V = 2\,V$$

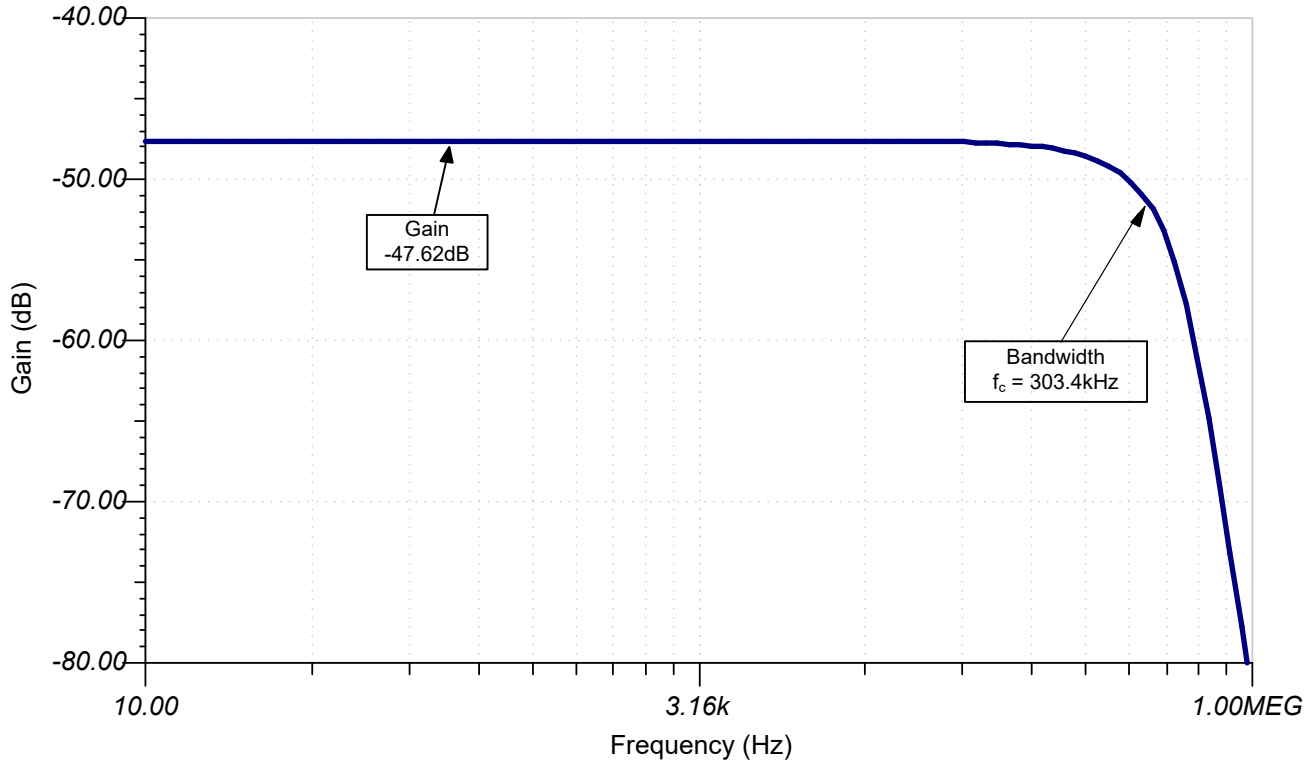
DC Transfer Characteristics

The following graph shows the simulated differential output of the AMC3330 for a ±800-V input. The output voltage is about 2 V for an input voltage of 480 V, as calculated on the previous page.



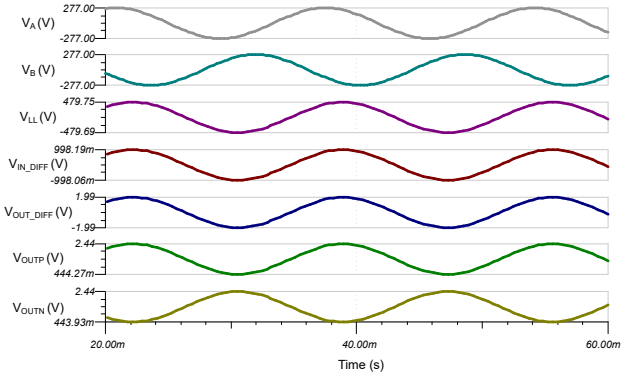
AC Transfer Characteristics

The simulated gain is –47.62 dB which closely matches the expected gain for the voltage divider and AMC3330.



Simulation Results

The following simulation shows the input and output signals of the AMC3330.



Design References

1. Isolated Amplifier Voltage Sensing Excel Calculator
2. Analog Engineer's Circuit Cookbooks
3. TI Precision Labs - Op Amps
4. TI Precision Labs - Analog-to-Digital Convertors

Design Featured Isolated Op Amp

AMC3330	
Input Voltage range	±1 V
Nominal Gain	2
Input Resistance	0.8 GΩ (typ)
Small Signal Bandwidth	375 kHz
Input Offset Voltage and Drift	±0.3 mV (max), ±4 µV/°C (max)
Gain Error and Drift	±0.2% (max), ±45 ppm/°C (max)
Nonlinearity and Drift	0.02% (max), ±0.4 ppm/°C (typ)
Isolation Transient Overvoltage	6 kV_{PEAK}
Working Voltage	1.2 kV_{RMS}
Common-mode transient immunity, CMTI	85 kV/µs (min)
AMC3330	

Design Alternate Isolated Op Amp

ISO224B	
VDD1	4.5 V–18 V
VDD2	4.5 V–5.5 V
Input Voltage range	±12 V
Nominal Gain	⅓
V_{OUT}	Differential ±4 V on output common-mode of VDD2 / 2
Input Resistance	1.25 MΩ (typ)
Small Signal Bandwidth	275 kHz
Input Offset Voltage and Drift	±5 mV (max), ±15 µV/°C (max)
Gain Error and Drift	±0.3% (max), ±35 ppm/°C (max)
Nonlinearity and Drift	0.01% (max), ±0.1 ppm/°C (typ)
Isolation Transient Overvoltage	7 kV_{PEAK}
Working Voltage	1.5 kV_{RMS}
Common-mode transient immunity, CMTI	55 kV/µs (min)
ISO224	

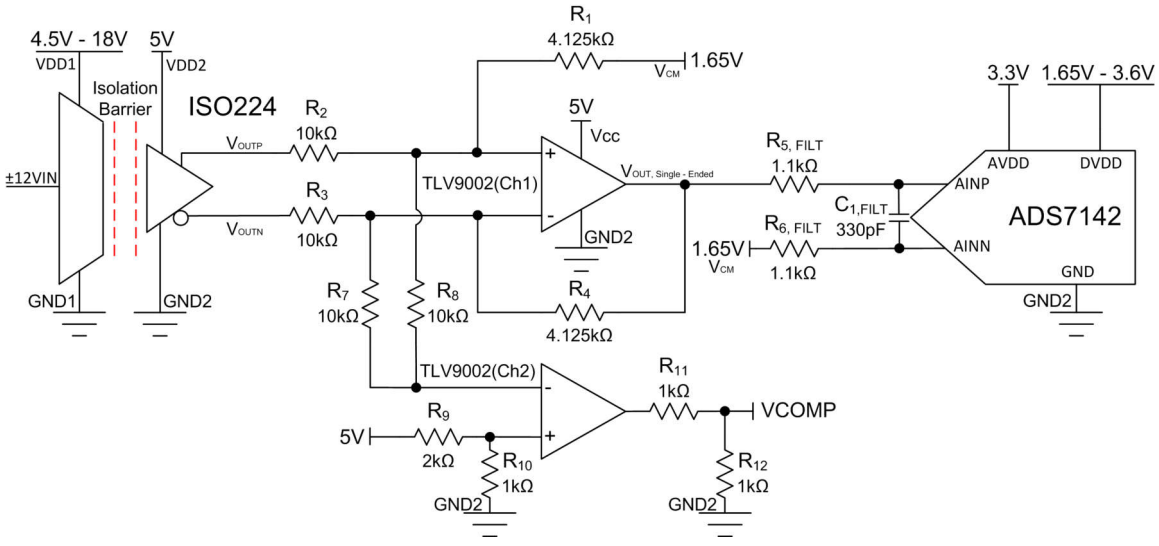
±12V Voltage Sensing Circuit With an Isolated Amplifier and Pseudo-Differential Input SAR ADC

ISO224 Input Voltage	ISO224 Output (V_{OUTP} – V_{OUTN})	ADS7142 Input (Pseudo-Differential)	ADS7142 Digital Output
12V	4V	3.3V	FFF_H
–12V	–4V	0V	000_H

Power Supplies and Reference Voltages			
VDD1	VDD2 and Vcc	AVDD	GND
4.5V - 18V	5V	3.3V	0V

Design Description

This circuit performs a ±12V isolated voltage sensing measurement using the **ISO224** isolated amplifier, **TLV9002** operational amplifier, and the **ADS7142** SAR ADC. The **ISO224** can measure single-ended signals of ±12V with a fixed gain of ⅓V/V and produces a ±4V isolated differential output voltage with an output common-mode voltage of VDD2 / 2. Channel 1 of the **TLV9002** conditions the output of the **ISO224** to fit the input range of the **ADS7142**, while channel 2 monitors the **ISO224** fail-safe output. The **ADS7142** is a dual-channel ADC with a full-scale input and reference voltage of AVDD which can range from 1.65V to 3.6V. For this cookbook circuit, the **ADS7142** dual-channel input is used in a pseudo-differential configuration which allows for both positive and negative signals to be measured by the **ISO224**. This circuit is applicable to many high voltage industrial applications, such as ***Train Control and Management Systems***, ***Analog Input Modules***, and ***Inverter and Motor Control***. The equations and explanation of component selection in this design can be customized based on system specifications and requirements.



Specifications

Specification	Calculated	Simulated
Transient ADC input settling at 140kSPS	403µV	88µV
Conditioned signal range	0V–3.3V	0V–3.3V
Noise (at the input)	262μV_{RMS}	526μV_{RMS}
Closed-loop bandwidth	175kHz	145kHz

Design Notes

1. The **ISO224** was selected due to the wide input range, flexible power configuration, and high accuracy.
2. The **ADS7142** was selected due to very low power, high level of integration, flexible power configurations, and small size.
3. The **TLV9002** operational amplifier was selected for the cost optimization, configuration options, and small size.
4. Select low impedance, low noise sources for AVDD, V_{CM}, and the pseudo-differential input to AINN which sets the common-mode voltage of the ADC.
5. Find the ADC full-scale range and common-mode specifications. This is discussed in component selection.
6. Select a COG capacitor for C_{FILT} to minimize distortion.
7. For best performance, consider using a 0.1% 20ppm/°C film resistor for $R_{FILT1,2}$ or better to minimize distortion.
8. ***Understanding and Calibrating the Offset and Gain for ADC Systems*** discusses methods for error analysis. Review the link for methods to minimize gain, offset, drift, and noise errors.
9. The ***TI Precision Labs - ADCs*** training video series discusses methods for selecting the charge bucket circuit R_{FILT} and C_{FILT}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here provide good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected. See ***Introduction to SAR ADC Front-End Component Selection*** for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select an isolated amplifier based on the input voltage range and determine the output common-mode voltage and output voltage range:

   The **ISO224** power supplies can be 4.5V to 18V for the high-side power supply, and 4.5V to 5.5V for the low-side power supply. The ISO224 has a ±12V single-ended input range with a fixed gain of ⅓V/V, yielding a ±4V differential output at a common-mode voltage of VDD2 / 2, 2.5V for this example:

$$\frac{\pm 12V_{\text{IN, Single}-\text{Ended}}}{3} = \pm 4V_{\text{OUT, Differential}} \text{ at } 2.5V\left(\frac{V_{DD2}}{2}\right) \text{common}-\text{mode}$$

2. Select an ADC with small size and low power:

   The **ADS7142** is a small sized, low power, dual channel ADC that can be used in a pseudo-differential configuration. The maximum input range is set by the reference voltage and is equal to AVDD, 3.3V for this example:

$$\text{ADC}_{\text{Full}-\text{Scale Range}} = V_{REF} = \text{AVDD} = 3.3V$$

   Find the required ADC common-mode voltage for pseudo-differential measurements:

$$V_{CM} = \frac{V_{REF}}{2} = 1.65V$$

3. Select an operational amplifier that can convert the ±4V differential, 2.5V common-mode output of the ISO224 to the 3.3V pseudo-differential, 1.65V common-mode input of the ADS7142. Additionally, selecting an operational amplifier with a second channel that can monitor the fail-safe output feature of the ISO224 is preferred.

The **TLV9002** is a 2 channel, rail-to-rail input and output amplifier optimized for cost sensitive and small size applications.

Channel 1 is used to convert the ±4V differential, 2.5V common-mode output of the ISO224 to a 3.3V peak pseudo-differential output with a common-mode voltage of 1.65V. When R1 = R4 and R2 = R3, the transfer function is set by the following equation:

$$V_{OUT} = V_{OUTP}\left(\frac{R_4}{R_3}\right) + V_{OUTN}\left(\frac{R_1}{R_2}\right) + V_{CM}$$

The signal must be converted from ±4V to 3.3V, this means that the signal must be reduced by a factor of 3.3V / ±4V = 3.3V / 8V. Substituting V_{CM} with the previously calculated value of 1.65V and setting R2 and R3 to 10kΩ yields the following equations:

$$3.3V = 4V\left(\frac{R_4}{10k\Omega}\right) + 1.65V \qquad 0V = -4V\left(\frac{R_1}{10k\Omega}\right) + 1.65V$$

Solving for R1 and R4 yields values of 4.125kΩ.

Additional information on this topic can be seen in the ***Interfacing a Differential-Output (Isolated) Amplifier to a Single-Ended Input ADC*** application brief.

Channel 2 of the TLV9002 is used to monitor the fail-safe output feature of the ISO224. The ISO224 fail-safe output feature becomes active whenever the high-side power supply (VDD1) is missing independent of the input signal on the V_{IN} pin. The TLV9002 channel 2 output (VCOMP) is fed to a GPIO port on the system controller and goes high whenever the fail-safe output feature is active. For additional details, see the ***Fail-Safe Output Feature*** application note.

4. Select R_{1FILT}, R_{2FILT}, and C_{FILT} for settling of the input signal and sample rate of 140kSPS:

Refine the R_{FILT} and C_{FILT} Values is a TI Precision Labs video showing the methodology for selecting R_{FILT} and C_{FILT}. The final value of 1.1kΩ and 330pF proved to settle to well below ½ of a least significant bit (LSB) within the acquisition window.

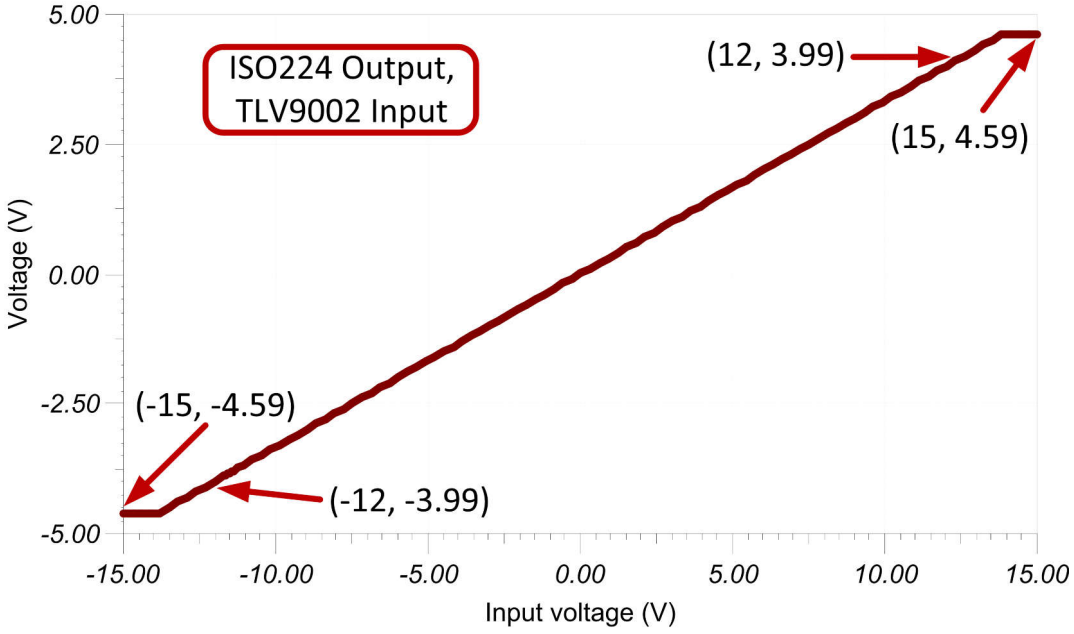
DC Transfer Characteristics

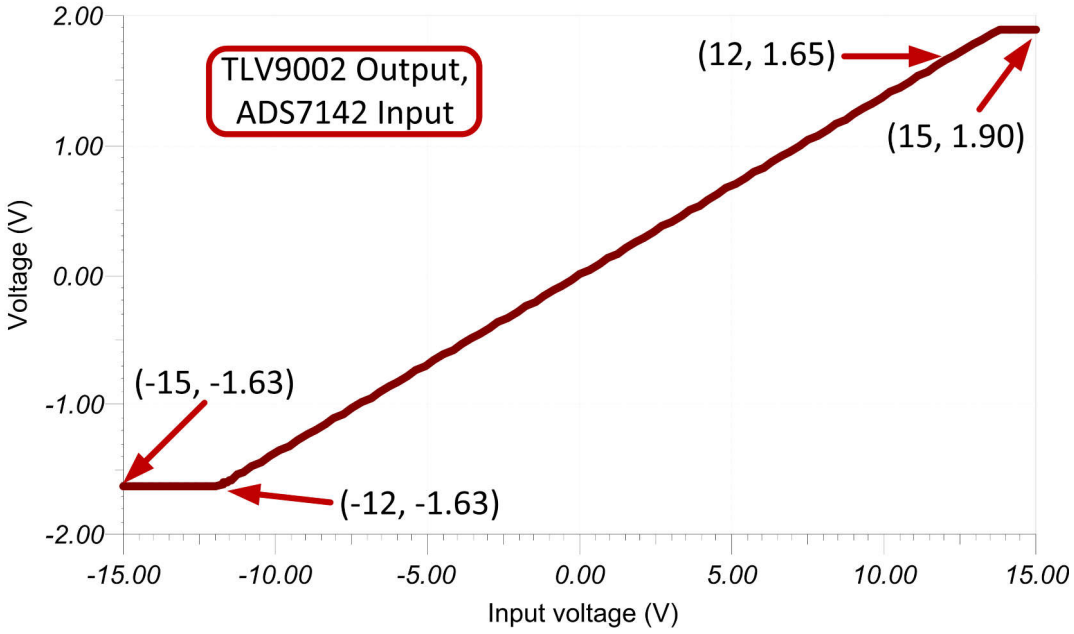
The following graphs show the simulated inputs of the TLV9002 and the ADS7142 from a ±15V input signal to the ISO224. The ISO224 has a linear output of ±VIN / 3 and the input to the TLV9002 can be seen in the first graph. The second graph shows that the TLV9002 further reduces the gain by VIN / 2.43 and shifts the common mode to 1.65V. This results in the full-range ±12V input signal using the 0V – 3.3V full-scale range (FSR) of the ADC with AVDD = VREF = 3.3V.

The following transfer function shows that the gain of the ISO224 and TLV9002 is 1/7.28V/V.

$$\text{Gain}_{\text{ISO224}} \times \text{Gain}_{\text{TLV9002}} \times V_{\text{IN}} = V_{\text{OUT}}$$

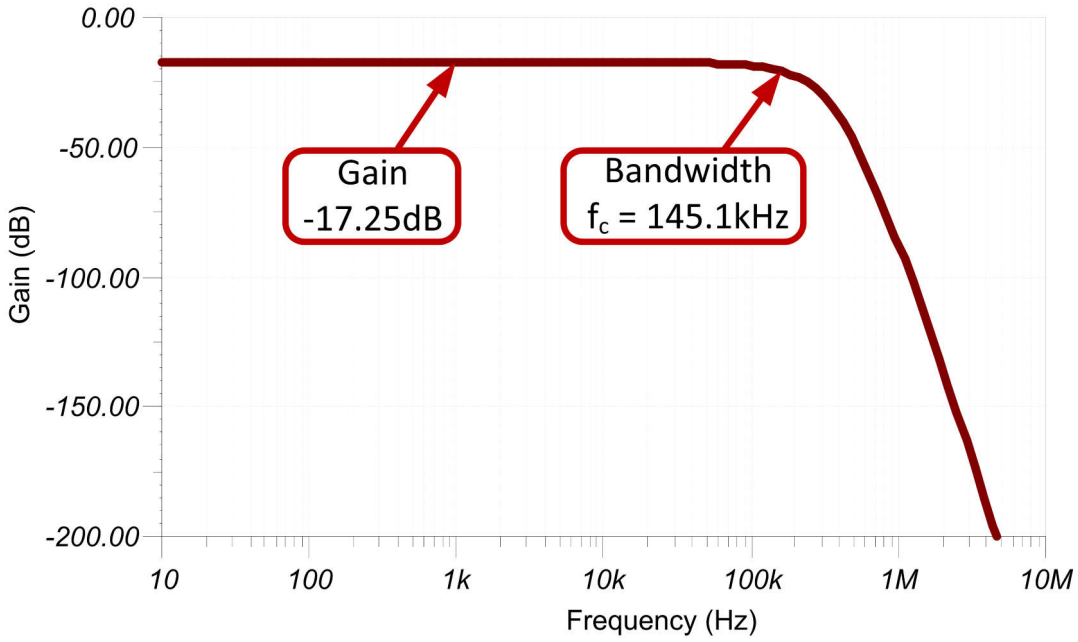
$$\frac{1}{3} \times \frac{1}{2.43} \times 12\text{V} = \frac{1}{7.28} \times 12\text{V} = 1.65\text{V}$$





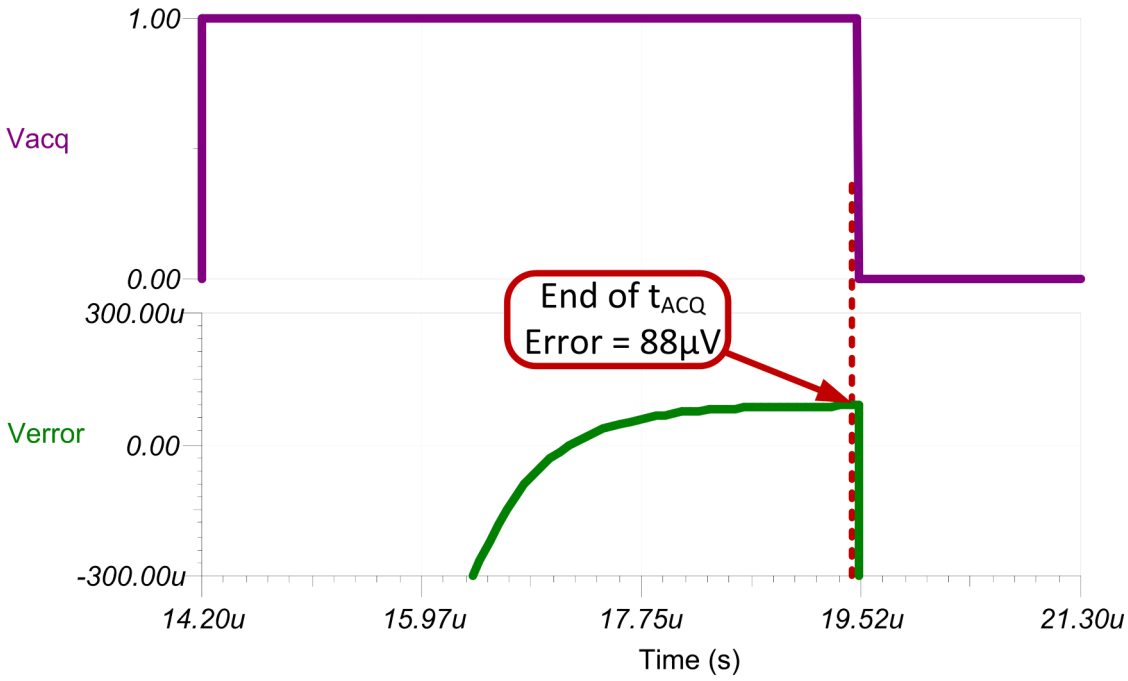
AC Transfer Characteristics

The simulated bandwidth of the signal chain is approximately 145kHz and the gain is –17.25dB, which is a linear gain of approximately 0.137V/V (attenuation ratio 1/7.28V/V). This matches the expected gain of the system.



Transient ADC Input Settling Simulation

The following simulation shows the transient settling results with an acquisition time of 5.3µs. The 88µV of noise is well within the 0.5 × LSB limit of 403µV. See ***Refine the Rfilt and Cfilt Values*** for detailed theory on this subject.



Noise Simulation

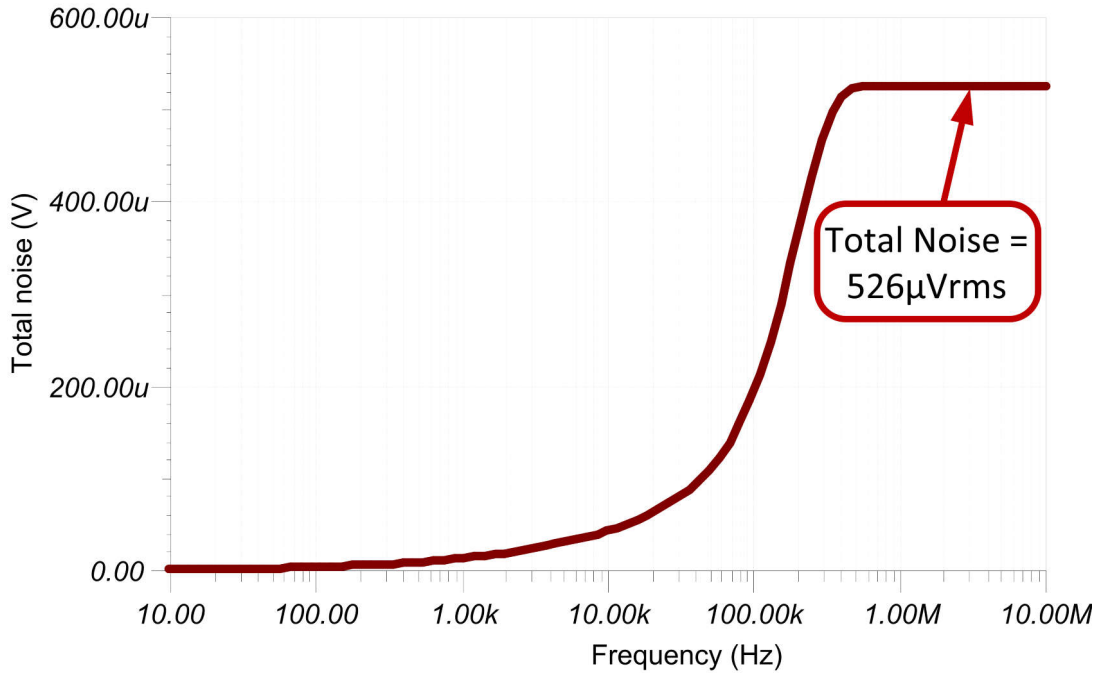
The simulated noise seen at the input of the ADC is greater than the expected calculated noise. This difference is due to noise peaking in the simulation model which is not included in the calculation. The following equations show that the ISO224 noise dominates the signal chain, and that the noise from the TLV9002 is negligible. See ***Calculating the Total Noise for ADC Systems*** for detailed theory on this subject.

$$E_n = \text{Gain}(e_n) = \sqrt{(1.57 \times BW)}$$

$$E_{nISO224A} = \frac{1}{3} \times \frac{1}{2.43}\left(\frac{4\mu V}{\sqrt{Hz}}\right) \times \sqrt{1.57 \times 145kHz} = 262\mu V_{RMS}$$

$$E_{nTLV9002} = \frac{1}{2.43}\left(\frac{27nV}{\sqrt{Hz}}\right) \times \sqrt{1.57 \times 145kHz} = 5\mu V_{RMS}$$

$$E_{nISO224A + TLV9002} = E_{nISO224A} + E_{nTLV9002} = \sqrt{262^2\mu V_{RMS} + 5^2\mu V_{RMS}} = 262\mu V_{RMS}$$



Design References

See ***Analog Engineer's Circuit Cookbooks*** for TI's comprehensive circuit library.

Link to Key Files

TINA files for Isolated Design: **SBAC226**.

Design Featured Devices

Device	Key Features	Link	Similar Devices
ISO224	±12V single-ended input range, fixed gain of ⅓, yielding ±4V differential output, output common-mode voltage of 2.5V, 4.5V to 18V high-side power supply, 4.5V to 5.5V low side power supply, input offset: ±5mV at 25°C, ±42µV/°C maximum, gain error: ±0.3% at 25°C, ±50ppm/°C maximum, nonlinearity: ±0.01% maximum, ±1ppm/°C, high-input impedance of 1.25MΩ.	ISO224	www.ti.com/isoamps
ADS7142	Dual-channel, full-scale input span and reference set by AVDD, 12-bit performance by default, 16-bit performance with high precision mode, very low current consumption of 0.45µA at 600SPS.	ADS7142	https://www.ti.com/PrecisionADCs
TLV9002	Dual-channel, rail-to-rail input and output amplifier, low broadband noise of 2727nV/√Hz, low input offset voltage of ±0.04mV.	TLV9002	https://www.ti.com/opamps

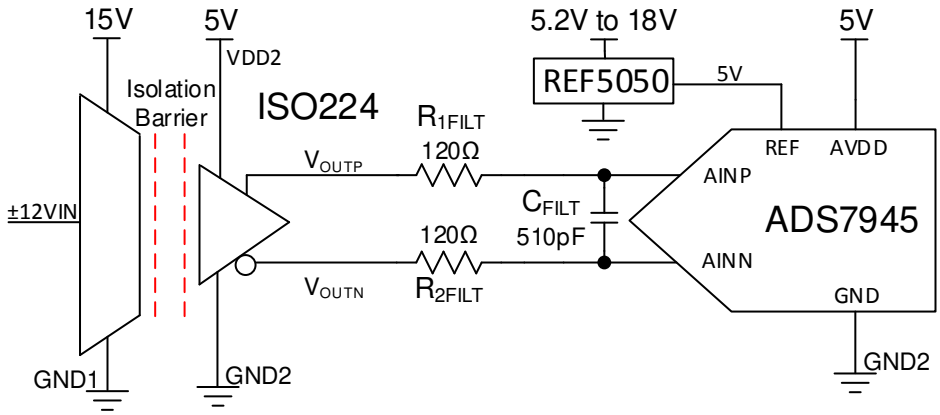
±12-V voltage sensing circuit with an isolated amplifier and differential input SAR ADC

ISO224 Input Voltage	ISO Output, ADC Input (V_{OUTP} - V_{OUTN})	Digital Output ADS7945
+12V	+4V	1999_H
–12V	–4V	$E666_H$

Power Supplies and Reference Voltages		
VDD1	VDD2 and AVDD	REF5050 External Ref
15V	5V	5V

Design Description

This circuit performs a ±12-V isolated voltage sensing measurement utilizing the **ISO224** isolated amplifier and the **ADS745** SAR ADC. The **ISO224** can measure true differential signals of ±12V with a fixed gain of ⅓V/V and produces an isolated differential output voltage with an output common-mode voltage of VDD2 / 2. The **ADS7945** is a fully differential input ADC with a full-scale input voltage of $\pm V_{REF}$ and a common-mode input voltage of V_{REF} / 2 ±200mV. Selecting a +5-V reference allows the ADS7945 to accept the full-scale and common-mode outputs from the **ISO224**. Capturing the **ISO224** output with a fully differential input ADC doubles the system dynamic range compared to a single-ended conversion. Many high-voltage industrial applications such as ***Protection Relays***, ***Channel-to-Channel Isolated ±10V Analog Input Cards***, and ***Inverter & Motor Control***. The equations and explanation of component selection in this design can be customized based on system specifications and needs.



Specifications

Specification	Calculated	Simulated
Transient ADC input settling at 100ksps	305µV	11µV
Conditioned signal range	±4V	±4V
Noise (at the input)	$1.9mV_{RMS}$	$1.73mV_{RMS}$
Closed-loop bandwidth	175kHz	185kHz

Design Notes

1. The **ADS7945** was selected due to its low power and a compatible analog input structure with the **ISO224**.
2. Verify the systems linear operation for the desired input signal range. This is verified using simulation in the DC Transfer Characteristics selection.

3. Select COG capacitors for C_{FILT} to minimize distortion.
4. ***Understanding and Calibrating the Offset and Gain for ADC Systems*** covers methods for error analysis. Review the link for methods to minimize gain, offset, drift, and noise errors.
5. The ***TI Precision Labs - ADCs*** training video series covers methods for selecting the charge bucket circuit R_{FILT} and C_{FILT}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to ***Introduction to SAR ADC Front-End Component Selection*** for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select an isolated amplifier based on the input voltage range and determine the output common-mode voltage and output voltage range:

   ISO224:

   - ±12-V single-ended input range
   - Fixed gain of ⅓, yielding ±4-V differential output
   - Output common-mode voltage of +2.5V
   - 4.5-V to 18-V high-side power supply, 4.5-V to 5.5-V low-side power supply
   - Input Offset: ±5mV at 25°C, ±42µV/°C maximum
   - Gain Error: ±0.3% at 25°C, ±50ppm/°C maximum
   - Nonlinearity: ±0.01% max, ±1ppm/°C
   - High-input impedance of 1.25MΩ
2. Select an ADC with an appropriate common-mode and differential input range to pair with the +2.5-V common-mode and ±4-V differential output of the ISO224:

   ADS7945:

   - ±5-V maximum analog input range
   - Full-scale input span set by ±voltage reference
   - Input common-mode range of V_{REF} / 2 ±0.2V
   - 2.7-V to 5.25-V power supply
   - High SNR of 84, low power of 11.6mW at 2Msps
3. Select a voltage reference that supports the common-mode constraint set by the 2.5-V common-mode output of the **ISO224** and the V_{REF} / 2 ±0.2-V common-mode input voltage of the ADS7945. This means that the reference output voltage must be 5V, low noise, and a configurable input voltage is preferred:

   REF5050:

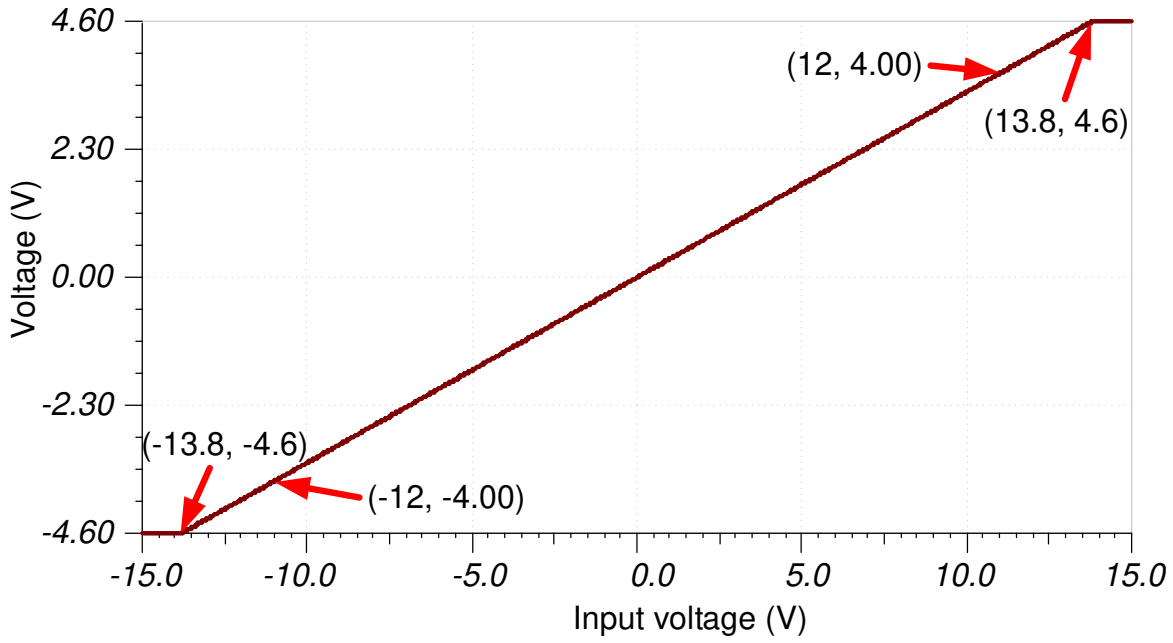
   - 5-V output
   - 5.2-V to 18-V input voltage power supply
   - 3µVPP/V noise
4. Select R_{1FILT}, R_{2FILT}, and C_{FILT} for settling of the input signal and sample rate of 100ksps:

Refine the R_{FILT} and C_{FILT} Values is a TI Precision Labs video showing the methodology for selecting R_{FILT} and C_{FILT}. The final value of 120Ω and 510pF proved to settle to well below ½ of a least significant bit (LSB) within the acquisition window.

DC Transfer Characteristics

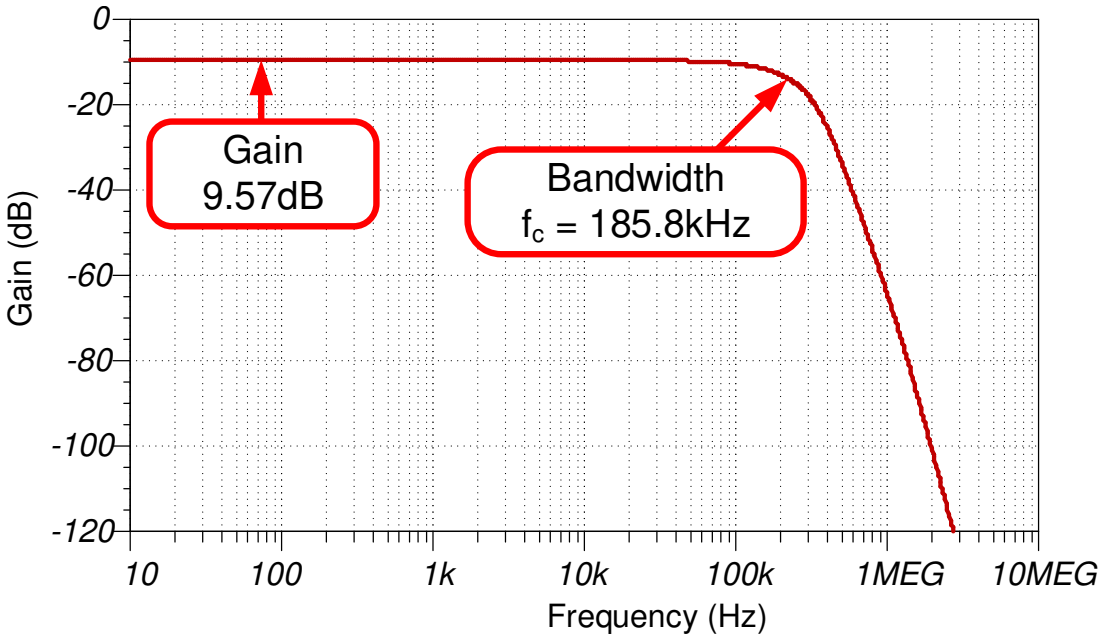
The following graph shows the simulated output for a ±15-V input. The desired linear range is a ±4-V output for a ±12-V input. This simulation shows that the linear output range is approximately ±4.6V which is well beyond the requirement.

The transfer function shows the ISO224 gain is ⅓ (that is, Gain · V_{IN} = V_{OUT}, (⅓)·(12V) = 4V).



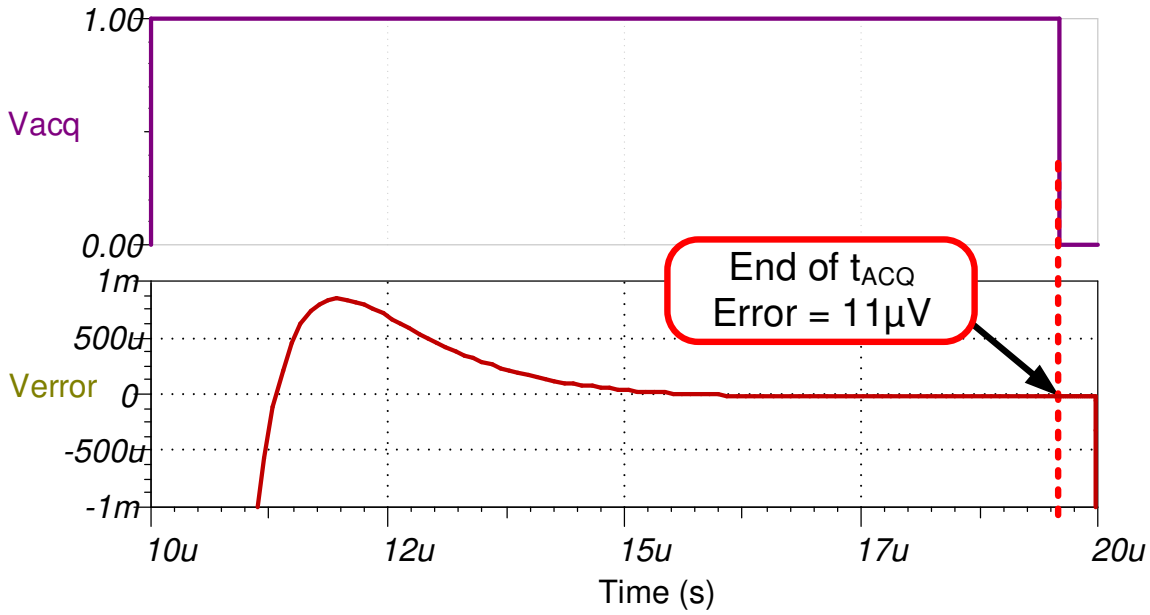
AC Transfer Characteristics

The simulated bandwidth is approximately 186kHz and the gain is –9.57dB (or 0.332V/V) which closely matches the expected gain and bandwidth for the **ISO224** (specified fc = 175kHz, gain = 0.333V/V).



Transient ADC Input Settling Simulation

The following simulation shows the transient settling results with an acquisition time of 9.6µs. The 11-µV settling error is well within the 0.5 × LSB limit of 305µV. See ***Refine the Rfilt and Cfilt Values*** for detailed theory on this subject.



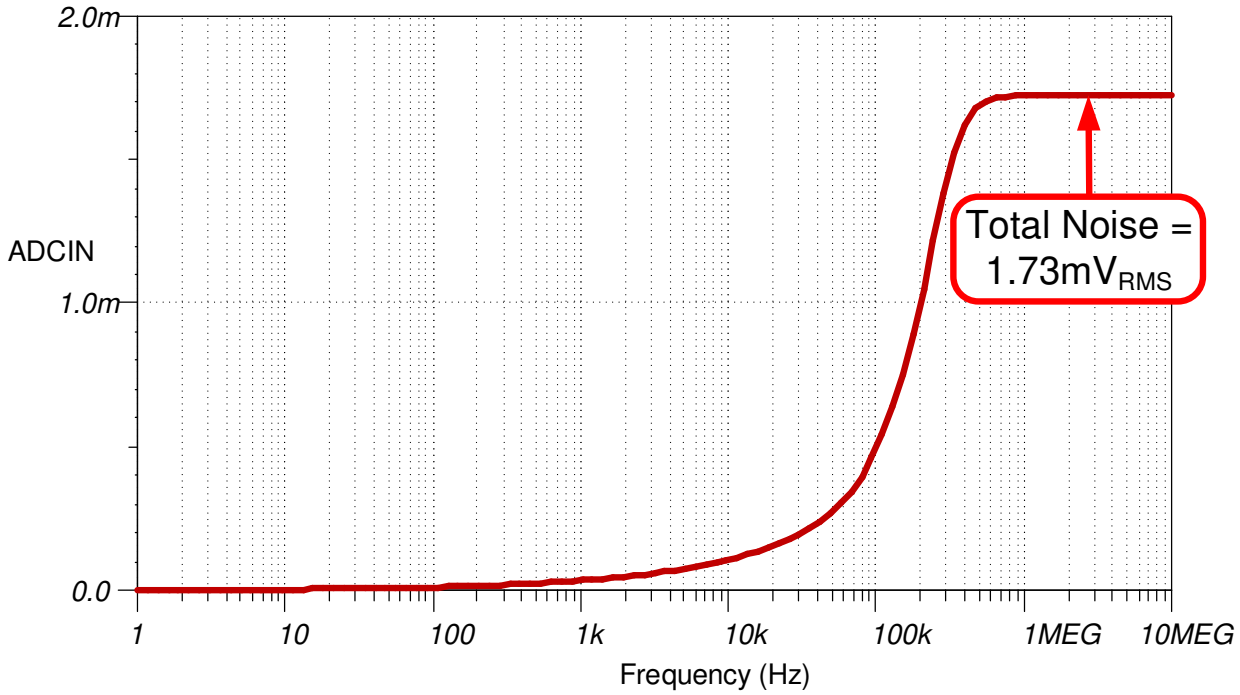
Noise Simulation

The following noise calculation looks only at the noise of the **ISO224**. The **ISO224** noise is substantially higher than other noise sources in the circuit, so the total noise can be approximated as the **ISO224** noise. The same method can be used for the B grade.

$$E_{nISO224A} = Gain(e_n)\sqrt{1.57 \cdot BW}$$

$$E_{nISO224A} = \frac{1}{3}\left(4\mu V / \sqrt{Hz}\right)\sqrt{1.57 \cdot 176kHz} = 0.7mV_{RMS}$$

The simulated noise is greater than the expected calculated noise. This difference is due to noise peaking in the simulation model. The noise peaking is not included in the calculation. Refer to ***Calculating the Total Noise for ADC Systems*** for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ISO224	±12-V single-ended input range, Fixed gain of ⅓, yielding ±4-V differential output, output common-mode voltage of +2.5V, 4.5-V to 18-V high-side power supply, 4.5-V to 5.5-V low side power supply, input offset: ±5mV at 25°C, ±42µV/°C max, gain error: ±0.3% at 25°C, ±50ppm/°C maximum, nonlinearity: ±0.01% maximum, ±1ppm/°C, high-input impedance of 1.25MΩ	www.ti.com/product/ISO224	www.ti.com/isoamps
ADS7945	±5 V max analog input range, full-scale input span set by ±voltage reference, input common mode range of V_{REF} / 2 ±0.2V, 2.7-V to 5.25-V power supply, high SNR of 84, low power of 11.6mW at 2Msps	www.ti.com/product/ADS7945	http://www.ti.com/opamps
REF5050	3ppm/°C drift, 0.05% initial accuracy, 4µVpp/V noise	www.ti.com/product/REF5050	http://www.ti.com/vref

Design References

See ***Analog Engineer's Circuit Cookbooks*** for TI's comprehensive circuit library.

Link to Key Files

See the **TINA files for Isolated Design**.

Isolated Undervoltage and Overvoltage Detection Circuit

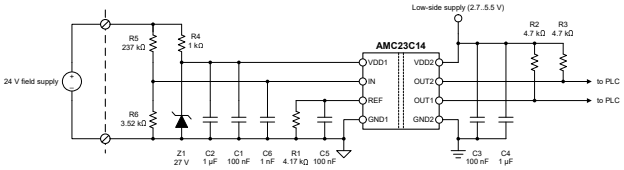
Design Goals

Overvoltage Level	Undervoltage Level	Low-Side V_{DD}	High-Side V_{DD}	Transient Response Time
28.8 V	20.4 V	2.7 V–5.5 V	24 V	360 ns

Design Description

This high-speed, isolated undervoltage and overvoltage detection circuit is implemented with a dual isolated window comparator with an adjustable threshold (AMC23C14). This circuit is designed for industrial field-supply applications where the controller-side must detect whether the remote module supply voltage is in a valid range.

The AMC23C14 is selected for its robust reinforced isolation with a high CMTI of 100 kV/µs (minimum), the adjustable dual window comparator thresholds, a wide high-side supply voltage range (3 V to 27 V), and the extended industrial temperature range (–40°C to +125°C).



Undervoltage and Overvoltage Detection Circuit Schematic

Design Notes

1. To minimize errors, choose precision resistors for the voltage divider (R_5 and R_6) and the threshold-setting resistor (R_1).
2. The AMC23C14 is powered from the field supply and is protected against voltage > 30 V (absolute maximum supply) by a Zener diode and shunt resistor.
3. Select the voltage divider and threshold-setting resistors based on the desired operating voltage range.

Design Steps

1. Determine the voltage divider ratio needed to trip the fixed internal 300-mV threshold when the power supply exceeds the minimum valid operating voltage of 20.4 (24 V – 15%). Size the total resistance of the voltage divider to set its current at 100 µA when the V_{supp} is at the desired operating voltage of 24 V.

$$IN = V_{supp}\left(\frac{R_6}{R_5 + R_6}\right)$$

$$300\ mV = 20.4\ V\left(\frac{R_6}{R_5 + R_6}\right)$$

$$V_{supp} = 100\ \mu A \times \left(R_5 + R_6\right)$$

$$24\ V = 100\ \mu A \times \left(R_5 + R_6\right)$$

Solving the system of equations results in R_5 = 236 kΩ, R_6 = 3.52 kΩ.

- Using the **Analog Engineer's Calculator**, the closest E96 resistor value is 237 kΩ and 3.48 kΩ.

2. Size the threshold-setting resistor to trip the adjustable-threshold comparator when the power supply exceeds 28.8 V (24 V + 20%).

$$IN = V_{supp}\left(\frac{R_6}{R_5 + R_6}\right)$$

$$IN = 28.8\ V\left(\frac{3.52\ k\Omega}{237\ k\Omega + 3.52\ k\Omega}\right)$$

$$IN = 0.42\ V$$

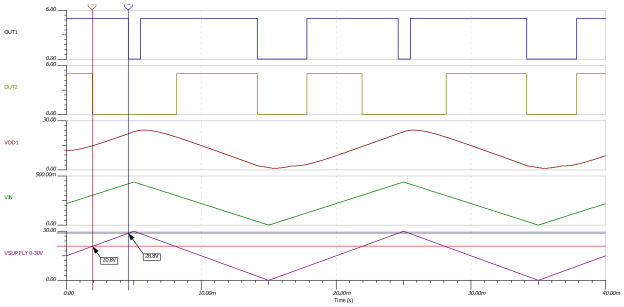
$$V_{ref} = IN$$

$$R_1 = \frac{V_{ref}}{I_{ref}} = \frac{0.42\ V}{100\ \mu A} = 4.2\ k\Omega$$

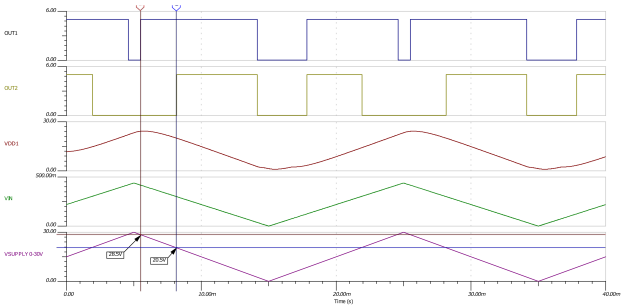
3. Select a 27-V Zener diode to protect the AMC23C14 from voltages greater than the recommended operating supply voltage.

Design Simulations

The following images are SPICE simulation waveforms of the undervoltage and overvoltage detection circuit. Included is the VDD1 input, which shows the Zener diode protects the VDD1 input from voltages outside of its operating range. **SPICE Simulation of the Undervoltage and Overvoltage Detection Circuit - Rising** shows the Spice simulation with the output trigger points on a rising input voltage. **SPICE Simulation of the Undervoltage and Overvoltage Detection Circuit - Falling** shows a similar image but with the output trigger points on a falling input voltage. Comparing the two figures, the trigger points differ by 0.3 V with the falling voltage input having a lower trigger value.



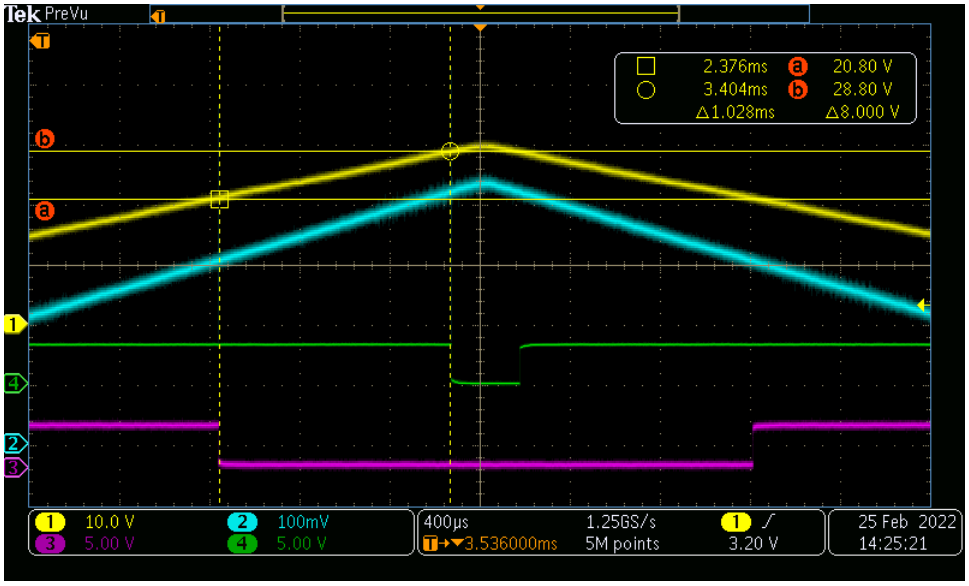
SPICE Simulation of the Undervoltage and Overvoltage Detection Circuit - Rising



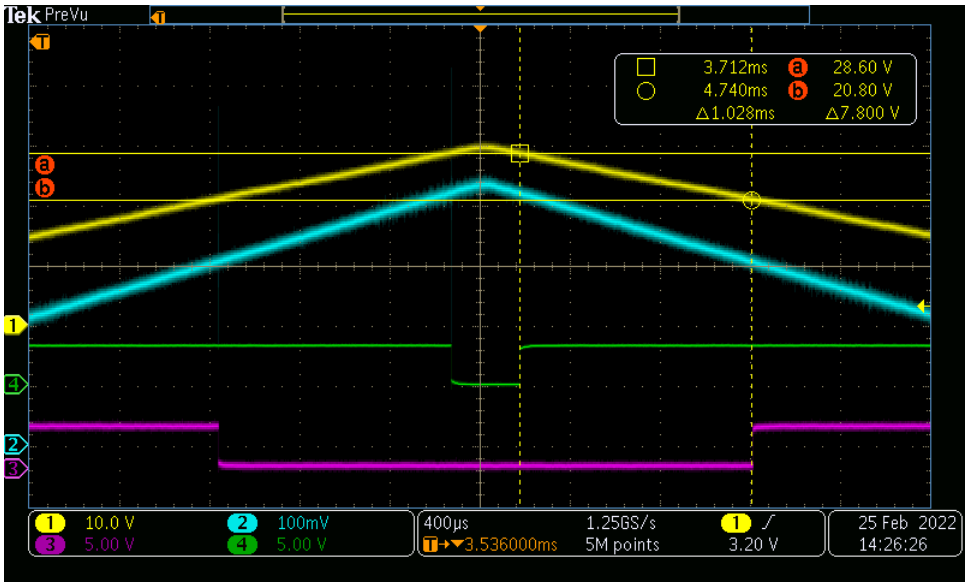
SPICE Simulation of the Undervoltage and Overvoltage Detection Circuit - Falling

Measured Response

The following images show the measured output of the undervoltage and overvoltage detection circuit, comparing the outputs to the V_{supp} voltage (trace 1). The AMC23C14 has open-drain outputs that are normally pulled up to VDD2, and is driven low when the input voltage exceeds the threshold voltage of each comparator. In these measurements OUT1 (trace 3) transitions low if V_{supp} exceeds 28.8 V, and OUT2 transitions low if Vsupp exceeds 20.8 V. Component variations and the comparator hysteresis can affect the trip thresholds, but in this case the trip point is within less than 1% of the desired values. The voltage thresholds vary slightly if V_{supp} is rising or falling. The second waveform depicts this with OUT1 triggering at 28.6 V instead of 28.8 V.

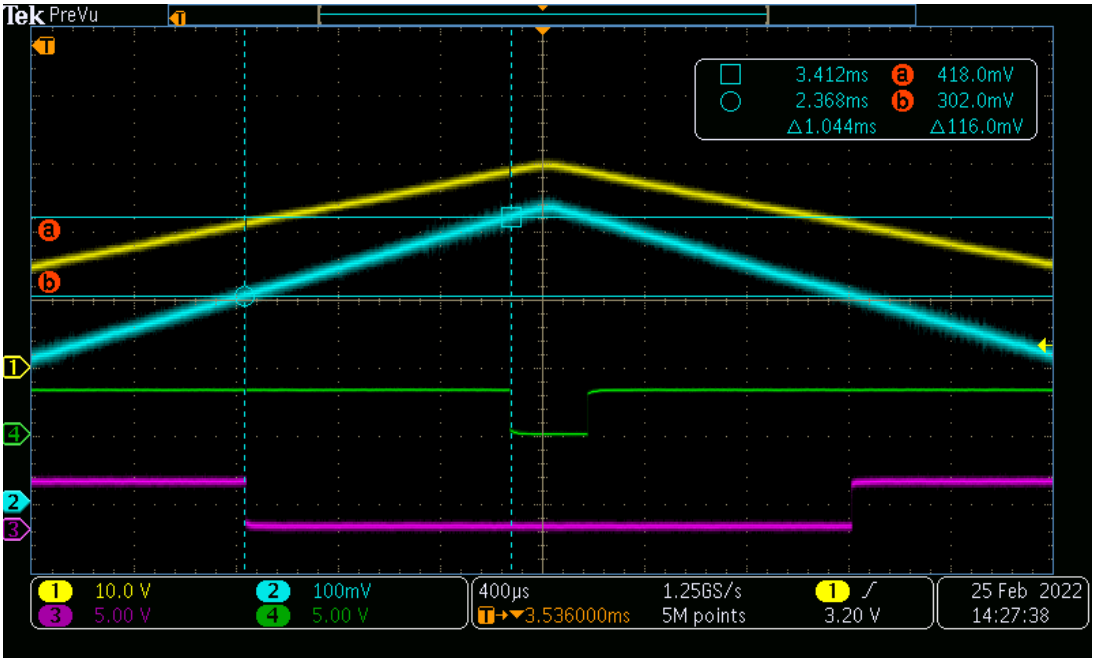


Waveform Capture With V_{supp} Increasing

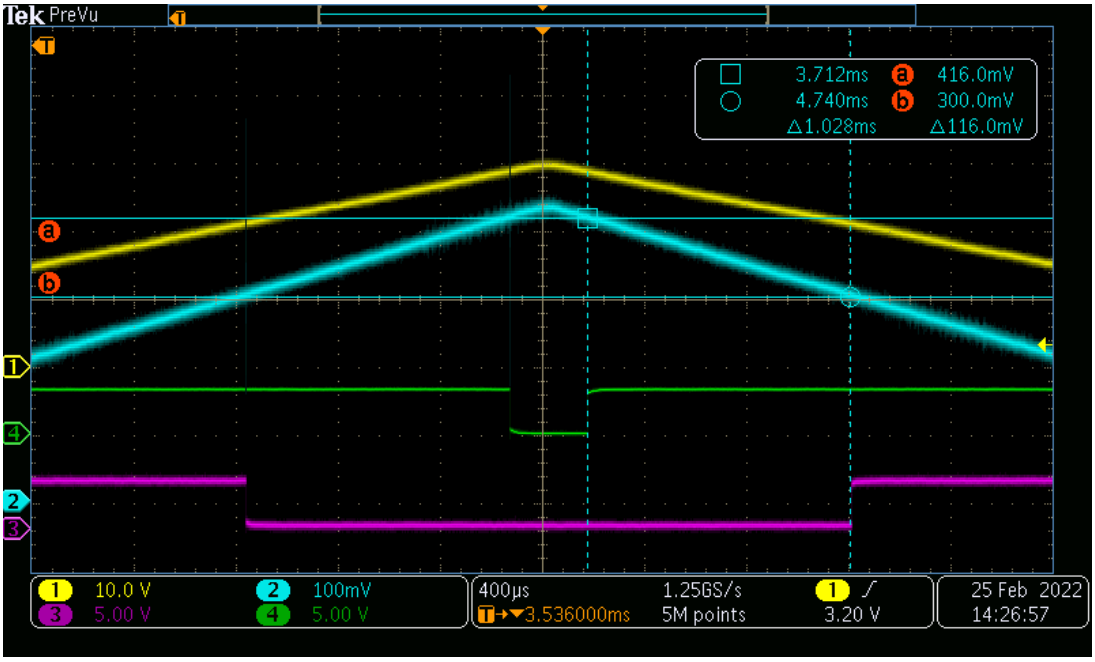


Waveform Capture With V_{supp} Decreasing

The following images show the measured output of the undervoltage and overvoltage detection circuit, comparing the AMC23C14 outputs to the VIN voltage (trace 2). These measurements confirm that the comparator trip thresholds match the desired values set by the internal comparator threshold at 300 mV, and the externally set threshold at 420 mV as defined in the **equation** in **2** of the **Design Steps** section.



Waveform of IN When V_{supp} is Increasing



Waveform of IN When V_{supp} is Decreasing

Design Featured Device

Device	Key Features	Device Link
AMC23C14	• Wide high-side supply range: 3 V to 27 V • Low-side supply range: 2.7 V to 5.5 V • Dual window comparator: – Window comparator 1: ±20-mV to ±300-mV adjustable threshold – Window comparator 2: ±300-mV fixed threshold • Supports positive-comparator mode: – Cmp0: 600-mV to 2.7-V adjustable threshold – Cmp2: 300-mV fixed threshold – Cmp1 and Cmp3: Disabled • Reference for threshold adjustment: 100 µA, ±2% • Trip threshold error: ±1% (max) at 250 mV • Propagation delay: 290 ns (typ) • High CMTI: 15 kV/µs (min) • Open-drain outputs • Safety-related certifications: – 7000-V_{pk} reinforced isolation per DIN VDE V 0884-11 – 5000-V_{RMS} isolation for 1 minute per UL1577 • Fully specified over the extended industrial temperature range: –40°C to +125°C	Device: **AMC23C14** Similar Devices: **Isolated amplifiers**

Design References

See **Analog Engineer's Circuit Cookbooks** for TI's comprehensive circuit library.

Texas Instruments, ***AMC23C14 AMC23C14 Dual, Fast Response, Reinforced Isolated Window Comparator With Adjustable Threshold*** data sheet

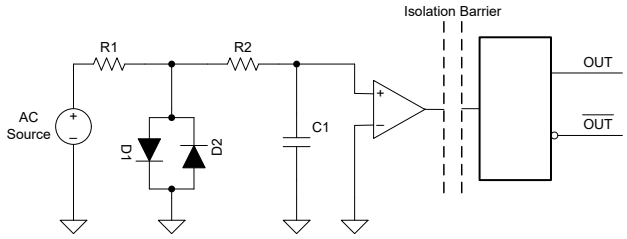
Isolated Zero-Cross Detection Circuit

Design Goals

High Side Supply	Input Voltage	Working Voltage	Low Side Supply	Output Voltage
12 V	±170 V_{pk} Sine Wave	≥ 400 V_{RMS}	3.3 V to 5.0 V ±10%	≤ Low-Side Supply

Design Description

A zero-crossing detector circuit changes output state when the AC input crosses the zero-cross reference voltage. This design features a single chip solution for zero-crossing detection of an AC sine wave with inverting and non-inverting digital outputs. The circuit is created by setting the comparator inverting input to ground and applying a clamped sine wave to the noninverting input. The input voltage is clamped by R1 and a pair of antiparallel diodes. In this case, diodes are used instead of an attenuator to maximize the slew rate of the input near the zero-crossing, which reduces output latency. The circuit is used for AC line zero-cross detection in control circuits to reduce standby and off-mode power consumption.



Isolated Zero-Cross Detection Circuit Schematic

Design Notes

1. The circuit must be capable of handling 750-V working voltage across the isolation barrier.
2. The maximum input voltage at IN+ must be ±1 V
3. Inverting and non-inverting output are desired
4. Maximum current flowing through R1 is 100 µA ±10%
5. Limit the operating voltage of each resistor in the string to 100 V ±10% maximum
6. The input AC source voltage is 120 V_{RMS}, higher AC voltages are easily accommodated with component modifications. See the **Alternate Design** section for details
7. Ensure the hysteresis voltage at the AC zero-cross is no more than ±30 mV

Design Steps

1. Determine the ideal R1 resistor value. The maximum peak input voltage of 120 V_{RMS} × √2 = 170 V_{PK}. Note that the forward voltage of the diode D1 is near zero, and not included in this calculation.

$$R1 = \frac{170\ V_{PK}}{100\ \mu A} = 1.70\ M\Omega$$

2. Divide R1 into 3 equal resistors to maintain design limits of ≤ 100 V per resistor:

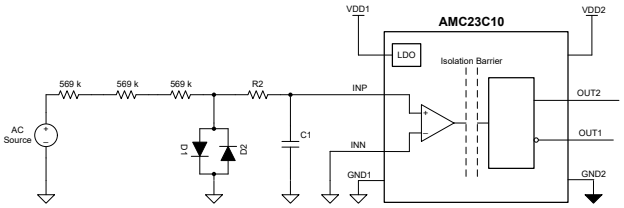
$$R1 = \frac{1.70\ M\Omega}{3} = 566.66\ k\Omega$$

3. Use the **Analog Engineer's Calculator** to find a standard E96 1% resistor value for R1. The nearest value is 569 kΩ.
4. Select the anti-parallel diodes. Choose diodes which will provide at least ± 350-mV forward voltage with the 100 µA supplied through R1.
5. Optional – design low-pass filter at VINP defined by R2 and C1. The frequency response is defined as:

$$F_C = \frac{1}{2\pi \times R2 \times C1}$$

Revised Design

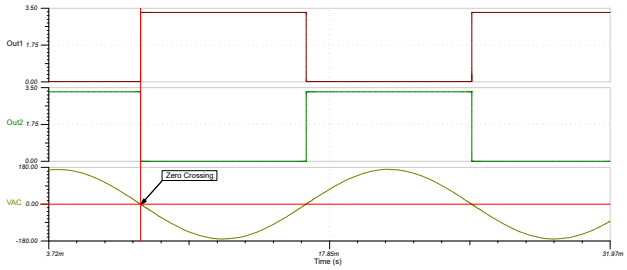
The following schematic shows implementation of the revised design using the AMC23C10.



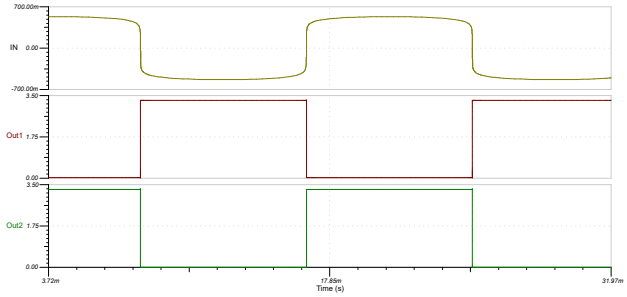
Revised Design With AMC23C10 Isolated Comparator

The AMC23C10 uses capacitive isolation to provide a working voltage of 1000 V. The voltage source for VDD1 is specified from 3 V to 27 V, controlled internally through an LDO. VDD2 is specified from 2.7 V to 5.5 V. The input voltage range under normal operation is ±1 V. The logic output on OUT1 is open drain which can be used with a pullup resistor to VDD1. OUT2 is a push-pull type output needing no external pullup resistors.

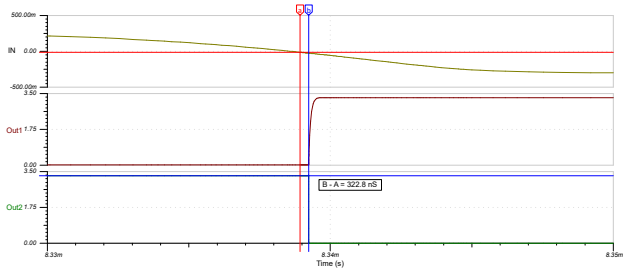
Design Simulations



Simulation of Zero-Crossing Detection With Sine Wave Input



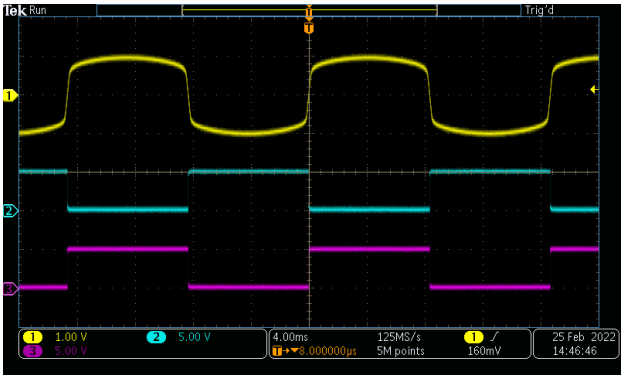
Simulation of Zero-Crossing Detection With Rectified Input



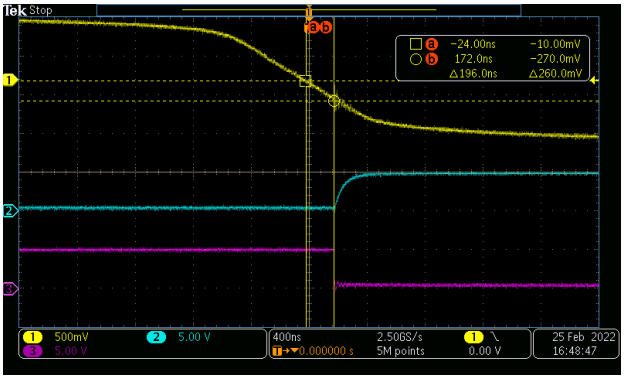
Simulation of Response Time for Zero-Crossing Detection

Measured Response

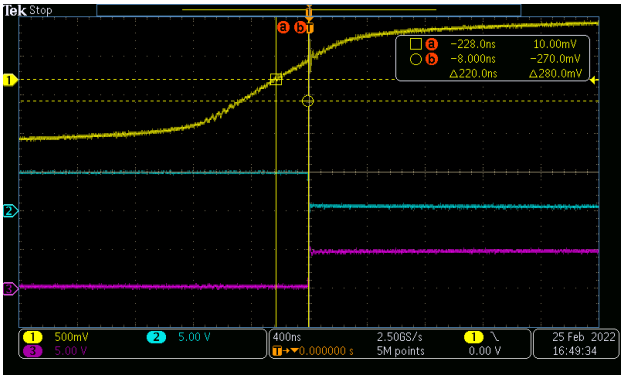
The following images show the measured response of the zero-crossing detection circuit using the AMC23C10 isolated comparator. The input is captured on trace 1, while OUT1 and OUT2 are shown on traces 2 and 3 respectively. When measured at both the rising and falling edges of the input, the delay between the zero-crossing of the input and the output transition does not exceed 220 ns.



Zero-Crossing Detection of Rectified Input



Zero-Crossing Detection Output Latency – Falling Edge



Zero-Crossing Detection Output Latency – Rising Edge

Design References

See ***Analog Engineer's Circuit Cookbooks*** for TI's comprehensive circuit library.

Texas Instruments, ***AMC23C10 Fast Response, Reinforced Isolated Comparator With Dual Output*** data sheet

Design Featured Isolated Comparator

AMC23C10	
Working Voltage	1000 V_{RMS}
VDD1	3.0 V–27 V
VDD2	2.7 V–5.5 V
Input Voltage Range	±1000 mV
Output Options	OUT1 - Open Drain
	OUT2 - Push-Pull
AMC23C10	

Alternate Design for 230-VAC Input

AMC23C10	
Working Voltage	1000 V_{RMS}
AC Input	325 V_{pk}
R1 Ideal	3.25 MΩ
R1 E96 Standard	Three each 1.09 MΩ

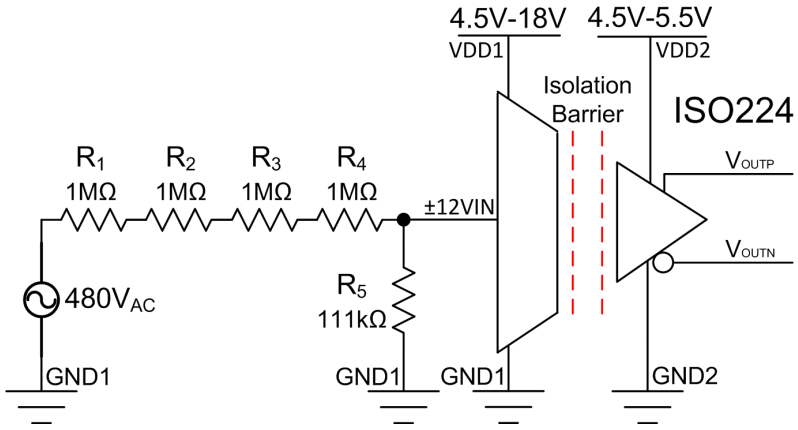
±480V Isolated Voltage-Sensing Circuit With Differential Output

Design Goals

Voltage Source		ISO224 Input Voltage		ISO224 Output Voltage VDD2 / 2 Common Mode (V_{OUTP} – V_{OUTN})		Power Supplies	
V_{MAX}	V_{MIN}	$V_{IN, MAX}$	$V_{IN, MIN}$	$V_{OUT, MAX}$	$V_{OUT, MIN}$	VDD1	VDD2
480V	–480V	12V	–12V	4V	–4V	4.5V–18V	4.5V–5.5V

Design Description

This circuit performs a ±480V, isolated, voltage-sensing measurement utilizing the **ISO224** isolated amplifier and a voltage-divider circuit. The voltage-divider circuit reduces the voltage from ±480V to ±12V which matches the input range of the **ISO224.** The **ISO224** is powered from both a high and low side power supply. Typically, the high side supply is generated using a floating supply or from the low side using an isolated transformer or isolated DC/DC converter. The **ISO224** can measure single-ended signals of ±12V with a fixed gain of ⅓V/V and produces an isolated differential output voltage of ±4V with an output common-mode voltage of VDD2 / 2. The differential output voltage can be scaled as required using an additional operational amplifier such as the **TLV6001** as shown in **SBOA274** to interface with an ADC.



Design Notes

1. Verify the systems linear operation for the desired input signal range. This is verified using simulation in the *DC Transfer Characteristics* section.
2. Verify that the resistors used in the resistor divider circuit (R_1–R_5) are capable of dissipating the power supplied from the voltage source.
3. Verify that the voltage on the input of the ISO224 is less than ±15V as stated in the absolute maximum ratings table of the data sheet and make sure that less than ±10mA is applied to the input. If the system is susceptible to transients, consider adding a TVS diode to the input. See the *I-V Curve of the Input Clamp Protection Circuit* image in the ***ISO224 Reinforced Isolated Amplifier with Single-Ended Input of ±12 V and Differential Output of ±4 V*** data sheet for additional details.

Design Steps

1. Calculate the ratio from the voltage source to the input of the ISO224 for the voltage-divider circuit.

$$\frac{12V_{ISO224,INPUT}}{480V} = 0.025$$

2. The typical input impedance of the ISO224 is 1.25MΩ. This impedance is in parallel with resistor R_5 and must be considered when designing the voltage-divider circuit. Select 1MΩ resistors for R_1, R_2, R_3, and R_4. Using the ratio from the previous step and the following voltage-divider equation, solve for the equivalent resistance required for the voltage-divider parallel combination (||) of R_5 and the ISO224 input impedance.

$$\frac{R_5 || R_{IN,ISO224}}{R_1 + R_2 + R_3 + R_4 + R_5 || R_{IN,ISO224}} = 0.025$$

$$\frac{R_5 || R_{IN,ISO224}}{4M\Omega + R_5 || R_{IN,ISO224}} = 0.025$$

$$R_5 || R_{IN,ISO224} = 102564\Omega = R_{EQ}$$

3. Substituting 1.25MΩ for the ISO224 input impedance and using the following equation, solve for R_5. Use the **analog engineer's calculator** to determine the closest standard value for R_5.

$$R_{EQ} = 102564\Omega = \frac{R_5 \times R_{IN,ISO224}}{R_5 + R_{IN,ISO224}} = \frac{R_5 \times 1.25M\Omega}{R_5 + 1.25M\Omega}$$

$$102564\Omega(R_5 + 1.25M\Omega) = R_5 \times 1.25M\Omega$$

$$R_5 = 111.73k\Omega; \text{closest standard value} = 111k\Omega$$

4. Verify that the equivalent resistance is close to the calculated resistance from step 2.

$$R_{EQ} = \frac{R_5 \times R_{IN,ISO224}}{R_5 + R_{IN,ISO224}} = \frac{111k\Omega \times 1.25M\Omega}{111k\Omega + 1.25M\Omega} = 101.947k\Omega$$

5. Verify that the voltage-divider circuit is within a reasonable error tolerance. For the following calculation, the input resistance of the ISO224 is assumed to be the typical value of 1.25MΩ and this results in an error of 0.6%. However, it is important to consider that the input resistance varies from device to device due to variations in the resistance of the internal clamp protection circuit. If the same calculation is performed using the minimum input resistance of 1MΩ, the error is 2.5%. If this error range is unacceptable then either a calibration must be performed or the resistance of the voltage-divider circuit can be scaled down.

$$\frac{101.947k\Omega}{4.101947M\Omega} = 0.02485$$

$$\text{Error}\% = \frac{|\text{Actual} - \text{Calculated}|}{\text{Calculated}} \times 100 = \frac{|0.02485 - 0.025|}{0.025} \times 100 = 0.6\%$$

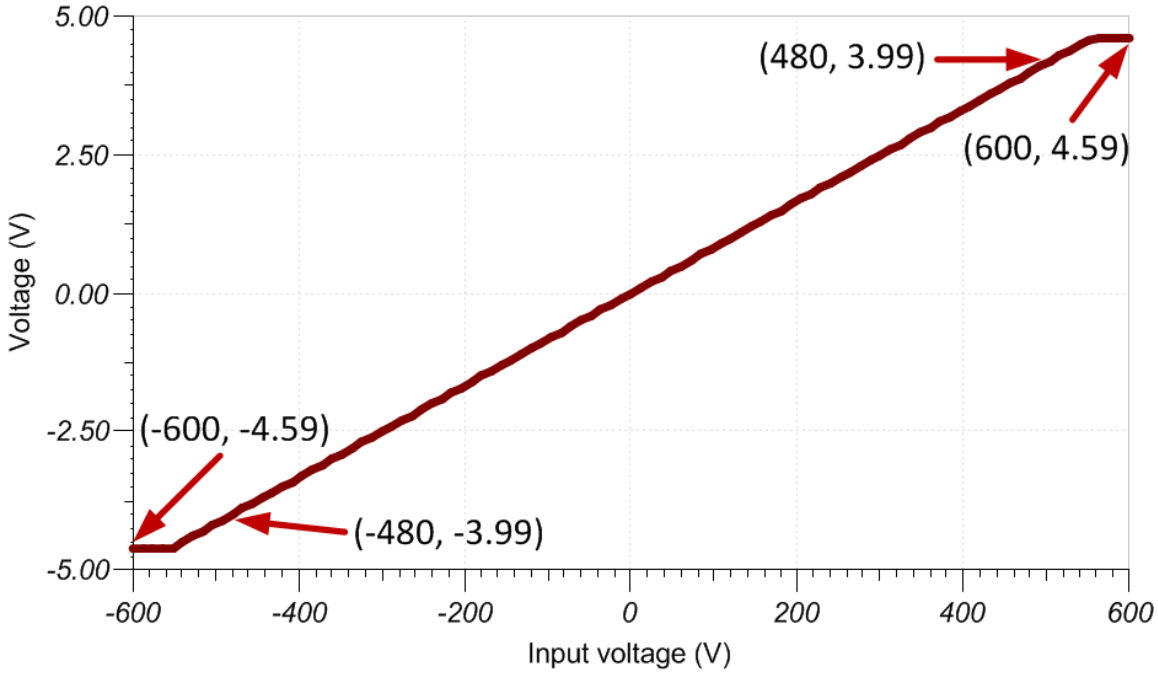
6. Calculate the current flowing through the voltage-divider circuit from the voltage source to make sure that the power dissipation does not exceed the ratings of the resistor. For additional details, see **Considerations for High Voltage Measurements**.

$V = IR;\ \frac{V}{R} = \frac{480V}{4M\Omega + 111k\Omega} = 117\mu A$

DC Transfer Characteristics

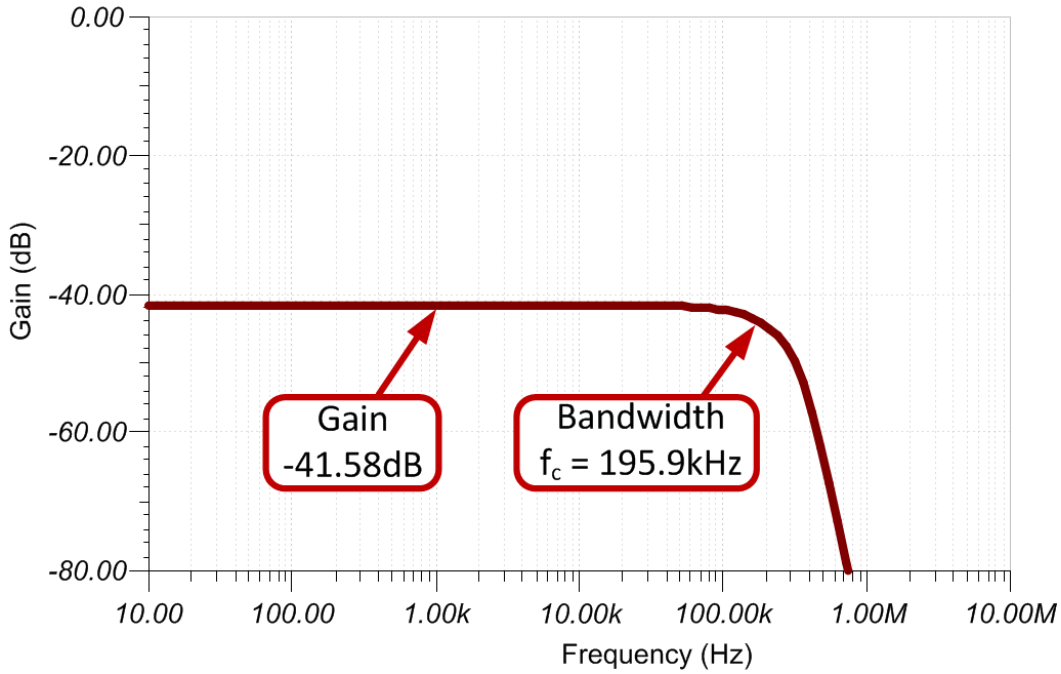
The following graph shows the simulated output for a ±600V input. The voltage divider scales the gain by 1/40, and the ISO224 scales the gain by an additional ⅓.

The transfer function shows the system gain is 1/40 from the voltage divider and ⅓ from the ISO224 (that is, gain × V_{IN} = V_{OUT}, (1/40) × (⅓) × (480V) = 4V).



AC Transfer Characteristics

The simulated gain is –41.58dB (or 0.008337V/V) which closely matches the expected gain for the voltage divider and **ISO224**.



References

1. **Analog Engineer's Circuit Cookbooks**
2. SPICE Simulation File **SBAC232**
3. TI Precision Designs **TIDA-00835**
4. **TI Precision Labs**

Design Featured Isolated Op Amp

ISO224B	
VDD1	4.5V–18V
VDD2	4.5V–5.5V
Input Voltage Range	±12V
Nominal Gain	⅓
V_{OUT}	Differential ±4V on output common mode of VDD2 / 2
Input Resistance	1.25MΩ (typ)
Small Signal Bandwidth	275kHz
Input Offset Voltage and Drift	±5mV (max), ±15µV/°C (max)
Gain Error and Drift	±0.3% (max), ±35ppm/°C (max)
Nonlinearity and Drift	0.01% (max), ±0.1ppm/°C (typ)
Isolation Transient Overvoltage	$7kV_{PEAK}$
Working Voltage	$1.5kV_{RMS}$
Common-mode transient immunity, CMTI	55 kV/µs (min)
ISO224	

Design Alternate Isolated Op Amp

AMC1311B	
VDD1	3V–5.5V
VDD2	3V–5.5V
Input Voltage range	2V
Nominal Gain	1
V_{OUT}	Differential ±2V on output common mode of 1.44V
Input Resistance	1GΩ (typ)
Small Signal Bandwidth	220kHz
Input Offset Voltage and Drift	±1.5mV (max), ±15µV/°C (max)
Gain Error and Drift	±0.3% (max), ±45ppm/°C (max)
Nonlinearity and Drift	0.01%, 1ppm/°C (typ)
Isolation Transient Overvoltage	$7kV_{PEAK}$
Working Voltage	$1.5kV_{RMS}$
Common-mode transient immunity, CMTI	75kV/µs (min)
AMC1311	

EMI Performance

- Best in Class Radiated Emissions EMI Performance with Isolated Amplifiers
- Best Practices to Attenuate AMC3301 Family Radiated Emissions EMI

Best in Class Radiated Emissions EMI Performance with Isolated Amplifiers

Best in Class Radiated Emissions EMI Performance with Isolated Amplifiers

Several industrial and automotive applications require some type of isolation to protect the digital circuitry from the high-voltage circuit performing a function. Texas Instruments has an extensive portfolio of **isolated amplifiers** and **data converters** featuring a capacitive isolation barrier to help customers address their isolated data conversion needs. Texas Instruments' capacitive isolation barrier allows for exceptional reliability, often over 100 years of operation. For more information on TI's capacitive isolation barrier, please review the **Isolation** website.

Radiated emissions testing is common in these applications to verify the system does not produce radiated emissions that exceed the defined levels which may negatively impact other components or circuits in the system. Please see this ***Understanding electromagnetic compliance tests in digital isolators*** marketing white paper for a more in-depth description of EMI. The magnitude of acceptable radiation and testing procedure for radiated emissions is put in place by the Comité International Spécial des Perturbations Radio, also known as CISPR. Industrial applications measure according to the CISPR 11 standard, while automotive applications measure to the CISPR 25 standard. For more information on the CISPR standards and their respective magnitudes over frequency, please see this ***An overview of conducted EMI specifications for power supplies*** marketing white paper.

This document shows the radiated emissions electromagnetic interference (EMI) performance for Texas Instruments' isolated amplifiers, including the **AMC1300B-Q1**, **AMC1300**, **AMC1302**, and **AMC1311** as well as radiated emissions performance for previous isolated amplifier generations.

For radiated emissions EMI guidance for the AMC3301 family, please see this ***Best Practices to Attenuate AMC3301 Family Radiated Emissions EMI*** application note.

Introduction

In isolated amplifiers with a capacitive isolation barrier, radiated emissions can be created when the capacitors that span the barrier are charged and discharged to transmit data in the form of either a 1 or a 0. The charges flow through the differential capacitors in opposite directions mostly canceling each other, however any difference in magnitude or time between these charge flows results in electro-magnetic energy injected between the isolated grounds GND1 and GND2. Because of the nature of the isolation barrier, the energy is unable to find a conductor to return to the source. With no path back to the source, the energy radiates from the device pins (and any traces or PCB planes they are connected to) in the form of radiated emissions. This radiation can extend to frequencies significantly above the amplifier signal bandwidth and data rates, since it is caused by timing mismatches in the pico-second range.

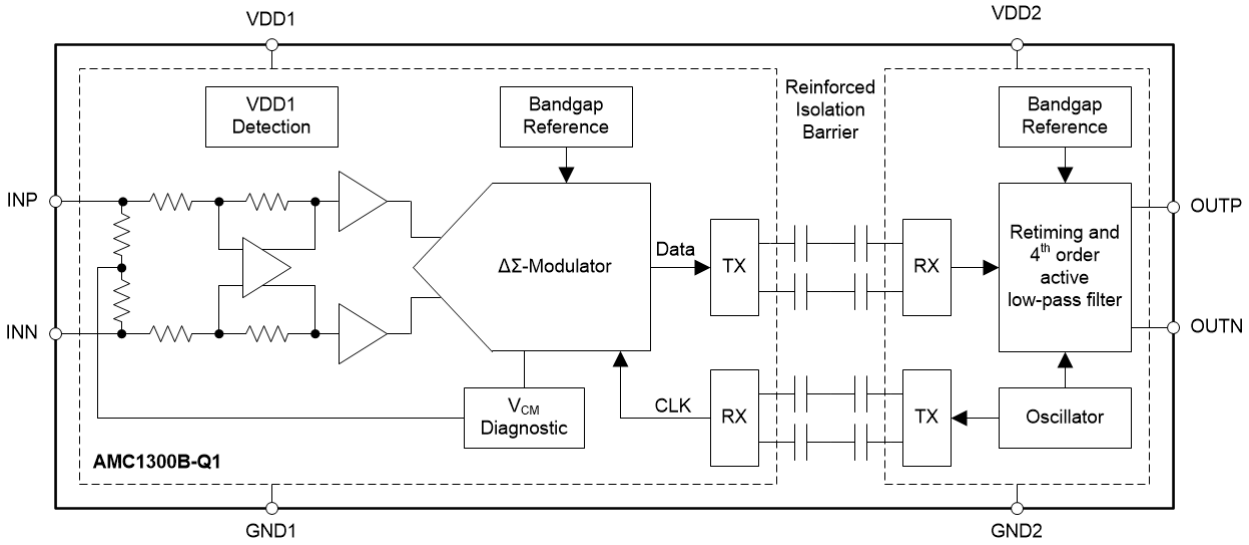


Figure 53. *Isolated Amplifier Block Diagram*

Within the recent years, there have been significant improvements to the architecture of Texas Instruments isolated amplifiers to optimize radiated EMI performance. Beginning in 2018 with the **ISO224**, isolated amplifiers from Texas Instruments began to use on or off keying (OOK) signal modulation compared to previously used pulse coding. The OOK modulation enabled significantly improved Common-Mode Transient Immunity levels. Then in 2020, the **AMC1300B-Q1** was the first isolated amplifier that significantly reduced the amount of energy crossing over the isolation barrier, which reduces the radiated emissions, providing sufficient margins to the standard specifications. These design changes, as well as a re-designed isolated signal path, are now present in the entire Texas Instruments isolated amplifier portfolio, with the exception of the **AMC1100**, **AMC1200**, and **ISO224** devices. The optimized timing and amplitude in the signal chain yields a reduction of radiated emissions EMI at high frequencies to an even lower level.

The following sections show the radiated emissions EMI performance for the Texas Instruments' isolated amplifiers. The current generation of isolated amplifiers radiated emissions performance is shown by using the **AMC1300B-Q1** as an example, while the **ISO224** and **AMC1200** are used to show data for the previous generation devices. The radiated emissions scans were all performed according to the standards set in place by CISPR 11. All tests were performed using the **AMC1300EVM** printed circuit board (PCB) with the inputs shorted to ground, transformer driver (U3) removed, and external 3.6 V batteries with short leads. Each scan shows the horizontal sweep results from the device under test (DUT) in blue as well as the ambient scan overlaid in red to show the noise floor of the chamber. Both CISPR 11 Class A and

Class B limits are shown on the plots as well. The horizontal polarization was selected because the emissions levels detected by the test equipment's antenna were higher than for the vertical polarization, due to alignment with the PCB.

Current Generation of Texas Instruments Isolated Amplifiers Radiated Emissions Performance

The isolated amplifiers from Texas Instruments such as the **AMC1300B-Q1**, **AMC1300**, **AMC1302**, and **AMC1311** incorporate several years of radiated emissions EMI performance advancements, including, but not limited to: an optimized analog signal chain, the amount of energy crossing over the isolation barrier was more closely managed, and OOK data transmission. As shown in **Figure 54**, these devices have excellent radiated emissions EMI performance, with only a few high frequency radiated emissions visible above the noise floor of the chamber. These high-frequency emissions are visible around 820 Mhz with 20 dB of margin and extends to 980 MHz with 16 dB of margin.

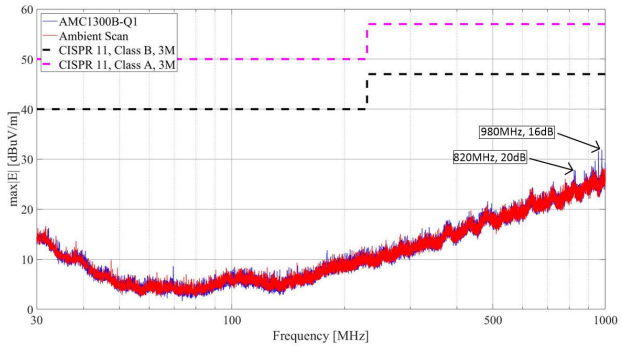


Figure 54. *AMC1300B-Q1 CISPR 11 Radiated Emissions EMI Scan*

Previous Generations of Texas Instruments Isolated Amplifiers Radiated Emissions Performance

Released in 2018, the **ISO224** closely managed the energy crossing over the isolation barrier, and added OOK data transmission. The radiated emissions EMI scan shown in **Figure 55** was performed using the **ISO224** and the emissions are first seen around 540 Mhz with 18 dB of margin and continues to 1 GHz which is the CISPR 11 test limit, with 6 dB of margin at 940 MHz.

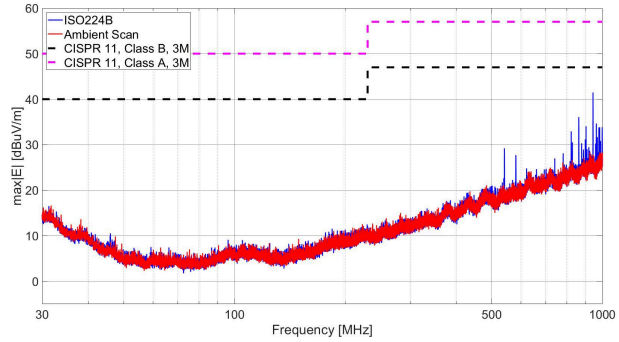


Figure 55. *ISO224 CISPR 11 Radiated Emissions EMI Scan*

Texas Instruments released the **AMC1100** and **AMC1200** isolated amplifiers in 2011. These devices feature a basic isolation barrier and meet the CISPR 11 Class A and Class B standards with sufficient margin.

As shown in **Figure 56**, the **AMC1200** has several radiated emissions peaks above the noise floor, however, there is a significant amount of margin available to the CISPR class B limit shown in black. The noise peaks in the 100 MHz to 230

MHz region have 24 dB of margin from the CISPR11 Class B limit, while the noise peaks in the higher frequency range, 480 MHz to 630 MHz, have 13 dB of margin.

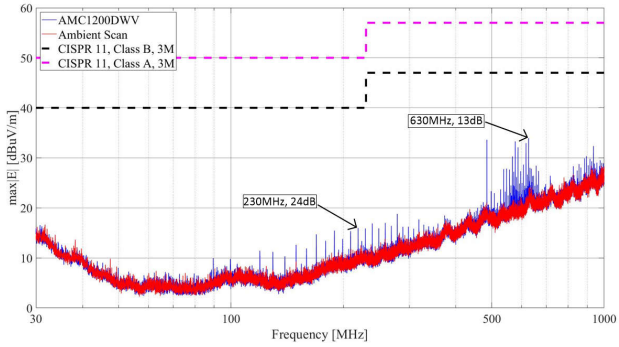


Figure 56. *AMC1200 CISPR 11 Radiated Emissions EMI Scan*

Conclusion

Over the past several years, capacitive isolation has been a popular choice for many customers in need of **isolated amplifiers** and **data converters** due to the long term reliability and strong analog performance. When using the re-designed isolated amplifiers from Texas Instruments, including **AMC1300B-Q1**, **AMC1300**, **AMC1302**, and **AMC1311**, customers can confidently create designs featuring the high reliability and high analog performance that capacitive isolation brings, with best in class radiated emissions EMI performance.

References

- Texas Instruments, ***Understanding Electromagnetic Compliance Tests in Digital Isolators*** application note.
- Texas Instruments, ***An Overview of Conducted EMI Specifications for Power Supplies*** application note.
- Texas Instruments, ***Best Practices to Attenuate AMC3301 Family Radiated Emissions EMI*** application note.

Best Practices to Attenuate AMC3301 Family Radiated Emissions EMI

Abstract

This document demonstrates how printed circuit board (PCB) input trace or cable design affects radiated emissions electromagnetic interference (EMI) performance for Texas Instruments' **AMC3301 precision isolated amplifier with integrated DC/DC converter**. The AMC3301 family as shown in **Table 9** does not produce excessive radiated emissions by themselves and are capable of passing CISPR 11 class B without additional components as shown in **Figure 59** if the length of the input traces connected to the device are short. For designs requiring additional radiated emissions attenuation, ferrite bead and common-mode choke selection and placement recommendations are provided.

Several industrial and automotive applications require some type of isolation to protect the digital circuitry from the high-voltage circuit performing a function. Texas Instruments has an **extensive portfolio** of isolated amplifiers and converters featuring a SiO_2 isolation barrier to help customers address their isolated data conversion needs. Texas instruments' SiO_2 isolation barrier allows for exceptional reliability, often over 100 years of operation. For more information on TI's SiO_2 isolation barrier, please review the **Isolation link**. EMI testing is common in these applications to verify the system does not produce radiated emissions that exceed the defined levels which may negatively impact other components or circuits in the system. Please see this **application note** for a more in-depth description of EMI. The magnitude of acceptable radiation and testing procedure for radiated emissions is put in place by the Comité International Spécial des Perturbations Radio, also known as CISPR. Industrial applications measure according to the CISPR 11 standard, while automotive applications measure to the CISPR 25 standard. For more information on the CISPR standards and their respective magnitudes over frequency, please see this **application note**.

Introduction

The AMC3301 family of devices has two sources of radiated emissions, as shown in **Figure 57**, the capacitive data path shown below in red and the integrated DC/DC converter shown in blue. The radiated emissions performance of the data path is the same as the AMC1300B-Q1 and contributes very little radiated emissions as shown in this **Best in Class Radiated Emissions EMI Performance with the AMC1300B-Q1 Isolated Amplifier** technical write paper. The second and largest source of radiated emissions for the AMC3301 family is the integrated DC/DC converter that operates at a frequency of 30 MHz with spread spectrum modulation. The coils of the internal DC/DC converter have a parasitic capacitance from the primary (user) side to the secondary (high) side of the isolation barrier. The primary driver generates a common-mode voltage between the isolated grounds, HGND and GND that has a quasi-resonant nature and generates harmonics to higher frequencies. Because of the nature of the isolation barrier, the energy is unable to find a conductor to return to the source. With no path back to the source, the energy radiates from the device pins (and any traces or PCB planes they are connected to) in the form of radiated emissions.

Input traces and cables that are connected to the isolated amplifier or converter act as antennas for the electro-magnetic energy injected between HGND and GND. The size and shape of the traces and cables directly affect the magnitude of the radiated emissions over frequency. As a general rule, shorter antennas radiate more effectively at higher frequencies, while longer antennas radiate more effectively at lower frequencies. When designing with the AMC3301 family, input traces and cables should be kept as short as possible to limit the magnitude of radiated emissions.

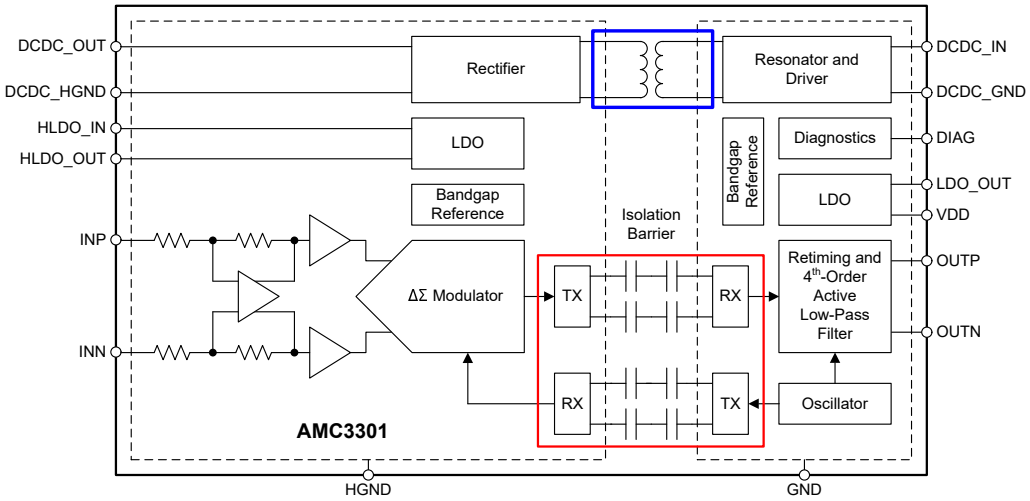


Figure 57. *AMC3301 Isolated Amplifier Block Diagram*

Effects of Input Connections on AMC3301 Family Radiated Emissions

CISPR 11 peak measurements were performed with various input cable lengths and Texas Instruments' AMC3301. The input cable lengths tested are a 1.5 m input, a 30 cm input and an input shorted at the input terminal of the evaluation module (EVM). The same **AMC3301EVM** was used for all tests and powered from an external battery. All measurements shown are in the horizontal, or worst-case, orientation. Refer to the test setups in **Figure 58** and CISPR 11 radiated emissions EMI plots in **Figure 59** and **Figure 60**.

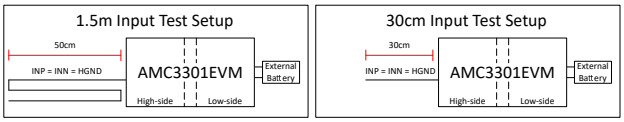


Figure 58. *Test setup with AMC3301EVM and Input Lengths*

Figure 59 shows the radiated emissions performance of the AMC3301 with an input short shown in blue. The AMC3301 shows very little radiated emissions above the noise floor in red – demonstrating that the AMC3301 does not produce excessive radiated emissions if the input traces or cables to the device are short.

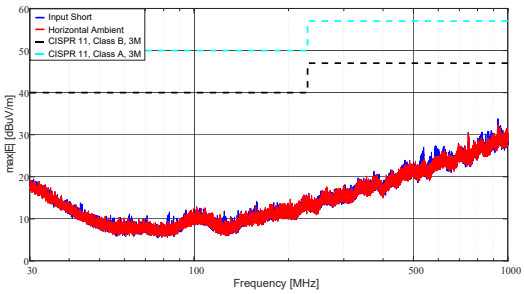


Figure 59. *AMC3301EVM Input Short and Horizontal Ambient CISPR 11 Measurement*

Figure 60 shows the radiated emissions measurement for the 1.5 m input in blue, 30 cm in red and input short in green. Longer input traces and cables connected to the AMC3301 increase the magnitude of radiated emissions as shown by the 1.5 m input and 30 cm input test cases compared to the input short.

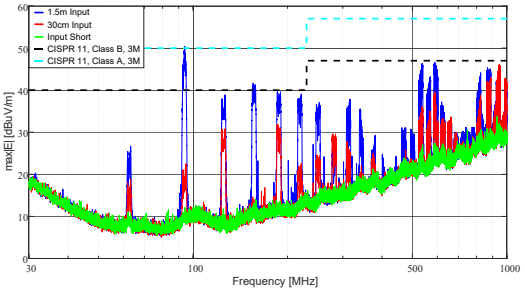


Figure 60. *AMC3301EVM with Different Input Lengths CISPR 11 Measurement*

Attenuating AMC3301 Family Radiated Emissions

Ferrite Beads and Common Mode Chokes

Designers need to limit the length of the input traces or cables connected to the AMC3301 family. However, some applications will require longer input traces or cables which will lead to excessive radiated emissions. This radiation can be attenuated by using ferrite beads or a common-mode choke in series with the input connections. When selecting a ferrite bead or common-mode choke, refer to the impedance over frequency plot in the components' data sheet. A minimum of 1 kΩ ohm impedance (z) is recommended over the frequency range of interest, 150 MHz to 800 MHz for CISPR 11, with higher impedances attenuating radiated emissions more effectively. **Table 8** lists recommended ferrite beads and a common-mode choke.

Table 8. Ferrite Bead and Common-mode Choke Recommendations

Type	Manufacturer	Part Number
Ferrite Bead	Wurth Elektronik	74269244182
Ferrite Bead	Murata	BLM15HD182SH1
Ferrite Bead	Taiyo Yuden	BKH1005LM182-T
Common-mode Choke	Murata	DLW31SN222SQ2

To demonstrate the benefits of adding the ferrite beads or a common-mode choke for the 1.5 m input and 30 cm input, refer to **Figure 61** and **Figure 62** respectively. The 74269244182 ferrite bead from Wurth Elektronik and DLW31SN222SQ2 common-mode choke from Murata were added in series to the input connections for these tests.

Figure 61 shows the radiated emissions of the 1.5 m input. Without ferrite beads or a common-mode choke is shown in blue and the CISPR 11 class B limit is violated. The attenuating benefit of the ferrite beads is shown in red and the common-mode choke in green. Both the ferrite beads and common-mode choke significantly attenuate the radiated emissions, allowing the AMC3301EVM to pass the CISPR 11 class B test.

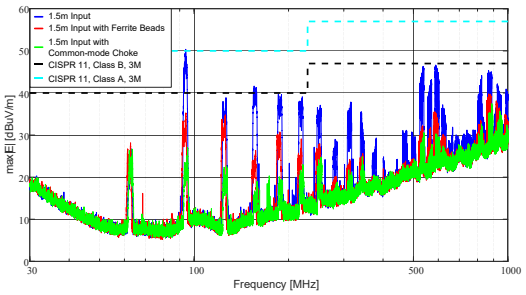


Figure 61. *AMC3301EVM CISPR 11 Measurements with 1.5 m Input*

Figure 62 shows the radiated emissions of the 30 cm input. All test cases pass the CISPR 11 class B test, including without ferrite beads or a common-mode choke as shown in blue. This indicates that additional components are not necessary to pass the test, but to demonstrate the attenuating benefits, the measurements with ferrite beads are shown in red and the common-mode choke in green.

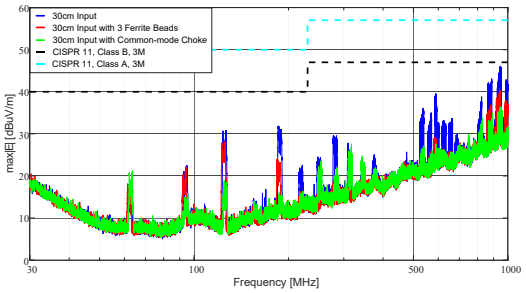


Figure 62. *AMC3301EVM CISPR 11 Measurements with 30 cm Input*

PCB Schematics and Layout Best Practices for AMC3301 Family

Figure 63 shows the schematic for the ferrite beads on the left and the common-mode choke on the right. Note that three ferrite beads are required, one for each input as well as one for the HGND trace to the shunt resistor. The common-mode choke has two channels and terminating the HGND connection to VINN near the common-mode choke is necessary. The differential RC filter created by R2, R4 and C12 is placed between the ferrite beads or common-mode choke and the AMC3301. Refer to the layout guidelines section in the device's data sheet for additional detail.

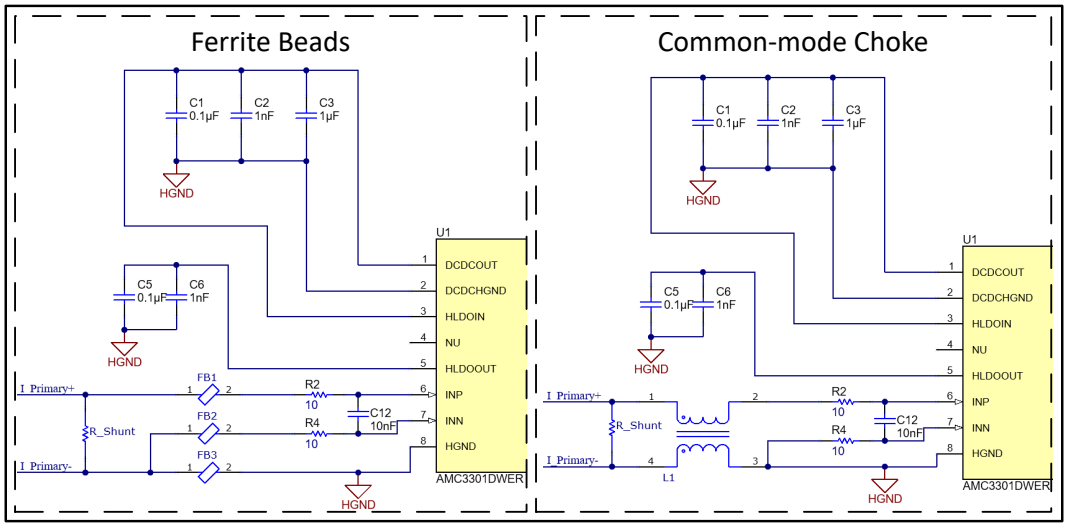


Figure 63. *AMC3301 Ferrite Bead and Common-mode Choke Schematics*

The ferrite beads or common-mode choke should be placed as close to the device as possible to limit the amount of copper area that will act as an antenna. A direct and low inductance connection should be made from pin 2 (DCDC_HGND) to pin 8 (HGND). **Figure 64** shows the recommended layouts for the ferrite beads on the left and the common-mode choke on the right.

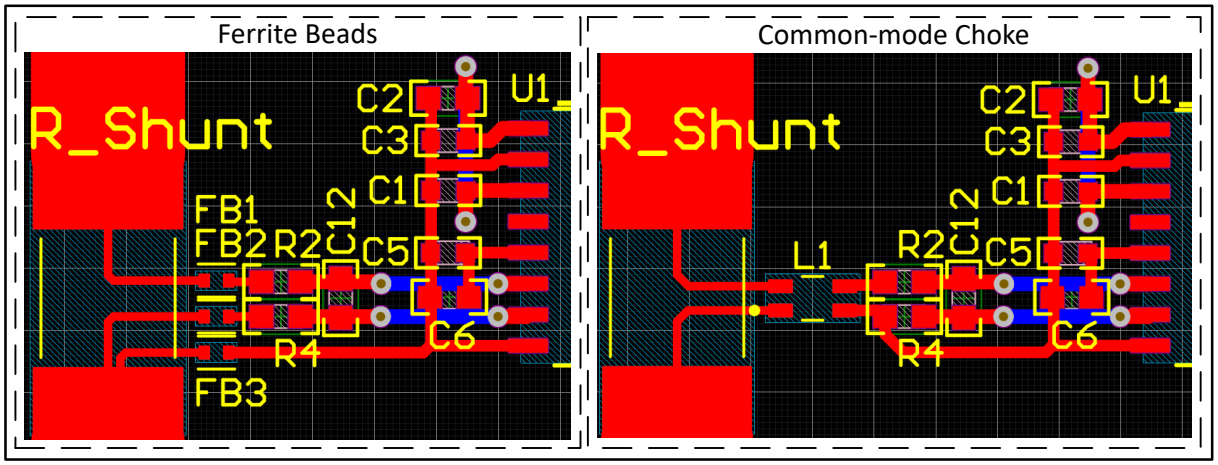


Figure 64. *AMC3301 Ferrite Bead and Common-mode Choke Layouts*

Using Multiple AMC3301 Devices

Device Orientation

As mentioned previously, the coils of the internal DC/DC converter have a parasitic capacitance from the primary side to the secondary side of the isolation barrier, and the energy radiates from the device pins, and traces connected to pins. As a result, it is important to consider how the AMC3301 family will radiate and affect other devices along the isolation barrier, including other AMC3301's.

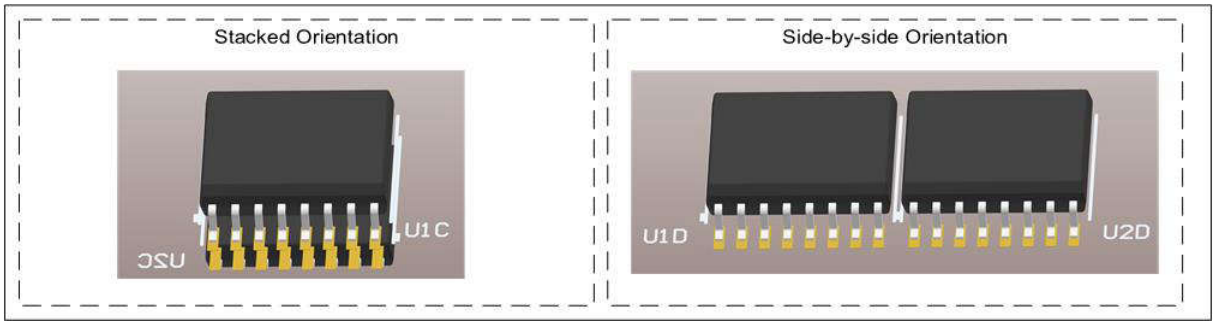


Figure 65. *Device orientation examples*

To demonstrate the effects of device orientation, a stacked orientation and side-by-side orientation are tested. The schematic used in testing is the same as the ferrite section of **Figure 65**. The input ferrite beads part number is 74269244182, and they were tested with 1.5 m input shorted together.

Figure 66 shows the orientations will meet the CISPR 11 class B limit as a result of the ferrite beads discussed previously. The stacked orientation is in red while the side-by-side orientation is in blue. In addition, the orientations fall within 5 dBuV/m of each other. However, placing both devices right on top of each other-in a stacked orientation-shows the best performance.

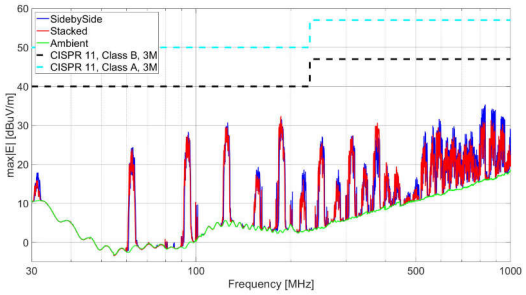


Figure 66. *Multiple AMC3301 CISPR 11 Measurements with 1.5 m Input*

PCB Layout Best Practices for Multiple AMC3301

The schematic used in testing is the same as the ferrite section of **Figure 67**. However, layout for stacking the AMC3301's is shown in **Figure 67**.

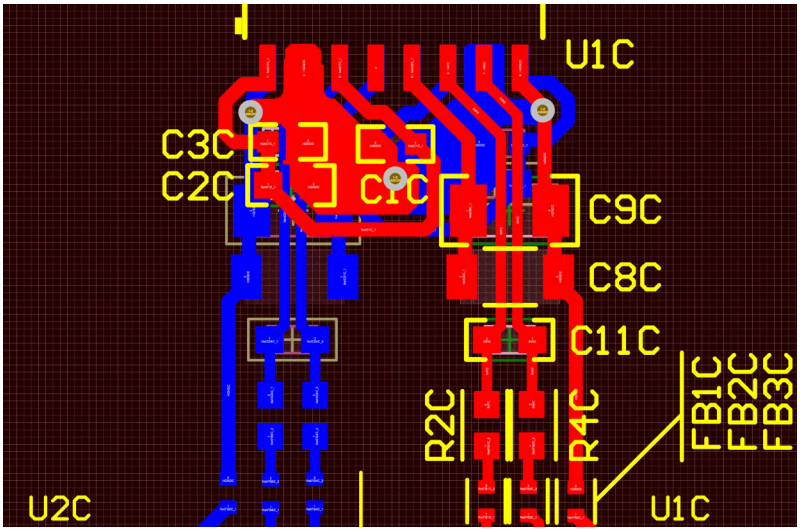


Figure 67. *Recommended Multiple AMC3301 Devices Layout*

In general, the same layout principles described in **Section 6.2.3.2** are followed with a two layer board design.

However, a direct and low inductance path from pin 2 (DCDC_HGND) to pin 8 (HGND) of each device is achieved differently. Instead of a trace, a star connection connects both devices between the top and bottom layers at pins 4 and 5. In addition, a pool of copper is used to connect the DC/DC capacitors to DCDC_HGND on the same layer.

Finally, the LDO_OUT capacitors are scaled up to a 1206 package to allow direct and uninterrupted path for the positive and negative inputs underneath the capacitors.

Conclusion

Over the past several years, SiO_2 isolation has been a popular choice for many customers in need of isolated amplifiers. Texas Instruments continues to innovate and recently released the **AMC3301 precision isolated amplifier with integrated DC/DC converter**. The AMC3301 family does not produce excessive radiated emissions by itself and is capable of passing CISPR 11 class B without additional components if the length of input traces or cables are short. Ferrite beads or a common-mode choke can be used to further attenuate radiated emissions if desired. AMC3301 devices can be stacked on top of each other on the top and bottom layers if multiple are used. When designing with

the AMC3301 family, customers can confidently create designs featuring the high reliability and high analog performance that capacitive isolation brings, while enjoying the convenience of an integrated DC/DC converter and best in class radiated emissions performance.

AMC3301 Family Table

The content discussed in this application note is applicable to all **isolated amplifiers** and **isolated converters** with integrated DC/DC converter in the AMC3301 family, listed in **Table 9**.

Table 9. AMC3301 Family Table

Device	Type	Description
AMC3301	Reinforced Isolated Amplifier	Current Sensing, ±250-mV Input
AMC3301-Q1	Reinforced Isolated Amplifier	Current Sensing, ±250-mV Input, Automotive
AMC3302	Reinforced Isolated Amplifier	Current Sensing, ±50-mV Input
AMC3302-Q1	Reinforced Isolated Amplifier	Current Sensing, ±50-mV Input, Automotive
AMC3330	Reinforced Isolated Amplifier	Voltage Sensing, ±1-V Input
AMC3330-Q1	Reinforced Isolated Amplifier	Voltage Sensing, ±1-V Input, Automotive
AMC3306M25	Reinforced Isolated Modulator	Current Sensing, ±250-mV Input
AMC3306M05	Reinforced Isolated Modulator	Current Sensing, ±50-mV Input
AMC3336	Reinforced Isolated Modulator	Voltage Sensing, ±1-V Input
AMC3336-Q1	Reinforced Isolated Modulator	Voltage Sensing, ±1-V Input, Automotive

End Equipment

- Comparing Shunt- and Hall-Based Isolated Current-Sensing Solutions in HEV/EV
- Design Considerations for Current Sensing in DC EV Charging Applications
- Using isolated comparators for fault detection in electric motor drives
- Discrete DESAT for Opto-Compatible Isolated Gate Driver UCC23513 in Motor Drives
- Isolated voltage sensing in AC motor drives
- Achieving High-Performance Isolated Current and Voltage Sensing in Server PSUs

Comparing Shunt- and Hall-Based Isolated Current-Sensing Solutions in HEV/EV

Introduction

The global market for electric vehicles (EVs) and hybrid electric vehicles (HEVs) is rapidly growing as these vehicles offer higher fuel-efficiency and lower emissions compared to gasoline or diesel vehicles and use power from renewable energy sources. To control energy flow and optimize efficiency in HEV/EV powertrain subsystems such as traction inverters, on-board chargers (OBCs), DC/DC converters, and battery management systems (BMS), precise and accurate current measurement is essential. These high-voltage subsystems must measure large currents at high voltages, typically >400 V. Thus, these current measurements require isolation as well as high performance in harsh automotive environments.

Different Isolated Current Measurement Methods

Each HEV/EV application has different cost, accuracy, signal bandwidth, latency, measurement range, isolation ratings, and package size requirements. There are several isolated current measurements methods. However, the primary methods used in HEV/EV subsystems are either shunt-based using isolated amplifiers (**Figure 68**) or isolated modulators (**Figure 69**) or hall-based using open-loop (**Figure 70**) or closed-loop (**Figure 71**) hall sensors.

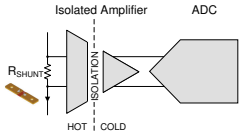


Figure 68. *Isolated Amplifier*

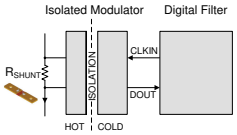


Figure 69. *Isolated Modulator*

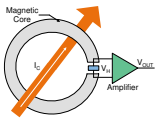


Figure 70. *Open-Loop Hall Sensor*

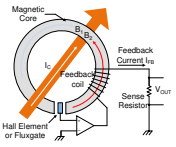


Figure 71. *Closed-Loop Hall Sensor*

Comparison of Shunt- and Hall-Based Methods

Historically, designers preferred shunt-based solutions for low-current (<50 A), and hall-based solutions for high-current (>50 A) measurements. However, because of the increasing current measurement accuracy requirements, automotive suppliers are migrating from hall-based to shunt-based methods, especially in high-current environments. There is even a trend amongst automotive suppliers to move from isolated amplifier based solutions to isolated modulator based solutions to further improve measurement accuracy.

Texas Instruments offers best-in-class **isolated amplifiers** and **isolated modulators** that help achieve very accurate isolated current measurements over temperature when paired with high-precision shunts. **Table 10** shows the basic differences between shunt- and hall-based isolated current-sensing solutions in high-current automotive environments.

Table 10. Difference Between Shunt- and Hall-Based Isolated Current Sensing

CATEGORY	SHUNT-BASED	HALL-BASED
Solution size	Similar	Similar
offset	Very low	Medium
Offset drift over temperature	Low	Medium
Accuracy	<0.5% after calibration	<2% after calibration
Noise	Very low	High
Bandwidth	Similar	Similar
Latency	Similar	Similar
Nonlinearity	Very low	High
Long-term stability	Very high	Medium
Cost	Similar	Similar
Vibration impact	Very low	Low
Power dissipation	Low	Very low
Customization	Flexible	Limited

Analysis of Shunt- and Hall-Based Methods

- Hall-sensors are inherently isolated, which allows a single-module approach. On the other hand, shunt-based solutions require an isolated amplifier or modulator, and an isolated power-supply for the high common-mode voltage side.
- Shunt-based solutions have very low initial offset, have lower offset drift over temperature, and are less susceptible to external magnetic fields.
- Shunt-based solutions are linear over the entire voltage range compared to hall-based solutions that are nonlinear, especially at zero crossing and near the magnetic core saturation region.
- Shunt-based solutions achieve better DC accuracy over temperature compared to hall-based solutions with basic one-time calibration. The accuracy of shunt-based solutions is much better particularly at low currents because of limited sensitivity to external magnetic fields.
- The voltage drop across the inline shunt results in thermal dissipation and power loss. However, with improvements in shunt technology, the shunts have become lighter, the ohmic values have decreased, and the accuracy and drift performance have improved. The use of low-value ohmic shunts results in less thermal dissipation. Additionally, Texas Instruments' isolated amplifiers and modulators support very small input voltage ranges (±50 mV and ±250 mV) with a superior overall accuracy. These improvements in shunt technology and the availability of small input range isolated devices allow systems to have less thermal dissipation without compromising the overall measurement accuracy.
- Hall-based sensors generally have a limited operating temperature range (typically from –40°C to +85°C), whereas shunt-based solutions can support higher operating temperature ranges (typically from –40°C to +125°C).
- Both hall-based and shunt-based isolated amplifier solutions offer similar signal bandwidth, typically up to a few hundred kilohertz (kHz). However, isolated modulators provide a high-speed bit-stream output that allows the user to implement and customize digital filtering externally. This customization allows the user to develop high-signal bandwidth and low-latency solutions.

Isolated Shunt-Based Current Sensing in Traction Inverters

A traction inverter controls the electric motor and is a key component in the HEV/EV drivetrain. A traction inverter requires accurate current sensing at high common-mode voltages. Current measurements in traction inverters can therefore be realized using one of two shunt-based methods.

Figure 72 shows the voltage drop across the shunt on the hot (high common-mode voltage) side is isolated from the cold side with an automotive grade, reinforced isolated amplifier such as the **AMC1301-Q1**.

Figure 73 shows the second shunt-based measurement method that uses an automotive-grade, reinforced isolated modulator such as the **AMC1305M25-Q1** to isolate the voltage drop across the shunt on the hot side from the cold side.

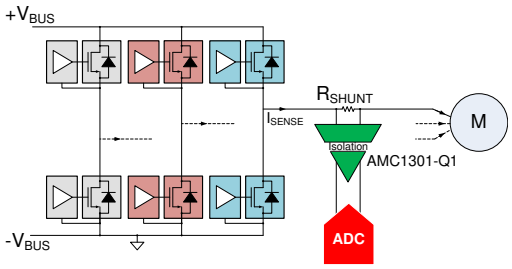


Figure 72. *Isolated Current Measurement Using Isolated Amplifiers*

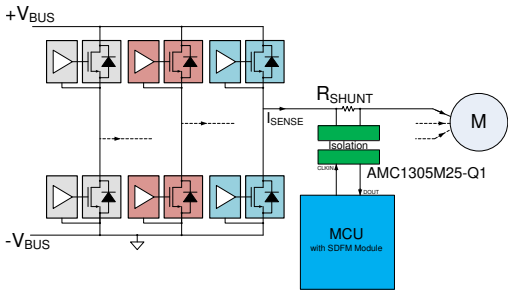


Figure 73. *Isolated Current Measurement Using Isolated Modulators*

For improved measurement accuracy, use an isolated modulator because this solution eliminates an additional analog-to-digital conversion stage and the associated subsequent errors. The high-speed bit-stream output from the isolated modulators is filtered by microcontrollers (MCUs) such as TI's **C2000 family** that have a built-in sigma-delta filter module (SDFM) or by an FPGA, allowing the user to fine-tune signal bandwidth and accuracy.

Automotive Isolated Device Recommendations

DEVICE	ISOLATION	DESCRIPTION
AMC1305-Q1	Reinforced	±50-mV, ±250-mV isolated modulator
AMC1301-Q1	Reinforced	±250-mV isolated amplifier
AMC1302-Q1	Reinforced	±50-mV isolated amplifier

Conclusion

Multiple measurement methods exist for isolated current sensing in HEV/EV subsystems including shunt-based and hall-based methods. With advancements in affordable high-precision shunts and high-performance isolated amplifiers and modulators, shunt-based solutions have become good alternatives to traditional hall-based solutions.

Design Considerations for Current Sensing in DC EV Charging Applications

Abstract

The shift from combustion engines to electric vehicles (EVs) seems inevitable as governments around the world commit to environmental sustainability goals and the automotive industry plans to invest more to accelerate vehicle electrification. The capacity of DC fast-charging stations has increased significantly in recent years. Where the standard was once 150 kW, capacities are now 350 kW and beyond — and the improvements continue. To get to 350 kW and above, a common technology is to stack modules with 20 kW to 40 kW in parallel and perform load balancing of those modules in parallel in a higher level control loop. The current and voltage-sensing technology plays an essential role in the power module control loop of DC fast-charging stations. This application report looks into design considerations for current sensing in EV charging applications, especially with a focus on the gain error, offset, bandwidth, and latency concerning system performance.

Introduction

DC Charging Station for Electric Vehicles

To supply or drain the power from the vehicle battery to the grid, multiple conversion stages are necessary between the AC and the DC rails, as **Figure 74** shows.

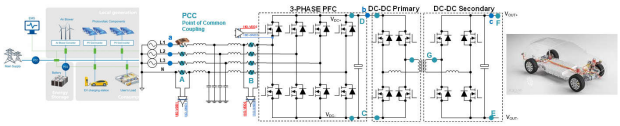


Figure 74. *Current Sensing Points of an EV Charging System*

AC/DC converters are responsible to convert AC into DC power by keeping under control the current Total Harmonic Distortion (THD) on the Point of Common Coupling (PCC) together with the DC voltage. At the same time, isolated DC/DC converters are mainly used for galvanic isolation between the grid and the car and to achieve Constant Current (CC) and Constant Voltage (CV) charging functionalities.

Figure 74 depicts typical current sensor locations of an EV charging system.

- Power regulation and protections of the AC/DC stage are achieved by means of sensors placed in point A, B, C, and D:
  - **Point A** is the main connection point of the converter toward the PCC. By placing sensors at this location, the currents pushed into or pulled from the grid can be most accurately monitored and controlled, thereby achieving accurate control of active and reactive powers interchanged with the grid.
  - **Point B** has the capability to measure the switch current in the Switching Node (SN). By placing the current sensors in this location, protection of power switches and control loop speed can be improved. Furthermore, when an isolated power supply is required by the current sensing circuit, gate driver supply can be leveraged, thus reducing the total cost of the design. However, the measurement does not include the losses in the EMI filter, therefore this location is less suitable for reactive power compensation.
  - **Point C** is the measurement point of the DC bus current. Placement of the current-sensing circuit in this location allows cost reduction when the power supply is shared with the bottom switch-driver supply.
  - **Point D** is the measurement point of the DC bus current placed on the positive rail of the DC bus.

- Power regulation and protection of the DC/DC stage are achieved by means of sensing placed in point G, F, and E.
  - **Point G** is required to control the windings currents.
  - **Point F** is the measurement point of the battery current located on the positive terminal.
  - **Point E** is the measurement point of the battery current located on the negative terminal. The benefit of sensing the current flowing to the negative terminal is that the gate-driver supply of the low-side FET can be leveraged for powering the current-sensing circuit.

In this application note, a study based on simulation results was conducted with the aim to define the minimal specifications required by the current sensors when used in DC charging applications for EVs. Optimal values of bandwidth, gain error, offset, and latency were derived for an 11-kW system presenting the system specifications listed in **Table 11**. Two different isolated DC/DC topologies are considered in this document: DAB (Dual Active Bridge) with phase-shift control and DAB with CLLLC resonant converter.

Section 7.2.2 discusses design considerations for AC/DC input current sensing Point A and B respectively with DC link current measurements in C and D. **Section 7.2.3** details the requirements for the current sensing points in the DC/DC stage (G, F, E) in how proprieties as bandwidth, gain and offset errors impact the performance of the DC/DC stage.

Table 11. Target Specifications for EV Charger

Condition	Description
Power ratings and power flow	11-kW bidirectional operation to support V2G/V2H
AC ratings	400 V_{AC} (3-phase each 230 V_{AC}) 16 A_{RMS} (each phase)
Total harmonic distortion of AC current	3.6% at PCC at full load
DC Ratings	V_{DCBUS} 800 V nominal (from 650 V to 800 V) I_{DCBUS} 14 A (from 14 A to 17 A) V_{BAT} 400 V (from 250 V to 450 V) I_{OUT} 27.5 A (from 24 A to 44 A)
Switching frequency of AC/DC	70 kHz (dead-time = 250 ns)
Switching frequency of DC/DC	100 kHz for phase-shifted DAB 500 kHz nominal for resonant CLLLC DAB
Accuracy required by the power controlled in the DC side	V_{DCBUS} ±1% V_{BAT} ±1% I_{BAT} ±1%
Implemented AC/DC bandwidths of the current and voltage loops	3-kHz grid current loops (id, iq) 400-Hz DC bus voltage loop
Implemented bandwidths of the voltage measurements: grid and DC link	100 kHz

Current-Sensing Technology Selection and Equivalent Model

Sensing of the Current With Shunt-Based Solution

In this application note, only shunt-based current sensing with isolated amplifiers or isolated delta-sigma modulators are considered. All products discussed have a linear input voltage range of ±50 mV which allows use of very small shunt-resistor values to keep power a low energy dissipation compared to the overall power of the system.

In the reference application, for an 11-kW AC/DC, the input currents have a maximum value or 16 A_{RMS} for 400 V_{AC} three-phase system. This results in ±22.5 A_{peak}. With a 2-mΩ shunt resistor, the maximum voltage across the shunt can be kept well below 50 mV (peak is 45 mV), meaning that at maximum power operation of 11 kW the power dissipation within the shunt is only 0.5 W per shunt. Assuming three shunts in a 3-phase system this is still negligible loss and

does not add any important hot spot on the PCB. Conversely, the currents in the DC/DC converter can be as high as 44 A as indicated in **Table 11**. This result drives the requirements to select a 1-mΩ shunt resistor for the 50-mV input voltage range of the isolated amplifier which results in a power dissipation lower than 2 W for each measurement point (negligible with respect to 11-kW total power).

Equivalent Model of the Sensing Technology

The analysis of each current-sensing point is done at a system level by considering four parameters: bandwidth, latency, gain error, and offset. **Figure 75** shows an equivalent model of the current sensing by showing all the mentioned parameters of the sensor.

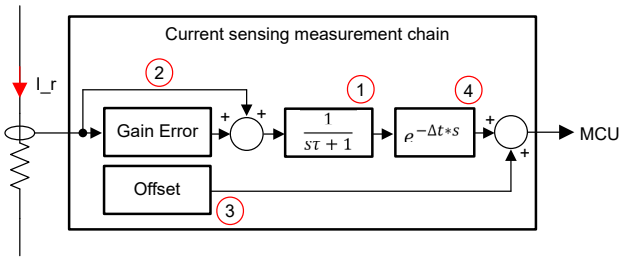


Figure 75. *Current Sensing Measurement Model*

A description of each single stage of the equivalent model follows:

1. Represents the bandwidth limitation presented by the current sensor. In this note, the sensing stage has been modeled as a first-order low-pass filter, where the constant time can be described as follows:

$$\tau = 1/(2\pi f_b) \quad (38)$$

where

- τ is the bandwidth of the current sensor

2. Represents the gain error and is modeled as follows:

$$i_m = (1 + \varepsilon) i_r \quad (39)$$

where

a. i_r is the real current
b. ε is the gain error of the sensor
c. i_m is the measurement

3. Represents the offset which in this study was defined with respect to the measurement range. The offset is represented as a percentage of the full-scale range.
4. Represents the time delay introduced by sensing stage, which becomes critical when overcurrents and short-circuits need to be detected as fast as possible.

Current Sensing in AC/DC Converters

Basic Hardware and Control Description of AC/DC

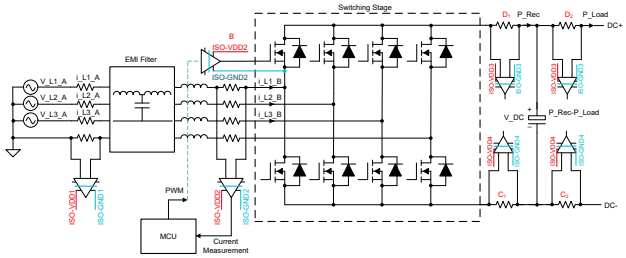


Figure 76. *Schematic Representation of a Two-Level AC/DC Converter*

Figure 76 illustrates a typical AC/DC converter. The following list describes each part of the converter:

- EMI filter used for mitigating the electromagnetic noise generated by the converter and to be compliant to the standards [7]
- Current sensors and voltage sensors (not represented in the scheme) on both the AC and DC side used for monitoring, control, and protection of the power converter
- Switching stage used for conversion of the power from AC to DC, which can be realized by using multiple topologies such as T-Type and ANPC converters [8, 9]
- Microcontroller used for taking the measurements and calculating the PWM duty cycles for the switches in the power stage to have controlled currents synchronous with the grid voltages

Section 7.2.2.1.1 and **Section 7.2.2.1.2** provide descriptions of the control routines executed internally by the microcontroller. The correlation between the current-sensing parameters and the digital control loops is described in detail.

AC Current Control Loops

Controlled power conversion between AC and DC is achieved by synchronizing the control unit with the grid frequency, achieving controlled amplitude and phase of the currents drained by the grid. To get the MCU synchronized with the grid, grid voltages (V_L1_A, V_L2_A, V_L3_A) are sampled by the MCU and fed to a phase-locked loop (PLL) [11] . By using the outcomes of the PLL (cos(φ), sin(φ)), plus Clarke and Park transforms, the three-phase system can be controlled by using the rotating frame reference technique (dq frame control), which allows the control to be simplified and improved.

Figure 77 is a schematic representation of the current control loop implemented in an AC/DC by using the rotating frame where measured Id and Iq can be derived by applying the Clarke and Park transformation to either I_L1_A, I_L2_A, I_L3_A or I_L1_B, I_L2_B, I_L3_B.

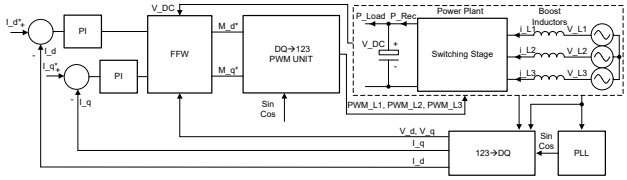


Figure 77. *dq Current Control (Feedforward, PI Proportion Integral Control)*

Figure 77 illustrates that the currents can be controlled by means of two PI controllers:

- By changing the reference current called direct current (I_d*), the three-phase currents can be controlled in phase with respect to the corresponding grid voltages. This feature allows a direct control of the active power drained or sourced by the AC/DC, as represented in **Equation 40**, where P_Rec is the three-phase active power. Changing the sign of the reference current makes it possible to drain and source power correspondingly.
- By changing the reference current called quadrature current (I_q*), the three-phase currents can be controlled 90° phase shifted with respect to the corresponding grid voltages. By changing this value, a direct control of the reactive power can be achieved, as shown in **Equation 41**, where Q is the total three-phase reactive power. By changing the sign of the reference current, it is possible to change the capacitive or inductive power drained by the equipment.

$$\mathrm{P\_Rec} = {}^{3}\!/_{2} V_d I_d^* \tag{40}$$

$$Q = {}^{3}\!/_{2} V_d I_q^* \tag{41}$$

In addition to the PI controllers, feedforwards (FFW) are typically implemented in the current loops to decrease the response time and remove dependencies of the control loop bandwidths when variables in the system change (for example, if V_DC is not compensated, when V_DC decreases, control loop bandwidth can increase causing possible instabilities).

DC Voltage Control Loop

In multiple applications, the load or source connected on the DC side of the rectifier stage is not always behaving as a voltage source, indeed the load can act as resistor or current sink or source. When no voltage source behavior is presented by the DC/DC stage, a dependency on the DC bus voltage with the requested power (P_Rec) can lead to no controlled voltage in the output. An uncontrolled DC bus voltage can cause the AC/DC to become unstable, triggering possible current and voltage protections or even damaging the converter itself. To address this, implement an additional control with a higher hierarchical level, with respect to the current loops, as **Figure 78** shows. A voltage control loop which has the capability to control the active power drained or sourced from the grid by means of I_d* of the lower level control loop Idq was added. The additional PI controller generates a reference (I_d*), which allows matching the rectifier and the load powers (P_Rec and P_Load), by achieving V_DC* equal to V_DC since no power is flowing in the DC-link cap. The matching between the rectifier power and load power is achieved by means of the integrative part.

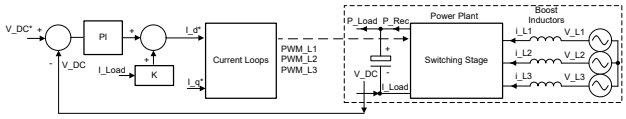


Figure 78. *Voltage Plus Current Control Loops*

As **Figure 78** shows, a feedforward which can be achieved by means of a DC current measurement was implemented to decrease the response time of the loop. A generic factor, K, was implemented since this factor is dependent on the voltages, currents, and control technique implementation. This feature is not critical for the converter operation itself but can improve the performance significantly as demonstrated in **Section 7.2.2.3**.

The I_q* reference is independent from the voltage loop since the reference is not involved in the active power regulation, thus in the charging and discharging process of the DC-link cap. As previously mentioned, I_q* directly controls the reactive power of the system.

Point A and B – AC/DC AC Phase-Current Sensing

This section describes design considerations of current sensors placed in the point of common coupling (point A) or switching node (point B). Investigation results of the control loop performances mentioned in **Section 7.2.2.1** when sensing parameters are changed are provided.

Offset, bandwidth, gain error, and latency of the current sensors are discussed at a system level with the aim to determine the minimum requirements. Not all scenarios are covered for both points A and B since many cases turned out to be a repetition, only the worst cases are described to determine minimum requirements. The following list shows all the details about the analysis of each current-sensor specification:

- **Sensor Bandwidth**: Analysis was conducted on both points A and B. In point A because the phase error needs to be negligible for the reactive power control. In point B because the AC currents need to be controlled as fast as possible.
- **Highest Latency**: Analysis was conducted only in the switching node because point B is the closest point to the power switches which require protection. Furthermore, between point A and B there is an EMI filter which can create a mismatch between the current present from the switching node with respect to the PCC.
- **Gain Error**: The impact of gain error is the same in both PCC and switching node. The analysis was conducted in the switching node because in point B higher current control loop bandwidth can be achieved, leading to a higher THD of the current when accuracy error is present. Subsequently, when the higher bandwidth is present in the system, the voltage loop injects noise in the grid currents.
- **Offset Error**: The impact of offset error is the same in both PCC and switching node. The analysis was conducted in the switching node because the switching node is the place where higher current control loop bandwidth can be achieved, leading to a higher THD of the current when an offset is present.

Impact of Bandwidth

Steady-state and transient analyses were conducted with the aim to observe the control-loop performance as a function of the current sensor bandwidth, defining the minimum bandwidth.

Steady State Analysis: Fundamental and Zero Crossing Currents

In this analysis, grid currents are controlled in the switching nodes (point-B) and a typical profile of the controlled currents are shown in **Figure 79**. **Figure 79** shows that the three currents and the three voltages are in phase, allowing an active power conversion from the DC toward the AC grid (11 kW toward the grid). The zoomed-in portion in **Figure 80** shows the current in the switching node is composed of a fundamental component at 50 Hz, plus an important current ripple amplitude caused by the switching of a 2-level converter.

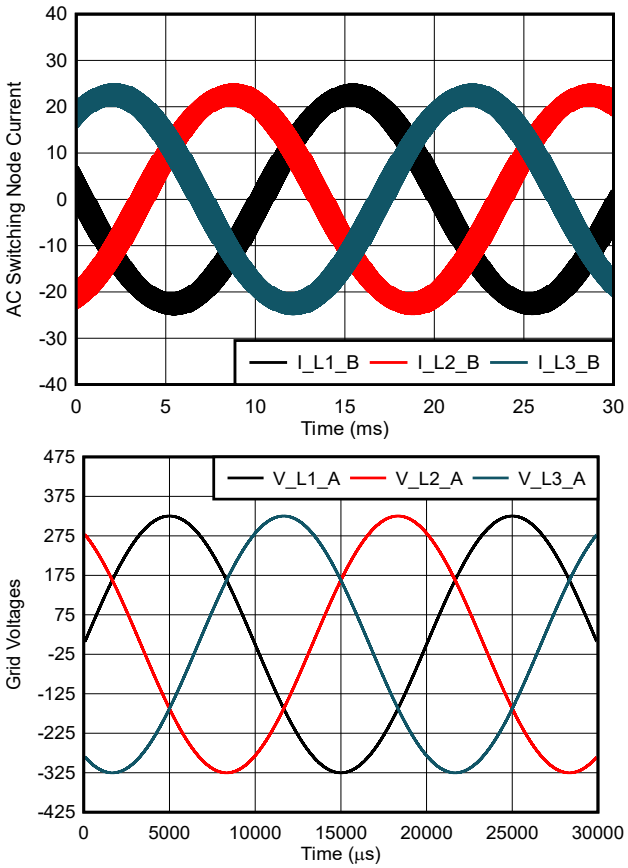


Figure 79. *Grid Voltages and Currents of an AC/DC Converter Working at the Nominal Load of 11 kW*

Figure 80 is a zoomed-in view of **Figure 79** which shows the rectifier current plus the average current having a fundamental harmonic of 50 Hz.

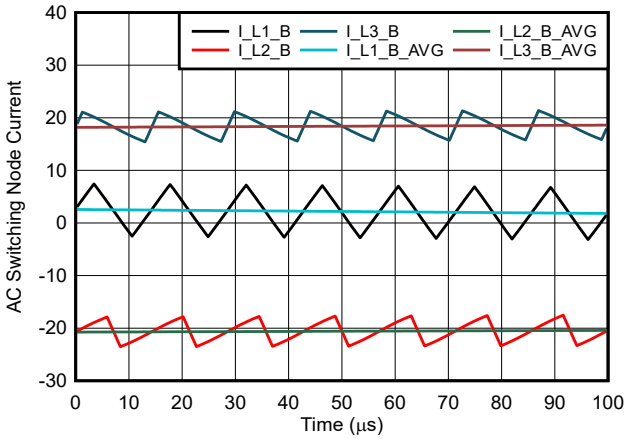


Figure 80. *Zoomed in Portion at t = 0s (Span 100µs)*

Power conversion between AC and DC is achieved by means of the currents controlled at the grid frequency. Therefore, the measurement of the fundamental harmonic of the current (for example, I_L1_B_AVG) with correct amplitude and no important phase-delay needs to be delivered to the MCU. The 50-Hz or 60-Hz component can be derived by means of sampling technique as synchronous sampling, average control, and so forth. By adopting these techniques, no important phase delay in the digital control loop is introduced, allowing a faster response of the loop [12]. Conversely, current sensors cannot be considered an ideal choice since current sensors have a bandwidth limitation. The current sensors can lead to important phase-delay and amplitude errors present at the MCU terminals. This error can be reflected in an error of the active and reactive powers exchanged and are expressed as in **Equation 42**.

$$\varphi = a\tan(2\pi \ f_e \ \tau) \tag{42}$$

where

- φ is the phase delay between the measured current and the real current
- f_e is the electrical frequency of the measured signal, which is equal for this application to 50 Hz or 60 Hz
- τ is the constant time of the low-pass filter behavior presented by the measurement chain

By using **Equation 42**, with a cutoff frequency higher than a hundred times the grid electrical frequency (6 kHz when having a grid at 60 Hz) a phase-angle delay lower than 0.6°can be achieved. This phase shift results in 50 Hz or 60 Hz to a negligible error of the active and reactive controlled power. The component to which the power conversion occurs, a 6-kHz bandwidth, is more than sufficient for controlling grid currents.

In general, 50 Hz or 60 Hz are not the only component to be controlled but there are higher frequency components in the grid currents introduced by the dead time in the power stage, leading to a significant increase of the THD. The high frequency component must be captured by the measurement such that the MCU can correct them, allowing a software cancellation. Increasing the dead time leads to higher distortions, in particular at the zero crossing of the current (at 11 ms) as shown in **Figure 81**. In this picture, current waveforms in point A drained by an AC/DC converter working at 11 kW are shown when the dead time of the controller is changed. The top graph shows the current waveform with 250-ns dead time, the bottom graph with 1.5-µs dead time.

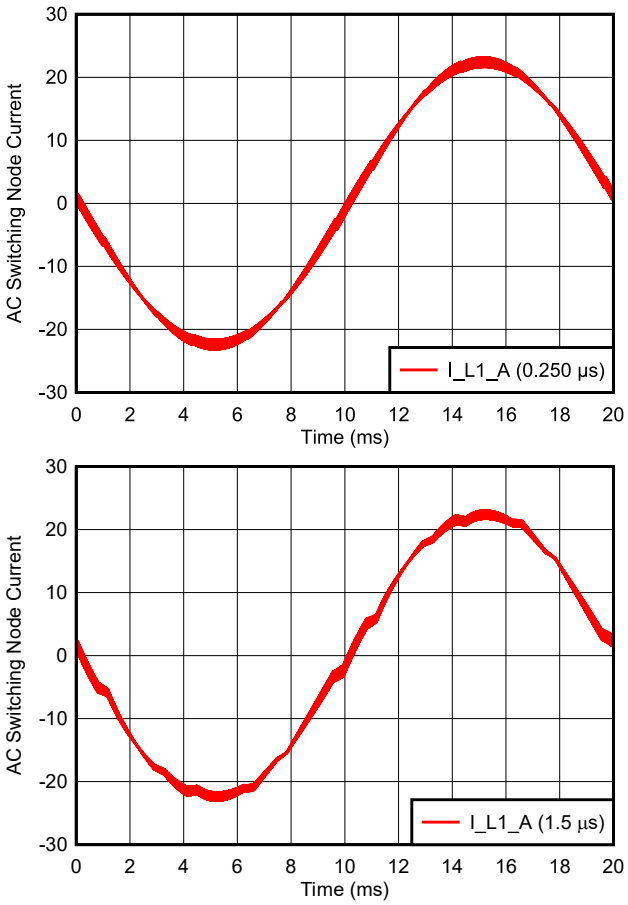


Figure 81. *Current Drained From the PCC When a Dead Time of 250ns and 1.5µs are Implemented (50-Hz Operation)*

Excessive dead time can lead to significant THD which exceeds the limits set by the standards. To comply with the standards, either a large output filter is needed or adequate software control must be provided. Multiple control techniques were developed with the aim to compensate this disturbance; however, all these options require sufficient bandwidth of the current sensor. To determine the minimum bandwidth requirements, an fast Fourier transform (FFT) transformation of the current waveform is performed to analyzed the frequency content of the disturbance.

Figure 82 shows the results of FFTs of the currents in the PCC when full power is required by the grid.

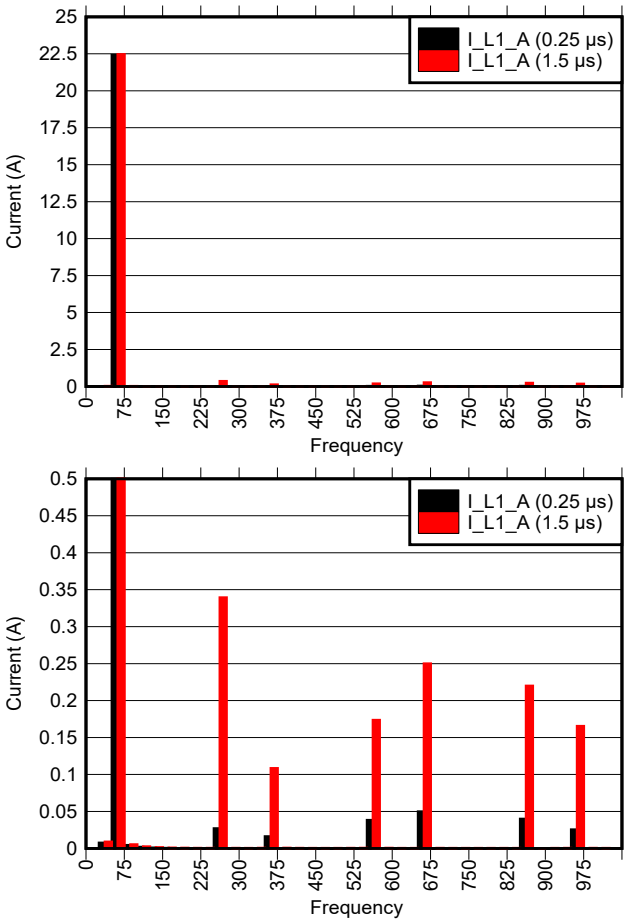


Figure 82. *FFT of the Currents Depicted in Figure 2-6 Plus Zoomed Portion (50 Hz)*

The most important frequencies to be compensated in **Figure 82** are the 5th, 13th, and 17th harmonics, leading to 250 Hz, 650 Hz, and 850 Hz when the grid is working at 50 Hz. Correspondingly, when the grid operates at 60 Hz the frequencies are 300 Hz, 780 Hz, and 1020 Hz. By applying **Equation 42** to the new frequencies, a minimum bandwidth from the current sensing stage of 102 kHz needs to be provided to make sure a proper compensation of the harmonics.

In conclusion, from steady-state analysis, a minimum bandwidth of 102 kHz when having a 60-Hz grid is necessary to improve the total harmonic distortion of the currents when an important dead-time is present in the PFC stage. When the grid is operating at 50 Hz, the minimum bandwidth can be scaled down to 95 kHz. The current sensor bandwidth is required in either point A or B depending where the currents are controlled because harmonic content generated by dead time is the same in both the measurement points. The reason is due to the fact that the EMI filter (see **Figure 76**) is optimized for much higher frequency content; therefore, no important mitigation can be achieved at low frequency.

Transient Analysis: Step Power and Voltage Sag Response

This section analyzes the performance of the control current loops with the aim of determining the minimum bandwidth of the current-sensing stage when transients caused by the grid are injected. The goal of the study is to find the minimum bandwidth allowed to keep the converter tied to the grid when no major malfunctions are present in the PCC without running in overcurrent protection status. Multiple stress scenarios which can cause overcurrents were

analyzed: AC voltage sag, step-power response, and AC overvoltage. Between the mentioned faults, only voltage sag and step-power response are explained.

Figure 83 depicts switching node currents (Point B) with respect to grid voltages when a converter operating with sensors has a bandwidth of 6 kHz. In the top graph, the output power of the AC/DC converter is stepped from zero to 11 kW at 3ms, resulting in an overcurrent in L1 (I_L1_B). In the bottom graph, the AC line voltage is dropped by 20% at 26ms, resulting in significant overcurrent in L2 (I_L2_B) that can lead to an unwanted converter shut-down.

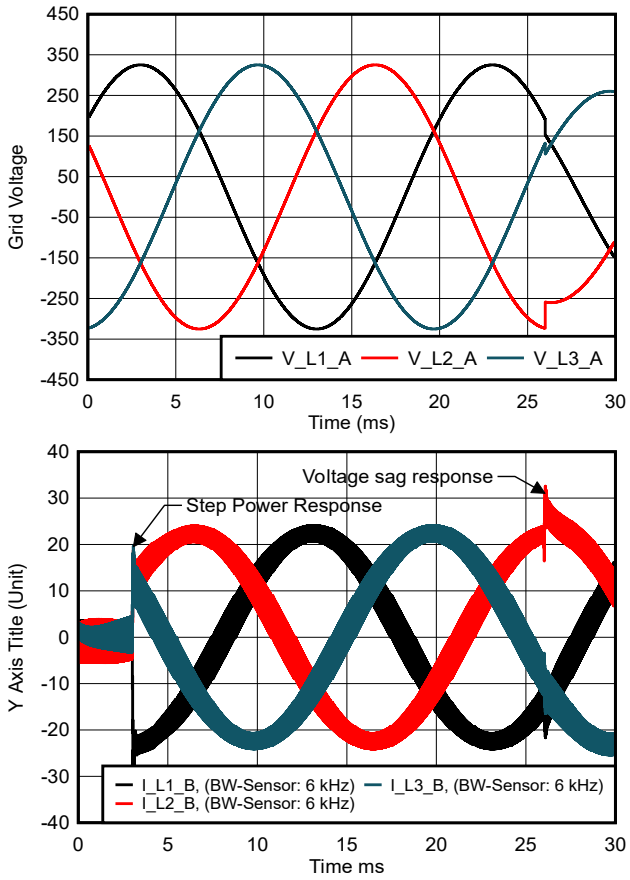


Figure 83. *Grid Voltages and Currents of AC/DC Converter: Step Power and Voltage Sag Responses*

Multiple simulations were run by only changing the bandwidth of the current sensor (6 kHz, 30 kHz, 60 kHz), then comparing of the peak overcurrent in the switching node when a step power is requested by the battery. **Figure 84** shows the results of the simulations. With a 6-kHz current sensor, the current in L1 overshoots by 30% (33-A peak) relative to the prime transient response that is achieved with a 30-kHz current sensor (10 times higher than the bandwidth of the current control loop). An additional increase in current-sensing bandwidth (from 30 kHz to 60 kHz) brings no additional benefit because both the curves overlap.

Figure 84 shows the zoomed-in portion at t = 3 ms (span 200 µs) of the step power response (11 kW) of the AC/DC converter with the current-sensor bandwidth as the parameter.

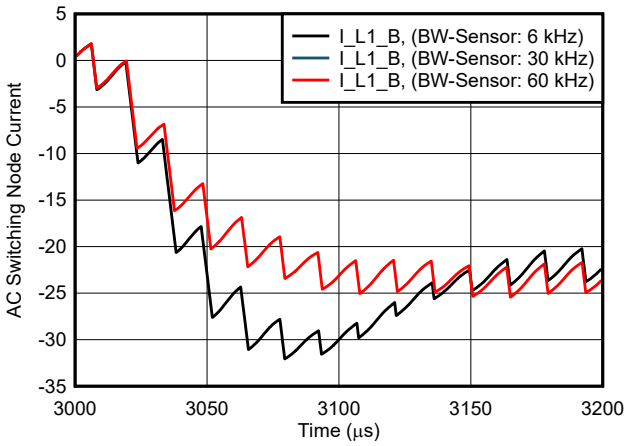


Figure 84. *Zoomed Portion at t = 3ms (Span 200µs)*

Multiple simulations were run by only changing the bandwidth of the current sensor. Comparisons of the peak current in the switching node when the converter is working at full load and unpredictable voltage sag on the grid occurs were conducted. **Figure 85** shows the line-transient response with 6 kHz, 30 kHz, and 60 kHz current sensors. With a 6-kHz current sensor, the current in L2 overshoots by > 2 A (to an approximate 33-A peak) relative to the prime transient response that is achieved with a 30-kHz current sensor (10 times higher than the bandwidth of the current control loop). An additional increase in current-sensing bandwidth (from 30 kHz to 60 kHz) brings no additional benefit (both curves overlap).

Figure 85 shows the zoomed-in portion at t = 26ms (span 200µs) of the AC/DC converter voltage sag response with the current-sensor bandwidth as the parameter.

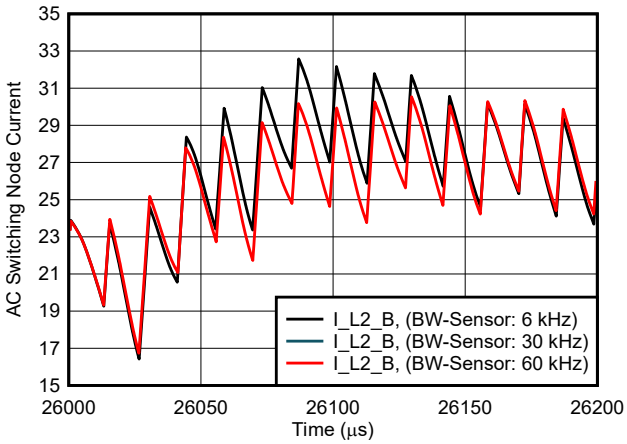


Figure 85. *Zoomed Portion at t = 26ms (Span 200µs)*

To take full advantage of the available current control loop bandwidth, keep the sensing bandwidth at least 10 times higher than the control loop bandwidth. By applying this guideline, the resolution of the current measurement is maximized because measurement range does not have to be sacrificed for overcurrent detection.

Impact of Latency

The latency is a critical parameter to consider when abnormal operation of the converter or faults from the grid occur. To protect the active power devices, the critical condition needs to be detected as soon as possible to shut the system down immediately and bring the system to a safe condition. The maximum acceptable latency was determined for the

sensor located in B to be as close as possible to the power switches. From a multitude of possible faults in the AC/DC stage, only the ones caused by the grid were considered in this section.

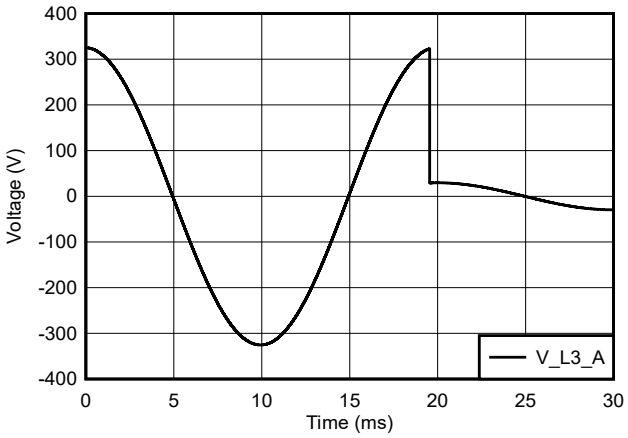
Fault Analysis: Grid Short-Circuit

To evaluate the maximum latency required by the AC/DC to shut down safely, system simulations were performed by applying the following conditions:

- DC bus voltage working at the maximum rated voltage (800 V)
- Converter operating at the nominal current (16 A_{RMS})
- Short circuit injected when the maximum current of a phase is drained
- No linear inductance of boost inductors with flux versus current profile of soft-magnetics materials; the inductance versus current is optimized for an 11-kW AC/DC and the inductance decreases down to 30% of the nominal value when saturation is achieved
- The overcurrent threshold of the current sensing in point B is set up at 30 A (93.7% of measurement range)
- Based on available data sheets of power components used in 11-kW applications, a maximum-allowed current of 60 A was selected

When a short-circuit is happening in the grid the converter is still switching, thus leading to uncontrolled currents. Since the fault is happening suddenly, there is not enough time for the MCU to update and correct the duty cycles. PWM updates typically happen at a fixed frequency (70 kHz or every 14.2µs in this example). By following single and double update refresh techniques, the minimum reaction time of the MCU can be 1/fs or 1/2fs. Within this time, the current in the inductor can exceed the short-circuit current rating of the power switch.

Figure 86 depicts the voltage and currents of the AC/DC converter. **Figure 86** shows that in the time frame between 0ms and 19ms, the converter is operating at the nominal condition with a grid voltage equal to 400 V_{RMS} and a current transferred from the DC to the AC. At 19ms, a short-circuit event is simulated by dropping the phase voltage to 10% of the nominal value. Simultaneously to the grid fault, the currents in the switching node start to increase due to the voltage difference between the grid and the applied one from the switching stage, as shown in **Figure 87**.



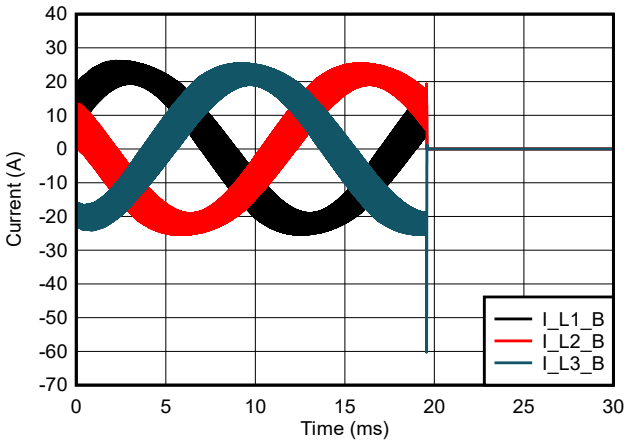


Figure 86. *Grid Voltages and Currents of AC/DC Converter: Short-Circuit Response of the AC/DC Converter*

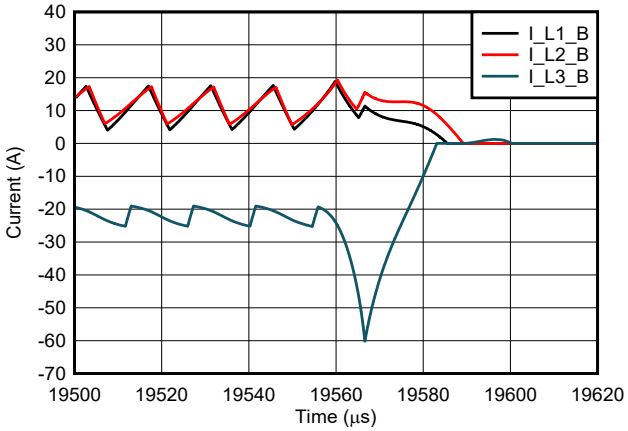


Figure 87. *Zoomed-in Portion at t = 19.5ms (Span 120µs): Short-Circuit Response of the AC/DC Converter*

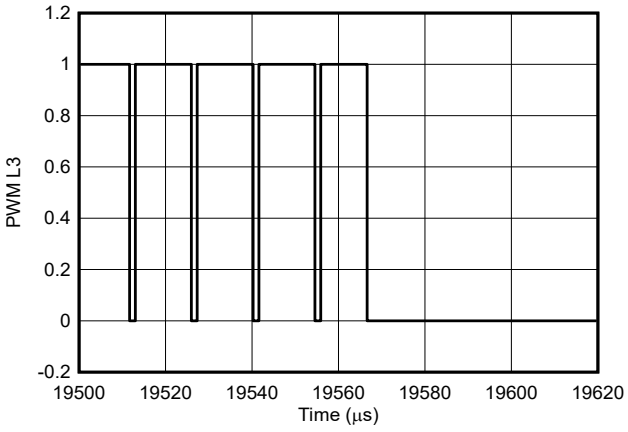


Figure 88. *Zoomed-in Portion of PWM at t = 19.5ms (Span 120µs): PWM Turn-off Behavior*

At the beginning, the current start-to-rise linearly is because the core is not saturated and is following a fixed di/dt since the inductance is nearly constant:

$$di/dt = V_{DC}/(1.5L(i)) \quad (43)$$

where

- L is the AC/DC boost current in function of the current
- V_{DC} is the DC bus voltage at the moment of the fault

When the saturation current of the core is reached, the inductance value drops significantly, leading to a sudden increase of the current. When the real current in phase L3 reaches 30 A (overcurrent threshold), the MCU must be able to detect the overcurrent as soon as possible, since the MCU cannot detect higher currents, and shuts down before the current reaches a level above 60 A. Based on the simulation results, the current takes 4µs to reach the critical value. After this timing is reached, turn off the PWM signals as shown in **Figure 88**.

In conclusion, the system must turn off within 4µs to avoid damage to power switches. Consider the latency of the current sensing together with those of the MCU and driver stage shut down. Based on typical values of latency time of the MCU and driver stage, a maximum latency of 3.5µs must be provided by the current sensor.

Impact of Gain Error

Figure 75 depicts the equivalent model of the current sensor by showing the presence of a gain error block. In this study, gain error is modeled as a fixed value as represented in **Section 7.2.1.2.2**.

Power Disturbance in AC/DC Caused by Gain Error

The goal of the current control loops of the AC/DC stage is to keep the currents detected by the MCU under control without determining the real currents in the system. If the measurement does not match the reality, there is an unwanted power disturbance in the system caused by the gain error, which is expressed in **Equation 44**.

$$\Delta P_{GAIN} = 0.5\ VI[(\varepsilon_1 + \varepsilon_2 + \varepsilon_3) + (0.5(\varepsilon_2 + \varepsilon_3) - \varepsilon_1)\cos(2\omega t) + (0.87(\varepsilon_2 - \varepsilon_3))\sin(2\omega t)] \quad (44)$$

where

- ΔP is the power disturbance caused by the gain errors in function of time, where this power is drained from the grid toward the DC link
- ε_1, ε_2 and ε_3 are the relative gain errors of each current-sensing stage
- V is the phase-to-neutral RMS voltage
- I is the RMS current controlled by the converter
- ω is the electrical pulsation derived from the grid frequency

The power disturbance is a function of the converter power between the AC and DC stage and reaches the maximum when the maximum power is requested by the AC/DC converter. Furthermore, **Equation 44** can be divided in two parts as in **Equation 45** and **Equation 46**.

$$P_{GAIN\_DC} = 0.5\ VI\left[(\varepsilon_1 + \varepsilon_2 + \varepsilon_3)\right] \quad (45)$$

$$P_{GAIN\_AC} = 0.5\ VI\left[(0.5(\varepsilon_2 + \varepsilon_3) - \varepsilon_1)\cos(2\omega t) + (0.87(\varepsilon_2 - \varepsilon_3))\sin(2\omega t)\right] \quad (46)$$

where

- P_{GAIN_DC} represents the presence of a fixed power disturbance drained by the PFC during the operation
- P_{GAIN_AC} represents a power ripple at double the grid frequency exchanged with the grid

Impacts of these power disturbances in the DC and AC sides are investigated by observing the voltage control loops together with the imperfection that was detected.

AC/DC Response to Power Disturbance Caused by Gain Error

Figure 89 shows a generic voltage controller and equivalent model of the power plant.

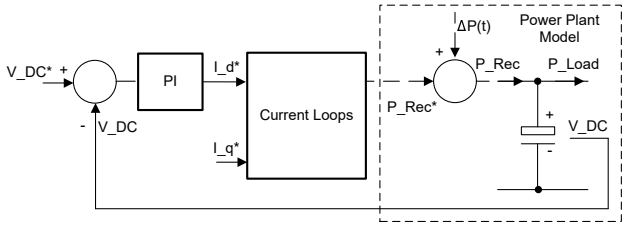


Figure 89. *Simplified DC Bus Voltage Control Loop With Power Plant Model*

As **Figure 89** shows, the term derived analytically before (**Equation 44**) was introduced in the loop as a disturbance to check the voltage control performance. By observing the control loop topology, it can be demonstrated that, thanks to the presence of an integrative part of a PI controller, the steady-state error caused by the DC disturbance **Equation 44** is completely rejected. Conversely, the AC component of the disturbance cannot be rejected completely, thus leading to a voltage ripple.

To evaluate the maximum acceptable gain error of a current sensor used in the AC side, simulations were run by applying the following hypothesis:

- DC bus voltage working at the minimum rated voltage to maximized the ripple voltage (650 V)
- Maximum power exchange between the AC and DC side, thus increasing the power disturbance (11 kW)
- Gain error for the three phases applied to reach the worst-case scenario, as follows:

  $\varepsilon_1 = -\varepsilon_2 = -\varepsilon_3$;
- Current control loop bandwidth kept constant in all the simulations (3 kHz)
- The AC filter is designed to keep the THD below 3% at the nominal output power when using prime current sensing
- The power line frequency is 50 Hz

Figure 90 shows simulation results of an AC/DC converter working with sensors having different gain error.

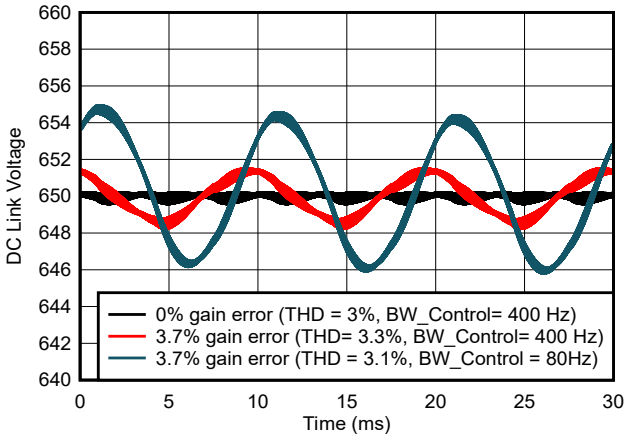


Figure 90. *DC Link Voltage Ripple Over Time With DC Link Bandwidth and Gain Error as Parameters*

The following results are present in **Figure 90**:

1. A 100-Hz ripple voltage on the DC-link. This is caused by the power ripple injected by the gain error of a current sensing stage.
2. The mean value of the voltage in all the cases is still the same when steady state is reached thanks to the integrative part of the PI controller, as confirmed by the theory.
3. The DC-link voltage ripple is correlated to the bandwidth of the DC-link voltage control loop. If the bandwidth of the voltage control loop is high enough, the controller tries to eliminate the ripple voltage by controlling very fast the current loops at the expense of grid THD.

In this example a 400-Hz bandwidth of the voltage control loop, paired with 3.7% gain error of the current sensor, leads to a THD of 3.3 % compared to a 3% THD with an ideal current sensor without gain error. Alternatively, a low bandwidth of the voltage control loop leads to low THD on the grid-side but the ripple voltage on the DC link can increase to an unacceptable level. Having a voltage ripple in the DC link can lead to power ripple on the battery which cannot be tolerated. Furthermore, low voltage control loop bandwidth leads to poor load-step response.

In conclusion, a current sensor located in the switching node with a gain error of 3.7% can lead to an increment of the grid current THD of more than 10%. To compensate for this increase, the input filter has to grow by more than 4% in volume to meet the design goal of < 3% THD at the grid-side of the converter.

Impact of Offset

Figure 75 shows the equivalent model of a real current sensor with offset. In this study, the current-sensor offset is modeled as a fixed-value normalized to the full scale of the measurement, see **Equation 47**.

$$I_O = I_{MAX} \quad \delta_O \tag{47}$$

where

- I_0 is the absolute offset value presented by the sensor
- I_{MAX} is the maximum of the measurement scale
- δ_0 is the per-unit value of the offset error introduced in the measurement

The goal of the current control loops of the AC/DC stage is to keep the currents detected by the MCU under control without determining the real currents in the system. If the measurement does not match the actual current due to an offset error, the current causes an undesired power disturbance in the system as is expressed with **Equation 48**.

$$\Delta P_O = V[I_{O1}\sin(\omega t) + I_{O2}\sin(\omega t - 2/3\pi) + I_{O3}\sin(\omega t + 2/3\pi)] \tag{48}$$

where

- ΔP_O is the power disturbance caused by the offset errors as function of time
- I_{O1}, I_{O2}, and I_{O3} are offset errors of each current sensor
- V is the phase to neutral RMS voltage
- ω is the electrical pulsation derived from the grid frequency

The power disturbance is not a function of the power conversion between the AC and DC stage, as opposed to the gain error case; therefore, the issue is always present for any operating condition. This reflects by always having voltage ripple in the DC link. The offset introduces a power disturbance in the system with a frequency equivalent to the line frequency of the grid. As mentioned in the **gain error** chapter, the DC bus voltage loop is not able to fully reject the power ripple coming out from the sensing point. For this reason control loop versus current-sensing performance must be simulated. Simulations were run for the following use-case and assumptions:

- DC bus voltage working at the minimum rated voltage to maximize the ripple voltage (650 V)
- Maximum power exchange between AC and DC side. This has no effect on the result. The results are the same for the no-load condition.
- Offset error defined with respect to the full measurement scale per unit. When using a shunt-based design with ±50-mV isolated device, the maximum scale is ±32 A.
- Offset for the three-phases applied to reach the worst-case scenario as follows: $I_{O1} = -I_{O2} = -I_{O3}$
- Current control-loop bandwidth kept constant in all the simulations (3 kHz)
- AC filter designed with the aim to keep the grid THD at the nominal power at 3% when using ideal sensing
- Power line frequency is 50 Hz

Figure 91 shows the simulation results of a AC/DC converter working with different current sensing and with different offset errors.

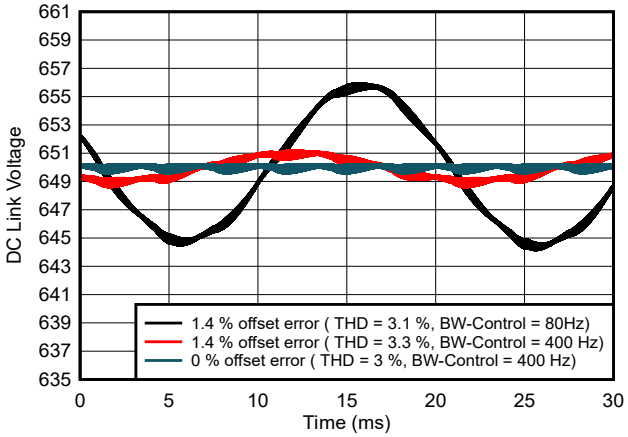


Figure 91. *DC-Link Voltage Ripple Over Time With DC Link Bandwidth and Offset Error as Parameters*

Observe the presence of a 50-Hz ripple voltage on the DC-link, caused by the power ripple injected by the current sensing stage with an offset. Additionally, the mean value of the voltage in all the cases is still the same when steady state is reached thanks to the integrative part of the PI controller.

The important correlation between the DC link voltage ripple and voltage control bandwidth is evident. If the bandwidth of the voltage control loop is high enough, the control loop tries to eliminate the ripple voltage by quickly controlling the current loops at the expense of the THD toward the grid. In fact, with a bandwidth of the control equal to 400 Hz, an offset of 1.4% offset error, leads to an increment of 10% of the THD (from 3% to 3.3%). Conversely, when the bandwidth of the voltage loop is not high, fluctuation in the DC link is very high because voltage loop is not trying to reject this variation, but this time not injecting any more harmonics in the grid. However, remember that having a voltage ripple in

the DC-link can lead to power ripple on the battery which cannot be tolerated. Furthermore, if the voltage bandwidth is significantly reduced, the performance of the step load response becomes quite poor.

In conclusion, a current sensor located in the switching node with an offset error of 1.4% can lead to an increment of the grid current THD of more than 10%.

Point C and D – AC/DC DC Link Current Sensing

This chapter provides the design considerations of current sensors used in the DC link for AC/DC converter.

Current sensors in the DC link are not mandatory for the basic functionality of the power conversion but sensors can be used for implementing features such as power measurement, protection and feedforwards for the voltage loop.

Sensing in the DC-link can be placed in point C or point D, before and after the DC-link capacitors used for PWM ripple frequency filtering and energy storage (**Figure 76**), respectively.

Offset, bandwidth, accuracy, and latency of current sensors are discussed at a system level base with the goal of determining the minimum requirements for each of the desired additional functions. Not all scenarios are discussed for both points C and D as many cases turned out to be a repetition, only the worst-case scenarios were analyzed to determine current sensor requirements. Details about each analysis follows:

- **Gain Error**: impact of gain error is the same in both C and D points. Minimum gain error required by this sensor needs to be evaluated for power measurement and feedforwards.
- **Offset Error**: impact of gain error is the same in both C and D points. Minimum offset error required by this sensor needs to be evaluated only for power measurement. Offset error is not critical for the feedforward since the error is compensated out from the integrative part of the DC bus voltage PI controller.
- **Minimum Bandwidth**: impact of bandwidth is the same in both C and D points. Bandwidth is required for the feedforward application, and most effective when placed in point D.
- **Maximum Latency**: Low latency is important for protecting the active switches of the power-stage, so it is evaluated for point C, the closest point to the active switches.

Impact of Bandwidth on Feedforward Performance

To evaluate the minimum bandwidth required of a current sensor located in position D, when used for feedforward, system simulations were executed by applying the following conditions:

- DC bus voltage working at the minimum rated voltage (650 V)
- Step power applied on the DC-link of 11 kW
- Grid operating at 400 V_{RMS}

Simulations were performed to compare load transient performance with and without feedforward. **Figure 92** shows the results. Without feedforward, the DC-link voltage drops significantly when the load is applied, leading to possible unstable converter operation. With feedforward, performance is drastically improved and the load transient response is reduced by a factor of 5. Conversely, the simulation results show how this additional sensor, in addition to the possibility to measure the power on the DC rail, is very useful when deployed with the load which connects and disconnects without giving a warning.

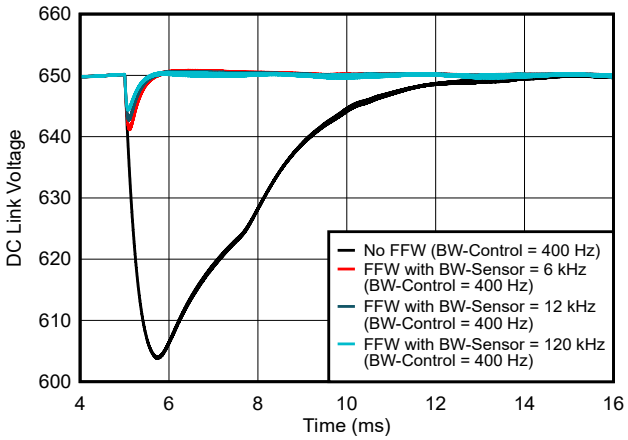


Figure 92. *DC-Link Voltage Response to Step Power With DC-Link Bandwidth as Parameter, With and Without Feedforward*

Figure 93 shows that the bandwidth of the current sensor only plays a minor role in the performance improvement since the overall bandwidth is limited by the dq current loop.

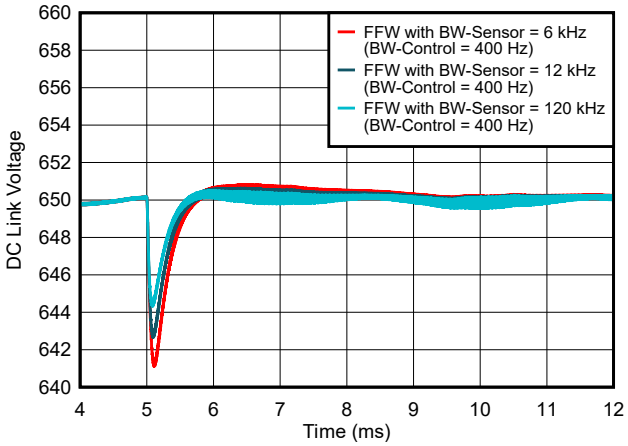


Figure 93. *DC-Link Voltage Response to Step Power With DC-Link Bandwidth as Parameter, With Feedforward*

In summary, when placing a current sensor in point D for feedforward purposes, a low bandwidth of < 10 kHz is sufficient. In general, the bandwidth of the current sensor needs to be at least two times higher than the bandwidth of the current loop.

Impact of Latency on Power Switch Protection

Maximum latency of the sensing stage needs to be evaluated only for point C, since point C is the closest one to the power devices. The position of this sensor allows detection of both overcurrent and short circuits but at the cost of increasing the parasitic inductances in the loop. Detection latency must be shorter than the short-circuit withstand time of the power switch and therefore depends on the switch technology. The following numbers are guidelines only. To make sure of the withstand time, refer to the device data sheets:

- SiC MOSFET: maximum latency of 1–3µs
- IGBT: maximum latency of 2–10µs
- GaN FETs < 3µs

In addition to the latency of the overcurrent sensor, the delay of the input filter, the response time of the MCU, and the turn-off-delay of the gate driver needs to be considered. To achieve an effective turn-off delay < 1.5µs, the latency of the overcurrent sensor must be < 1µs. TI offers a line of isolated comparators with latencies < 300ns that are specifically designed for this application.

Impact of Gain Error on Power Measurement

Transient Analysis: Feedforward in Point D

To evaluate the impact of the gain error of a current sensor on the performance of the feedforward, simulations were performed for the following operating condition:

- DC bus voltage working at the minimum rated voltage (650 V)
- 11-kW load step is applied to DC-link as t = 1ms
- Grid voltage is 400 V_{RMS}

As **Figure 94** shows, with an increment in the gain error in point D has only deteriorate slightly. This demonstrates that gain error is not a critical parameter when considering feedforward applications.

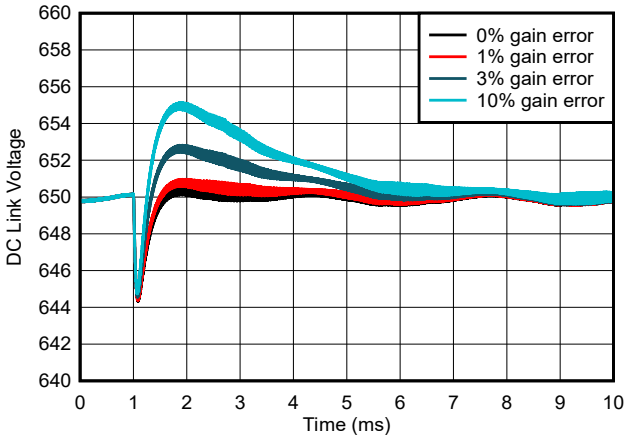


Figure 94. *DC-Link Voltage Response to Step Power With DC-Link Gain Error as Parameter, With Feedforward*

In summary, gain error in the DC-link current sensor has a minor effect on the overall transient load-step performance and gain errors up to 3% still achieve acceptable performance.

Impact of Offset

Offset of the sensing stage can only affect steady state. In dynamic applications, where the sensing is used for creating a feedforward, the voltage loop compensates automatically for the error introduced by the offset.

Summary of Positives and Negatives at Point A, B, $C_{1/2}$ and $D_{1/2}$ and Product Suggestions

Power switches are the most sensitive components that can be damaged by overload or overcurrent. The close proximity of power switches allows faster fault detection, leading to have sensing in B and C vitally important. For point B, the high-side power supply of the isolated amplifier can be shared with the high-side gate driver supply and fast overcurrent (OC) detection is possible. The current sensing at point B needs to be able to handle high Common Mode Transient Immunity (CMTI) and this measurement can get affected by noise during power-stage switching, in particular when GaN or SiC designs are adopted. The precise reactive power control is the best possible at point A, where

the measurement is behind the filter far away from switching noise. The drawback is the requirement of an isolated power supply at point A. Only slow OC detection is possible. **Table 12** summarizes the pros and cons of the various current-sensing points. **Table 13** summarizes requirements and provides an excellent choice of products for each point.

Table 12. Positives and Negatives of the Current-Sensing Points A, B, $C_{1/2}$, and $D_{1/2}$

	A	B	C1	D1	C2	D2
Accurate power regulation	(+)(1)	(–)	(+)	(+)	(++)	(++)
Feedforward loop	N/A	N/A	(–)	(–)	(+)	(+)
Fault protection	(–)	(++)	(++)	(+)	(–)	(–)
Sharing of power supply	(–)	(+)	(+)	(–)(2)	(+)	(–)(2)

(1) Precise reactive power control at PCC is possible – accuracy to be defined by the manufacturer (often < 1%)

(2) D_1 and D_2 need a floating supply above VDC+

Table 13. AC/DC Minimum Requirements and Available Products for Current Sensing at Points A, B, $C_{1/2}$, and $D_{1/2}$

I-Sensing Point	Primary Applications	Iso-Supply Voltage	Minimum Bandwidth	Maximum Latency	Requested CMTI	Minimum Accuracy	TI Products (ISO-)AMP| ISO-ΔΣ
A	Able to adjust precisely reactive power	Floating needed (ISO-VDD1)	> 102 kHz	-	Low	< 3.7 %	AMC3302| AMC3306M05
B	Overcurrent protection and control	From upper gate driver	> 102 kHz	< 3.5 µs	High	< 3.7 %	AMC1302 | AMC1306M05 | AMC23Cxx
C1	Current in neg branch and fault detection	From lower gate driver	-	< 1.5 µs	Low	<1 %	AMC1302 |AMC1306M05 | AMC3302 | AMC23Cxx| AMC22Cxx
D1	Current in positive branch and fault detection	Floating above VDC+ needed	-	< 1.5 µs	Low	<1 %	AMC3306M05 |AMC3302 | AMC23Cxx| AMC22Cxx
C2	Current in neg branch and fault detection	From lower Gate Driver	> 6 kHz	-	Low	<1 %	AMC1302| AMC1306M05|AMC3302
D2	Current in positive branch and fault protection	Floating above VDC+ needed	> 6 kHz	-	Low	<1 %	AMC3302| AMC3306M05| AMC23Cxx| AMC22Cxx

(1) 1% accuracy is only required in cases where it is necessary to measure the power precisely. 3% is sufficient for systems that do not require accurate power control.

Current Sensing in DC/DC Converters

There are many implementations for DC/DC converters applicable to be used for EV charging applications. Typically, an isolated architecture is chosen. Two topologies that are used frequently as bidirectional topologies are *Dual Active Bridge with Phase Shift Control* and *Dual Active Bridge in Resonant CLLLC* configuration. Both topologies are explained in detail and how to implement current sensing in the topologies are discussed in the next sections.

Basic Operation Principle of Isolated DC/DC Converter With Phase-Shift Control

Figure 95 shows a typical control loop of a phase-shift dual active bridge (DAB) DC/ DC converter. There are two control loops in this system: (a) an outer voltage loop and (b) an inner current loop.

For the voltage loop, the output voltage is fed into an ADC of a MCU (denoted as V_{fb}) in **Figure 95**. V_{fb} is compared with a reference voltage (denoted as V_{ref}). The error between the measured voltage and reference voltage is fed to a compensator, which can be realized as a PID controller. The output of the voltage loop is used as reference (I_{ref}) for the inner current loop. The compensator of the inner current loop (G_I) compares the reference (I_{ref}) and actual value of sensed current (I_{OUT}) and uses this error to adjust the phase of a PWM waveform to the leading or lagging

bridge depending on the direction of the current. For constant current charging, the voltage loop is optional or can be implemented for protections only. For constant power charging, both loops are needed. The theoretical limits for the phase shift are ±π, practical implementations are much smaller than this.

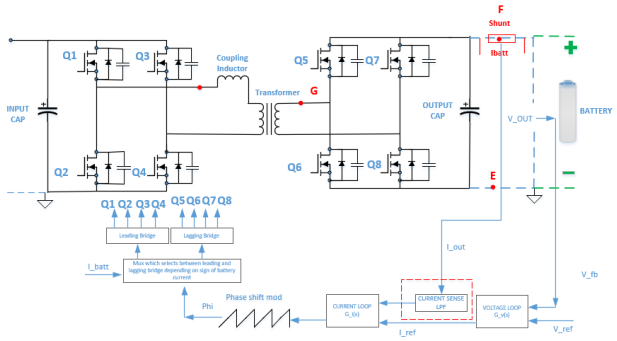


Figure 95. *Typical Control Loop of Dual Active Bridge (DAB) DC/DC Converter With Phase-Shift Control*

Point E, F - DC/DC Current Sensing

This section covers the output current sensing of the DC/DC stage. There is an option to place the current sensor at the negative battery connection (point E) or at positive battery connection (point F) as shown in **Figure 96**. Both options are equivalent from the control-loop regulation perspective. For point F, the power supply for the current sensor is floating above VBAT+ whereas for point E, the supply can be derived from the lower gate driver.

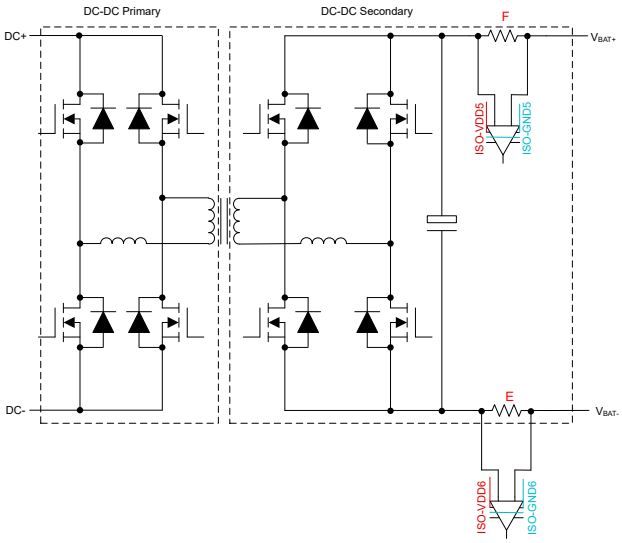


Figure 96. *Current-Sensing Point E, F*

To assess the impact of gain error, offset error, and bandwidth of the current sensor on the performance of the DC/DC converter, the model shown in **Figure 75** was used for simulations.

Impact of Bandwidth

In this simulation, the dual active bridge with phase shift control is running at a switching frequency of 100 kHz and is configured as constant current source output that drives a fixed current of 20 A into a pure resistive 10-Ω load (that results in a 200-V DC output, representing a 4-kW load).

At time t1 = 2ms, the load is changed from 10 Ω to 20 Ω. This results in an immediate current change down to 10 A (since voltage is 200 V at that time). After some time, the control loop starts to regulate back to the 20-A constant current which forces the output voltage to increase to 400-V DC when settled (resulting in a load change from 4 kW to 2 kW). **Figure 97** shows the transient response of the output current.

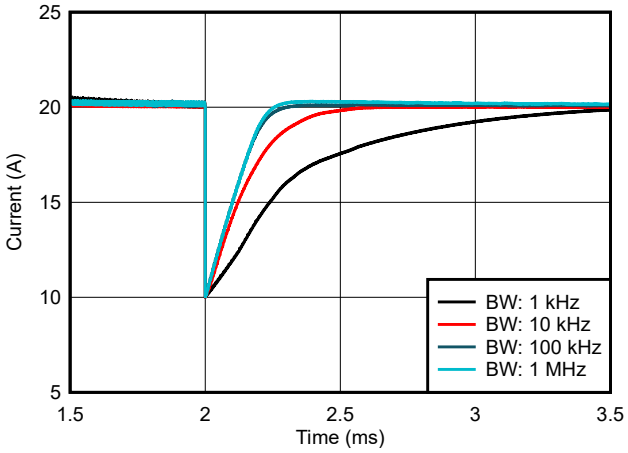


Figure 97. *DC/DC Step Load Response vs Current Sensor Bandwidth*

Figure 97 shows the response to the same load step for different bandwidth settings or the current sensor in the control loop. With a current sensor bandwidth of only 1 kHz, there is a long settling time of 1.6 ms. Increasing the bandwidth to 10 kHz and 100 kHz, brings the settling time (90% of end value) down to 0.6ms and 0.3ms, respectively. A further increase of current-sensor bandwidth does not improve the transient response significantly because the settling time is limited by the control-loop bandwidth of the current loop which was set to 10 kHz.

In conclusion, a current sensor at point E or F with a bandwidth lower than 100 kHz is sufficient to keep the settling time < 1ms for any load step change at the converter output.

Impact of Gain Error

Current sensors have gain error that may impact on the accuracy of the control loop. A simulation with the current sensor model from **Figure 75** is performed to study the settling time at turn-on of the converter. The bandwidth of the sensor is set to 100 kHz and gain errors of 0%, 1%, and 2% are chosen. **Figure 98** show the impact of the errors.

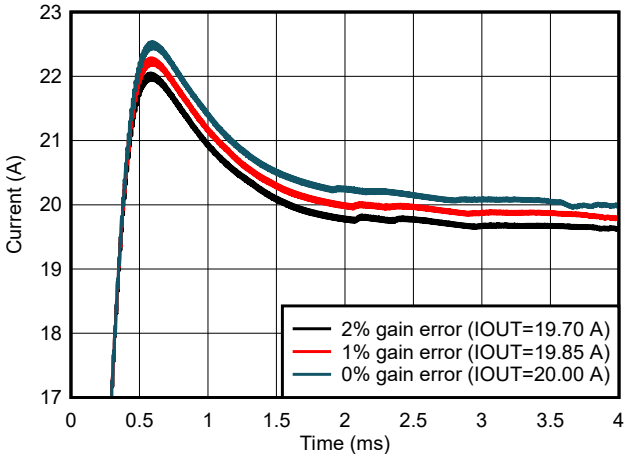


Figure 98. *Steady State Output Current Errors vs Current Sensor Gain Errors*

Settling time after a load change is quite similar since the bandwidth of the sensor is defining the settling time for all cases, meaning the gain error does not impact settling time significantly. But the gain error impacts the value to which the output current settles. This simulation shows that the remaining constant error at the output current is about 0.66% (about 0.15 A) below the ideal 20 A if the current sensor has gain error of 1% (about 1.33% / 0.32 A below the ideal 20-A output current if the current sensor has a gain error 2% respectively).

The gain error is defined as the error relative to full-scale of the current. In our example the full-scale current is 32 A. This means for a 20-A current, the resulting gain error is only about two thirds of the full-scale (about 0.66%). For a 2% full scale error, the remaining output current error settles at about 1.33%.

If the output current needs to settle within a 1% window, the full-scale gain error of a current sensor must not be bigger than 1%.

Impact of Offset Error

This chapter investigates offset error on the DC/DC converter. The same control-loop settings, current-sensor bandwidth of 100 kHz, and 0% gain error of the current sensor were assumed in the simulation for the settling time simulation shown in **Figure 99**. The offset error has been varied from 0%, 1%, to 2%.

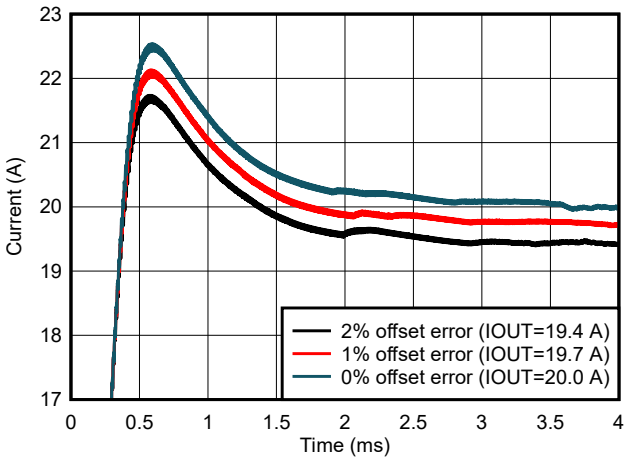


Figure 99. *Steady State Output Current Errors vs Current Sensor Offset Errors*

Again, settling time is unaffected by offset error. The settled output current is significantly affected. For 1% offset error the current output is 1.5% or 0.3 A lower (for 2% offset the output shows 3% or 0.6 A error, respectively).

Like the Gain Error, the Offset Error is specified to the full-scale error. In our example, the full-scale current was 32 A. This means at a 1% error, the absolute error is 0.3 A (for 2%, absolute 0.6 A). The simulation indicates these results are precise.

Unlike the gain error that scales relative to the output, the offset error adds in absolute to the output current that is set in a converter. Offset error is either calibrated out or compensated by feedforward techniques (adding the known error to the output).

In summary, both gain and offset error do not impact the settling time of the control loop as long as the current sensor has a high enough bandwidth not to limit the control-loop bandwidth. Both gain and offset error impacts the accuracy of the DC-charger output. For the target specifications of the EV-Charger defined in **Table 11**, this means the current sensor

needs to have a bandwidth between 10 kHz and 100 kHz and total error (for both gain and offset) smaller than 1%. Use offset calibration to achieve the target.

Point G - DC/DC Tank Current Sensing

This section details the current-sensing requirement at the switching tank - point G. In a resonant CLLLC bidirectional isolated DC/ DC converter zero crossing detection (ZCD) is required for synchronous rectification, which helps reducing the conduction loss and improve system efficiency.

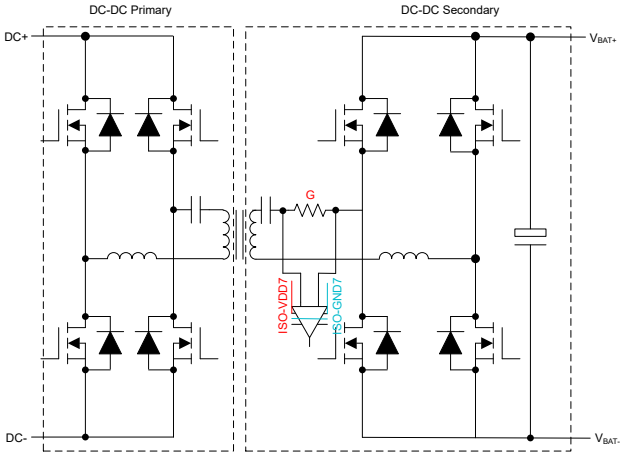


Figure 100. *Current Sensing at Primary or Secondary Tank of Isolated DC/ DC Converter*

In **Figure 100**, the two green cursor lines indicate the propagation delay between zero crossing and secondary side FET turn-on.

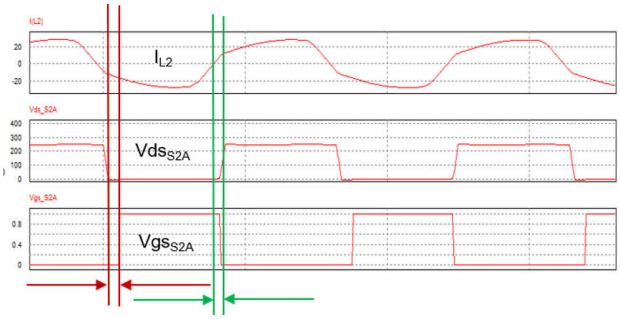


Figure 101. *Propagation Delay of Zero Crossing Detection*

A state-of-the-art implementation of the ZCD circuit in CLLLC topology is placing a Current Transformer (CT) or a Rogowski coil at the primary and secondary side in series with the resonant capacitor. Typical propagation delays of the CT or Rogowski coil approach are between 100ns and 200ns. This delay can cause significant losses in a CLLLC topology impacting overall efficiency of the DC/DC converter in a negative way. Assuming peak current is about 30 A, the resonate switching frequency of 500 kHz and turn-on delay of 100ns, the body diode (with a forward voltage of 4.5 V) the FET carries 9.3 A until the FET is turned on, which results in a peak energy loss of about 42 W per FET.

An alternative approach is shown in **Figure 102**. Here, the resonate capacitor voltage in conjunction with a differentiator circuit is implemented to recreate the sinusoidal current. The recreated sinusoidal signal is further processed by a differential-to-single-end OPA(OPA354) and a fast Comparator (TLV3501) for ZCD.

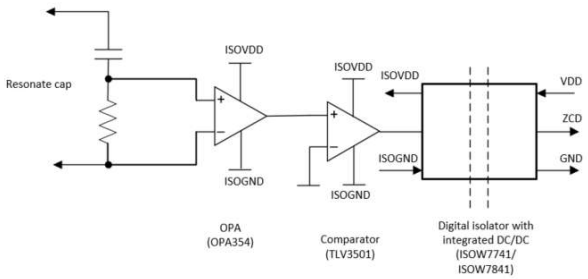


Figure 102. *ZCD Circuit With ISOW7741, ISOW7841*

The zero-crossing signal is isolated by a digital isolator (ISOW7741 or ISOW7841). These digital isolators have integrated isolated DC/DC converters to generate an isolated supply for the OPA and Comparator devices. The OPA354, TLV3501, and ISOW7741 have propagation delays of 0.6ns, 4.5ns, and 10.7ns, respectively, resulting in a total propagation delay 15.8ns for the complete design, which is about 10 times smaller than a CT or Rogowski coil approach. Assume the same switching frequency and peak current as in the previous example, the peak energy loss in one FET can be reduced from 42 W down to 6.7 W only (impacting overall efficiency positively).

Summary of Sensing Points E, F, and G and Product Suggestions

Table 14 summarizes the positives and negatives of current sensing points at E, F, and G. Fault protection needs to be handled with smart gate drivers, the current sensors cannot detect fast enough. A significant power loss improvement can be achieved by using the new ZCD shown in **Figure 102**.

Table 14. Positives and Negatives of Current Sensing Point at E, F, and G

	E	F	G
Accurate current output regulation	(+)	(+)	(–)
Overcurrent fault protection	(–)	(–)	(+)
Power supply easy	(+)	(–)(1)	(–)
ZCD	N/A	N/A	(+)

(1) Point F needs a floating supply above VOUT+

Table 15. Products for Current Sensing at Points E, F, and G

I-Sensing Point	Comments, Challenge	Iso-Supply Voltage	Minimum Bandwidth	Maximum Latency	CMTI	Minimum Accuracy	Products (ISO-)AMP | ISO-ADC
E	Current in negative branch and fault detection	From lower Gate Driver	> 10 kHz	–	Low	< 1%	AMC1302 AMC1306M05 | AMC23Cxx| AMC22Cxx
F	Current in positive branch and fault detection	Floating above OUT+ needed	> 10 kHz	–	Low	< 1%	AMC3302 AMC3306M05 | AMC23Cxx| AMC22Cxx
G	For ZCD	From upper Gate Driver	> 1 MHz	< 200 ns	High	–	OPA354| TLV3501| ISOW7841| ISOW7741

Conclusion

The control loops regulation performances of the power conversion system in DC charging stations are significantly impacted by current-sensor parameters such bandwidth, gain, and offset error.

This application note defined system simulations of AC/DC and DC/DC, correspondingly, with the minimum requirements of current sensors based on the different features. The results in this document illustrate that in DC charging stations, shunt-based designs can match and even present higher performances in all the measurement points by having low power consumption. Challenges for the shunt-based current sensing were found in the switching node of the DC/DC converter when low-latency zero-crossing current detection needs to be achieved. An alternative method for detecting the zero crossing of the current was proposed.

In conclusion, the methodology applied in this application note is not valid only for an 11-kW system but can be scaled up to higher power, leading to a proper guideline in the selection of current sensors.

References

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2. Texas Instruments, ***AMC1306x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With High CMTI*** data sheet
3. Texas Instruments, ***AMC3302 High-Precision, ±50-mV Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter*** data sheet
4. Texas Instruments, ***AMC3306M05 High-Precision, ±50-mV Input, Reinforced Isolated Delta-Sigma Modulator With Integrated DC/DC Converter*** data sheet
5. Texas Instruments, ***ISOW784x High-Performance, 5000-VRMS Reinforced Quad-Channel Digital Isolators with Integrated High-Efficiency, Low-Emissions DC-DC Converter*** data sheet
6. Texas Instruments, ***ISOW774x Quad-Channel Digital Isolator with Integrated Low-Emissions, Low-Noise DC-DC Converter*** data sheet
7. Texas Instruments, ***An overview of conducted EMI specifications for power supplies*** marketing white paper
8. Texas Instruments, ***TIDA-01606 10-kW, bidirectional three-phase three-level (T-type) inverter and PFC*** reference design
9. Texas Instruments, ***TIDA-010210 11-kW, bidirectional, three-phase ANPC based on GaN reference design***
10. Texas Instruments, ***TIDA-010054 Bidirectional, dual active bridge reference design for level 3 electric vehicle charging stations***

11. Texas Instruments, ***Software Phase Locked Loop Design Using C2000™ Microcontrollers for Three Phase Grid Connected Applications*** application note
12. ***Multirate Harmonic Compensation Control for Low Switching Frequency Converters Scheme, Modeling, and Analysis***

Using isolated comparators for fault detection in electric motor drives

Introduction

An **electric motor drive** is an electrical system that provides a variable frequency output to an electric motor to drive industrial loads such as heating and air-conditioning, ventilation, pumps, compressors, and elevators, and factory automation loads such as conveyor belts, mining, and papermill equipment.

Electric motor drives in industrial environments experience conditions such as high temperatures and high humidity, AC power-line fluctuations, and mechanical overloads. Users are demanding greater efficiency, along with more reliability. The switching speeds of power semiconductor devices such as insulated-gate bipolar transistors (IGBTs) are continuously increasing, with greater adoption of wide-bandgap technologies such as silicon carbide (SiC) and gallium nitride (GaN) that enable faster switching speeds. Given the increasing need for higher switching speeds and more system reliability, modern motor-drive systems must both detect and protect against several fault events to minimize industrial equipment downtime.

In this article, I will discuss the priority level and impact of different fault events, along with how to detect them to prevent damage to motor-drive circuits.

Introduction to electric motor drives

An electric motor-drive system, as shown in **Figure 103**, takes power from the AC mains, rectifies it to a DC voltage, and inverts the DC back to AC with variable magnitude and frequency based on load demand through complex feedback control algorithms.

A motor-drive system typically has two voltage domains: the “high-voltage” domain and the “low-voltage” domain. The microcontroller or digital signal processor, typically on the low-voltage domain, receives feedback signals (voltage, current, temperature, etc.) from the three-phase IGBT power stage and generates pulse-width modulated signals for controlling the power switching transistors and other high-side power circuitry. Such systems demand resilient and reliable galvanic isolation to isolate high-voltage circuits from low-voltage circuits. An isolation architecture enables reliable operation of motor-drive systems, preventing damage to expensive circuitry by breaking the ground loops between the high- and low- voltage circuits and helping protect human operators from high voltages.

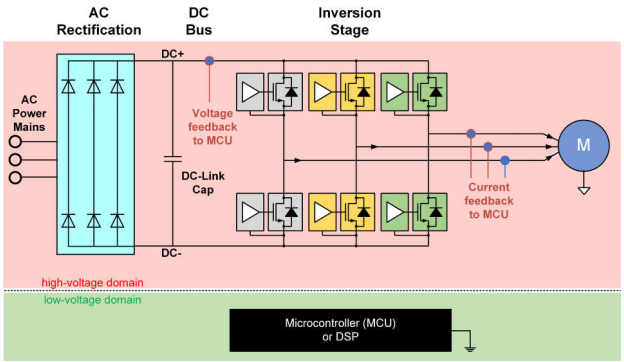


Figure 103. *AC-input electric motor-drive block diagram*

Understanding fault events in electric motor drives

Electric motor drives are susceptible to several electrical fault events. As shown in **Figure 104**, a shoot-through fault occurs when the adjacent power switching transistors, 1 and 2, accidentally turn on at the same time. This fault can

occur because of several reasons: electromagnetic interference, a malfunction in the microcontroller controlling the switching transistors, or simply worn-out switching transistors. This fault short-circuits the DC-link capacitor and can cause catastrophic failure, resulting in excessive heating, fire or even an explosion. Thus, it is imperative to detect shoot-through faults and take corrective actions such as turning off the power switching transistor very quickly.

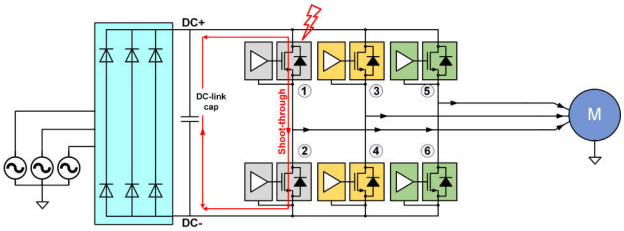


Figure 104. *A shoot-through fault in electric motor drives.*

As shown in **Figure 105**, a ground fault occurs when the motor cables, motor casing or motor windings are shorted to ground. Such shorts to ground can occur because of dielectric strength degradation in insulation caused by overstress conditions in temperature or voltage over an extended period of time. Old motors and cables are more vulnerable to ground-fault events, which can put human operators at risk for electric shocks. Thus, a ground fault requires detection and corrective actions such as rewinding or replacing the motor.

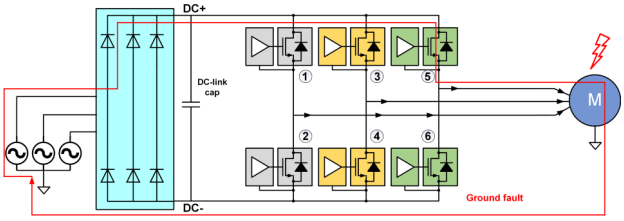


Figure 105. *A ground fault in electric motor drives.*

As shown in **Figure 106**, a phase-to-phase short fault occurs when there is an insulation breakdown in between two windings of the two phases at the stator. These phase-to-phase shorts can occur because of dielectric strength degradation in insulation caused by overstress conditions in temperature or voltage over an extended period of time. This short results in a huge increase in stator current, resulting in potential damage to the IGBTs in the power stage. Old motors and cables are more vulnerable to phase-to-phase shorts. Like ground faults, phase-to-phase faults need detection and corrective actions such as rewinding or replacing the motor.

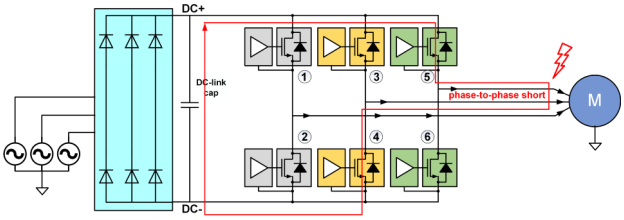


Figure 106. *A phase-to-phase short in electric motor drives.*

Overvoltage occurs for several reasons – back-injection from the motor to the DC-link rail during breaking, poor regulation of AC power abnormal circuit loads, wiring errors and insulation failures. Overvoltage can result in voltage overstresses and excessive current that can damage DC-link capacitors and IGBTs, degrade the electrical insulation,

and damage or reduce the lifetime of a motor-drive system. It is extremely important to limit the thermal energy through the IGBT by interrupting or reducing shoot-through, ground faults and phase-to-phase shorts, and avoiding transient overvoltage conditions.

Achieving reliable detection and protection in electric motor drives

Designers must incorporate multiple levels of reliable detection and protection to prevent damage to motor-drive circuits. Power switching transistors such as IGBTs have relatively short withstand times (less than 10 µs) and can quickly overheat and become damaged from excessive currents.

Current-limiting fuses and circuit breakers provide excellent overcurrent protection, but have slow reaction times and require user intervention. They are often the last resort for protection during a failure event.

To detect and quickly protect the motor drive against these fault conditions, one solution senses the current and voltage at critical electrical paths within the motor drive. The measured current and voltage are received by a host microcontroller that controls high-side power circuits such as power switching transistors and circuit breakers. To suppress overcurrents or overvoltage faults, the host microcontroller either turns off or modifies the switching characteristics of power transistors, or trips the circuit breakers.

Figure 107 shows the Texas Instruments (TI) **AMC23C14** family of low-latency reinforced isolated comparators in short-circuit current, overcurrent, undercurrent, overvoltage, undervoltage and overtemperature fault-detection scenarios. These devices integrate adjustable comparator threshold functions, include a high-side low-dropout regulator for the power supply, and have a response time of sub-0.5 µs in an eight-pin small-outline integrated circuit package.

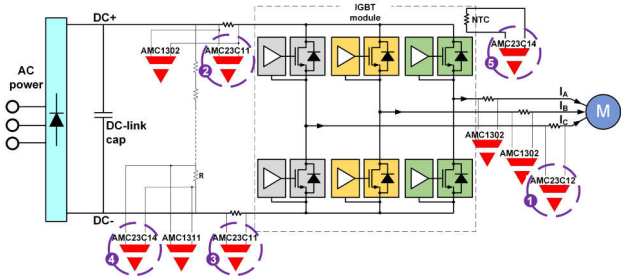


Figure 107. *Ultra-fast fault detection in electric motor drives.*

Next, review the several use cases for **AMC23C14** family of isolated comparators in electric motor drives.

Use case No. 1: Bidirectional in-phase overcurrent detection

Figure 108 shows how **AMC23C12** can be used for bidirectional in-phase overcurrent detection.

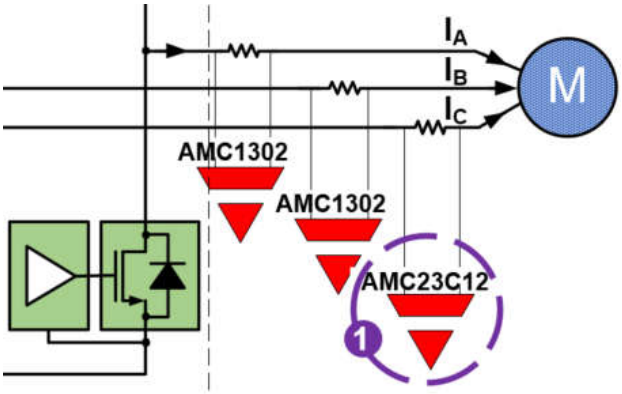


Figure 108. *Bidirectional in-phase overcurrent detection.*

In a fully operational three-phase AC motor-drive system, the sum of three-phase current to the AC motor should be zero, regardless of braking or running conditions (that is, IA + IB + IC = 0).

Calculating the third-phase current in low- to mid-end motor drives from measured current on two phases can help reduce costs. I recommend monitoring the current on the third phase to detect any electrical fault events. While you could place a current sensor on the third phase with an isolated amplifier or isolated modulator, you could also use a reinforced isolated window comparator **AMC23C12** for simplicity, cost-effectiveness and solution size. The AMC23C12offers bidirectional overcurrent detection with an integrated window comparator.

As shown in location 1 of **Figure 108**, a shunt resistor produces a voltage drop that the AMC23C12 reinforced window comparator senses. The AMC23C12 has an open-drain output, OUT, which actively pulls low when the input voltage exceeds the pre-defined threshold values of the voltage on the reference pin for the purposes of overcurrent detection. **Figure 109** shows an overcurrent event output waveform.

For both overcurrent and short-circuit detection, you can use the AMC23C14 dual window comparator.

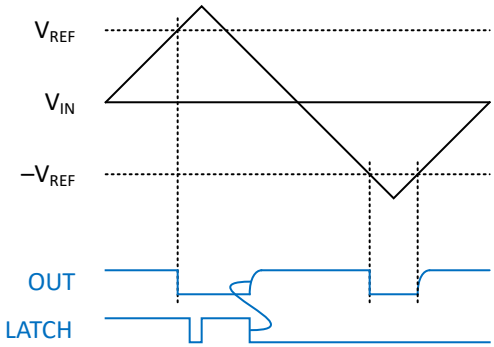


Figure 109. *AMC23C12 output waveform.*

Use case No. 2: DC+ overcurrent detection

As shown in location 2 of **Figure 110**, the **AMC23C11** can be a good choice for DC+ overcurrent detection.

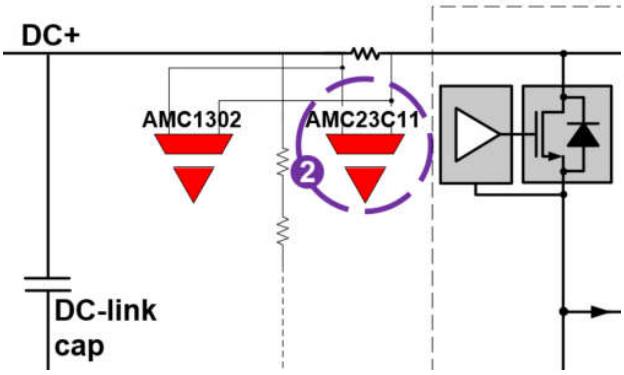


Figure 110. *DC+ overcurrent detection.*

Figure 111 shows an overcurrent event output waveform. Like the AMC23C12, the AMC23C11 has an open-drain output, OUT, that actively pulls low when the input voltage exceeds the pre-defined threshold value of the voltage on the reference pin. The AMC23C11 also supports latched mode with a LATCH input pin that clears the output only after the latch clears. If you require both overcurrent and short-circuit detection, you can use the AMC23C14 to set the two threshold levels for overcurrent and short-circuit detection, respectively.

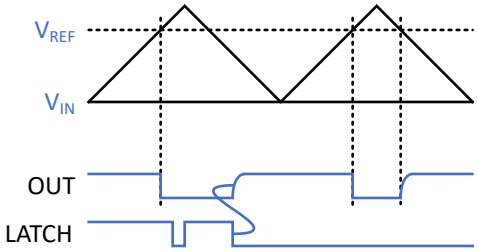


Figure 111. *AMC23C11 output waveform.*

Use case No. 3: DC– overcurrent or short-circuit detection

Similar to the details as explained in use case No. 2, you can also use the AMC23C11 to detect overcurrent on the DC– line. If you require both overcurrent and short-circuit detection, you can use the AMC23C14 to set the two threshold levels for overcurrent and short-circuit detection, respectively.

Use case No. 4: DC-link (DC+ to DC–) overvoltage and undervoltage detection

The DC-link voltage should be within the specified range for proper operation of the motor drive. The AMC23C14 can be a good choice for detecting overvoltage and undervoltage conditions.

As shown in location 4 of **Figure 112**, the bottom resistor of a resistor-divider network produces a voltage drop that is sensed by the AMC23C14 dual reinforced window comparator.

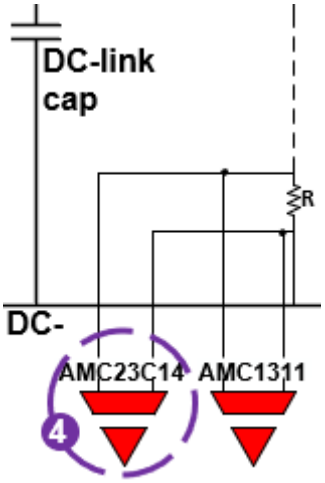


Figure 112. *DC-link overvoltage and undervoltage detection.*

The AMC23C14 has two open-drain outputs, OUT1 and OUT2, one for each window comparator. OUT1 actively pulls low when the input voltage exceeds the pre-defined threshold valuesof the voltage on the reference pin for the purposes of undervoltage detection. OUT2 actively pulls low when the input voltage exceeds the threshold values defined by the internal 300-mV reference for the purposes of overvoltage detection. **Figure 113** shows the OUT1 and OUT2 outputs for overvoltage and undervoltage events. If you only require overvoltage detection, you can use the AMC23C11.

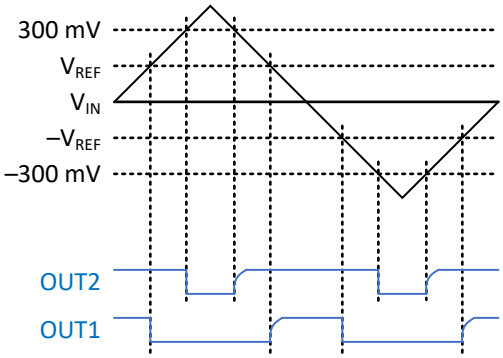


Figure 113. *AMC23C14 output waveform.*

Use case No. 5: IGBT module overtemperature detection

As shown in **Figure 114**, a negative temperature coefficient thermistor (NTC) is typically placed inside the IGBT module for the detection of long-term overload conditions. These NTC terminals are routed to the main power board, where the AMC23C14 can be used for overtemperature detection.

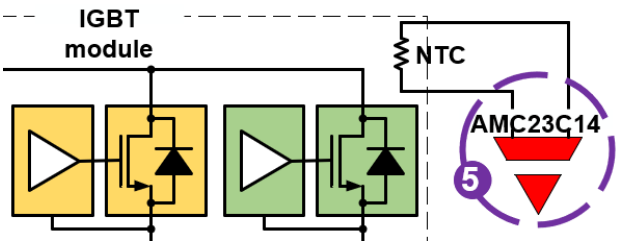


Figure 114. *IGBT module overtemperature detection.*

Figure 115 shows the output waveform for an overtemperature event, where OUT2 pulls high when the input voltage exceeds the threshold values defined by the internal 300-mV reference. The reference pin of the AMC23C14 connects to a 100-µA current source that can bias the NTC.

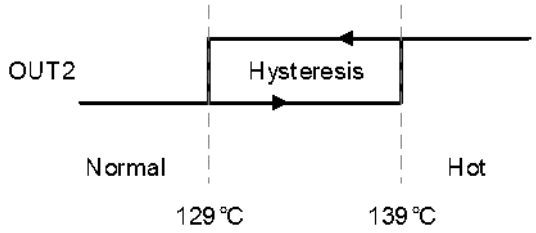


Figure 115. *AMC23C14 output waveform.*

As the demand to improve system reliability and the adoption of faster switching devices proliferates, the **AMC23C14** family of low-latency reinforced isolated comparators solves the critical need for accurate and fast detection in electric motor drives

Discrete DESAT for Opto-Compatible Isolated Gate Driver UCC23513 in Motor Drives

Abstract

Reinforced isolated gate drivers are key components in 3-phase inverters for industrial motor drives, and DESAT is a popular approach for overcurrent protection (OCP) or short circuit protection (SCP) in these applications. This application note presents a small form factor, cost-optimized design based on the 6-pin opto-compatible reinforced isolated gate driver UCC23513 with a discrete DESAT implementation using the isolated comparator AMC23C11. This combination achieves a smaller PCB size and lower cost, compared to the 16-pin package smart gate drivers with integrated DESAT protection, and helps to enhance flexibility in applications of compact motor drives. The design also keeps the flexibility to configure the application parameters of the DESAT function.

Introduction

In 3-phase inverters for motor drives, OCP and SCP are critical to protect the system from damage caused by abnormal operating conditions. Shunt-based system level OCP or SCP are often implemented by sensing the current through the negative DC bus or the three low-side switches; especially in many lower power, compact models, where form factor and system cost are critical. These protections are effective for the commonly seen fault patterns of arm shoot-through and phase-to-phase short. However, neither of them can detect an earth ground short when the fault current flows through a high-side switch, as shown in **Figure 116**. A DESAT function on the gate driver can help to protect the power switch against this fault. In fact, device level DESAT protection is effective to all these fault modes in a 3-phase inverter, thus has been widely used in many high power, high performance models.

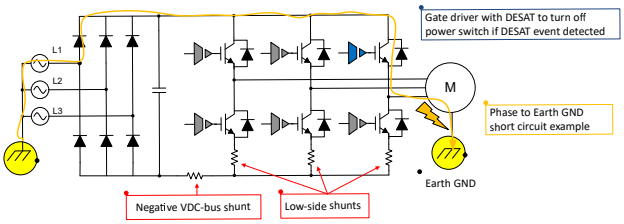


Figure 116. *Short Circuit Due to Earth Ground Fault in A 3-Phase Inverter*

Many industrial motor drives also have a regeneration brake switch to shunt the current to the negative VDC- bus and discharge the bulk capacitor when the voltage goes too high during a regeneration brake operation. Often this brake resistor needs to be installed externally and then connected to the system by a specific terminal on the drive. If a user makes an error in connecting this resistor, or mistakenly used one with a very low resistance, an overcurrent fault can occur once a brake operation is started by the system controller, as shown in **Figure 117**. In this case, a DESAT function on the gate driver can detect the problem and protect the power switch in time.

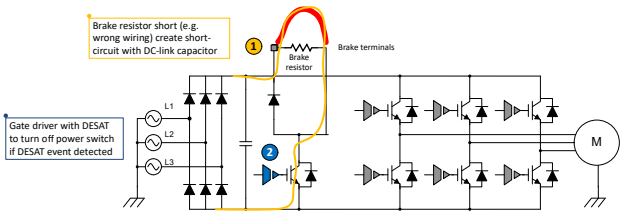


Figure 117. *Short Circuit Due to Miswiring of External Brake Resistor Terminal*

A typical approach to protect the system against these faults uses an isolated smart gate driver with DESAT function, like the UCC21750 reinforced isolated gate driver with CMOS input. As seen in **Figure 118**, a DESAT pin monitors the voltage drop of V_{CE} when the IGBT is turned ON. Once this voltage drop goes up and reaches the set threshold, which means an over current or short circuit condition is happening, the output of the gate driver will be pulled to low at once and a fault output wii be activated to inform the system controller on the fault.

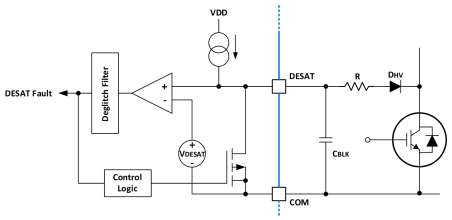


Figure 118. *UCC21750 With Integrated DESAT Protection*

System Challenge on Isolated Gate Drivers With Integrated DESAT

Reinforced isolated smart gate drivers with integrated DESAT function are typically offered in a 16-pin SOIC package, which is physically much larger than a compact gate driver without DESAT function in a stretched SO-6 package, as is shown in **Figure 119**. Consider placing six pieces of such devices of a 3-phase inverter on a power inverter PCB, the package length will stack up accordingly. A design using a shorter length compact device can offer an advantage on the PCB size. Even for a regeneration brake power switch, a smaller size gate driver can help to reduce the application layout area significantly. However, such gate drivers sacrifice the overcurrent protection function for application circuit simplicity and cost reasons.

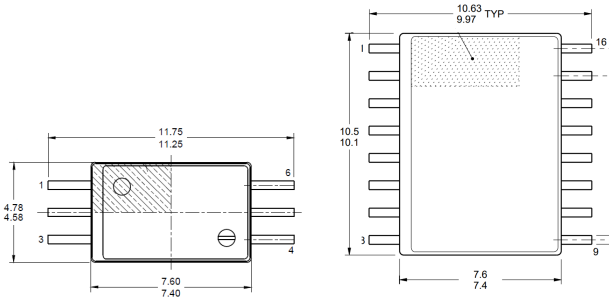


Figure 119. *Package Size Comparison: SO-6 vs. SOIC-16*

An alternative approach is to use the smaller footprint compact gate driver without DESAT and implement the DESAT function discretely using an isolated comparator.

For circuit configurations that only require DESAT function on either the three low-side switches or the three high-side ones, this discrete DESAT design allows all six switches to use a same 6-pin reinforced isolated gate driver; thus avoids mixing simple gate drivers with smart gate drivers in one application system. The external DESAT function can be added to the low-side or high-side gate drivers, respectively. This discrete DESAT implementation adds flexibility to the application design to configure parameters of DESAT voltage, DESAT bias current, DESAT detection blanking time, and DESAT output deglitch filter, thus helps to increase immunity against the PWM switching noise.

System Approach With UCC23513 and AMC23C11

The UCC23513 is a 4-A source, 5-A sink, 5.7-kV_{RMS} reinforced isolated, opto-compatible single channel gate driver. The AMC23C11 is a fast response, reinforced isolated comparator with adjustable threshold and latch function. Using the two devices together, we can achieve an external DESAT on the compact gate driver and maintain a small circuit form factor with reinforced isolation.

System Overview and Key Specification

Figure 120 shows a simplified block diagram of the proposed circuit. Here, we use an IGBT as the power switch; and the design is also appropriate for a power MOSFET with some minor changes.

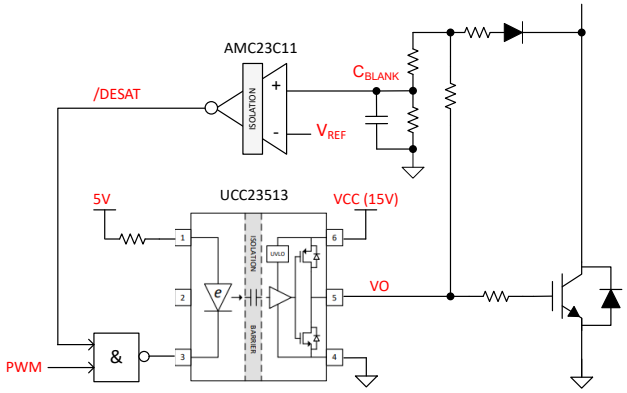


Figure 120. *Simplified System Block Diagram*

A NAND gate is used to realize a function to monitor the V_{CE} only when the PWM input is high. The chip disables the gate driver's input, once the sensed V_{CE} exceeds the DESAT threshold VREF. **Table 16** shows the key parameters of the application circuit.

Table 16. Key System Parameters of the Design

Parameter	Value	Comment
Reinforced isolated gate driver	UCC23513 or UCC23511(1)	6-pin DWY (SO-6) package, see figure 2-1. B version to support 8-V UVLO.
Isolated gate drive supply, VDD	+15 V (IGBT), +12 V (FET)	Unipolar supply
DESAT V_{CE} threshold voltage, $V_{CE(DESAT)}$	8.0 V	Configurable. See section 3.2.2.
DESAT bias current, $i_{BIAS(DESAT)}$	5.5 mA	Configurable. See section 3.2.2.
DESAT blanking filter time constant, t_{BLANK}	0.8 µs	Valid for $V_{CE(SAT)}$=12.5V. Configurable. See equation 8 and table 3-2 in section 3.2.3.
DESAT deglitch filter delay, $t_{DEGLITCH}$	0.2 µs	Configurable. See equation 10 in section 3.2.3.
DESAT latch with reset	Enabled	Can be disabled.
DESAT reaction time(2)	About 1.1 µs to 1.6 µs	By default configuration. Refer to test results.
PCB size without connectors	26 mm x 8.4 mm	

Note

(1) UCC23511 is a 1.5-A source, 2-A sink device in same package as UCC23513.

(2) For clear and simple description on the protection process, in this application note, we use 'DESAT reaction time' for the period from the sensed power switch's current reaches to the set trigger level to the point the current begin to drop due to the DESAT protection.

The UCC2351x series can be used to drive power switches of IGBT, SiC, or MOSFET. Both UCC23511 and UCC23513 are offered in a stretched SO-6 package of 7.50 mm x 4.68 mm body size, with greater than 8.5 mm creepage and clearance. Both devices bring significant performance and reliability upgrades over the standard optocoupler based gate drivers while maintaining pin-to-pin compatibility. Their performance advantages include high CMTI, low propagation delay, and small pulse width distortion. The input stage is an emulated diode (ediode) which provides long term reliability and excellent aging characteristics over the traditional LEDs.

The AMC23C11 isolated comparator comes in a 8-pin wide-body SOIC package with a body size of 5.85 mm × 7.50 mm. The device compares the input voltage on the VIN pin against a threshold, adjustable from 20 mV to 2 V, and set by an internal 100-µA reference current and an external resistor. The open-drain output is actively pulled to low when the input voltage VIN is higher than the reference value VREF. When VIN drops below the trip threshold, the device's behavior is determined by the LATCH pin:

- When the LATCH pin is pulled to low, the device is set to transparent mode, allowing the output state to change and follow the input signal with respect to the trip threshold.
- When the LATCH pin is pulled to high, the device is set to latch mode. Once an out-of-range condition is detected, the OUT pin is pulled to low and latched, until the LATCH pin is pulled to low for at least 4 µs to release this latch.

The isolation barrier in AMC23C11 is highly resistant to magnetic interference, and certified to provide a reinforced galvanic isolation of up to 5 kV_{RMS}.

Schematic Design

Figure 121 shows the schematic of a design with a 15-V unipolar supply to drive an IGBT. With some minor changes this design can be fit to a 12-V power supply design for power MOSFETs driving or bipolar power supply applications. See reference design **TIDA-00448** for more details.

Resistors R9 through R14 and the high voltage diode D1 are used to sense the actual V_{CE} of the IGBT during the turn-on period and scale it according to the reference voltage VREF of the isolated comparator AMC23C11. R10 and R11 are in parallel to spilit the power dissipation.

The capacitor C14 in parallel to R14 sets a blanking time to avoid false trig during the IGBT turn-on. A 5.1-V Zener diode D2 is added as an option to suppress possible high voltage spikes due to the IGBT switching. Note that the internal capacitance of D2 will be in parallel to C14 and contribute to the blanking time. In our tests we did not assemble this D2. A fast switching diode D1 with low internal capacitance is recommended to avoid false DESAT trigger and minimize the blanking time required.

The low voltage side uses a 3.3-V supply to directly interface the I/O level of popular MCUs, like the C2000™ and the Sitara MCUs. R6 and C11 set a deglitch delay (default 0.2 µs) for the comparator's output, in case of the LATCH is not activated.

Circuit Schematic

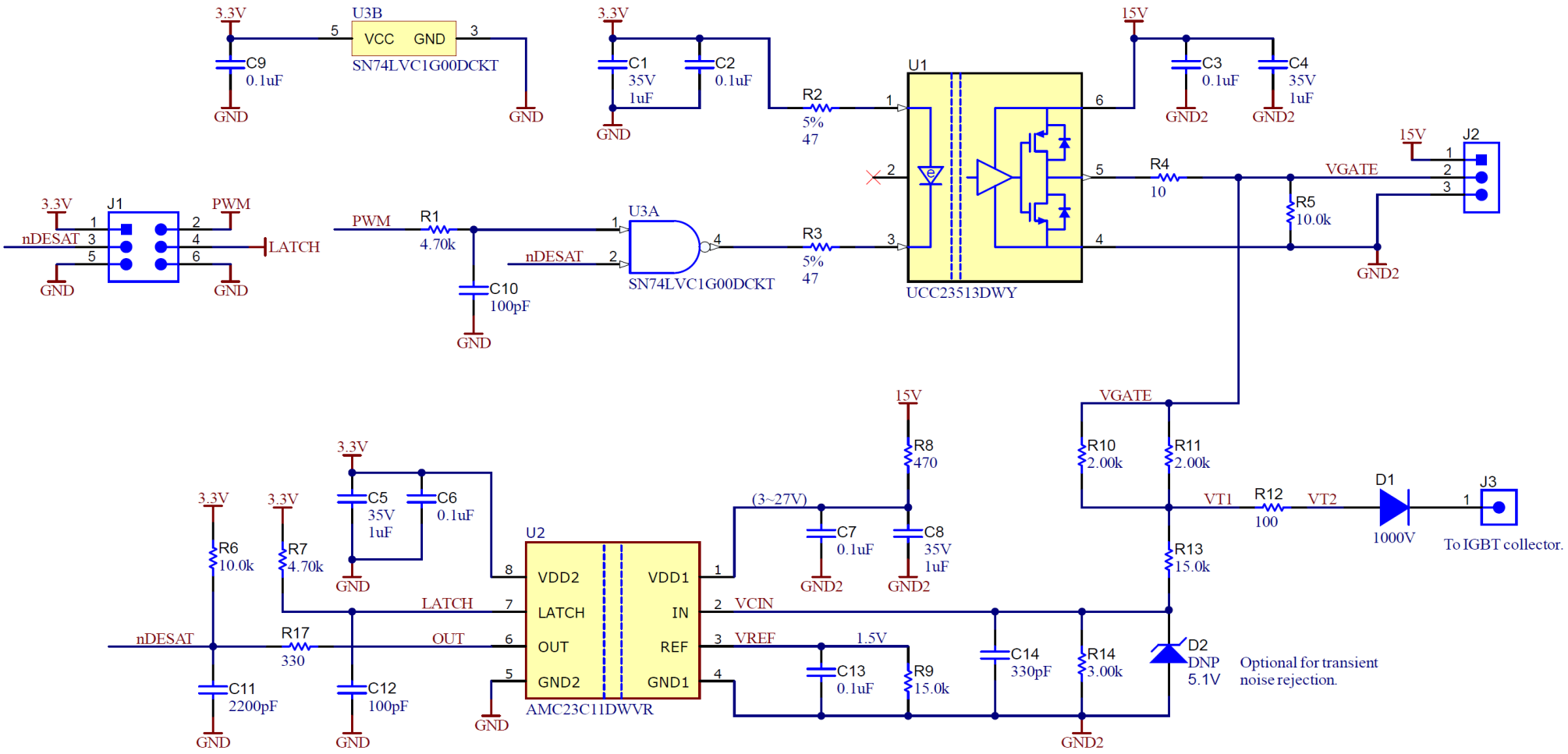


Figure 121. *Schematic of the Proposed Circuit*

Configure $V_{CE(DESAT)}$ Threshold and DESAT Bias Current

Resistors R9 to R14 can be used to adjust the $V_{CE(DESAT)}$ threshold and the DESAT bias current $i_{BIAS(DESAT)}$. The following equations are simplified for a quick estimation on their values for different DESAT threshold and DESAT bias current configurations.

The isolated comparator AMC23C11 has a reference voltage VREF which is set by an internal 100 µA current source and the external resistor R9. The value of R9 is calculated per **Equation 49** to set the VREF to 1.5 V in this design. Here 1.5 V is chosen to make the AMC23C11 to operate in the high-hysteresis mode[1].

$$\mathrm{R9} = \frac{VREF}{100\ \mu\mathrm{A}} = 15\ \mathrm{k\Omega} \tag{49}$$

R10 and R11 determine the DESAT bias current and are calculated per **Equation 50**:

$$\mathrm{R10} = \mathrm{R11} = 2 \times \frac{VDD - V_{CE(DESAT)} - V_{FW(D1)} - R12 \times i_{BIAS(DESAT)}}{i_{BIAS(DESAT)} + i_{R13R14(DESAT)}} \tag{50}$$

Here:

- VDD is the UCC23513's supply voltage; 15 V in this case for IGBT driving;
- $V_{CE(DESAT)}$ is the desired DESAT threshold; 8 V by default in this design;
- $V_{FW(D1)}$ is the forward voltage of the high-voltage diode D1; assumed to be 0.5 V;
- R12 is set to 100 Ω as a common practice[9];
- $i_{R13R14(DESAT)}$ is the current through R13 and R14. Set to 0.5 mA. Lower setting may reduce noise immunity.
- $i_{BIAS(DESAT)}$ is DESAT bias current when the IGBT's V_{CE} reaches $V_{CE(DESAT)}$. Set to 5.5 mA in this design.

So R10 and R11 could be calculated at 2 kΩ for this design.

The power rating of R10 and R11 needs to be selected for normal IGBT operation, where the $V_{CE(DESAT)}$ is significantly smaller. Assuming R12 << R10, the simplified maximum power losses are per **Equation 51**:

$$P_{R10,\ MAX} = P_{R11,\ MAX} = \frac{\left(VDD - V_{FW(D1)} - R12 \times i_{BIAS(DESAT)} - V_{CE(SAT)}\right)^2}{R10} \times PWM_{DUTY,\ MAX} \tag{51}$$

With the default settings in table 3-1 and a typical $V_{CE(SAT)}$ of 1.5V, the maximum power losses of $P_{R10(MAX)}$ and $P_{R11(MAX)}$ are around 69.8 mW even at 1000% PWM duty cycle.

R13 and R14 are calculated per **Equation 52** and **Equation 53**:

$$\mathrm{R13} = \frac{VREF}{i_{R13R14(DESAT)}} \tag{52}$$

$$\mathrm{R14} = \frac{VDD - \left(i_{BIAS(DESAT)} + i_{R13R14(DESAT)}\right) \times R10 \div 2}{i_{R13R14(DESAT)}} - R13 \tag{53}$$

Applying the parameters' values, we can get R13 of 3 kΩ and R14 of 15 kΩ.

DESAT Blanking Time

The blanking time for DESAT monitoring, the t_{BLANK} , is required to prevent false trig at the turn-on event of the IGBT. Capacitor C14 and resistors of R10 to R14 delay the V_{CE} sensing signal to reach the isolated comparator's input VCIN.

The delay is controlled by the charging time of C14 through the equivalent resistance R_{EQ} of the voltage divider R13 and R14:

$$R_{EQ} \approx R13 \,//\, R14 = 3\,\text{k}\Omega \,//\, 15\,\text{k}\Omega = 2.5\,\text{k}\Omega \quad (54)$$

Choose a C14 of 330 pF, then the time constant of the RC filter is:

$$T_{au} = R_{EQ} \times C14 = 2.5\,\text{k}\Omega \times 330\,\text{pF} = 0.82\,\mu\text{s} \quad (55)$$

The actual blanking time depends on the ratio of the configured $V_{CE(DESAT)}$ steady state threshold over the actual $V_{CE(SAT)}$ voltage of the IGBT in an over-current event, and can be approximated per **Equation 56**.

$$t_{BLANK} = -\ln\left(1 - \frac{V_{CE(DESAT)}}{V_{CE(SAT)}}\right) \times R_{EQ} \times C14 \quad (56)$$

Therefore, it is important to adjust the steady state $V_{CE(DESAT)}$ threshold and the blanking time constant according to the individual IGBT used in the system. Refer to below table for some values with the default settings of the $V_{CE(DESAT)}$ steady state threshold at 8 V:

Table 17. Effective Blanking Time With Default $V_{CE(DESAT)}$ Setting

IGBT $V_{CE(SAT)}$ [V]	≥ 14.5	12.5	11	10	9	8.5
t_{BLANK} [µS]	0.7	0.9	1.1	1.4	1.9	2.4

CAUTION

Avoid to configure the steady state threshold $V_{CE(DESAT)}$ too close to the IGBT's actual $V_{CE(SAT)}$ in an over-current condition, since the effective blanking time will be significantly larger than the configured blanking time constant.

DESAT Deglitch Filter

R17 and C11 form a deglitch filter for the nDESAT output signal with a time constant:

$$\tau = 330\,\Omega \times 2200\,\text{pF} = 726\,\text{ns} \quad (57)$$

When a TTL logic IC with a minimum low-level input of 0.8 V is followed, the deglitch time is merely 0.2 µs:

$$t_{DEGLITCH} = -\ln\left(1 - \frac{0.8\,V}{3.3\,V}\right) \times \tau = 202\,\text{ns} \quad (58)$$

Consider the isolated comparator's internal resistance on the OUT pin is in series with R17, the tested deglitch time is about 340 ns to 380 ns in this design. Refer to test results in section 4 for details.

Reference PCB Layout

A reference layout is made for this circuit with an active area of 26 mm x 8.4 mm on a four-layer PCB.

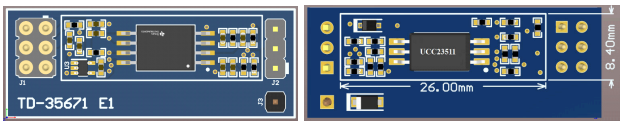


Figure 122. *Top and Bottom Sides of the Example Layout*

With careful layout design placing the gate driver and the comparator on the opposite sides of the PCB, a smaller form factor is achieved, compared to a 16-pin smart gate driver's, taking advantage of their smaller package lengths. In comparison, a typical layout of ISO5451, a smart gate driver with CMOS input in a SOIC 16 package, has an active area of 20.83 mm x 12.95 mm on the PCB[10], as shown in **Figure 123**, which is about 23.5% bigger than the proposed design of UCC23513 and AMC23C11 in **Figure 122**.

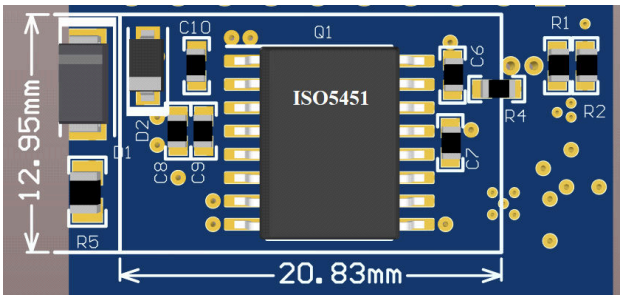


Figure 123. *Typical Layout of the Smart Gate Driver ISO5451*

Simulation and Test Results

Simulation Circuit and Results

Simulations have been made for the circuit to drive a low side IGBT of an active brake circuit in PSpice™ for TI. **Figure 124** shows the schematic for the simulation.

The simulation uses an AMC23C14's PSpice™ simulation model as the model of AMC23C11 is yet unavailable on ti.com. For the DESAT implementation discussed in this application note, the circuitry connected to the OUT2 (pin7) in the schematic can be ignored, and the AMC23C14 shows the same behavior as the AMC23C11 with the LATCH input (pin7) tied to low.

Simulation Circuit

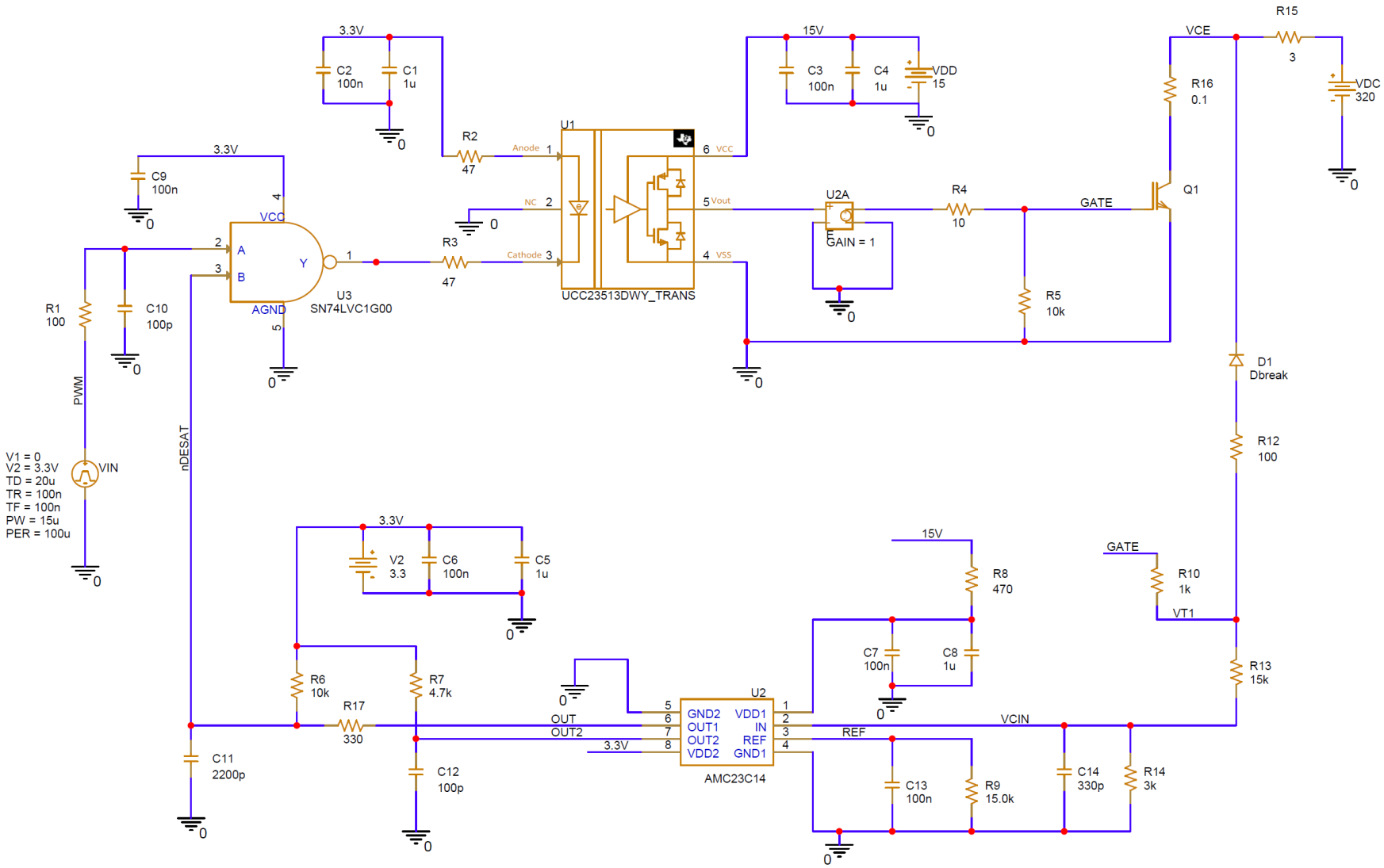


Figure 124. *Simulation Circuit*

Simulation Results

In this simulation, the input PWM signal is set to 10 kHz, 15% duty cycle square waveform. Other conditions are set to a common application situation. **Figure 125** is a simulation result on a DESAT protection case.

In static state, the PWM input is low, so the NAND gate output is high. UCC23513 has no input current, so the output on the GATE is also low. Thus, the isolated comparator AMC23C11's input voltage of VCIN is pulled to zero; the output OUT and the nDESAT are pulled to high.

When the input PWM signal goes to high, the NAND gate's output will shift to low, as long as the nDESAT is still in high. The UCC23513 then gets the input current and outputs high on the GATE. Then the IGBT U4 turns on and the V_{CE} drops to the $V_{CE(SAT)}$. A sense current flows from GATE through R10, R12 and D1 to the collector of the IGBT U4, makes the VT1 node's voltage follow the IGBT's actual V_{CE} and the VCIN voltage follow the VT1 voltage through the resistor divider of R13 and R14. In case the VCIN does not reach the threshold of VREF, the comparator's output OUT and the filtered output nDESAT will remain at high.

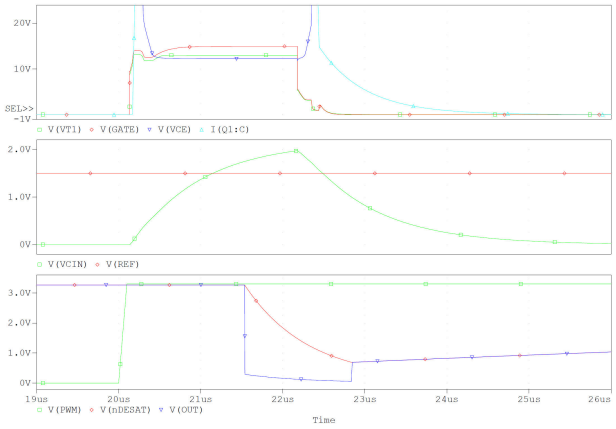


Figure 125. *Simulation Result of DESAT Triggered*

In case of a DESAT triggered process, as shown in the above figure, when the input PWM signal (green trace in the bottom plot) goes to high, the GATE voltage of the IGBT (the red trace in the top plot) will rise up soon after, and the IGBT's V_{CE} sense voltage VT1 (green trace in the top plot) will also rise up. The comparator's input VCIN (the green trace in the middle plot) will then begin to rise up to follow the VT1 voltage in proportional.

Then the IGBT's V_{CE} (blue trace in the top plot) begins to drop. When V_{CE} drops to below the GATE voltage, the VT1 voltage begin to follow the V_{CE}.

Before the VCIN reaches the 1.5 V trigger threshold, set by the VREF (the red line in the middle plot), the comparator's output OUT (the blue trace in the bottom plot) will remain at high. Once VCIN reaches the trigger level, the comparator's OUT will be pulled to low with an internal propagation delay of 240 ns typically. The filtered output of nDESAT (the red trace in the bottom plot) will begin to drop, too.

As an input to the NAND gate U3, once the nDESAT triggers the negative going threshold of U3, the gate driver U1's input current will be cut off and the output GATE will be pulled down. Thus the IGBT will also be turned off and the V_{CE} will rise up soon. This process is the DESAT protection of the circuit.

As the GATE is pulled down, the VT1 will also be pulled down and the VCIN will begin to drop. When VCIN drops to below the threshold of the comparator's input, the OUT will rise up again. This is the case with AMC23C14.

The AMC23C11 behaves exactly the same as the above process when pin 7, the LATCH input, is tied to low. When the LATCH pin is pulled to high, the output low on the comparator's OUT pin will be latched; untill the LATCH pin is pulled to low for at least 4 µs to release the latch state.

Test Results With 3-Phase IGBT Inverter

Tests have been conducted on a sample board of the proposed circuit on DESAT protection. Two cases were tested, in which the sample board was used as (1) the gate driver of a low-side brake IGBT, and (2) the gate driver of a high-side switch IGBT in a 3-phase motor drive inverter.

Brake IGBT Test

Figure 126 shows the platform for the low-side brake IGBT gate driving tests. A C2000™ LaunchPad™ of **LAUNCHXL-F28379D** has been used as the system controller to generate a series of PWM pulses of 10 kHz with 10% duty cycle, or 10 µs ON time in each 100 µs period, to drive a low-side IGBT. The LaunchPad also generates a high output for the LATCH input of the AMC23C11 and monitors the nDESAT signal with a GPIO.

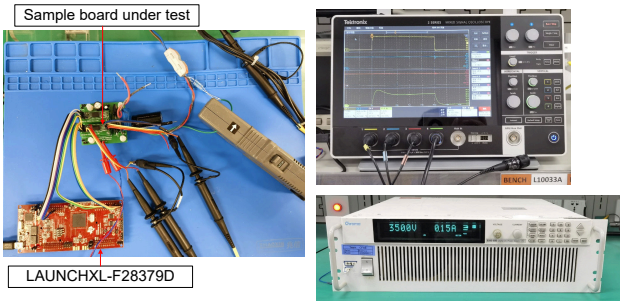


Figure 126. *Platform for the Low-Side Driving Test*

To test on an OCP or SCP situation, a 600-V 10-A discrete IGBT is used and two 1.5-Ω 3-W resistors are put in parallel to emulate a brake resistor. The resistors are inserted between the IGBT collector and the 350-V DC+ rail. The test result is show in **Figure 127**.

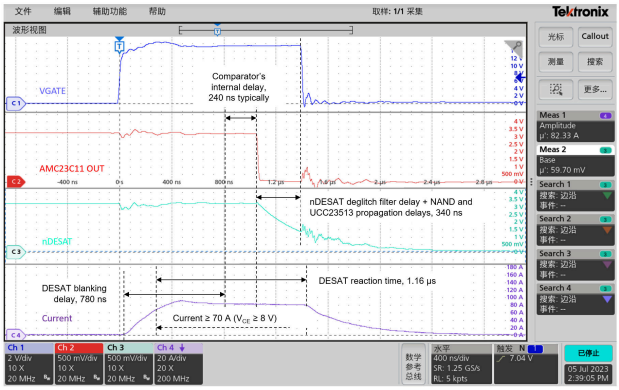


Figure 127. *Short-Circuit Protection Delays in Low-side Driving Test*

In this test, once the IGBT was turned on (t = 0 s), the collector current began to rise up and soon got saturated at around 90 A (t = 480 ns). According to the tested IGBT's data sheet, when the collector current reaches 70 A, the V_{CE} will

increase to the 8 V trigger level set for the circuit. DESAT was detected by the isolated comparator AMC23C11 after a blanking time of around 780 ns. Then, after an internal delay of 240 ns typically, the AMC23C11's OUT shifted to low (t = 1.04 µs) and latched (when LATCH is set to high). After another delay by the deglitch filter for nDESAT of about 340 ns, the NAND gate SN74LVC1G00's output shifted to high and cut off the USS23513's input current, made the gate driver pulling the VGATE down (t = 1.44 µs). The DESAT reaction time, from IGBT's the current reached 70 A to the point the current began to drop after the GATE turned to low, was only about 1.16 µs.

Test Results on a 3-Phase Inverter With Phase to Phase Short

Tests on a 3-phase inverter platform of a TI reference design, the **TIDA-010025**, have been performed to check a phase to phase short circuit condition when driving an ACIM motor. In these tests, the U phase high side IGBT's gate driver was replaced by a sample board of the proposed circuit:

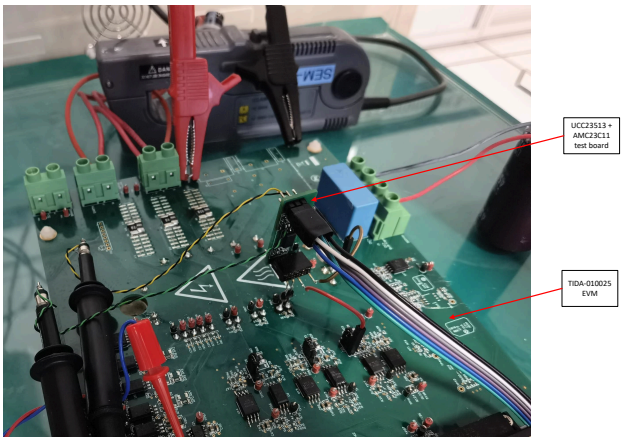


Figure 128. *Platform for Run Motor Test*

The TIDA-010025 reference design has a 1200-V, 25-A PIM power module on the power board, which has integrated six pieces of IGBT with the same ratings in the 3-phase inverter stage. To prepare for the tests, we first removed the original gate driving resistor for the U phase high-side IGBT, then connected the VGATE output, the 15-V power supply, and the VCE sense terminal of the sample board to the power board. To avoid the influence of the reference design's own hardware OCP function, we added a 5 mΩ shunt resistor in parallel to the original 10 mΩ one in all three phases, so that we can triple the OCP trigger level to 72 A. After checked on the output characteristics of the IGBTs, we also made some changes on our sample board for the DESAT threshold to be reached when the $V_{CE(SAT)}$ goes up to 2.5 V, which is corresponding to about 45 A collector current. During these tests, we first run the motor (with no load) to 50 rps, then short the inverter's U and W phases with a circuit breaker connected to the terminals of the power board. **Figure 129** is a test result waveform.

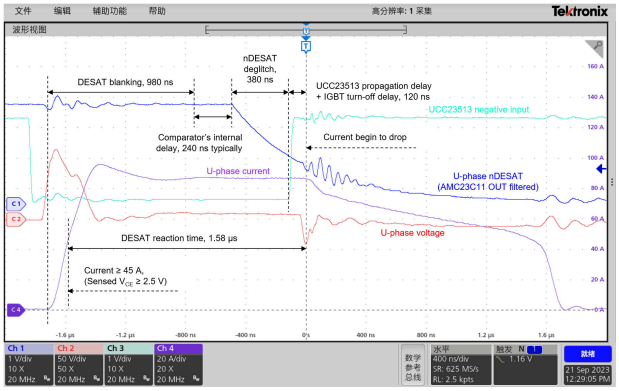


Figure 129. *Short-Circuit Protection Delays in Run Motor Test*

Once the circuit breaker was turned on, the U and W phases got shorted, and the U-phase current began to rise up rapidly. The saturate current soon reached a peak of about 95 A, then dropped a little and got stable at around 86 A. After a blinking time of 980 ns, the AMC23C11 detected the DESAT condition. After another internal propogation delay of 240 ns typically, the output OUT shifted to low. It took about 380 ns for the nDESAT to drop to the NAND gate input's negative going threshold and cut off the UCC23513's input current. The gate driver then took about 120 ns to make the IGBT's current began to drop off. The DESAT reaction time was about 1.58 µs in total.

There are some differences to the results in the low-side driving test. The differences in the two tested IGBTs' characteristics and the application circuits along with the DESAT threshold adjustment have contributed to these variations.

Summary

The combination of a compact, isolated simple gate driver with an isolated comparator for DESAT protection has been validated in this application note. The discrete approach reduces the design size compared to a 16-pin smart gate driver with integrated DESAT. This approach also adds flexibility to configure the key parameters for the DESAT function such as threshold, bias current, blanking time, and deglitch filter. The discrete approach also offers a DESAT latch function which can be reset by the MCU too.

This concept can also be expanded to bipolar gate driver supplies, and is equally fitting for both low-side and high-side gate drivers. For more details on these applications, refer to **TIDA-00448**.

References

1. Texas Instruments, **AMC23C11: Fast-Response, Reinforced, Isolated Comparator With Adjustable Threshold and Latch Function**, data sheet.
2. Texas Instruments, **UCC23513: 4-A Source, 5-A Sink, 5.7-kVRMS Opto-Compatible Single-Channel Isolated Gate Driver** data sheet.
3. Texas Instruments, **UCC23511: 1.5-A Source, 2-A Sink, 5.7-kVRMS Opto-Compatible Single-Channel Isolated Gate Driver** data sheet.
4. Texas Instruments, **UCC21750: 10-A Source/Sink Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Active Protection, Isolated Analog Sensing and High-CMTI** data sheet.
5. Texas Instruments, **AMC23C14: Dual, Fast Response, Reinforced Isolated Window Comparator With Adjustable Threshold** data sheet.

6. Texas Instruments, **ISO5451: 5.7kVrms, 2.5A/5A single-channel isolated gate driver with active protection features**, data sheet.
7. Texas Instruments, **PSpice for TI design and Simulation** tool.
8. Texas Instruments, **UCC21750: How can we adjust the DESAT detection threshold in UCC217xx & ISO5x5x?** FAQ.
9. Texas Instruments, **TIDA-00448: Flexible High Current IGBT Gate Driver with Reinforced Digital Isolator** reference design.
10. Texas Instruments, **TIDA-00638: Reference Design for Isolated Gate Driver Power Stage with Active Miller Clamp for Solar Inverters** reference design.
11. Texas Instruments, **TIDA-010025: Three-phase inverter reference design for 200-480 VAC drives with opto-emulated input gate drivers** reference design,

Isolated voltage sensing in AC motor drives

Introduction

Automotive and industrial end equipment such as **motor drives**, **string inverters** and **onboard chargers** operate at high voltages that are not safe for direct interaction with humans. Isolated voltage measurements help optimize operation and ensure the safety of humans by protecting them from the high-voltage circuit performing a function.

Designed for high performance, isolated amplifiers transfer voltage-measurement data across an isolation barrier. The criteria for determining isolated amplifier selection includes isolation specifications, the input voltage range, accuracy requirements, and how you plan to power the high-voltage side – something that the measurement's location in the application will often influence.

This paper gives guidance on selecting the right isolated amplifier by evaluating three common voltage measurements in an AC motor-drive end equipment.

The first criterion is the required isolation specification; [**1**] covers the relevant isolation definitions. Texas Instruments (TI) isolated amplifiers and modulators are usually rated and certified at basic or reinforced isolation levels against device-level standards such as Deutsches Institut für Normung e.V. (DIN), Verband der Elektrotechnik Elektronik Informationstechnik e.V. (VDE) 0884-17, DIN European Norm (EN) International Electrotechnical Commission (IEC) 60747-17, and Underwriters Laboratories (UL) 1577. For additional information, see the device-specific data sheet and [**2**].

The selection of input voltage range, accuracy requirement and your high-voltage-side power method of choice depend on the location of the voltage node measured in the application. **Figure 130** is a simplified block diagram of an AC motor drive with the three common locations for voltage measurements: the AC mains on the left, the DC link in the middle and the motor phase on the right. Isolated amplifiers are excellent devices for these measurements because of their high accuracy and ease of use.

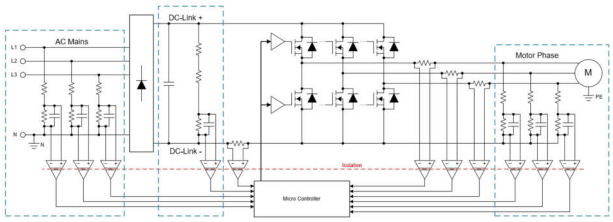


Figure 130. *An AC motor-drive application.*

Shown on the left side of **Figure 130**, the AC mains input is often connected as a three-phase center-earthed power system with voltages that are $120V_{RMS}$/208 V_{RMS} in the U.S. and 230 V_{RMS}/400 V_{RMS} in Europe. The required accuracy for this voltage measurement is typically low and not always needed. If you will be measuring the AC mains, consider devices with a bipolar high-impedance input such as TI's **AMC1350** or **AMC3330**. When making three-phase AC voltage measurements with respect to the neutral voltage, you can use a single isolated power supply for all three isolated amplifiers performing the measurement. When making three-phase AC voltage measurements phase-to-phase, consider using a device with an integrated C/DC converter to simply the design. **Figure 131** shows the corresponding AMC3330 circuit diagram.

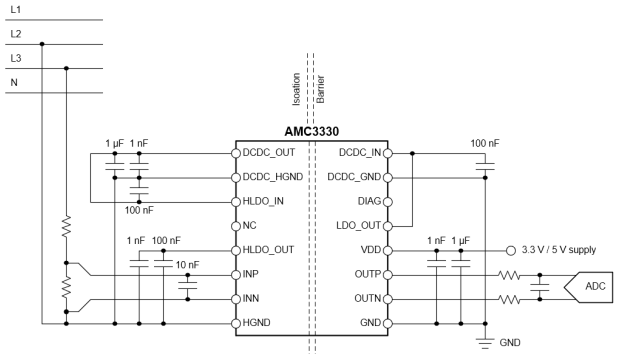


Figure 131. *The AMC3330 isolated amplifier with an internal DC/DC converter.*

Calculating the pulse-width modulation (PWM) duty cycle in a motor drive typically requires measurement of the DC link voltage shown in the middle of **Figure 130** with an accuracy of 1% or better.

During braking operation, the DC link voltage increases and needs to be actively limited to protect the power stage by switching on a regenerative brake, for example. A low-latency measurement provides a faster reaction time to overvoltage events and enables the system to operate closer to the limits of its hardware, enabling tighter design margins and lower system costs. The DC link capacitance is usually several 100 µF, and determining whether the DC link capacitor has been properly discharged to a safe level before servicing the equipment requires accurate measurements at low voltages (<100 V). Furthermore, high-resolution AC ripple measurements allow for a phase-detection loss of the connected AC mains, potentially eliminating the need for a separate grid-side phase measurement. The frequency of the ripple voltage is either 360 Hz for a 60-Hz three phase mains voltage or 300 Hz for 50-Hz three-phase mains voltage, as there are six half waves being rectified. At a low load (when the motor is not spinning), the magnitude of the ripple voltage can be very low; thus, you may prefer a modulator for the highest resolution measurements. For more information on isolated amplifiers vs. isolated modulators, see [3]. Isolated amplifiers with unipolar input ranges such as TI's **AMC1351** (with a 0- to 5-V input range) or the **AMC1311** (with a 0- to 2-V input range) are specifically designed for DC link voltage measurements. They require a local power supply referenced to DC- to power the high-voltage side such as the isolated transformer circuit shown in **Figure 132**. An alternative approach is to use a device such as the AMC3330 with an integrated DC/DC converter.

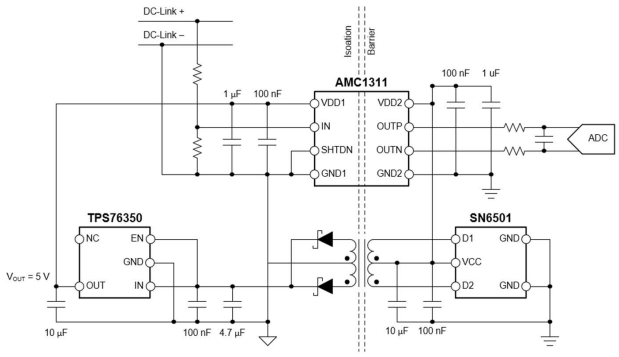


Figure 132. *The AMC1311 isolated amplifier with a discrete isolated transformer circuit.*

Measuring the actual phase voltage rather than estimating the phase voltage based on the DC-link measurement and PWM duty cycle further improves the performance of sensorless AC motor drives. The direct measurement of the phase voltage gives a more precise result because it includes all losses in the system and the effect of PWM dead-time

distortions. One method is to measure all three phases in respect to the DC– rail, with three unipolar-input isolated amplifiers and a single isolated power supply (as shown in **Figure 132**) to power the high side for all three isolated amplifiers.

An alternative method that saves on hardware cost is to measure only two phase-to-phase voltages and calculate the third. This method requires only two isolated amplifiers with a bipolar input range and minimal additional effort on the firmware side. The two measurements are made with respect to one of the phase voltages, which requires powering the isolated amplifiers from the floating high-side gate-driver supply of the top insulated gate bipolar transistor (IGBT), as shown in **Figure 133**. Devices with internal DC/DC converters such as the AMC3330 greatly simplify the circuit, enabling additional space savings and higher system efficiency.

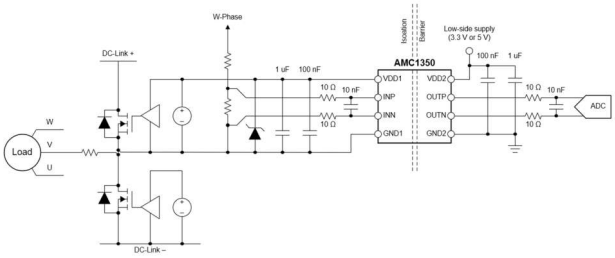


Figure 133. *The AMC1350 isolated amplifier with a floating power supply.*

For each of these voltage measurements, a resistor divider must scale down the high-voltage node to match the input range of the isolated amplifier [4]. There are three common challenges when designing a resistor-divider circuit:

- The input bias current from the isolated amplifier that flows through the sensing resistor, creating an offset error.
- The sensing resistor is in parallel with the isolated amplifier's input impedance, reducing the effective sensing resistance and creating a gain error. Additionally, the input impedance of the isolated amplifier can vary ±20% from device to device because of process variations and will appear as a gain error if unaccounted for.
- Temperature drift in both the resistor divider and input impedance of the isolated amplifier.

Selecting a device with high input impedance and negligible input bias current from TI's line of isolated voltage sensing amplifiers significantly reduces the required effort to overcome these challenges; however, it is possible to design a high-accuracy voltage measurement circuit using a low-input-impedance isolated amplifier with input bias current [5].

Isolated amplifiers with a wider input range provide lower sensitivity to input noise and allow higher accuracy at low input levels. However, higher input voltage devices often have lower input impedance, as shown in Table 1, and require gain calibration to achieve highest level of accuracy. A high-impedance-input device provides higher uncalibrated accuracy and reduces design effort. For more information when comparing data-sheet accuracy and the typical and maximum error calculations of TI isolated amplifiers, see [6].

Table 18. Voltage sensing isolated amplifiers from Texas Instruments.

Device	Input Voltage Range	Input Impedance	Integrated DC/DC	Automotive Available
AMC1211A-Q1	0 V to 2 V	1 GΩ	No	Yes
AMC1311/B	0 V to 2 V	1 GΩ	No	Yes
AMC1411	0 V to 2 V	1 GΩ	No	Yes
AMC1351	0 V to 5 V	1.25 MΩ	No	Yes
AMC3330	±1 V	1 GΩ	Yes	Yes
AMC1350	±5 V	1.25 MΩ	No	Yes

Table 18. Voltage sensing isolated amplifiers from Texas Instruments. (continued)

Device	Input Voltage Range	Input Impedance	Integrated DC/DC	Automotive Available
ISO224A/B	±12 V	1.25 MΩ	No	No

Conclusion

Texas Instrument's wide selection of isolated amplifiers for high-impedance voltage measurements allows you make the right trade-off between cost, performance, ease of implementation, and board space to optimize the design to your requirements and meet industry isolation performance standards.

References

1. Texas Instruments: ***Design considerations for isolated current sensing***
2. Texas Instruments: ***TUEV Technical Report No. 713203936***
3. Texas Instruments: ***Comparing Isolated Amplifiers and Isolated Modulators***
4. Texas Instruments: ***±480-V isolated voltage-sensing circuit with differential output***
5. Texas Instruments: ***Isolated Voltage-Measurement Circuit With ±250-mV Input and Differential Output***
6. Texas Instruments: ***Isolated Amplifier Voltage Sensing Excel Calculator***

Achieving High-Performance Isolated Current and Voltage Sensing in Server PSUs

Application Brief

The growing demand for cloud-based technology among internet content providers, communications service providers, and many consumer and business entities are driving a strong demand for data centers. The power-supply distribution networks in these data center servers, starting from the front-end power-factor correction (PFC) stage to the DC-DC stages, are required to meet high-efficiency and power density standards.

A certification standard, called 80 PLUS, developed by Electric Power Research (EPRI) in collaboration with Ecos consulting, promotes efficient energy use in data center server power-supply units (PSU). The server PSUs can receive one of the many 80 Plus certifications such as Gold, Platinum, and so forth, based on achievable energy efficiency at rated load and power factor (PF) levels.

Understanding Titanium Standard Requirements

The 80 Plus Titanium standard efficiency, PF and current total harmonic distortion (iTHD) requirements are shown in **Table 19**, **Table 20**, and **Table 21**, respectively.

Table 19. Titanium Standard Efficiency Requirements

	115-V Internal Non-redundant				230-V Internal Redundant				230-V EU Internal Non-redundant			
	Rated Load											
	10%	20%	50%	100%	10%	20%	50%	100%	10%	20%	50%	100%
Titanium Efficiency	90%	92%	94%	90%	90%	94%	96%	91%	90%	94%	96%	94%

Table 20. 80 Plus Titanium Standard PF Requirements

Output Power	10%	20%	50%	100%
Power Factor	> 0.90	> 0.96	> 0.98	> 0.99

Table 21. 80 Plus Titanium Standard iTHD Requirements

Output Power	> 5% and ≤ 10%	> 10% and < 20%	≥ 20%	≥ 40%	≥ 50%
iTHD	< 20%	< 15%	< 10%	≤ 8%	≤ 5%

High-Efficiency Server PSU Implementation

Figure 134 shows such an implementation of a server power supply with PFC and DC-DC stages. A non-isolated PFC stage ensures the rectified line current follows the rectified line voltage. This front-end PFC stage creates an intermediate DC bus with a relatively large ripple. An isolated DC-DC stage then provides galvanic isolation and a well-regulated output voltage with minimum output current ripple.

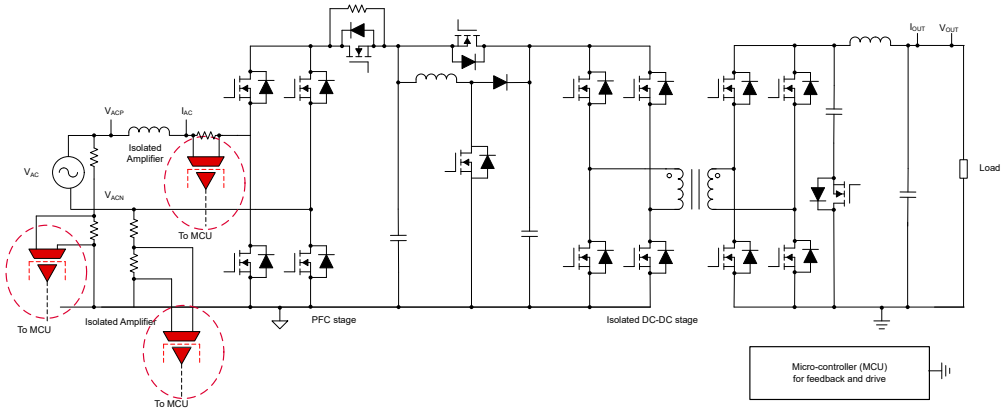


Figure 134. *Implementation of a Server Power Supply With PFC and DC-DC Stages*

The power factor for maximum efficiency should be close to unity. An efficient PFC is done by a single-phase totem pole bridgeless topology with a voltage and a current control feedback loop. The voltage feedback loop is used to regulate the PFC bus voltage to a preselected value and the current feedback loop regulate the total average inductor current. The current loop requires high measurement accuracy and high bandwidth to meet the Titanium standard efficiency, PF, and iTHD requirements. Depending on the architecture and the location of MCU, the current and voltage sensing feedback path might or might not need to be isolated.

Isolated High-Performance Current and Voltage Sensing in Server PSUs

Shunt-based current measurements are the preferred option to achieve the high accuracy levels and bandwidth in the current feedback loop. Shunt-based solutions offer higher accuracy, lower temperature drift, and higher bandwidth than open-loop Hall-based current sensors. Closed-loop Hall sensor modules could be an alternative, but they are very expensive compared to shunt-based solutions to reach the required performance.

Shunt resistors paired with reinforced isolated amplifiers such as the **AMC3301** (±250-mV input range) or **AMC3302** (±50-mV input range), that can operate using a single supply and offer bandwidth up to 300 kHz, provide a simple, easy-to-implement, solution for accurate shunt-based isolated current sensing. These products include a fully-integrated DC-DC converter that eliminates the need for supply on the current measurement side. For voltage measurements, a resistor divider network followed by reinforced isolated amplifiers such as **AMC3330** (±1-V input range) allows very accurate isolated voltage sensing. **Figure 135** and **Figure 136** show the block diagrams of AMC3301 and AMC3330 respectively.

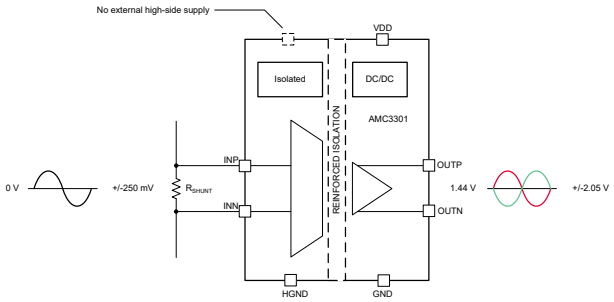


Figure 135. *AMC3301 Block Diagram*

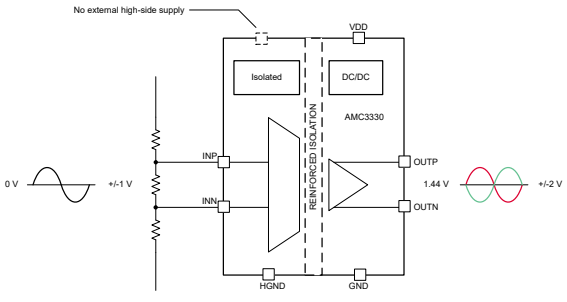


Figure 136. *AMC3330 Block Diagram*

Conclusion

As the trend of server PSU manufacturers striving to achieve Titanium standard certifications increases, the **AMC33xx** family of products, provide a high-performance, cost-optimized, easy-to-implement solution for isolated current and voltage sensing.

Resources

- Texas Instruments, ***Isolated amplifiers and modulators*** TI training and videos
- Texas Instruments, ***Comparing Isolated Amplifiers and Isolated Modulators*** white paper
- Texas Instruments, ***Comparing shunt- and Hall-based current-sensing solutions in onboard chargers and DC/DC converters*** white paper
- Texas Instruments, ***Accuracy Comparison of Isolated Shunt and Closed-Loop Current Sensing*** application brief

Additional Reference Designs/Circuits

- Designing a Bootstrap Charge-Pump Power Supply for an Isolated Amplifier
- Clock Edge Delay Compensation With Isolated Modulators Digital Interface to MCUs
- Utilizing AMC3311 to Power AMC23C11 for Isolated Sensing and Fault Detection

Designing a Bootstrap Charge-Pump Power Supply for an Isolated Amplifier

Abstract

Isolated amplifiers provide isolation between their input signal and output signal, which is useful in many applications, such as phase current sensing in motor drives. Providing the high-side power to an isolated amplifier can be challenging. This application note introduces a bootstrap charge-pump circuit as a small, low-cost alternative for generating the high-side power supply and goes into detail regarding the design of such a circuit.

Introduction

Isolated amplifiers can measure voltage or current with relatively high accuracy while keeping the measurements isolated from the low-side. This is useful in applications where the high-side voltage requires isolation for safety-related concerns, or when the high-side can experience sudden transients which can damage a controller on the low-side. Common applications include measuring a high-voltage motor bus or measuring motor phase current.

However, isolated amplifiers require the high-side power supply to be isolated from the low-side power supply, which can lead to increased size and complexity. One alternative is a transformer-isolated power supply, which produces the high-side rail from the low-side while keeping the high-side isolated from the low-side. However, transformers can be large and costly. A bootstrap charge-pump power supply is a cost-effective alternative. The power is supplied from a pulse-width modulation (PWM) signal, and only requires a capacitor, a diode, and a current-limiting resistor. In some cases, a linear dropout regulator (LDO) can be required as well.

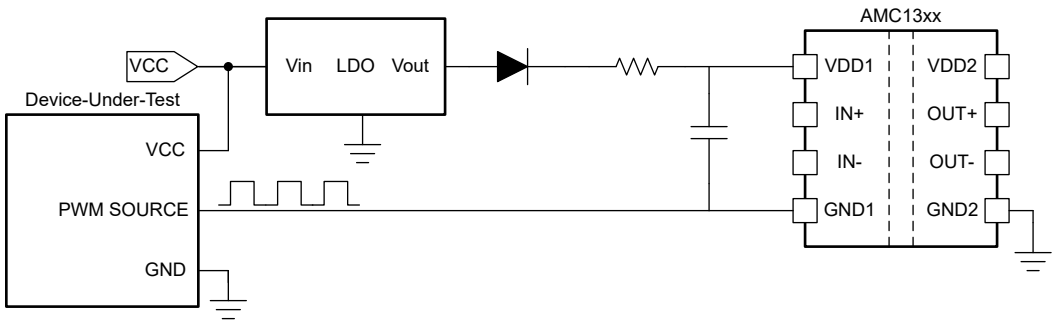


Figure 137. *Bootstrap Power Supply*

Bootstrap Power Supply Design

The bootstrap operates from an input voltage and a PWM signal. The input voltage is supplied from the same supply powering the device-under-test (DUT), and the input voltage can be stepped down using an LDO. Since the bootstrap requires a PWM signal to operate, the signal can only be used with DUTs which produce or operate with a PWM signal. The DUT is not necessarily isolated from the low-side of the amplifier, as shown in **Figure 137**, which is why a DC-DC power converter alone cannot be used. The high-side of the amplifier does not share a ground connection with the DUT. The PWM signal is tied to the isolated amplifier's high-side ground. The bootstrap make sure the high-side power supply always floats above the PWM signal, so the high-side power supply has a steady signal, even though the high-side ground is a PWM signal.

The input voltage to the bootstrap circuit determines the output steady state value, so the input voltage must be close to the desired high-side supply voltage to avoid violating the amplifier’s high-side supply specifications. An LDO is required if the DUT VCC bus is outside of the isolated amplifier's recommended operating conditions. LDOs generally require few

additional external components, and LDOs produce cleaner signals than switching regulators, which is why LDOs are recommended in this application. The input voltage to the bootstrap circuit is greater than the DUT ground, so when the PWM signal is low, there is a positive voltage drop across the diode, and it conducts, charging the capacitor, as shown in **Figure 138**.

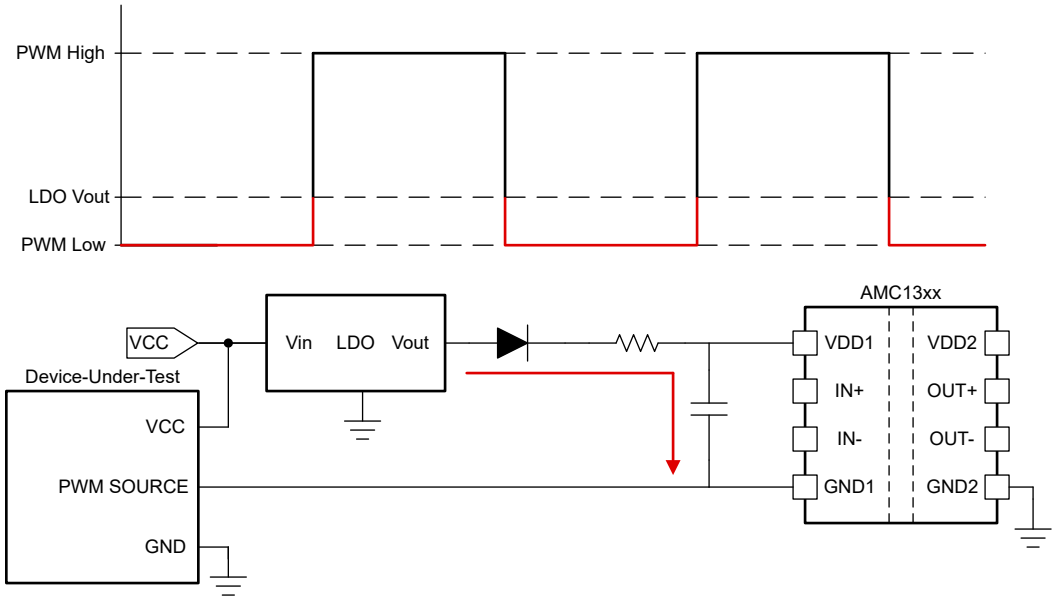


Figure 138. *Charging the Bootstrap Capacitor*

When the PWM signal is high, there is no voltage drop or a negative voltage drop across the capacitor, and the signal stops conducting, so the capacitor discharges into the high-side supply, as shown in **Figure 139**. The bootstrap circuit can achieve steady state when the amount of voltage stored by the capacitor when the PWM signal is low is equal to the amount of voltage discharged by the capacitor when the PWM signal is high. This means that the start-up time and steady state ripple are dependent on the RC time constant and can be impacted by the frequency and duty cycle of the PWM signal.

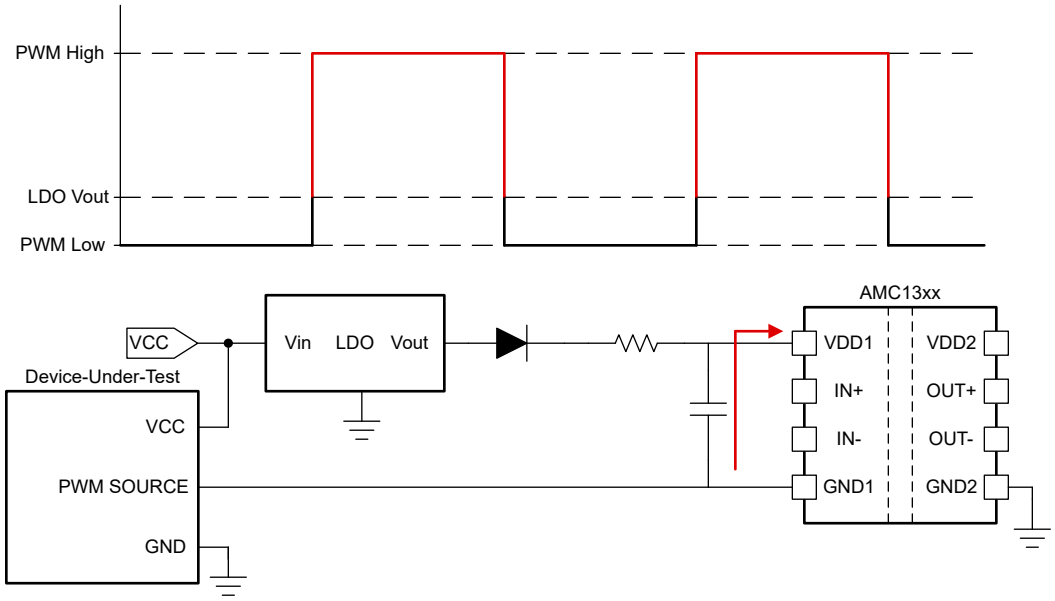


Figure 139. *Discharging the Bootstrap Capacitor*

Selection of Charge Pump Capacitor

The maximum value supplied by the bootstrap can be approximated by taking the input supply to the bootstrap and subtracting the voltage drop of the diode. However, the bootstrap can reach steady state before the bootstrap reaches the maximum value, depending on the value of the RC circuit and the PWM signal. The RC time constant is defined as:

$$\tau = R \times C \tag{59}$$

The capacitor and resistor determine the RC time constant for charging and discharging the capacitor. There is a trade-off between start-up time and steady-state ripple. A smaller time constant means that the capacitor can charge and discharge more quickly, reaching steady-state sooner. However, once the capacitor reaches steady-state, the capacitor can charge or discharge more voltage per PWM duty cycle than the capacitor can with a larger time constant, which leads to larger ripple. Likewise, a larger time constant can result in less ripple due to longer charge or discharge times. The capacitor value can be estimated using the following parameters:

1. PWM switching frequency
2. PWM duty cycle
3. Current required to power the isolated amplifier
4. Allowable ripple

We can rearrange **Equation 60** as shown in **Equation 61** to solve for capacitance.

$$Q = I \times t = \Delta V_{ripple} \times C \tag{60}$$

$$C = \frac{I \times t}{\Delta V_{ripple}} \tag{61}$$

Assuming a 20 kHz switching frequency with a 50% duty cycle, using the maximum current draw from the AMC1311-Q1 data sheet, and mandating a 100 mV maximum ripple requirement, the following minimum capacitance value is received:

$$C = \frac{9.7\text{mA} \times 0.5 \times \frac{1}{20\text{kHz}}}{100\text{mV}} = 2.4\mu\text{F} \tag{62}$$

From there, the bootstrap can be simulated to estimate start-up time, and an appropriate capacitor and resistor can be selected based on the start-up time requirements. The resistor needs to be selected so the resistor does not prevent the high-side of the amplifier from drawing sufficient current.

Simulation in TINA-TI

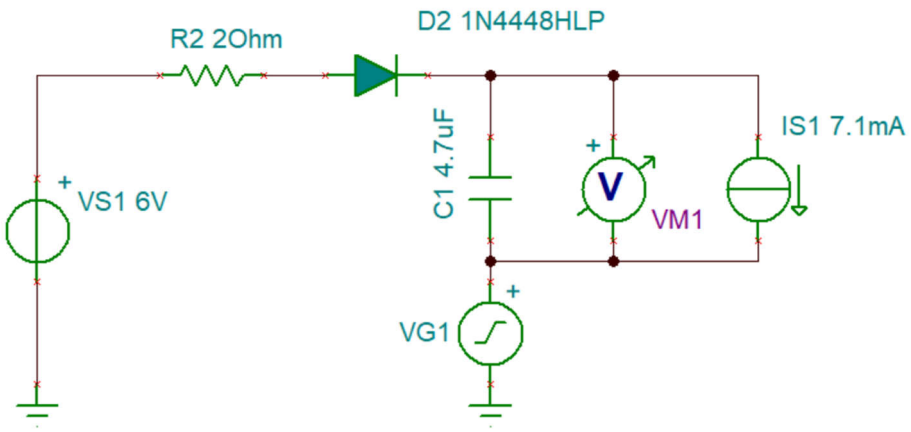


Figure 140. *Simulation Model*

VS1 is the output from the LDO, VG1 is used to simulate the PWM signal, and IS1 simulates the load draw from the isolated amplifier. Since VS1 is 6 V and the voltage drop across the diode is 300 mV, the maximum output of the bootstrap is 5.4 V. VG1 is sourcing a 20 kHz, 50 V_{pp} PWM signal with a duty cycle of 50%. C1 is stepped through four different capacitor values.

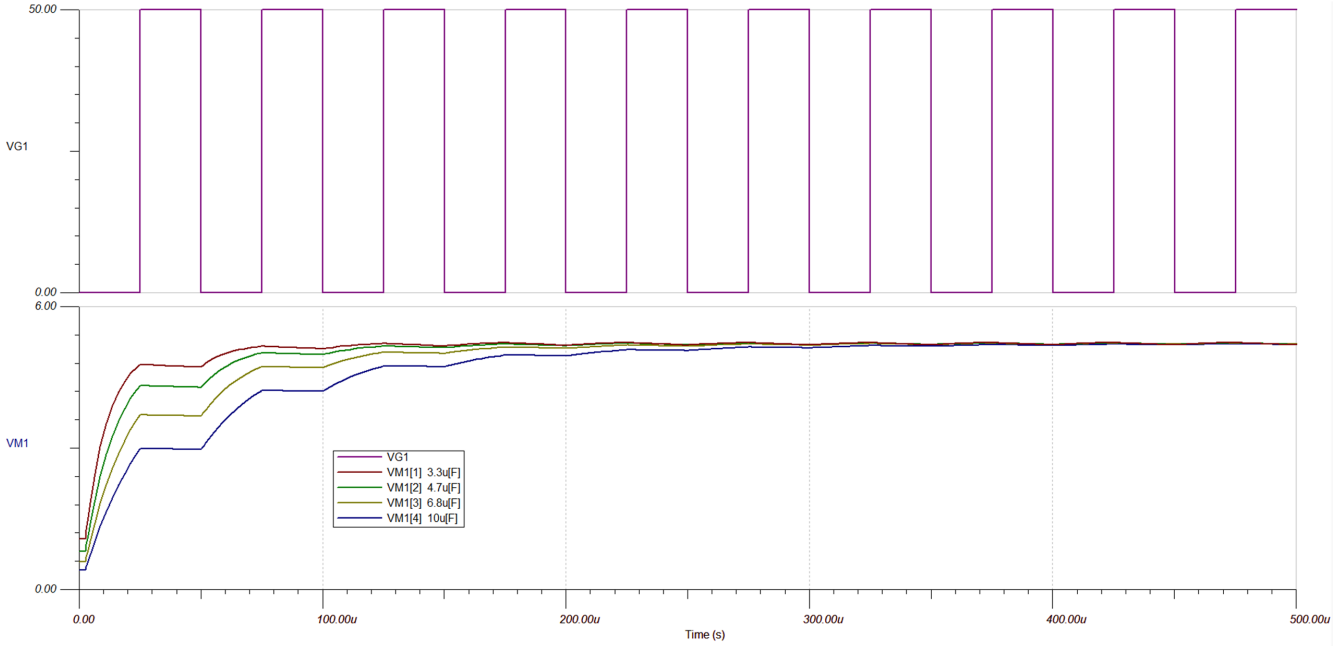


Figure 141. *Comparing Capacitor Values*

Table 22. Steady State Output Voltage with Different Capacitors

Capacitor Value (µF)	Steady State Ripple (mV)	Average Steady State Value (V)
3.3	53.6	5.215
4.7	37.7	5.200
6.8	25.8	5.215
10	17.7	5.215

Figure 141 shows four different capacitor values with the same PWM signal. **Table 22** shows the steady state output voltage with the different capacitors. Notice that none of the capacitors reach the theoretical maximum steady state value of 5.4 V. However, as the ripple decreases, the start-up time clearly increases. The signal with 4.7 µF has a good balance between start-up time and ripple.

The start-up time and the steady state ripple of the bootstrap circuit also depends on the frequency and duty cycle of the input PWM signal. We can observe this in simulation by setting C1 to a single value and changing the PWM signal generated by VG1.

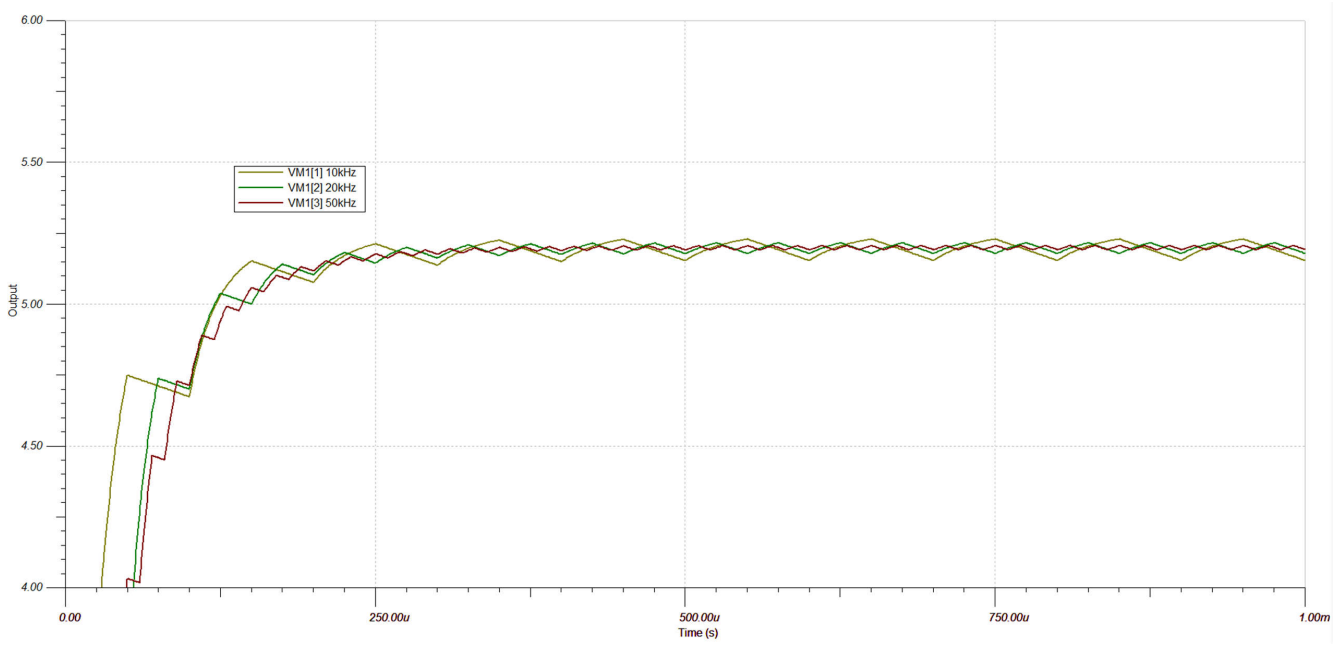


Figure 142. *Change PWM Frequency*

Table 23. Start-Up Time and Steady State Voltage for Different Frequencies

PWM Frequency (kHz)	Steady State Ripple (mV)	Average Steady State Value (V)
10	75.1	5.190
20	37.7	5.200
50	14.7	5.200

C1 is 4.7 µF, and the PWM signal has an amplitude of 50 V_{pp} and a 50% duty cycle. The frequency has a much bigger impact on the output ripple without affecting the start-up time and average steady state too dramatically, as shown in **Table 23**.

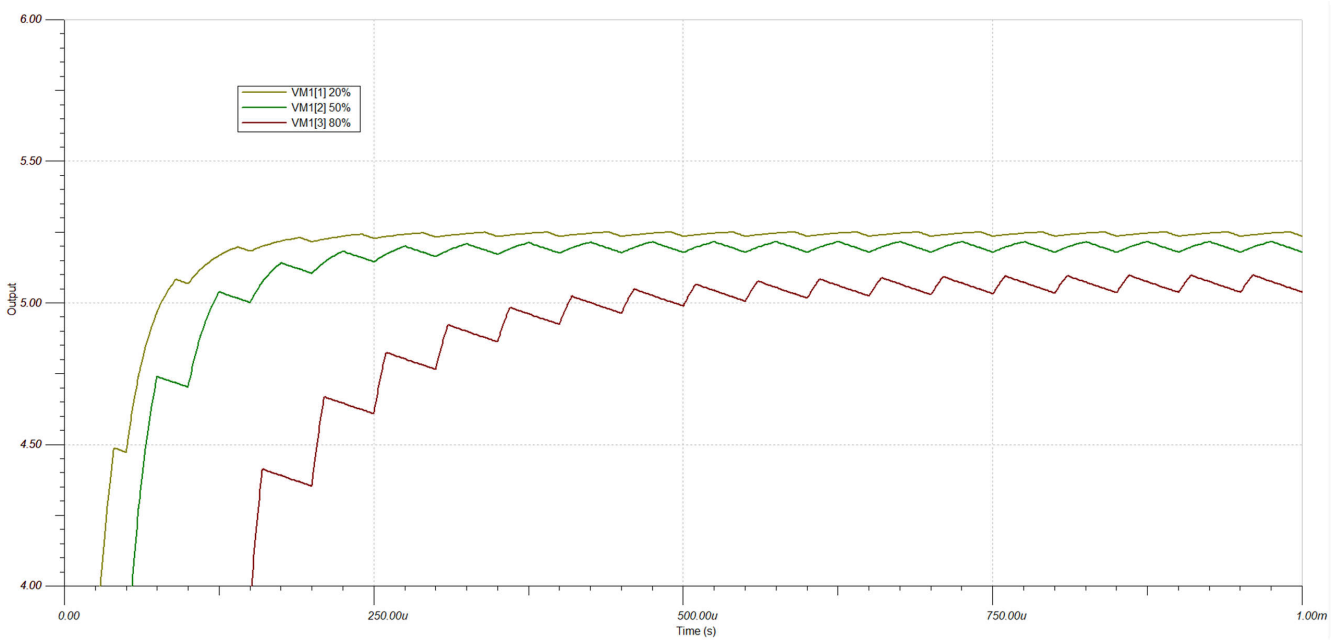


Figure 143. *Change PWM Duty Cycle*

Table 24. Start-Up Time and Steady State Voltage for Different Duty Cycles

PWM Duty Cycle	Steady State Ripple (mV)	Average Steady State Value (V)
20%	14.7	5.245
50%	37.7	5.200
80%	59.9	5.070

C1 is 4.7 µF and the PWM signal has an amplitude of 50 V_{pp} and a 20 kHz frequency. The start-up time and average output are impacted much more, as shown in **Figure 143** and **Table 24**.

Too much ripple can impact the performance of the isolated amplifier as the bouncing power supply can cause common-mode errors on the output. However, the isolated amplifier cannot be verified to measure the DUT accurately until the amplifier has reached the minimum recommended value for the amplifier's high-side power supply. Knowing the expected PWM output signal is crucial to designing an effective bootstrap circuit within the system's parameters. However, the 4.7 µF capacitor was selected under the assumption that the PWM signal can have a duty cycle of 50% and have a 20 kHz frequency (see **Section 8.1.2.1**), so the minimum capacitance can be adjusted based on the PWM signal characteristics (see **Equation 62**).

Hardware Test with AMC1311-Q1

The actual circuit is built as **Figure 137** to verify the simulations. C=4.7 µF, R=2 Ω, the output of the LDO is 6 V, and the input PWM signal is 50 V_{pp} at 20 kHz with a 50% duty cycle. **AMC1311-Q1** is the selected isolated amplifier and **TPS7A4101** is the selected LDO for the wide input range.

The start-up time is around 260 µs, and the steady-state output is 5.1 V with 29.7 mV ripple, matching reasonably well with the **Figure 140**. The discrepancy between simulation and hardware is due to equipment current limitations, which are not accounted for in an designed for simulation.

The ripple from the bootstrap power supply had minimal impact on the performance of AMC1311-Q1 when compared to the performance with a clean power supply. The clean signal was generated using a transformer and an LDO from the low-side power rail. This transformer power supply is approximately twice the size of the bootstrap power supply and much more expensive than the bootstrap, due to the cost of the transformer. If the ripple was too high, the bootstrap power supply can also be smoothed with simple RC filters. This can add minimal size and cost to the circuit.

Summary

A charge-pump bootstrap circuit is an effective way to produce an isolated power rail for an isolated amplifier in PWM applications. A well-designed boostrap power supply can operate just as effectively as a clean power supply, while saving space and cost.

There are several key factors to consider when designing a bootstrap circuit. It is important to know the current draw of the isolated amplifier, the frequency and duty cycle of the PWM signal, the allowable range for circuit start-up time, and the allowable power supply ripple for the isolated amplifier. All of these specifications can affect the selection of the RC circuit used in the bootstrap circuit. A bootstrap can be simulated easily, making the selection process much simpler since the designer can easily test various RC values under different circuit conditions.

Reference

1. Texas Instruments, ***AMC13xx Parametric Table***.
2. Texas Instruments, ***DC+ Bus Power-Supply Solution Using Bootstrap Charge Pump Technique*** application note.
3. Texas Instruments, ***Using Isolated Comparators for Fault Detection in Electric Motor Drives*** analog design journal.
4. Texas Instruments, ***Design Considerations for Isolated Current Sensing*** analog design journal.

Clock Edge Delay Compensation With Isolated Modulators Digital Interface to MCUs

Abstract

Isolated Delta-Sigma modulators such as **AMC1306M25** with high-speed digital interface are commonly used for accurate, low latency and high noise immunity shunt-based phase current sensing in **servo drives** and **robotics** applications. Especially at higher clock frequencies, proper routing, termination, and compliance with the corresponding MCU's setup and hold timings are critical for a reliable operation. A commonly used method and compromise to meet the MCU timing requirements is to reduce the modulator clock frequency, which also reduces the data output rate. This application note shows more designed for clock edge compensation methods to meet the setup and hold timing requirements up to the maximum clock rate of the modulator. This enables the system to operate at maximum data rate. The application note outlines options for clock edge compensation and shows example measurements with TI's isolated modulators AMC130x connected to C2000™ and Sitara™ MCUs. In addition, a calculation tool is provided to validate the digital interface timing.

Introduction

Isolated Delta-Sigma Modulators are commonly used for shunt-based phase current sensing in **servo drives** and **robotics** applications as accurate and low latency isolated phase current sensing has a significant impact on the performance of three-phase inverters. Delta-Sigma modulators provide a digital bit stream with either LVDS or CMOS interface to an MCU that allows for exceptional noise immunity, high precision, and low latency phase current measurement. For additional information on isolated modulators, please see ***Comparing Isolated Amplifiers and Isolated Modulators***, application note.

Often the shunts and the isolated Delta-Sigma modulators are placed on the power stage printed circuit board (PCB), while the MCU is placed on a separate control board PCB, as shown in figure 1. Proper routing schemes on the PCBs and the interface connector are crucial for digital signal integrity. Best practices for clock and data line routing and termination are discussed in ***Better Signal Integrity w/ Isolated Delta-Sig. Modulators in Motor Drives (ti.com)***, application report.

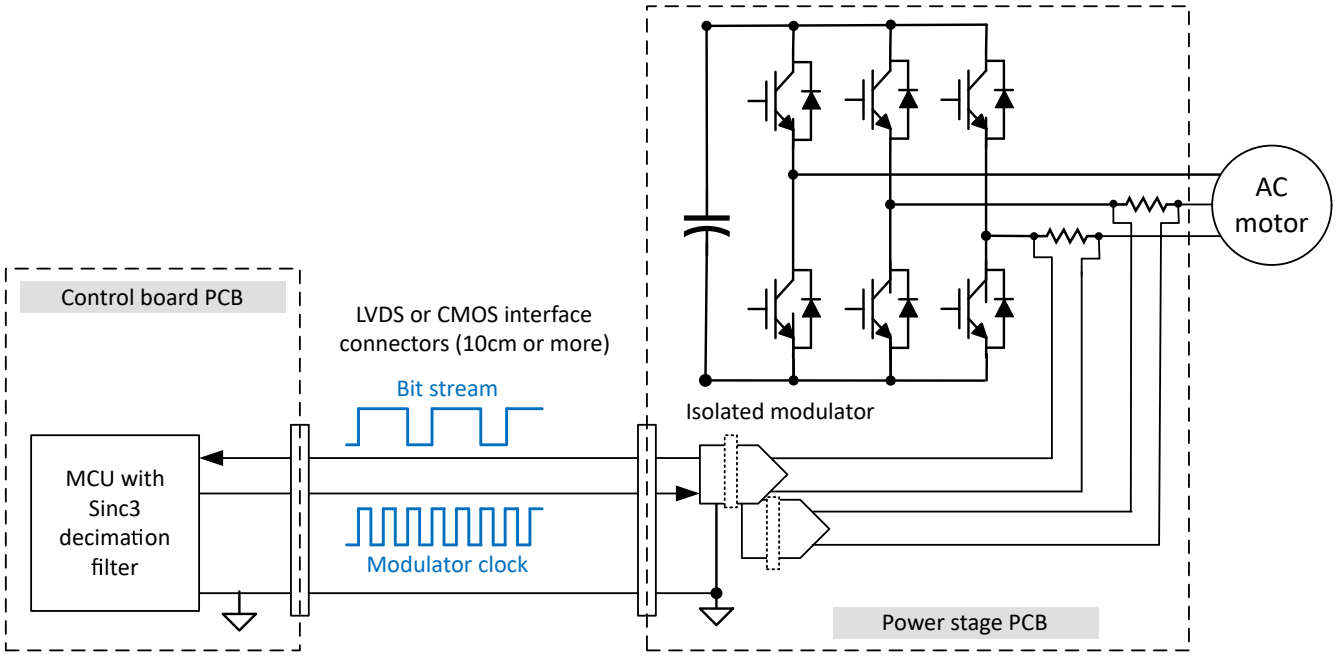


Figure 144. *Simplified 3-Phase Inverter Block Diagram With Digital Interface From MCU to Isolator Modulators*

There can be further design challenges to meet the timing between the modulator clock edge and the digital bitstream, especially when the signal traces are quite long, additional buffers and level translators are used. Then an additional propagation delay of the modulator clock and bitstream signal can even force designers to reduce the modulator clock from the maximum 21 MHz (AMC1306) to e.g. 15 MHz to meet the timing between clock edge and bitstream data at the MCU. Due to that the overall phase current measurement latency increases reverse proportional to the selected modulator clock. For example, a typically used Sinc3 decimation filter with an oversampling ratio of 64 has a measurement latency (propagation delay) of 4.8us at 20 MHz modulator clock, while the latency increases to 6.4us when only a 15 MHz modulator clock can be used.

The following sections of this document provide an overview of digital timing compensation methods to overcome this design challenge and show that designing with an isolated modulator offers not only the highest precision measurement but also the easiest.

Design Challenge With Digital Interface Timing Specifications

Isolated Delta-Sigma modulators offer interface options for both an externally and internally generated clock signal with either a CMOS interface or a LVDS interface. For devices with externally-provided clock source, for example **AMC1306M25** with CMOS interface or **AMC1305L25** with LVDS interface the clock signal is routed from the MCU to the Delta-Sigma modulator's clock input, whereas for devices with an internally-provided clock source, the output bit-stream is synchronized to the internally generated clock, for example**AMC1303M2520**. There are also isolated Delta-Sigma modulator devices with Manchester coded output bit stream that support single-wire data and clock transfer, for example **AMC1306E25**. For all isolated Delta-Sigma modulators, the data output of the modulator provides a bit stream of digital ones and zeros that is shifted out synchronous to the clock edge.

Figure 145 shows a simplified example of CMOS interface with 3.3V I/O between the isolated Delta-Sigma modulator AMC1306M25 and a C2000 MCU **TMS320F28379D**. As the AMC1306M25 requires an externally-provided clock source, the clock signal is generated by the MCU TMS320F28379D and is provided to the Delta-Sigma modulators clock input, CLKIN. In parallel, the generated clock signal is also routed to the clock input to the MCUs Sigma-Delta Filter Module (SDFM) SD1_C1 (GPIO123). Depending on the system design there can be a clock buffer included in the clock interface between the MCU and the isolated Delta-Sigma modulator. The isolated data output DOUT of the Delta-Sigma modulator is directly connected to the MCUs Sigma-Delta Filter Module (SDFM) data input SD1_D1 (GPIO122).

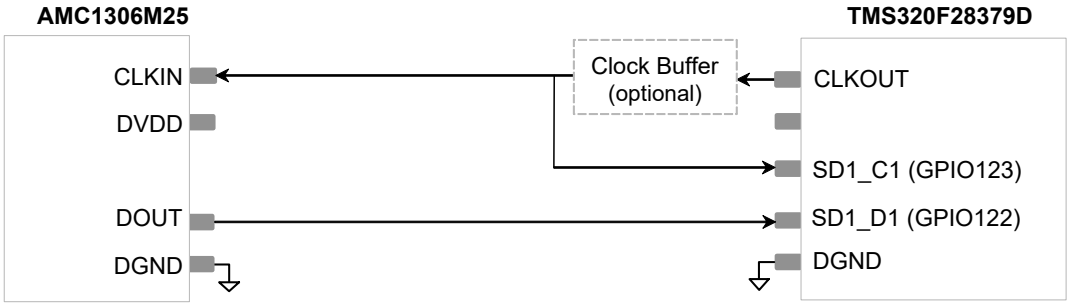


Figure 145. *Simplified AMC1306M25 Digital Interface to TMS320F28379D*

Valid communication between the isolated Delta-Sigma modulator and the MCU is described in the respective device data sheets by the setup and hold timing requirements. The setup time is the amount of time that the data signal must be valid and stable prior to a clock signal transition to capture the data signal in the MCU. Hold time is the amount of

time that a signal must be held valid and stable after a clock signal transition occurs. Meeting the MCUs setup and hold time requirements is crucial as any violation can cause incorrect data to be captured. Incompatibility between the digital interface setup and hold timing requirements of the isolated Delta-Sigma modulator and the MCU can present a design challenge.

Figure 146 outlines the digital interface timing for setup and hold time of the AMC1306x which supports a recommended clock frequency (CLKIN) from 5 MHz to 21 MHz with a data hold time t_h(MIN) = 3.5 ns and a data delay time t_d (MAX) = 15 ns.

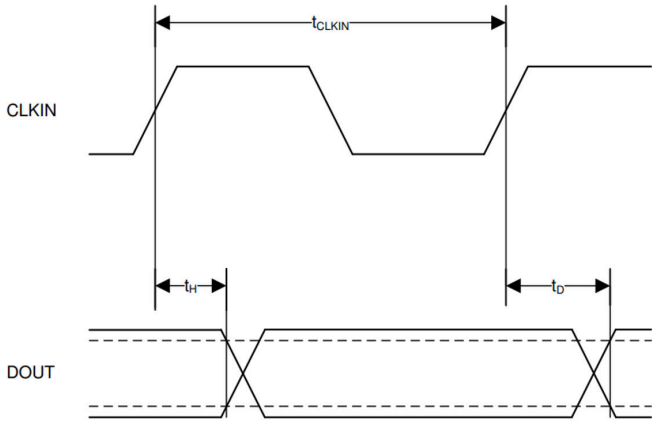


Figure 146. *AMC1306x Digital Interface Timing*

Figure 147 outlines the timing diagram, of the TMS320F28379D Sigma-Delta Filter Module (SDFM) for Mode 0. The data input at SDx_Dy needs to meet the minimum setup time $t_{su(SDDV-SDCH)M0}$ and minimum hold time $t_{h(SDCH-SDD)M0}$ with reference to the rising clock edge of the SDx_Cy signal in the SDFM module.

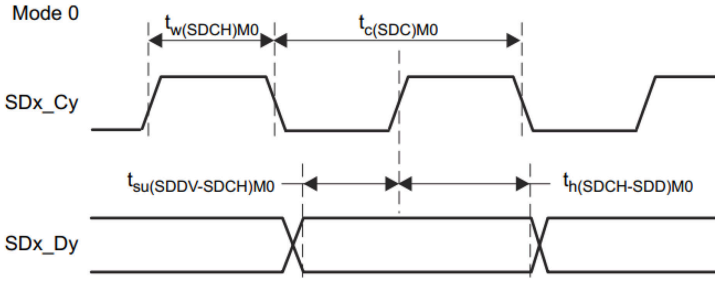


Figure 147. *TMS320F28379D SDFM Timing Diagram – Mode 0*

For the TMS320F28379D SDFM module in Mode 0, we recommend to use the SDFM operation with qualified GPIO (3-sample window). This mode provides protection against random noise glitches with the input clock signal (SDx_Cy) and data input (SDx_Dy) to avoid false comparator over-current trip and false Sinc filter output. The minimum setup and hold times for a 200 MHz system clock with TMD320F28379D are both 10 ns: $t_{su\ (SDDV-SDCH)M0}$ (MIN) = 10 ns and $t_{h(SDCH-SDD)M0}$ (MIN) = 10 ns.

This creates a design challenge as the AMC1306M25 minimum hold time t_h(MIN) is 3.5 ns, but 10 ns is required for the SDFM module to maintain correct acquisition at the data input SDx_Dy with reference to the rising clock edge of the SDx_Cy signal.

An additional challenge is that the propagation delay of additional components in the signal chain with the digital interface such as a clock buffer as well as the propagation delay of the clock and data signals introduced by the trace length on the PCB have an impact on the timings between SDx_Cy and SDx_Dy inputs and complicate the correct acquisition timing of the data input.

The same applies to Delta-Sigma modulators with a LVDS interface, such as the **AMC1305L25**. The only difference to AMC1306M25 Delta-Sigma modulators with CMOS interface type is that additional components like a **LVDS driver and receiver** are required with the digital signal chain to a MCU with CMOS interface, which contribute to further propagation delays. **Figure 148** shows a simplified digital interface between the isolated Delta-Sigma modulator AMC1305L25 with LVDS interface and the MCU TMS320F28379D with CMOS interface.

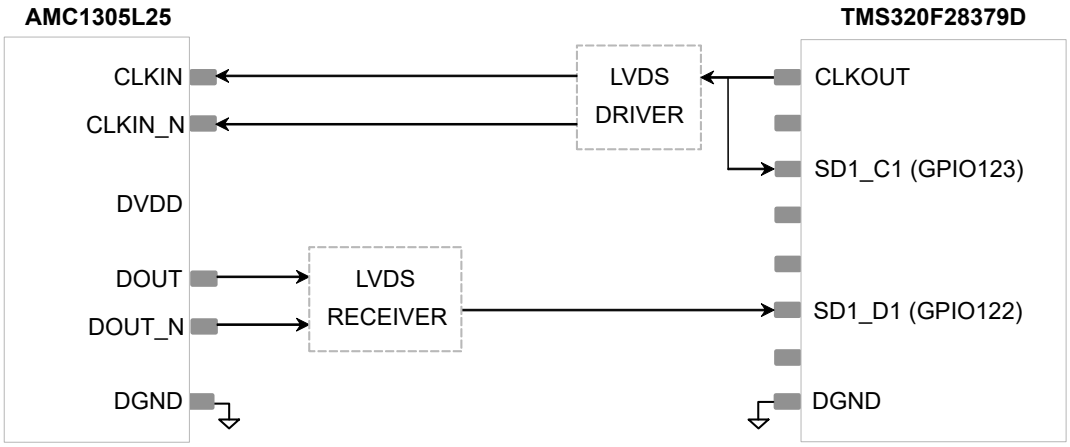


Figure 148. *AMC1305L25 Digital Interface to TMS320F28379D*

Figure 149 shows a simplified digital interface of an isolated Delta-Sigma modulator with internally-created clock source AMC1303Mx with CMOS interface to TMS320F28379D with CMOS interface. The internally generated clock signal CLKOUT of the AMC1303Mx is input to the MCUs Sigma-Delta Filter Module (SDFM) SD1_C1 (GPIO123). The isolated data output DOUT of the Delta-Sigma Modulator is directly connected to MCUs data input SD1_D1 (GPIO122) of the SDFM.

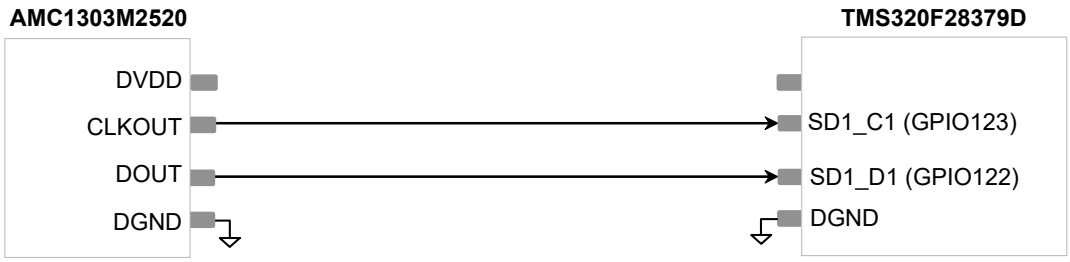


Figure 149. *AMC1303M2520 3.3-V CMOS Digital Interface to TMS320F28379D*

When using an isolated modulator with an internal clock, the digital interface challenge is limited to the different timing specifications of the isolated Delta-Sigma modulator and the MCUs setup and hold times. The propagation delay of clock and data signals introduced by the trace length on the PCB can be neglected if the clock and data signals are routed at the same length. Typically, the modulator is directly interfaced to the MCU and there's no need for a buffer or level-shifter, which adds additional propagation delay.

The AMC1303Mx hold time t_h(MIN) is 7 ns and the delay time t_d (MAX) is 15 ns for the 10 MHz and 20 MHz clock versions. The challenge is that the AMC1303Mx minimum hold t_h(MIN) is 7 ns, but 10 ns is required by the SDFM module for correct acquisition of the data input at SDx_Dy without any setup and hold time violations.

For isolated Delta-Sigma modulators with a Manchester encoded bitstream output, e.g. AMC1306E25, data and clock are transferred through a single-wire. So that the setup and hold time requirements of the receiving device versus the modulator clock do not have to be considered.

A commonly used method and compromise to meet the MCUs setup and hold time requirements is to reduce the clock frequency. However, reducing the clock frequency is also reducing the data output rate of the isolated Delta-Sigma modulator and increases the latency of the current measurement. A more suitable method is to use clock edge delay compensation which enables moving the clock edge of the clock signal to an ideal sample point of the data signal to meet the setup and hold timing requirements. By using this method, the clock frequency limitations are eliminated which allows the isolated Delta-Sigma modulator and the system to operate at full performance.

Design Approach With Clock Edge Delay Compensation

To meet and further optimize the MCUs setup and hold timing requirements for reliable data acquisition, clock edge delay compensation is recommended. Clock edge delay compensation can be implemented by various methods, summarized below and expanded upon in the following section:

1. Additional clock signal with software configurable phase delay
2. Clock signal with hardware configurable phase delay
3. Clock return
4. Clock inversion at MCU

Clock Signal Compensation With Software Configurable Phase Delay

Figure 150 shows the first compensation method, where an additional phase locked clock signal with a software configurable phase delay is used. For this compensation method the phase-shifted clock signal CLKOUT_delay is used as the clock input to SD0_CLK of the Sigma-Delta Filter Module (SDFM). For other types of Delta-Sigma Modulators and MCUs e.g. C2000 MCUs, the compensation method follows the same principle.

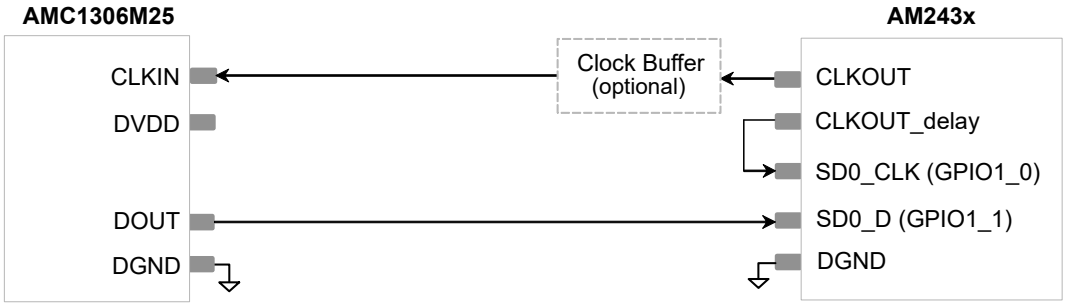


Figure 150. *AMC1306M25 to AM243x MCU Interface With Software Configurable Clock Phase Delay*

The implementation of a second phase-shifted clock signal offers the highest degree of freedom and user configurability. This means that various values for minimum hold time t_h(MIN) of various isolated modulators can be compensated by a simple change to the phase-shift value in software. The clock signals rising edge at the SD0_CLK input is phase-shifted such that the clocking signal complies with the data sampling point of the SDFM, as shown in **Figure 151**. The **AM243x**

PRU_ICSSG PRU Timing Requirements in Sigma Delta Mode are 10 ns for minimum setup time $t_{su\ (SD\_D\text{-}SD\_CLK)}$ (MIN) = 10 ns and 5 ns for minimum hold time $t_{h(SD\_CLK\text{-}SD\_D)}$ (MIN) = 5 ns. This creates a need for compensation to maintain correct acquisition at the data input SDx_D with reference to the rising clock edge of the SDx_CLK signal as the AMC1306M25 minimum hold time t_h(MIN) is 3.5 ns, but 5 ns can be required. After this compensation method is applied, the 10-ns minimum setup and 5-ns hold timings for the Sigma Delta Mode of the AM243x PRU_ICSSG PRU timing requirements are met, see **Figure 151**.

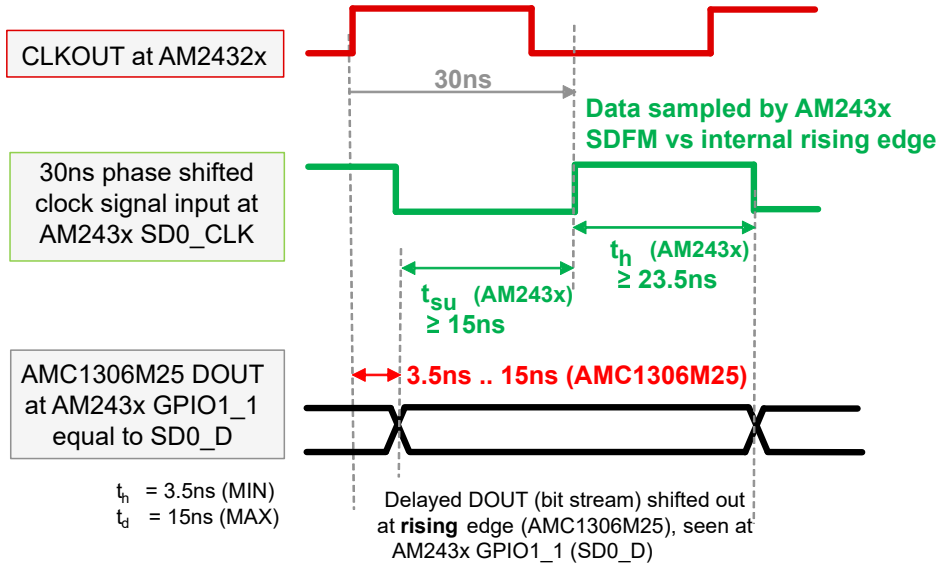


Figure 151. *AM243x SDFM Timing With 30-ns Phase-Shifted Clock Signal Input at SD0_CLK (GPIO1_1)*

Clock Signal Compensation With Hardware Configurable Phase Delay

Clock signal compensation with hardware configurable phase delay of the digital interface between AMC1306M25 and MCU is shown in **Figure 152**. With this compensation method a phase-shifted clock signal by a phase delay in hardware is connected to the clock input SDFM_CLKIN of the SDFM module of the MCU. This type of compensation works for any MCU with Sigma-Delta Filter Module, but is only recommended for isolated Delta-Sigma Modulator's with an external clock source and CMOS interface.

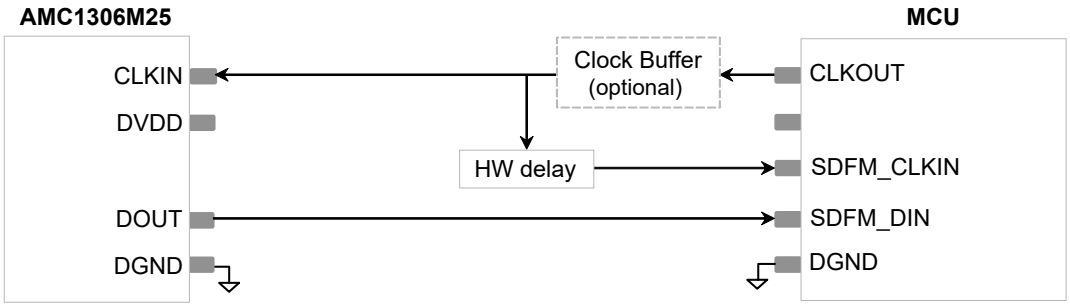


Figure 152. *AMC1306M25 Digital Interface to MCU With Compensation by Hardware Configurable Phase Delay*

To implement a phase delay in hardware, a logic gate or buffer can be used to introduce a propagation delay in the clock signal. However, when implementing a delay in hardware the value of the delay is strongly dependent on the propagation delay of the hardware block limiting the degree of freedom and user configurability. The working principle

of the compensation by clock signal with hardware configurable phase delay follows the same principle described in **Section 8.2.3.1**.

Clock Signal Compensation by Clock Return

Clock Signal Compensation by Clock Return is shown in Figure 3-4. With this compensation method, the clock signal that is fed into CLKIN the clock input of the AMC1306M25, is routed back from the CLKIN Pin of the AMC1306M25 to the SDFM clock input SDFM_CLKIN of the MCU.

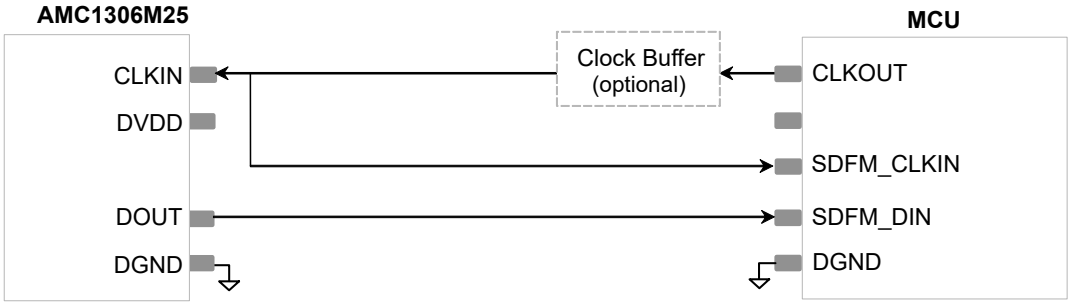


Figure 153. *AMC1306M25 Digital Interface to MCU With Compensation by Clock Return*

By using this method, the same propagation delay by the clock buffer and the propagation delay introduced by the PCB trace length is achieved for the clock and data signal. Therefore, these delays in the clock and data signals cancel each other out.

However, the AMC1306M25 digital interface timing for data hold time t_h(MIN) = 3.5 ns and data delay time t_d (MAX) = 15 ns remains. This means that the timing needs to be checked after the PCB has been built to verify that the setup and hold timing requirements of the MCU for the SDFM are met. This type of compensation method is only recommended for isolated Delta-Sigma modulator with external clock source and CMOS interface.

Clock Signal Compensation by Clock Inversion at the MCU

The last method for clock signal compensation is clock inversion at the MCU and works for Delta-Sigma modulators with external and internal clock source. In that case, the selected MCU must be capable of inverting the GPIO input. The TMS320F28379D GPIO inputs prior to the SDFM (Sigma Delta Filter Module) can be configured to invert the input signal at any GPIO, as shown in **Figure 154**. For example, the clock input signal is inverted at GPIO123, hence the SD1_C1 clock signal is inverted versus the AMC1303Mx clock signal. As a result, the SDFM samples the input data SD1_D1 versus the falling edge of the external clock signal at the input of GPIO123, as shown in **Figure 155**.

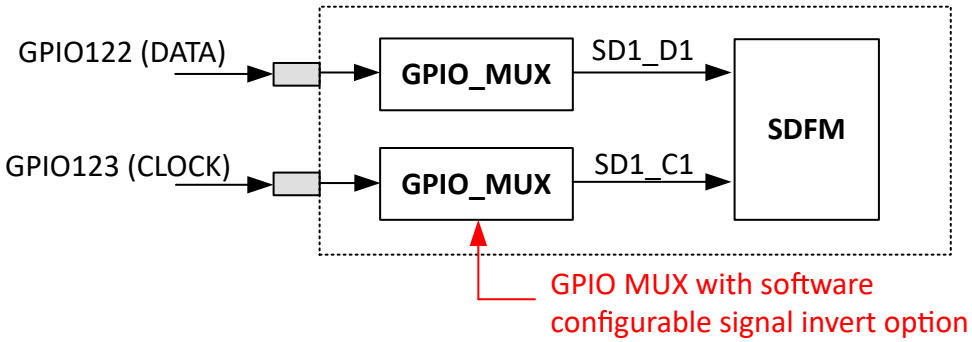


Figure 154. *TMS320F28379D SDFM/GPIO Block Diagram*

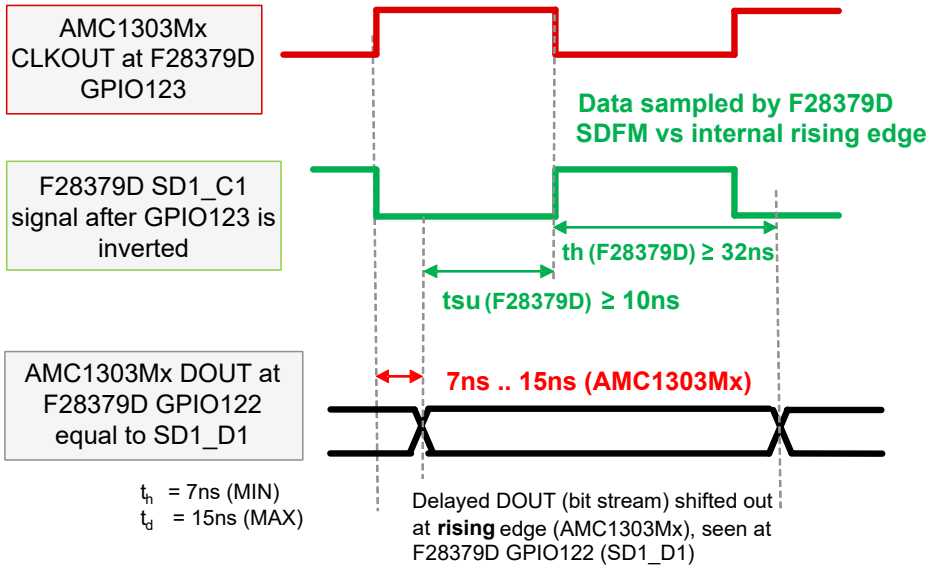


Figure 155. *TMS320F28379D SDFM Timing With Inverted Clock at GPIO123*

By inverting the clock input signal by using the GPIO a fixed delay of one-half of the clock period is added to the clock signal. Depending on the timing specifications and propagation delays of the system setup, this additional delay may be sufficient to meet the TMS320F28379D setup and hold timings of minimum 10 ns for the SDFM qualified GPIO (3-sample) mode 0. However, as this clock signal compensation method's additional delay time is fixed and cannot be changed, it must be verified for each system design that the resulting timings for setup and hold of the MCU for the SDFM qualified GPIO (3-sample) mode 0 are met.

This compensation method is also applicable to Sitara MCUs, where both the rising and falling edges of the external clock signal can be set as data acquisition point by software.

Test and Validation

The following sections present clock edge compensation test results using an additional clock signal with phase delay in software as described in **Section 8.2.3.1** as well as clock inversion as described in **Section 8.2.3.4**. First, the test equipment and software are described, followed by the test setup, measurements and test results of the clock signal compensation methods.

Test Equipment and Software

The key test equipment for the measurements are listed in **Table 25**.

Table 25. List of Test Equipment

Description	Part Number
AMC1306 reinforced isolated modulator evaluation module	**AMC1306EVM**
F28379D LaunchPad™ development kit for C2000™ Delfino™ MCU	**LAUNCHXL-F28379D**
AM243x general purpose LaunchPad™ development kit for Arm®-based MCU	**LP-AM243**
High-speed oscilloscope	Tektronix MSO 4104
Single-ended probes	Tektronix P6139A

Software development and debugging is done with **Code Composer Studio™(CCS) version 12.4.0**. CCS is an integrated development environment (IDE) that supports Texas Instruments microcontroller (MCU) and embedded

processor portfolios. An internal TI test software was used for the TMS320F28379D based on the **C2000WARE — C2000Ware for C2000 Microcontrollers**. For the Sitara AM243x Launchpad an internal TI test software was used based on the AM243x software development kit (SDK) for Sitara™ microcontrollers **MCU-Plus-SDK-AM243X Version 09.00.00.35**. For specific implementation and software support of C2000 and Sitara refer to **TI E2E support forums**.

Testing of Clock Signal Compensation With Software Configurable Phase Delay

This measurement validates that the setup and hold timing requirements are met with clock signal compensation by using an additional clock signal with a software configurable phase delay. This test was performed and validated with both the C2000 TMS320F28379D Launchpad and Sitara AM243x Launchpad.

Test Setup

The test setup of the clock signal compensation by using an additional clock signal with a software configurable phase delay measurement with an AMC1306EVM and C2000 TMS320F28379D Launchpad is shown in **Figure 156**. For this measurement, single-ended probes are used to measure the clock signal at AMC1306EVM clock input CLKIN and the data output, DOUT, of the Delta-Sigma modulator measured at the MCUs data input, SD1_D1 (GPIO122), of the SDFM. The clock signal with software programmable phase delay is measured at the clock input of the MCUs Sigma-Delta Filter Module (SDFM) SD1_C1 (GPIO123). The input pins AINP and AINN of the AMC1306EVM are shorted together tied to ground such that a 50/50 1's and 0's density is output. The analog supply, AVDD, is generated using the isolated transformer circuit on the EVM. The isolated modulators digital power supply, DVDD (3.3V), is supplied from the C2000 TMS320F28379D Launchpad.

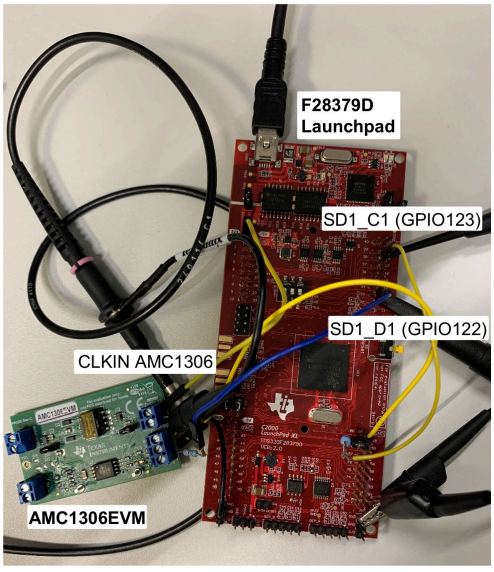


Figure 156. *Test Setup of Clock Signal Compensation by Phase Delay in Software With AMC1306EVM and C2000 TMS320F28379D Launchpad*

Figure 157 shows the same measurement setup with Sitara AM243x Launchpad with the corresponding measurement points.

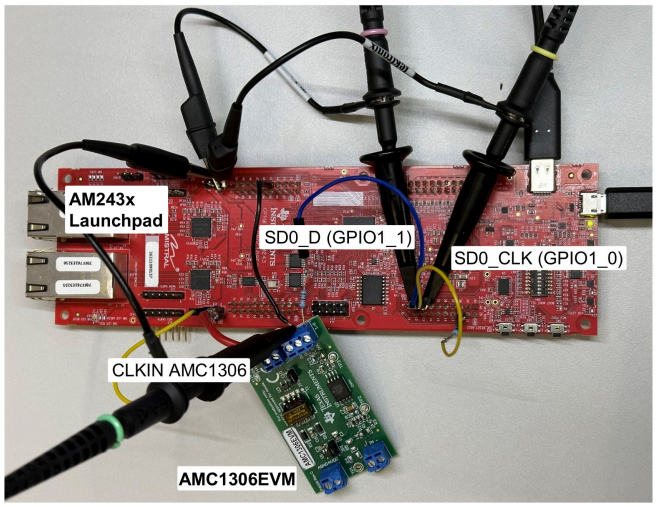


Figure 157. *Test Setup of Clock Signal Compensation by Software Configurable Phase Delay With AMC1306EVM and Sitara AM243x Launchpad*

Test Measurement Results

The TMS320F28379D was running an internal TI SDFM software project, where the two GPIOs GPIO122 and GPIO123 are configured for SDFM mode. The SDFM data filter is configured for Sinc3 with an oversampling ratio of 64 (OSR64). To conduct the test, a 20-MHz clock signal with a 50% duty cycle is generated with the ePWM4 module and fed into the CLKIN Pin of the AMC1306EVM. The ePWM5 module is configured to output a phase-locked 20-MHz clock signal with 50% duty cycle and 30-ns phase-shift. This signal is fed into SD1_C1 (GPIO123). Note that the AMC1306EVM DOUT data bitstream only changes at the rising clock edge, hence once per clock cycle as described in Section 7.11 *Switching Characteristics* of the AMC1306 data sheet.

Figure 158 shows the oscilloscope measurement and the interface diagram. The clock signal fed into the AMC1306EVM CLKIN Pin is represented by the green waveform on channel 3. The data signal output by the AMC1306EVM is the SD1_D1 (GPIO122) signal in red on channel 2. The phase-shifted clock signal fed into SD1_C1 (GPIO123) is the measured waveform in blue on channel 1. As the SDFM module samples the data signal against the rising edge of the phase-shifted clock signal SD1_C1 (GPIO123), the resulting setup time is approximately 18 ns and the resulting hold time is approximately 24 ns. With that the TMS320F28379D setup and hold timing of minimum 10 ns for the SDFM qualified GPIO (3-sample) mode 0 is met. In addition, this design offers an optimum margin to allow tolerances for changes (positive or negative) in the system propagation delay.

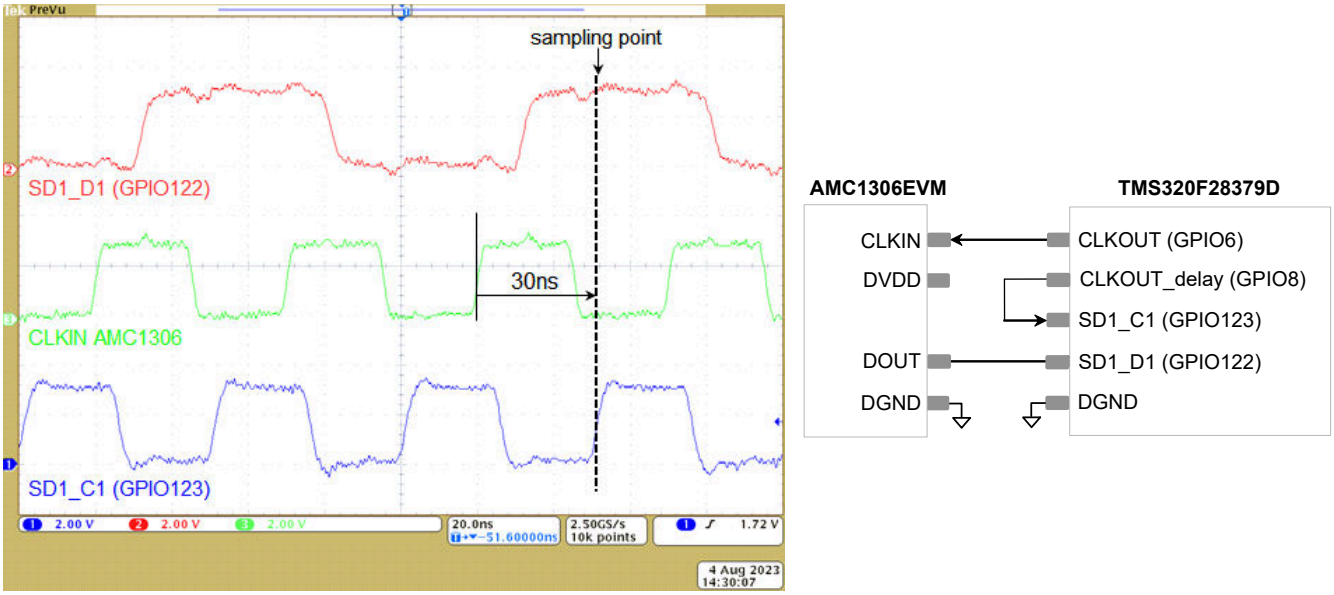


Figure 158. *Measurement Results of Digital Interface Timing of AMC1306EVM and TMS320F28379D With Clock Signal Compensation by Software Configurable Phase Delay*

Figure 159 shows the same measurement results for the test performed with the Sitara AM243x Launchpad. In conclusion the clock signal compensation by using an additional clock signal with a software configurable phase delay is an approved method to meet the MCUs setup and hold timing requirements. This method offers the highest degree of freedom, since not only the value of the phase shift is configurable, but this method also works for a wide range of MCUs due to only requiring an additional GPIO pin for the implementation of a phase shifted clock signal.

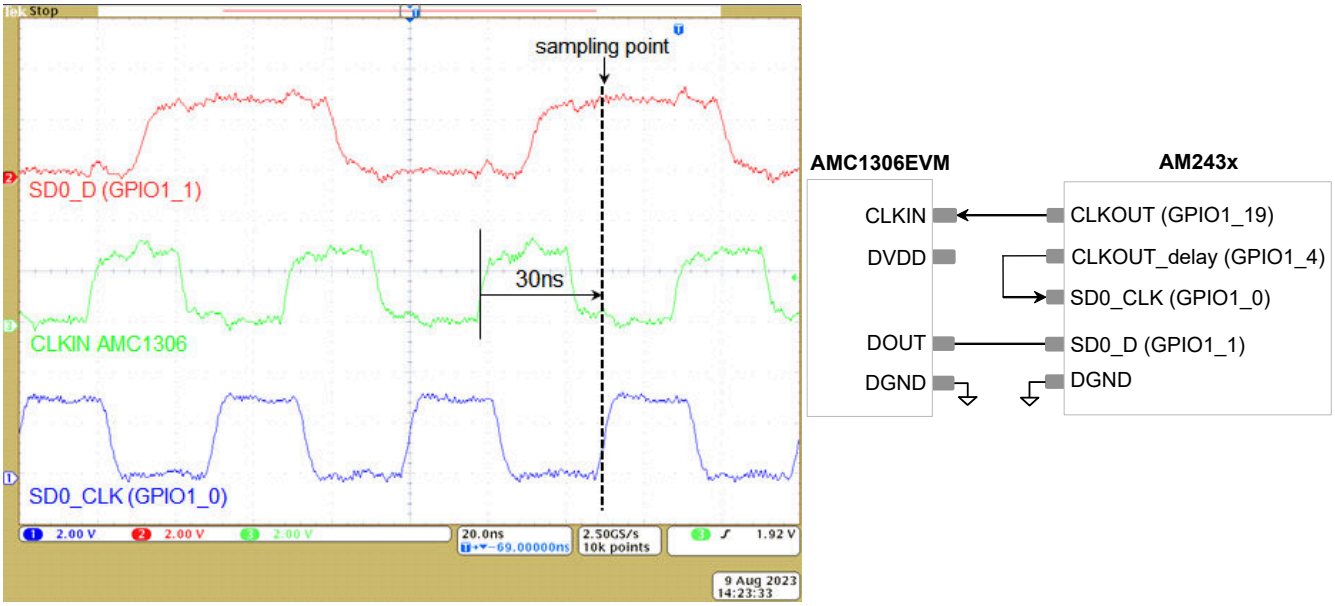


Figure 159. *Measurement Results of Digital Interface Timing of AMC1306EVM and AM243x With Clock Signal Compensation by Software Configurable Phase Delay*

Testing of Clock Signal Compensation by Clock Inversion at MCU

This configuration has been tested and validated with the C2000 TMS320F28379D Launchpad.

Test Setup

The test setup for clock signal compensation by clock inversion at the MCU using the C2000 TMS320F28379D Launchpad is shown in **Figure 160**. For this measurement two test signals are created by the MCU. One signal is connected to the clock input, SD1_C1, (GPIO123) of the MCUs SDFM and the other signal is connected to the data input, SD1_D1, (GPIO122) of the SDFM.

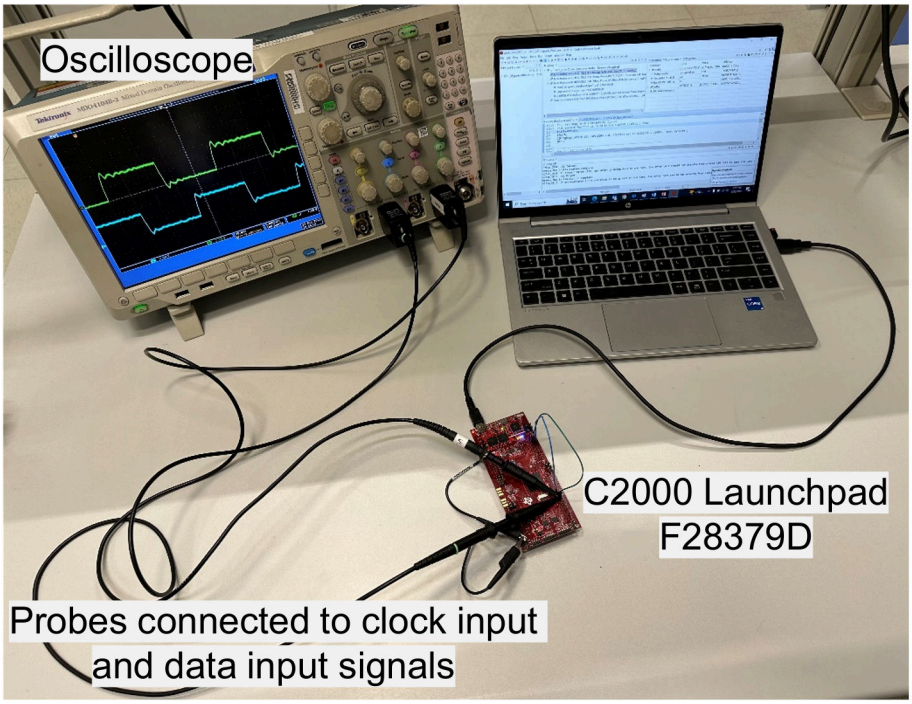


Figure 160. *Test Setup of Digital Interface Timing Validation*

Test Measurement Results

The TMS320F28379D was running an internal TI SDFM software project, where the two GPIOs GPIO122 and GPIO123 are configured for SDFM mode. The SDFM filter is configured for Sinc3 and OSR™ 64 filter. The Sinc3 OSR64 filter outputs a 16-bit two's complement integer number with a maximum full-scale range from +16384 to -16384.

To conduct the test, two 90-degree phase shifted 10-MHz clock signals with a 50% duty cycle are fed into GPIO123 (SD1_C1) and GPIO122 (SD1_D1) respectively. Note that the AMC1306EVM DOUT data bitstream only changes on the rising clock edge, hence once per clock cycle. For this test the SD1_D1 data toggles between 0 and 1 at every half clock cycle. This is different than the AMC1306EVM DOUT data signal, which changes at every clock cycle.

Due to applying this specific test signal, the input data at GPIO122 (SD1_D1) is always logic '1' at the rising clock edge of GPIO123 and always logic '0' at the falling edge. Hence the output of the Sinc3 filter with OSR 64 filter depends on which clock edge the test data is sampled in the SDFM and the Sinc3 OSR 64 filter output is either 16384 (always sampling '1') if there is no clock inversion at GPIO123 and -16384, if there is a clock inversion at GPIO123 (always sampling '0').

Test Result – No Clock Inversion of Clock Input at GPIO123

Figure 161 shows the oscilloscope measurement of the clock signal SD1_C1 which is input to GPIO123 and the phase shifted data signal SD1_D1 which is input to GPIO122. In this measurement GPIO123 is not inverted by the software, as shown below.

```
// Set 3-sample qualifier for GPIO122 and GPIO123 and do not invert GPIO123
GPIO_SetupPinOptions(122, GPIO_INPUT, GPIO_QUAL3);       // GPIO123 not inverted
GPIO_SetupPinMux(122,GPIO_MUX_CPU1,7); // MUX position 7 for SD1_D1
GPIO_SetupPinMux(123,GPIO_MUX_CPU1,7); // MUX position 7 for SD1_C1
```

The data SD1_D1 is sampled by the TMS320F28379D SDFM at the rising edge of SD1_C1. This corresponds to the rising edge of the non-inverted clock signal at GPIO123. The data sampled by the TMS320F28379D was always logic '1', validated through output of the Sinc3 OSR64 filter = +16384 in Code Composer Studio™ (CCS), as shown below.

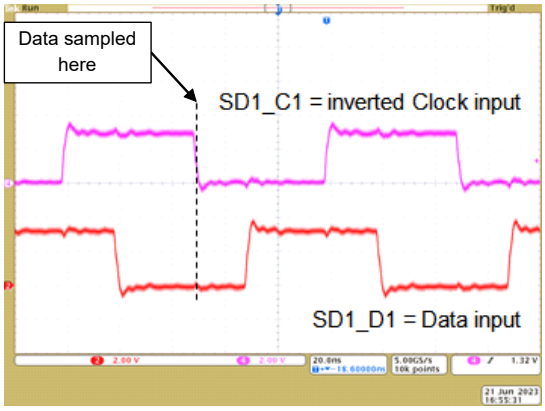
Figure 161. *Clock and Data Input Test Signals (Non-Inverted GPIO123) and Sinc3 OSR 64 Filter Output in CCS*

Test Result – Clock Inversion of Clock Input at GPIO123

Figure 162 shows the clock signal SD1_C1 which is input to GPIO123 and the phase shifted data signal SD1_D1 which is input to GPIO122. In this test setup GPIO123 is inverted by the software, as shown below.

```
// Set 3-sample qualifier for GPIO122 and GPIO123 and do not invert GPIO123
GPIO_SetupPinOptions(123, GPIO_INPUT, GPIO_INVERT | GPIO_QUAL3);
GPIO_SetupPinMux(122,GPIO_MUX_CPU1,7); // MUX position 7 for SD1_D1
GPIO_SetupPinMux(123,GPIO_MUX_CPU1,7); // MUX position 7 for SD1_C1
```

The data SD1_D1 is now sampled by F28379D SDFM at the falling edge of SD1_C1, which corresponds to the rising edge of the inverted clock signal at GPIO123 input. The data sampled by the F28379D was always logic '0', validated though output of the Sinc3 OSR64 filter = -16384 in Code Composer Studio, as shown below.



Variables | Expressions | Registers

Expression	Type	Value	Address
GpioCtrlRegs.GPDINV.bit.GPIO123	unsigned int : 1	1	0x00007CD1@Data bit 11
SD1_D1_SincOSR64	int	-16384	0x00014147@Data

Figure 162. *Clock and Data Input Test Signals (Non-Inverted GPIO123) and Sinc3 OSR 64 Filter Output in CCS*

In conclusion the method of clock signal compensation by inverting the clock input of the GPIO input in software was validated. By inverting the clock, a fixed delay of half of the clock period is added to the clock signal which can be sufficient to meet the TMS320F28379D setup and hold of minimum timings of 10 ns for the SDFM qualified GPIO (3-sample) mode 0. However, each system design needs to be checked individually if the resulting timings for setup and hold of the MCU for the SDFM qualified GPIO (3-sample) mode 0 can be met.

Digital Interface Timing Validation by Calculation Tool

A **calculation tool** was developed for simulation and validation purposes of the digital interface timings between an MCU and isolated Delta-Sigma modulators. The most common used isolated Delta-Sigma modulators **AMC1306M25** and **AMC1305L25** were selected for the digital interface timing analysis. **AMC1305L25** has a LVDS interface type and requires LVDS driver and LVDS receiver when interfacing a MCU with CMOS interface. The MCU can be individually selected by the user, as only the setup and hold time requirements are entered into the calculation tool. In the following use of the calculation tool for the optimization of the digital interface timing between **AMC1305L25** and C2000 MCU **TMS320F28379D** is shown step by step.

Digital Interface With No Compensation Method

The C2000 MCU **TMS320F28379D** is operated in SDFM GPIO input qualification (3-sample window) option in mode 0 at 200 MHz system clock. The minimum setup and hold time are both 10 ns: $t_{su\ (SDDV-SDCH)M0}$(MIN) = 10 ns and $t_{h(SDCH-SDD)M0}$ (MIN) =10 ns are entered into the calculation tool. Furthermore, propagation delays of LVDS driver **DSLVDS1047** and LVDS receiver **DSLVDS1048** are entered for reference. With a 20-MHz clock signal at the isolated Delta-Sigma modulator clock input, which is the maximum clock frequency specified in the data sheet, the MCUs setup time requirements are violated when the data delay time t_D of AMC1305L25 equals the minimum specification given in the data sheet with t_D (MIN) = 0 ns, as shown in table 2.

Table 26. Results for C2000 MCU TMS320F28379D Digital Interface Timings Using AMC1305L25 at 20-MHz Clock Frequency

Min. Setup Time @MCU	5.6 ns
Max. Setup Time @MCU	23.3 ns
Min. Hold Time @MCU	26.7 ns

Table 26. Results for C2000 MCU TMS320F28379D Digital Interface Timings Using AMC1305L25 at 20-MHz Clock Frequency (continued)

Max. Hold Time @MCU	44.4 ns

Commonly Used Method - Reduction of the Clock Frequency

A compromise to meet the MCUs timing requirements is to reduce the modulator clock frequency. In this example a 17 MHz clock frequency allows the setup and hold timing requirements of the MCU to be met. The calculated setup and hold times including minimum and maximum values at a clock frequency of 17 MHz are shown in **Table 27**. The margin for the minimum setup time to the MCUs setup time requirement is 0 ns. This means tolerances in the system can possibly lead to incorrect acquisition of data. A larger margin for tolerances in the system can be achieved by further reducing the clock frequency, but this has a negative effect on the system performance.

Table 27. TMS320F28379D Digital Interface Timings Using AMC1305L25 at 17-MHz Clock

Min. Setup Time @MCU	10.0 ns
Max. Setup Time @MCU	27.7 ns
Min. Hold Time @MCU	31.1 ns
Max. Hold Time @MCU	48.8 ns

Clock Edge Compensation With Software Configurable Phase Delay

The digital interface with clock edge compensation with software configurable phase delay is shown in **Figure 163**. The timing diagram shows a clock signal with a clock frequency of 20 MHz, representing the clock signal which is fed into the isolated Delta-Sigma modulator, as the first signal. The second signal plotted in the timing diagram represents the data output of the isolated Delta-Sigma modulator for typical specifications given in the data sheet. The third signal represents the 20-MHz clock signal phase-shifted by 10 ns in reference to the first signal which is fed into the clock input of the MCUs SDFM.

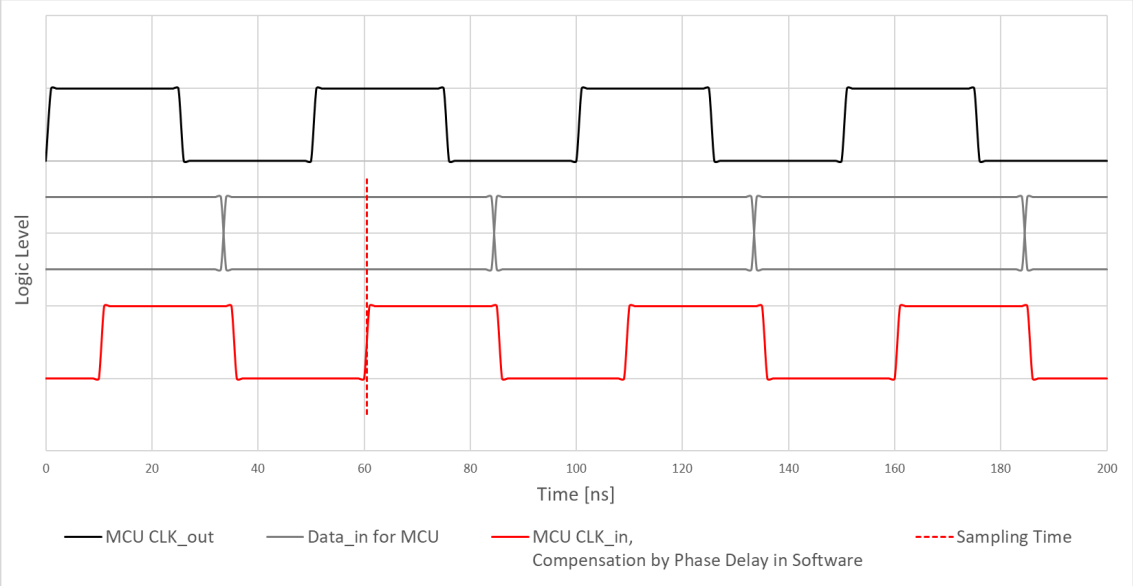


Figure 163. *Timing Diagram C2000 Digital Interface to AMC1305L25 for Typical Specifications in the Data Sheet at 20-MHz Clock Frequency With Clock Edge Compensation With Software Configurable Phase Delay*

The calculated setup and hold times including minimum and maximum values are shown in **Table 28**. As the phase delay is configurable in the software, the value of the phase delay can be selected such that the data acquisition timing is centered in the data signal. This allows the maximum possible margin to be available for setup and hold timing so that tolerances in the system do not affect the data acquisition. The calculation tool is providing the margin of the digital timing interface helping to understand the acceptable tolerances of the system. For a selected phase delay of 10 ns, the minimum setup time is 15.6 ns, resulting in a margin of 5.6 ns after subtracting the MCU setup time requirement of 10 ns. The margin for the minimum hold time is calculated accordingly and amounts to 6.7 ns.

Table 28. TMS320F28379D Digital Interface Timings With AMC1305L25 at 20-MHz Clock With Software Configurable Phase Delay

Phase Delay	**Suggested Phase Delay**		**Selected Phase Delay**
	min	**4.4 ns**	**10.0 ns**
	max	**16.7 ns**	
Min. Setup Time @MCU			15.6 ns
Max. Setup Time @MCU			33.3 ns
Min. Hold Time @MCU			16.7 ns
Max. Hold Time @MCU			34.4 ns

Conclusion

Clock edge delay compensation helps to meet setup and hold time requirements with isolated Delta-Sigma modulators and the MCUs digital interface without the necessity of reducing the modulator clock frequency. This allows the system to operate at full performance.

The clock edge delay compensation can be implemented by various methods these are compensation by:

- Additional Clock Signal with software configurable phase delay
- Clock Signal with hardware configurable phase delay
- Clock Return
- Clock Inversion at MCU

Compensation methods such as additional clock signal with software configurable phase delay and clock inversion at MCU were analyzed in more detail for the most common used isolated Delta-Sigma modulator variants and validated with AMC1306EVM evaluation module and C2000 TMS320F28379D Launchpad as well as Sitara AM243x Launchpad chosen as MCUs. The test results hold true for MCUs with CMOS interface and SDFM as well as for Sitara MCUs with no SDFM when working with PRU.

Table 29 shows the benefits and drawbacks of each clock signal compensation method. In the following the abbreviations SW Phase Delay and HW Phase Delay are used for compensation with software configurable phase delay and hardware configurable phase delay.

Table 29. Comparison of clock edge compedation methods

Method	Benefits	Drawbacks
SW Phase delay	• Compensation of any propagation delays • Allows the use of the maximum clock frequency enabling highest reliable communication • Implementation of precise phase delays • Change during run-time possible • No additional BoM cost	• One additional MCU GPIO and internal phase locked clock source is required • Additional MCU software
HW Phase delay	• No change of MCU software • No additional MCU GPIO is required	• Compensation dependent on implemented hardware delay hardware • Tolerance in the precision of phase delay by hardware components • No changes during run-time possible • Adds BoM cost
Clock Return	• No software and hardware efforts	• Does not work for all configurations • Adaptation of the layout • Longer clock signal more sensitive to transient noise
Clock Inversion	• Simple implementation, if compensation by one half of the clock period solves the timing differences	• Does not work for all configurations • Fixed compensation by one half of the clock period only • MCU needs to be capable of inverting the clock signal at the GPIO input

Depending on the type of the Delta-Sigma Modulator, differentiated by external or internal clock source and CMOS or LVDS interface, different clock signal compensation methods can be better than others. **Table 30** compares the suggested compensation methods for each type of Delta-Sigma modulator which are commonly used.

Table 30. Suggested clock edge compensation methods for modulators with internal or external clock

Method	AMC1306M25 external clock (CMOS)	AMC1305L25 external clock (LVDS)	AMC1303M2520/10 internal clock (CMOS)
Software Phase Delay	+	+	N/A
Hardware Phase Delay	o	o	o
Clock Return	o	-	N/A
Clock Inversion	o	o	+

For modulators which require an external clock, the clock signal compensation with software configurable phase delay offers the best performance, followed by the clock inversion at the MCU, if a fixed one-half of clock cycle meets the requirements. Both of these clock signal compensation methods help to meet the setup and hold timing

requirements of the MCU especially at higher modulator clock frequencies. The following calculation tool can be used to validate the setup and hold timing requirements of the MCU when using the Delta-Sigma modulator AMC1306M25 and AMC1305L25.

References

- Texas Instruments, ***Achieving Better Signal Integrity With Isolated Delta-Sigma Modulators in Motor Drives*** application report
- Texas Instruments, **High-performance isolated ADCs for high-voltage systems**, overview
- Texas Instruments, ***Comparing isolated amplifiers and isolated modulators*** white paper
- Texas Instruments, ***AMC1306x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With High CMTI*** data sheet
- Texas Instruments, ***AMC1305x High-Precision, Reinforced Isolated Delta-Sigma Modulators*** data sheet
- Texas Instruments, ***AMC1303x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With Internal Clock*** data sheet
- Texas Instruments, ***TMS320F2837xD Dual-Core Microcontrollers*** data sheet
- Texas Instruments, ***TMS320F2837xD Dual-Core Microcontrollers*** technical reference manual
- Texas Instruments, ***AM243x Sitara™ Microcontrollers*** data sheet
- Texas Instruments, ***MCU-PLUS-SDK-AM243X Software development kit (SDK)*** tool

Utilizing AMC3311 to Power AMC23C11 for Isolated Sensing and Fault Detection

Application Brief

Introduction

Fault-detection is essential in applications including **motor drives** , **servo drives** , **onboard chargers (OBCs)**, **string inverters** , and **micro inverters** . Separating the high voltage domain and the low voltage domain across an isolation barrier allows the system to operate at different common-mode voltages. The high voltage domain performs a function while the low voltage domain controls equipment. This prevents both electrical damage to the low voltage circuitry and harm to users. Detecting faults such as overvoltage is required when operating at high common-mode voltages. This document highlights how the AMC3311 can offer high-side supply current from HLDO_OUT to power the high voltage domain of the AMC23C11 isolated comparator for a compact fault detection design.

The AMC3311 is a precision, reinforced, isolated amplifier. This device has a 0-2 V input voltage range, which is an option for precision isolated DC voltage measurements that drive the control loop. This device features an integrated DC/DC converter that supports high-side supply current for auxiliary circuitry of 4 mA. This allows for single-supply operation from the low-side to high-side of the device for both the feedback measurement of the AMC3311 and the overvoltage fault detection of the AMC23C11. The AMC23C11 is a fast response, reinforced, isolated comparator. The device can be used for rapid overcurrent or overvoltage sensing with an adjustable trip threshold. The device requires a high-side supply current of 2.7 mA. The AMC3311 is the first isolated amplifier with an integrated DC/DC converter to enable the two devices to work as a pair for applications that require a precision isolated amplifier for control functions and a fast-acting comparator for overcurrent or overvoltage protection.

AMC3311 used to power AMC23C11

The AMC3311 offers an isolated power supply capable of providing up to 4 mA through the HLDO_OUT pin for connected components that require a high-side supply. This feature directly allows the use of higher performance isolated comparators such as the AMC23C11.

The available supply current from the AMC3311 allows a wider range of companion devices to be used with the isolated amplifier. **Figure 164** shows an example schematic of how to use the AMC3311 to power the high side of the AMC23C11. In the schematic, HLDO_OUT at pin five on the AMC3311 shows a trace that extends to VDD1 at pin one of the AMC23C11. The isolated comparator compares the input voltage to the reference voltage at pin three. The device pulls down the open-drain output if the input voltage exceeds the threshold established as the reference voltage. The threshold voltage can be adjusted by modifying the value of the reference resistor in relation to the internal 100-µA current source.

Additionally, the AMC23C11 has a 1.4-V margin overhead voltage. The threshold voltage cannot be higher than the difference of the 3.2-V input and 1.4-V margin (1.8 V.) A resistor is placed between REF and GND1 to define the trip voltage as 1.07 V. As a result, this overhead requirement limits the threshold voltage on the isolated comparator to be lower than the true cutoff voltage seen on the amplifier. For example, when the true cutoff voltage is 2.14 V on the amplifier, the isolated comparator cannot monitor the voltage because the voltage exceeds the bounds set by the margin overhead voltage. As a result, RSNS is separated into two equal resistors (RSNS1 and RSNS2) to define the cutoff

voltage to be proportionately half of the voltage that the AMC3311 requires. Instead, the AMC23C11 reads 1.07 V as the reference voltage.

Figure 165 shows an example of a PCB layout example that routes the devices in combination.

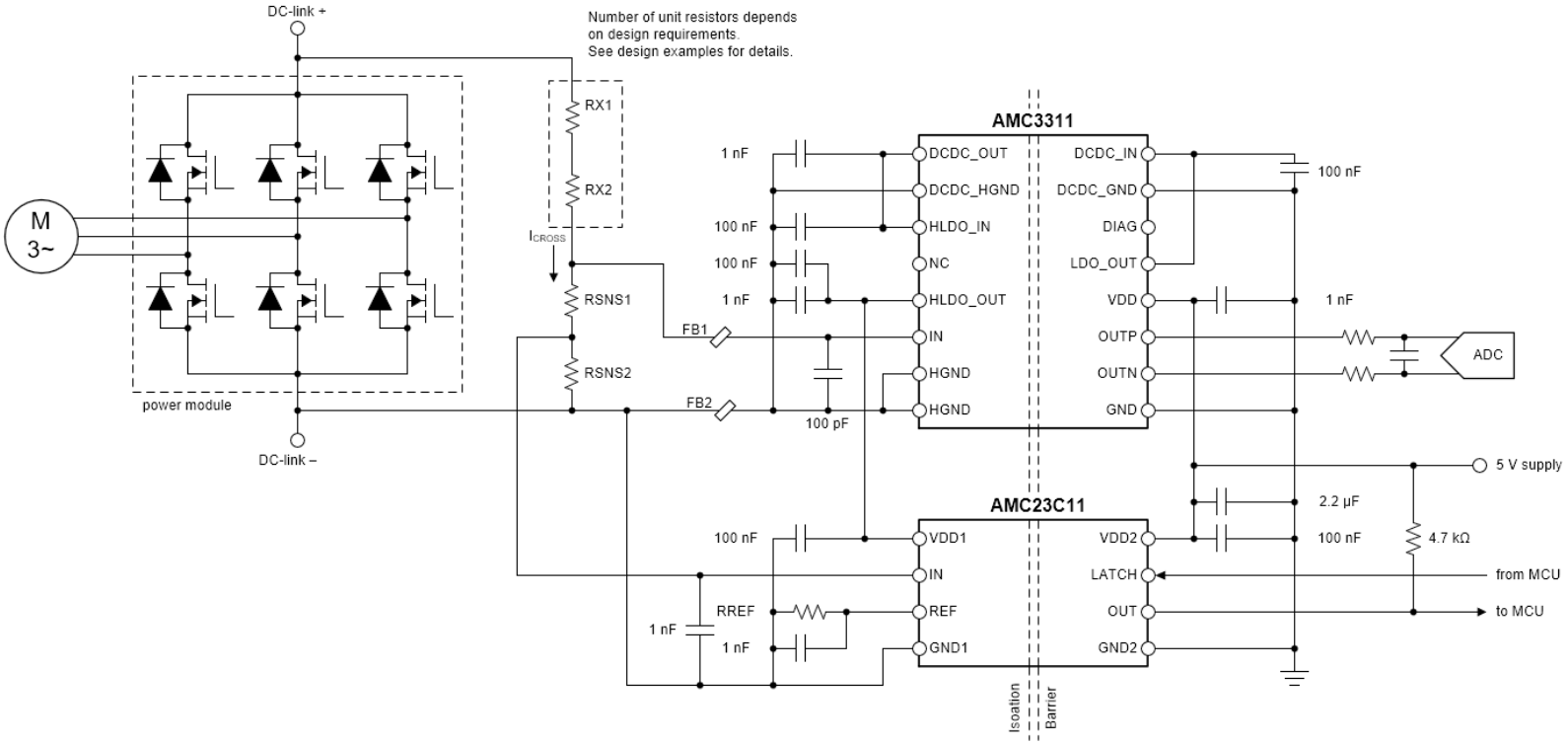


Figure 164. *AMC3311 and AMC23C11 Schematic*

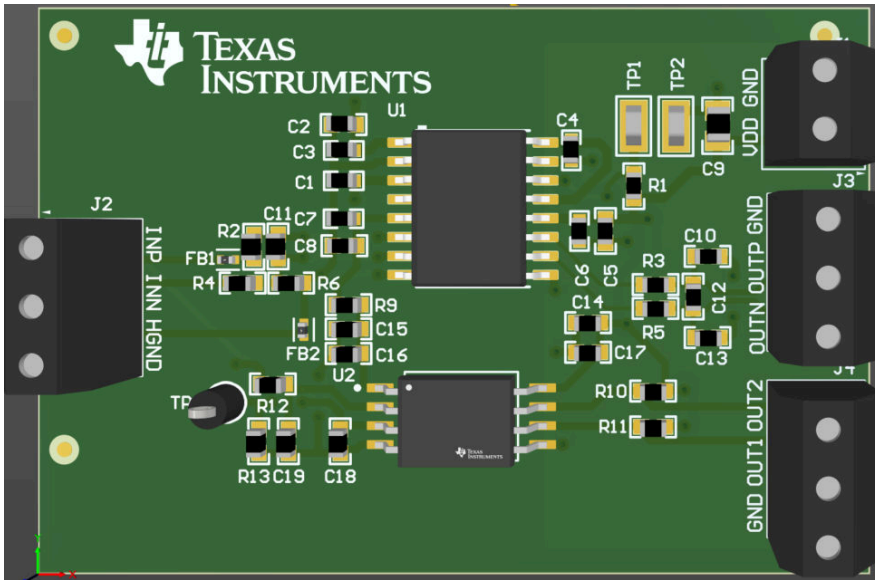


Figure 165. *AMC3311 and AMC23C11 PCB Layout*

AMC23C11 used for overvoltage detection

Figure 166 and **Figure 167** show the overvoltage response times in the AMC3311 and the AMC23C11, respectively. Using a 3.2-V power supply, the input signal (CH4) shows the voltage rise above the 1.07 V overvoltage threshold.

The response time on the AMC3311, VOUTP (CH2), and VOUTN channels (CH1) is 2.906 µs, while the response time on the AMC23C11, OUT (CH3), is 314.015 ns. The amplifier takes greater than nine times the length the isolated comparator takes to detect overvoltage. This time delay can be too long for low latency applications. To supplement the AMC3311 amplifier, the isolated comparator can be used to prevent an overvoltage, as the comparator quickly detects voltages higher than the set threshold. This notifies the controller to shut down all affected electronics, which offers increased safety and reliability in high voltage applications.

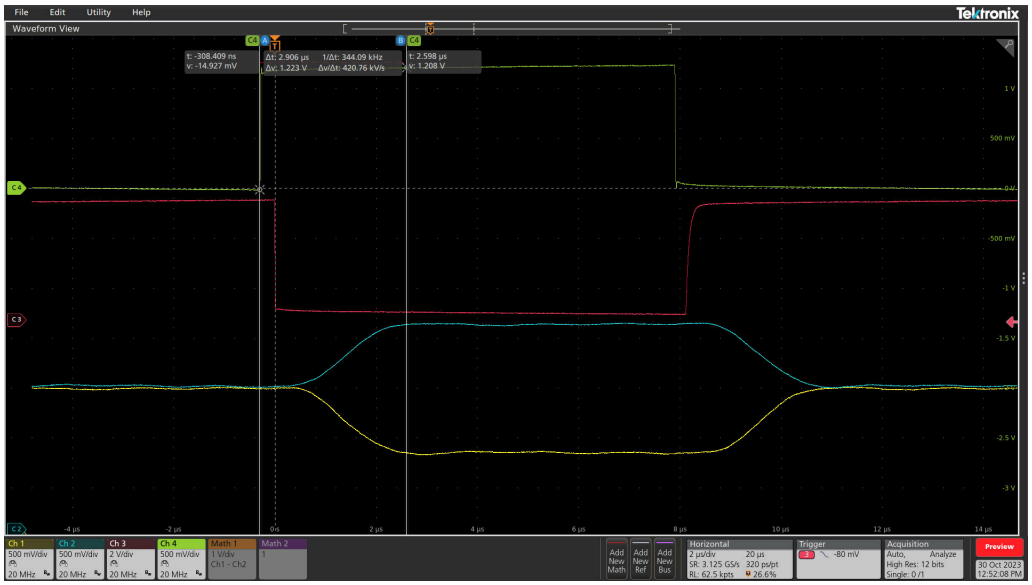


Figure 166. *AMC3311 Overvoltage Response Timing Waveform*

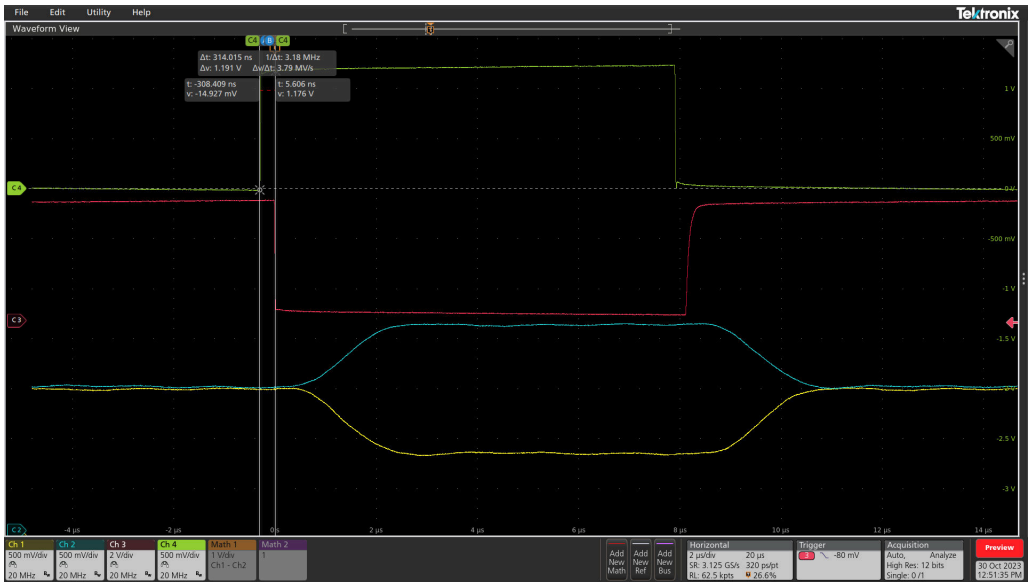


Figure 167. *AMC23C11 Overvoltage Response Timing Waveform*

Conclusion

The AMC3311 is an isolated amplifier with a high-side current supply that can be leveraged to power auxiliary sensing circuits. The device can power external devices up to 4 mA on the high-side, and is compatible with high-speed isolated comparators such as the AMC23C11. This comparator offers the advantage of a significantly faster response time to enable overvoltage protection. Using the AMC3311 and AMC23C11 together can be a useful option for voltage and current sensing applications.

Additional Resources

- Texas Instruments, **Precision labs series: Introduction to isolation**, video series.
- Texas Instruments, ***AMC3311-Q1 Automotive, Precision, 2-V Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter***, data sheet.
- Texas Instruments, ***AMC23C11 Fast Response, Reinforced Isolated Comparator With Adjustable Threshold and Latch Function***, data sheet.
- Texas Instruments, ***Isolation Glossary***
- Texas Instruments, ***Isolated Amplifier Voltage Sensing Excel Calculator***, design resource.

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