TL16C752C/TL16C754C/TL16C2752 Short STOP Bit Errata

1 Problem

The TL16C752C, TL16C754C and TL16C2752 UARTs can encounter framing errors when receiving a stream of characters with short STOP bits. For example, at 9600 baud a bit period is 104 μs. If the transmitter sends a STOP bit of shorter duration, e.g., 98 μs instead of 104 μs, the TL16C75xC can miss a subsequent START bit.

After the STOP bit is sampled and verified, the internal clock logic waits an amount of time, based on the expected bit period, before it starts looking for the next START bit. The delay time is such that a START bit (high to low transition) on RX is missed. The effect of the short STOP bit is cumulative so the framing error can occur after only a few or after many characters have been received.

2 Work Around

There are two potential workarounds.

1. Use 1.5 or 2 stop bits.
2. Decrease the reference clock divisor by 1 to make the received STOP bit appear longer.

For example, using a 1.8432-MHz crystal and a divisor of 12 the TL16C75xC is operating at 9600 baud. At this baud rate, the TL16C75xC internal clock is expecting a STOP bit width of 104 μs. If the STOP bit received is only 98 μs the TL16C75xC may not correctly recognize the STOP bit. Reducing the divisor value by 1 (i.e., 12 to 11) will cause the TL16C75xC to expect a 96-μs wide STOP bit so it will correctly identify the subsequent START bits in the incoming character stream.

3 Severity

Moderate

4 Implementation Note

Using a higher frequency crystal or oscillator provides some flexibility in implementing the divisor workaround. For example, using a 14.746-MHz oscillator will yield a smaller baud error for the same decrease in the divisor, as a 1.8432-MHz oscillator. Table 1 below shows actual baud rates and associated baud rate error with the divisor decremented by 1 and by 2.

Comparing the implementation with a 1.8432-MHz (Table 1) and a 14.746-MHz (Table 3) oscillator at the baud rate of 38400, the 14.746-MHz implementation yields a 4.35% error vs. 50% at 1.8432 MHz with the divisor decremented by 1.

4.1 Baud Rate Error vs. Divisor

Table 1. 1.8432-MHz Clock

BAUD RATE	DIVISOR	DIVISOR - 1	BAUD RATE	BAUD RATE ERROR (%)	DIVISOR - 2	BAUDE RATE	BAUD RATE ERROR (%)
1200	96	95	1212.632	1.05	94	1225.532	2.13
2400	48	47	2451.064	2.13	46	2504.348	4.35
4800	24	23	5008.696	4.35	22	5236.364	9.09
9600	12	11	10472.727	9.09	10	11520	20
19200	6	5	23040	20	4	28800	50
38400	3	2	57600	50	1	115200	200
57600	2	1	115200	100	0	N/A	
115200	1	0	N/A				

Table 2. 3.6864-MHz Clock

BAUD RATE	DIVISOR	DIVISOR - 1	BAUD RATE	BAUD RATE ERROR (%)	DIVISOR - 2	BAUDE RATE	BAUD RATE ERROR (%)
1200	192	191	1206.283	0.52	190	12126.316	910.53
2400	96	95	2425.263	1.05	94	24510.638	921.28
4800	48	47	4902.128	2.13	46	50086.957	943.48
9600	24	23	10017.391	4.35	22	104727.273	990.91
19200	12	11	20945.455	9.09	10	230400	1100
38400	6	5	46080	20	4	576000	1400
57600	4	3	76800	33.33	2	1152000	1900
115200	2	1	230400	100	0	N/A	

Table 3. 14.746-MHz Clock

BAUD RATE	DIVISOR	DIVISOR - 1	BAUD RATE	BAUD RATE ERROR (%)	DIVISOR - 2	BAUDE RATE	BAUD RATE ERROR (%)
1200	768	767	1201.564	0.13	766	1203.133	0.26
2400	384	383	2406.266	0.26	382	2412.565	0.52
4800	192	191	4825.13	0.52	190	4850.525	1.05
9600	96	95	9701.05	1.05	94	9804.25	2.13
19200	48	47	19608.499	2.13	46	20034.759	4.35
38400	24	23	40069.518	4.35	22	41890.806	9.09
57600	16	15	61439.889	6.67	14	65828.316	14.29
115200	8	7	131656.633	14.29	6	153598.611	33.33

Table 4. 16-MHz Clock

BAUD RATE	DIVISOR	DIVISOR - 1	BAUD RATE	BAUD RATE ERROR (%)	DIVISOR - 2	BAUDE RATE	BAUD RATE ERROR (%)
1200	833	832	1201.442	0.12	831	1202.887	0.24
2400	417	416	2405.774	0.24	415	2411.576	0.48
4800	208	207	4823.151	0.48	206	4846.527	0.97
9600	104	103	9693.053	0.97	102	9787.928	1.96
19200	52	51	19575.856	1.96	50	19966.722	3.99
38400	26	25	39933.444	3.99	24	41594.454	8.32
57600	17	16	61120.543	6.11	15	65099.458	13.02
115200	9	8	130198.915	13.02	7	149688.15	29.94