Functional Safety Information

TPS3840-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS3840-Q1 (DBV package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

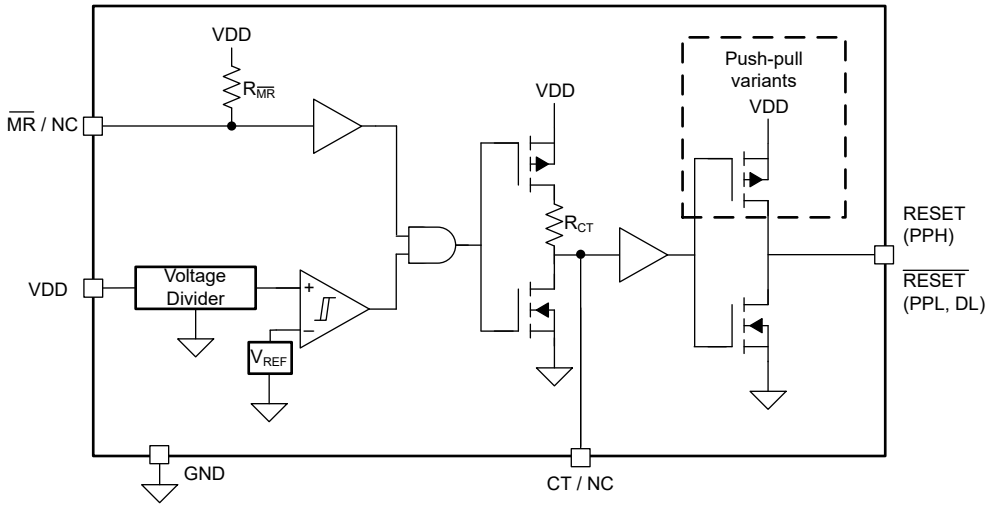

Figure 1-1. Functional Block Diagram

The TPS3840-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS3840-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	2
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: TBD mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS3840-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Incorrect channel selected	15
Channel-channel short	10
ADC output code bit error	15
ADC gain out of specification	20
ADC offset out of specification	20
Communication error	20

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS3840-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS3840-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS3840-Q1 data sheet.

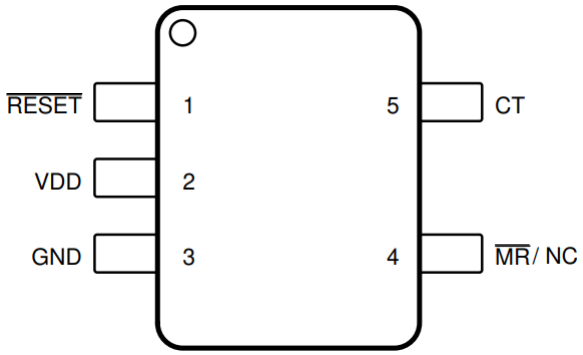

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Vdd(min) < Vdd < Vdd (max) Assumption
- Reset is connected to VDD with 10.5 kΩ pull-up resistor

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
$\overline{\text{RESET}}$	1	Forces $\overline{\text{RESET}}$ to be held low	B
VDD	2	VDD short to GND Fault. The device is non-operational	B
GND	3	No damage to device. No impact to functionality	D
$\overline{\text{MR}}$ / NC	4	Normal operation. $\overline{\text{RESET}}$ will be asserted	B
CT	5	$\overline{\text{RESET}}$ is forced and held low when VDD goes below threshold. Device is non-operational	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
$\overline{\text{RESET}}$	1	Unreliable reset output functionality	B
VDD	2	The device is unpowered and non-operational	B
GND	3	The $\overline{\text{RESET}}$ and VDD are both held low	B
$\overline{\text{MR}}$ / NC	4	Normal Operation. This pin can be left floating	D
CT	5	Normal Operation. This pin can be left floating	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
$\overline{\text{RESET}}$	1	VDD	Large current can flow into $\overline{\text{RESET}}$ when in error condition. This can cause permanent damage	A
VDD	2	GND	The device is non-operational	B
GND	3	$\overline{\text{MR}}$ / NC	Normal operation. $\overline{\text{RESET}}$ will be asserted	B
$\overline{\text{MR}}$ / NC	4	CT	$\overline{\text{RESET}}$ is forced and held low when VDD goes below threshold. Device is non-operational	B
CT	5	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ is forced and held low when VDD goes below threshold. Device is non-operational	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
$\overline{\text{RESET}}$	1	Large current can flow into $\overline{\text{RESET}}$ when in error condition. This can cause permanent damage	A
VDD	2	Normal Operation	D
GND	3	VDD short to GND fault. Device is non-operational	B
$\overline{\text{MR}}$ / NC	4	Normal operation	D
CT	5	Forces $\overline{\text{RESET}}$ to be held low. Device is non-operational	B

5 Revision History

Changes from Revision * (December 2019) to Revision A (November 2023)	Page
• Added pin diagram and pin FMA data in Section 4	5

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265