LOW-POWER, 16-BIT, 1-MHz, SINGLE/DUAL UNIPOLAR INPUT, ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL INTERFACE

FEATURES

- **2.7-V to 5.5-V Analog Supply, Low Power:**
  - **15.5 mW (1 MHz, +VA = 3 V, +VBD = 1.8 V)**
- **1-MHz Sampling Rate 3 V ≤ +VA ≤ 5.5 V, 900-kHz Sampling Rate 2.7 V ≤ +VA ≤ 3 V**
- **Excellent DC Performance:**
  ±1.0 LSB Typ, ±1.75 LSB Max INL
  ±0.5 LSB Typ, ±1 LSB Max DNL
  16-Bit NMC Over Temperature
  ±0.5 mV Max Offset Error at 3 V
  ±1 mV Max Offset Error at 5 V
- **Excellent AC Performance at f_I = 10 kHz with 93 dB SNR, 105 dB SFDR, –102 dB THD**
- **Built-In Conversion Clock (CCLK)**
- **1.65 V to 5.5 V I/O Supply:**
  SPI/DSP Compatible Serial
  SCLK up to 50 MHz
- **Comprehensive Power-Down Modes:**
  Deep Power-Down
  Nap Power-Down
  Auto Nap Power-Down
- **Unipolar Input Range: 0 V to V_{REF}**
- **Software Reset**
- **Global $\overline{\text{CONVST}}$ (Independent of $\overline{\text{CS}}$)**
- **Programmable Status/Polarity EOC/$\overline{\text{INT}}$**
- **16-Pin 4 × 4 QFN and 16-Pin TSSOP Packages**
- **Multi-Chip Daisy Chain Mode**
- **Programmable TAG Bit Output**
- **Auto/Manual Channel Select Mode (ADS8330)**

APPLICATIONS

- **Communications**
- **Transducer Interface**
- **Medical Instruments**
- **Magnetometers**
- **Industrial Process Control**
- **Data Acquisition Systems**
- **Automatic Test Equipment**

DESCRIPTION

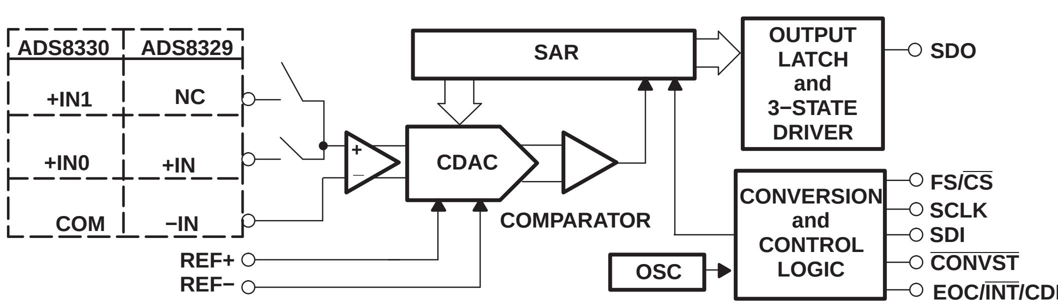
The ADS8329 is a low-power, 16-bit, 1-MSPS analog-to-digital converter (ADC) with a unipolar input. The device includes a 16-bit capacitor-based SAR ADC with inherent sample-and-hold.

The ADS8330 is based on the same core and includes a 2-to-1 input MUX with programmable option of TAG bit output. Both the ADS8329 and ADS8330 offer a high-speed, wide voltage serial interface and are capable of chain mode operation when multiple converters are used.

These converters are available in 4 × 4 QFN and 16-pin TSSOP packages, and are fully specified for operation over the industrial –40°C to +85°C temperature range.

Low Power, High-Speed SAR Converter Family

Type/Speed		500 kSPS	1 MSPS
16-bit single-ended	Single	ADS8327	ADS8329
	Dual	ADS8328	ADS8330
14-bit single-ended	Single	—	ADS7279
	Dual	—	ADS7280
12-bit single ended	Single	—	ADS7229
	Dual	—	ADS7230



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	MAXIMUM OFFSET ERROR (mV)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA, QUANTITY
ADS8329I	±2.5	–1/+2	±0.8	4 × 4 QFN-16	RSA	–40°C to +85°C	ADS8329IRSAT	Small tape and reel, 250
							ADS8329IRSAR	Tape and reel, 3000
				TSSOP-16	PW		ADS8329IPW	Tube, 90
							ADS8329IPWR	Tape and reel, 2000
ADS8329IB	±1.75	±1	±0.5	4 × 4 QFN-16	RSA	–40°C to +85°C	ADS8329IBRSAT	Small tape and reel, 250
							ADS8329IBRSAR	Tape and reel, 3000
				TSSOP-16	PW		ADS8329IBPW	Tube, 90
							ADS8329IBPWR	Tape and reel, 2000
ADS8330I	±2.5	–1/+2	±0.8	4 × 4 QFN-16	RSA	–40°C to +85°C	ADS8330IRSAT	Small tape and reel, 250
							ADS8330IRSAR	Tape and reel, 3000
				TSSOP-16	PW		ADS8330IPW	Tube, 90
							ADS8330IPWR	Tape and reel, 2000
ADS8330IB	±1.75	±1	±0.5	4 × 4 QFN-16	RSA	–40°C to +85°C	ADS8330IBRSAT	Small tape and reel, 250
							ADS8330IBRSAR	Tape and reel, 3000
				TSSOP-16	PW		ADS8330IBPW	Tube, 90
							ADS8330IBPWR	Tape and reel, 2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted.(1)

			UNIT
	Voltage	+IN to AGND	–0.3 V to +VA + 0.3 V
		–IN to AGND	–0.3 V to +VA + 0.3 V
	Voltage range	+VA to AGND	–0.3 V to 7 V
		+REF to AGND	–0.3 V to +VA + 0.3 V
		–REF to AGND	–0.3 V to 0.3 V
		+VBD to BDGND	–0.3 V to 7 V
		AGND to BDGND	–0.3 V to 0.3 V
	Digital input voltage to BDGND		–0.3 V to +VBD + 0.3 V
	Digital output voltage to BDGND		–0.3 V to +VBD + 0.3 V
T_A	Operating free-air temperature range		–40°C to +85°C
T_{stg}	Storage temperature range		–65°C to +150°C
	Junction temperature (T_J max)		+150°C
	4 × 4 QFN-16 package	Power dissipation	$(T_J Max – T_A)/\theta_{JA}$
		θ_{JA} thermal impedance	+47°C/W
	TSSOP-16 package	Power dissipation	$(T_J Max – T_A)/\theta_{JA}$
		θ_{JA} thermal impedance	+86°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, +VA = 4.5 V to 5.5 V, +VBD = 1.65 V to 5.5 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MHz, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT							
	Full-scale input voltage (1)		+IN – (–IN) or (+INx – COM)	0		$+V_{REF}$	V
	Absolute input voltage		+IN, +IN0, +IN1	AGND – 0.2		+VA + 0.2	V
			–IN or COM	AGND – 0.2		AGND + 0.2	
	Input capacitance				40	45	pF
	Input leakage current		No ongoing conversion, dc input	–1		1	nA
	Input channel isolation, ADS8330 only		At dc		109		dB
			V_I = ±1.25 V_{PP} at 50 kHz		101		
SYSTEM PERFORMANCE							
	Resolution				16		Bits
	No missing codes			16			Bits
INL	Integral linearity	ADS8329IB, ADS8330IB		–1.75	±1.2	1.75	LSB (2)
		ADS8329I, ADS8330I		–2.5	±1.5	2.5	
DNL	Differential linearity	ADS8329IB, ADS8330IB		–1	±0.4	1	LSB (2)
		ADS8329I, ADS8330I		–1	±0.5	2	
E_O	Offset error (3)	ADS8329IB, ADS8330IB		–1	±0.27	1	mV
		ADS8329I, ADS8330I		–1.25	±0.8	1.25	
	Offset error drift		FSR = 5 V		+0.4		ppm/°C
E_G	Gain error			–0.25	–0.04	0.25	%FSR
	Gain error drift				+0.75		ppm/°C
CMRR	Common-mode rejection ratio		At dc		70		dB
			V_I = 0.4 V_{PP} at 1 MHz		50		
	Noise				33		µV RMS
PSRR	Power-supply rejection ratio		At FFFFh output code (3)		78		dB
SAMPLING DYNAMICS							
t_{CONV}	Conversion time				18		CCLK
$t_{SAMPLE1}$	Acquisition time		Manual trigger	3			CCLK
$t_{SAMPLE2}$			Auto trigger		3		
	Throughput rate					1	MHz
	Aperture delay				5		ns
	Aperture jitter				10		ps
	Step response				100		ns
	Overvoltage recovery				100		ns

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input [+IN – (–IN)] of 4.096 V when +VA = 5 V.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, +VA = 4.5 V to 5.5 V, +VBD = 1.65 V to 5.5 V, V_{REF} = 5 V, and f_{SAMPLE} = 1 MHz, unless otherwise noted.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS								
THD	Total harmonic distortion[4]		V_{IN} = 5 V_{PP} at 10 kHz			–102		dB
			V_{IN} = 5 V_{PP} at 100 kHz			–95		
SNR	Signal-to-noise ratio		V_{IN} = 5 V_{PP} at 10 kHz			93		dB
			V_{IN} = 5 V_{PP} at 100 kHz	ADS8329/30IB	90	92		
				ADS8329/30I		90		
SINAD	Signal-to-noise + distortion		V_{IN} = 5 V_{PP} at 10 kHz			92		dB
			V_{IN} = 5 V_{PP} at 100 kHz			90		
SFDR	Spurious-free dynamic range		V_{IN} = 5 V_{PP} at 10 kHz			105		dB
			V_{IN} = 5 V_{PP} at 100 kHz			97		
	–3dB small-signal bandwidth					30		MHz
CLOCK								
	Internal conversion clock frequency				21	22.9	24.5	MHz
	SCLK external serial clock		Used as I/O clock only				50	MHz
			As I/O clock and conversion clock		1		42	
EXTERNAL VOLTAGE REFERENCE INPUT								
V_{REF}	Input reference range	V_{REF}[(REF+) – (REF–)]	5.5 V ≥ +VA ≥ 4.5 V		0.3		+VA	V
		(REF–) – AGND			–0.1		0.1	
	Resistance[5]		Reference input			40		kΩ
DIGITAL INPUT/OUTPUT								
	Logic family—CMOS							
V_{IH}	High-level input voltage		5.5 V ≥ +VBD ≥ 4.5 V		0.65 × (+VBD)		+VBD + 0.3	V
V_{IL}	Low-level input voltage		5.5 V ≥ +VBD ≥ 4.5 V		–0.3		0.35 × (+VBD)	V
I_I	Input current		V_I = +VBD or BDGND		–50		50	nA
C_I	Input capacitance					5		pF
V_{OH}	High-level output voltage		5.5 V ≥ +VBD ≥ 4.5 V, I_O = 100 µA		+VBD – 0.6		+VBD	V
V_{OL}	Low-level output voltage		5.5 V ≥ +VBD ≥ 4.5 V, I_O = 100 µA		0		0.4	V
C_O	Output capacitance					5		pF
C_L	Load capacitance						30	pF
	Data format—straight binary							
POWER-SUPPLY REQUIREMENTS								
	Power-supply voltage	+VBD			1.65	3.3	5.5	V
		+VA			4.5	5	5.5	V
	Supply current		1-MHz Sample rate			7.0	7.8	mA
			NAP/Auto-NAP mode			0.3	0.5	
			Deep power-down mode			4	50	nA
	Buffer I/O supply current		1 MSPS			1.7		mA
	Power dissipation		+VA = 5 V, +VBD = 5 V			44	48	mW
			+VA = 5 V, +VBD = 1.8 V			35	39.5	
TEMPERATURE RANGE								
T_A	Operating free-air temperature				–40		+85	°C

(4) Calculated on the first nine harmonics of the input frequency.
(5) Can vary ±30%.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, +VA = 2.7 V to 3.6 V, +VBD = 1.65 V to 1.5×(+VA), V_{REF} = 2.5 V, f_{SAMPLE} = 1 MHz for 3 V ≤ +VA ≤ 3.6 V, f_{SAMPLE} = 900 kHz for 3 V < +VA ≤ 2.7 V using external clock (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT							
	Full-scale input voltage(1)		+IN – (–IN) or (+INx – COM)	0		$+V_{REF}$	V
	Absolute input voltage		+IN, +IN0, +IN1	AGND – 0.2		+VA + 0.2	V
			–IN or COM	AGND – 0.2		AGND + 0.2	
	Input capacitance				40	45	pF
	Input leakage current		No ongoing conversion, DC Input	–1		1	nA
	Input channel isolation, ADS8330 only		At dc		108		dB
			V_I = ±1.25 V_{PP} at 50 kHz		101		
SYSTEM PERFORMANCE							
	Resolution				16		Bits
	No missing codes			16			Bits
INL	Integral linearity	ADS8329IB, ADS8330IB		–1.75	±1	1.75	LSB(2)
		ADS8329I, ADS8330I		–2.5	±1.5	2.5	
DNL	Differential linearity	ADS8329IB, ADS8330IB		–1	±0.5	1	LSB(2)
		ADS8329I, ADS8330I		–1	±0.8	2	
E_O	Offset error(3)	ADS8329IB, ADS8330IB		–0.5	±0.05	0.5	mV
		ADS8329I, ADS8330I		–0.8	±0.2	0.8	
	Offset error drift		FSR = 2.5 V		+0.8		ppm/°C
E_G	Gain error			–0.25	–0.04	0.25	%FSR
	Gain error drift				+0.5		ppm/°C
CMRR	Common-mode rejection ratio		At dc		70		dB
			V_I = 0.4 V_{PP} at 1 MHz		50		
	Noise				33		µV RMS
PSRR	Power-supply rejection ratio		At FFFFh output code(3)		78		dB
SAMPLING DYNAMICS							
t_{CONV}	Conversion time				18		CCLK
$t_{SAMPLE1}$	Acquisition time		Manual trigger	3			CCLK
$t_{SAMPLE2}$			Auto trigger		3		
	Throughput rate					1	MHz
	Aperture delay				5		ns
	Aperture jitter				10		ps
	Step response				100		ns
	Overvoltage recovery				100		ns

(1) Ideal input span, does not include gain or offset error.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input [+IN – (–IN)] of 2.5 V when +VA = 3 V.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, +VA = 2.7 V to 3.6 V, +VBD = 1.65 V to 1.5×(+VA), V_{REF} = 2.5 V, f_{SAMPLE} = 1 MHz for 3 V ≤ +VA ≤ 3.6 V, f_{SAMPLE} = 900 kHz for 3 V < +VA ≤ 2.7 V using external clock (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
THD	Total harmonic distortion(4)		V_{IN} = 2.5 V_{PP} at 10 kHz		–102		dB
			V_{IN} = 2.5 V_{PP} at 100 kHz		–93		
SNR	Signal-to-noise ratio		V_{IN} = 2.5 V_{PP} at 10 kHz		89		dB
			V_{IN} = 2.5 V_{PP} at 100 kHz		88		
SINAD	Signal-to-noise + distortion		V_{IN} = 2.5 V_{PP} at 10 kHz		88.5		dB
			V_{IN} = 2.5 V_{PP} at 100 kHz		88		
SFDR	Spurious-free dynamic range		V_{IN} = 2.5 V_{PP} at 10 kHz		104		dB
			V_{IN} = 2.5 V_{PP} at 100 kHz		94.2		
	–3dB small-signal bandwidth				30		MHz
CLOCK							
	Internal conversion clock frequency			21	22.3	23.5	MHz
	SCLK external serial clock		Used as I/O clock only			42	MHz
			As I/O clock and conversion clock	1		42	
EXTERNAL VOLTAGE REFERENCE INPUT							
V_{REF}	Input reference range	V_{REF}[(REF+) – (REF–)]	f_{SAMPLE} ≤ 500kSPS, 2.7 V ≤ +VA < 3V	0.3		2.525	V
			f_{SAMPLE} ≤ 500kSPS, 3 V ≤ +VA < 3.6V	0.3		3	
			f_{SAMPLE} > 500kSPS, 2.7 V ≤ +VA < 3V	2.475		2.525	
			f_{SAMPLE} > 500kSPS, 3 V ≤ +VA ≤ 3.6V	2.475		3	
		(REF–) – AGND		–0.1		0.1	
	Resistance(5)		Reference input		40		kΩ
DIGITAL INPUT/OUTPUT							
	Logic family—CMOS						
V_{IH}	High-level input voltage		(+VA × 1.5) V ≥ +VBD ≥ 1.65 V	0.65 × (+VBD)		+VBD + 0.3	V
V_{IL}	Low-level input voltage		(+VA × 1.5) V ≥ +VBD ≥ 1.65 V	–0.3		0.35 × (+VBD)	V
I_I	Input current		V_I = +VBD or BDGND	–50		50	nA
C_I	Input capacitance				5		pF
V_{OH}	High-level output voltage		(+VA × 1.5) V ≥ +VBD ≥ 1.65 V, I_O = 100 µA	+VBD – 0.6		+VBD	V
V_{OL}	Low-level output voltage		(+VA × 1.5) V ≥ +VBD ≥ 1.65 V, I_O = 100 µA	0		0.4	V
C_O	Output capacitance				5		pF
C_L	Load capacitance					30	pF
	Data format—straight binary						

(4) Calculated on the first nine harmonics of the input frequency.
(5) Can vary ±30%.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, +VA = 2.7 V to 3.6 V, +VBD = 1.65 V to 1.5×(+VA), V_{REF} = 2.5 V, f_{SAMPLE} = 1 MHz for 3 V ≤ +VA ≤ 3.6 V, f_{SAMPLE} = 900 kHz for 3 V < +VA ≤ 2.7 V using external clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY REQUIREMENTS						
Power-supply voltage	+VBD		1.65	+VA	1.5 × (+VA)	V
	+VA	f_s ≤ 1 MHz	3		3.6	V
		f_s ≤ 900 kHz	2.7		3.6	
Supply current		1-MHz sample rate, 3 V ≤ +VA ≤ 3.6 V		5.1	6.1	mA
		900-kHz sample rate, 2.7 V ≤ +VA ≤ 3 V		4.84		
		NAP/Auto-NAP mode		0.25	0.4	
		Deep power-down mode		2	50	nA
Buffer I/O supply current		1 MSPS, +VBD = 1.8 V		0.05		mA
Power dissipation		+VBD = 1.8 V, 3 V ≤ +VA ≤ 3.6 V		15.5	19	mW
		+VBD = 1.8 V, 2.7 V ≤ +VA ≤ 3 V		13.2		
TEMPERATURE RANGE						
T_A	Operating free-air temperature		–40		+85	°C

TIMING CHARACTERISTICS

All specifications typical at –40°C to 85°C and +VA = +VBD = 5 V. (1)(2)

PARAMETER			MIN	TYP	MAX	UNIT
f_{CCLK}	Frequency, conversion clock, CCLK	External, f_{CCLK} = 1/2 f_{SCLK}	0.5		21	MHz
		Internal, f_{CCLK} = 1/2 f_{SCLK}	21	22.9	24.5	MHz
$t_{su(CSF-EOC)}$	Setup time, falling edge of $\overline{CS}$ to EOC		1			CCLK
$t_{h(CSF-EOC)}$	Hold time, falling edge of $\overline{CS}$ to EOC		0			ns
$t_{wL(CONVST)}$	Pulse duration, $\overline{CONVST}$ low		40			ns
$t_{su(CSF-EOS)}$	Setup time, falling edge of $\overline{CS}$ to EOS		20			ns
$t_{h(CSF-EOS)}$	Hold time, falling edge of $\overline{CS}$ to EOS		20			ns
$t_{su(CSR-EOS)}$	Setup time, rising edge of $\overline{CS}$ to EOS		20			ns
$t_{h(CSR-EOS)}$	Hold time, rising edge of $\overline{CS}$ to EOS		20			ns
$t_{su(CSF-SCLK1F)}$	Setup time, falling edge of $\overline{CS}$ to first falling SCLK		5			ns
$t_{wL(SCLK)}$	Pulse duration, SCLK low		8		$t_{c(SCLK)} – 8$	ns
$t_{wH(SCLK)}$	Pulse duration, SCLK high		8		$t_{c(SCLK)} – 8$	ns
$t_{c(SCLK)}$	Cycle time, SCLK	I/O Clock only	20			ns
		I/O and conversion clock	23.8		2000	ns
		I/O Clock, chain mode	20			ns
		I/O and conversion clock, chain mode	23.8		2000	ns
$t_{d(SCLKF-SDOINVALID)}$	Delay time, falling edge of SCLK to SDO invalid	10-pF Load	2			ns
$t_{d(SCLKF-SDOVALID)}$	Delay time, falling edge of SCLK to SDO valid	10-pF Load			10	ns
$t_{d(CSF-SDOVALID)}$	Delay time, falling edge of $\overline{CS}$ to SDO valid, SDO MSB output	10-pF Load			8.5	ns
$t_{su(SDI-SCLKF)}$	Setup time, SDI to falling edge of SCLK		8			ns
$t_{h(SDI-SCLKF)}$	Hold time, SDI to falling edge of SCLK		4			ns
$t_{d(CSR-SDOZ)}$	Delay time, rising edge of $\overline{CS}$/FS to SDO 3-state				5	ns
$t_{su(16th\ SCLKF-CSR)}$	Setup time, 16th falling edge of SCLK before rising edge of $\overline{CS}$/FS		10			ns
$t_{d(SDO-CDI)}$	Delay time, CDI high to SDO high in daisy chain mode	10-pF Load, chain mode			16	ns

(1) All input signals are specified with $t_r = t_f$ = 1.5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagrams.

TIMING CHARACTERISTICS

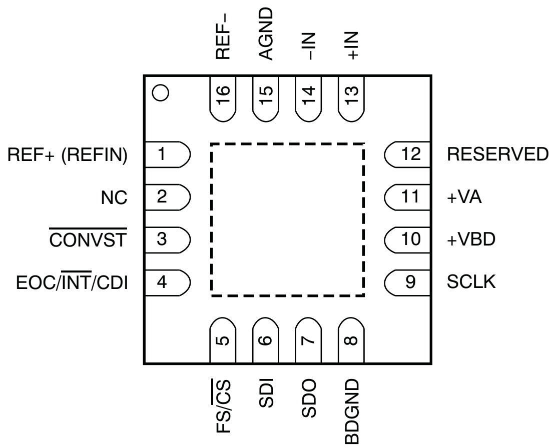
All specifications typical at –40°C to 85°C, +VA = 2.7 V, +VBD = 1.8 V (unless otherwise noted) (1) (2)

PARAMETER			MIN	TYP	MAX	UNIT
f_{CCLK}	Frequency, conversion clock, CCLK	External, 3 V ≤ +VA ≤ 3.6 V, f_{CCLK} = 1/2 f_{SCLK}	0.5		21	MHz
		External, 2.7 V ≤ +VA ≤ 3 V, f_{CCLK} = 1/2 f_{SCLK}	0.5		18.9	
		Internal, f_{CCLK} = 1/2 f_{SCLK}	20	22.3	23.5	
$t_{su(CSF-EOC)}$	Setup time, falling edge of $\overline{CS}$ to EOC		1			CCLK
$t_{h(CSF-EOC)}$	Hold time, falling edge of $\overline{CS}$ to EOC		0			ns
$t_{wL(CONVST)}$	Pulse duration, $\overline{CONVST}$ low		40			ns
$t_{su(CSF-EOS)}$	Setup time, falling edge of $\overline{CS}$ to EOS		20			ns
$t_{h(CSF-EOS)}$	Hold time, falling edge of $\overline{CS}$ to EOS		20			ns
$t_{su(CSR-EOS)}$	Setup time, rising edge of $\overline{CS}$ to EOS		20			ns
$t_{h(CSR-EOS)}$	Hold time, rising edge of $\overline{CS}$ to EOS		20			ns
$t_{su(CSF-SCLK1F)}$	Setup time, falling edge of $\overline{CS}$ to first falling SCLK		5			ns
$t_{wL(SCLK)}$	Pulse duration, SCLK low		8		$t_{c(SCLK)}$ – 8	ns
$t_{wH(SCLK)}$	Pulse duration, SCLK high		8		$t_{c(SCLK)}$ – 8	ns
$t_{c(SCLK)}$	Cycle time, SCLK	All modes, 3 V ≤ +VA ≤ 3.6 V	23.8		2000	ns
		All modes, 2.7 V ≤ +VA < 3 V	26.5		2000	
$t_{d(SCLKF-SDOINVALID)}$	Delay time, falling edge of SCLK to SDO invalid	10-pF Load	7.5			ns
$t_{d(SCLKF-SDOVALID)}$	Delay time, falling edge of SCLK to SDO valid	10-pF Load			16	ns
$t_{d(CSF-SDOVALID)}$	Delay time, falling edge of $\overline{CS}$ to SDO valid, SDO MSB output	10-pF Load, 2.7 V ≤ +VA ≤ 3 V			13	ns
		10-pF Load, 3 V ≤ +VA ≤ 3.6 V			11	
$t_{su(SDI-SCLKF)}$	Setup time, SDI to falling edge of SCLK		8			ns
$t_{h(SDI-SCLKF)}$	Hold time, SDI to falling edge of SCLK		4			ns
$t_{d(CSR-SDOZ)}$	Delay time, rising edge of $\overline{CS}$/FS to SDO 3-state				8	ns
$t_{su(16th\ SCLKF-CSR)}$	Setup time, 16th falling edge of SCLK before rising edge of $\overline{CS}$/FS		10			ns
$t_{d(SDO-CDI)}$	Delay time, CDI high to SDO high in daisy chain mode	10-pF Load, chain mode			23	ns

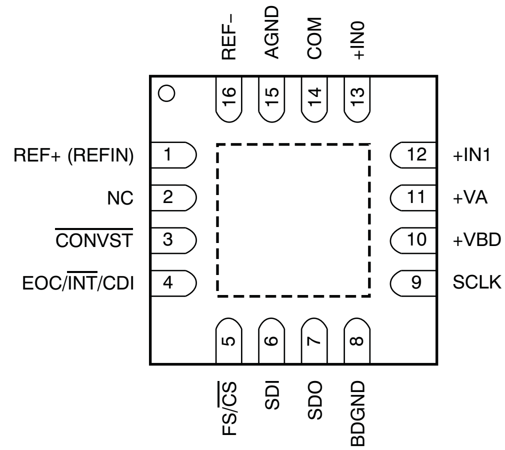
(1) All input signals are specified with t_r = t_f = 1.5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) See timing diagrams.

PIN ASSIGNMENTS

ADS8329
RSA PACKAGE
(TOP VIEW)

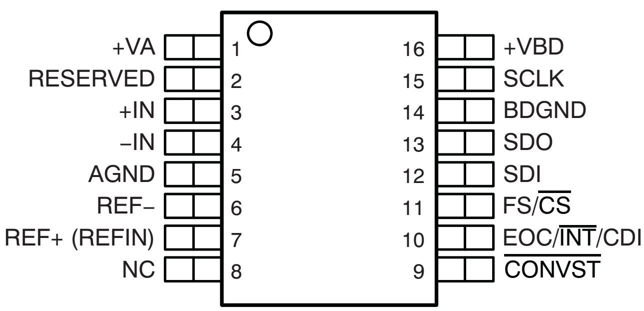


ADS8330
RSA PACKAGE
(TOP VIEW)



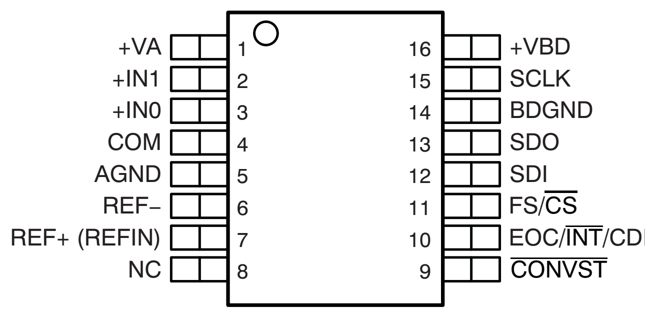
CAUTION: The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

ADS8329
PW PACKAGE
(TOP VIEW)



NC = No internal connection

ADS8330
PW PACKAGE
(TOP VIEW)



ADS8329 Terminal Functions

NAME	NO. QFN	NO. TSSOP	I/O	DESCRIPTION
AGND	15	5	—	Analog ground
BDGND	8	14	—	Interface ground
$\overline{\text{CONVST}}$	3	9	I	Freezes sample and hold, starts conversion with next rising edge of internal clock
EOC/ $\overline{\text{INT}}$/ CDI	4	10	O	Status output. If programmed as EOC, this pin is low (default) when a conversion is in progress. If programmed as an interrupt ($\overline{\text{INT}}$), this pin is low for a preprogrammed duration after the end of conversion and valid data are to be output. The polarity of EOC or $\overline{\text{INT}}$ is programmable. This pin can also be used as a chain data input when the device is operated in chain mode.
FS/$\overline{\text{CS}}$	5	11	I	Frame sync signal for TMS320 DSP serial interface or chip select input for SPI interface slave select (SS–).
+IN	13	3	I	Noninverting input
–IN	14	4	I	Inverting input, usually connected to ground
NC	2	8	—	No connection.
REF+	1	7	I	External reference input.
REF–	16	6	I	Connect to AGND through individual via.
RESERVED	12	2	I	Connect to AGND or +VA
SCLK	9	15	I	Clock for serial interface
SDI	6	12	I	Serial data in
SDO	7	13	O	Serial data out
+VA	11	1		Analog supply, +2.7 V to +5.5 VDC.
+VBD	10	16		Interface supply

ADS8330 Terminal Functions

NAME	NO. QFN	NO. TSSOP	I/O	DESCRIPTION
AGND	15	5	—	Analog ground
BDGND	8	14	—	Interface ground
COM	14	4	I	Common inverting input, usually connected to ground
$\overline{\text{CONVST}}$	3	9	I	Freezes sample and hold, starts conversion with next rising edge of internal clock
EOC/ $\overline{\text{INT}}$/ CDI	4	10	O	Status output. If programmed as EOC, this pin is low (default) when a conversion is in progress. If programmed as an interrupt ($\overline{\text{INT}}$), this pin is low for a preprogrammed duration after the end of conversion and valid data are to be output. The polarity of EOC or $\overline{\text{INT}}$ is programmable. This pin can also be used as a chain data input when the device is operated in chain mode.
FS/$\overline{\text{CS}}$	5	11	I	Frame sync signal for TMS320 DSP serial interface or chip select input for SPI interface
+IN1	12	2	I	Second noninverting input.
+IN0	13	3	I	First noninverting input
NC	2	8	—	No connection.
REF+	1	7	I	External reference input.
REF–	16	6	I	Connect to AGND through individual via.
SCLK	9	15	I	Clock for serial interface
SDI	6	12	I	Serial data in (conversion start and reset possible)
SDO	7	13	O	Serial data out
+VA	11	1		Analog supply, +2.7 V to +5.5 VDC.
+VBD	10	16		Interface supply

MANUAL TRIGGER / READ While Sampling
(use internal CCLK, EOC and $\overline{INT}$ polarity programmed as active low)

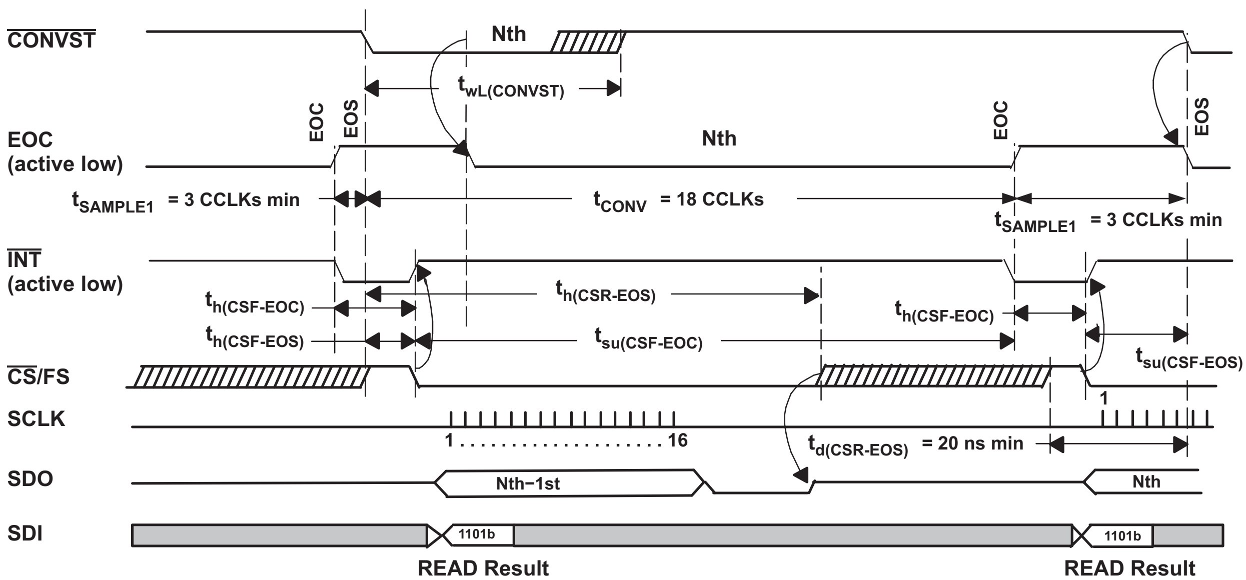


Figure 1. Timing for Conversion and Acquisition Cycles for Manual Trigger (Read while sampling)

AUTO TRIGGER / READ While Sampling
(use internal CCLK, EOC and $\overline{INT}$ polarity programmed as active low)

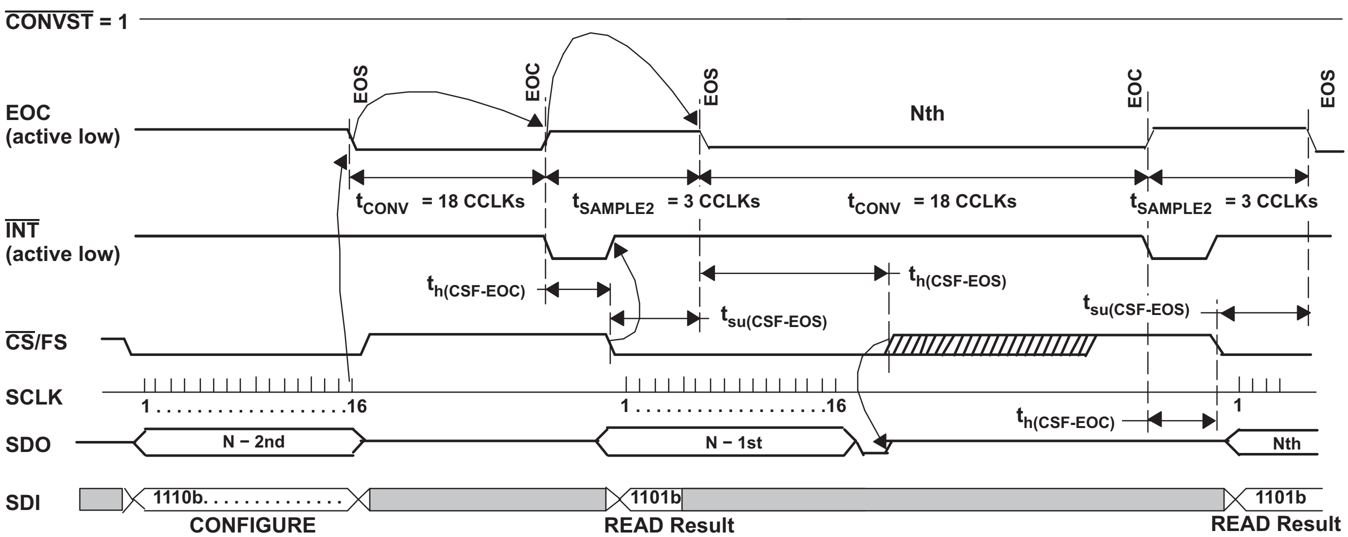


Figure 2. Timing for Conversion and Acquisition Cycles for Autotrigger (Read while sampling)

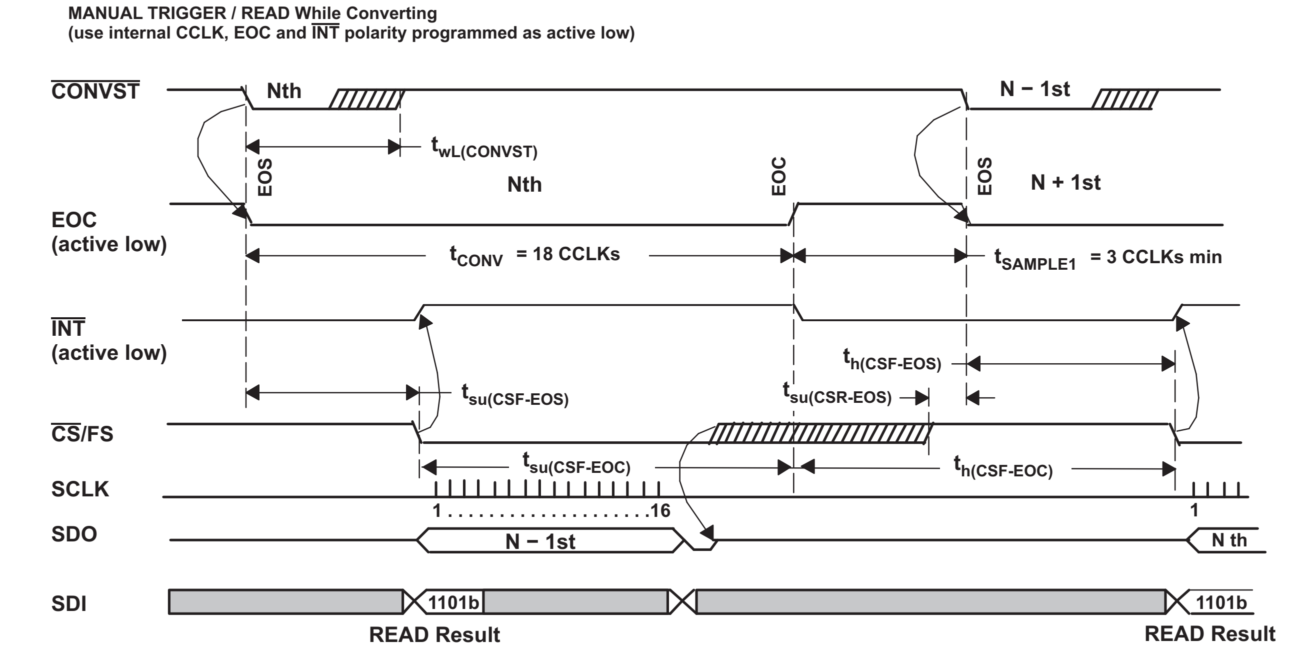


Figure 3. Timing for Conversion and Acquisition Cycles for Manual Trigger (Read while converting)

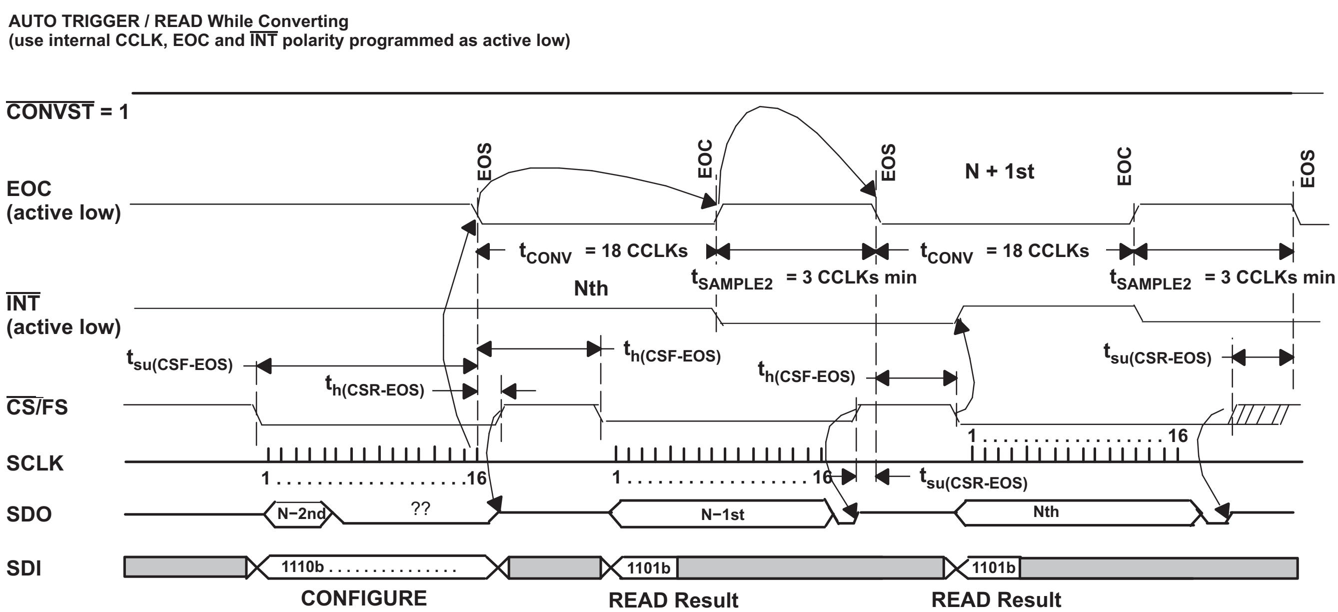


Figure 4. Timing for Conversion and Acquisition Cycles for Autotrigger (Read while converting)

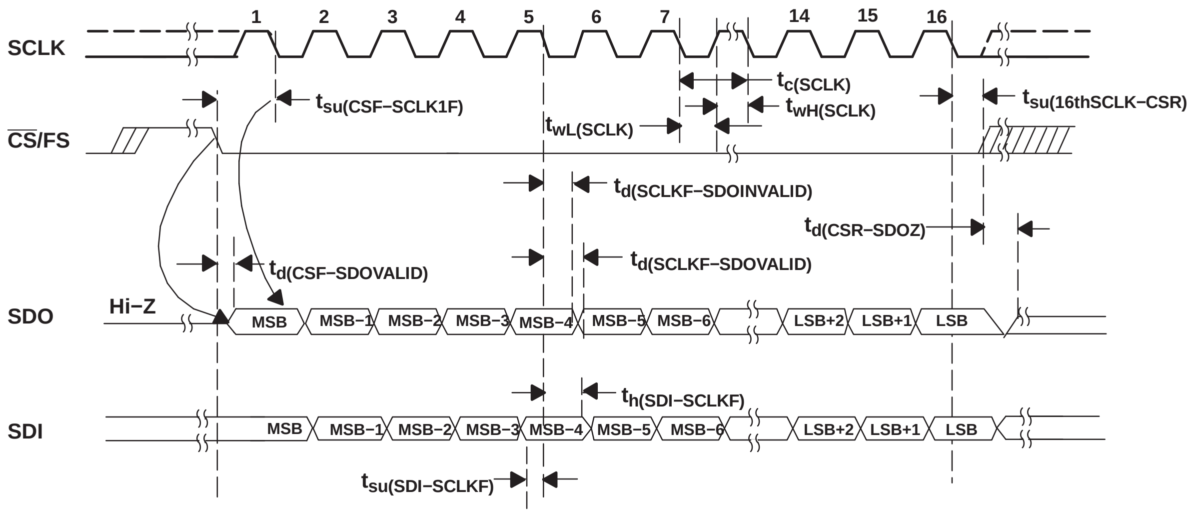


Figure 5. Detailed SPI Transfer Timing

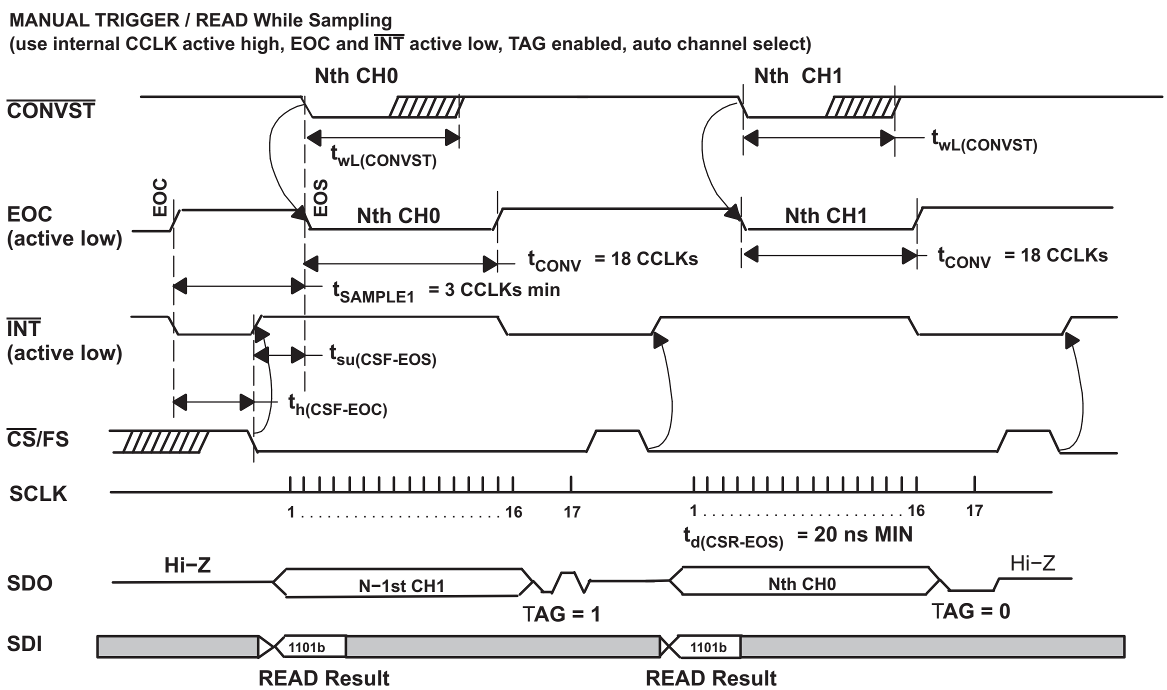


Figure 6. Simplified Dual Channel Timing

TYPICAL CHARACTERISTICS

At –40°C to 85°C, V_{REF} [REF+ – (REF–)] = 5 V when +VA = +VBD = 5 V or V_{REF} [REF+ – (REF–)] = 2.5 V when +VA = +VBD = 3 V, f_{SCLK} = 42 MHz, or V_{REF} = 2.5 when +VA = +VBD = 2.7 V, f_{SCLK} = 37.8 MHz, f_I = dc for dc curves, f_I = 100 kHz for ac curves with 5-V supply and f_I = 10 kHz for ac curves with 3-V supply (unless otherwise noted).

CROSSTALK vs FREQUENCY

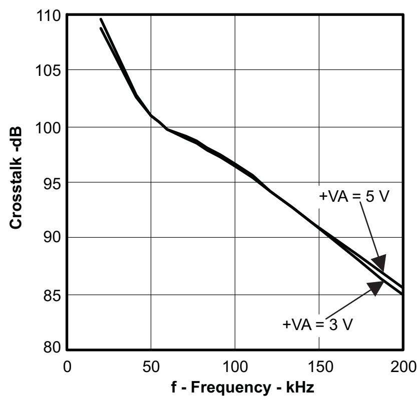


Figure 7.

DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE

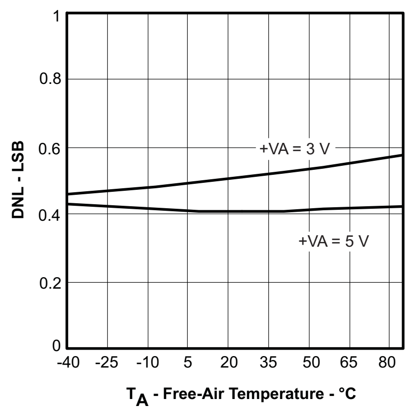


Figure 8.

INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE

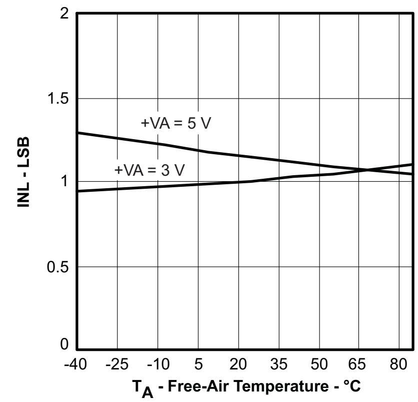


Figure 9.

DIFFERENTIAL NONLINEARITY vs EXTERNAL CLOCK FREQUENCY

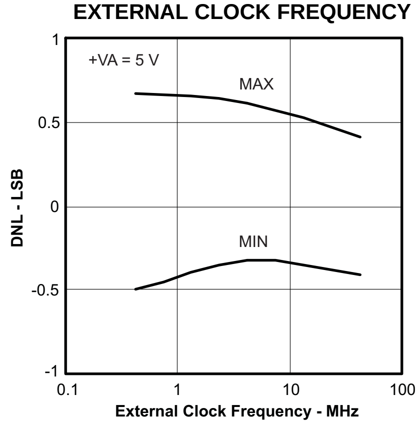


Figure 10.

INTEGRAL NONLINEARITY vs EXTERNAL CLOCK FREQUENCY

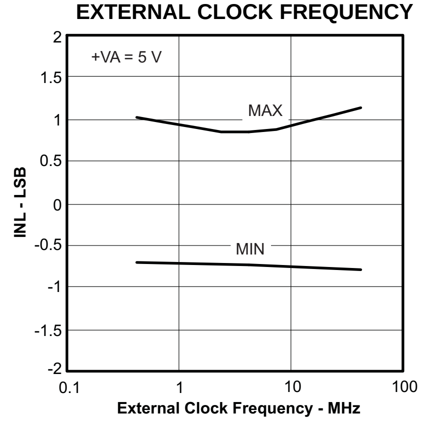


Figure 11.

DIFFERENTIAL NONLINEARITY vs EXTERNAL CLOCK FREQUENCY

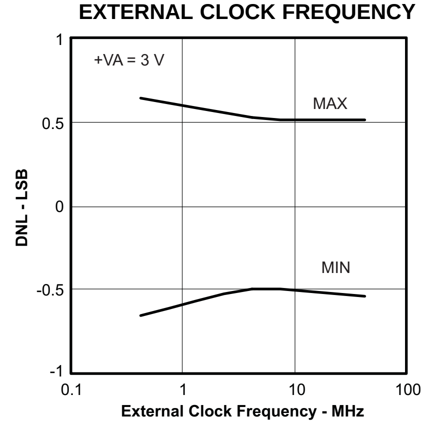


Figure 12.

TYPICAL CHARACTERISTICS (continued)

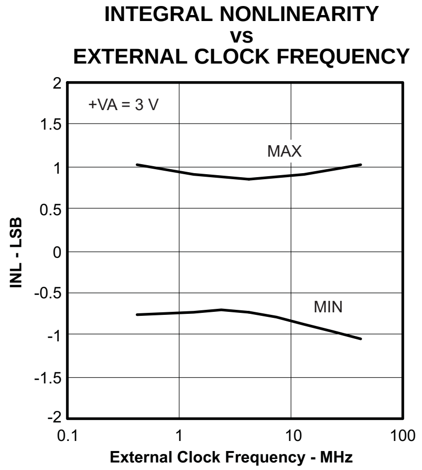


Figure 13.

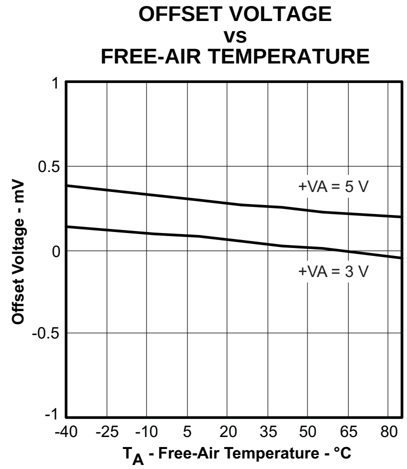


Figure 14.

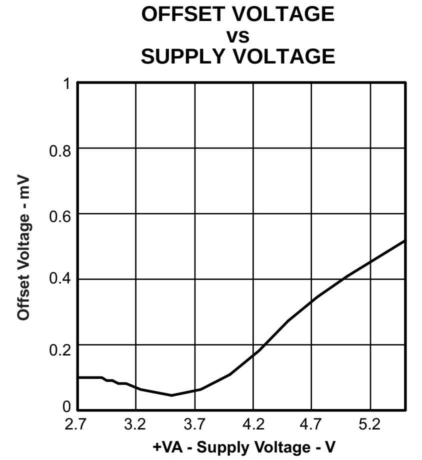


Figure 15.

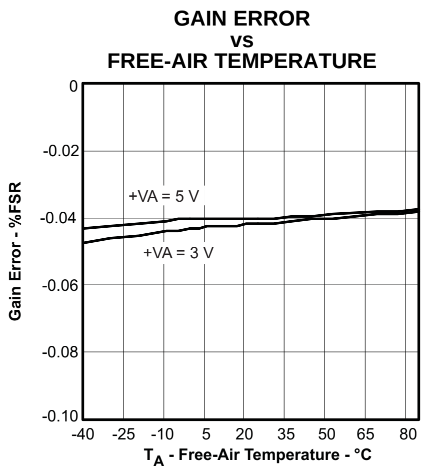


Figure 16.

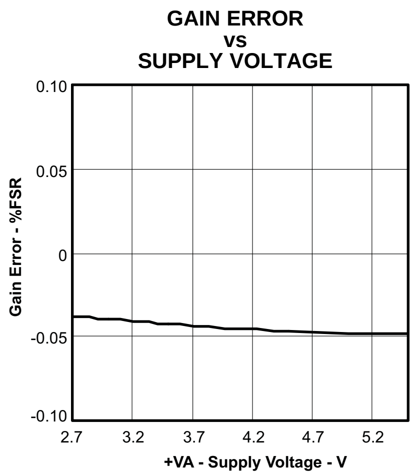


Figure 17.

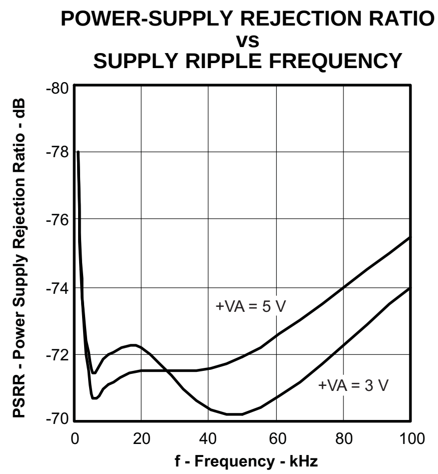


Figure 18.

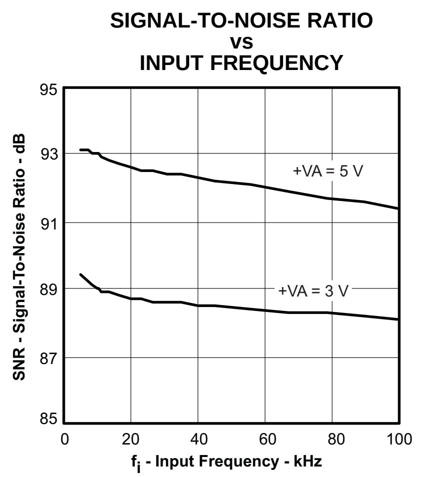


Figure 19.

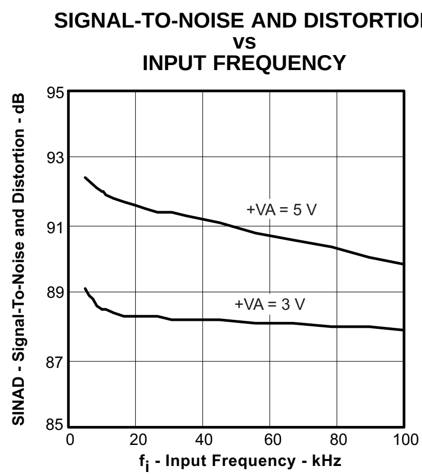


Figure 20.

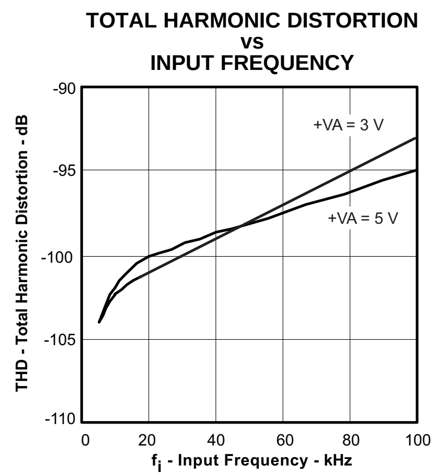


Figure 21.

TYPICAL CHARACTERISTICS (continued)

SPURIOUS-FREE DYNAMIC RANGE vs INPUT FREQUENCY

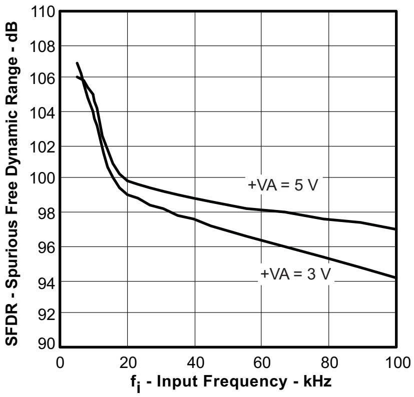


Figure 22.

SIGNAL-TO-NOISE RATIO vs FULL-SCALE RANGE

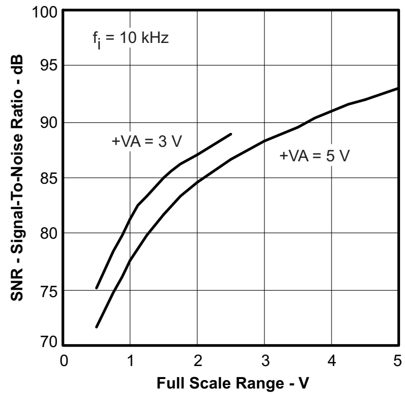


Figure 23.

SIGNAL-TO-NOISE AND DISTORTION vs FULL-SCALE RANGE

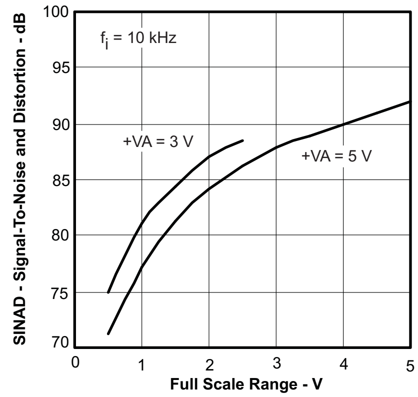


Figure 24.

TOTAL HARMONIC DISTORTION vs FULL-SCALE RANGE

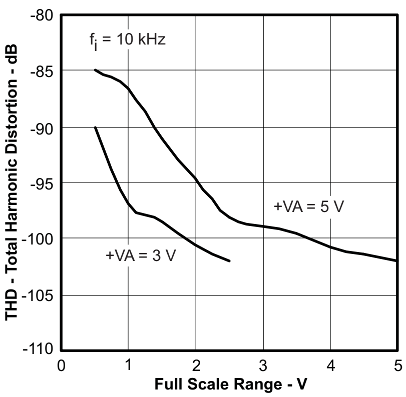


Figure 25.

SPURIOUS-FREE DYNAMIC RANGE vs FULL-SCALE RANGE

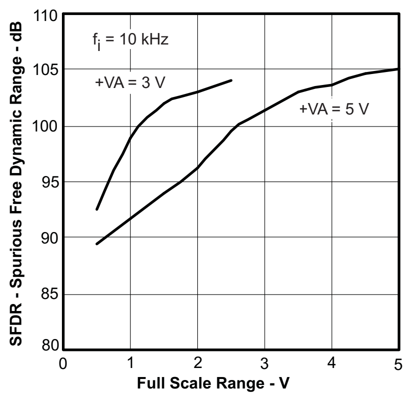


Figure 26.

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

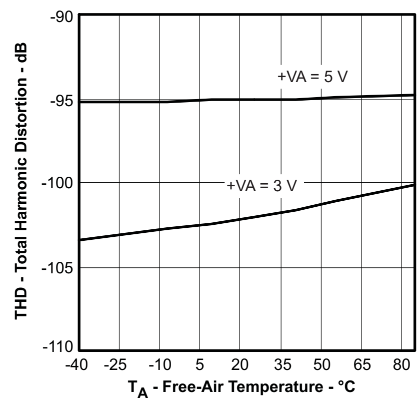


Figure 27.

SPURIOUS-FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

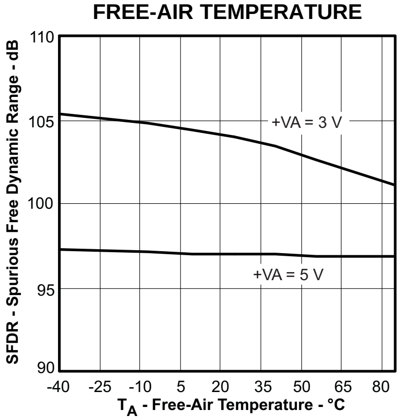


Figure 28.

SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE

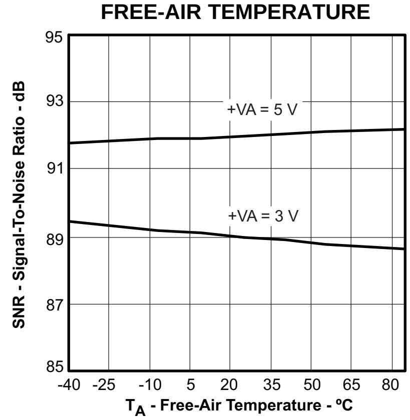


Figure 29.

SIGNAL-TO-NOISE AND DISTORTION vs FREE-AIR TEMPERATURE

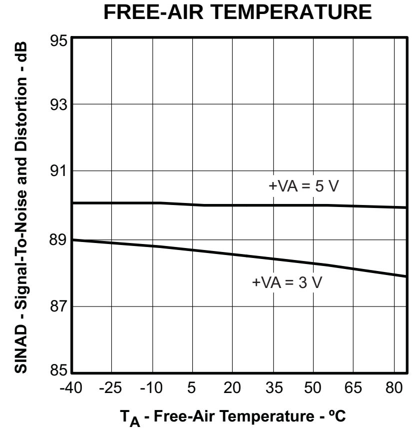


Figure 30.

TYPICAL CHARACTERISTICS (continued)

EFFECTIVE NUMBER OF BITS vs FREE-AIR TEMPERATURE

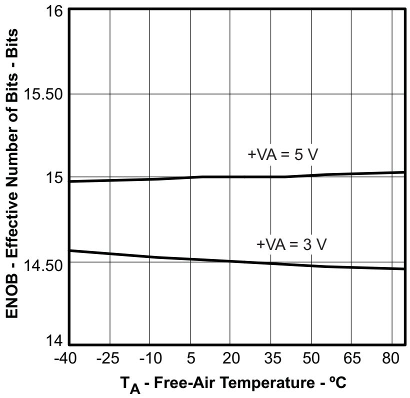


Figure 31.

INTERNAL CLOCK FREQUENCY vs SUPPLY VOLTAGE

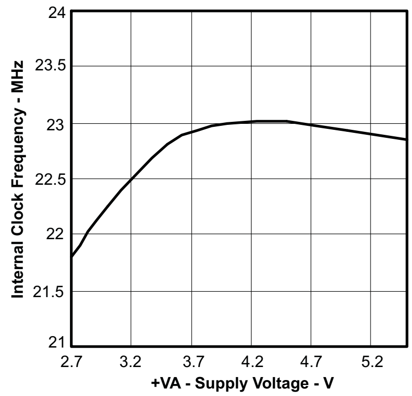


Figure 32.

INTERNAL CLOCK FREQUENCY vs FREE-AIR TEMPERATURE

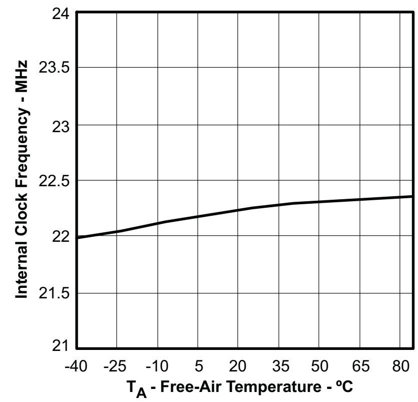


Figure 33.

ANALOG SUPPLY CURRENT vs SUPPLY VOLTAGE

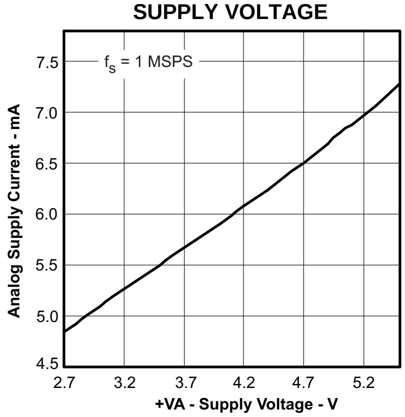


Figure 34.

ANALOG SUPPLY CURRENT vs SUPPLY VOLTAGE

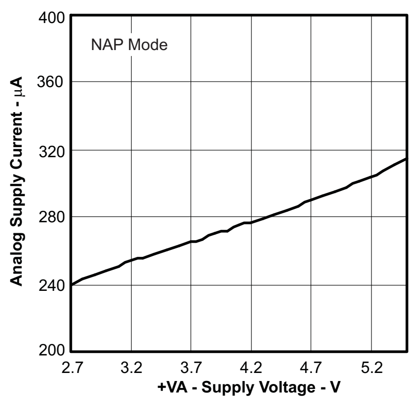


Figure 35.

ANALOG SUPPLY CURRENT vs SUPPLY VOLTAGE

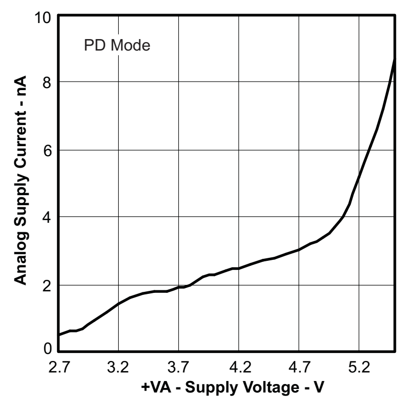


Figure 36.

ANALOG SUPPLY CURRENT vs SAMPLE RATE

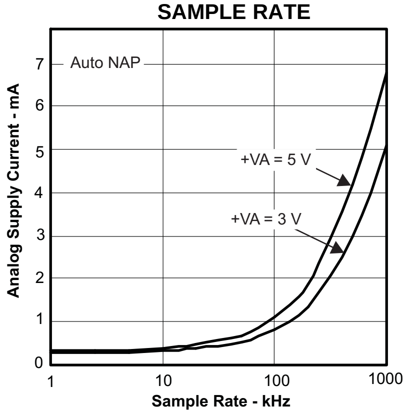


Figure 37.

ANALOG SUPPLY CURRENT vs SAMPLE RATE

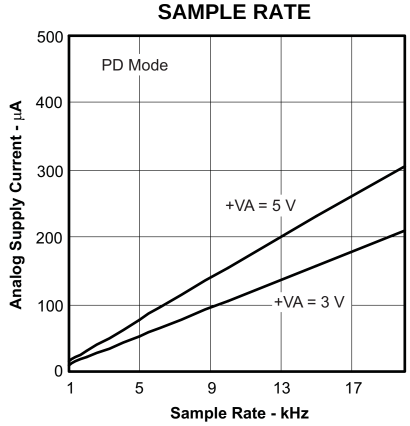


Figure 38.

ANALOG SUPPLY CURRENT vs FREE-AIR TEMPERATURE

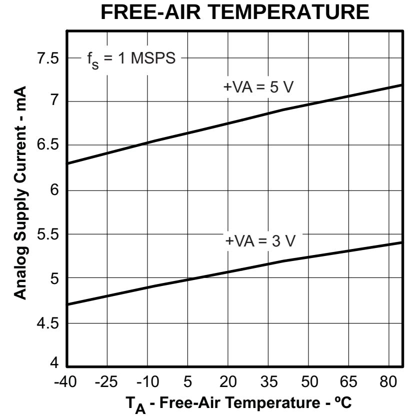


Figure 39.

TYPICAL CHARACTERISTICS (continued)

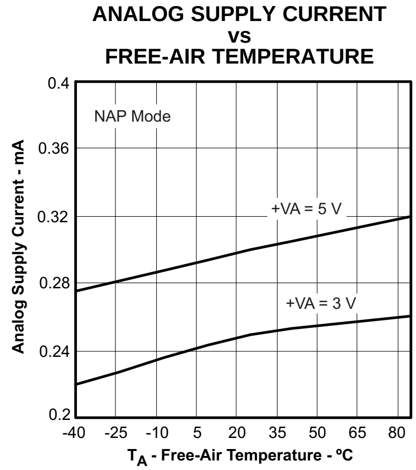


Figure 40.

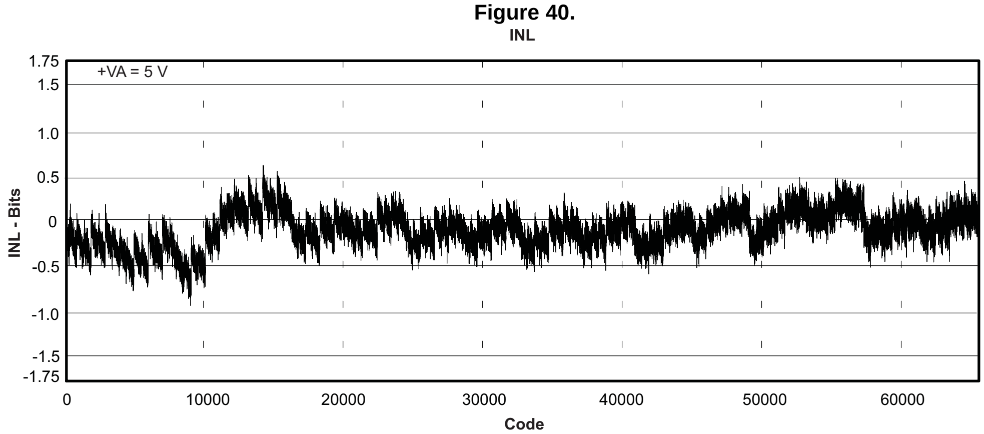


Figure 41.

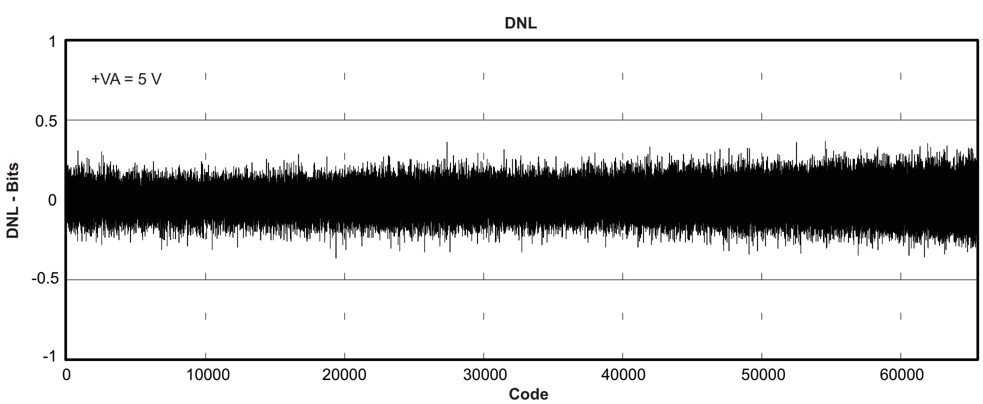


Figure 42.

TYPICAL CHARACTERISTICS (continued)

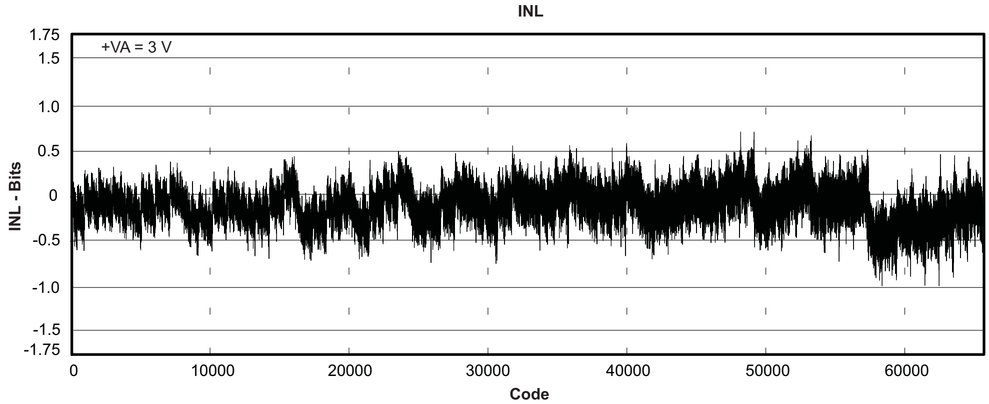


Figure 43.

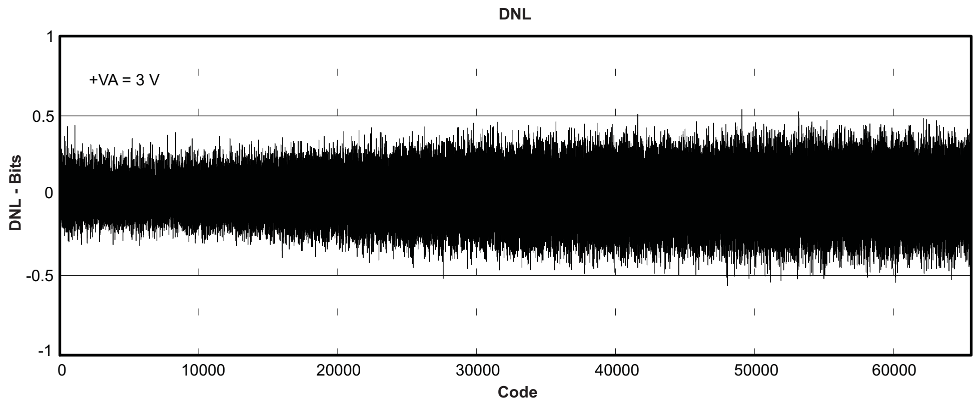


Figure 44.

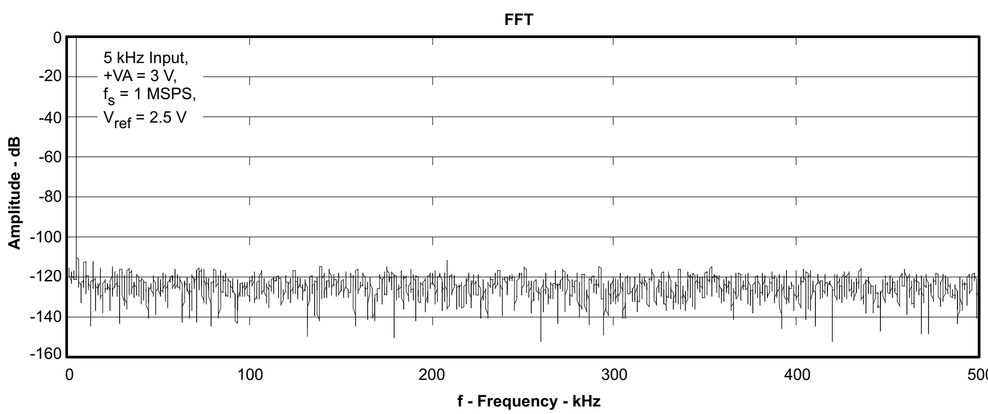


Figure 45.

TYPICAL CHARACTERISTICS (continued)

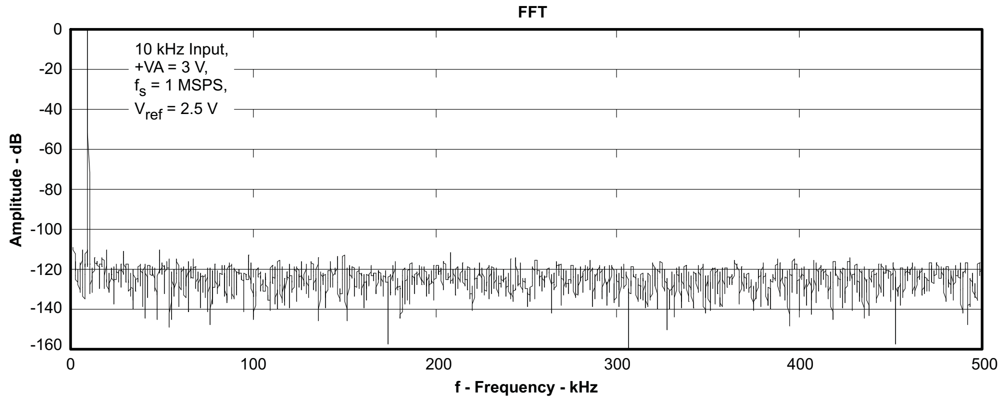


Figure 46.

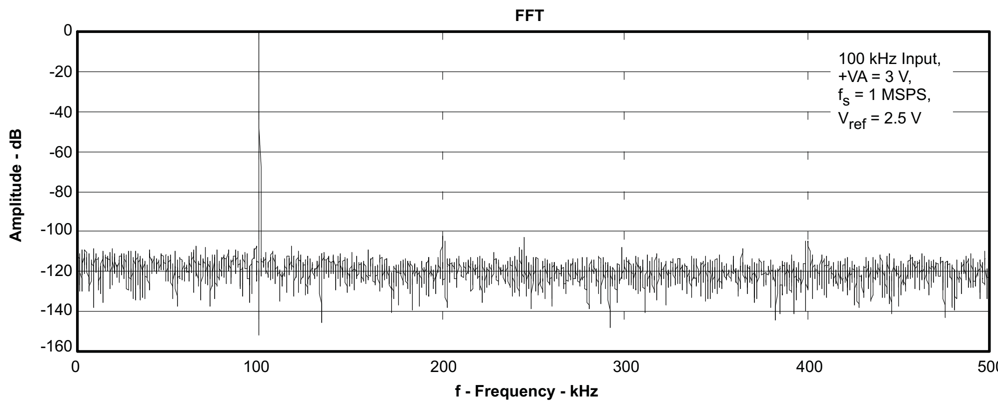


Figure 47.

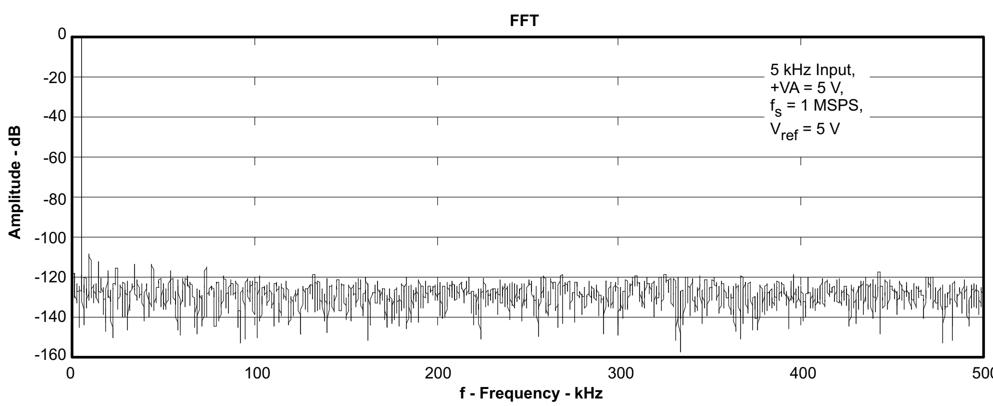


Figure 48.

TYPICAL CHARACTERISTICS (continued)

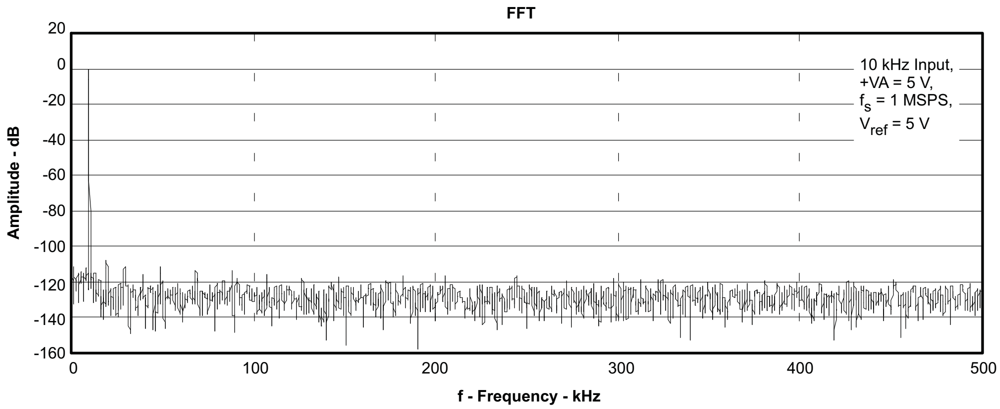


Figure 49.

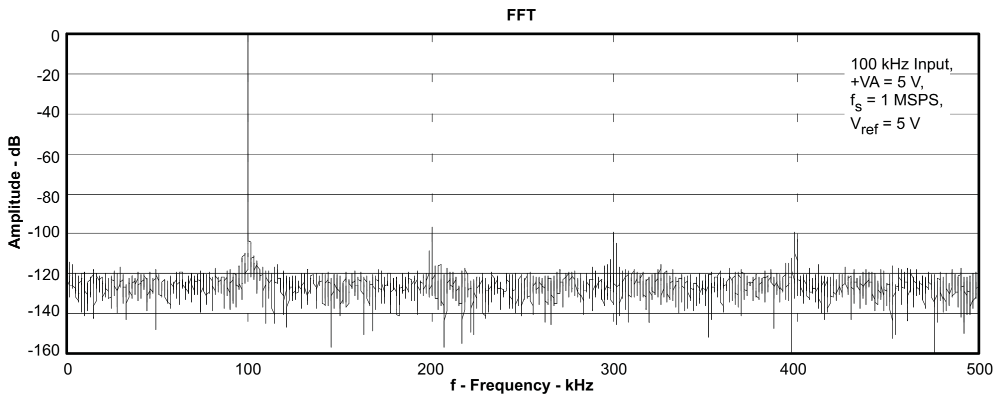


Figure 50.

THEORY OF OPERATION

The ADS8329/30 is a high-speed, low power, successive approximation register (SAR) analog-to-digital converter (ADC) that uses an external reference. The architecture is based on charge redistribution, which inherently includes a sample/hold function.

The ADS8329/30 has an internal clock that is used to run the conversion but can also be programmed to run the conversion based on the external serial clock, SCLK.

The ADS8329 has one analog input. The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both +IN and –IN inputs are disconnected from any internal function.

The ADS8330 has two inputs. Both inputs share the same common pin, COM. The negative input is the same as the –IN pin for the ADS8329. The ADS8330 can be programmed to select a channel manually or can be programmed into the auto channel select mode to sweep between channel 0 and 1 automatically.

ANALOG INPUT

When the converter enters hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The voltage on the –IN input is limited between AGND – 0.2 V and AGND + 0.2 V, allowing the input to reject small signals which are common to both the +IN and –IN inputs. The +IN input has a range of –0.2 V to V_{REF} + 0.2 V. The input span [+IN – (–IN)] is limited to 0 V to V_{REF}.

The (peak) input current through the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. The current into the ADS8329/30 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45 pF) to a 16-bit settling level within the minimum acquisition time (120 ns). When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain linearity of the converter, the +IN and –IN inputs and the span [+IN – (–IN)] should be within the limits specified. Outside of these ranges, converter linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used. Care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this is not observed, the two inputs could have different settling times. This may result in an offset error, gain error, and linearity error which change with temperature and input voltage.

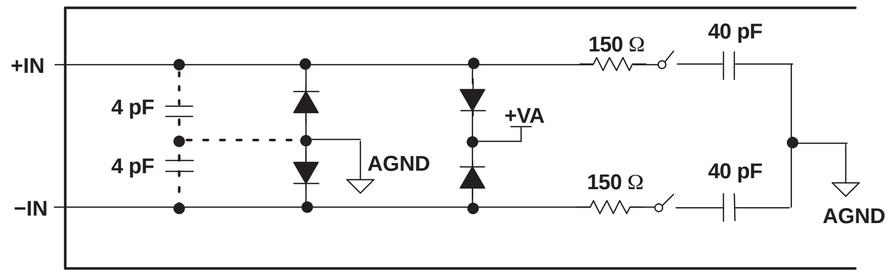


Figure 51. Input Equivalent Circuit

Driver Amplifier Choice

The analog input to the converter needs to be driven with a low noise, op-amp like the THS4031 or OPA365. An RC filter is recommended at the input pins to low-pass filter the noise from the source. Two resistors of 20 Ω and a capacitor of 470 pF are recommended. The input to the converter is a unipolar input voltage in the range 0 V to V_{REF}. The minimum –3dB bandwidth of the driving operational amplifier can be calculated to:

$$f_{3db} = (\ln(2) \times (n+1))/(2\pi \times t_{ACQ})$$

where *n* is equal to 16, the resolution of the ADC (in the case of the ADS8329/30). When t_{ACQ} = 120 ns (minimum acquisition time), the minimum bandwidth of the driving amplifier is 15.6 MHz. The bandwidth can be relaxed if the acquisition time is increased by the application. The OPA365, OPA827, or THS4031 from Texas Instruments are recommended. The THS4031 used in the source follower configuration to drive the converter is shown in the typical input drive configuration, Figure 52. For the ADS8330, a series resistor of 0Ω should be used on the COM pin (or no resistor at all).

Bipolar to Unipolar Driver

In systems where the input is bipolar, the THS4031 can be used in the inverting configuration with an additional DC bias applied to its + input so as to keep the input to the ADS8329/30 within its rated operating voltage range. This configuration is also recommended when the ADS8329/30 is used in signal processing applications where good SNR and THD performance is required. The DC bias can be derived from the REF3225 or the REF3240 reference voltage ICs. The input configuration shown in Figure 53 is capable of delivering better than 91 dB SNR and –96 dB THD at an input frequency of 10 kHz. In case bandpass filters are used to filter the input, care should be taken to ensure that the signal swing at the input of the bandpass filter is small so as to keep the distortion introduced by the filter minimal. In such cases, the gain of the circuit shown in Figure 53 can be increased to keep the input to the ADS8329/30 large to keep the SNR of the system high. Note that the gain of the system from the + input to the output of the THS4031 in such a configuration is a function of the gain of the AC signal. A resistor divider can be used to scale the output of the REF3225 or REF3240 to reduce the voltage at the DC input to THS4031 to keep the voltage at the input of the converter within its rated operating range.

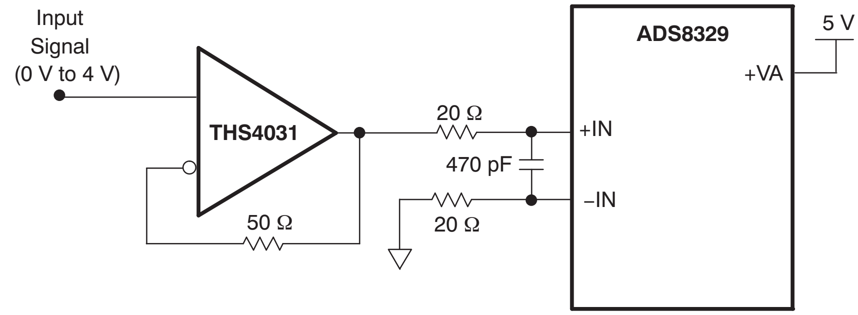


Figure 52. Unipolar Input Drive Configuration

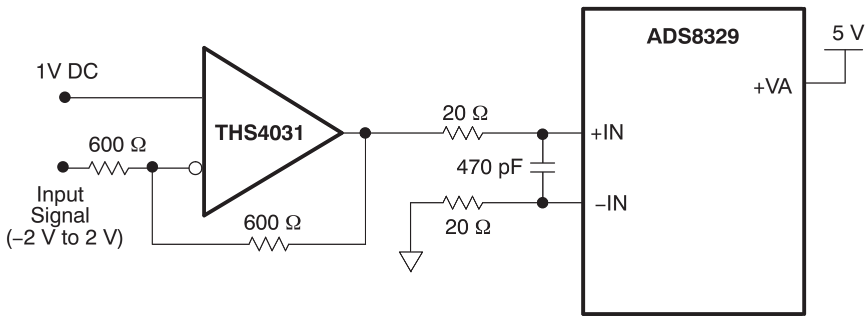


Figure 53. Bipolar Input Drive Configuration

REFERENCE

The ADS8329/30 can operate with an external reference with a range from 0.3 V to 5 V. A clean, low noise, well-decoupled reference voltage on this pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF3240 can be used to drive this pin. A 22-µF ceramic decoupling capacitor is required between the REF+ and REF– pins of the converter. These capacitors should be placed as close as possible to the pins of the device. The REF– should be connected to its own via to the analog ground plane with the shortest possible distance.

CONVERTER OPERATION

The ADS8329/30 has an oscillator that is used as an internal clock which controls the conversion rate. The frequency of this clock is 21 MHz minimum. The oscillator is always on unless the device is in the deep power-down state or the device is programmed for using SCLK as the conversion clock (CCLK). The minimum acquisition (sampling) time takes 3 CCLKs (this is equivalent to 120 ns at 24.5 MHz) and the conversion time takes 18 conversion clocks (CCLK) (≈780 ns) to complete one conversion.

The conversion can also be programmed to run based on the external serial clock, SCLK, if is so desired. This allows a system designer to achieve system synchronization. The serial clock SCLK, is first reduced to 1/2 of its frequency before it is used as the conversion clock (CCLK). For example, with a 42-MHz SCLK this provides a 21-MHz clock for conversions. If it is desired to start a conversion at a specific rising edge of the SCLK when the external SCLK is programmed as the source of the conversion clock (CCLK) (and manual start of conversion is selected), the setup time between $\overline{\text{CONVST}}$ and that rising SCLK edge should be observed. This ensures the conversion is complete in 18 CCLKs (or 36 SCLKs). The minimum setup time is 20 ns to ensure synchronization between $\overline{\text{CONVST}}$ and SCLK. In many cases the conversion can start one SCLK period (or CCLK) later which results in a 19 CCLK (or 37 SCLK) conversion. The 20 ns setup time is not required once synchronization is relaxed.

The duty cycle of SCLK is not critical as long as it meets the minimum high and low time requirements of 8 ns. Since the ADS8329/30 is designed for high-speed applications, a higher serial clock (SCLK) must be supplied to be able to sustain the high throughput with the serial interface and so the clock period of SCLK must be at most 1 µs (when used as conversion clock (CCLK). The minimum clock frequency is also governed by the parasitic leakage of the capacitive digital-to-analog (CDAC) capacitors internal to the ADS8329/30.

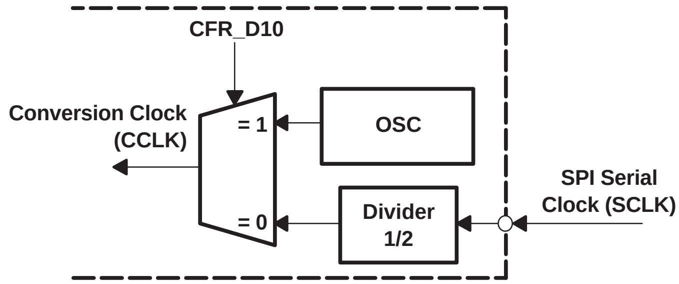


Figure 54. Converter Clock

Manual Channel Select Mode

The conversion cycle starts with selecting an acquisition channel by writing a channel number to the command register (CMR). This cycle time can be as short as 4 serial clocks (SCLK).

Auto Channel Select Mode

Channel selection can also be done automatically if auto channel select mode is enabled. This is the default channel select mode. The dual channel converter, ADS8330, has a built-in 2-to-1 MUX. If the device is programmed for auto channel select mode then signals from channel 0 and channel 1 are acquired with a fixed order. Channel 0 is accessed first in the next cycle after the command cycle that configured CFR_D11 to 1 for auto channel select mode. This automatic access stops the cycle after the command cycle that sets CFR_D11 to 0.

Start of a Conversion

The end of acquisition or sampling instance (EOS) is the same as the start of a conversion. This is initiated by bringing the CONVST pin low for a minimum of 40 ns. After the minimum requirement has been met, the CONVST pin can be brought high. CONVST acts independent of FS/CS so it is possible to use one common CONVST for applications requiring simultaneous sample/hold with multiple converters. The ADS8329/30 switches from sample to hold mode on the falling edge of the CONVST signal. The ADS8329/30 requires 18 conversion clock (CCLK) edges to complete a conversion. The conversion time is equivalent to 1500 ns with a 12-MHz internal clock. The minimum time between two consecutive CONVST signals is 21 CCLKs.

A conversion can also be initiated without using CONVST if it is so programmed (CFR_D9 = 0). When the converter is configured as auto trigger, the next conversion is automatically started 3 conversion clocks (CCLK) after the end of a conversion. These 3 conversion clocks (CCLK) are used as the acquisition time. In this case the time to complete one acquisition and conversion cycle is 21 CCLKs.

Table 1. Different Types of Conversion

MODE	SELECT CHANNEL	START CONVERSION
Automatic	**Auto Channel Select(1)**	**Auto Trigger**
	No need to write channel number to the CMR. Use internal sequencer for the ADS8330.	Start a conversion based on the conversion clock CCLK.
Manual	**Manual Channel Select**	**Manual Trigger**
	Write the channel number to the CMR.	Start a conversion with CONVST.

(1) Auto channel select should be used with auto trigger and also with the TAG bit enabled.

Status Output EOC/$\overline{\text{INT}}$

When the status pin is programmed as EOC and the polarity is set as active low, the pin works in the following manner: The EOC output goes LOW immediately following $\overline{\text{CONVST}}$ going LOW when manual trigger is programmed. EOC stays LOW throughout the conversion process and returns to HIGH when the conversion has ended. The EOC output goes low for 3 conversion clocks (CCLK) after the previous rising edge of EOC, if auto trigger is programmed.

This status pin is programmable. It can be used as an EOC output (CFR_D[7:6] = 1, 1) where the low time is equal to the conversion time. This status pin can be used as $\overline{\text{INT}}$. (CFR_D[7:6] = 1, 0) which is set LOW at the end of a conversion is brought to HIGH (cleared) by the next read cycle. The polarity of this pin, used as either function (EOC or $\overline{\text{INT}}$), is programmable through CFR_D7.

Power-Down Modes

The ADS8329/30 has a comprehensive built-in power-down feature. There are three power-down modes: Deep power-down mode, Nap power-down mode, and auto nap power-down mode. All three power-down modes are enabled by setting the related CFR bits. The first two power-down modes are activated when enabled. A wakeup command, 1011b, can resume device operation from a power-down mode. Auto nap power-down mode works slightly different. When the converter is enabled in auto nap power-down mode, an end of conversion instance (EOC) puts the device into auto nap power-down. The beginning of sampling resumes operation of the converter. The contents of the configuration register is not affected by any of the power-down modes. Any ongoing conversion when nap or deep power-down is activated is aborted.

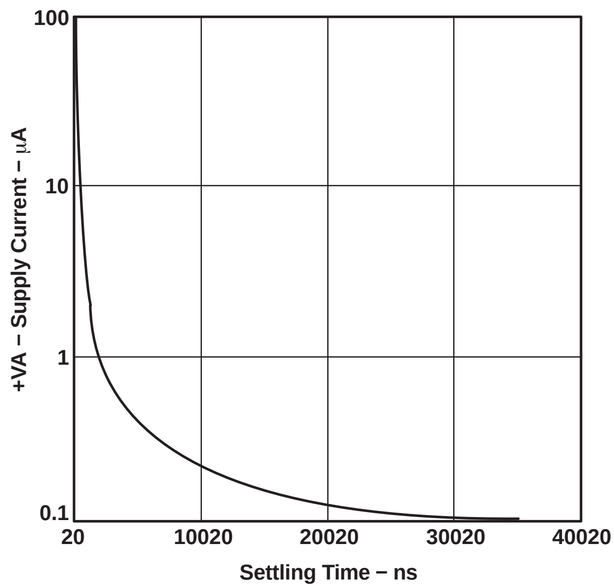


Figure 55. Typical Analog Supply Current Drop vs Time After Power-Down

Deep Power-Down Mode

Deep power-down mode can be activated by writing to configuration register bit CFR_D2. When the device is in deep power-down mode, all blocks except the interface are in power-down. The external SCLK is blocked to the analog block. The analog blocks no longer have bias currents and the internal oscillator is turned off. In this mode, supply current falls from 7 mA to 4 nA in 100 ns. The wake-up time after a power-down is 1 µs. When bit D2 in the configuration register is set to 0, the device is in deep power-down. Setting this bit to 1 or sending a wake-up command can resume the converter from the deep power-down state.

Nap Mode

In nap mode the ADS8329/230 turns off biasing of the comparator and the mid-volt buffer. In this mode supply current falls from 7 mA in normal mode to about 0.3 mA in 200 ns after the configuration cycle. The wake-up (resume) time from nap power-down mode is 3 CCLKs (120 ns with a 24.5-MHz conversion clock). As soon as the CFR_D3 bit in the control register is set to 0, the device goes into nap power-down mode, regardless of the conversion state. Setting this bit to 1 or sending a wake-up command can resume the converter from the nap power-down state.

Auto Nap Mode

Auto nap mode is almost identical to nap mode. The only difference is the time when the device is actually powered down and the method to wake up the device. Configuration register bit D4 is only used to enable/disable auto nap mode. If auto nap mode is enabled, the device turns off biasing after the conversion has finished, which means the end of conversion activates auto nap power-down mode. Supply current falls from 7 mA in normal mode to about 0.3 mA in 200 ns. A $\overline{\text{CONVST}}$ resumes the device and turns biasing on again in 3 CCLKs (120 ns with a 24.5-MHz conversion clock). The device can also be woken up by disabling auto nap mode when bit D4 of the configuration register is set to 1. Any channel select command 0XXXb, wake up command or the set default mode command 1111b can also wake up the device from auto nap power-down.

NOTE:

1. This wake-up command is the word 1011b in the command word. This command sets bits D2 and D3 to 1 in the configuration register but not D4. But a wake-up command does remove the device from either one of these power-down states, deep/nap/auto nap power-down.
2. Wake-up time is defined as the time between when the host processor tries to wake up the converter and when a convert start can occur.

Table 2. Power-Down Mode Comparisons

TYPE OF POWER-DOWN	POWER CONSUMPTION: 5 V/3 V	ACTIVATED BY	ACTIVATION TIME	RESUME POWER BY	RESUME TIME	ENABLE
Normal operation	7 mA/5.1 mA					
Deep power-down	4 nA/2 nA	Setting CFR	100 ns	Woken up by command 1011b	1 µs	Set CFR
Nap power-down	0.3 mA/0.25 mA	Setting CFR	200 ns	Woken up by command 1011b to achieve 6.6 mA since (1.3 + 12)/2 = 6.6	3 CCLKs	Set CFR
Auto nap power-down		EOC (end of conversion)	200 ns	Woken up by $\overline{\text{CONVST}}$, any channel select command, default command 1111b, or wake up command 1011b.	3 CCLKs	Set CFR

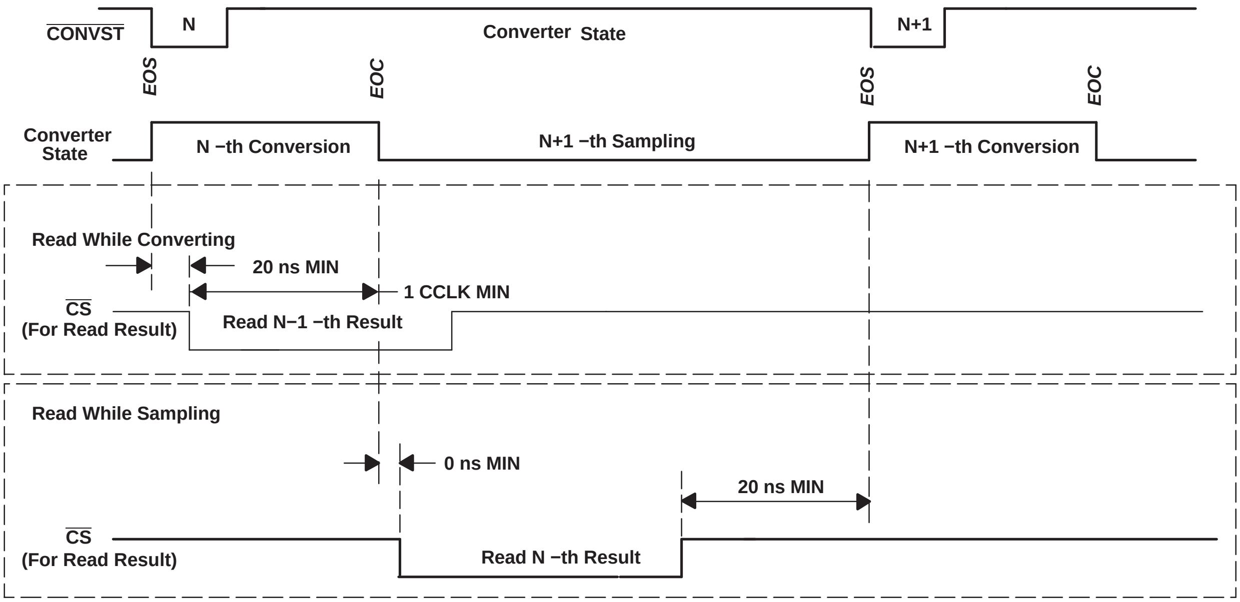


Figure 56. Read While Converting versus Read While Sampling (Manual Trigger)

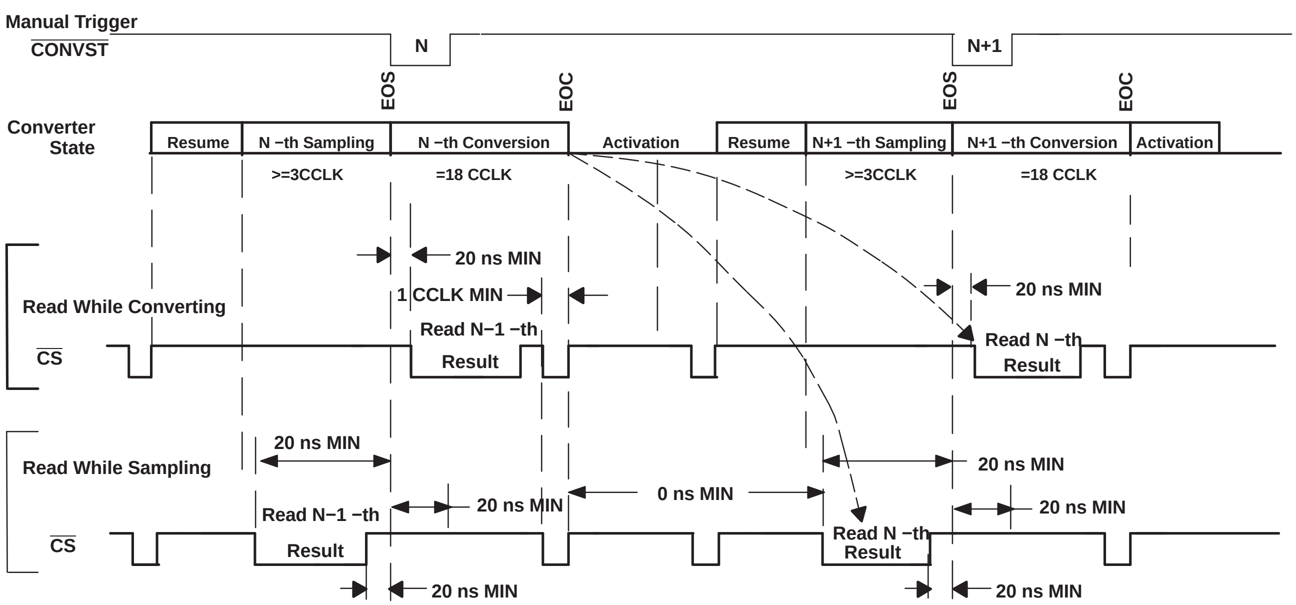


Figure 57. Read While Converting versus Read While Sampling with Deep or Nap Power-Down

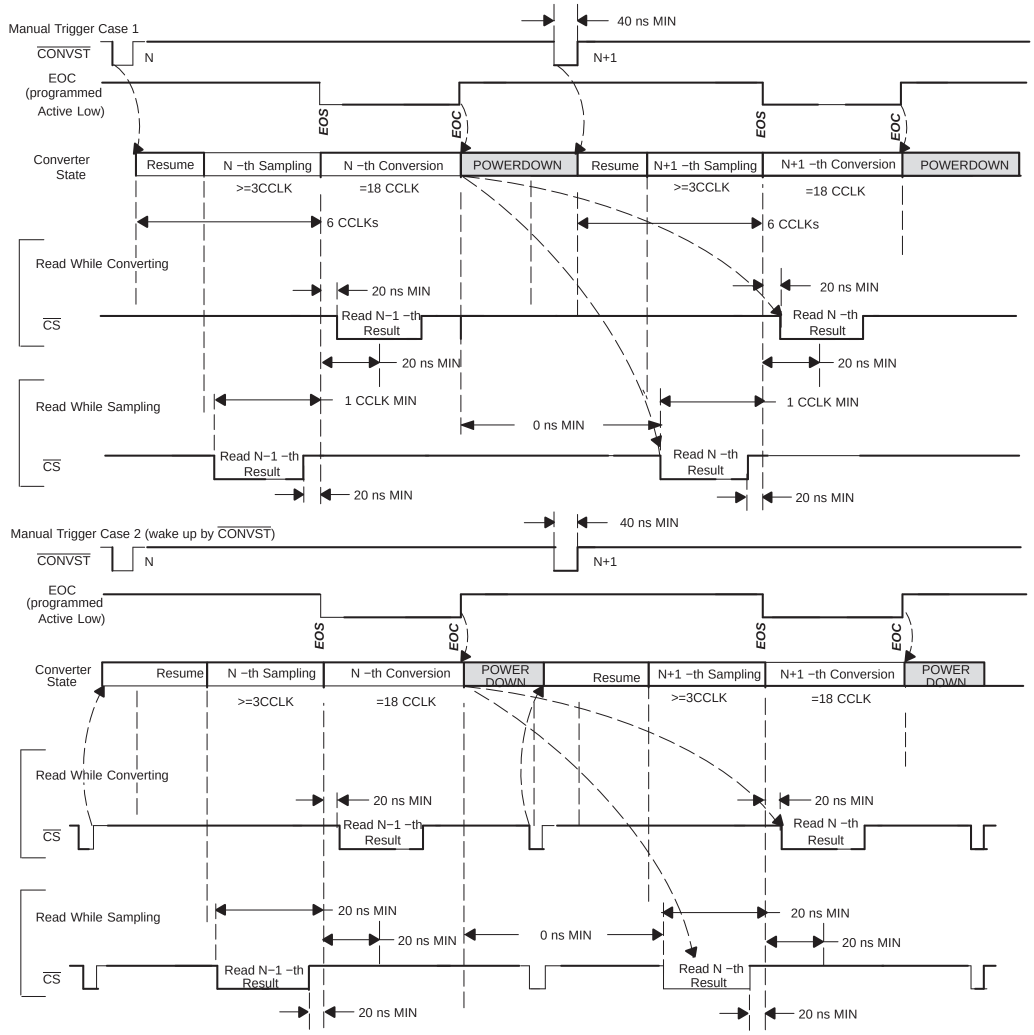


Figure 58. Read While Converting versus Read While Sampling with Auto Nap Power-Down

Total Acquisition + Conversion Cycle Time:

Automatic:	= 21 CCLKs
Manual:	≥ 21 CCLKs
Manual + deep power-down:	≥ 4SCLK + 100 µs + 3 CCLK + 18 CCLK +16 SCLK + 1 µs
Manual + nap power-down:	≥ 4 SCLK + 3 CCLK + 3 CCLK + 18 CCLK +16 SCLK
Manual + auto nap power-down:	≥ 4 SCLK + 3 CCLK + 3 CCLK + 18 CCLK +16 SCLK (use wakeup to resume)
Manual + auto nap power-down:	≥ 1 CCLK + 3 CCLK + 3 CCLK + 18 CCLK +16 SCLK (use $\overline{\text{CONVST}}$ to resume)

DIGITAL INTERFACE

The serial clock is designed to accommodate the latest high-speed processors with an SCLK frequency up to 50 MHz. Each cycle is started with the falling edge of FS/$\overline{CS}$. The internal data register content which is made available to the output register at the EOC presented on the SDO output pin at the falling edge of FS/$\overline{CS}$. This is the MSB. Output data are valid at the falling edge of SCLK with $t_{d(SCLKF\text{-}SDOVALID)}$ delay so that the host processor can read it at the falling edge. Serial data input is also read at the falling edge of SCLK.

The complete serial I/O cycle starts with the first falling edge of SCLK after the falling edge of FS/$\overline{CS}$ and ends 16 (see NOTE) falling edges of SCLK later. The serial interface is very flexible. It works with CPOL = 0 , CPHA = 1 or CPOL = 1, CPHA = 0. This means the falling edge of FS/$\overline{CS}$ may fall while SCLK is high. The same relaxation applies to the rising edge of FS/$\overline{CS}$ where SCLK may be high or low as long as the last SCLK falling edge happens before the rising edge of FS/$\overline{CS}$.

NOTE:

There are cases where a cycle is 4 SCLKs or up to 24 SCLKs depending on the read mode combination. See Table 3 for details.

Internal Register

The internal register consists of two parts, 4 bits for the command register (CMR) and 12 bits for configuration data register (CFR).

Table 3. Command Set Defined by Command Register (CMR)(1)

D[15:12]	HEX	COMMAND	D[11:0]	WAKE UP FROM AUTO NAP	MINIMUM SCLKs REQUIRED	R/W
0000b	0h	Select analog input channel 0(2)	Don't care	Y	4	W
0001b	1h	Select analog input channel 1(2)	Don't care	Y	4	W
0010b	2h	Reserved	Reserved	–	–	–
0011b	3h	Reserved	Reserved	–	–	–
0100b	4h	Reserved	Reserved	–	–	–
0101b	5h	Reserved	Reserved	–	–	–
0110b	6h	Reserved	Reserved	–	–	–
0111b	7h	Reserved	Reserved	–	–	–
1000b	8h	Reserved	Reserved	–	–	–
1001b	9h	Reserved	Reserved	–	–	–
1010b	Ah	Reserved	Reserved	–	–	–
1011b	Bh	Wake up	Don't care	Y	4	W
1100b	Ch	Read CFR	Don't care	–	16	R
1101b	Dh	Read data	Don't care	–	16	R
1110	Eh	Write CFR	CFR value	–	16	W
1111b	Fh	Default mode (load CFR with default value)	Don't care	Y	4	W

(1) When SDO is not in 3-state (FS/$\overline{CS}$ low and SCLK running), the bits from SDO are always part (depending on how many SCLKs are supplied) of the previous conversion result.
(2) These two commands apply to the ADS8330 only.

WRITING TO THE CONVERTER

There are two different types of writes to the register, a 4-bit write to the CMR and a full 16-bit write to the CMR plus CFR. The command set is listed in Table 3. A simple command requires only 4 SCLKs and the write takes effect at the 4th falling edge of SCLK. A 16-bit write or read takes at least 16 SCLKs (see Table 6 for exceptions that require more than 16 SCLKs).

Configuring the Converter and Default Mode

The converter can be configuring with command 1110b (write to the CFR) or command 1111b (default mode). A write to the CFR requires a 4-bit command followed by 12-bits of data. A 4-bit command takes effect at the 4th falling edge of SCLK. A CFR write takes effect at the 16th falling edge of SCLK.

A default mode command can be achieved by simply tying SDI to +VBD. As soon as the chip is selected at least four 1s are clocked in by SCLK. The default value of the CFR is loaded into the CFR at the 4th falling edge of SCLK.

CFR default values are all 1s (except for CFR_D1, this bit is ignored by the ADS8329 and is always read as a 0). The same default values apply for the CFR after a power-on reset (POR) and SW reset.

READING THE CONFIGURATION REGISTER

The host processor can read back the value programmed in the CFR by issuing command 1100b. The timing is similar to reading a conversion result except CONVST is not used and there is no activity on the EOC/INT pin. The CFR value read back contains the first four MSBs of conversion data plus valid 12-bit CFR contents.

Table 4. Configuration Register (CFR) Map

SDI BIT CFR - D[11 - 0]	DEFINITION	
D11 default = 1	Channel select mode	
	0: Manual channel select enabled. Use channel select commands to access a different channel.	1: Auto channel select enabled. All channels are sampled and converted sequentially until the cycle after this bit is set to 0.
D10 default = 1	Conversion clock (CCLK) source select	
	0: Conversion clock (CCLK) = SCLK/2	1: Conversion clock (CCLK) = Internal OSC
D9 default = 1	Trigger (conversion start) select: start conversion at the end of sampling (EOS). If D9 = 0, the D4 setting is ignored.	
	0: Auto trigger automatically starts (4 internal clocks after EOC inactive)	1: Manual trigger manually started by falling edge of CONVST
D8 default = 1	Don't care	Don't care
D7 default = 1	Pin 10 polarity select when used as an output (EOC/INT)	
	0: EOC Active high / INT active high	1: EOC active low / INT active low
D6 default = 1	Pin 10 function select when used as an output (EOC/INT)	
	0: Pin used as INT	1: Pin used as EOC
D5 default = 1	Pin 10 I/O select for chain mode operation	
	0: Pin 10 is used as CDI input (chain mode enabled)	1: Pin 10 is used as EOC/INT output
D4 default = 1	Auto nap power-down enable/disable (mid voltage and comparator shut down between cycles). This bit setting is ignored if D9 = 0.	
	0: Auto nap power-down enabled (not activated)	1: Auto nap power-down disabled
D3 default = 1	Nap power-down (mid voltage and comparator shut down between cycles). This bit is set to 1 automatically by wake-up command.	
	0: Enable/activate device in nap power-down	1: Remove device from nap power-down (resume)
D2 default = 1	Deep power-down. This bit is set to 1 automatically by wake-up command.	
	0: Enable/activate device in deep power-down	1: Remove device from deep power-down (resume)
D1 default = 0: ADS8329 1: ADS8330	TAG bit enable. This bit is ignored by the ADS8329 and is always read 0.	
	0: TAG bit disabled.	1: TAG bit output enabled. TAG bit appears at the 17th SCLK.
D0 default = 1	Reset	
	0: System reset	1: Normal operation

READING CONVERSION RESULT

The conversion result is available to the input of the output data register (ODR) at EOC and presented to the output of the output register at the next falling edge of CS or FS. The host processor can then shift the data out via the SDO pin any time except during the quiet zone. This is 20 ns before and 20 ns after the end of sampling (EOS) period. End of sampling (EOS) is defined as the falling edge of CONVST when manual trigger is used or the end of the 3rd conversion clock (CCLK) after EOC if auto trigger is used.

The falling edge of FS/CS should not be placed at the precise moment (minimum of at least one conversion clock (CCLK) delay) at the end of a conversion (by default when EOC goes high), otherwise the data is corrupt. If FS/CS is placed before the end of a conversion, the previous conversion result is read. If FS/CS is placed after the end of a conversion, the current conversion result is read.

The conversion result is 16-bit data in straight binary format as shown in Table 4. Generally 16 SCLKs are necessary, but there are exceptions where more than 16 SCLKS are required (see Table 6). Data output from the serial output (SDO) is left adjusted MSB first. The trailing bits are filled with the TAG bit first (if enabled) plus all zeros. SDO remains low until FS/CS is brought high again.

SDO is active when FS/CS is low. The rising edge of FS/CS 3-states the SDO output.

NOTE:

Whenever SDO is not in 3-state (when FS/CS is low and SCLK is running), a portion of the conversion result is output at the SDO pin. The number of bits depends on how many SCLKs are supplied. For example, a manual select channel command cycle requires 4 SCLKs, therefore 4 MSBs of the conversion result are output at SDO. The exception is SDO outputs all 1s during the cycle immediately after any reset (POR or software reset).

If SCLK is used as the conversion clock (CCLK) and a continuous SCLK is used, it is not possible to clock out all 16 SDO bits during the sampling time (6 SCLKs) because of the quiet zone requirement. In this case it is better to read the conversion result during the conversion time (36 SCLKs or 48 SCLKs in auto nap mode).

Table 5. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
Full-scale range	V_{REF}		
Least significant bit (LSB)	$V_{REF}/65536$	BINARY CODE	HEX CODE
Full-scale	$+V_{REF}$ – 1 LSB	1111 1111 1111 1111	FFFF
Midscale	$V_{REF}/2$	1000 0000 0000 0000	8000
Midscale – 1 LSB	$V_{REF}/2$– 1 LSB	0111 1111 1111 1111	7FFF
Zero	0 V	0000 0000 0000 0000	0000

TAG Mode

The ADS8330 includes a feature, TAG, that can be used as a tag to indicate which channel sourced the converted result. An address bit is added after the LSB read out from SDO indicating which channel the result came from if TAG mode is enabled. This address bit is 0 for channel 0 and 1 for channel 1. The converter requires more than the 16 SCLKs that are required for a 4 bit command plus 12 bit CFR or 16 data bits because of the additional TAG bit.

Chain Mode

The ADS8329/30 can operate as a single converter or in a system with multiple converters. System designers can take advantage of the simple high-speed SPI compatible serial interface by cascading them in a single chain when multiple converters are used. A bit in the CFR is used to reconfigure the EOC/INT status pin as a secondary serial data input, chain data input (CDI), for the conversion result from an upstream converter. This is chain mode operation. A typical connection of three converters is shown in Figure 59.

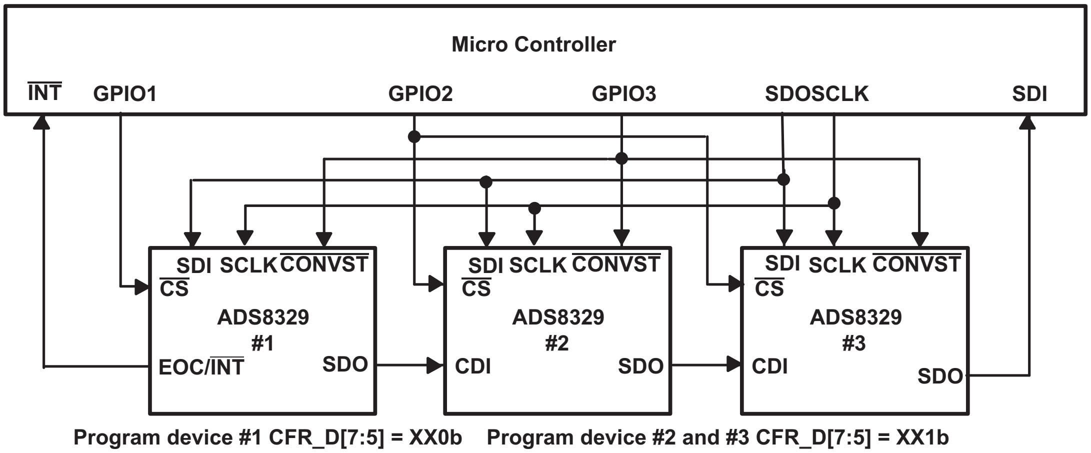


Figure 59. Multiple Converters Connected Using Chain Mode

When multiple converters are used in chain mode, the first converter is configured in regular mode while the rest of the converters downstream are configured in chain mode. When a converter is configured in chain mode, the CDI input data goes straight to the output register, therefore the serial input data passes through the converter with a 16 SCLK (if the TAG feature is disabled) or a 24 SCLK delay, as long as CS is active. See Figure 60 for detailed timing. In this timing the conversion in each converters are done simultaneously.

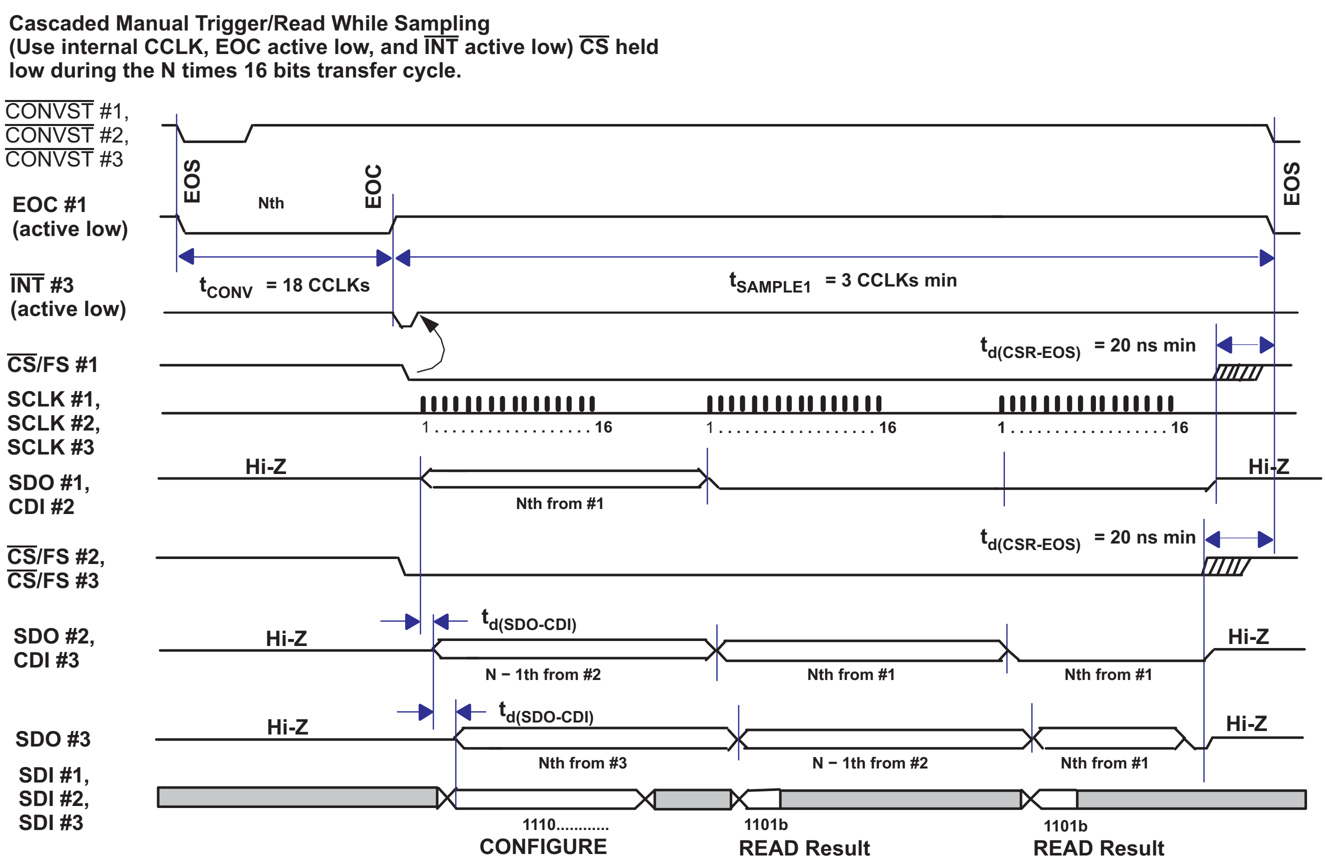


Figure 60. Simplified Cascade Mode Timing with Shared CONVST and Continuous CS

Care must be given to handle the multiple $\overline{CS}$ signals when the converters are operating in chain mode. The different chip select signals must be low for the entire data transfer (in this example 48 bits for three converters). The first 16-bit word after the falling chip select is always the data from the chip that received the chip select signal.

Case 1: If chip select is not toggled ($\overline{CS}$ stays low), the next 16 bits are data from the upstream converter, and so on. This is shown in Figure 60. If there is no upstream converter in the chain, as converter #1 in the example, the same data from the converter is going to be shown repeatedly.

Case 2: If the chip select is toggled during a chain mode data transfer cycle, as illustrated in Figure 61, the same data from the converter is read out again and again in all three discrete 16-bit cycles. This is not a desired result.

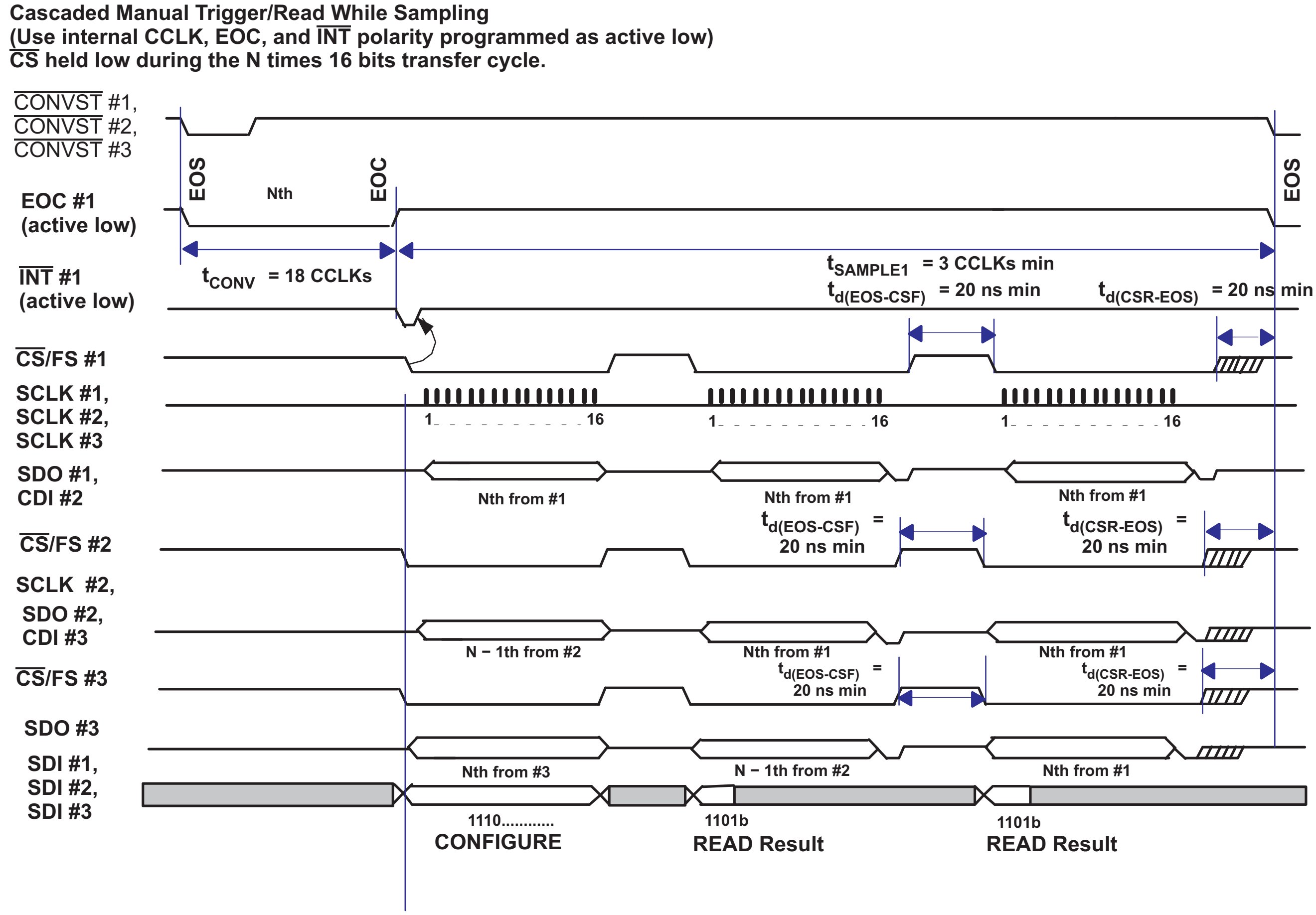


Figure 61. Simplified Cascade Mode Timing with Shared $\overline{CONVST}$ and Discrete $\overline{CS}$

Figure 62 shows a slightly different scenario where $\overline{CONVST}$ is not shared by the second converter. Converters #1 and #3 have the same $\overline{CONVST}$ signal. In this case, converter #2 simply passes previous conversion data downstream.

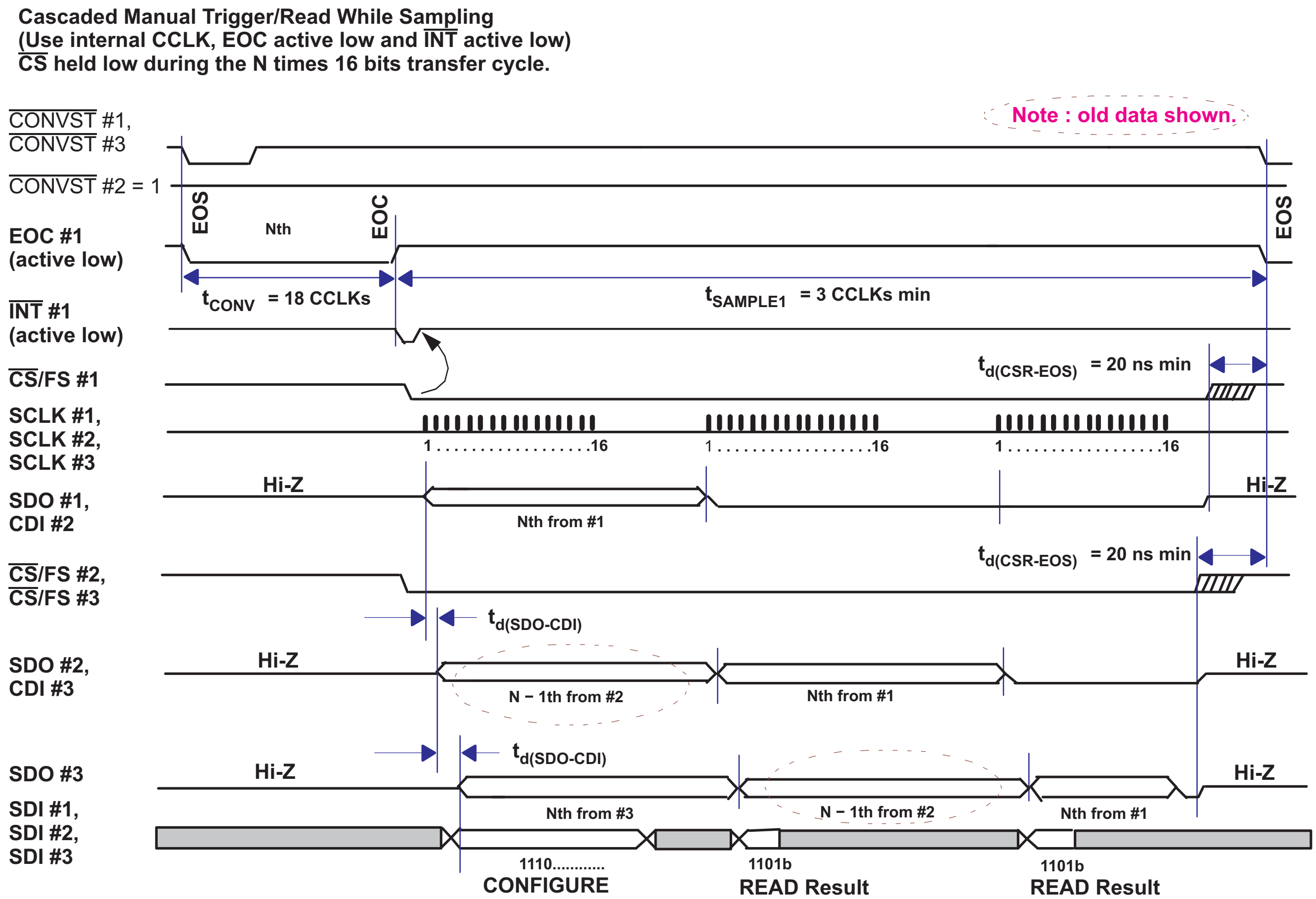


Figure 62. Simplified Cascade Timing (Separate $\overline{\text{CONVST}}$)

The number of SCLKs required for a serial read cycle depends on the combination of different read modes, TAG bit, chain mode, and the way a channel is selected (that is, auto channel select). This is listed in Table 6.

Table 6. Required SCLKs For Different Read Out Mode Combinations

CHAIN MODE ENABLED CFR.D5	AUTO CHANNEL SELECT CFR.D11	TAG ENABLED CFR.D1	NUMBER OF SCLK PER SPI READ	TRAILING BITS
0	0	0	16	None
0	0	1	≥17	MSB is TAG bit plus zero(s)
0	1	0	16	None
0	1	1	≥17	TAG bit plus 7 zeros
1	0	0	16	None
1	0	1	24	TAG bit plus 7 zeros
1	1	0	16	None
1	1	1	24	TAG bit plus 7 zeros

SCLK skew between converters and data path delay through the converters configured in chain mode can affect the maximum frequency of SCLK. The delay can also be affected by supply voltage and loading. It may be necessary to slow down the SCLK when the devices are configured in chain mode.

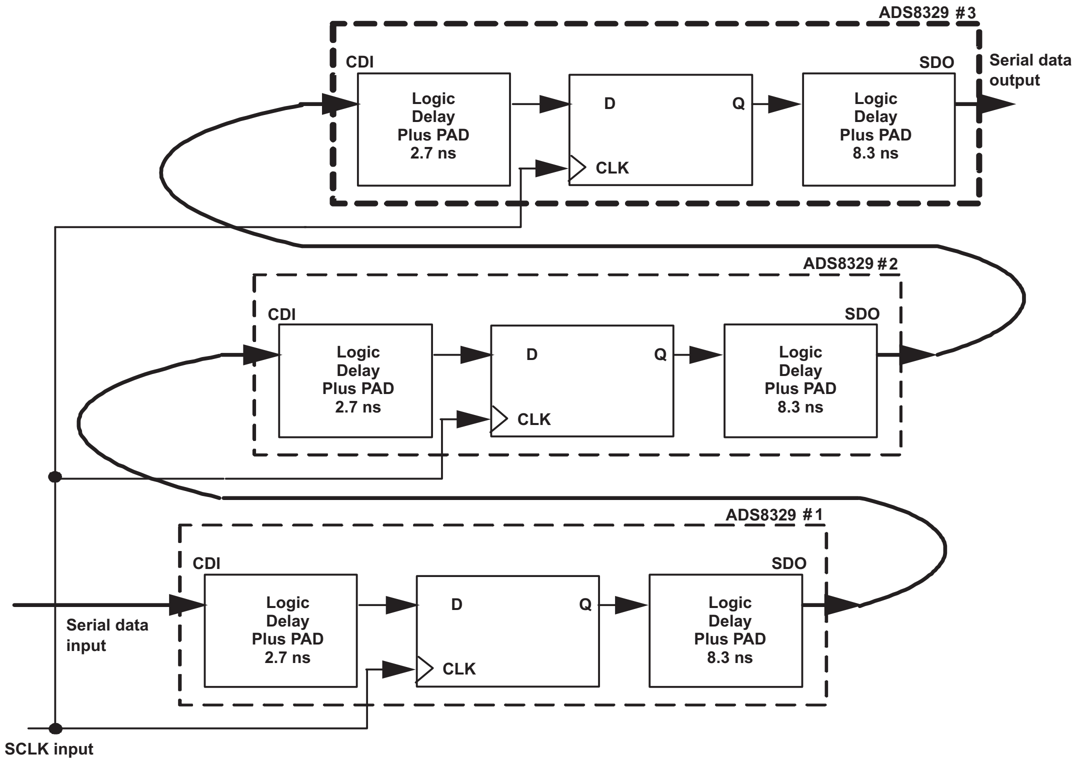


Figure 63. Typical Delay Through Converters Configured in Chain Mode

RESET

The converter has two reset mechanisms, a power-on reset (POR) and a software reset using CFR_D0. These two mechanisms are NOR-ed internally. When a reset (software or POR) is issued, all register data are set to the default values (all 1s) and the SDO output (during the cycle immediately after reset) is set to all 1s. The state machine is reset to the power-on state.

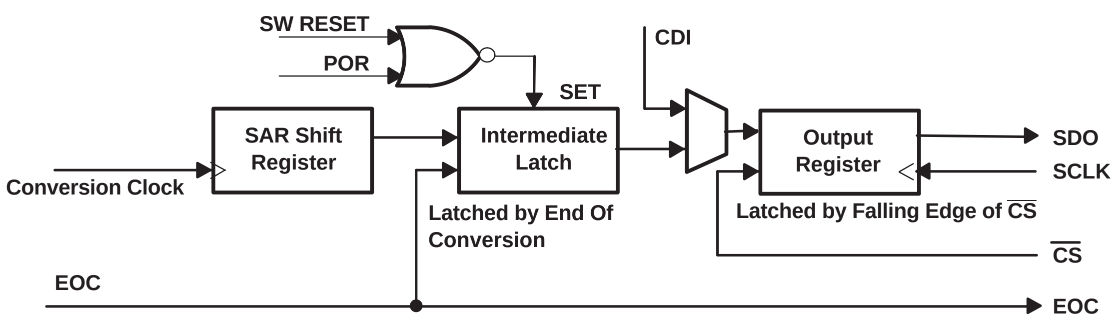


Figure 64. Digital Output Under Reset Condition

When the device is powered up, the POR sets the device to default mode when AVDD reaches 1.5V. When the device is powered down, the POR circuit requires AVDD to remain below 125mV for at least 350ms to ensure proper discharging of internal capacitors and to correct the behavior of the ADC when powered up again. If AVDD drops below 400mV but remains above 125mV, the internal POR capacitor does not discharge fully and the device requires a software reset to perform correctly after the recovery of AVDD (this condition is shown as the *undefined zone* in Figure 65).

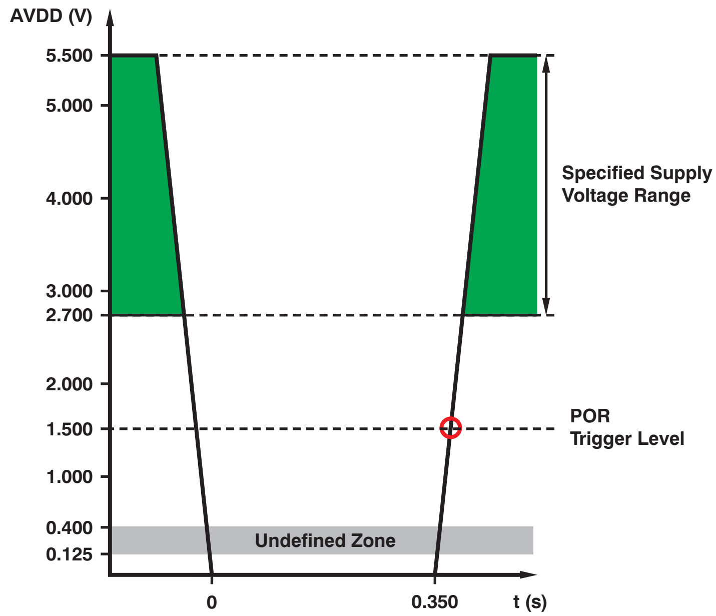


Figure 65. Relevant Voltage Levels for POR

APPLICATION INFORMATION

TYPICAL CONNECTION

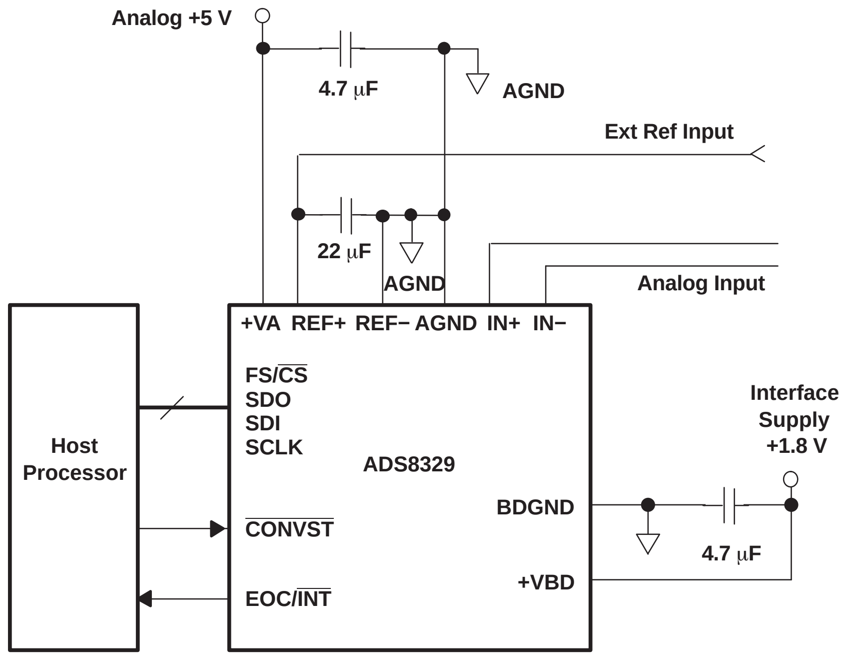


Figure 66. Typical Circuit Configuration

Part Change Notification # 20071101001

The ADS8329 and ADS8330 devices underwent a silicon change under Texas Instruments Part Change Notification (PCN) number 20071101001. Details on this part change can be obtained from the Product Information Center at Texas Instruments or by contacting your local sales/distribution office. Devices with a date code of **82xx** and higher are covered by this PCN.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2008) to Revision C **Page**

Changes from Revision A (March 2008) to Revision B **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8329IBPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8329I A B	Samples
ADS8329IBRSAR	ACTIVE	QFN	RSA	16	3000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8329I A	Samples
ADS8329IBRSAT	ACTIVE	QFN	RSA	16	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8329I A	Samples
ADS8329IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8329I A	Samples
ADS8329IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8329I A	Samples
ADS8329IRSAR	ACTIVE	QFN	RSA	16	2000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8329I A	Samples
ADS8329IRSAT	ACTIVE	QFN	RSA	16	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8329I A	Samples
ADS8330IBPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8330I A B	Samples
ADS8330IBPWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8330I A B	Samples
ADS8330IBPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8330I A B	Samples
ADS8330IBRSAR	ACTIVE	QFN	RSA	16	3000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8330I A	Samples
ADS8330IBRSAT	ACTIVE	QFN	RSA	16	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8330I A	Samples
ADS8330IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8330I A	Samples
ADS8330IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8330I A	Samples
ADS8330IRSAT	ACTIVE	QFN	RSA	16	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS 8330I A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

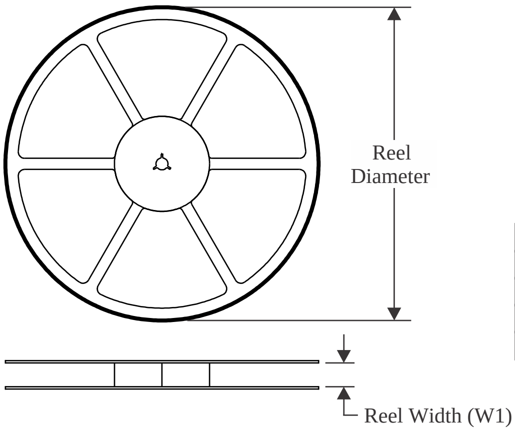
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

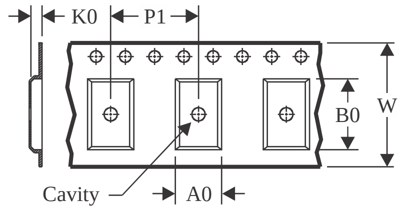
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

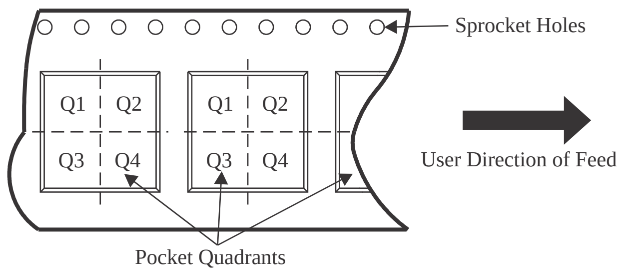


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

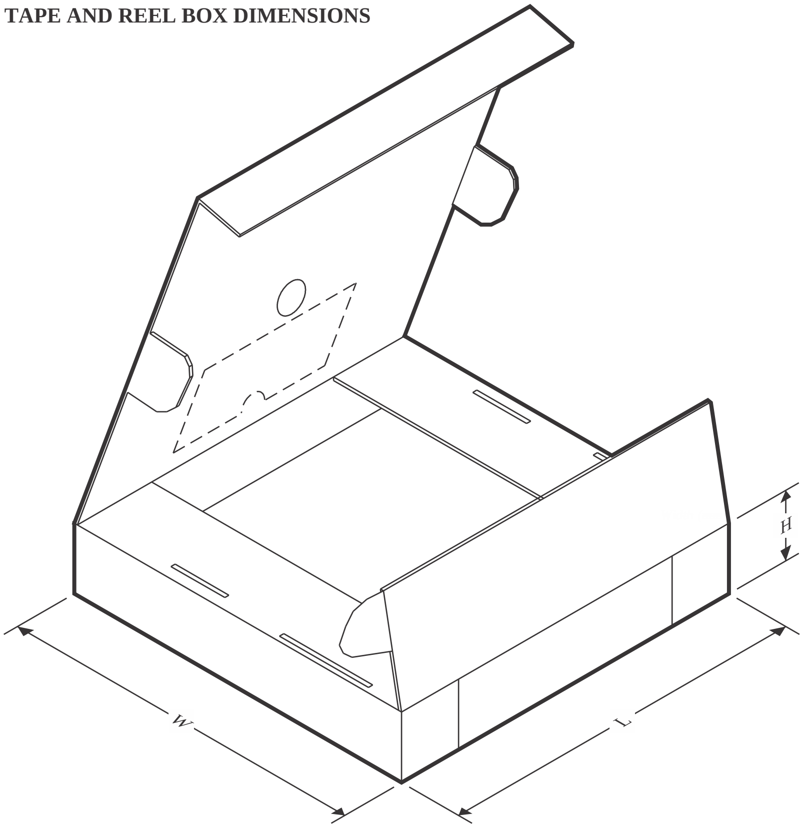
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8329IBRSAR	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
ADS8329IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS8329IRSAR	QFN	RSA	16	2000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
ADS8330IBPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS8330IBRSAR	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
ADS8330IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

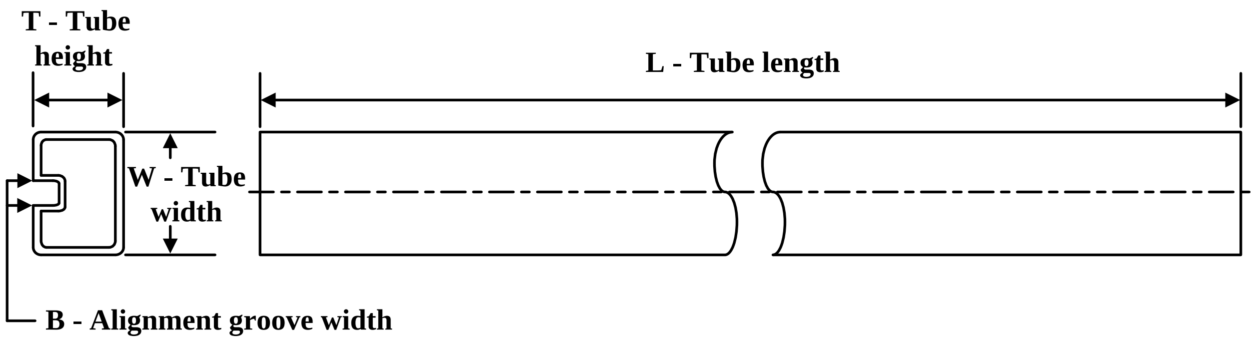
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

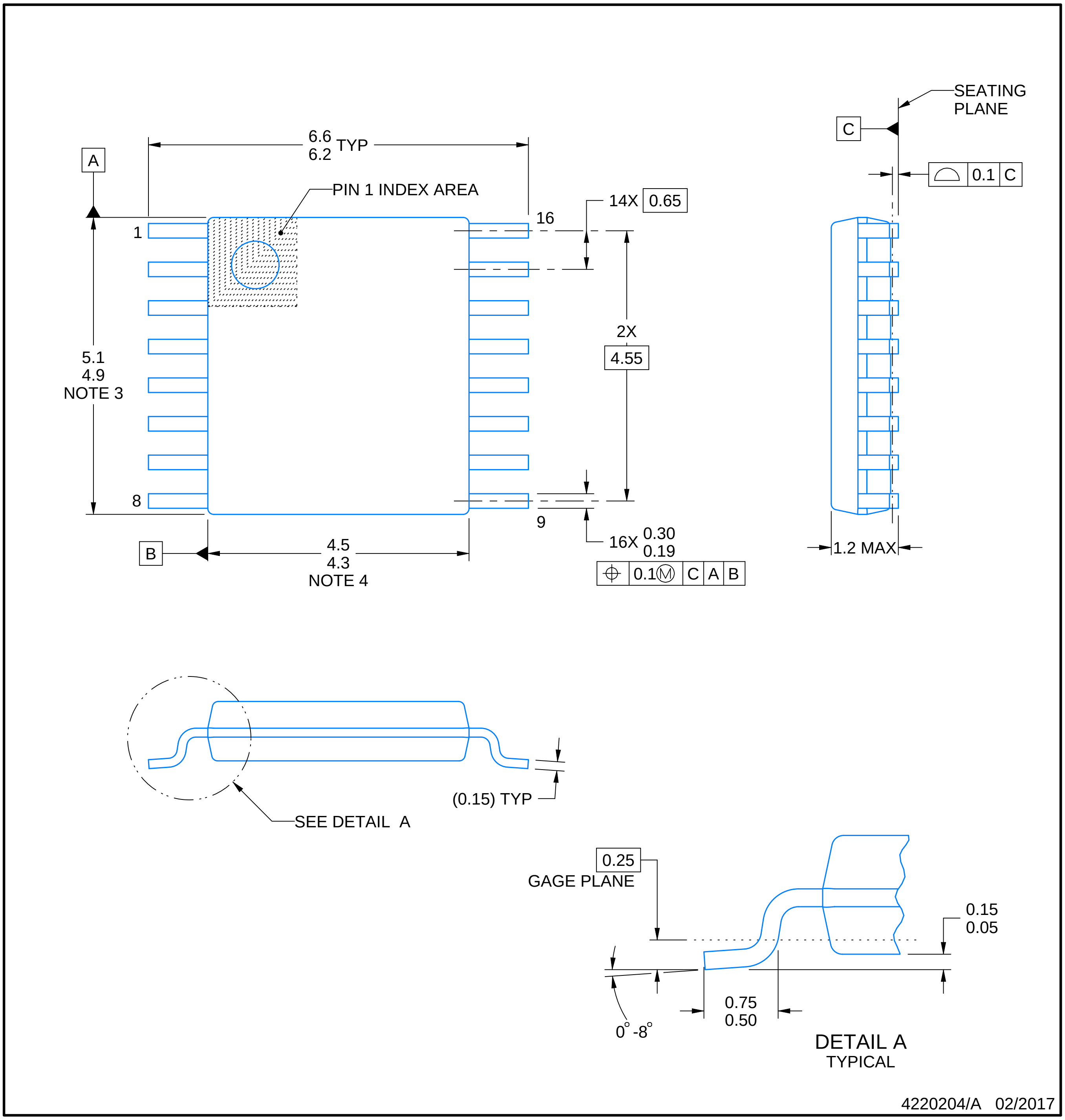
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8329IBRSAR	QFN	RSA	16	3000	350.0	350.0	43.0
ADS8329IPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
ADS8329IRSAR	QFN	RSA	16	2000	350.0	350.0	43.0
ADS8330IBPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
ADS8330IBRSAR	QFN	RSA	16	3000	350.0	350.0	43.0
ADS8330IPWR	TSSOP	PW	16	2000	350.0	350.0	43.0

TUBE



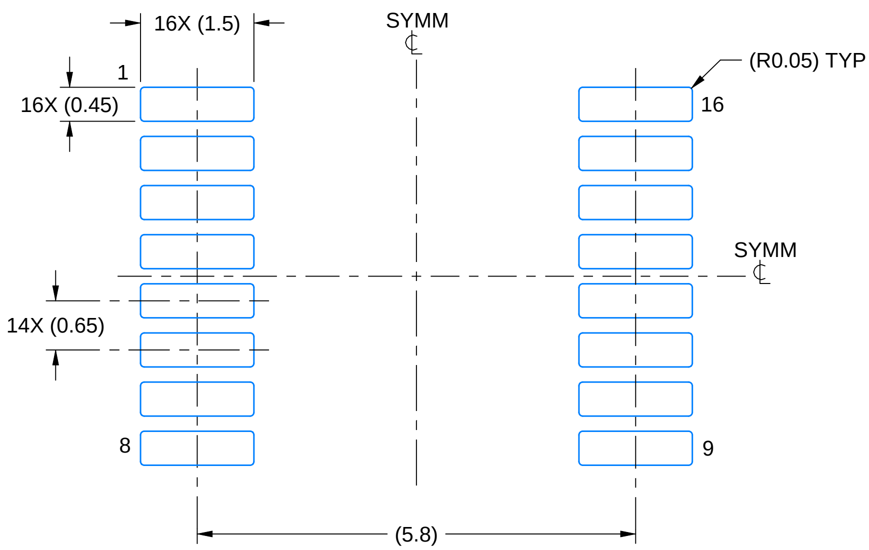
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS8329IBPW	PW	TSSOP	16	90	530	10.2	3600	3.5
ADS8329IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
ADS8330IBPW	PW	TSSOP	16	90	530	10.2	3600	3.5
ADS8330IBPWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
ADS8330IPW	PW	TSSOP	16	90	530	10.2	3600	3.5

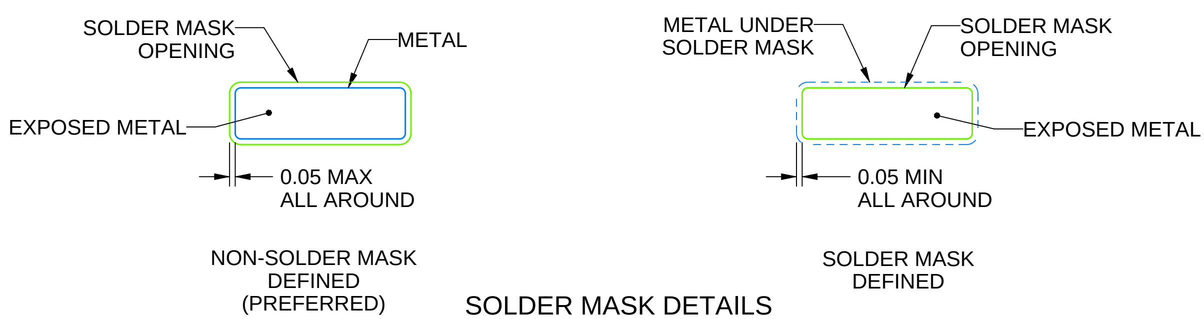


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

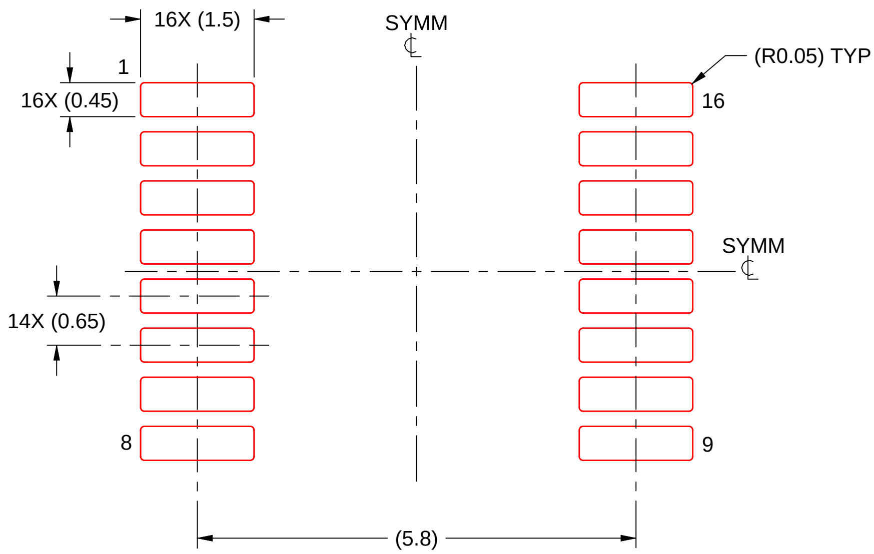


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



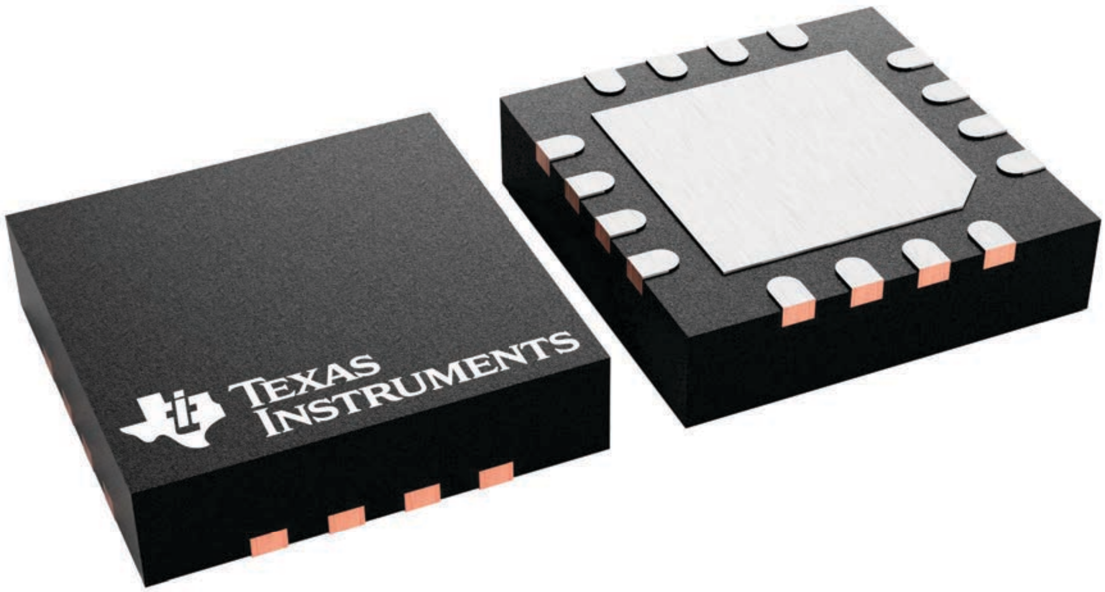
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

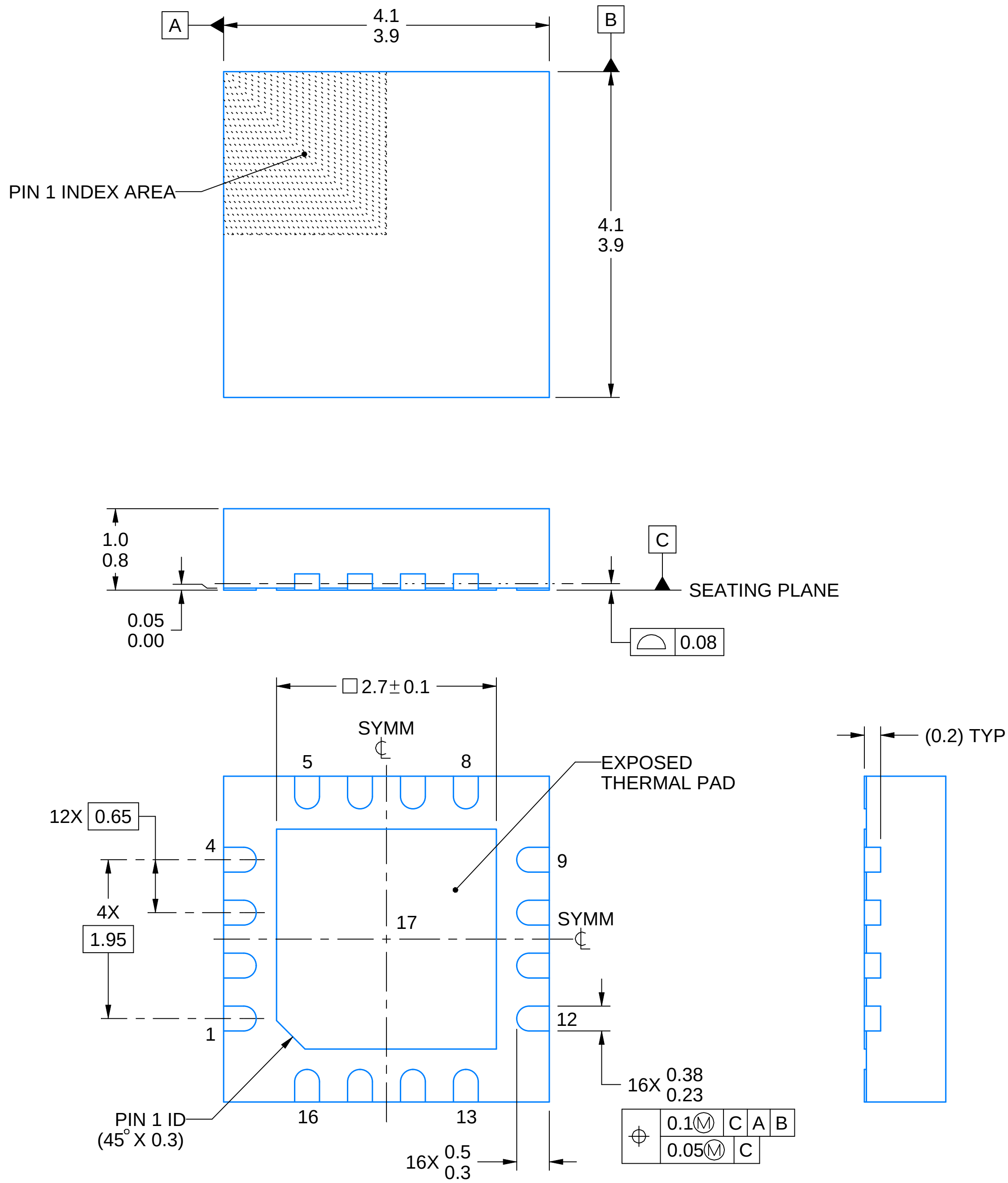
4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

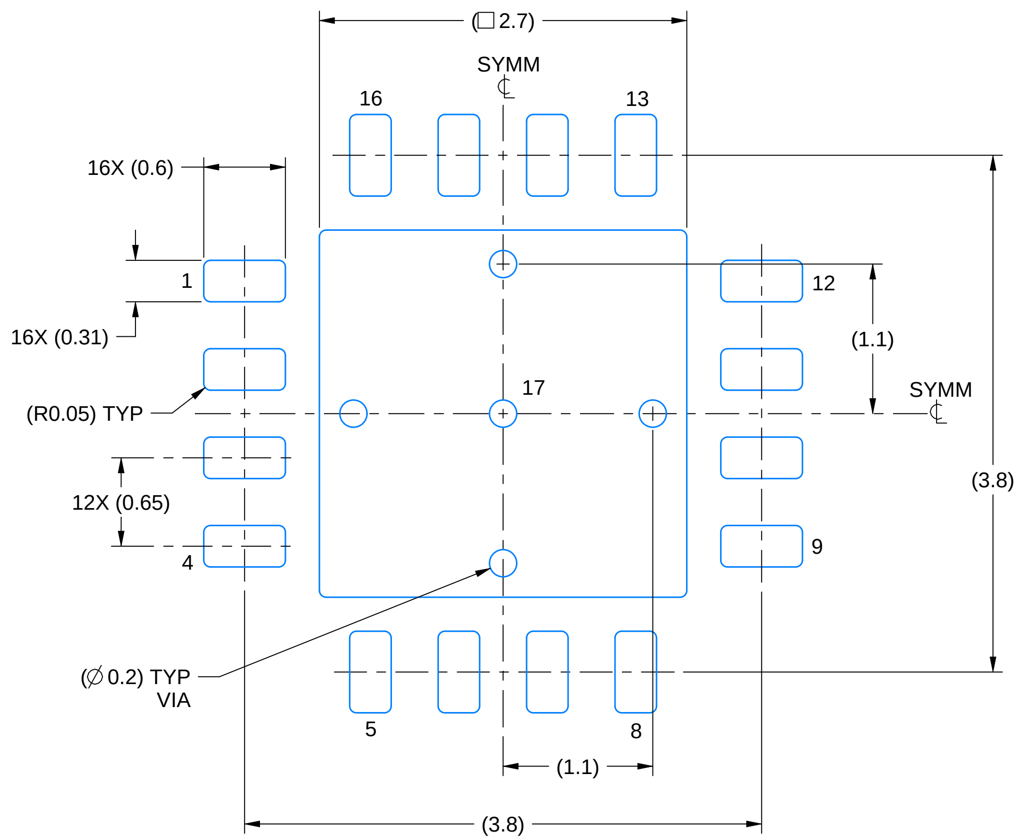




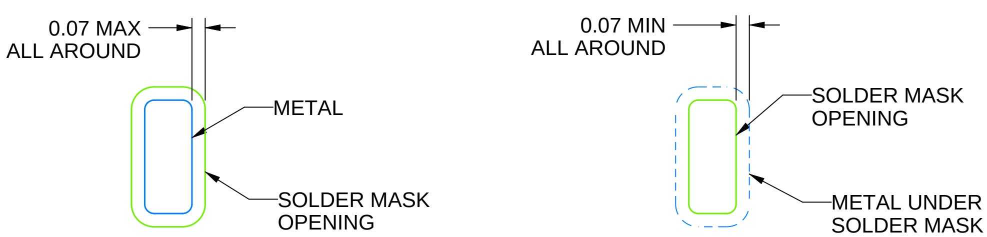
4219093/A 08/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

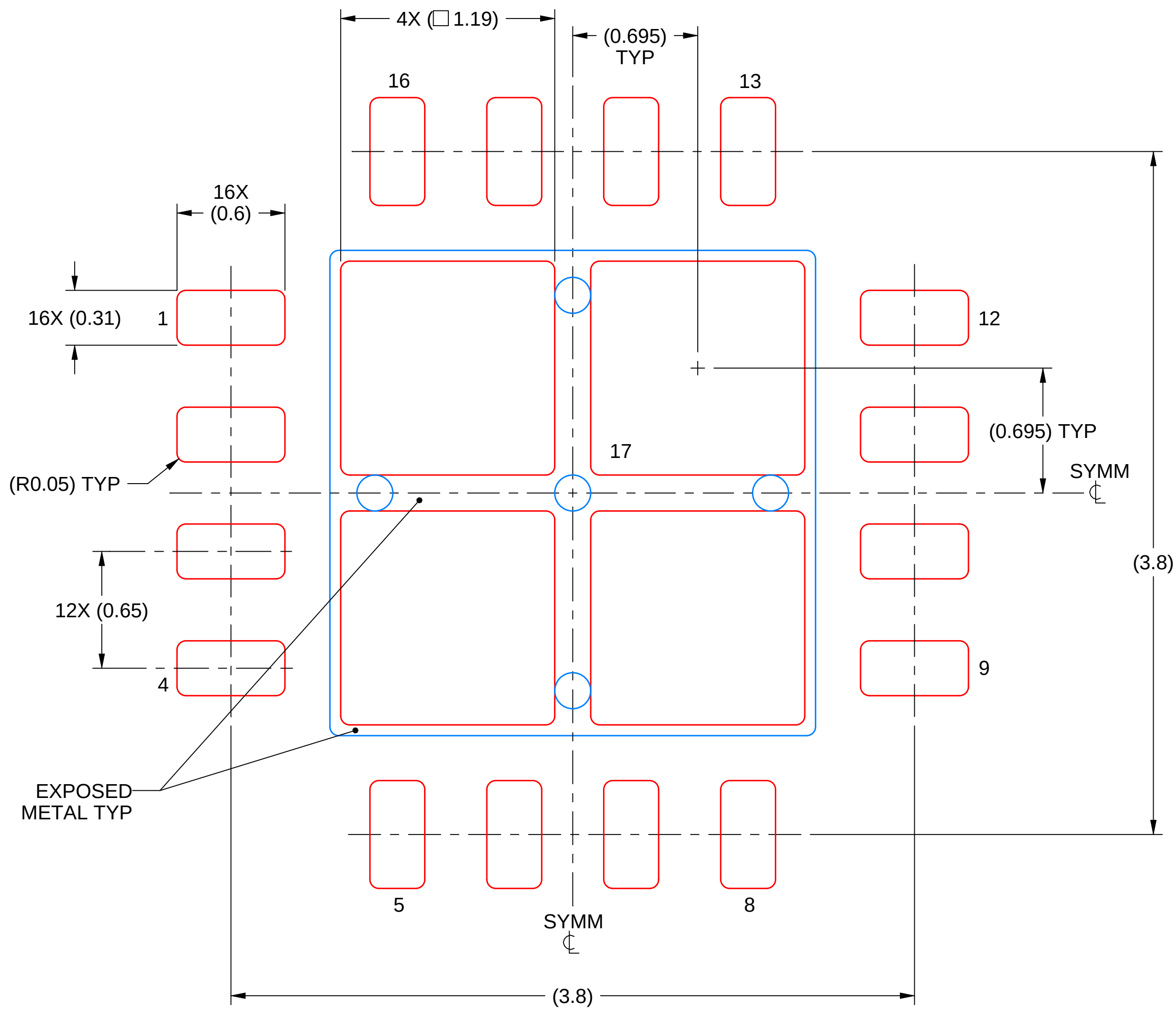
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219093/A 08/2021

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4219093/A 08/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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