

# AFE7950-x 4T6R RF Sampling AFE with 12GSPS DACs and 3GSPS ADCs

## 1 Features

- [Request full data sheet](#)
- Radiation hardness assured AFE7950-SP:
  - Single-event latch up (SEL): 70MeV-cm<sup>2</sup>/mg
  - RLAT Total ionizing dose (TID): 100krad (Si)
- Radiation tolerant AFE7950-SEP:
  - Single-event latch up (SEL): 43MeV-cm<sup>2</sup>/mg
  - RLAT Total ionizing dose (TID): 30krad (Si)
- Four RF sampling 12GSPS TX DACs
- Six RF sampling 3GSPS RX ADCs
- Maximum RF signal bandwidth: 1200MHz (or 2400MHz for 2TX)
- RF frequency range:
  - TX: 600MHz to 12GHz
  - RX: 5MHz to 12GHz
- Digital Step Attenuators (DSA):
  - TX: 40dB range, 0.125dB steps
  - RX or FB: 25dB range, 0.5dB steps
- Single or dual-band DUC or DDCs for TX and RX
- SerDes data interface:
  - 8 SerDes transceivers up to 24.75Gbps
  - JESD204B/C subclass 1 compatible
- Package: 17mm × 17mm FCBGA, 0.8mm pitch
- Screening:
  - One fabrication, assembly, and test site
  - Product traceability
  - Extended product life cycle
  - Extended product change notification
  - Vendor item drawing
  - Radiation lot acceptance Test (RLAT) (AFE7950-Sx only)
  - Meets ASTM E595 out gassing specification (AFE7950-Sx only)
  - Production burn-in (AFE7950-SP only)

## 2 Applications

- [Satellite communications payload downlink](#)
- [Satellite telemetry payload downlink](#)

## 3 Description

The AFE7950-x is a high performance, wide bandwidth multi-channel transceiver, integrating four RF sampling transmitter chains, four RF sampling receiver chains and two RF sampling feedback chains (six RF sampling ADCs total). With operation up to 12GHz, this device enables direct RF sampling in the L, S, C and X-band frequency ranges without the need for additional frequency conversions stages. This improvement in density and flexibility enables high-channel-count, multi-mission systems.

The TX signal paths support interpolation and digital up conversion options that deliver up to 1200MHz of signal bandwidth for four TX or 2400MHz for two TX. The output of the DUCs drives a 12GSPS DAC (digital to analog converter) with a mixed mode output option to enhance 2<sup>nd</sup> Nyquist operation. The DAC output includes a variable gain amplifier (TX DSA) with 40dB range and 1dB analog and 0.125dB digital steps.

Each receiver chain includes a 25dB range Digital Step Attenuator (DSA), followed by a 3GSPS ADC (analog-to-digital converter). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. Flexible decimation options provide optimization of data bandwidth up to 1200MHz for four RX without FB paths or 600MHz with two FB paths (1200MHz BW each).

### Device Information

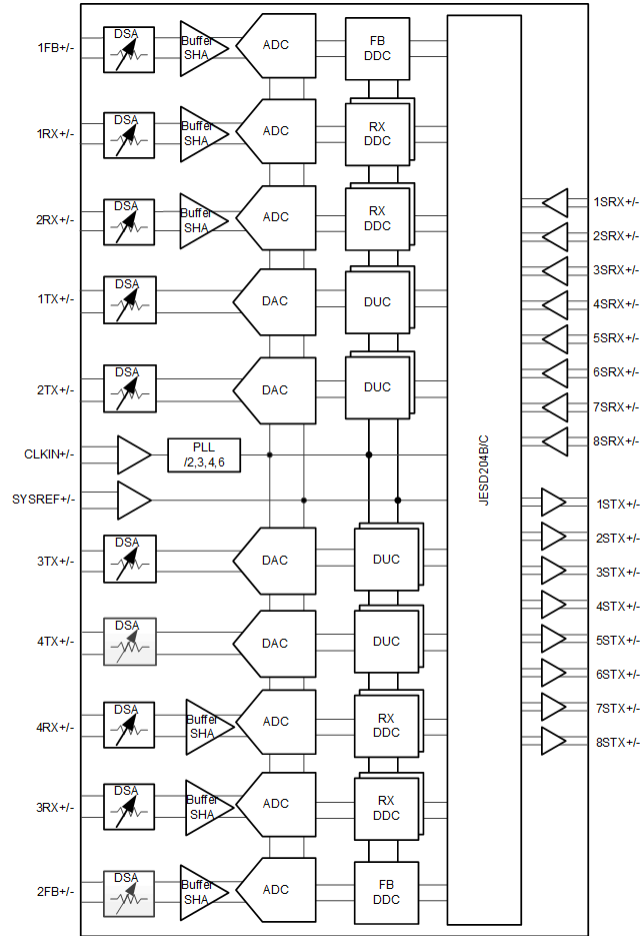
PART NUMBER	GRADE	PACKAGE SIZE <sup>(1)</sup> <sup>(2)</sup>
AFE7950-SP	Radiation-hardness-assured space (RHA)	17mm x 17mm plastic substrate
AFE7950-SEP <sup>(3)</sup>	Radiation-tolerant Space Enhanced Product	FC-BGA 400 SnPb balls 0.8mm pitch
AFE7950-EP <sup>(3)</sup>	Enhanced Product	

(1) For more information, see [Section 7](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) Product preview





Functional Block Diagram

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## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	-0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	-0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVC0, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	-0.5	2.1	V
Pin Voltage Range	{1/2/3/4}RXIN+/-	-0.5	VDDR1P8+0.3	V
	1FBIN+/-, 2FB+/-	-0.5	VDDFB1P8+0.3	V
	{1/2/3/4}TXOUT+/-	-0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	-0.3	1.4	V
	{1:8}SRX+/-	-0.3	1.4	V
	{1:8}STX+/-	-0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	-0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	-0.3	VDDCLK1P8 + 0.3	V
SRDAMUX1, SRDAMUX2	-0.3	VDDA1P8+0.3	V	
Peak Input Current	any input		20	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 4.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	1000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins	150	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/ PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/ TXENC/PLL/PLLVCO/FB/FBCLK/ GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T <sub>A</sub>	Ambient temperature	-45		85	°C
T <sub>J</sub>	Operating Junction Temperature			105	°C

### 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		FC-BGA	UNIT
		400 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	15.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	0.44	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	4.8	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	4.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 4.5 Transmitter Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC <sub>RES</sub>	DAC resolution			14		bits
F <sub>DAC</sub>	DAC Sample Rate		9		12	GSPS
f <sub>RFout_MIN</sub>	RF output frequency range	Requires PCB matching based on frequency range		600		MHz
f <sub>RFout_MAX</sub>	RF output frequency range	Requires PCB matching based on frequency range		12000		MHz
P <sub>max_FS</sub>	Max Full Scale Output Power, max gain 1 tone, at device pins	f <sub>out</sub> = 850 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS		4.2		dBm
		f <sub>out</sub> = 1800 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS		4.6		dBm
		f <sub>out</sub> = 2600 MHz, f <sub>DAC</sub> = 8847.36 MSPS, -0.5dBFS		4.0		dBm
		f <sub>out</sub> = 3500 MHz, -0.5dBFS		3.9		dBm
		f <sub>out</sub> = 4900 MHz, -0.5dBFS		3.1		dBm
		f <sub>out</sub> = 3500 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS, straight mode		1.0		dBm
		f <sub>out</sub> = 4900 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS, straight mode		0.1		dBm
		f <sub>out</sub> = 4900 MHz, f <sub>DAC</sub> = 8847.36 MSPS, -0.5dBFS, straight mode		-0.7		dBm
		f <sub>out</sub> = 8100 MHz, -0.1dBFS, mixed mode		-2.8		dBm
f <sub>out</sub> = 9600 MHz, -0.1dBFS, mixed mode		-4.3		dBm		
R <sub>TERM</sub>	Output termination resistor	Default setting		50		Ω
ATT <sub>range</sub>	DSA Attenuation range			40		dB
ATT <sub>step</sub>	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, before calibration		±0.2		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, after calibration		±0.1		dB
ATT <sub>phase-err</sub>	DSA Gain Steps Phase accuracy, any 8dB range	f <sub>out</sub> = 850MHz <sup>(2)</sup>		±1		deg
		f <sub>out</sub> = 1800MHz <sup>(2)</sup>		±1		deg
		f <sub>out</sub> = 2600MHz <sup>(2)</sup>		±1		deg
		f <sub>out</sub> = 3500MHz <sup>(2)</sup>		±1		deg
		f <sub>out</sub> = 4900MHz <sup>(2)</sup>		±1		deg
		f <sub>out</sub> = 8100MHz <sup>(2)</sup>		±2		deg
G <sub>flat</sub>	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F <sub>out</sub> < 4.9G		1.2		

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion, 2 tones at $f_{\text{IF}} \pm 10\text{ MHz}$	$f_{\text{out}} = 850\text{MHz}$ , -7dBFS each tone		-66		dBc
		$f_{\text{out}} = 1800\text{MHz}$ , -7dBFS each tone		-63		dBc
		$f_{\text{out}} = 2600\text{MHz}$ , -7dBFS each tone		-62		dBc
		$f_{\text{out}} = 3500\text{MHz}$ , -7dBFS each tone		-61		dBc
		$f_{\text{out}} = 4900\text{MHz}$ , -7dBFS each tone		-57		dBc
		$f_{\text{out}} = 8100\text{MHz}$ , -7dBFS each tone		-55		dBc
		$f_{\text{out}} = 9600\text{MHz}$ , -7dBFS each tone		-52		dBc
		$f_{\text{out}} = 850\text{MHz}$ , -13dBFS each tone		-74		dBc
		$f_{\text{out}} = 1800\text{MHz}$ , -13dBFS each tone		-71		dBc
		$f_{\text{out}} = 2501\text{MHz}$ , -12dBFS each tone		-67	-60	dBc
		$f_{\text{out}} = 2600\text{MHz}$ , -13dBFS each tone		-73		dBc
		$f_{\text{out}} = 3500\text{MHz}$ , -13dBFS each tone		-72		dBc
		$f_{\text{out}} = 4900\text{MHz}$ , -13dBFS each tone		-68		dBc
		$f_{\text{out}} = 8100\text{MHz}$ , -13dBFS each tone		-64		dBc
$f_{\text{out}} = 9600\text{MHz}$ , -13dBFS each tone		-68		dBc		
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		51		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		52		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		42		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		44		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		46		dBc
$f_{\text{S}}/2 - f_{\text{OUT}}$	Interleaving Image	$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode		-52		dBc
		$f_{\text{DAC}} = 8847.36\text{ MSPS}$ , interleave mode		-46		dBc
		$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode		-42		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-49		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-48		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-47		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 850\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 1800\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-64		dBc
		$f_{\text{out}} = 2600\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-45		dBc
		$f_{\text{out}} = 3500\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-57		dBc
		$f_{\text{out}} = 4900\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-58		dBc
		$f_{\text{out}} = 8100\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 9600\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-62		dBc

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850 \text{ MHz}$		-62		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		-55		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		-57		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		-60		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		-54		dBc
		$f_{\text{out}} = 8100 \text{ MHz}$		-54		dBc
		$f_{\text{out}} = 9600 \text{ MHz}$		-56		dBc
		$f_{\text{out}} = 850 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
		$f_{\text{out}} = 1800 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-79		dBc
		$f_{\text{out}} = 2600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 3500 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 4900 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-78		dBc
		$f_{\text{out}} = 8100 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-82		dBc
		$f_{\text{out}} = 9600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	$f_{\text{out}} = 850 \text{ MHz}$		-81		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		-88		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		-86		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		-79		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		-86		dBc
		$f_{\text{out}} = 8100 \text{ MHz}$		-87		dBc
		$f_{\text{out}} = 9600 \text{ MHz}$		-85		dBc
		$f_{\text{out}} = 850 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-93		dBc
		$f_{\text{out}} = 1800 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-98		dBc
		$f_{\text{out}} = 2600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-84		dBc
		$f_{\text{out}} = 3500 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 4900 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 8100 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 9600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	$f_{\text{out}} = 850 \text{ MHz}$		69		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		79		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		77		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		75		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		76		dBc
		$f_{\text{out}} = 8100 \text{ MHz}$		61		dBc
		$f_{\text{out}} = 9600 \text{ MHz}$		64		dBc
$f_s/4$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-64		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-75		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}$		-67		dBFS
$f_s/2$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-49		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-48		dBFS
		$f_{\text{DAC}} = 11796.48 \text{ MSPS}$		-48		dBFS



Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3*f <sub>S</sub> /4	Fixed Spur	2nd Nyquist, f <sub>DAC</sub> = 5898.24MSPS		-76		dBFS
		2nd Nyquist, f <sub>DAC</sub> = 8847.36MSPS		-89		dBFS
		2nd Nyquist, f <sub>DAC</sub> = 11796.48MSPS		-63		dBFS
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 0.85 GHz	Atten=0dB, Pout=-13dBFS		-68.5		dBc
		Atten=20dB, Pout=-13dBFS		-67.2		dBc
		Atten=28dB, Pout=-13dBFS		-64.5		dBc
		Atten=39dB, Pout=-13dBFS		-53.9		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 1.8425 GHz	Atten=0dB, Pout=-13dBFS		-70.7		dBc
		Atten=20dB, Pout=-13dBFS		-68.3		dBc
		Atten=28dB, Pout=-13dBFS		-62.9		dBc
		Atten=39dB, Pout=-13dBFS		-52.0		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 2.6 GHz	Atten=0dB, Pout=-13dBFS		-71		dBc
		Atten=20dB, Pout=-13dBFS		-68		dBc
		Atten=28dB, Pout=-13dBFS		-62		dBc
		Atten=39dB, Pout=-13dBFS		-51.3		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 3.5 GHz	Atten=0dB, Pout=-13dBFS		-70		dBc
		Atten=20dB, Pout=-13dBFS		-67		dBc
		Atten=28dB, Pout=-13dBFS		-60		dBc
		Atten=39dB, Pout=-13dBFS		-49.8		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 4.9 GHz	Atten=0dB, Pout=-13dBFS		-68.8		dBc
		Atten=20dB, Pout=-13dBFS		-65.9		dBc
		Atten=28dB, Pout=-13dBFS		-60.6		dBc
		Atten=39dB, Pout=-13dBFS		-49.5		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 2.6 GHz	Atten=0dB, Pout=-13dBFS		-65		dBc
		Atten=20dB, Pout=-13dBFS		-62		dBc
		Atten=20dB, Pout=-13dBFS		-55		dBc
		Atten=39dB, Pout=-13dBFS		-44.3		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 3.5 GHz	Atten=0dB, Pout=-13dBFS		-64		dBc
		Atten=20dB, Pout=-13dBFS		-59		dBc
		Atten=28dB, Pout=-13dBFS		-52		dBc
		Atten=39dB, Pout=-13dBFS		-41.1		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 4.9 GHz	Atten=0dB, Pout=-13dBFS		-64.1		dBc
		Atten=20dB, Pout=-13dBFS		-60.4		dBc
		Atten=28dB, Pout=-13dBFS		-53.5		dBc
		Atten=39dB, Pout=-13dBFS		-42.5		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 8.1 GHz	Atten=0dB, Pout=-13dBFS		-58		dBc
		Atten=20dB, Pout=-13dBFS		-53		dBc
		Atten=28dB, Pout=-13dBFS		-46		dBc
		Atten=39dB, Pout=-13dBFS		-36		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 9.6 GHz	Atten=0dB, Pout=-13dBFS		-57		dBc
		Atten=20dB, Pout=-13dBFS		-50		dBc
		Atten=28dB, Pout=-13dBFS		-42		dBc
		Atten=39dB, Pout=-13dBFS		-31		dBc

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	$F_{\text{out}} = 0.85\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.16		%
		$F_{\text{out}} = 1.8425\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.29		%
		$F_{\text{out}} = 2.6\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.28		%
		$F_{\text{out}} = 3.5\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.38		%
		$F_{\text{out}} = 4.9\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.43		%
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 0.85\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-156		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-151		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-145		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-134		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 1.8\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-158		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-152		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-146		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-135		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-157		dBFS/ Hz
		Atten=20dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-151		dBFS/ Hz
		Atten=28dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-144		dBFS/ Hz
		Atten=39dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , $P_{\text{out}} = -13\text{dBFS}$		-133		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $F_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, $P_{\text{out}} = -13\text{dBFS}$		-158		dBFS/ Hz
		Atten=20dB, $P_{\text{out}} = -13\text{dBFS}$		-150		dBFS/ Hz
		Atten=28dB, $P_{\text{out}} = -13\text{dBFS}$		-143		dBFS/ Hz
		Atten=39dB, $P_{\text{out}} = -13\text{dBFS}$		-132		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $F_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, $P_{\text{out}} = -13\text{dBFS}$		-155		dBFS/ Hz
		Atten=20dB, $P_{\text{out}} = -13\text{dBFS}$		-148		dBFS/ Hz
		Atten=28dB, $P_{\text{out}} = -13\text{dBFS}$		-141		dBFS/ Hz
		Atten=39dB, $P_{\text{out}} = -13\text{dBFS}$		-130		dBFS/ Hz

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD <sub>dBFS</sub>	Noise Spectral Density 50MHz offset $F_{\text{out}} = 8.1\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-149		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-141		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-130		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 50MHz offset $F_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-148		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-144		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-137		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-126		dBFS/ Hz
S22	Output Return Loss, <6GHz, +/- fc * 10%	with matching		-17		dB
	Output Return Loss, >8GHz, +/- fc * 10%	with matching		-13		dB
Isolation	Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT <sup>(1)</sup>	$f_{\text{out}} = 900\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-49		dB
		$f_{\text{out}} = 1850\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-59		dB
		$f_{\text{out}} = 2600\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-64		dB
		$f_{\text{out}} = 3500\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-66		dB
		$f_{\text{out}} = 4900\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-60		dB
		$f_{\text{out}} = 900\text{ MHz}$ , $f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode		-90		dB
		$f_{\text{out}} = 1850\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-91		dB
		$f_{\text{out}} = 2600\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-93		dB
		$f_{\text{out}} = 3500\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-94		dB
		$f_{\text{out}} = 4900\text{ MHz}$ , $f_{\text{DAC}} =$ 8847.36MSPS, straight mode		-83		dB
		$f_{\text{out}} = 8100\text{ MHz}$		-47		dB
		$f_{\text{out}} = 9600\text{ MHz}$		-60		dB
	Far Channel: 1/2TXOUT to 3/4TXOUT	$f_{\text{out}} = 8100\text{ MHz}$		-80		dB

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN <sub>TXADD</sub>	Additive Phase Noise External Clock Mode <sup>(3)</sup>	$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{Hz}$		-88		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 1\text{kHz}$		-102		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 10\text{kHz}$		-110		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{kHz}$		-123		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 1\text{MHz}$		-136		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 10\text{MHz}$		-143		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{MHz}$		-146		dBc/Hz

- (1) Measured with differential 50 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.
- (2) After DSA calibration procedure
- (3) Single side band, input clock phase noise subtracted.

## 4.6 RF ADC Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC <sub>RES</sub>	ADC resolution			14		bits
F <sub>ADC</sub>	ADC Sample Rate		1.5		3	GSPS
F <sub>RFin_MAX</sub>	RF input frequency range	Requires PCB matching based on frequency range		12000		MHz
F <sub>RFin_MIN</sub>	RF input frequency range	Requires PCB matching based on frequency range		5		MHz
P <sub>FS_CW,min</sub>	Min Full scale input power, at device pins (1)	$f_{\text{IN}} = 830\text{ MHz}$ , DSA=0dB		-2.9		dBm
		$f_{\text{IN}} = 1760\text{ MHz}$ , DSA=0dB		-2.8		dBm
		$f_{\text{IN}} = 2610\text{ MHz}$ , DSA=0dB		-1.8		dBm
		$f_{\text{IN}} = 3610\text{ MHz}$ , DSA=0dB		-0.4		dBm
		$f_{\text{IN}} = 4910\text{ MHz}$ , DSA=0dB		0.1		dBm
		$f_{\text{IN}} = 8150\text{ MHz}$ , DSA=0dB		2.1		dBm
		$f_{\text{IN}} = 9610\text{ MHz}$ , DSA=0dB		4.3		dBm
P <sub>FS_CW,MAX</sub>	MAX Full scale input power - reliability limited, at device pins	$f_{\text{IN}} = 830\text{ MHz}$ , DSA = 20dB		16.7		dBm
		$f_{\text{IN}} = 1760\text{ MHz}$ , DSA = 20dB		17.0		dBm
		$f_{\text{IN}} = 2610\text{ MHz}$ , DSA = 20dB		18		dBm
		$f_{\text{IN}} = 3610\text{ MHz}$ , DSA = 20dB		18.5		dBm
		$f_{\text{IN}} = 4910\text{ MHz}$ , DSA = 20dB		19.3		dBm
		$f_{\text{IN}} = 8150\text{ MHz}$ , DSA = 20dB		21.3		dBm
		$f_{\text{IN}} = 9610\text{ MHz}$ , DSA = 20dB		23.5		dBm
S11	Input Return Loss	with matching network		-12		dB
ATT <sub>range</sub>	DSA Attenuation range			25		dB
ATT <sub>step</sub>	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), F <sub>in</sub> =3610MHz, after calibration		±0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	F <sub>in</sub> =3610MHz, after calibration		±0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	F <sub>in</sub> =4910MHz, after calibration		±1.8		deg

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Density (small signal)	$f_{\text{IN}} = 830\text{ MHz}$ , DSA = 3dB <sup>(3)</sup>		-155.2		dBFS/Hz
		$f_{\text{IN}} = 1760\text{ MHz}$ , DSA = 3dB <sup>(3)</sup>		-155.0		dBFS/Hz
		$f_{\text{IN}} = 2610\text{ MHz}$ , DSA = 3dB <sup>(3)</sup>		-154.4		dBFS/Hz
		$f_{\text{IN}} = 3610\text{ MHz}$ , DSA = 3dB <sup>(3)</sup>		-154.1		dBFS/Hz
		$f_{\text{IN}} = 4910\text{ MHz}$ , DSA = 3dB <sup>(3)</sup>		-155.1		dBFS/Hz
		$f_{\text{IN}} = 8150\text{ MHz}$ , DSA = 3dB <sup>(3)</sup>		-150		dBFS/Hz
		$f_{\text{IN}} = 9610\text{ MHz}$ , DSA = 3dB <sup>(3)</sup>		-151		dBFS/Hz
		$f_{\text{IN}} = 830\text{ MHz}$ , 3<=Atten<=22		-156.0		dBFS/Hz
		$f_{\text{IN}} = 1760\text{ MHz}$ , 3<=Atten<=25		-155.8		dBFS/Hz
		$f_{\text{IN}} = 2610\text{ MHz}$ , 3<=Atten<=25		-155.7		dBFS/Hz
		$f_{\text{IN}} = 3610\text{ MHz}$ , 3<=Atten<=25		-155.4		dBFS/Hz
		$f_{\text{IN}} = 4910\text{ MHz}$ , 3<=Atten<=25		-155.8		dBFS/Hz
		$f_{\text{IN}} = 8150\text{ MHz}$ , 3<=Atten<=25		-152.5		dBFS/Hz
		$f_{\text{IN}} = 9610\text{ MHz}$ , 3<=Atten<=25		-152.5		dBFS/Hz
NF <sub>min</sub>	Noise Figure min DSA Atten=0 - 3dB	$f_{\text{IN}} = 830\text{ MHz}$		19.1		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		19.0		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		20.9		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		22.8		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		22.4		dB
		$f_{\text{IN}} = 8150\text{ MHz}$		27.3		dB
		$f_{\text{IN}} = 9610\text{ MHz}$		30		dB
NF	Noise Figure DSA Atten=4dB	$f_{\text{IN}} = 830\text{ MHz}$ <sup>(4)</sup>		20.0		dB
		$f_{\text{IN}} = 1760\text{ MHz}$ <sup>(4)</sup>		20.6		dB
		$f_{\text{IN}} = 2610\text{ MHz}$ <sup>(4)</sup>		21.9		dB
		$f_{\text{IN}} = 3610\text{ MHz}$ <sup>(4)</sup>		23.5		dB
		$f_{\text{IN}} = 4910\text{ MHz}$ <sup>(4)</sup>		22.3		dB
		$f_{\text{IN}} = 8150\text{ MHz}$ <sup>(4)</sup>		27.9		dB
		$f_{\text{IN}} = 9610\text{ MHz}$ <sup>(4)</sup>		30.7		dB
NF <sub>max</sub>	Noise Figure DSA Atten=20dB	$f_{\text{IN}} = 830\text{ MHz}$		34.7		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		35.2		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		36.0		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		37.3		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		37.6		dB
		$f_{\text{IN}} = 8150\text{ MHz}$		42.8		dB
		$f_{\text{IN}} = 9610\text{ MHz}$		45		dB

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3 <sup>rd</sup> order intermodulation 2 tones at at $f_{\text{IN}} \pm 10\text{MHz}$ -7dBFS each tone	$f_{\text{IN}} = 840\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-82		dBc
		$f_{\text{IN}} = 1770\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-84		dBc
		$f_{\text{IN}} = 2610\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-74		dBc
		$f_{\text{IN}} = 3610\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-77		dBc
		$f_{\text{IN}} = 4920\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-76		dBc
		$f_{\text{IN}} = 8150\text{ MHz}, 3 \leq \text{Atten} \leq 12$ , 25MHz tone spacing		-55		dBc
		$f_{\text{IN}} = 9610\text{ MHz}, 3 \leq \text{Atten} \leq 12$ , 25MHz tone spacing		-60		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, $A_{\text{IN}} = -3$ dBFS	$f_{\text{IN}} = 830\text{ MHz}$		88		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		81		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		84		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		79		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		78		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		71		dBFS
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -3\text{ dBFS}^{(2)}$	$f_{\text{IN}} = 830\text{ MHz}$		-86		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-91		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-87		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-84		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-70		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -3\text{ dBFS}$	$f_{\text{IN}} = 830\text{ MHz}$		-80		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-85		dBFS
		$f_{\text{IN}} = 2501\text{ MHz}$		-80	-58	dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-85		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-75		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-70		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -3\text{ dBFS}$	$f_{\text{IN}} = 830\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-81		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-84		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-82		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-78		dBFS

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious Free Dynamic Range $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830\text{ MHz}$		89		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		89		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		90		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		90		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		83		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		80		dBFS
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830\text{ MHz}$ , with board trim		-79		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$ , with board trim		-102		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$ , with board trim		-100		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$ , with board trim		-101		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$ , with board trim		-99		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$ , with board trim		-107		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-98		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-97		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-94		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-100		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830\text{ MHz}$		-89		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-89		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-83		dBFS
RX-RX Isolation	Near Channel: 1RXIN to 2RXIN 3RXIN to 4RXIN	$f_{\text{IN}} = 830\text{ MHz}$		-77		dBc
		$f_{\text{IN}} = 1760\text{ MHz}$		-71		dBc
		$f_{\text{IN}} = 2610\text{ MHz}$		-74		dBc
		$f_{\text{IN}} = 3610\text{ MHz}$		-77		dBc
		$f_{\text{IN}} = 4910\text{ MHz}$		-65		dBc
		$f_{\text{IN}} = 8150\text{ MHz}$		-64		dBc
TX-FB Isolation	Near Channel: 2TXOUT to 1FBIN 4TXOUT to 2FBIN	$f_{\text{IN}} = 830\text{ MHz}$		-84		dBc
		$f_{\text{IN}} = 1760\text{ MHz}$		-88		dBc
		$f_{\text{IN}} = 2610\text{ MHz}$		-85		dBc
		$f_{\text{IN}} = 3610\text{ MHz}$		-75		dBc
		$f_{\text{IN}} = 4910\text{ MHz}$		-82		dBc
		$f_{\text{IN}} = 8150\text{ MHz}$		-71		dBc
		$f_{\text{IN}} = 9610\text{ MHz}$		-69		dBc



Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1474.56MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX-RX Isolation	Far Channel: 2TXOUT to 1RXIN 4TXOUT to 3RXIN	$f_{\text{IN}} = 830 \text{ MHz}$		-86		dBc
		$f_{\text{IN}} = 1760 \text{ MHz}$		-87		dBc
		$f_{\text{IN}} = 2610 \text{ MHz}$		-91		dBc
		$f_{\text{IN}} = 3610 \text{ MHz}$		-83		dBc
		$f_{\text{IN}} = 4910 \text{ MHz}$		-82		dBc
		$f_{\text{IN}} = 8150 \text{ MHz}$		-68		dBc
		$f_{\text{IN}} = 9610 \text{ MHz}$		-68		dBc

- (1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
- (2) NLE correction of HD2
- (3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
- (4) NF increase 1dB per DSA 1dB above DSA = 3dB

#### 4.7 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T<sub>A,MIN</sub> = -40°C to T<sub>J,MAX</sub> = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f<sub>DAC</sub> = f<sub>VCO</sub>, f<sub>OUT</sub> = f<sub>DAC</sub>/4, normalized to f<sub>VCO</sub>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>VCO1</sub>	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f <sub>VCO2</sub>	VCO2 min frequency				8.8	GHz
	VCO2 max frequency		9.1			GHz
f <sub>VCO3</sub>	VCO3 min frequency				9.7	GHz
	VCO3 max frequency		10.24			GHz
f <sub>VCO4</sub>	VCO4 min frequency				11.6	GHz
	VCO4 max frequency		12.08			GHz
DIV <sub>DAC</sub>	DAC sample rate divider			1, 2 or 3		
DIV <sub>FBAD</sub> C	ADC sample rate divider from DAC sample rate			1, 2, 3, 4, 6 or 8		
DIV <sub>RXAD</sub> C	ADC sample rate divider			1, 2, 3, 4, 6 or 8		
PN <sub>VCO</sub>	Closed Loop Phase Noise F <sub>PLL</sub> = 11.79848 GHz F <sub>REF</sub> =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		-141		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> =8.84736 GHz F <sub>REF</sub> =491.52MHz	600kHz		-114		dBc/Hz
		800kHz		-118		dBc/Hz
		1MHz		-120		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-135		dBc/Hz
		50MHz		-142		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> = 9.8403 GHz F <sub>REF</sub> =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-134		dBc/Hz
		50MHz		-140		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> = 7.86432GHz F <sub>REF</sub> =491.52MHz	600kHz		-116		dBc/Hz
		800kHz		-119		dBc/Hz
		1MHz		-122		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-136		dBc/Hz
		50MHz		-143		dBc/Hz
F <sub>rms</sub>	Clock PLL integrated phase error <sup>(1)</sup>	f <sub>PLL</sub> =11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f <sub>PLL</sub> =8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f <sub>PLL</sub> =9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f <sub>PDF</sub>	PFD frequency		100		500	MHz
F <sub>REF</sub>	Input clock minimum frequency			0.1		GHz
F <sub>REF</sub>	Input Clock maximum frequency			12		GHz
V <sub>CLKMIN</sub>	Input clock minimum level			0.6		Vppdiff

Typical values at TA = +25°C, full temperature range is T<sub>A,MIN</sub> = -40°C to T<sub>J,MAX</sub> = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f<sub>DAC</sub> = f<sub>VCO</sub>, f<sub>OUT</sub> = f<sub>DAC</sub>/4, normalized to f<sub>VCO</sub>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CLKMAX</sub>	Input Clock maximum level			1.8		V <sub>ppdiff</sub>
PN <sub>pll_flat</sub>	Normalized PLL flat Noise	f <sub>VCO</sub> = 11796.48MHz		-226.5		dBc/Hz
Coupling				AC Coupling Only		
	REFCLK input impedance <sup>(2)</sup>	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

- (1) Single Sideband, not including the reference clock contribution  
 (2) Refer to S11 data available from TI for impedance vs frequency

## 4.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T<sub>A,MIN</sub> = -40°C to T<sub>J,MAX</sub> = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CML SerDes Inputs [8:1]SRX+/-</b>						
V <sub>SRDIFF</sub>	SerDes Receiver Minimum Input Amplitude			100		mVpp
V <sub>SRDIFF</sub>	SerDes Receiver Maximum Input Amplitude			1200		mVpp
V <sub>SRCOM</sub>	SerDes Minimum Input Common Mode			0.5		V
V <sub>SRCOM</sub>	SerDes Maximum Input Common Mode			0.6		V
Z <sub>SRdiff</sub>	SerDes Internal Differential Termination <sup>(1)</sup>			115		Ω
F <sub>SerDes</sub>	SerDes Bit Rate	Minimum full rate mode		19		Gbps
F <sub>SerDes</sub>	SerDes Bit Rate	Maximum full rate mode		24.75		Gbps
F <sub>SerDes</sub>	SerDes Bit Rate	Minimum half rate mode		9.5		Gbps
F <sub>SerDes</sub>	SerDes Bit Rate	Maximum half rate mode		16.25		Gbps
F <sub>SerDes</sub>	SerDes Bit Rate	Minimum quarter rate mode		4.75		Gbps
F <sub>SerDes</sub>	SerDes Bit Rate	Maximum quarter rate mode		8.125		Gbps
	Insertion Loss Tolerance <sup>(2)</sup>	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance			0.42		UI
<b>CML SerDes Outputs [8:1]STX+/-</b>						
V <sub>STDIFF</sub>	SerDes Transmitter Minimum Output Amplitude	differential		500		mVpp
V <sub>STDIFF</sub>	SerDes Transmitter Maximum Output Amplitude	differential		1000		mVpp
V <sub>STCOM</sub>	SerDes Output Minimum Common Mode			0.5		V
V <sub>STCOM</sub>	SerDes Output Common Mode			0.6		V
Z <sub>STdiff</sub>	SerDes Output Impedance			115		Ω
TRF	Output rise and fall time	20-80%		8		ps
TEQS	Equalization range			7		dB
TTJ	Output total jitter			0.21		UI
<b>CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPIDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1</b>						
V <sub>IH</sub>	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
V <sub>IL</sub>	Low-Level Input Voltage			0.4×VDD1 P8GPIO		V
V <sub>OH</sub>	High-Level Output Voltage		VDD1P8G PIO-0.2			V
V <sub>OL</sub>	Low-Level Output Voltage				0.2	V
<b>Differential Inputs: SYSREF+/- Mode A</b>						
F <sub>SYSREFMAX</sub>	SYSREF Input Frequency Maximum			40		MHz
V <sub>SWINGSRMAX</sub>	SYSREF Input Swing Maximum			1.8		Vppdiff <sup>(3)</sup>
V <sub>SWINGSRMIN</sub>	SYSREF Input Swing Minimum	f <sub>REF</sub> < 500MHz		0.3		Vppdiff <sup>(3)</sup>
V <sub>SWINGSRMIN</sub>	SYSREF Input Swing Minimum	f <sub>REF</sub> > 500MHz		0.6		Vppdiff <sup>(3)</sup>
V <sub>COMSRMAX</sub>	SYSREF Input Common Mode Voltage Maximum			0.8		V
V <sub>COMSRMIN</sub>	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z <sub>T</sub>	Input termination	differential		108 <sup>(1)</sup>		Ω

Typical values at TA = +25°C, full temperature range is TA,MIN = -40°C to TJ,MAX = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CL	Input capacitance	Each pin to GND		0.5		pF
<b>LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-</b>						
V <sub>ICOM</sub>	Input Common Voltage			1.2		V
V <sub>ID</sub>	Differential Input Voltage swing			450		mVppdiff <sup>(3)</sup>
Z <sub>T</sub>	Input termination	differential		100		Ω
<b>LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-</b>						
V <sub>OCOM</sub>	Output Common Voltage			1.2		V
V <sub>OD</sub>	Differential Output Voltage swing			355		mVppdiff <sup>(3)</sup>

- (1) Default setting. SYSREF termination is programmable between nominally 100Ω, 150Ω and 300Ω
- (2) Loss tolerance is bump to bump from STX to SRX
- (3) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

#### 4.9 Power Supply Electrical Characteristics

Typical values at TA = +25°C, full temperature range is TA,MIN = -40°C to TJ,MAX = +110°C; TX Input Rate = 491.52MSPS, f<sub>DAC</sub> = 8847.36MSPS interleave mode; f<sub>ADC</sub> = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I <sub>VDD1P8</sub>	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4T2F - FDD FB 100% on, no RX TX/FB Rate: 491.52 Msps Single Band: 12x Int, FB 6x Dec f <sub>DAC</sub> = 5898.24 SPS f <sub>ADC</sub> = 2949.12MSPS f <sub>TX</sub> = 1.85 GHz 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1		948.2		mA	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			533.7		mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			77.3		mA	
I <sub>VDD1P2</sub>	Group 2A: VDD1P2FB + VDD1P2RX				299.4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC				804.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF				49.1		mA
I <sub>VDD0P9</sub>	Group 1A: DVDD0P9 + VDDT0P9				2041.3		mA
P <sub>diss</sub>	Power Dissipation				6027.1		mW
I <sub>VDD1P8</sub>	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 2: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Dual Band: 12x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps f <sub>DAC</sub> = 8847.36MSPS f <sub>ADC</sub> = 2949.12MSPS f <sub>OUT</sub> =f <sub>IN</sub> = 1.9, 2.6 GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1		820.4		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			735.2		mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			74.4		mA	
I <sub>VDD1P2</sub>	Group 2A: VDD1P2FB + VDD1P2RX				289.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC				822.0		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF				45.6		mA
I <sub>VDD0P9</sub>	Group 1A: DVDD0P9 + VDDT0P9				2263.8		mA
P <sub>diss</sub>	Power Dissipation				6359.2		mW

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{A,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 4T4R2F - FDD FB 100% on TX Dual Band: 12x Int, FB 6x Dec RX Dual Band: RX 24x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 11796.48\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = 1.85 + 2.15\text{GHz}$ $f_{\text{RX}} = 1.75 + 1.88\text{GHz}$ 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1	1668.6			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		965.1			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		77.6			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX		893.4			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		879.5			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		50.7			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		3826.9			mA
$P_{\text{diss}}$	Power Dissipation		10513.0			mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 4: 4T4R2F - FDD FB 100% on 7.5 GSPS DAC, 2.5 GSPS ADC Single Band: 15x Int, FB 5x Dec Dual Band: RX 20x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps $f_{\text{DAC}} = 7372.8\text{MSPS}$ $f_{\text{ADC}} = 2457.6\text{MSPS}$ $f_{\text{TX}} = 1.85 + 2.15\text{GHz}$ $f_{\text{RX}} = 1.75 + 1.88\text{GHz}$ 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-16-16-1	1611.5		
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8	694.5				mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0	72.8				mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX	768.5				mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC	940.5				mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF	45.5				mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9	3000.5				mA
$P_{\text{diss}}$	Power Dissipation	9087.4				mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps $f_{\text{DAC}} = 11796.48\text{MSPS}$ $f_{\text{ADC}} = 2949.12\text{MSPS}$ $f_{\text{TX}} = 3.5\text{GHz}$ $f_{\text{RX}} = 3.5\text{GHz}$ 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1		821.8		
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		808.5			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		77.4			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX		289.5			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		682.0			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		49.0			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		2123.3			mA
$P_{\text{diss}}$	Power Dissipation		6209.3			mW

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,MIN} = -40^\circ\text{C}$  to  $T_{J,MAX} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{DAC} = 8847.36\text{MSPS}$  interleave mode;  $f_{ADC} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7a: TDD 4T1FB (RX iin Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, non-interleave mode RX 3G : 368.64M. 16 bit, Standby Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		658.1		mA	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			431.1		mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			75.3		mA	
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			189.2		mA	
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1041.1		mA	
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			39.0		mA	
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9				2208.7		mA
$P_{diss}$	Power Dissipation				5607.0		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX			Mode 7b: TDD 4R (TX in Standby) TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, Standby RX 3G : 368.64M. 16 bit Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		789.5	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8	471.3				mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0	73.4				mA	
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX	599.3				mA	
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC	169.6				mA	
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF	39.1				mA	
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9		1645.3				mA
$P_{diss}$	Power Dissipation		4851.9				mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7c: TDD 4T4R1FB TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, 75% on RX 3G : 368.64M. 16 bit 25% on Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx				691.0	
$I_{VDD1P8}$	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			441.2		mA	
$I_{VDD1P8}$	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			74.8		mA	
$I_{VDD1P2}$	Group 2A: VDD1P2FB + VDD1P2RX			291.7		mA	
$I_{VDD1P2}$	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			823.2		mA	
$I_{VDD1P2}$	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			39.0		mA	
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9				2067.9		mA
$P_{diss}$	Power Dissipation				5418.2		mW

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Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{A,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7d: FDD 4T4R1FB TX 9G and FB 3G -16bit: 368.64M; DSA = 6dB, , non-interleave mode, RX 3G : 368.64M. 16 bit Serdes: 25gbps) -> 2 lanes for Rx/FB (lane shared) and 2lanes for Tx		1283.8		mA
$I_{\text{VDD1P8}}$	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			752.0		mA
$I_{\text{VDD1P8}}$	Group 3C: VDD1P8PLL + VDD1P8PLLCO			74.6		mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX			750.5		mA
$I_{\text{VDD1P2}}$	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1077.6		mA
$I_{\text{VDD1P2}}$	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			47.7		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			2695.5		mA
$P_{\text{diss}}$	Power Dissipation		8475.5		mW	
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 8: same configuration as mode 7, Sleep Mode. SLEEP pin is pull high.		20.3		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			292.8		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			12.6		mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX			4.6		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			54.3		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			15.3		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			313.1		mA
$P_{\text{diss}}$	Power Dissipation			956.8		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 9: 4T4R2F - FDD FB 100% on TX Single Band: 24x Int, FB 12x Dec RX Single Band: RX 24x TX/FB Rate 245.76 Msp RX Rate 122.88 Msp $f_{\text{DAC}} = 5898.24\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 0.85\text{ GHz}$ $f_{\text{RX}} = 0.8\text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-8-8-1		1593.2	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			840.6		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			77.3		mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX			905.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			817.7		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			52.1		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			2405.2		mA
$P_{\text{diss}}$	Power Dissipation			8814.3		mW



Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 10: 4T4R2F - FDD FB 100% on TX Single Band: 18x Int, FB 6x Dec RX Single Band: RX 12x TX/FB Rate 491.52 Msps RX Rate 245.76 Msps $f_{\text{DAC}} = 8847.36\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = 1.85\text{ GHz}$ $f_{\text{RX}} = 1.75\text{ GHz}$ 8/10 coding, 9.8304Gbps TX: 8-8-2-1, FB: 4-4-2-1, RX: 4-8-4-1  Mode 11a: TDD 4T1FB (RX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2  Mode 11b: TDD 4R (TX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2	1626.2			mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		976.4			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		74.6			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX		902.7			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		1111.9			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		48.0			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		3578.9			mA
$P_{\text{diss}}$	Power Dissipation		10515.0			mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 11a: TDD 4T1FB (RX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2  Mode 11b: TDD 4R (TX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2	800		
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8	840				mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0	73				mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX	190				mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC	1440				mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF	75				mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9	3070				mA
$P_{\text{diss}}$	Power Dissipation	8010				mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11b: TDD 4R (TX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2		750		
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8		890			mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0		72			mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX		610			mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC		280			mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF		72			mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9		2360			mA
$P_{\text{diss}}$	Power Dissipation		6460			mW

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Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$  interleave mode;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11c: TDD 4T4R1FB average TX/FB: 75%, RX 25% Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2		790		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			850		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			73		mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX			300		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1150		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			75		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			2890		mA
$P_{\text{diss}}$	Power Dissipation			7620		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX		Mode 11d: FDD 4T4R Single Band: 8x Int, RX uses FB TX/FB/RX Rate = 1474.56 Msps $f_{\text{DAC}} = 11796.48\text{ MSPS}$ $f_{\text{ADC}} = 2949.12\text{ MSPS}$ $f_{\text{TX}} = f_{\text{RX}} = 8\text{ GHz}$ 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 4-4-4-2		1260	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			940		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			73		mA
$I_{\text{VDD1P2}}$	Group 2A: VDD1P2FB + VDD1P2RX			630		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1480		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			78		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			4200		mA
$P_{\text{diss}}$	Power Dissipation			10640		mW

## 4.10 Timing Requirements

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
<b>Timing: SYSREF+/-</b>					
$t_{\text{s}}(\text{SYSREF})$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{\text{h}}(\text{SYSREF})$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
<b>Timing: Serial ports</b>					
$t_{\text{s}}(\text{SENB})$	Setup Time, SENB to Rising Edge of SCLK		15		ns
$t_{\text{h}}(\text{SENB})$	Hold Time, SENB after last Rising Edge of SCLK <sup>(1)</sup>		$5 + t_{\text{SCLK}}$		ns
$t_{\text{s}}(\text{SDIO})$	Setup Time, SDIO valid to Rising Edge of SCLK		15		ns
$t_{\text{h}}(\text{SDIO})$	Hold Time, SDIO valid after Rising Edge of SCLK		5		ns
$t_{\text{(SCLK)_W}}$	Minimum SCLK period: registers write		25		ns
$t_{\text{(SCLK)_R}}$	Minimum SCLK period: registers read		50		ns
$t_{\text{(SCLK)_R}}$	SCLK period: temp sensor <sup>(2)</sup>		1000		ns
$t_{\text{d}}(\text{data\_out})$	Minimum Data Output delay after Falling Edge of SCLK		0		ns
	Maximum Data Output delay after Falling Edge of SCLK		15		ns
$t_{\text{RESET}}$	Minimum RESETZ Pulse Width		1		ms

- (1) SDEN\ need to be held one more extra clock cycle with the last SCLK edge  
(2) Temp sensor requires a maximum of 1MHz SCLK cycle.

## 4.11 Switching Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

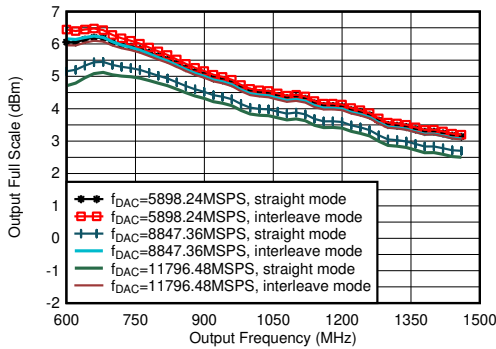
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TX Channel Latency</b>						
$t_{\text{JESD TX}}$	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles <sup>(1)</sup>
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
<b>RX Channel Latency</b>						
	SerDes Transmitter Analog Delay			3.6		ns
$t_{\text{JESD RX}}$	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles <sup>(1)</sup>
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
<b>FB Channel Latency</b>						
	SerDes Transmitter Analog Delay			3.6		ns
$t_{\text{JESD FB}}$	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation		151		interface clock cycles <sup>(1)</sup>
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation		177		

(1) Interface clock cycles is the period of the digital interface sample rate, e.g. 1GSPS = 1ns.

## 4.12 Typical Characteristics

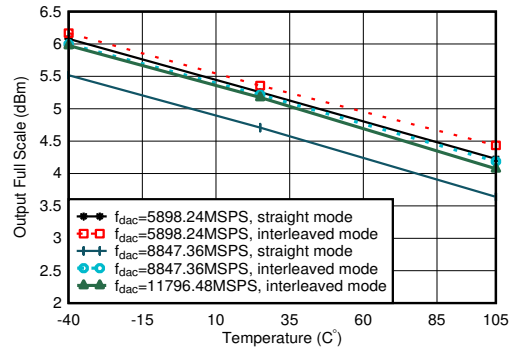
### 4.12.1 TX Typical Characteristics 800MHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



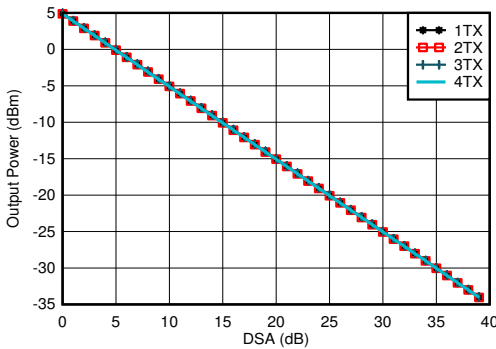
including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 0.8GHz matching

**Figure 4-1. TX Output Fullscale vs Output Frequency**



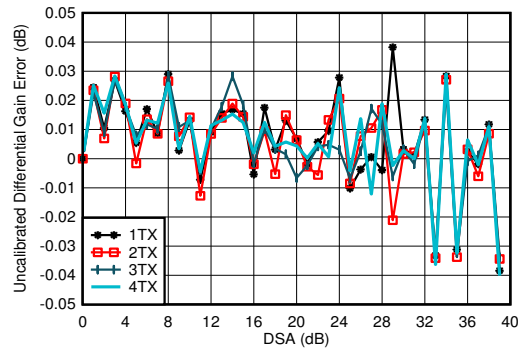
including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 0.8GHz matching

**Figure 4-2. TX Output Fullscale vs Temperature**



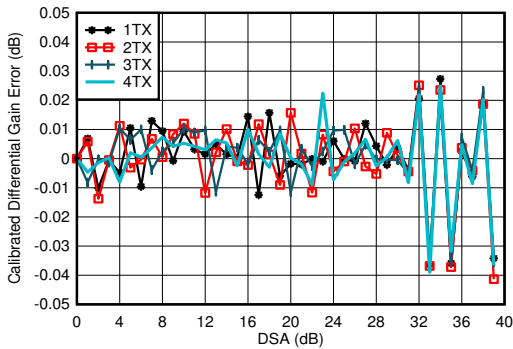
$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $A_{out} = -0.5\text{dBFS}$ , matching 0.8GHz

**Figure 4-3. TX Output Power vs DSA Setting and Channel at 0.85GHz**



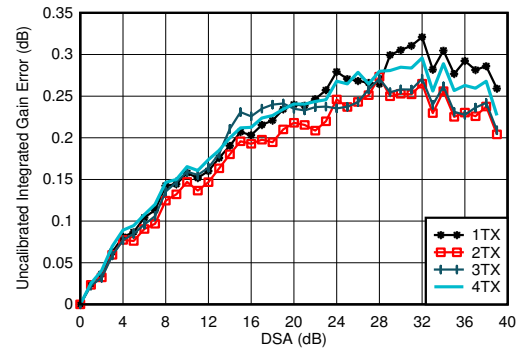
$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
Differential Gain Error =  $P_{OUT}(\text{DSA Setting} - 1) - P_{OUT}(\text{DSA Setting}) + 1$

**Figure 4-4. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85GHz**



$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
Differential Gain Error =  $P_{OUT}(\text{DSA Setting} - 1) - P_{OUT}(\text{DSA Setting}) + 1$

**Figure 4-5. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85GHz**

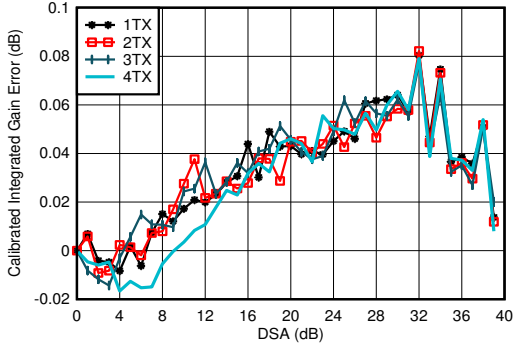


$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
Integrated Gain Error =  $P_{OUT}(\text{DSA Setting}) - P_{OUT}(\text{DSA Setting} = 0) + \text{DSA Settings}$

**Figure 4-6. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85GHz**

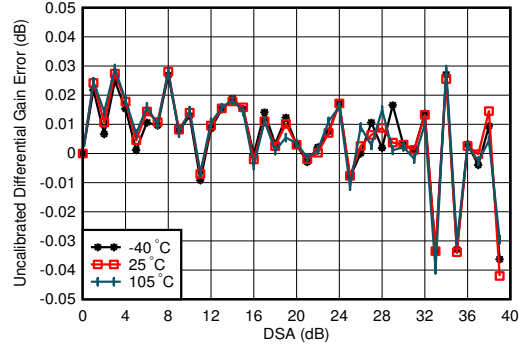
### 4.12.1 TX Typical Characteristics 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



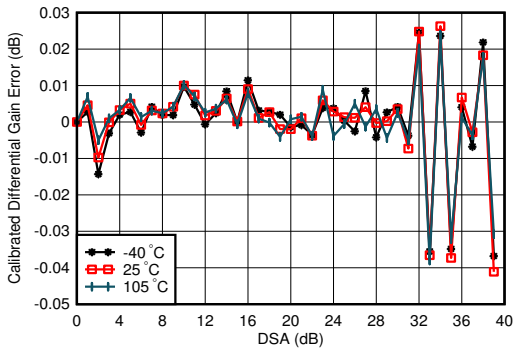
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

**Figure 4-7. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85GHz**



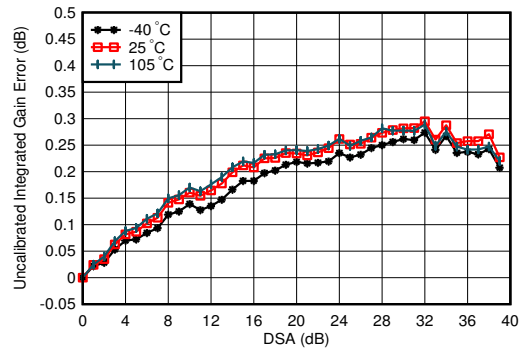
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-8. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85GHz**



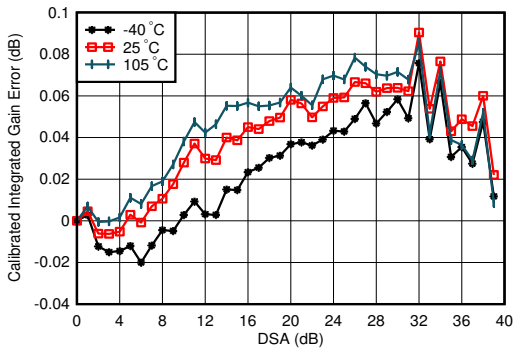
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-9. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85GHz**



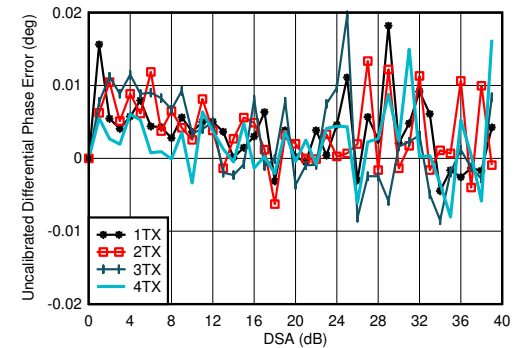
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

**Figure 4-10. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

**Figure 4-11. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85GHz**

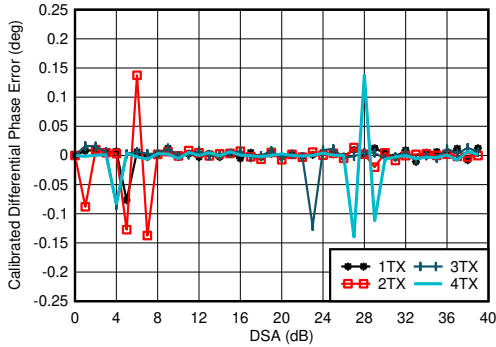


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-12. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85GHz**

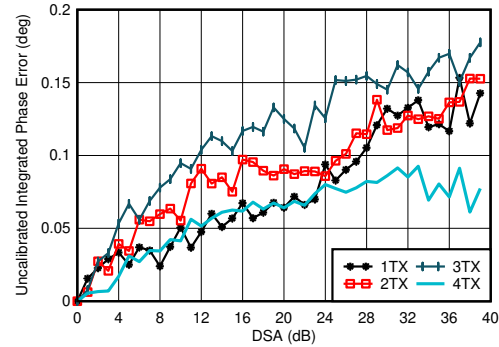
**4.12.1 TX Typical Characteristics 800MHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



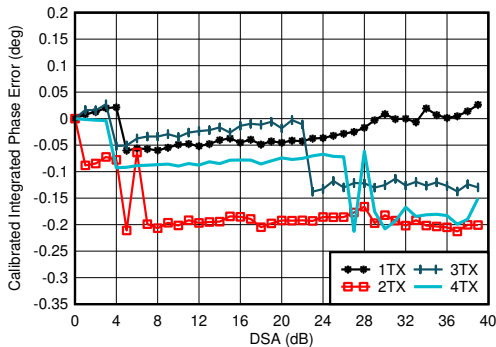
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
 Phase DNL spike may occur at any DSA setting.

**Figure 4-13. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85GHz**



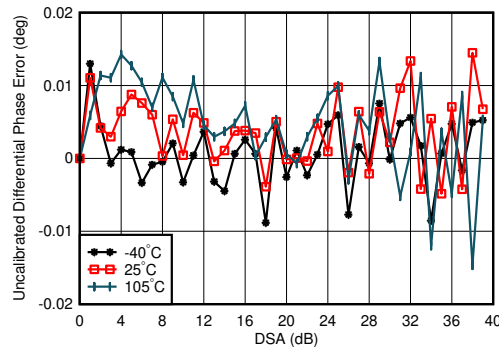
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 4-14. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 4-15. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85GHz**

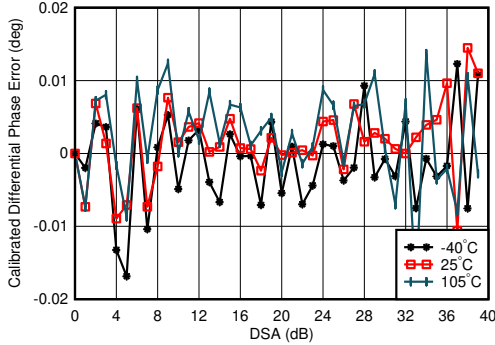


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-16. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85GHz**

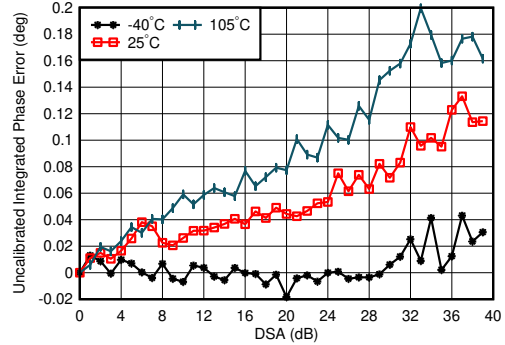
### 4.12.1 TX Typical Characteristics 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



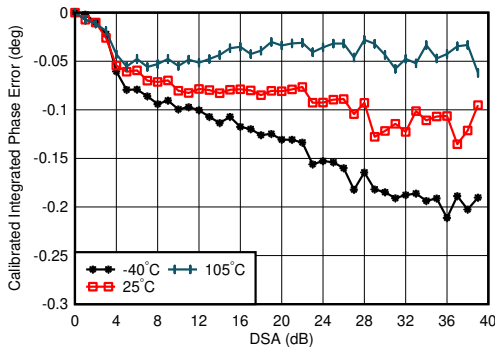
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz, channel with the median variation over DSA setting at 25°C  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-17. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85GHz**



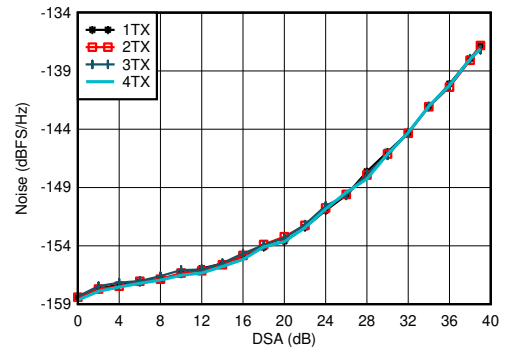
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 4-18. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz  
 Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 4-19. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85GHz**



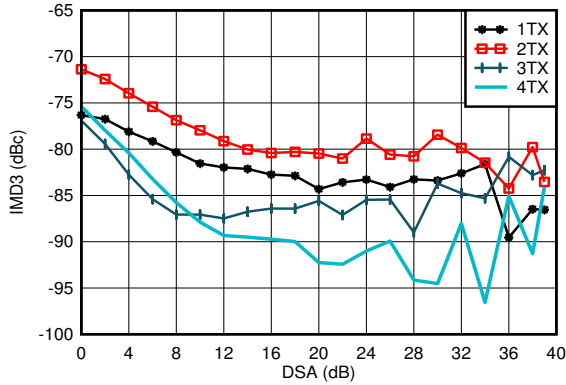
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 0.8GHz,  $P_{\text{OUT}} = -13\text{ dBFS}$

**Figure 4-20. TX Output Noise vs Channel and Attenuation at 0.85GHz**



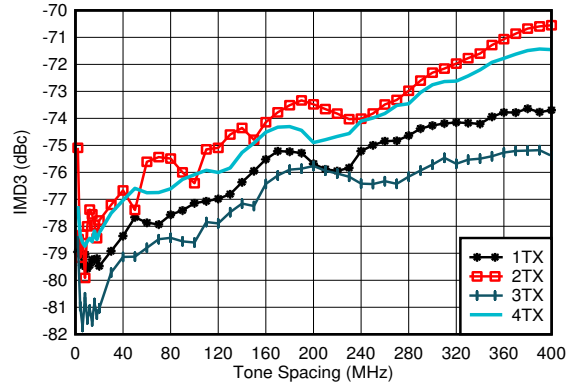
### 4.12.1 TX Typical Characteristics 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



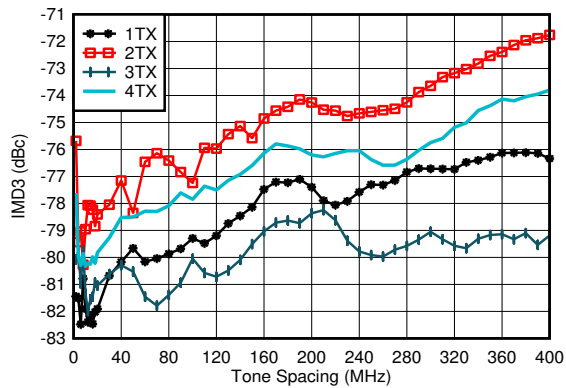
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 0.85\text{GHz}$ , matching at 0.8 GHz,  $-13\text{dBFS}$  each tone

**Figure 4-21. TX IMD3 vs DSA Setting at 0.85GHz**



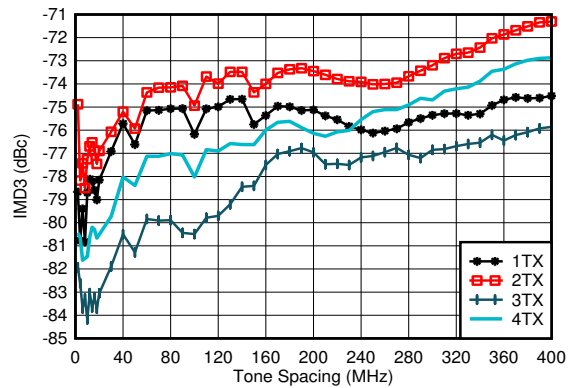
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85\text{GHz}$ , matching at 0.8GHz,  $-13\text{dBFS}$  each tone

**Figure 4-22. TX IMD3 vs Tone Spacing and Channel at 0.85GHz**



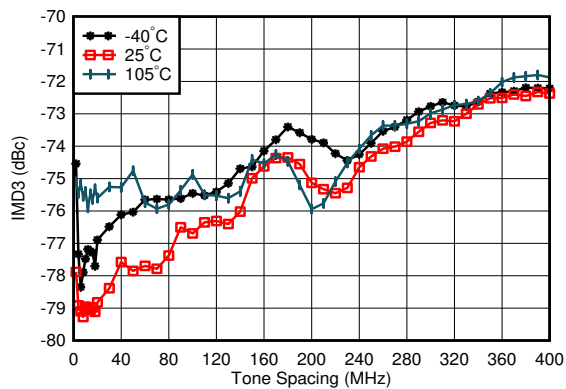
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85\text{GHz}$ , matching at 0.8GHz,  $-13\text{dBFS}$  each tone

**Figure 4-23. TX IMD3 vs Tone Spacing and Channel at 0.85GHz**



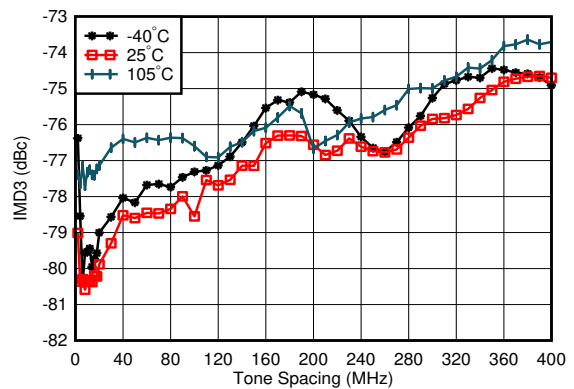
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode,  $f_{\text{CENTER}} = 0.85\text{GHz}$ , matching at 0.8GHz,  $-13\text{dBFS}$  each tone

**Figure 4-24. TX IMD3 vs Tone Spacing and Channel at 0.85GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85\text{GHz}$ , matching at 0.8GHz,  $-13\text{dBFS}$  each tone, worst channel

**Figure 4-25. TX IMD3 vs Tone Spacing and Temperature at 0.85GHz**



$\text{DAC} = 8847.3 \text{ MSPS}$ , straight mode,  $f_{\text{CENTER}} = 0.85\text{GHz}$ , matching at 0.8 GHz,  $-13\text{dBFS}$  each tone, worst channel

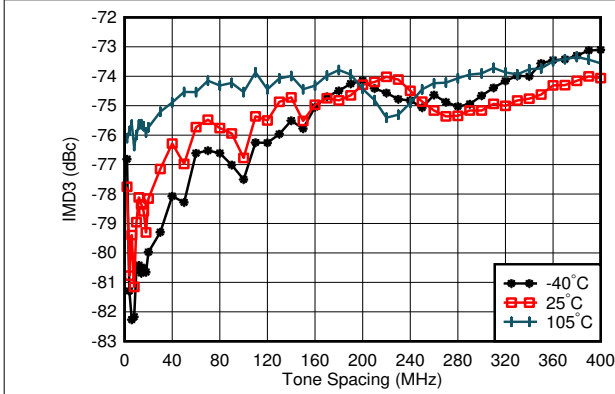
**Figure 4-26. TX IMD3 vs Tone Spacing and Temperature at 0.85GHz**

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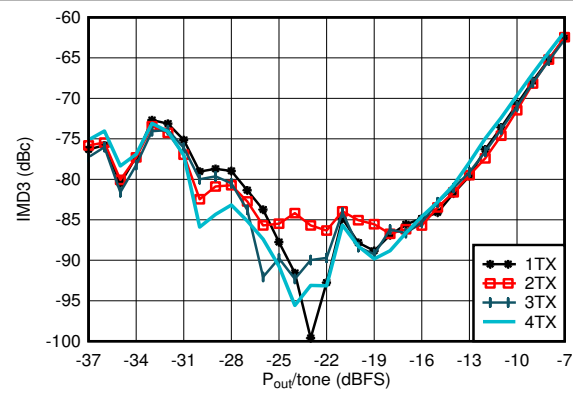
**4.12.1 TX Typical Characteristics 800MHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



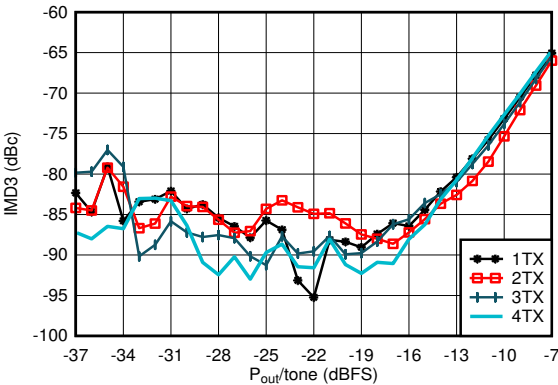
$f_{DAC} = 11796.48\text{MSPS}$ , straight mode,  $f_{CENTER} = 0.85\text{GHz}$ , matching at 0.8GHz, -13dBFS each tone, worst channel

**Figure 4-27. TX IMD3 vs Tone Spacing and Temperature at 0.85GHz**



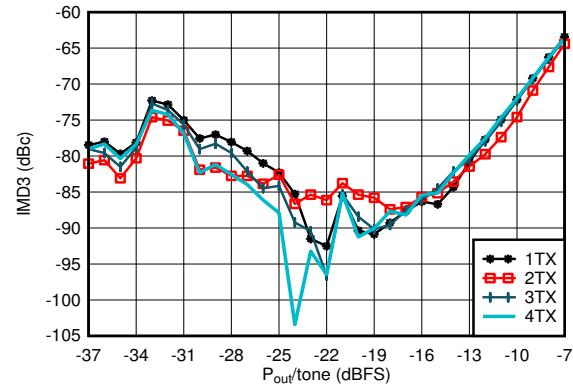
$f_{DAC} = 5898.24\text{MSPS}$ , straight mode,  $f_{CENTER} = 0.85\text{GHz}$ ,  $f_{SPACING} = 20\text{MHz}$ , matching at 0.8GHz

**Figure 4-28. TX IMD3 vs Digital Level at 0.85GHz**



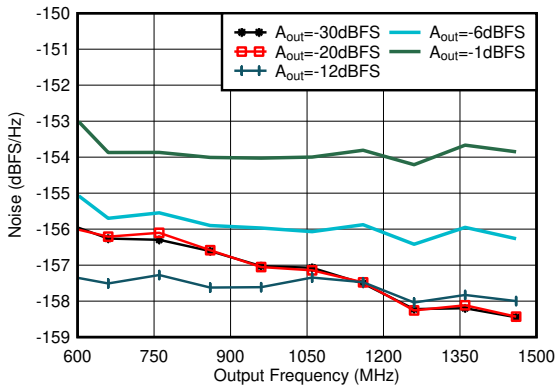
$f_{DAC} = 8847.36\text{MSPS}$ , straight mode,  $f_{CENTER} = 0.85\text{GHz}$ ,  $f_{SPACING} = 20\text{MHz}$ , matching at 0.8GHz

**Figure 4-29. TX IMD3 vs Digital Level at 0.85GHz**



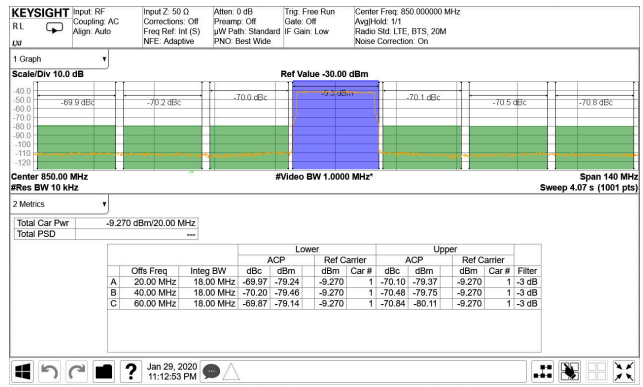
$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $f_{CENTER} = 0.85\text{GHz}$ ,  $f_{SPACING} = 20\text{MHz}$ , matching at 0.8GHz

**Figure 4-30. TX IMD3 vs Digital Level at 0.85GHz**



Matching at 2.6GHz, Single tone,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, 40MHz offset, DSA = 0dB

**Figure 4-31. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85GHz**

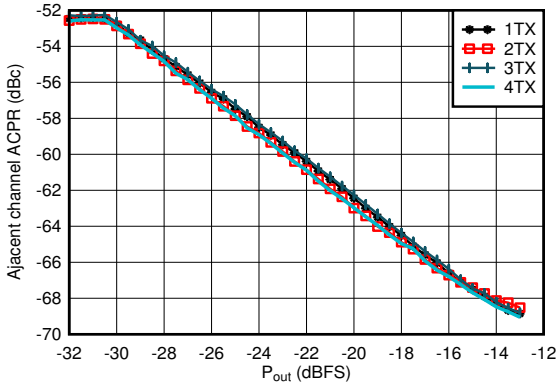


TM1.1,  $P_{OUT\_RMS} = -13\text{dBFS}$

**Figure 4-32. TX 20-MHz LTE Output Spectrum at 0.85 GHz**

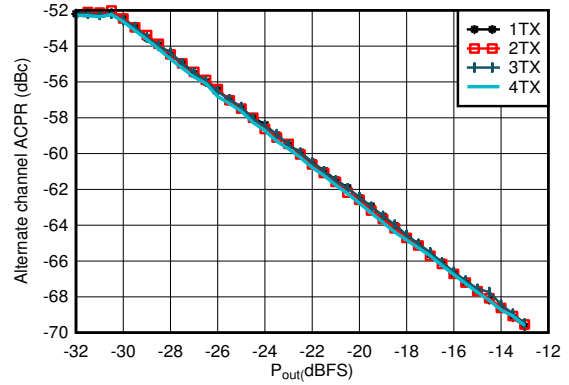
**4.12.1 TX Typical Characteristics 800MHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



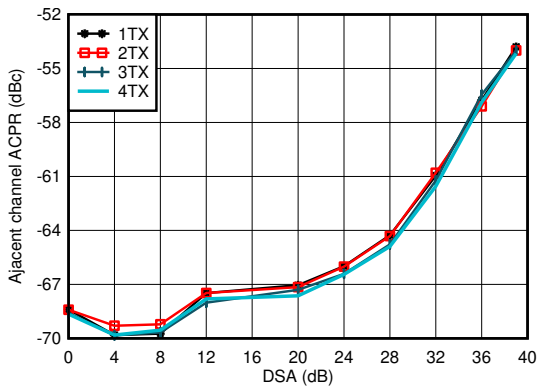
Matching at 0.8GHz, single carrier 20MHz BW TM1.1 LTE

**Figure 4-33. TX 20-MHz LTE ACPR vs Digital Level at 0.85GHz**



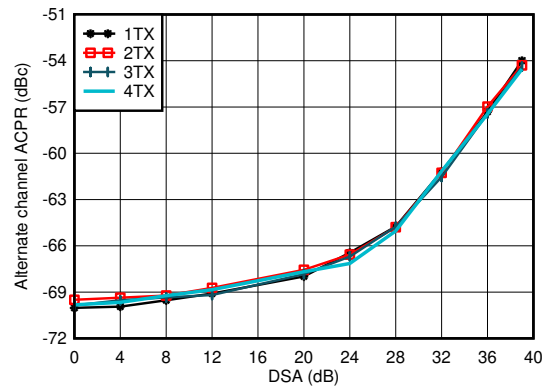
Matching at 0.8GHz, single carrier 20MHz BW TM1.1 LTE

**Figure 4-34. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85GHz**



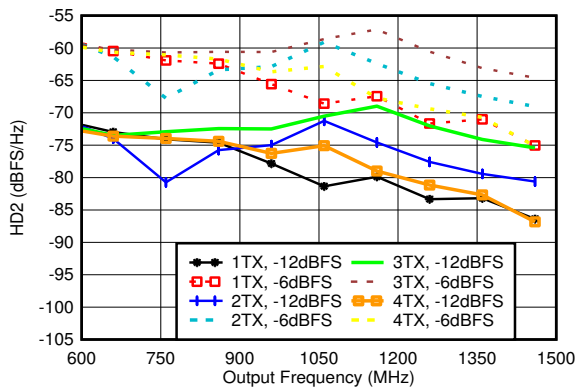
Matching at 0.8GHz, single carrier 20MHz BW TM1.1 LTE

**Figure 4-35. TX 20-MHz LTE ACPR vs DSA at 0.85GHz**



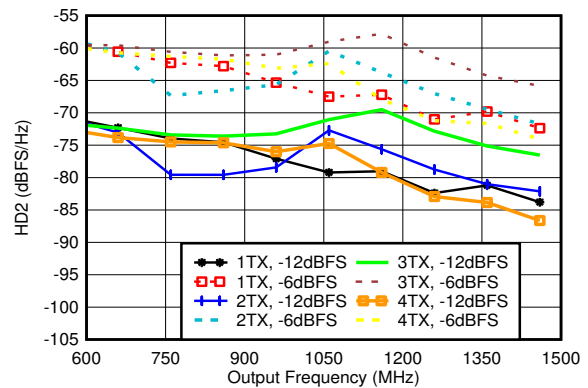
Matching at 0.8GHz, single carrier 20MHz BW TM1.1 LTE

**Figure 4-36. TX 20-MHz LTE alt-ACPR vs DSA at 0.85GHz**



Matching at 0.8GHz,  $f_{DAC} = 5898.2\text{ GSPS}$ , straight mode

**Figure 4-37. TX HD2 vs Digital Amplitude and Output Frequency at 0.85GHz**

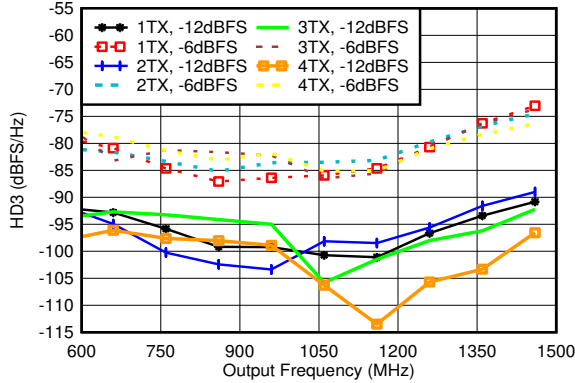


Matching at 0.8GHz,  $f_{DAC} = 8847.36\text{GSPS}$ , straight mode

**Figure 4-38. TX HD2 vs Digital Amplitude and Output Frequency at 0.85GHz**

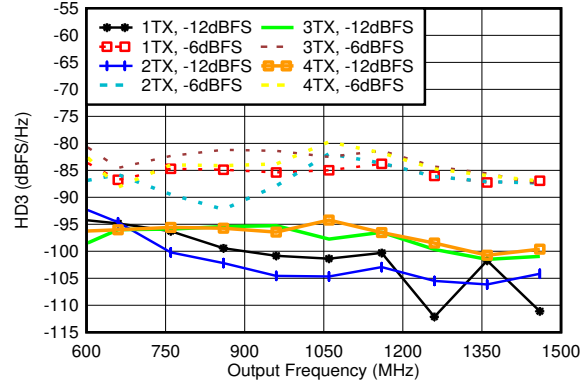
**4.12.1 TX Typical Characteristics 800MHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



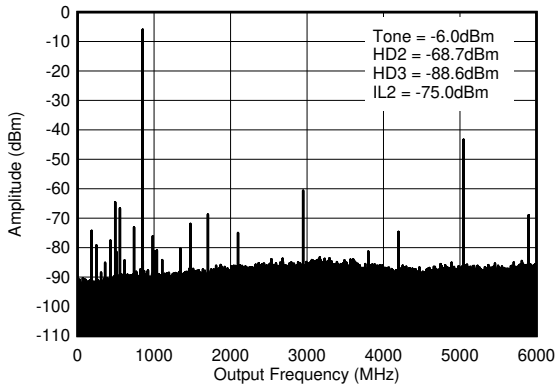
Matching at 0.8GHz,  $f_{DAC} = 5898.24\text{MSPS}$ , straight mode, normalized to output power at harmonic frequency

**Figure 4-39. TX HD3 vs Digital Amplitude and Output Frequency at 0.85GHz**



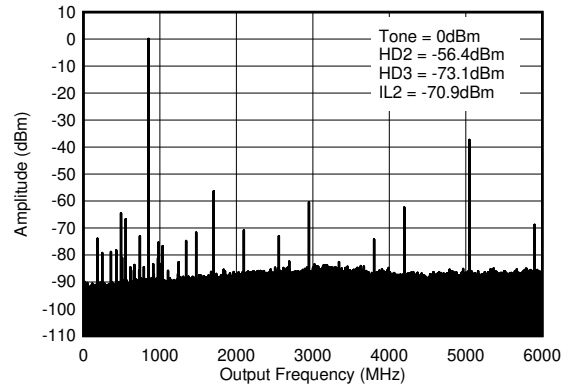
Matching at 0.8GHz,  $f_{DAC} = 8847.36\text{MSPS}$ , straight mode, normalized to output power at harmonic frequency

**Figure 4-40. TX HD3 vs Digital Amplitude and Output Frequency at 0.85GHz**



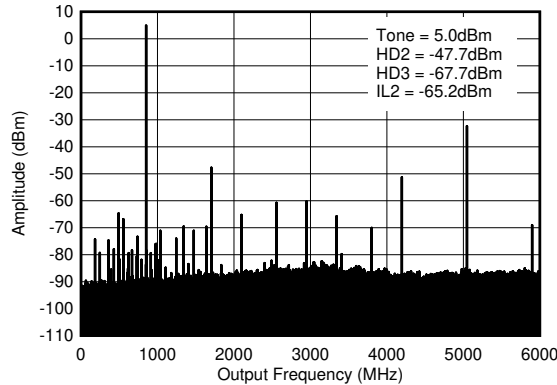
$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, 0.8GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{OUT}$ .

**Figure 4-41. TX Single Tone (-12 dBFS) Output Spectrum at 0.85GHz (0- $f_{DAC}$ )**



$f_{DAC} = 5898.2\text{MSPS}$ , interleave mode, 0.8GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{OUT}$ .

**Figure 4-42. TX Single Tone (-6dBFS) Output Spectrum at 0.85GHz (0- $f_{DAC}$ )**

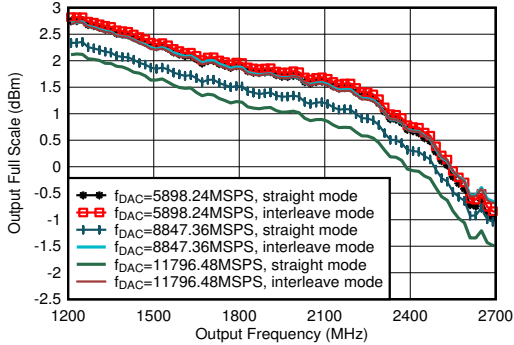


$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, 0.8GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{OUT}$ .

**Figure 4-43. TX Single Tone (-1dBFS) Output Spectrum at 0.85GHz (0- $f_{DAC}$ )**

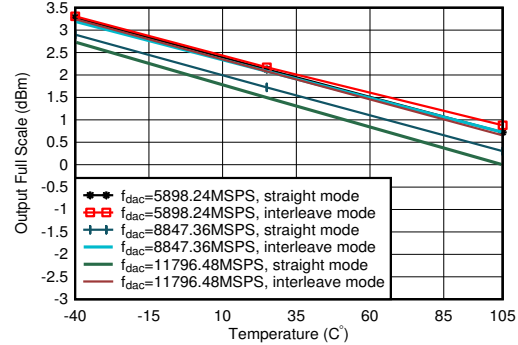
### 4.12.2 TX Typical Characteristics at 1.8GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated



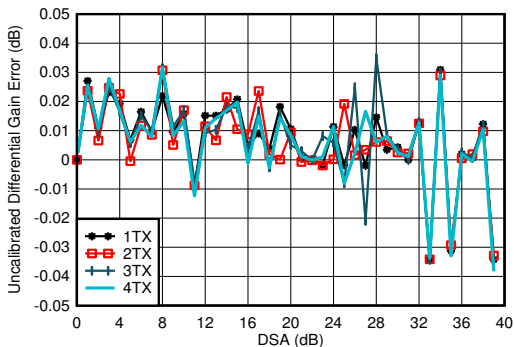
including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 1.8GHz matching

**Figure 4-44. TX Output Fullscale vs Output Frequency**



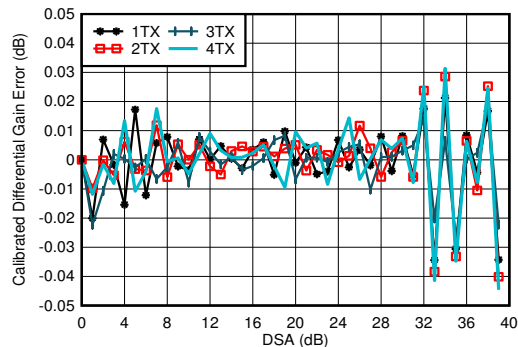
$A_{out} = -0.5\text{dBFS}$ , matching 1.8GHz

**Figure 4-45. TX Output Power vs Temperature at 1.8GHz**



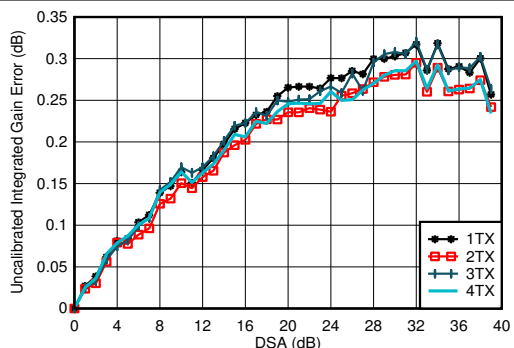
$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
Differential Gain Error =  $P_{OUT}(\text{DSA Setting} - 1) - P_{OUT}(\text{DSA Setting}) + 1$

**Figure 4-46. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 1.8GHz**



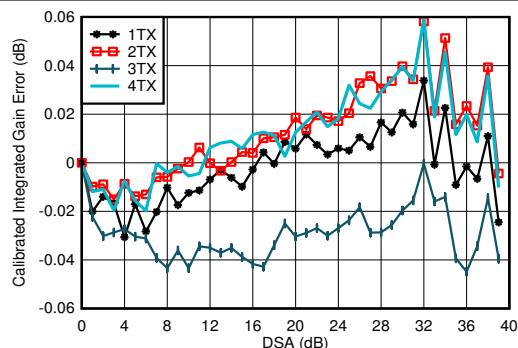
$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
Differential Gain Error =  $P_{OUT}(\text{DSA Setting} - 1) - P_{OUT}(\text{DSA Setting}) + 1$

**Figure 4-47. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 1.8GHz**



$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
Integrated Gain Error =  $P_{OUT}(\text{DSA Setting}) - P_{OUT}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-48. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 1.8GHz**

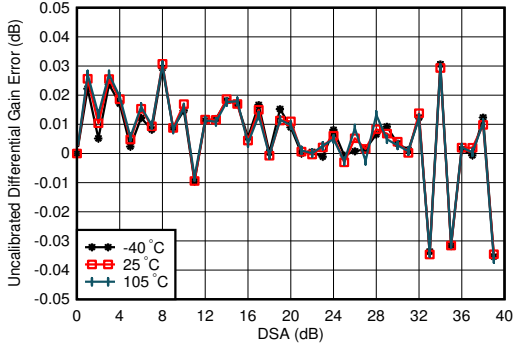


$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
Integrated Gain Error =  $P_{OUT}(\text{DSA Setting}) - P_{OUT}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-49. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 1.8GHz**

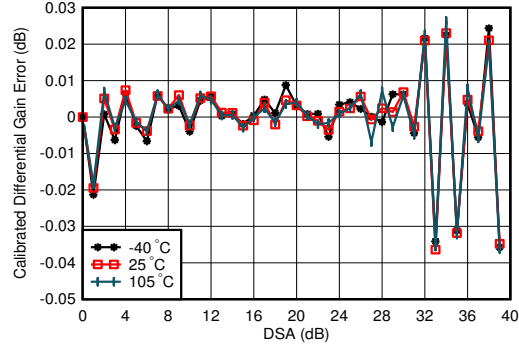
### 4.12.2 TX Typical Characteristics at 1.8GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



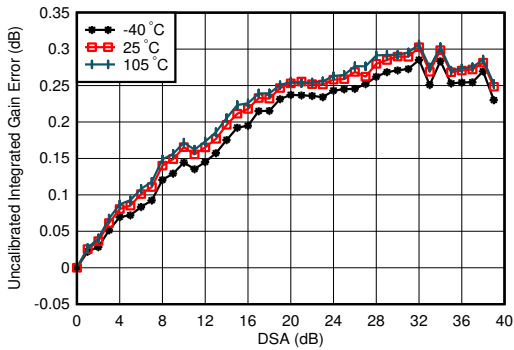
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-50. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 1.8GHz**



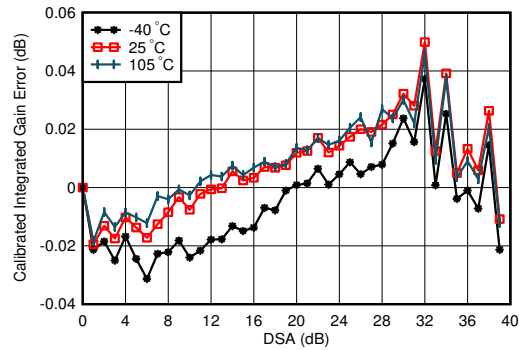
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-51. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 1.8GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-52. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8GHz**

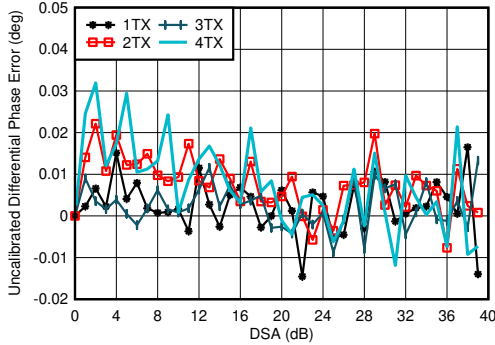


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-53. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8GHz**

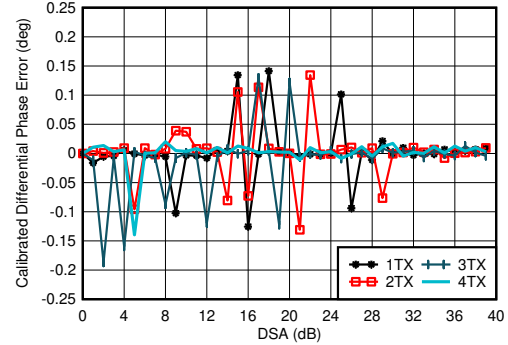
### 4.12.2 TX Typical Characteristics at 1.8GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

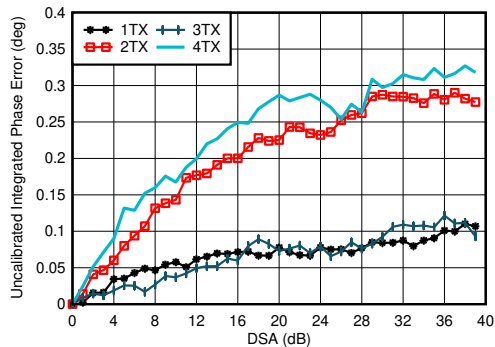
**Figure 4-54. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 1.8GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

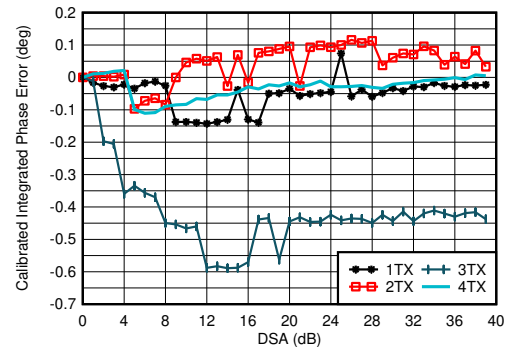
Phase DNL spike may occur at any DSA setting.

**Figure 4-55. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 1.8GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-56. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 1.8GHz**

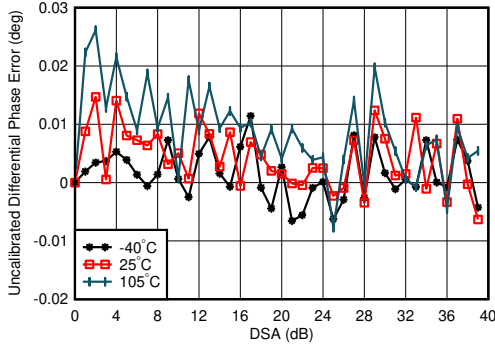


$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-57. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 1.8GHz**

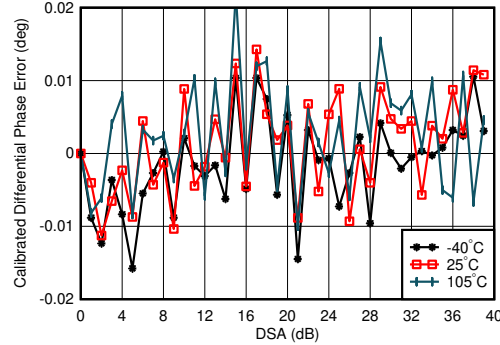
### 4.12.2 TX Typical Characteristics at 1.8GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



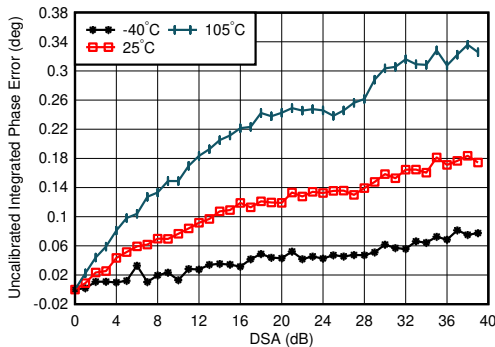
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-58. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 1.8GHz**



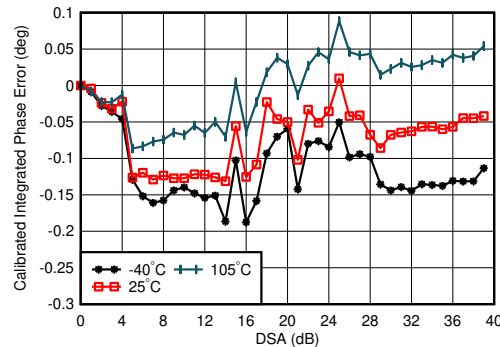
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz, channel with the median variation over DSA setting at 25°C  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-59. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 1.8GHz**



$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz, channel with the median variation over DSA setting at 25°C  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-60. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8GHz**



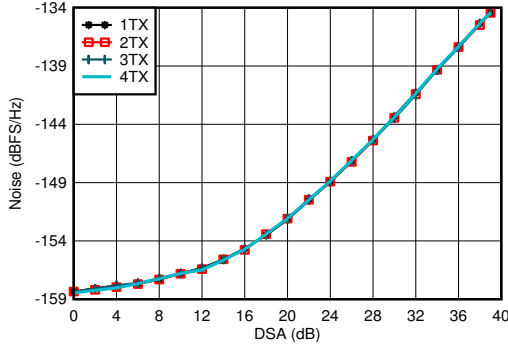
$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz, channel with the median variation over DSA setting at 25°C  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-61. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8GHz**



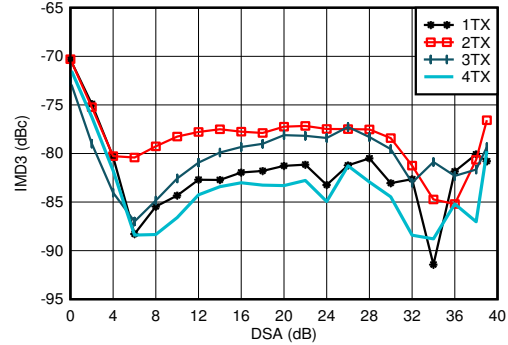
**4.12.2 TX Typical Characteristics at 1.8GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



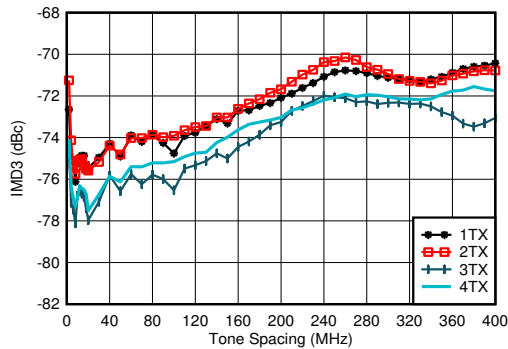
$f_{DAC} = 5898.24\text{MSPS}$ , interleave mode, matching at 1.8GHz,  $P_{OUT} = -13\text{dBFS}$

**Figure 4-62. TX Output Noise vs Channel and Attenuation at 1.8GHz**



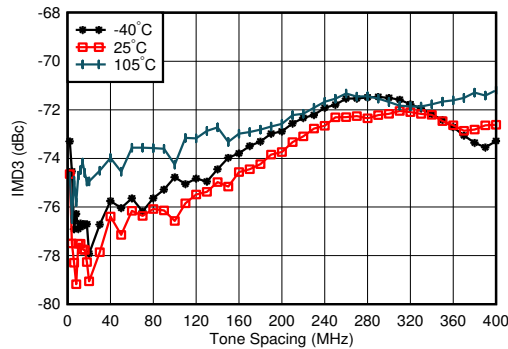
$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $f_{CENTER} = 1.8\text{GHz}$ , matching at 1.8GHz,  $-13\text{dBFS}$  each tone

**Figure 4-63. TX IMD3 vs DSA Setting at 1.8GHz**



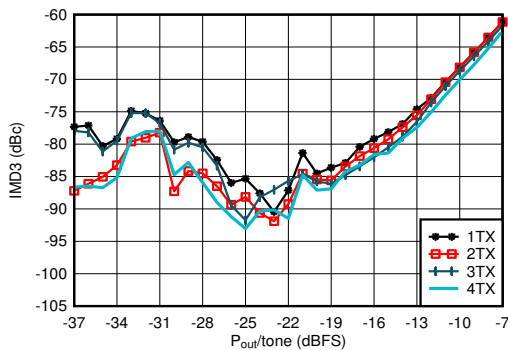
$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $f_{CENTER} = 1.8\text{GHz}$ , matching at 1.8GHz,  $-13\text{dBFS}$  each tone

**Figure 4-64. TX IMD3 vs Tone Spacing and Channel at 1.8GHz**



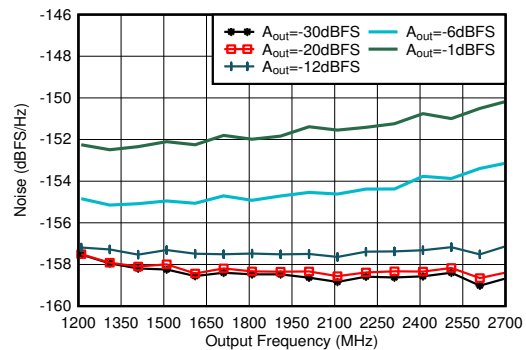
$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $f_{CENTER} = 1.8\text{GHz}$ , matching at 1.8GHz,  $-13\text{dBFS}$  each tone, worst channel

**Figure 4-65. TX IMD3 vs Tone Spacing and Temperature at 1.8GHz**



$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode,  $f_{CENTER} = 1.8\text{GHz}$ ,  $f_{SPACING} = 20\text{MHz}$ , matching at 1.8GHz

**Figure 4-66. TX IMD3 vs Digital Level at 1.8GHz**

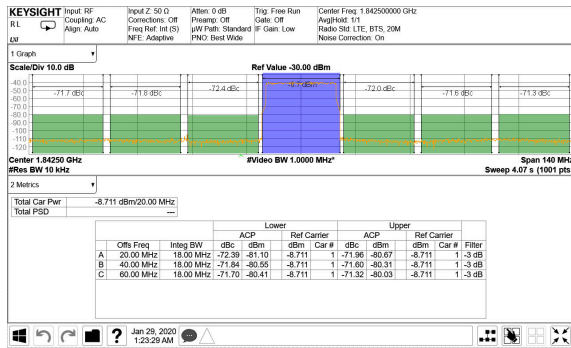


Matching at 2.6GHz, Single tone,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, 40MHz offset

**Figure 4-67. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8GHz**

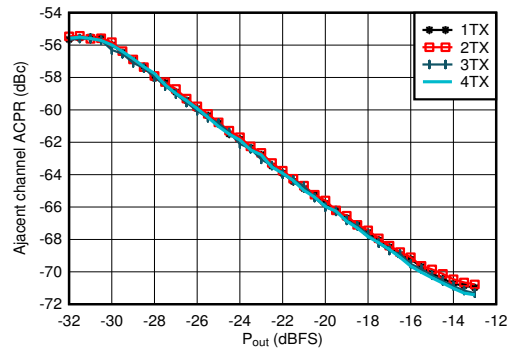
**4.12.2 TX Typical Characteristics at 1.8GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{ dBFS}$ , DSA = 0dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated



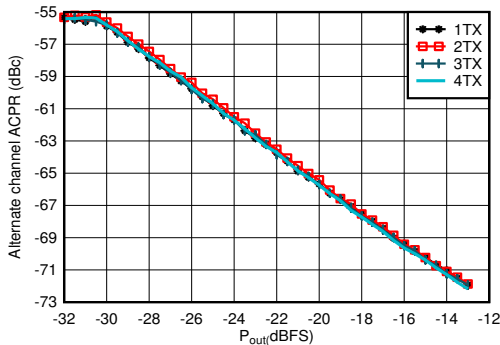
TM1.1,  $P_{OUT\_RMS} = -13\text{dBFS}$

**Figure 4-68. TX 20-MHz LTE Output Spectrum at 1.8425GHz**



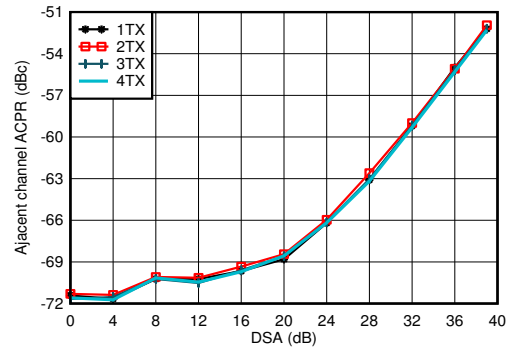
Matching at 1.8GHz, single carrier 20MHz BW TM1.1 LTE

**Figure 4-69. TX 20MHz LTE ACPR vs Digital Level at 1.8425GHz**



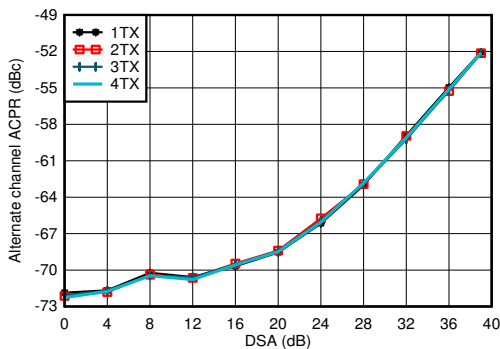
Matching at 1.8GHz, single carrier 20MHz BW TM1.1 LTE

**Figure 4-70. TX 20MHz LTE alt-ACPR vs Digital Level at 1.8425GHz**



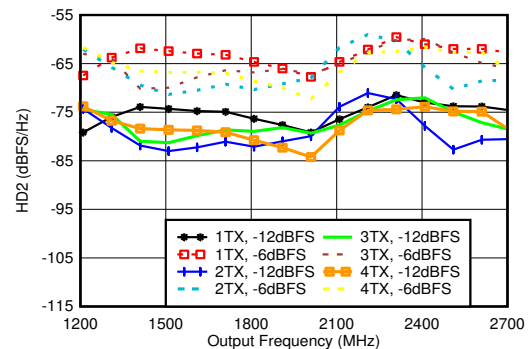
Matching at 1.8GHz, single carrier 20MHz BW TM1.1 LTE

**Figure 4-71. TX 20MHz LTE ACPR vs DSA at 1.8GHz**



Matching at 1.8GHz, single carrier 20MHz BW TM1.1 LTE

**Figure 4-72. TX 20MHz LTE alt-ACPR vs DSA at 1.8GHz**

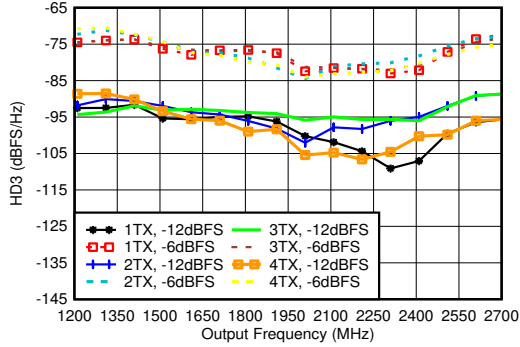


Matching at 1.8GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

**Figure 4-73. TX HD2 vs Digital Amplitude and Output Frequency at 1.8GHz**

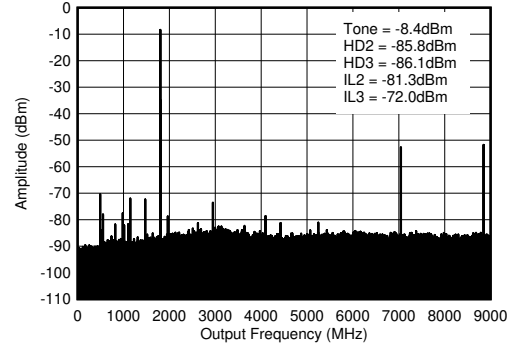
### 4.12.2 TX Typical Characteristics at 1.8GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{ dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



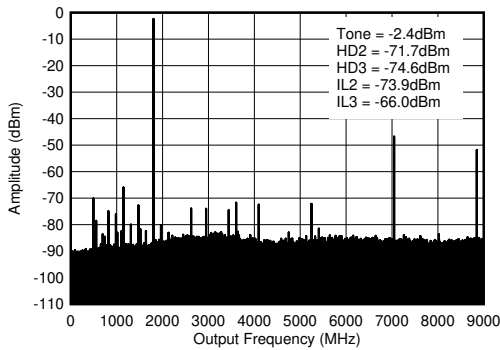
Matching at 1.8GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

**Figure 4-74. TX HD3 vs Digital Amplitude and Output Frequency at 1.8GHz**



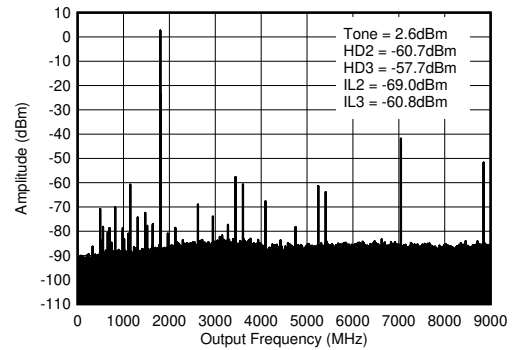
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 4-75. TX Single Tone (-12 dBFS) Output Spectrum at 1.8GHz ( $0-f_{\text{DAC}}$ )**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 4-76. TX Single Tone (-6 dBFS) Output Spectrum at 1.8GHz ( $0-f_{\text{DAC}}$ )**

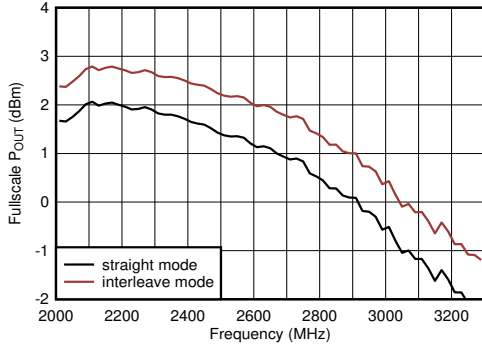


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 1.8GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 4-77. TX Single Tone (-1dBFS) Output Spectrum at 1.8GHz ( $0-f_{\text{DAC}}$ )**

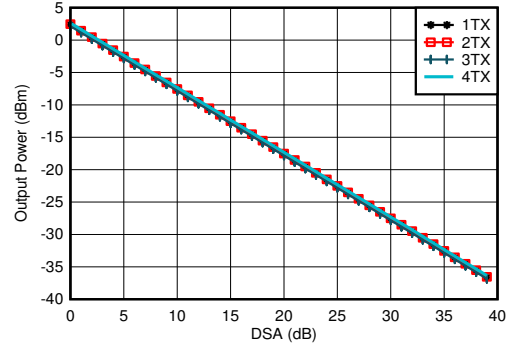
### 4.12.3 TX Typical Characteristics at 2.6GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



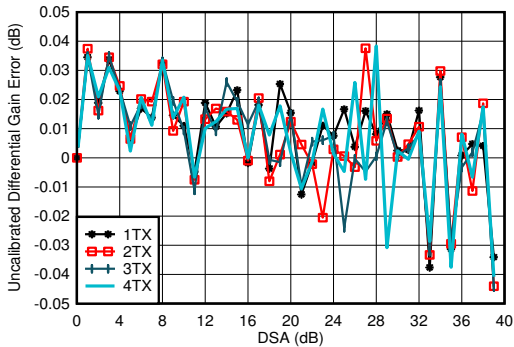
Including PCB and cable losses,  $A_{out} = -0.5\text{dBFS}$ , DSA = 0, 2.6GHz matching

Figure 4-78. TX Full Scale vs RF Frequency at 11796.48MSPS



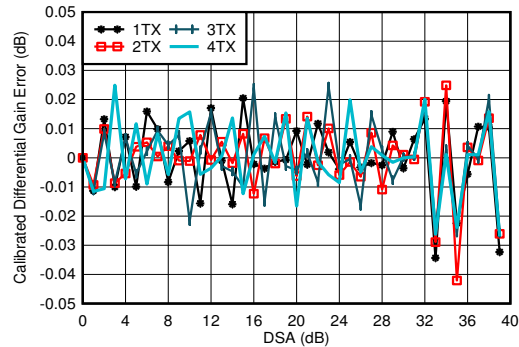
$f_{DAC} = 8847.36\text{MSPS}$ ,  $A_{out} = -0.5\text{dBFS}$ , matching 2.6GHz

Figure 4-79. TX Output Power vs DSA Setting and Channel at 2.6GHz



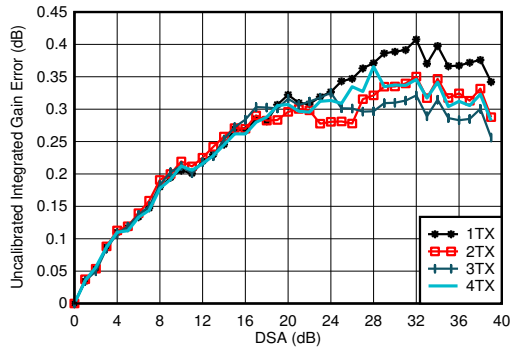
$f_{DAC} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz  
Differential Gain Error =  $P_{OUT}(\text{DSA Setting} - 1) - P_{OUT}(\text{DSA Setting}) + 1$

Figure 4-80. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6GHz



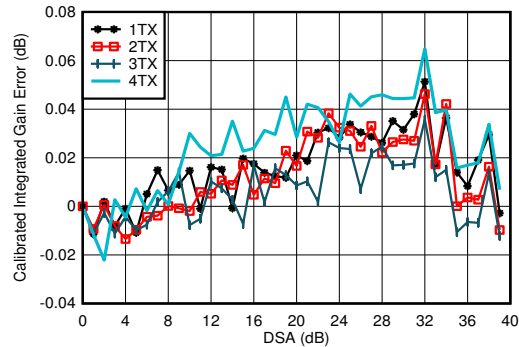
$f_{DAC} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz  
Differential Gain Error =  $P_{OUT}(\text{DSA Setting} - 1) - P_{OUT}(\text{DSA Setting}) + 1$

Figure 4-81. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6GHz



$f_{DAC} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz  
Integrated Gain Error =  $P_{OUT}(\text{DSA Setting}) - P_{OUT}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 4-82. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6GHz

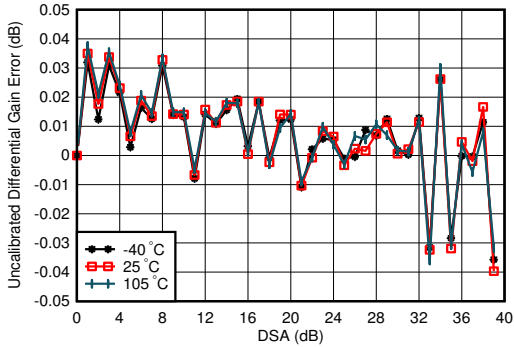


$f_{DAC} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz  
Integrated Gain Error =  $P_{OUT}(\text{DSA Setting}) - P_{OUT}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 4-83. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6GHz

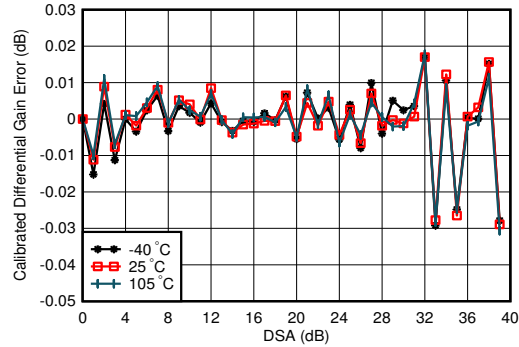
**4.12.3 TX Typical Characteristics at 2.6GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



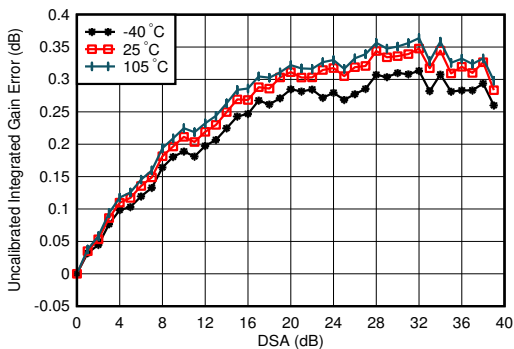
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-84. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6GHz**



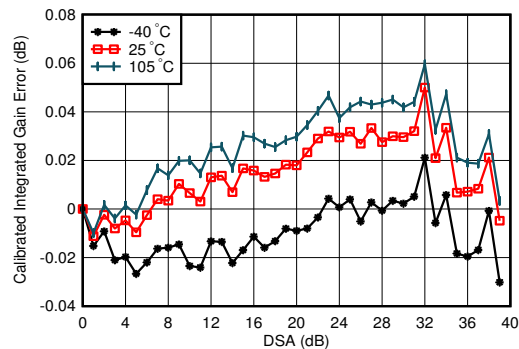
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C  
 Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-85. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-86. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6GHz**

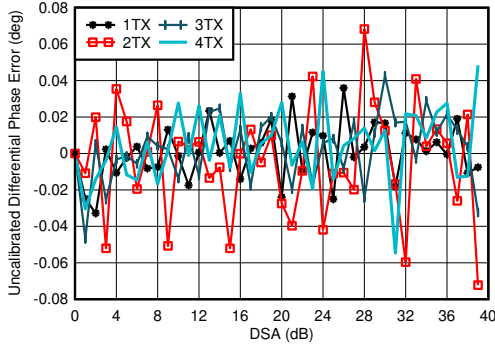


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C  
 Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-87. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6GHz**

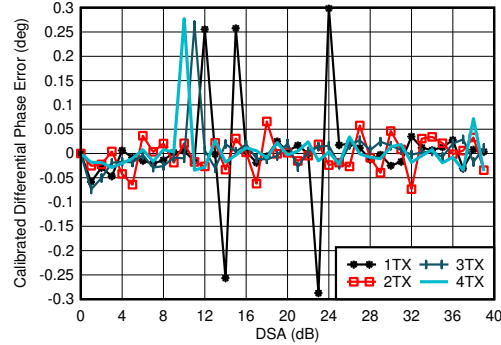
### 4.12.3 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

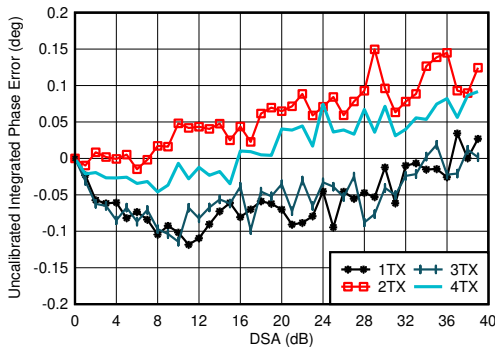
**Figure 4-88. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

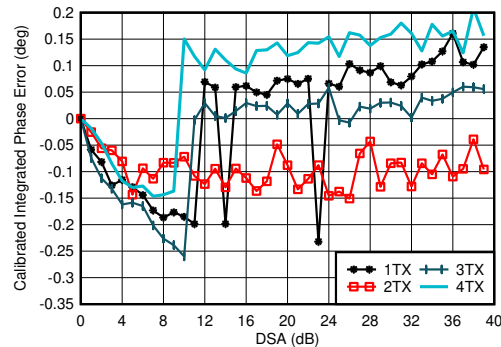
Phase DNL spike may occur at any DSA setting.

**Figure 4-89. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-90. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6GHz**

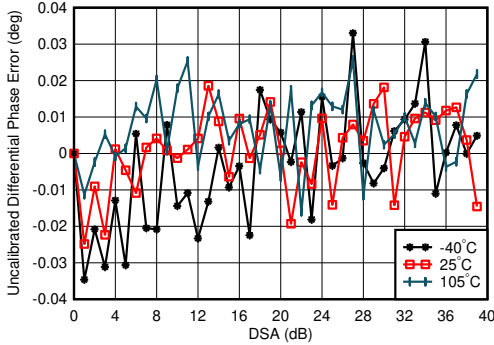


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-91. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6GHz**

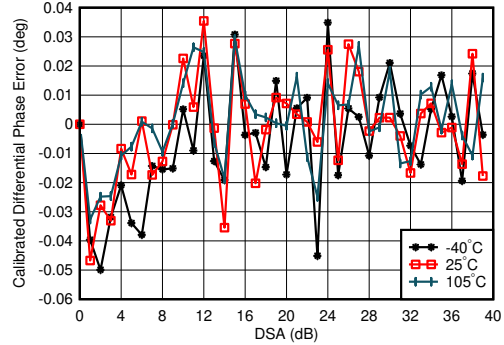
**4.12.3 TX Typical Characteristics at 2.6GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



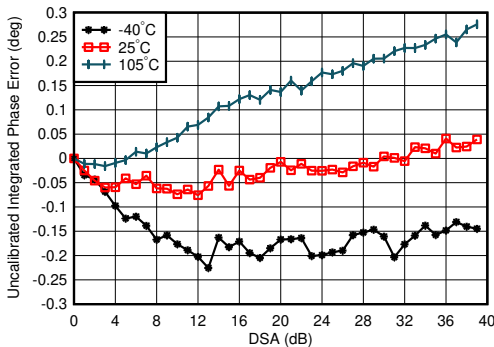
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-92. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6GHz**



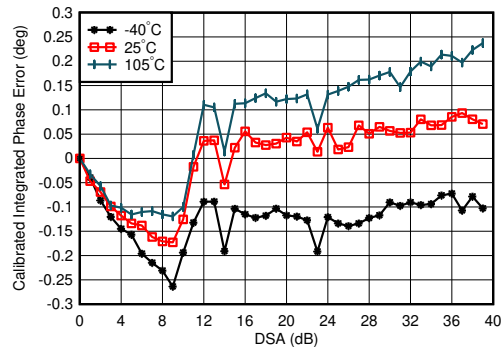
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-93. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz, channel with the medium variation over DSA setting at 25°C  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-94. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6GHz**

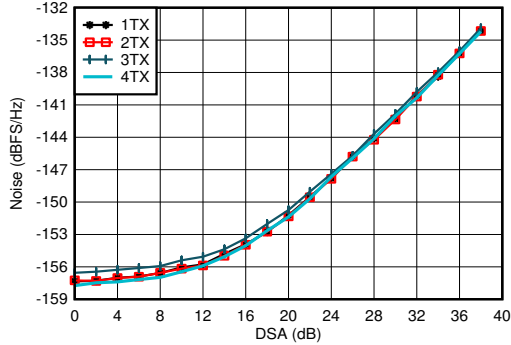


$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz, channel with the median variation over DSA setting at 25°C  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-95. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6GHz**

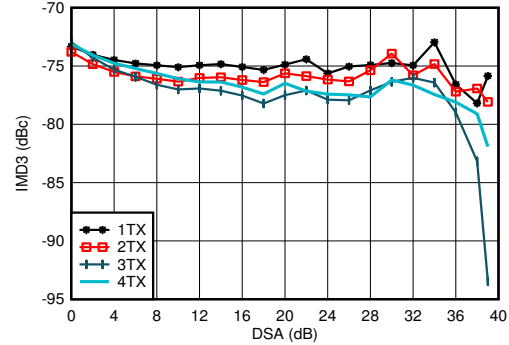
**4.12.3 TX Typical Characteristics at 2.6GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



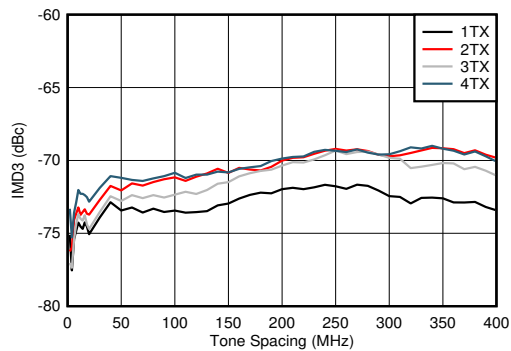
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, matching at 2.6GHz,  $P_{\text{OUT}} = -13\text{ dBFS}$

**Figure 4-96. TX Output Noise vs Channel and Attenuation at 2.6GHz**



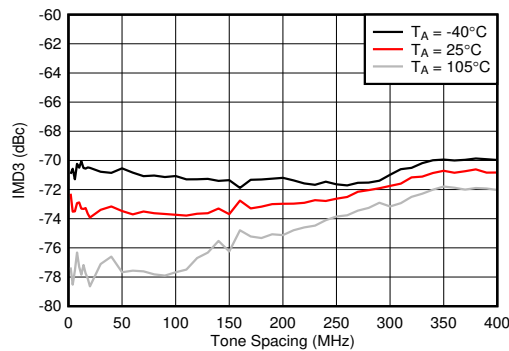
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{GHz}$ , matching at 2.6GHz,  $-13\text{ dBFS}$  each tone

**Figure 4-97. TX IMD3 vs DSA Setting at 2.6GHz**



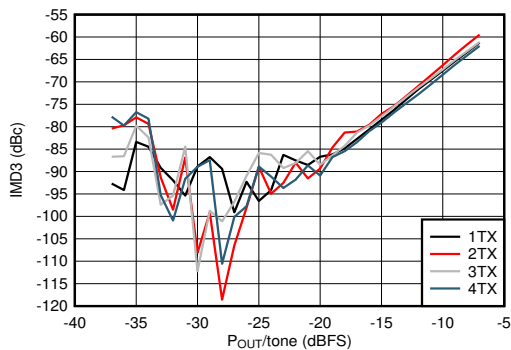
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{GHz}$ , matching at 2.6GHz,  $-13\text{ dBFS}$  each tone

**Figure 4-98. TX IMD3 vs Tone Spacing and Channel at 2.6GHz**



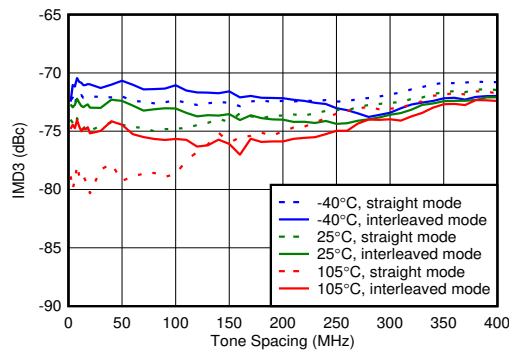
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{GHz}$ , matching at 2.6GHz,  $-13\text{ dBFS}$  each tone, worst channel.

**Figure 4-99. TX IMD3 vs Tone Spacing and Temperature at 2.6GHz**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{GHz}$ ,  $f_{\text{SPACING}} = 20\text{ MHz}$ , matching at 2.6GHz

**Figure 4-100. TX IMD3 vs Digital Level at 2.6GHz**



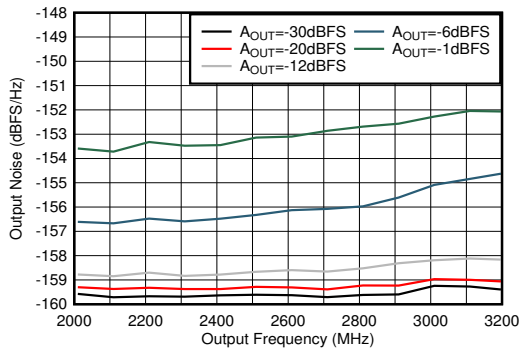
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode,  $f_{\text{CENTER}} = 2.6\text{GHz}$ , matching at 2.6GHz,  $-13\text{ dBFS}$  each tone

**Figure 4-101. TX IMD3 vs Tone Spacing and Temperature**



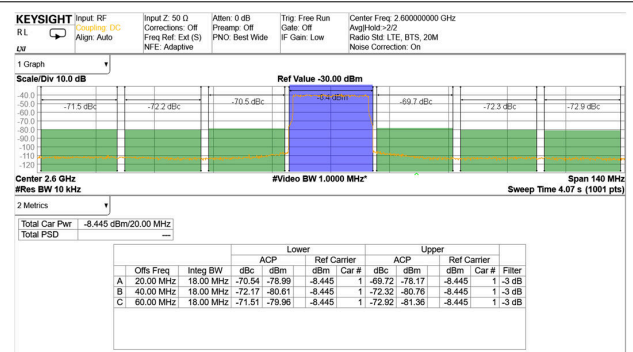
### 4.12.3 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



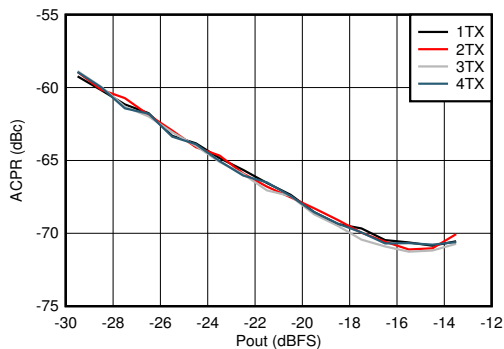
Matching at 2.6GHz, Single tone,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, 40-MHz offset

Figure 4-102. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6GHz



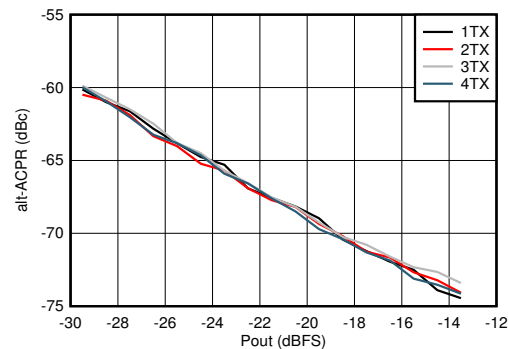
TM1.1,  $P_{OUT\_RMS} = -13\text{dBFS}$

Figure 4-103. TX 20-MHz LTE Output Spectrum at 2.6GHz (Band 41)



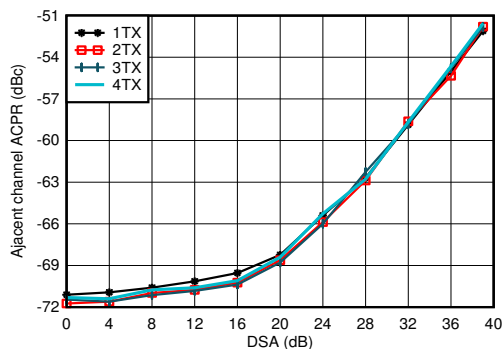
Matching at 2.6GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-104. TX 20-MHz LTE ACPR vs Digital Level at 2.6GHz



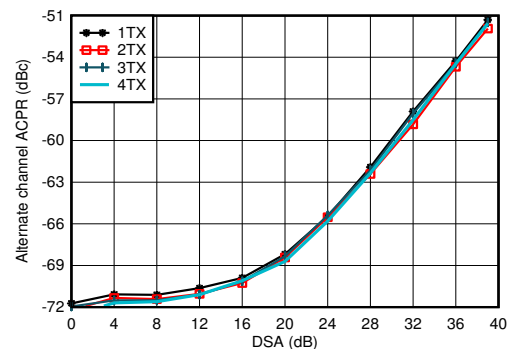
Matching at 2.6GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-105. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6GHz



Matching at 2.6GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-106. TX 20-MHz LTE ACPR vs DSA at 2.6GHz

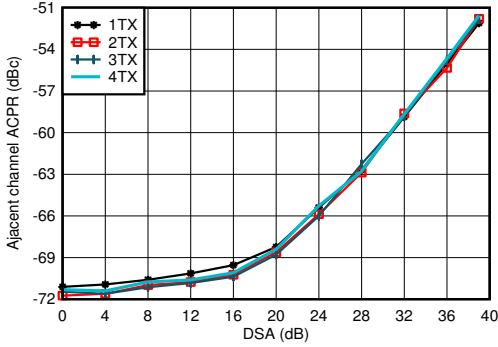


Matching at 2.6GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-107. TX 20-MHz LTE alt-ACPR vs DSA at 2.6GHz

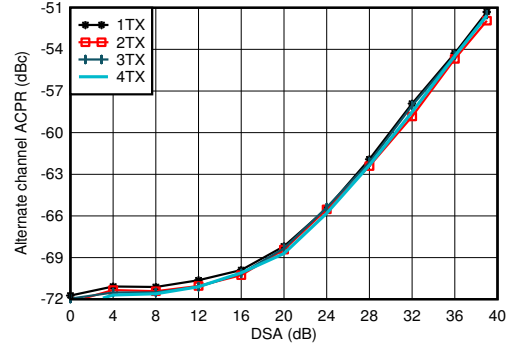
### 4.12.3 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



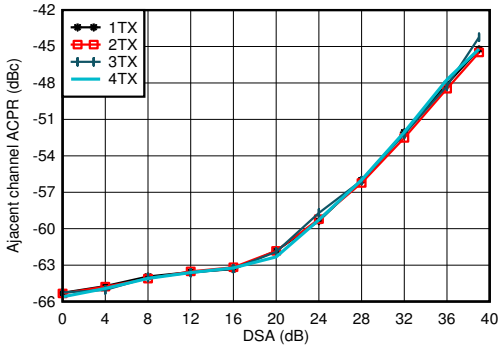
Matching at 2.6GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-108. TX 20-MHz LTE ACPR vs DSA at 2.6GHz



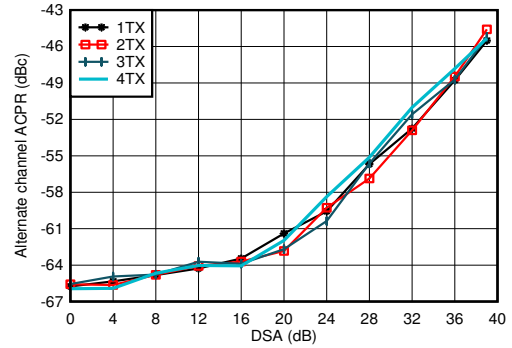
Matching at 2.6GHz, single carrier 20MHz BW TM1.1 LTE

Figure 4-109. TX 20-MHz LTE alt-ACPR vs DSA at 2.6GHz



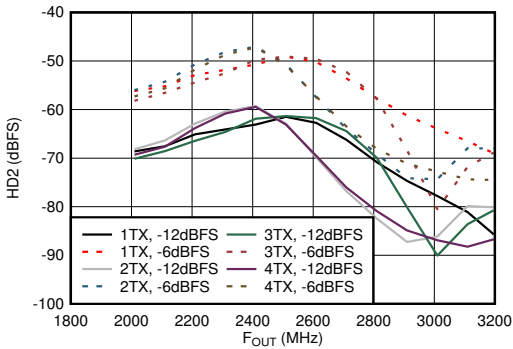
Matching at 2.6GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-110. TX 100-MHz NR ACPR vs DSA at 2.6GHz



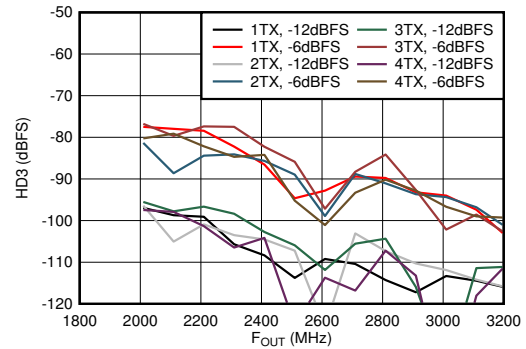
Matching at 2.6GHz, single carrier 100MHz BW TM1.1 NR

Figure 4-111. TX 100-MHz NR alt-ACPR vs DSA at 2.6GHz



Matching at 2.6GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

Figure 4-112. TX HD2 vs Digital Amplitude and Output Frequency at 2.6GHz

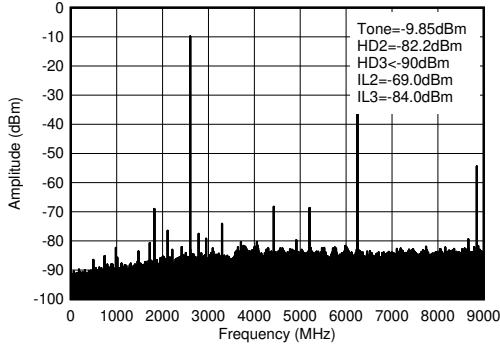


Matching at 2.6GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

Figure 4-113. TX HD3 vs Digital Amplitude and Output Frequency at 2.6GHz

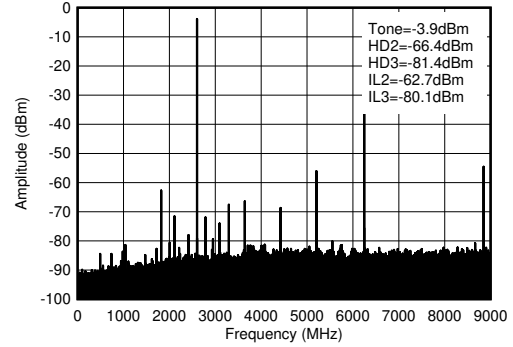
### 4.12.3 TX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



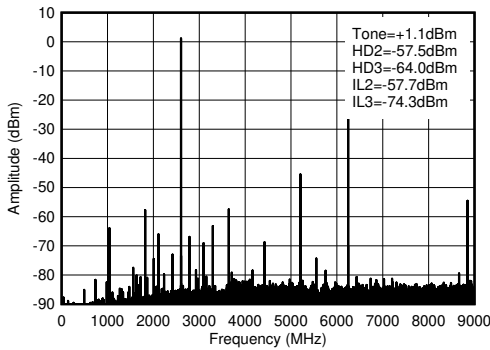
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 4-114. TX Single Tone (-12dBFS) Output Spectrum at 2.6GHz ( $0-f_{\text{DAC}}$ )**



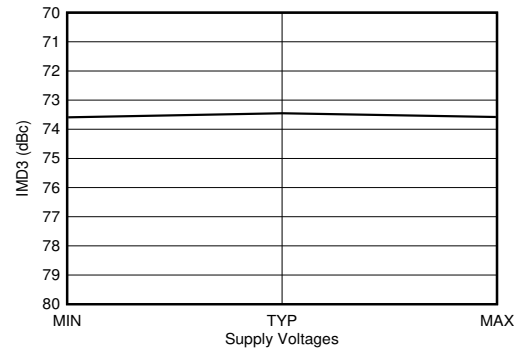
$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 4-115. TX Single Tone (-6dBFS) Output Spectrum at 2.6GHz ( $0-f_{\text{DAC}}$ )**



$f_{\text{DAC}} = 8847.36\text{MSPS}$ , straight mode, 2.6GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 4-116. TX Single Tone (-1dBFS) Output Spectrum at 2.6GHz ( $0-f_{\text{DAC}}$ )**

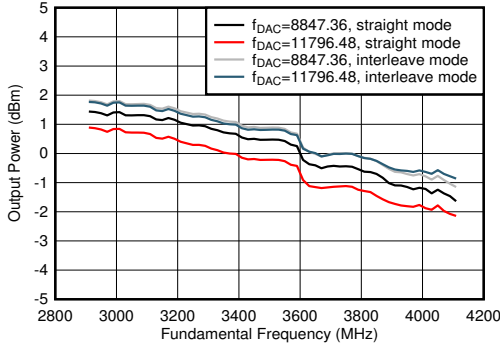


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 2.6GHz matching. 40MHz offset from tone. Output Power = -13dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

**Figure 4-117. TX IMD3 vs Supply Voltage at 2.6GHz**

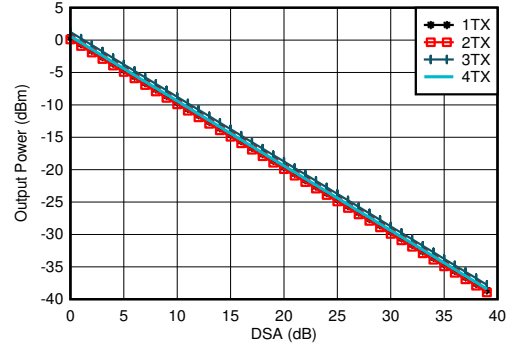
### 4.12.4 TX Typical Characteristics at 3.5GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



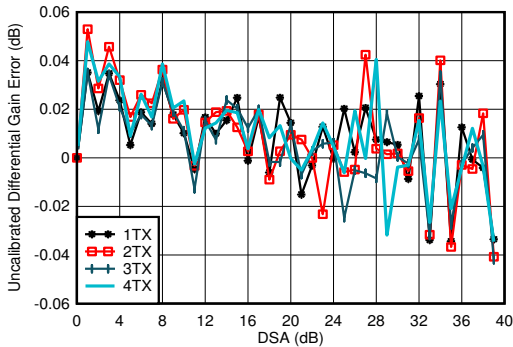
$A_{\text{out}} = -0.5\text{dBFS}$ , 3.5GHz Matching, included PCB and cable losses

**Figure 4-118. TX Output Power vs Frequency**



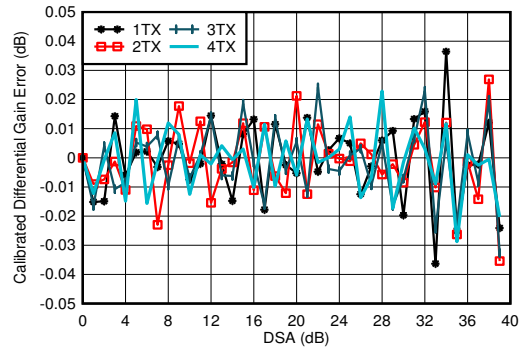
$A_{\text{out}} = -0.5\text{dBFS}$ , 3.5GHz Matching, included PCB and cable losses

**Figure 4-119. TX Output Power vs DSA Setting at 3.5GHz**



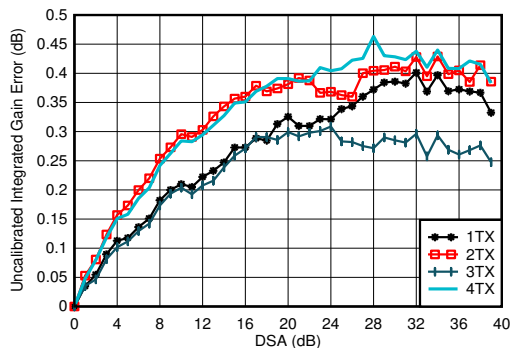
3.5GHz Matching, included PCB and cable losses  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-120. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5GHz**



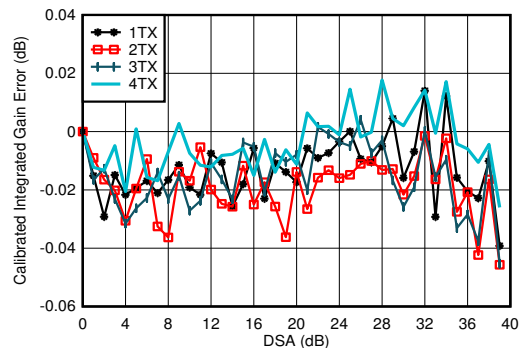
3.5GHz Matching, included PCB and cable losses  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-121. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5GHz**



3.5GHz Matching, included PCB and cable losses  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-122. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5GHz**

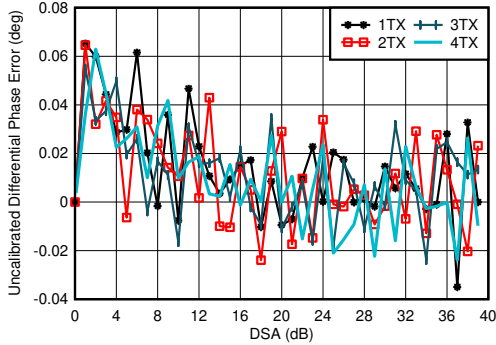


3.5GHz Matching, included PCB and cable losses  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-123. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5GHz**

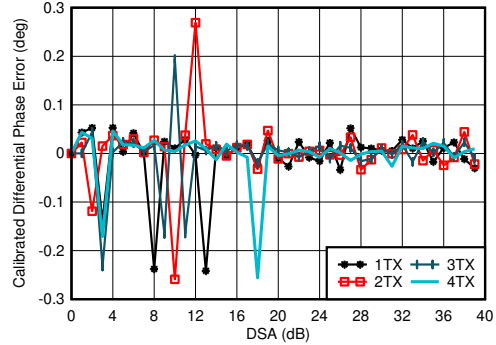
**4.12.4 TX Typical Characteristics at 3.5GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



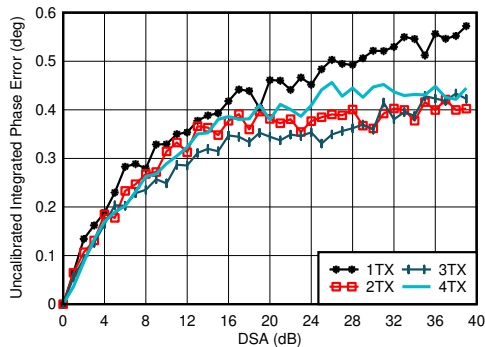
3.5GHz Matching, included PCB and cable losses

**Figure 4-124. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5GHz**



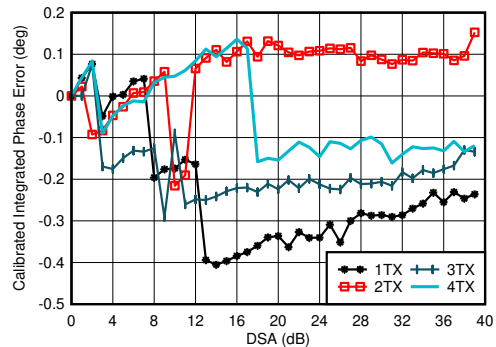
3.5GHz Matching, included PCB and cable losses  
Phase DNL spike may occur at any DSA setting.

**Figure 4-125. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5GHz**



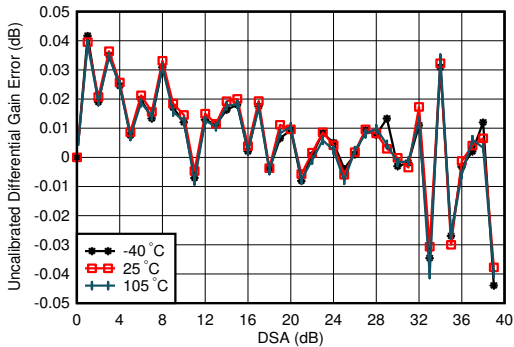
3.5GHz Matching, included PCB and cable losses

**Figure 4-126. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5GHz**



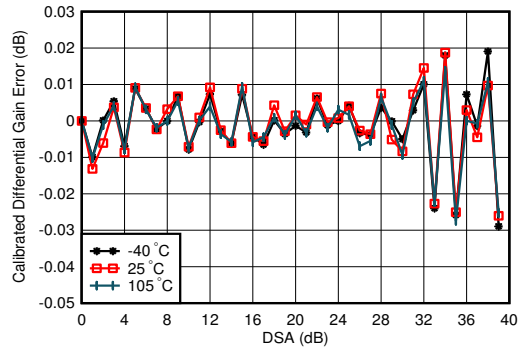
3.5GHz Matching, included PCB and cable losses

**Figure 4-127. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5GHz**



3.5GHz Matching, 1TX

**Figure 4-128. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5GHz**

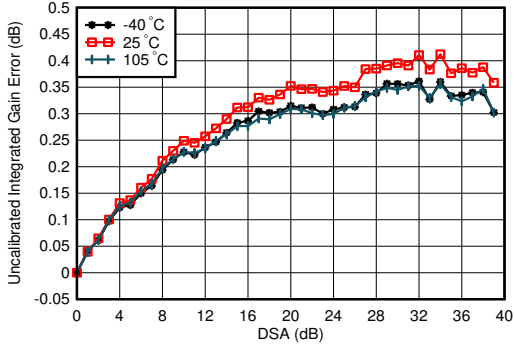


3.5GHz Matching, 1TX, Calibrated at 25°C

**Figure 4-129. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5GHz**

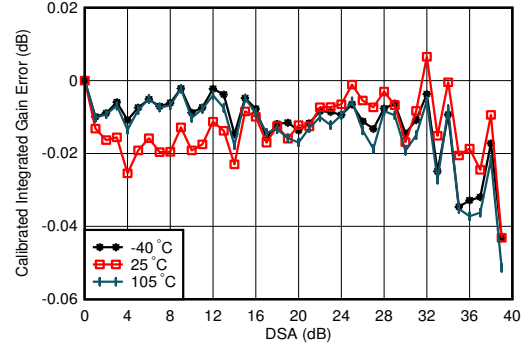
### 4.12.4 TX Typical Characteristics at 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



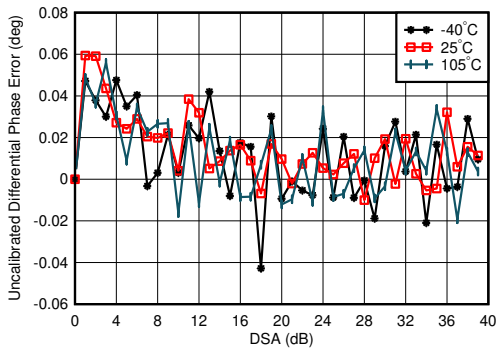
3.5GHz Matching, 1TX

**Figure 4-130. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5GHz**



3.5GHz Matching, 1TX, Calibrated at 25°C

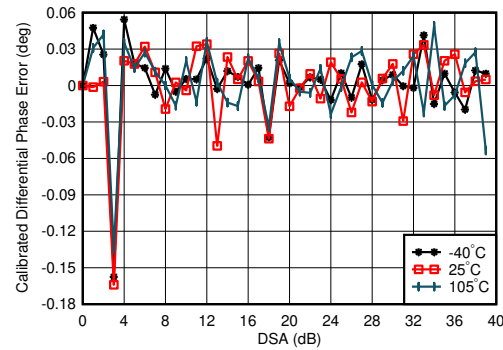
**Figure 4-131. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5GHz**



3.5GHz Matching, 1TX

$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

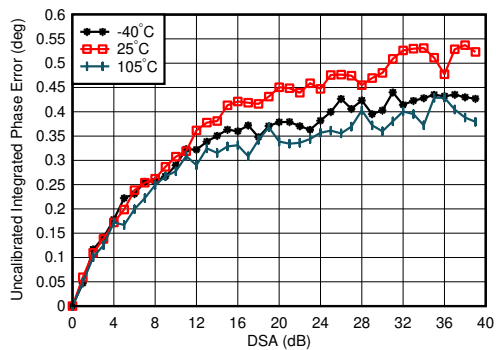
**Figure 4-132. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5GHz**



3.5GHz Matching, 1TX, Calibrated at 25°C

$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

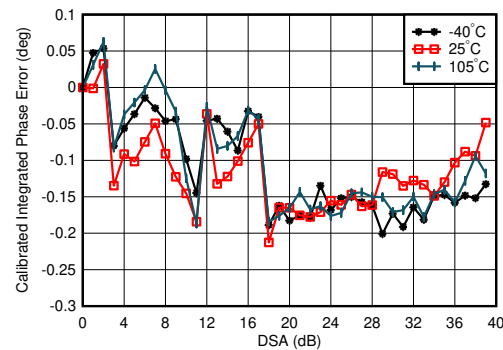
**Figure 4-133. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5GHz**



3.5GHz Matching, 1TX

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 4-134. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5GHz**



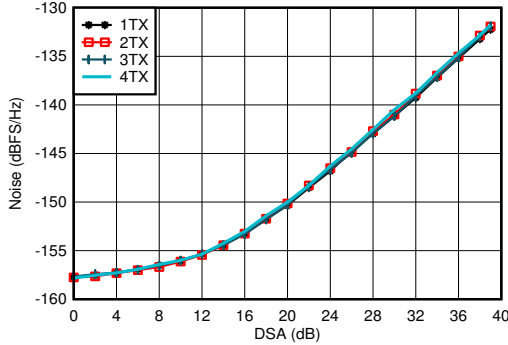
3.5GHz Matching, 1TX, Calibrated at 25°C

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 4-135. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5GHz**

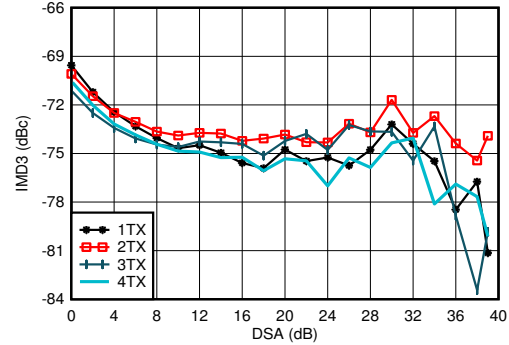
**4.12.4 TX Typical Characteristics at 3.5GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



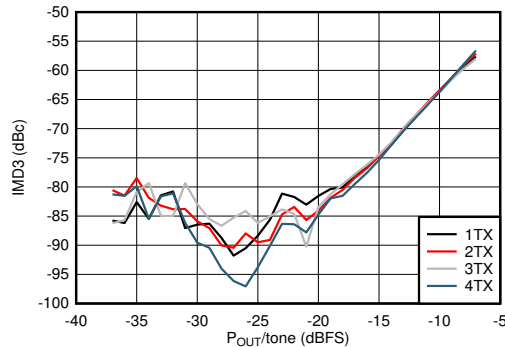
A.  $f_{DAC} = 11796.48\text{MSPS}$ , interleave mode, matching at 3.5GHz,  $A_{out} = -13\text{ dBFS}$ .

**Figure 4-136. TX NSD vs DSA Setting at 3.5GHz**



20MHz tone spacing, 3.5GHz Matching,  $-13\text{ dBFS}$  each tone, included PCB and cable losses

**Figure 4-137. TX IMD3 vs DSA Setting at 3.5GHz**



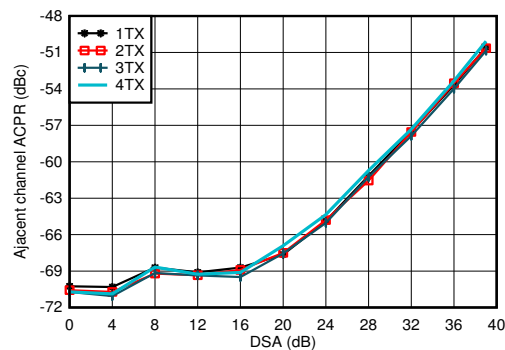
20MHz tone spacing, 3.5GHz Matching

**Figure 4-138. TX IMD3 vs Digital Amplitude and Channel at 3.5GHz**



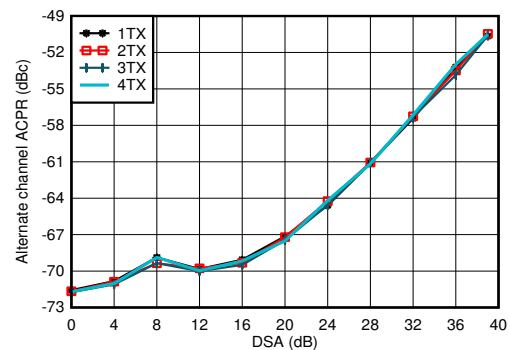
3.5GHz Matching, single carrier 20MHz BW TM1.1 LTE

**Figure 4-139. TX 20MHz LTE Output Spectrum at 3.5GHz (Band 42)**



3.5GHz Matching, single carrier 20MHz BW TM1.1 LTE

**Figure 4-140. TX 20MHz LTE ACPR vs DSA Setting at 3.5GHz**

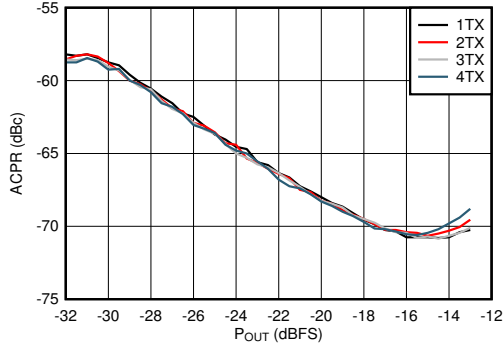


3.5GHz Matching, single carrier 20MHz BW TM1.1 LTE

**Figure 4-141. TX 20MHz LTE alt-ACPR vs DSA Setting at 3.5GHz**

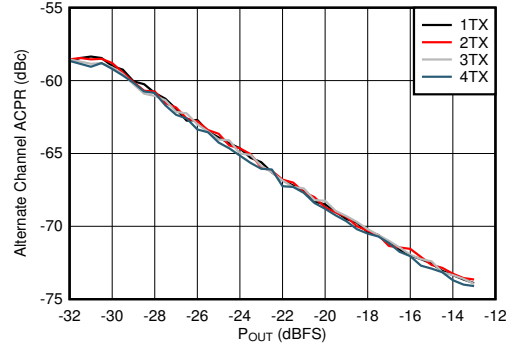
**4.12.4 TX Typical Characteristics at 3.5GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



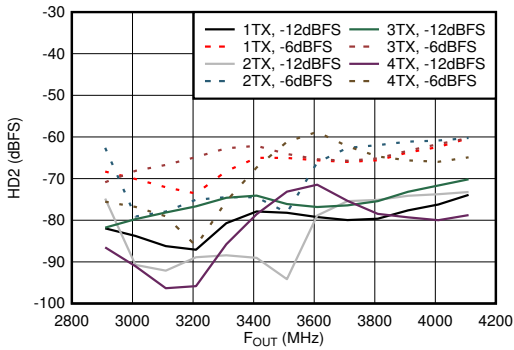
3.5GHz Matching, single carrier 20MHz BW TM1.1 LTE

**Figure 4-142. TX 20MHz LTE ACPR vs Digital Level at 3.5GHz**



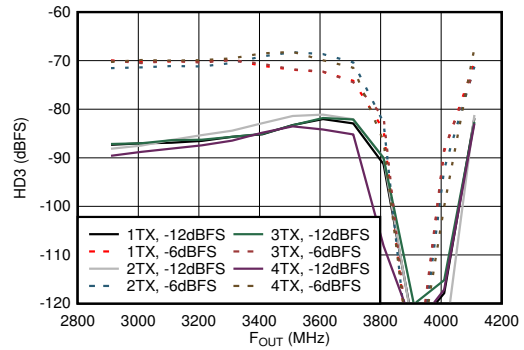
3.5GHz Matching, single carrier 20MHz BW TM1.1 LTE

**Figure 4-143. TX 20MHz LTE alt-ACPR vs Digital Level at 3.5GHz**



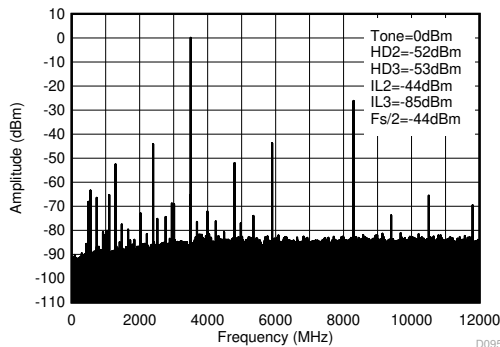
Matching at 3.5GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency

**Figure 4-144. TX Single Tone HD2 vs Frequency and Digital Level at 3.5GHz**



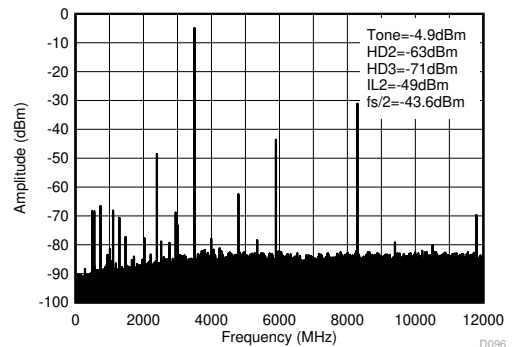
Matching at 3.5GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

**Figure 4-145. TX Single Tone HD3 vs Frequency and Digital Level at 3.5GHz**



Matching at 3.5GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 4-146. TX Single Tone (-1dBFS) Output Spectrum at 3.5GHz (0 -  $f_{DAC}$ )**



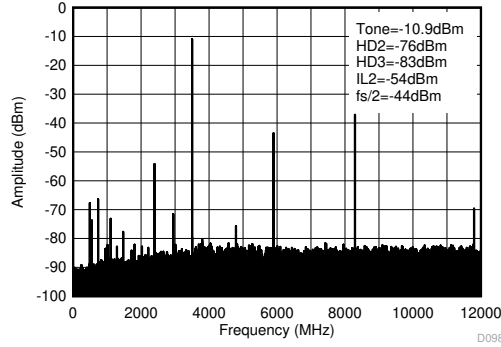
Matching at 3.5GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 4-147. TX Single Tone (-6dBFS) Output Spectrum at 3.5GHz (0 -  $f_{DAC}$ )**



**4.12.4 TX Typical Characteristics at 3.5GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated

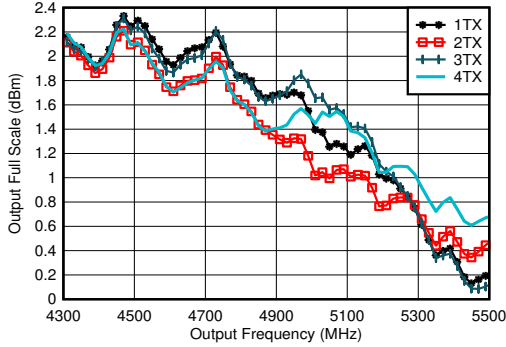


Matching at 3.5GHz,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode.

**Figure 4-148. TX Single Tone (-12dBFS) Output Spectrum at 3.5GHz (0- $f_{\text{DAC}}$ )**

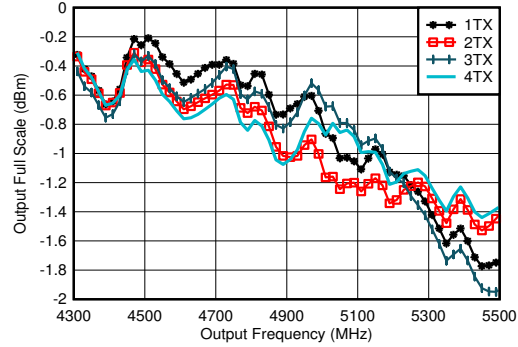
### 4.12.5 TX Typical Characteristics at 4.9GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



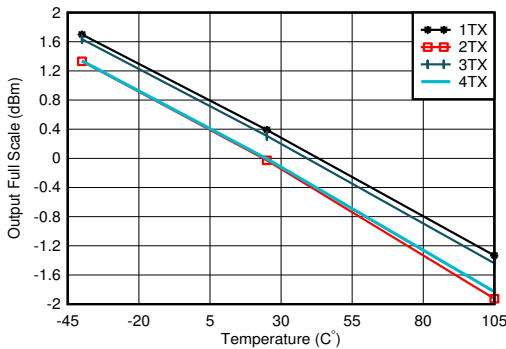
Excluding PCB and cable losses,  $A_{\text{out}} = -0.5\text{ dBFS}$ , DSA = 0, 4.9GHz matching

**Figure 4-149. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS**



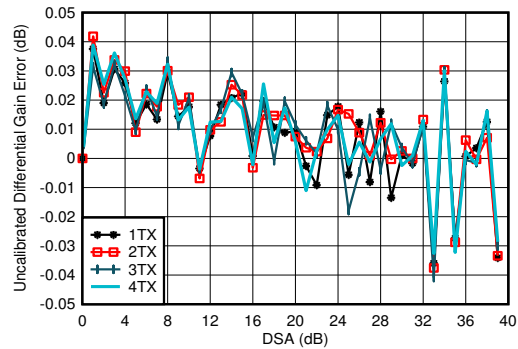
Excluding PCB and cable losses,  $A_{\text{out}} = -0.5\text{ dBFS}$ , DSA = 0, 4.9GHz matching

**Figure 4-150. TX Full Scale vs RF Frequency and Channel at 5898.24 MSPS, Straight Mode, 2nd Nyquist Zone**



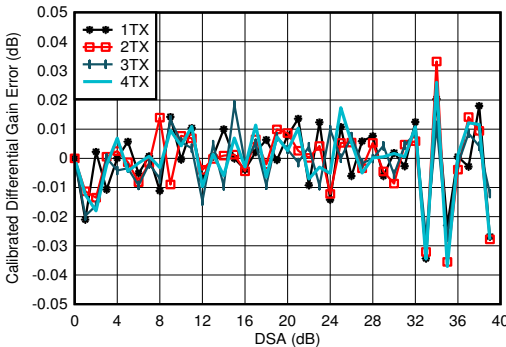
$f_{\text{DAC}} = 11796.48\text{MSPS}$ ,  $A_{\text{out}} = -0.5\text{ dBFS}$ , matching 4.9GHz

**Figure 4-151. TX Output Power vs DSA Setting and Channel at 4.9GHz**



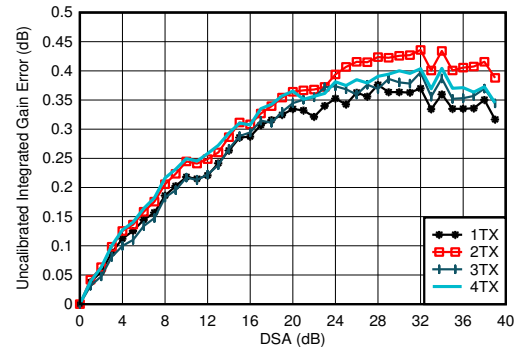
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-152. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-153. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9GHz**

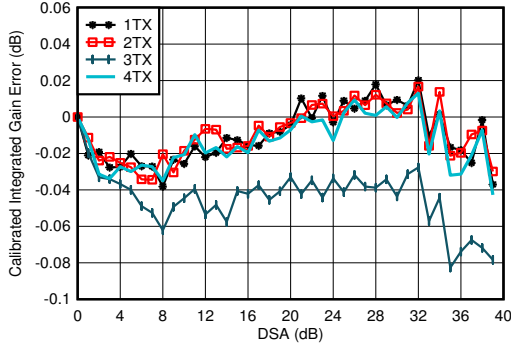


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-154. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9GHz**

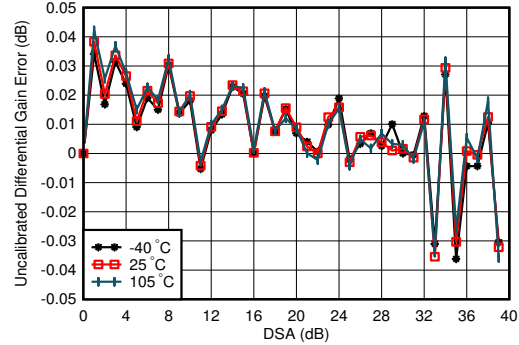
### 4.12.5 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



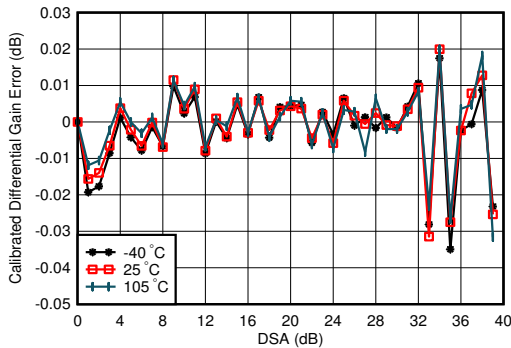
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, matching at 4.9GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-155. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9GHz**



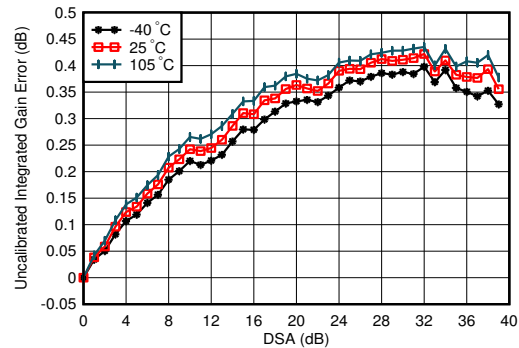
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-156. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9GHz**



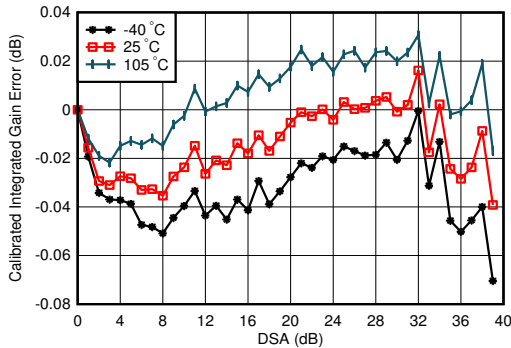
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 4-157. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9GHz**



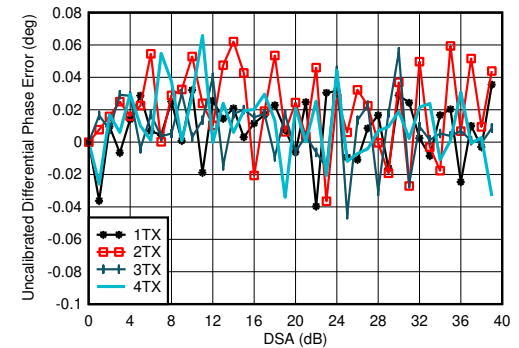
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-158. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-159. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9GHz**

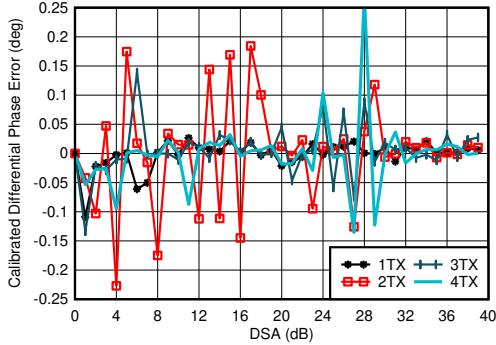


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-160. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9GHz**

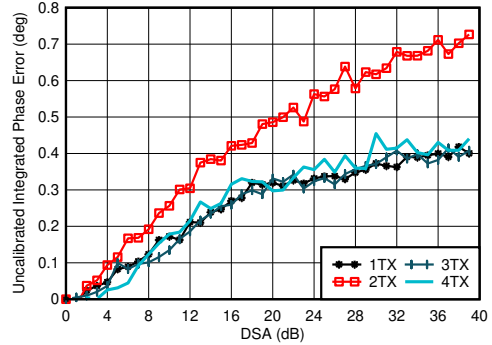
### 4.12.5 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



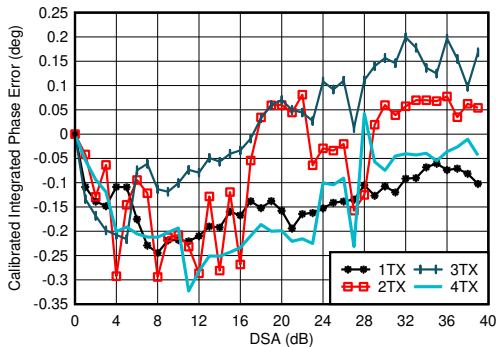
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
 Phase DNL spike may occur at any DSA setting.

**Figure 4-161. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9GHz**



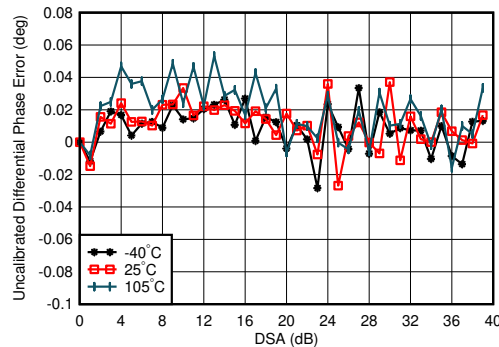
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-162. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-163. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9GHz**

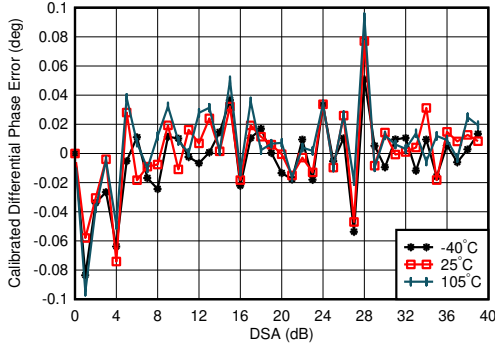


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-164. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9GHz**

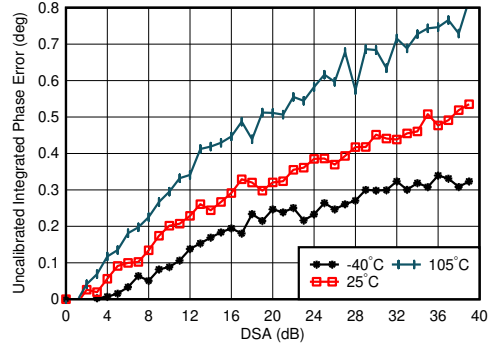
### 4.12.5 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleaved mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



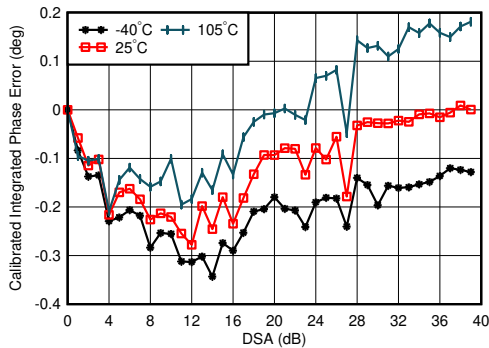
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 4-165. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9GHz**



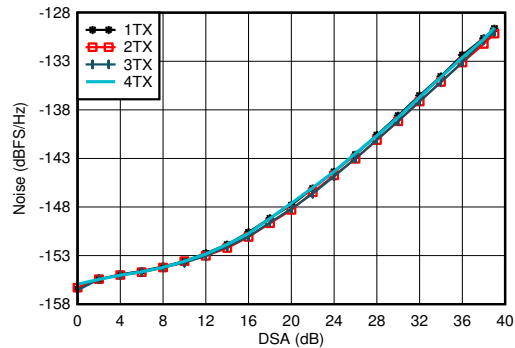
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-166. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9GHz**



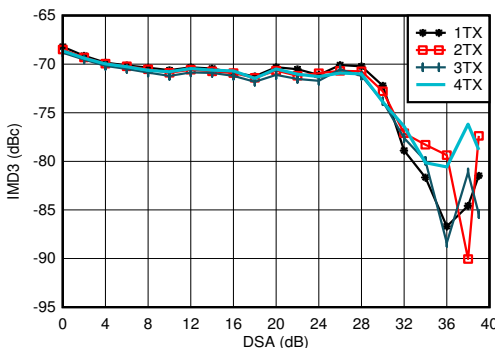
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz, channel with the median variation over DSA setting at 25°C  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-167. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9GHz**



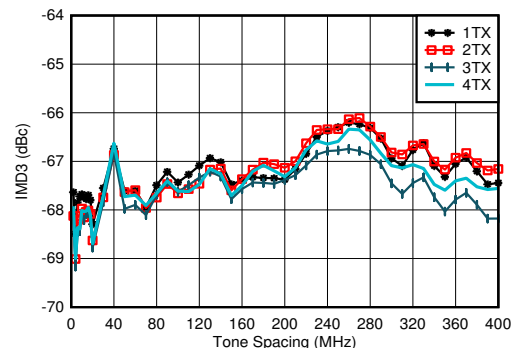
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz,  $P_{\text{OUT}} = -13\text{ dBFS}$

**Figure 4-168. TX Output Noise vs Channel and Attenuation at 2.6GHz**



$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ , -13 dBFS each tone

**Figure 4-169. TX IMD3 vs DSA Setting at 4.9GHz**

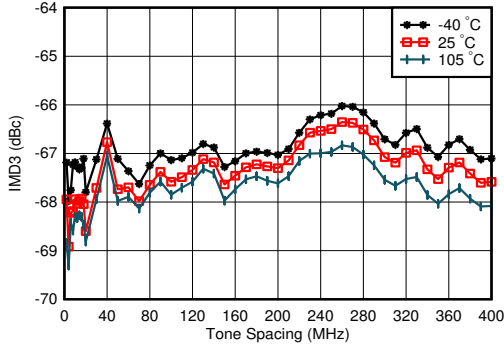


$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ , -13 dBFS each tone

**Figure 4-170. TX IMD3 vs Tone Spacing and Channel at 4.9GHz**

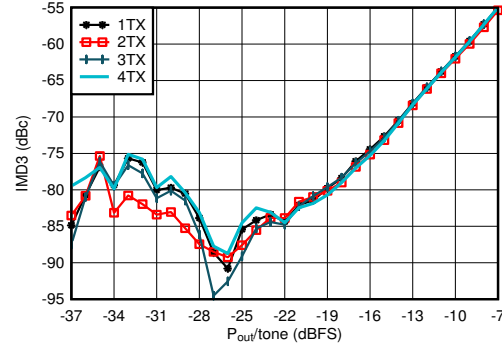
### 4.12.5 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



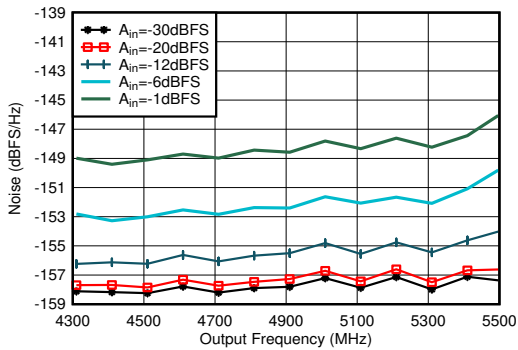
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ , -13 dBFS each tone, worst channel

**Figure 4-171. TX IMD3 vs Tone Spacing and Temperature at 4.9GHz**



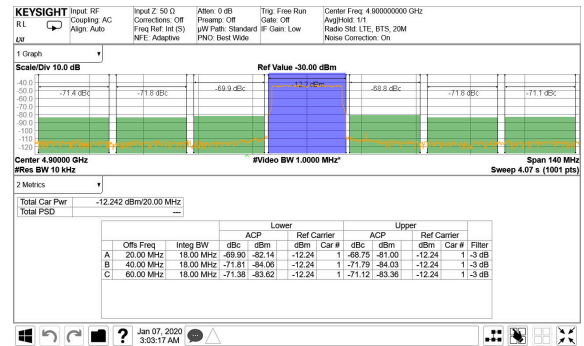
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleaved mode, matching at 4.9GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ ,  $f_{\text{SPACING}} = 20\text{MHz}$

**Figure 4-172. TX IMD3 vs Digital Level at 4.9GHz**



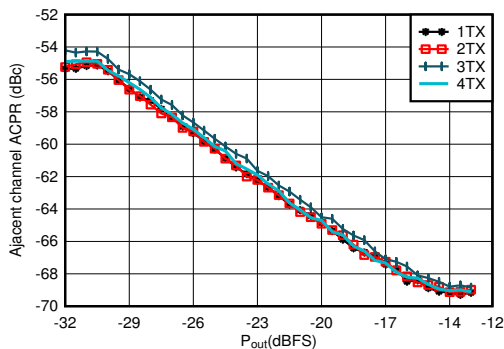
Matching at 4.9GHz, Single tone,  $f_{\text{DAC}} = 11.79648\text{GSPS}$ , interleave mode, 40MHz offset, DSA = 0dB

**Figure 4-173. TX Single Tone Output Noise vs Frequency and Amplitude at 4.9GHz**



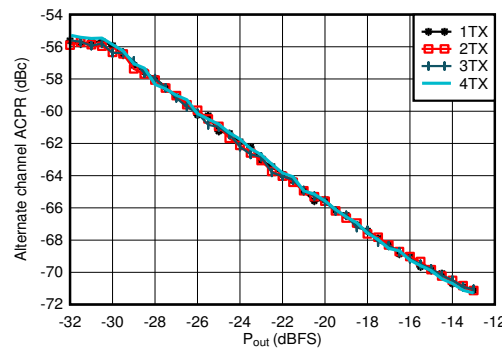
TM1.1,  $P_{\text{OUT\_RMS}} = -13\text{dBFS}$

**Figure 4-174. TX 20MHz LTE Output Spectrum at 4.9GHz**



Matching at 4.9GHz, single carrier 20MHz BW TM1.1 LTE

**Figure 4-175. TX 20MHz LTE ACPR vs Digital Level at 4.9GHz**

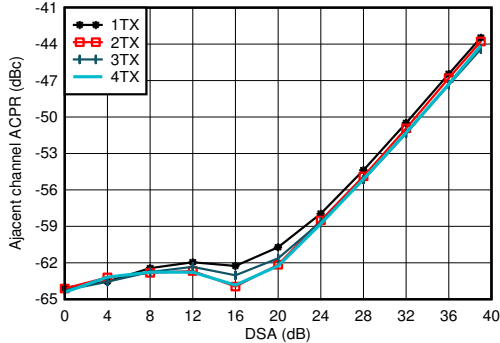


Matching at 4.9GHz, single carrier 20MHz BW TM1.1 LTE

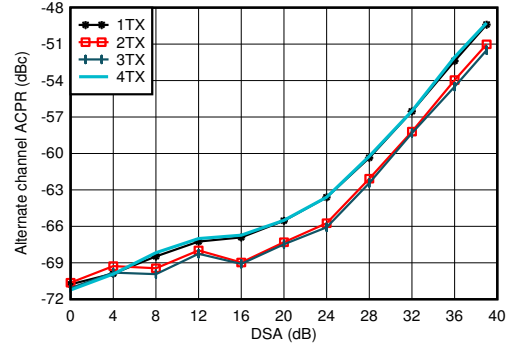
**Figure 4-176. TX 20MHz LTE alt-ACPR vs Digital Level at 4.9GHz**

### 4.12.5 TX Typical Characteristics at 4.9GHz (continued)

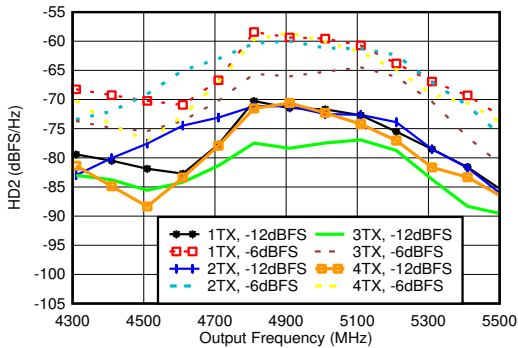
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



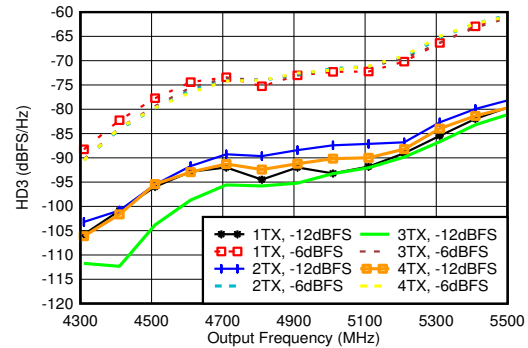
Matching at 4.9GHz, single carrier 20MHz BW TM1.1 LTE  
**Figure 4-177. TX 20MHz LTE ACPR vs DSA at 4.9GHz**



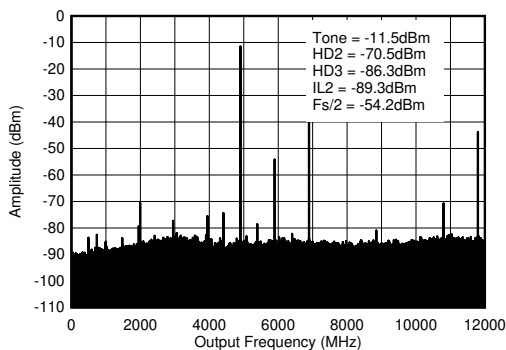
Matching at 4.9GHz, single carrier 20MHz BW TM1.1 LTE  
**Figure 4-178. TX 20MHz LTE alt-ACPR vs DSA at 4.9GHz**



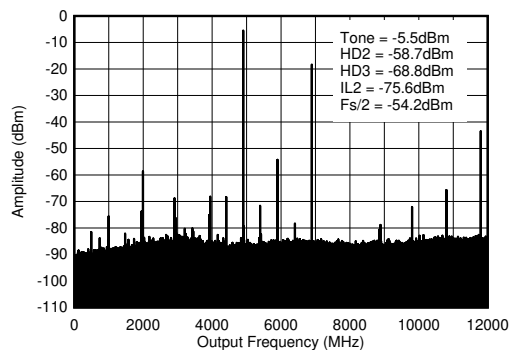
Matching at 4.9GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency  
**Figure 4-179. TX HD2 vs Digital Amplitude and Output Frequency at 4.9GHz**



Matching at 4.9GHz,  $f_{DAC} = 11.79648\text{GSPS}$ , interleave mode, normalized to output power at harmonic frequency  
**Figure 4-180. TX HD3 vs Digital Amplitude and Output Frequency at 4.9GHz**



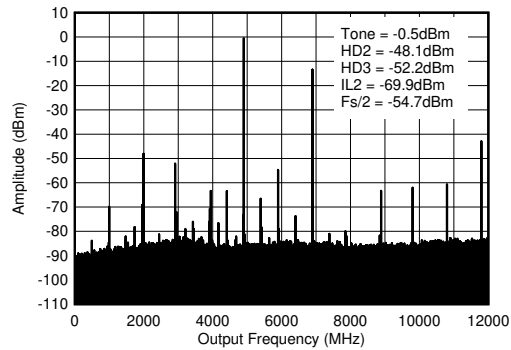
$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode, 4.9GHz matching, includes PCB and cable losses.  $ILn = f_s/n \pm f_{OUT}$ .  
**Figure 4-181. TX Single Tone (-12 dBFS) Output Spectrum at 4.9GHz ( $0-f_{DAC}$ )**



$f_{DAC} = 11796.48\text{MSPS}$ , interleave mode, 4.9GHz matching, includes PCB and cable losses.  $ILn = f_s/n \pm f_{OUT}$ .  
**Figure 4-182. TX Single Tone (-6 dBFS) Output Spectrum at 4.9GHz ( $0-f_{DAC}$ )**

#### 4.12.5 TX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated



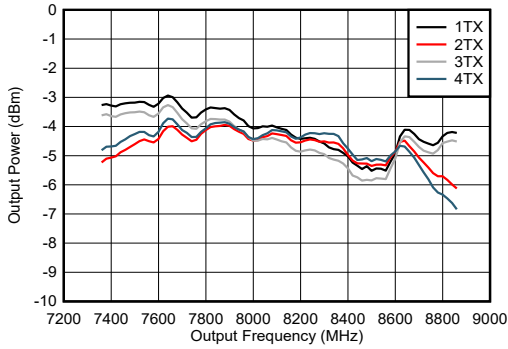
$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode, 4.9GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{\text{OUT}}$ .

**Figure 4-183. TX Single Tone (-1 dBFS) Output Spectrum at 4.9GHz (0- $f_{\text{DAC}}$ )**



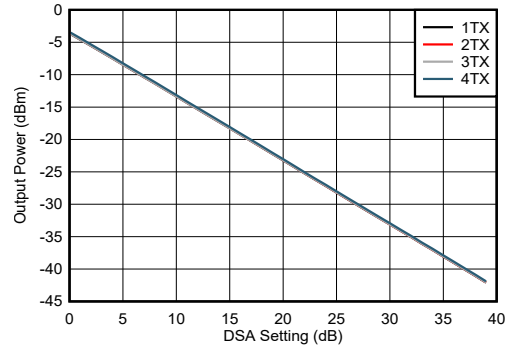
### 4.12.6 TX Typical Characteristics at 8.1GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1GHz matching



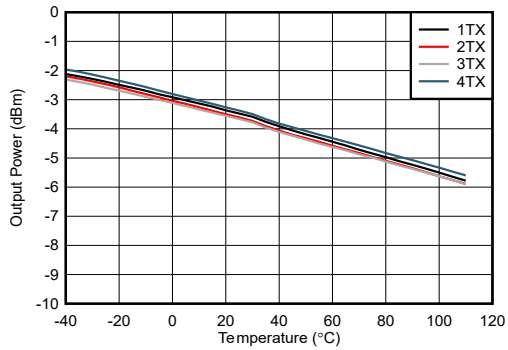
includes PCB and cable losses.

**Figure 4-184. TX Output Power vs Frequency at 8.11GHz**



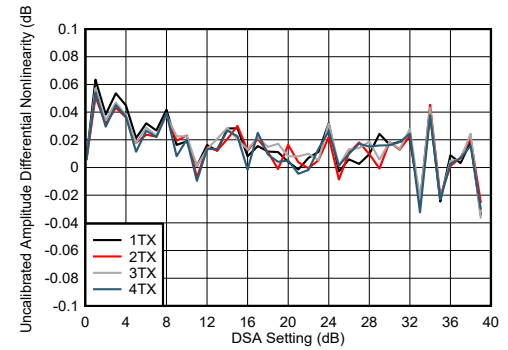
includes PCB and cable losses.

**Figure 4-185. TX Output Power vs DSA Setting at 8.11GHz**

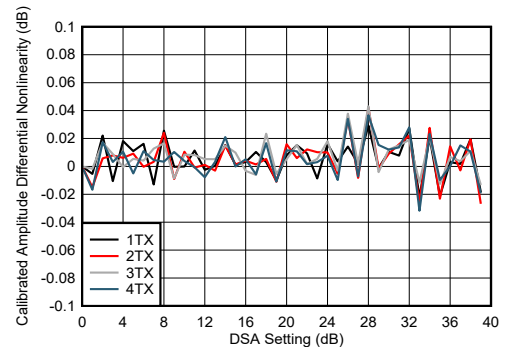


includes PCB and cable losses.

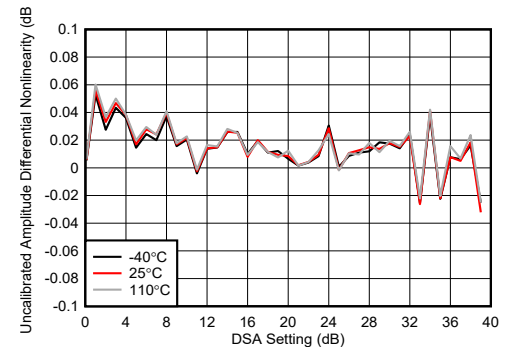
**Figure 4-186. TX Output Power vs Temperature at 8.11GHz**



**Figure 4-187. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11GHz**



**Figure 4-188. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11GHz**



**Figure 4-189. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11GHz**

### 4.12.6 TX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1GHz matching

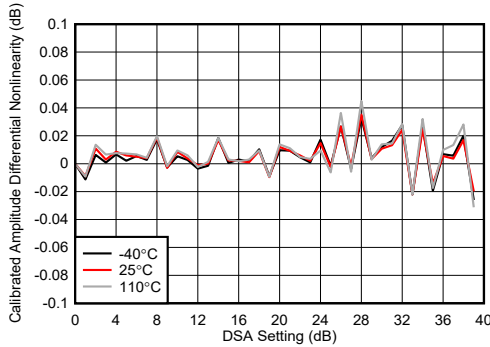


Figure 4-190. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11GHz

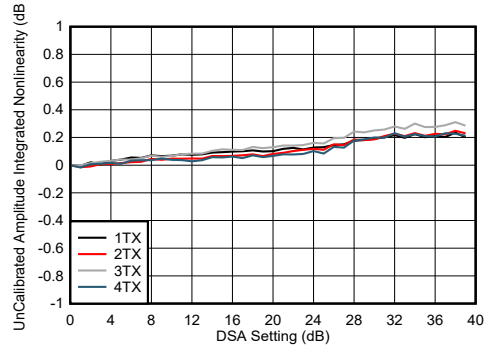


Figure 4-191. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11GHz

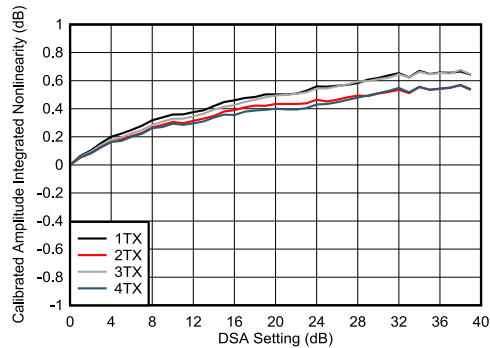


Figure 4-192. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11GHz

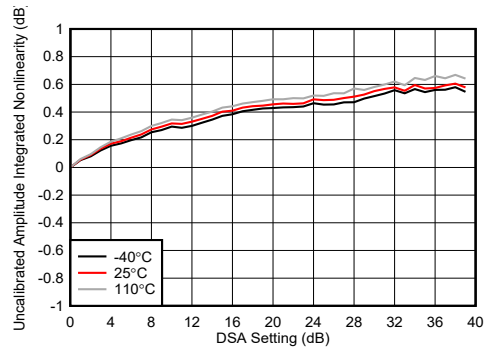


Figure 4-193. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11GHz

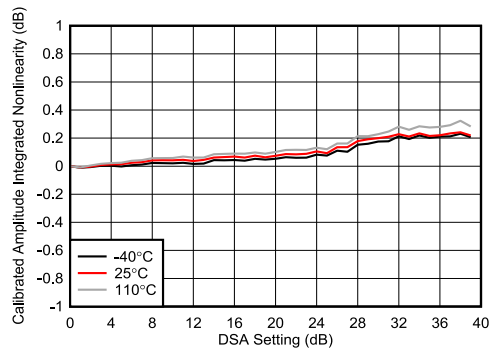


Figure 4-194. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11GHz

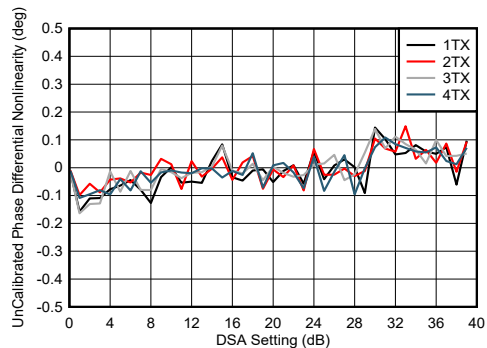
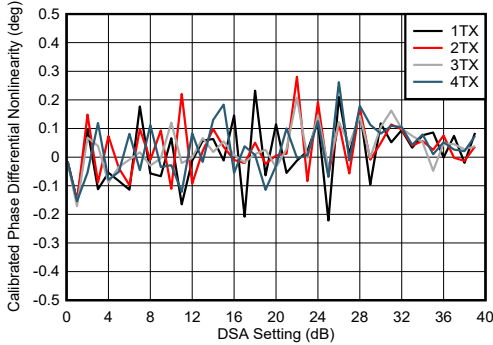


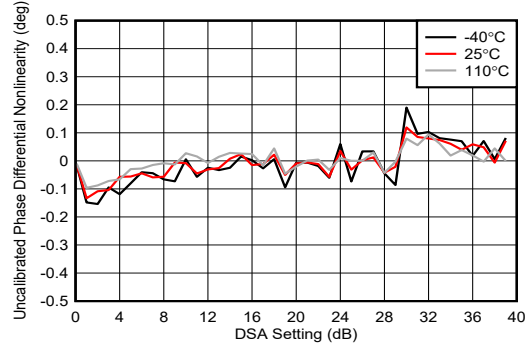
Figure 4-195. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11GHz

### 4.12.6 TX Typical Characteristics at 8.1GHz (continued)

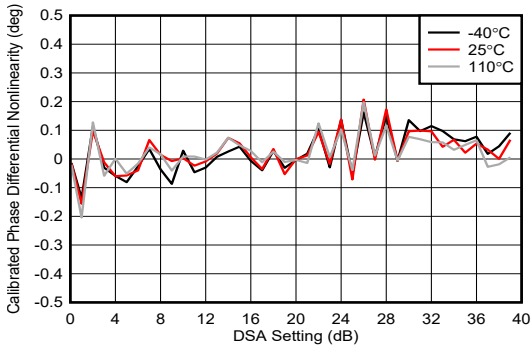
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1GHz matching



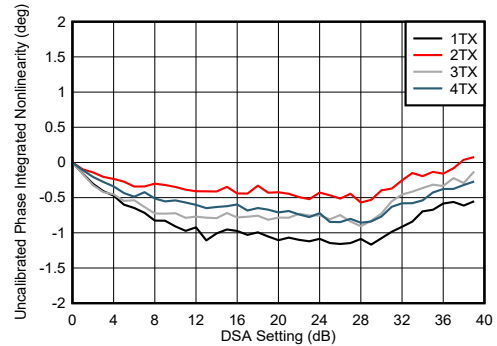
**Figure 4-196. TX DSA Calibrated Phase Differential Nonlinearity at 8.11GHz**



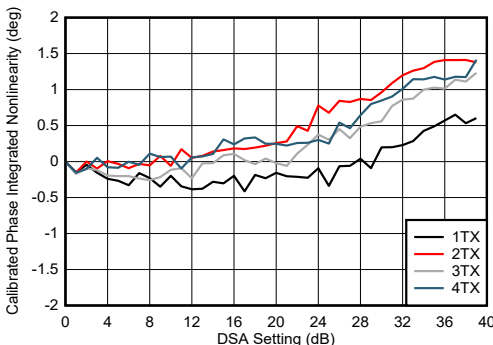
**Figure 4-197. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11GHz**



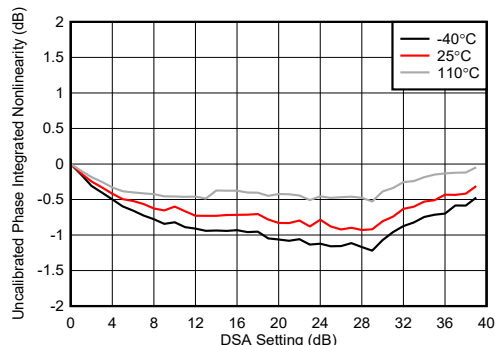
**Figure 4-198. TX DSA Calibrated Phase Differential Nonlinearity at 8.11GHz**



**Figure 4-199. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.11GHz**



**Figure 4-200. TX DSA Calibrated Phase Integrated Nonlinearity at 8.11GHz**



**Figure 4-201. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.11GHz**

### 4.12.6 TX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1GHz matching

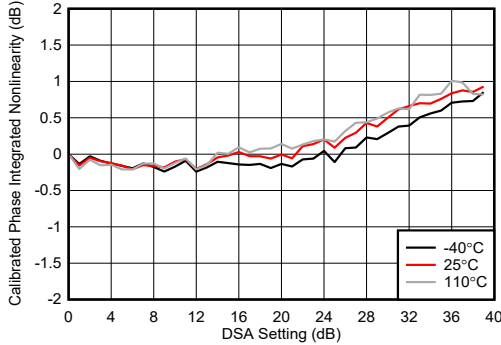
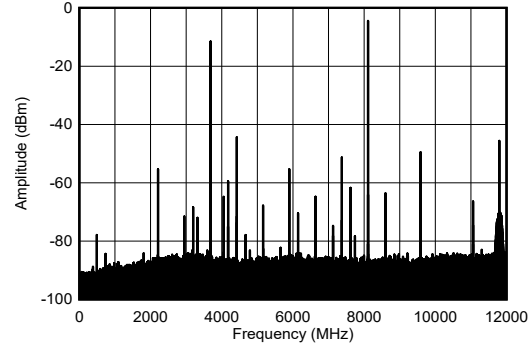
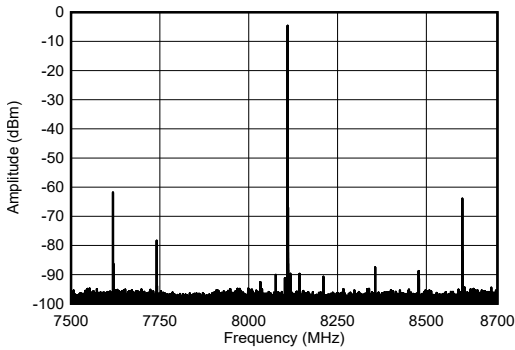


Figure 4-202. TX DSA Calibrated Phase Integrated Nonlinearity at 8.11GHz



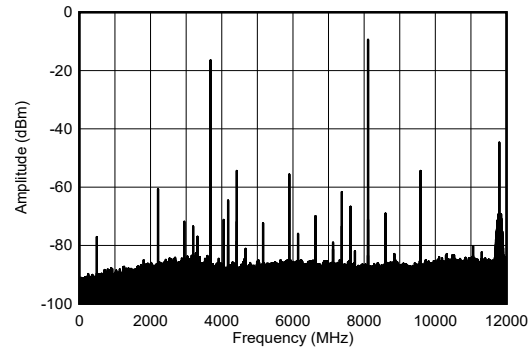
-1dBFS

Figure 4-203. TX Single Tone Output Spectrum at 8.11GHz



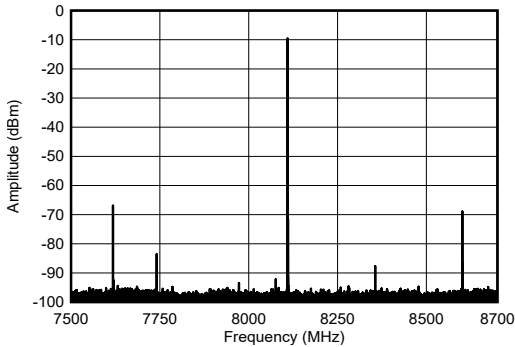
-1dBFS

Figure 4-204. TX Single Tone Output Spectrum at 8.11GHz



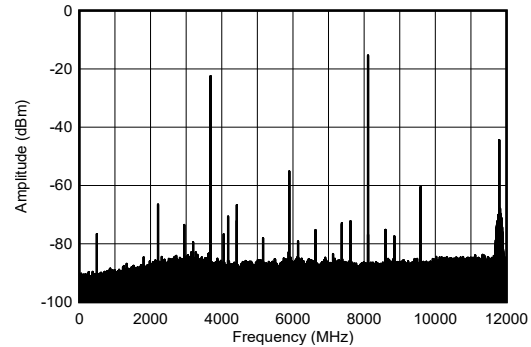
-6dBFS

Figure 4-205. TX Single Tone Output Spectrum at 8.11GHz



-6dBFS

Figure 4-206. TX Single Tone Output Spectrum at 8.11GHz

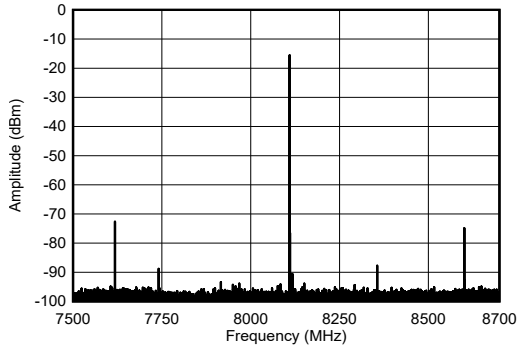


-12dBFS

Figure 4-207. TX Single Tone Output Spectrum at 8.11GHz

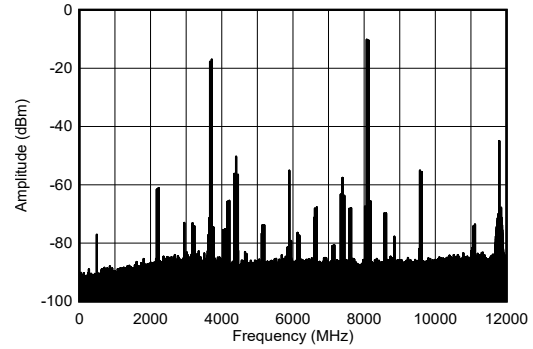
### 4.12.6 TX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1GHz matching



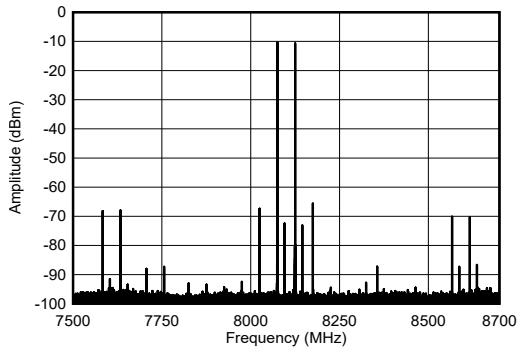
-12dBFS

**Figure 4-208. TX Single Tone Output Spectrum at 8.11GHz**



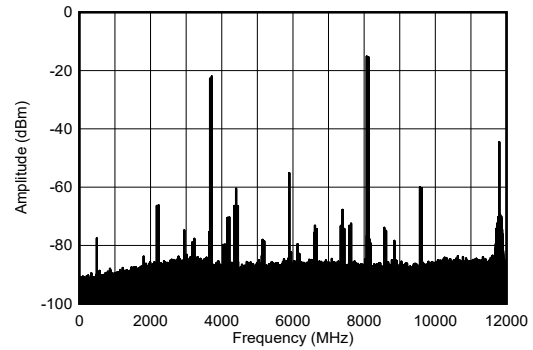
50MHz tone spacing, -7dBFS each tone

**Figure 4-209. TX Dual Tone Output Spectrum at 8.11GHz**



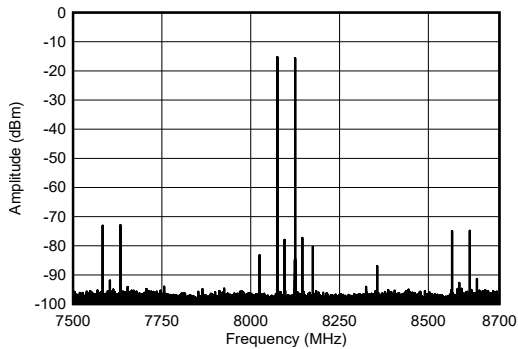
50MHz tone spacing, -7dBFS each tone

**Figure 4-210. TX Dual Tone Output Spectrum at 8.11GHz**



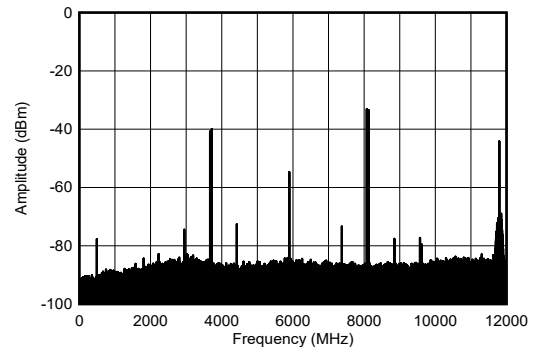
50MHz tone spacing, -12dBFS each tone

**Figure 4-211. TX Dual Tone Output Spectrum at 8.11GHz**



50MHz tone spacing, -12dBFS each tone

**Figure 4-212. TX Dual Tone Output Spectrum at 8.11GHz**

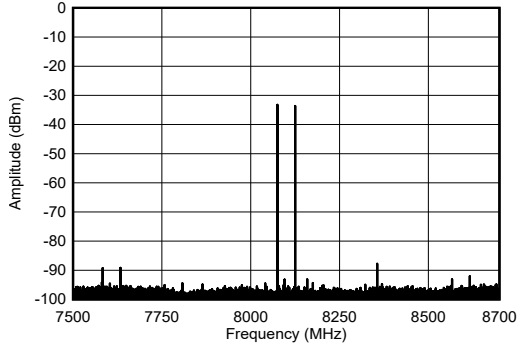


50MHz tone spacing, -30dBFS each tone

**Figure 4-213. TX Dual Tone Output Spectrum at 8.11GHz**

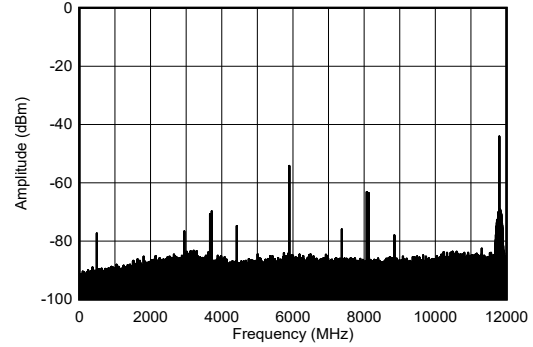
### 4.12.6 TX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1GHz matching



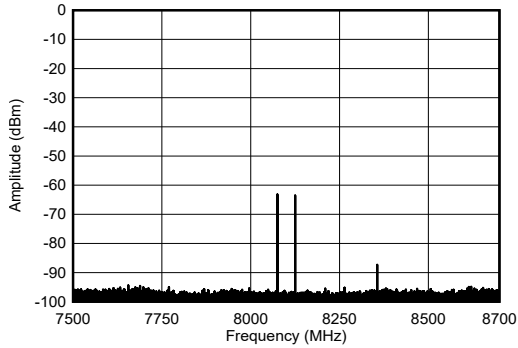
50MHz tone spacing, -30dBFS each tone

Figure 4-214. TX Dual Tone Output Spectrum at 8.11GHz



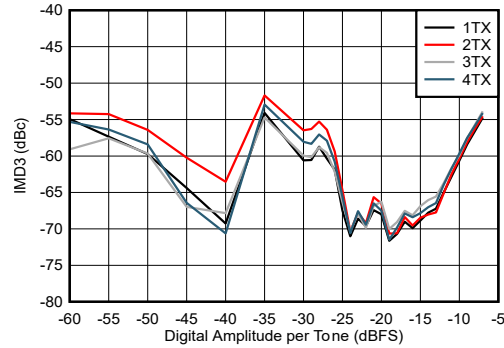
50MHz tone spacing, -60dBFS each tone

Figure 4-215. TX Dual Tone Output Spectrum at 8.11GHz



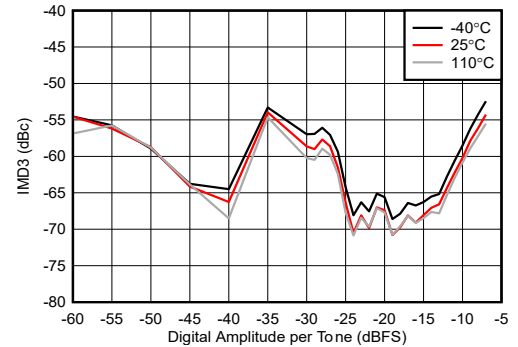
50MHz tone spacing, -60dBFS each tone

Figure 4-216. TX Dual Tone Output Spectrum at 8.11GHz



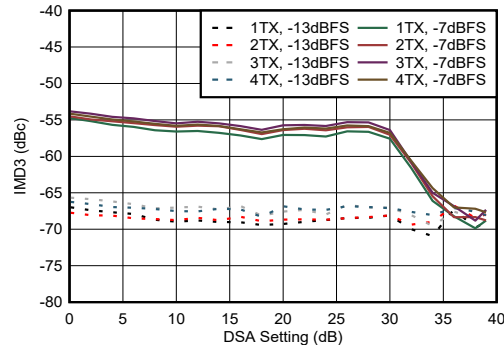
-7dBFS each tone, 50MHz tone spacing

Figure 4-217. TX IMD3 vs Digital Amplitude at 8.11GHz



-7dBFS each tone, 50MHz tone spacing

Figure 4-218. TX IMD3 vs Digital Amplitude at 8.11GHz

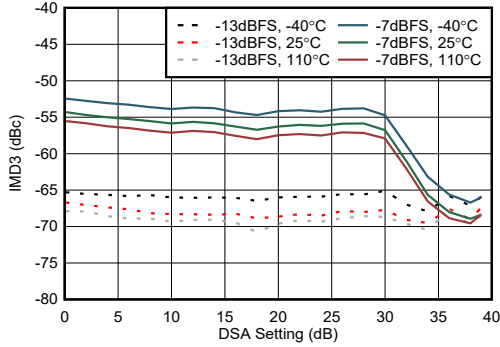


50MHz tone spacing

Figure 4-219. TX IMD3 vs DSA Setting at 8.11GHz

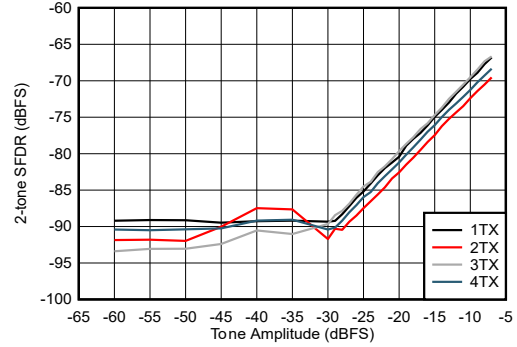
**4.12.6 TX Typical Characteristics at 8.1GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1GHz matching



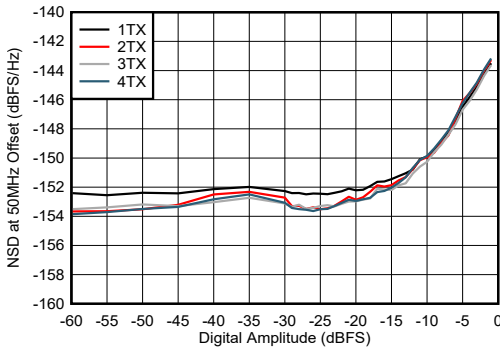
50 MHz tone spacing

**Figure 4-220. TX IMD3 vs DSA Setting at 8.11GHz**



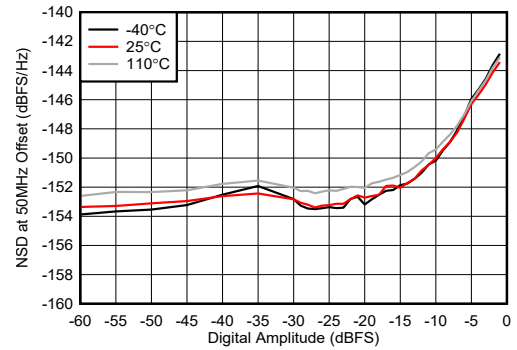
50 MHz tone spacing

**Figure 4-221. TX 2-Tone SFDR vs Digital Amplitude at 8.11GHz**



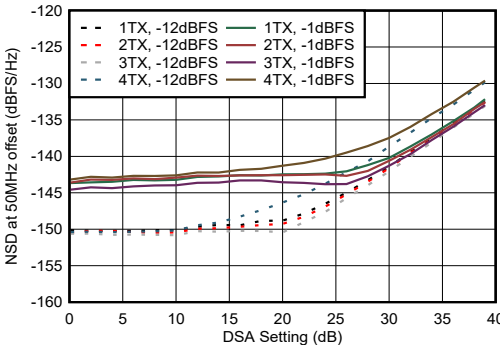
50 MHz offset

**Figure 4-222. TX NSD vs Digital Amplitude at 8.11GHz**



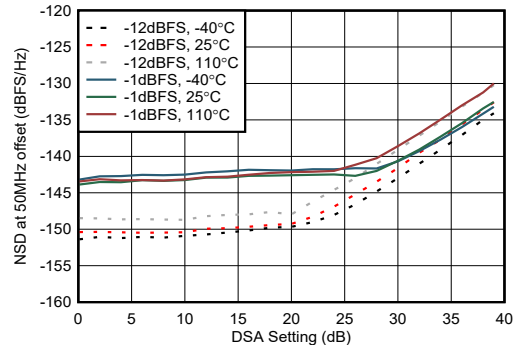
50 MHz offset

**Figure 4-223. TX NSD vs Digital Amplitude at 8.11GHz**



50 MHz offset

**Figure 4-224. TX NSD vs DSA Setting at 8.11GHz**



50 MHz offset

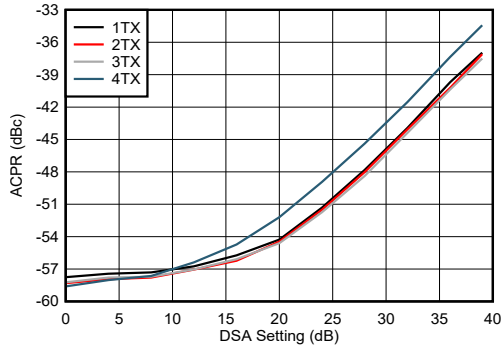
**Figure 4-225. TX NSD vs DSA Setting at 8.11GHz**

**AFE7950-SP**

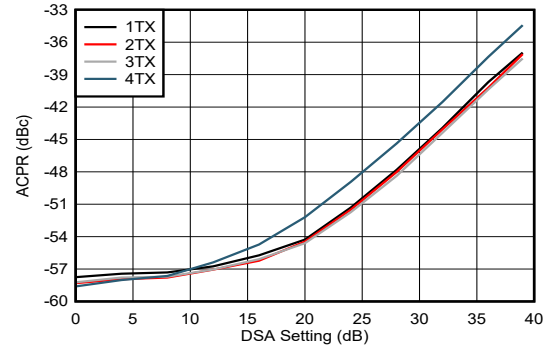
SBASAG7A – MARCH 2024 – REVISED AUGUST 2024

**4.12.6 TX Typical Characteristics at 8.1GHz (continued)**

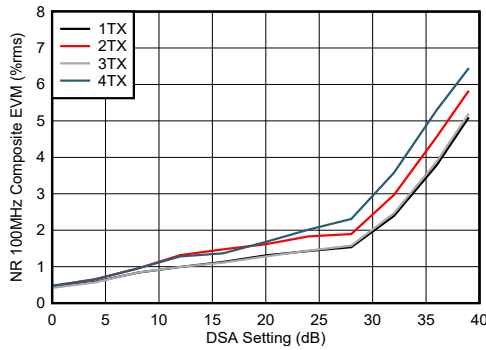
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1GHz matching



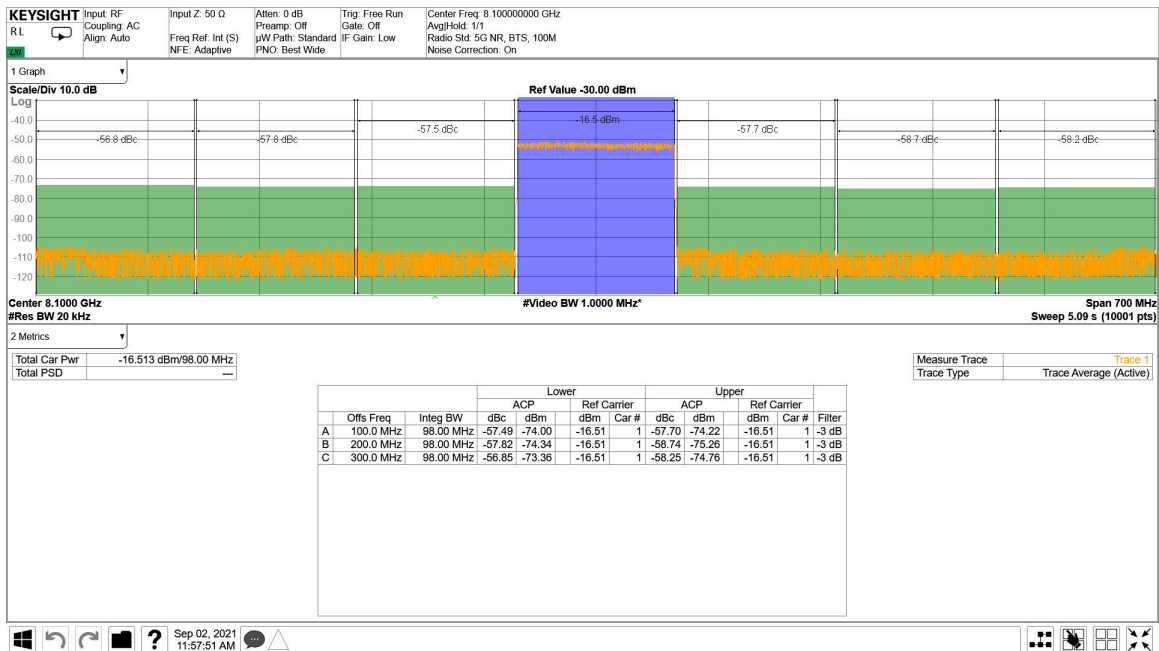
**Figure 4-226. TX NR100MHz ACPR vs DSA Setting 8.11GHz**



**Figure 4-227. TX NR100MHz alt-ACPR vs DSA Setting 8.11GHz**



**Figure 4-228. TX NR100MHz EVM vs DSA Setting 8.11GHz**



**Figure 4-229. TX 100MHz NR Output Spectrum at 8.11GHz**



### 4.12.6 TX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1GHz matching

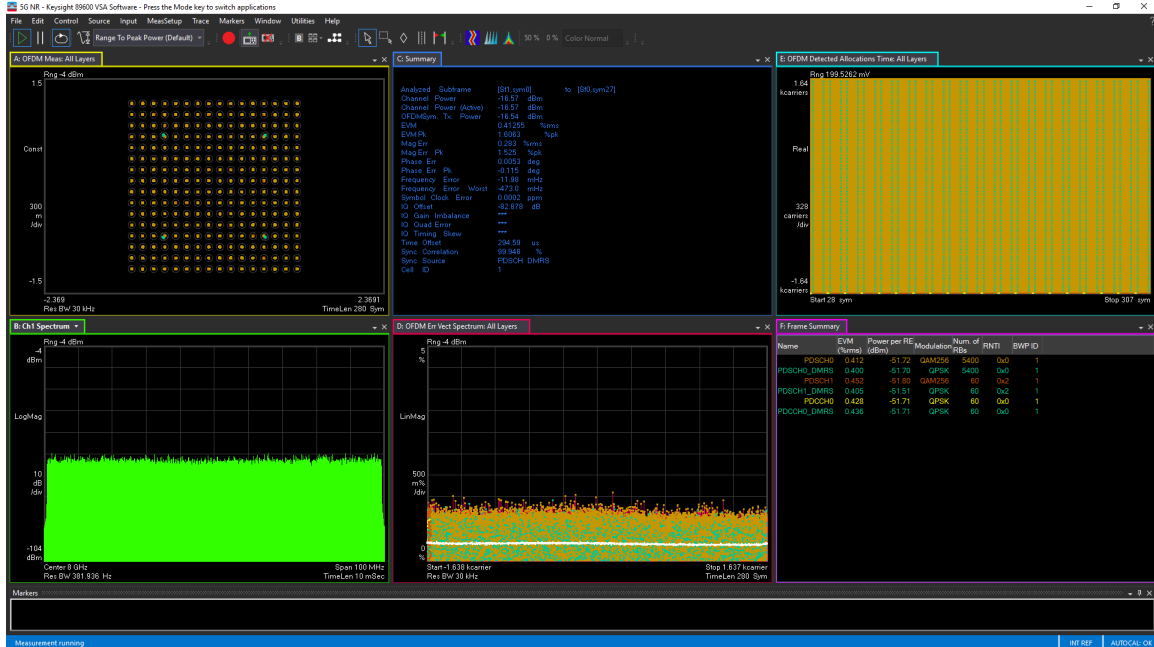


Figure 4-230. TX 100MHz NR EVM at 8.11GHz

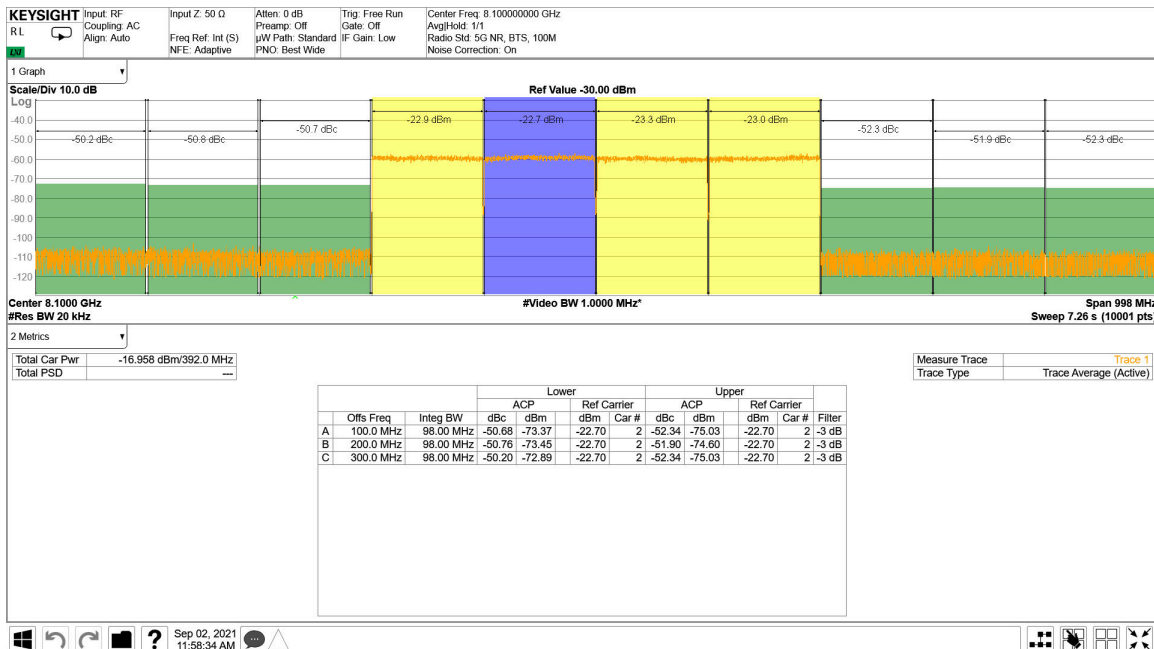


Figure 4-231. TX 4x100MHz NR Output Spectrum 8.11GHz

### 4.12.6 TX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, 8.1GHz matching

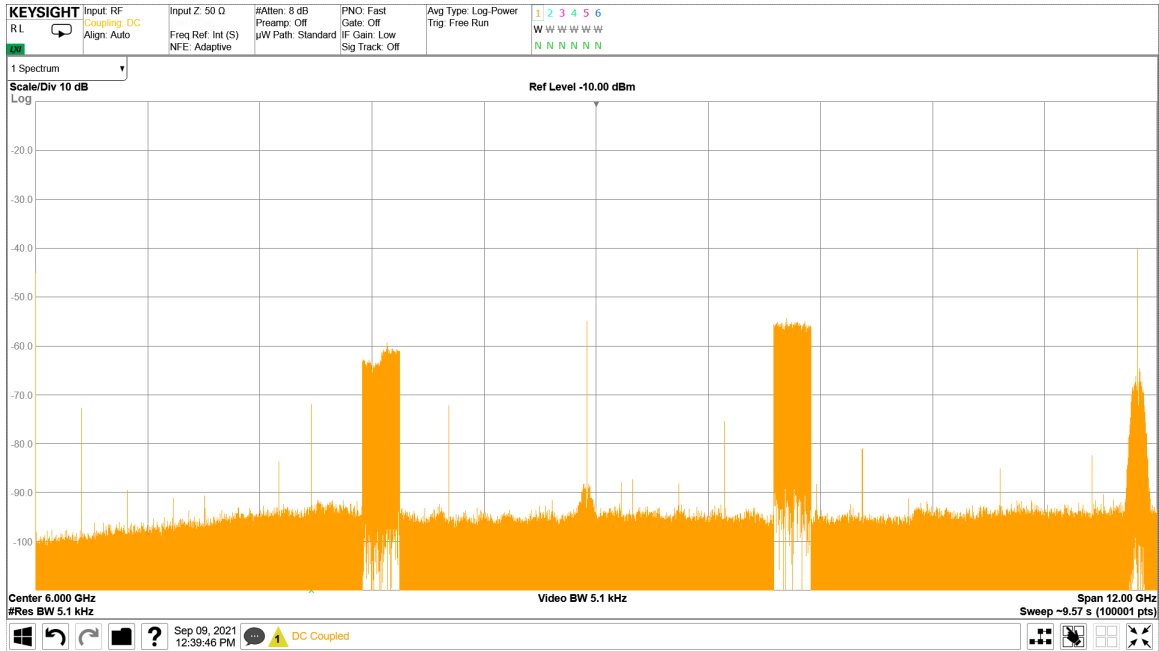
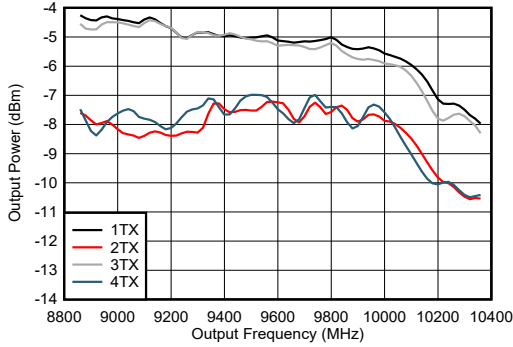


Figure 4-232. TX 4x100MHz NR Output Spectrum 8.11GHz

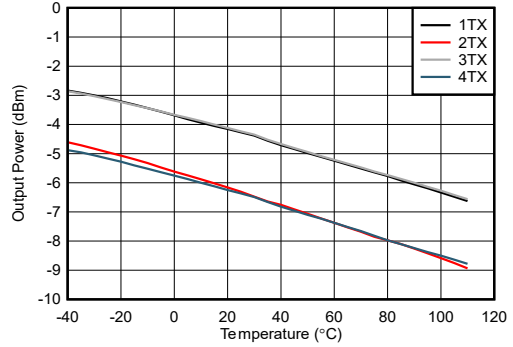
### 4.12.7 TX Typical Characteristics at 9.6GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



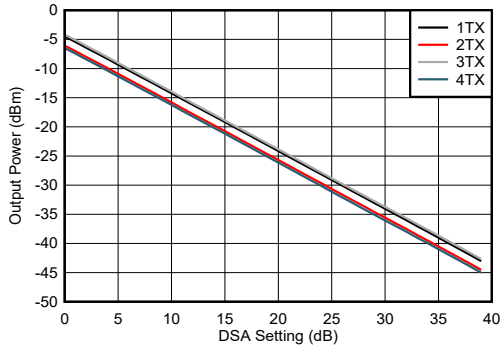
Includes PCB and cable losses.

**Figure 4-233. TX Output Power vs Frequency at 9.61GHz**



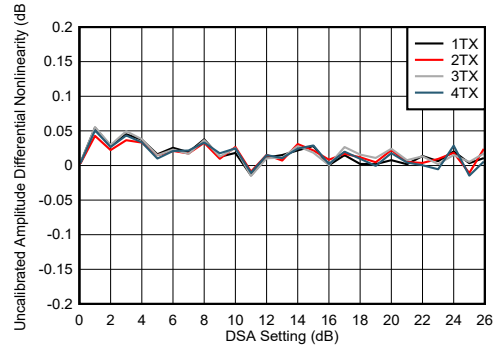
Includes PCB and cable losses.

**Figure 4-234. TX Output Power vs Frequency at 9.61GHz**

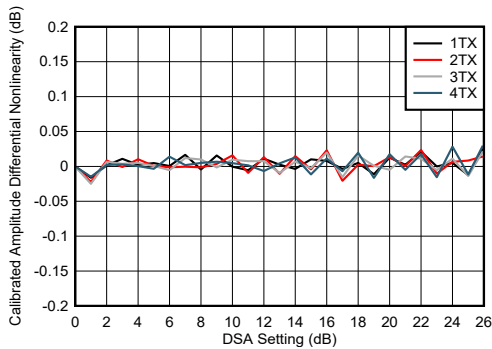


Includes PCB and cable losses.

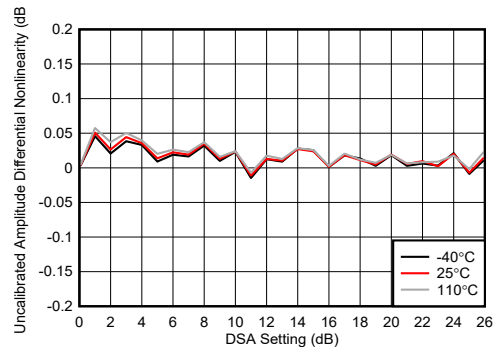
**Figure 4-235. TX Output Power vs DSA Setting at 9.61GHz**



**Figure 4-236. TX DSA Uncalibrated Amplitude Differential Nonlinearity**



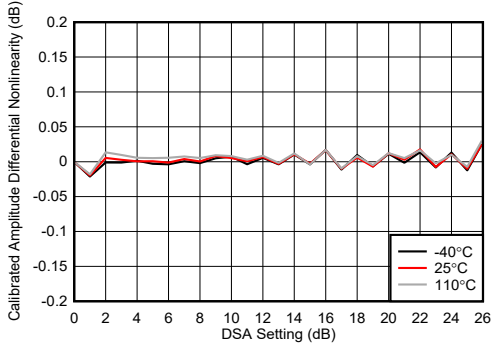
**Figure 4-237. TX DSA Calibrated Amplitude Differential Nonlinearity**



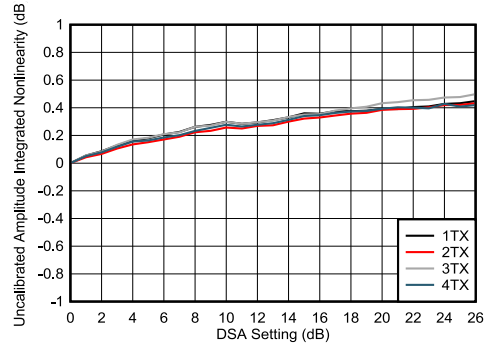
**Figure 4-238. TX DSA Uncalibrated Amplitude Differential Nonlinearity**

**4.12.7 TX Typical Characteristics at 9.6GHz (continued)**

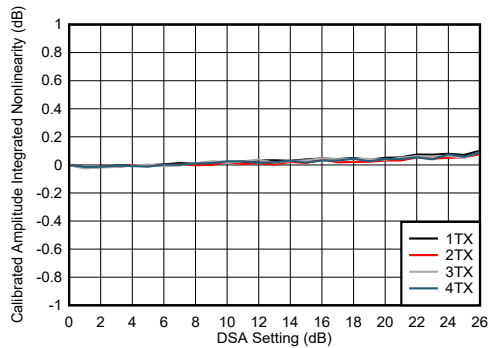
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



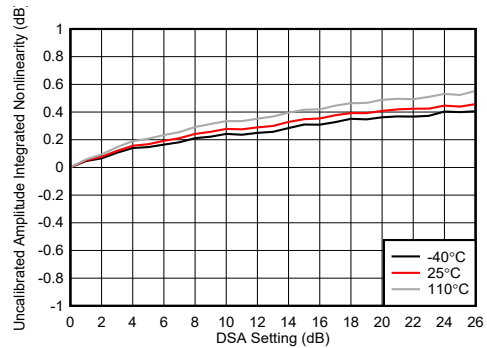
**Figure 4-239. TX DSA Calibrated Amplitude Differential Nonlinearity**



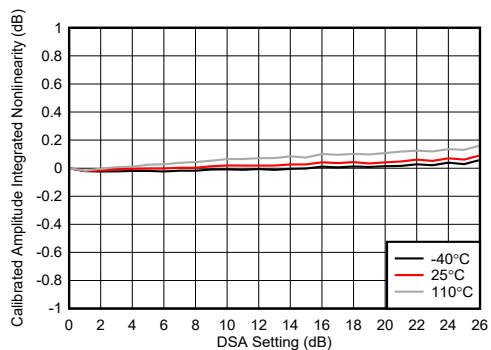
**Figure 4-240. TX DSA Uncalibrated Amplitude Integrated Nonlinearity**



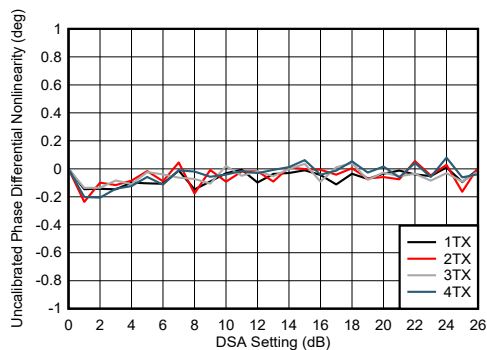
**Figure 4-241. TX DSA Calibrated Amplitude Integrated Nonlinearity**



**Figure 4-242. TX DSA Uncalibrated Amplitude Integrated Nonlinearity**



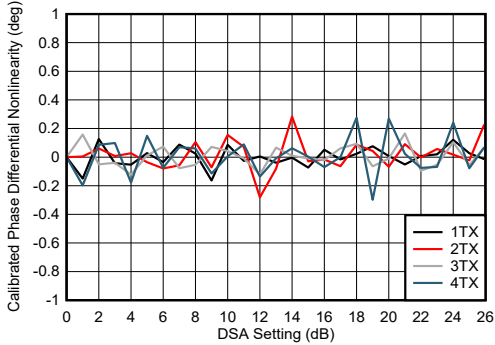
**Figure 4-243. TX DSA Calibrated Amplitude Integrated Nonlinearity**



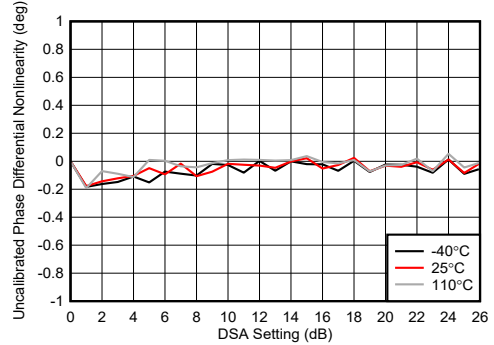
**Figure 4-244. TX DSA Uncalibrated Phase Differential Nonlinearity**

**4.12.7 TX Typical Characteristics at 9.6GHz (continued)**

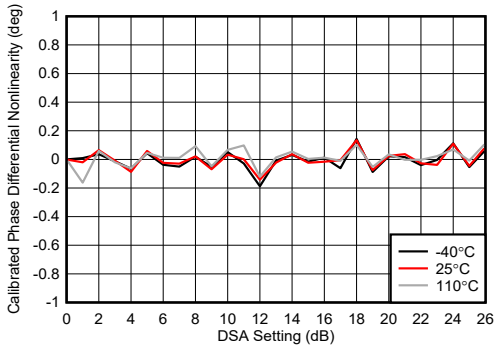
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



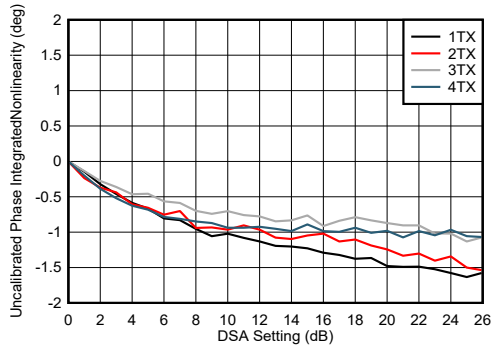
**Figure 4-245. TX DSA Calibrated Phase Differential Nonlinearity**



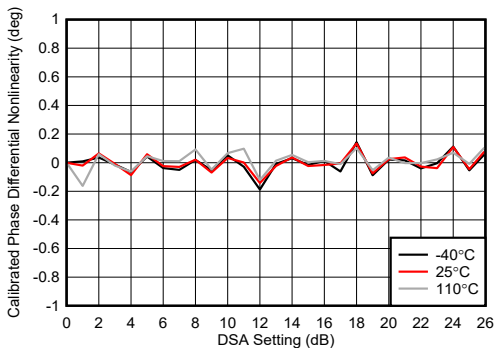
**Figure 4-246. TX DSA Uncalibrated Phase Differential Nonlinearity**



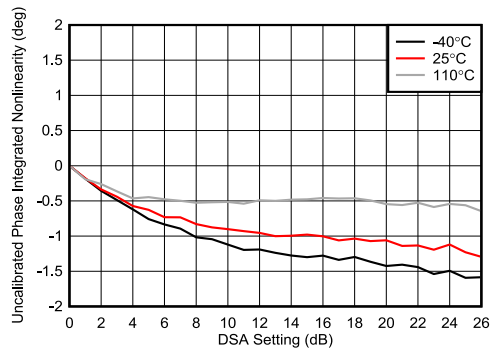
**Figure 4-247. TX DSA Calibrated Phase Differential Nonlinearity**



**Figure 4-248. TX DSA Uncalibrated Phase Integrated Nonlinearity**



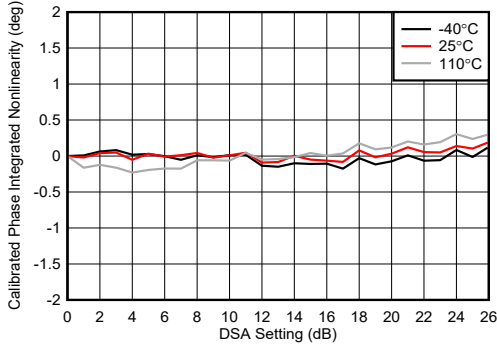
**Figure 4-249. TX DSA Calibrated Phase Integrated Nonlinearity**



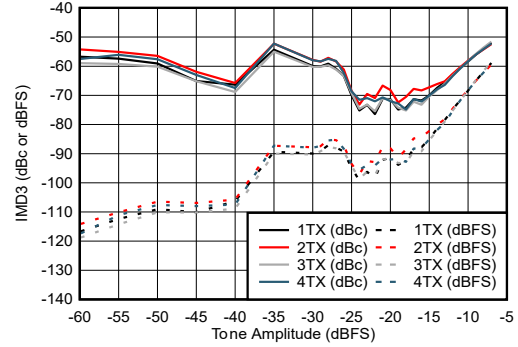
**Figure 4-250. TX DSA Uncalibrated Phase Integrated Nonlinearity**

**4.12.7 TX Typical Characteristics at 9.6GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching

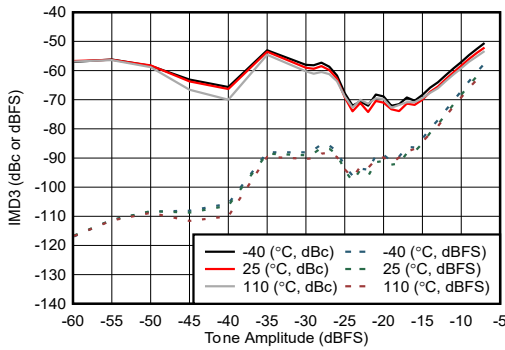


**Figure 4-251. TX DSA Calibrated Amplitude Integrated Nonlinearity**



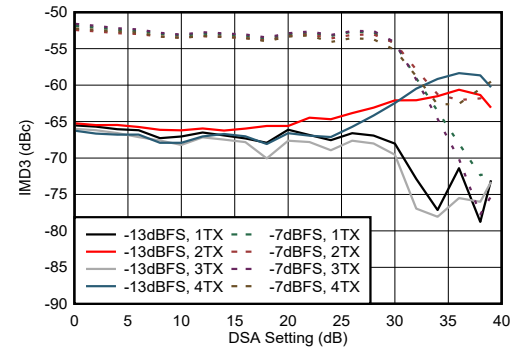
50MHz tone spacing

**Figure 4-252. TX IMD3 vs Digital Amplitude at 9.61GHz**



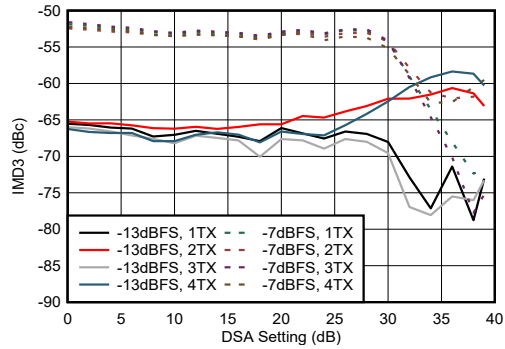
50MHz tone spacing

**Figure 4-253. TX IMD3 vs Digital Amplitude at 9.61GHz**



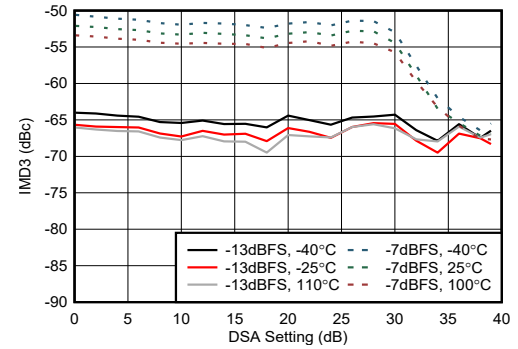
50MHz tone spacing

**Figure 4-254. TX IMD3 vs DSA Setting at 9.61GHz**



50MHz tone spacing

**Figure 4-255. TX IMD3 vs DSA Setting at 9.61GHz**

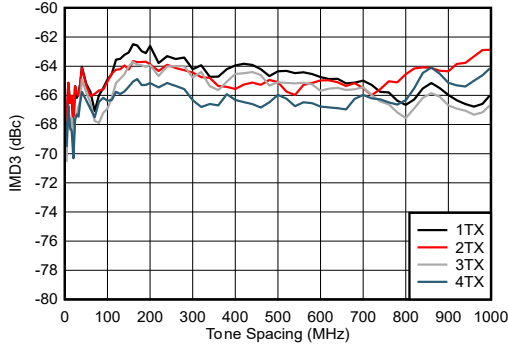


50MHz tone spacing

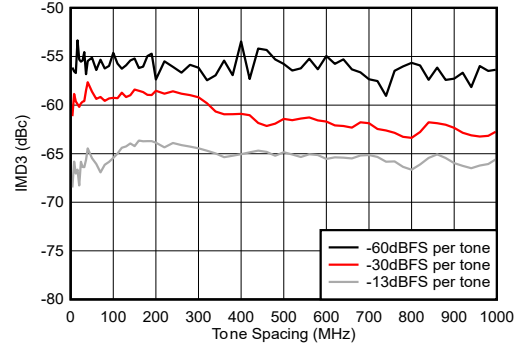
**Figure 4-256. TX IMD3 vs DSA Setting at 9.61GHz**

**4.12.7 TX Typical Characteristics at 9.6GHz (continued)**

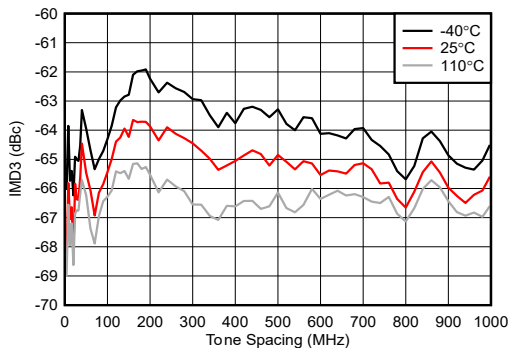
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



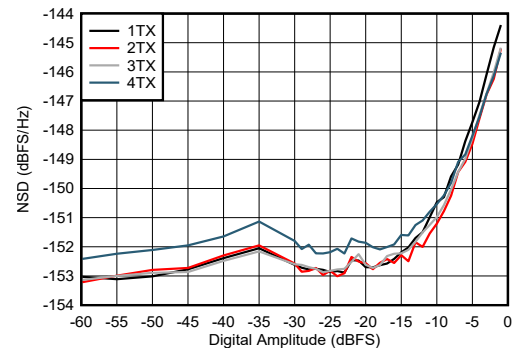
**Figure 4-257. TX IMD3 vs Tone Spacing at 9.61GHz**



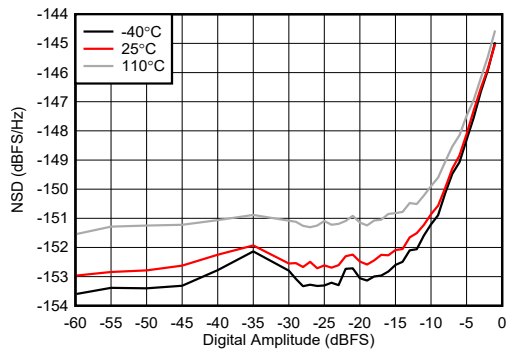
**Figure 4-258. TX IMD3 vs Tone Spacing at 9.61GHz**



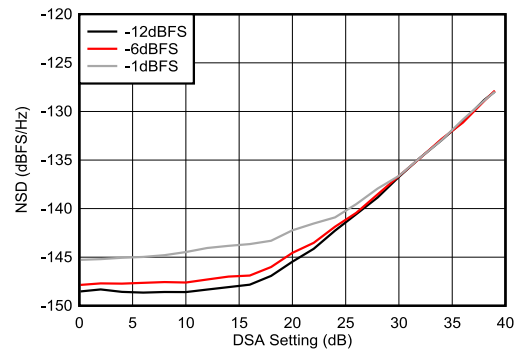
**Figure 4-259. TX IMD3 vs Tone Spacing at 9.61GHz**



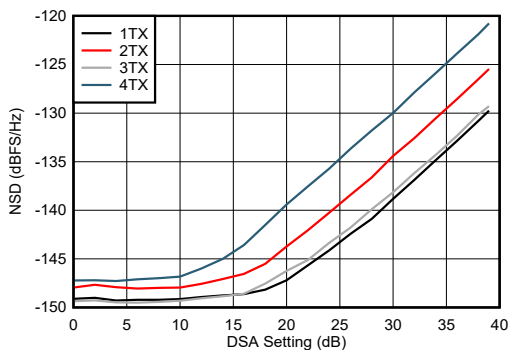
**Figure 4-260. TX NSD vs Digital Amplitude at 9.61GHz**



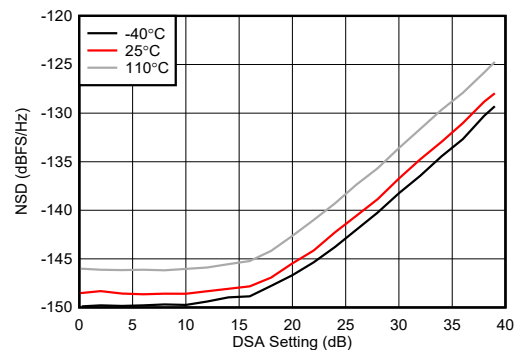
**Figure 4-261. TX NSD vs Digital Amplitude at 9.61GHz**



**Figure 4-262. TX NSD vs DSA Setting at 9.61GHz**



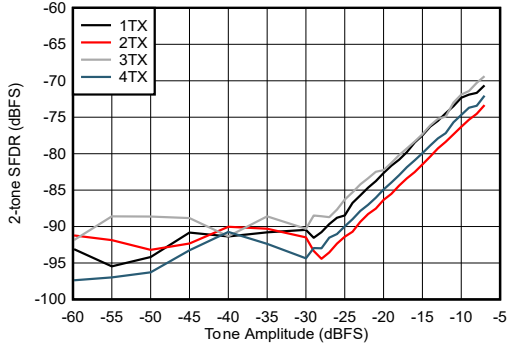
**Figure 4-263. TX NSD vs DSA Setting at 9.61GHz**



**Figure 4-264. TX NSD vs DSA Setting at 9.61GHz**

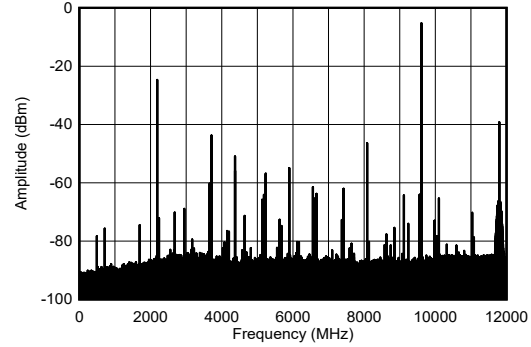
**4.12.7 TX Typical Characteristics at 9.6GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56MSPS,  $f_{DAC} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{OUT} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



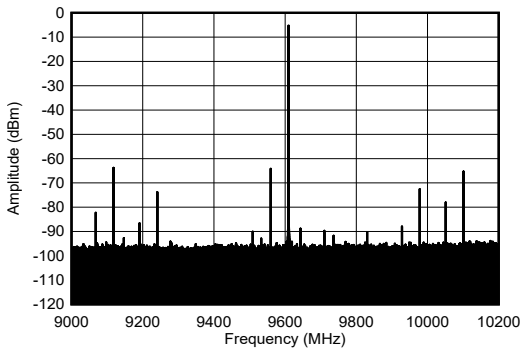
50 MHz tone spacing

**Figure 4-265. TX 2-tone SFDR vs Digital Amplitude at 9.61GHz**



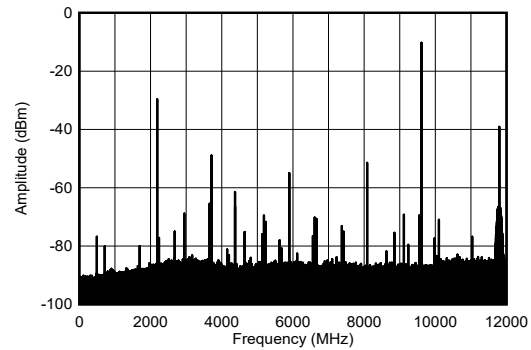
Includes PCB and cable losses.

**Figure 4-266. TX Single Tone Spectrum at 9.61GHz and -1dBFS (wideband)**



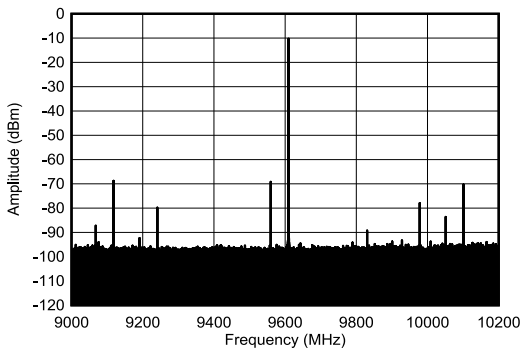
Includes PCB and cable losses.

**Figure 4-267. TX Single Tone Spectrum at 9.61GHz and -1dBFS (1.2GHz BW)**



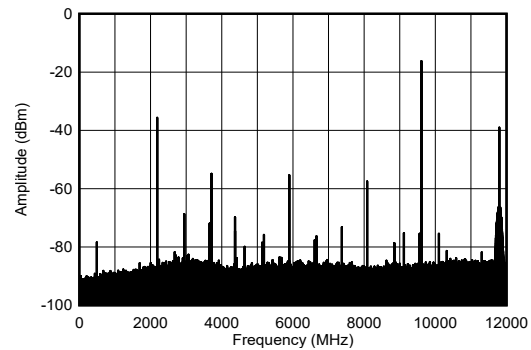
Includes PCB and cable losses.

**Figure 4-268. TX Single Tone Spectrum at 9.61GHz and -6dBFS (wideband)**



Includes PCB and cable losses.

**Figure 4-269. TX Single Tone Spectrum at 9.61GHz and -6dBFS (1.2GHz BW)**



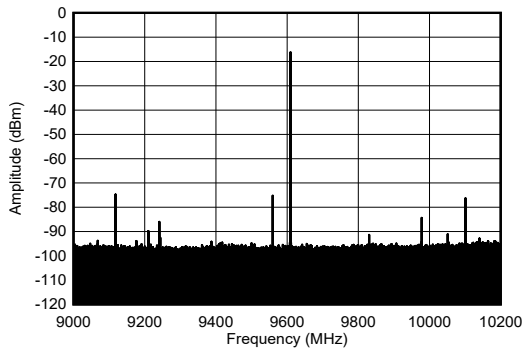
Includes PCB and cable losses.

**Figure 4-270. TX Single Tone Spectrum at 9.61GHz and -12dBFS (wideband)**



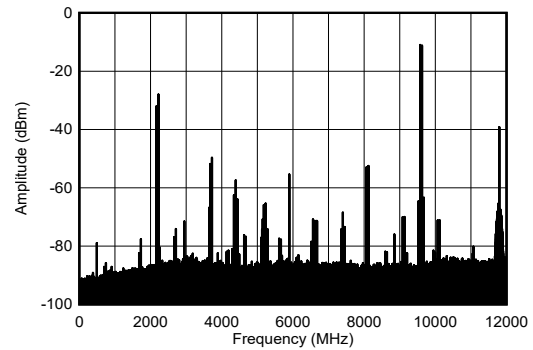
#### 4.12.7 TX Typical Characteristics at 9.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



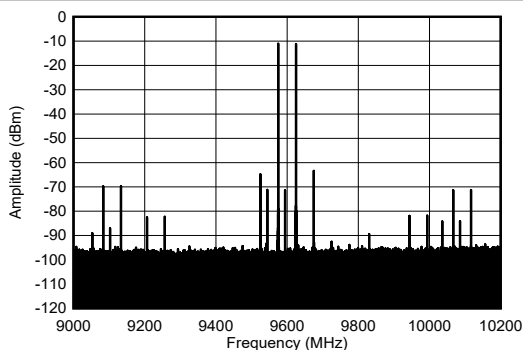
Includes PCB and cable losses.

**Figure 4-271. TX Single Tone Spectrum at 9.61GHz and -12dBFS (1.2GHz BW)**



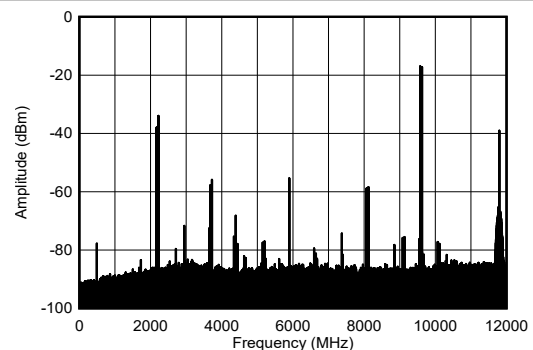
Includes PCB and cable losses, 50MHz tone spacing.

**Figure 4-272. TX 2-Tone Spectrum at 9.61GHz and -7dBFS (wideband)**



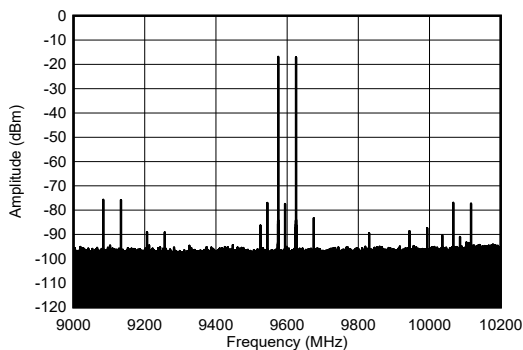
Includes PCB and cable losses, 50MHz tone spacing.

**Figure 4-273. TX 2-Tone Spectrum at 9.61GHz and -7dBFS (1.2GHz BW)**



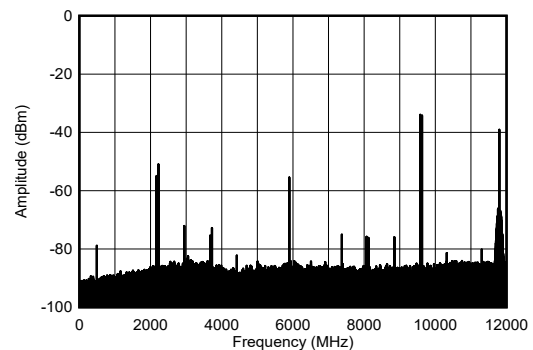
Includes PCB and cable losses, 50MHz tone spacing.

**Figure 4-274. TX 2-Tone Spectrum at 9.61GHz and -13dBFS (wideband)**



Includes PCB and cable losses, 50MHz tone spacing.

**Figure 4-275. TX 2-Tone Spectrum at 9.61GHz and -13dBFS (1.2GHz BW)**

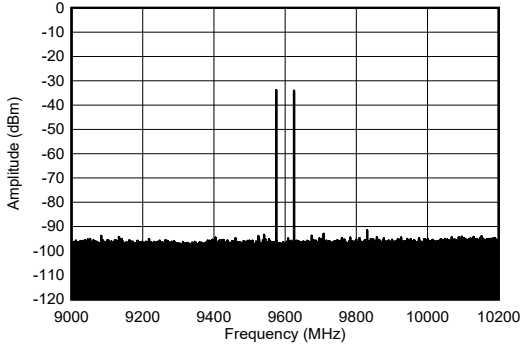


Includes PCB and cable losses, 50MHz tone spacing.

**Figure 4-276. TX 2-Tone Spectrum at 9.61GHz and -30dBFS Each (wideband)**

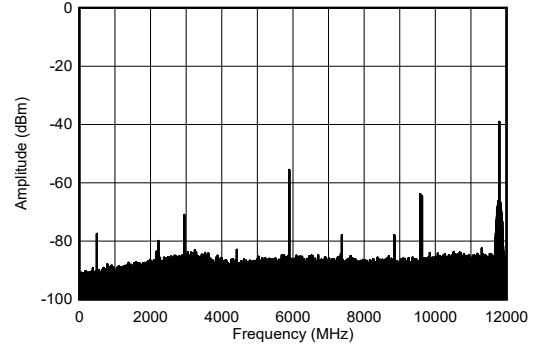
### 4.12.7 TX Typical Characteristics at 9.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



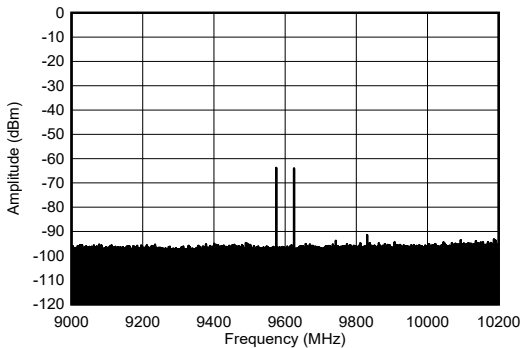
Includes PCB and cable losses, 50MHz tone spacing.

**Figure 4-277. TX 2-Tone Spectrum at 9.61GHz and -30dBFS Each (1.2GHz BW)**



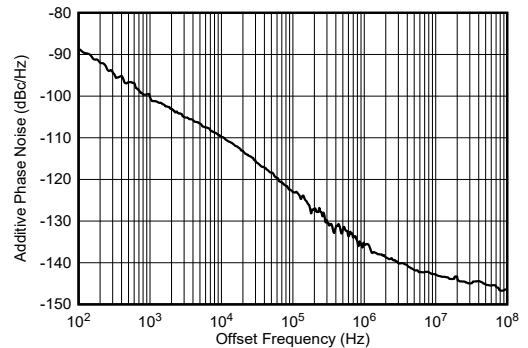
Includes PCB and cable losses, 50MHz tone spacing.

**Figure 4-278. TX 2-Tone Spectrum at 9.61GHz and -60dBFS Each (wideband)**



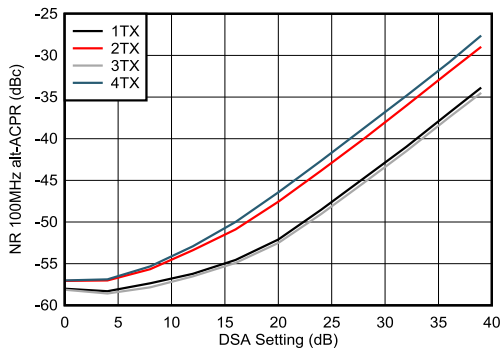
Includes PCB and cable losses, 50MHz tone spacing.

**Figure 4-279. TX 2-Tone Spectrum at 9.61GHz and -60dBFS Each (1.2GHz BW)**

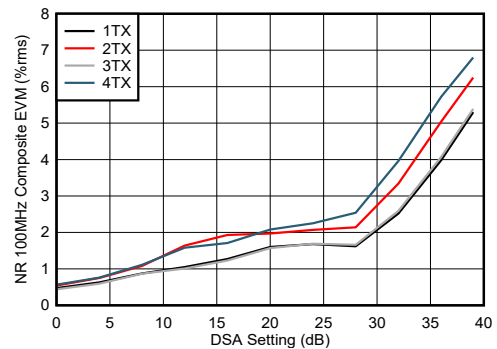


Single sideband, external clock mode, input clock phase noise removed

**Figure 4-280. TX Additive Phase Noise vs Offset Frequency at 9.61GHz**



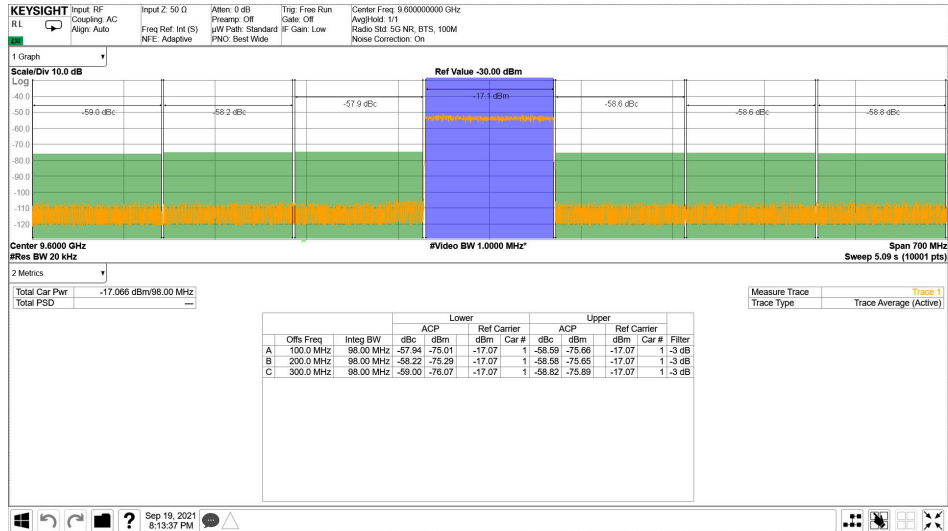
**Figure 4-281. TX NR100MHz alt-ACPR vs DSA Setting at 9.61GHz**



**Figure 4-282. TX NR100MHz EVM vs DSA Setting at 9.61GHz**

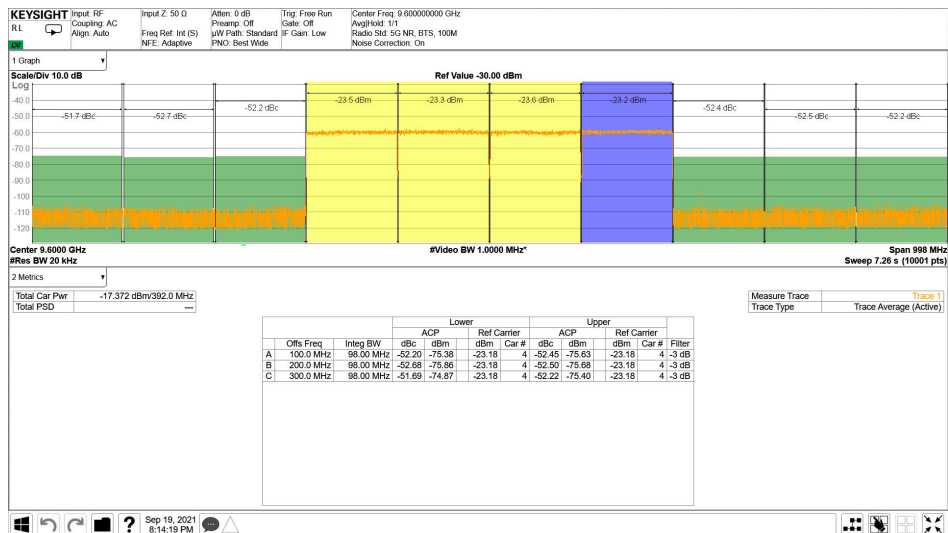
### 4.12.7 TX Typical Characteristics at 9.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 1474.56MSPS,  $f_{\text{DAC}} = 11796.48\text{MSPS}$  (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{OUT}} = -1\text{dBFS}$ , DSA = 0dB, Sin(x)/x enabled, DSA calibrated, 9.6GHz matching



Includes PCB and cable losses.

Figure 4-283. TX NR100MHz Output Spectrum at 9.61GHz

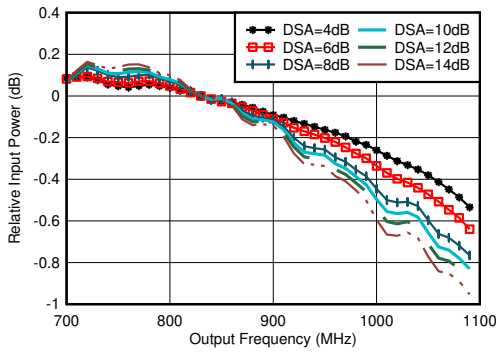


Includes PCB and cable losses.

Figure 4-284. TX 4xNR100MHz Output Spectrum at 9.61GHz

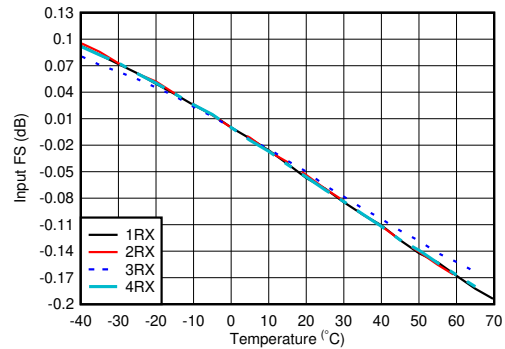
### 4.12.8 RX Typical Characteristics at 800MHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



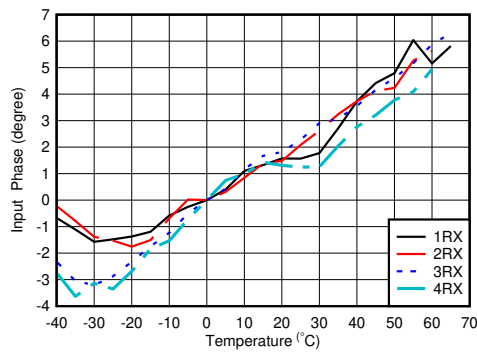
With 0.8GHz matching, normalized to 830MHz

**Figure 4-285. RX In-Band Gain Flatness for Channel 1RX,  $f_{IN} = 830\text{MHz}$**



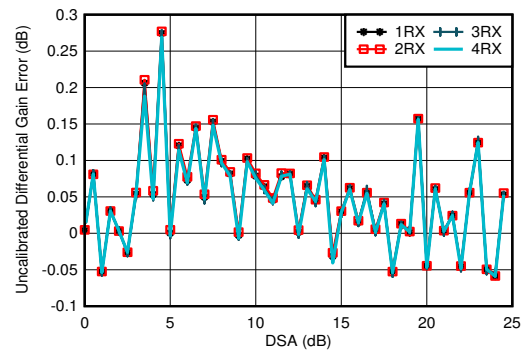
With 0.8GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

**Figure 4-286. RX Input Fullscale vs Temperature and Channel at 800MHz**



With 0.8GHz matching, normalized to phase at  $25^\circ\text{C}$

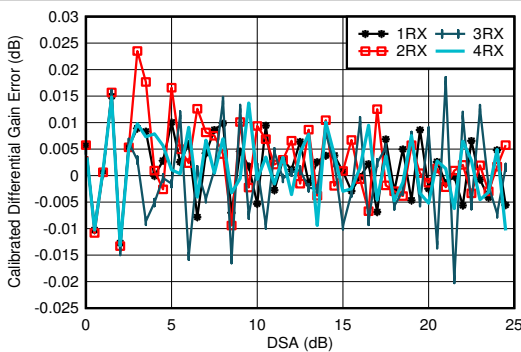
**Figure 4-287. RX Input Phase vs Temperature and DSA at  $f_{OUT} = 8.0\text{GHz}$**



With 0.8GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

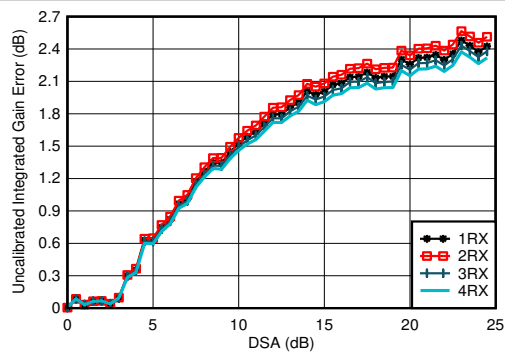
**Figure 4-288. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8GHz**



With 0.8GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

**Figure 4-289. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8GHz**



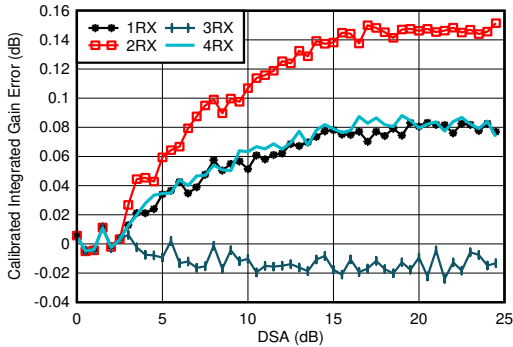
With 0.8GHz matching

Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-290. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8GHz**

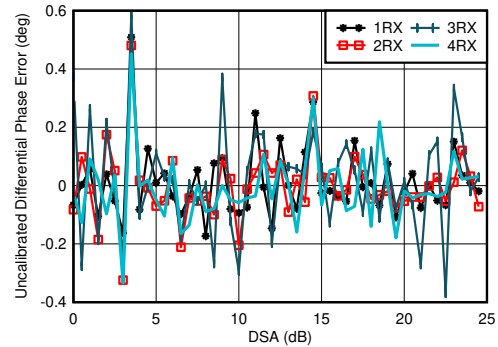
**4.12.8 RX Typical Characteristics at 800MHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



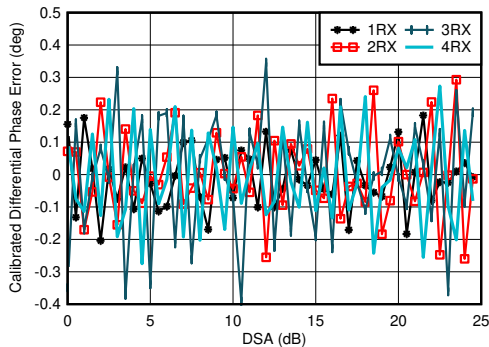
With 0.8GHz matching  
Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-291. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6GHz**



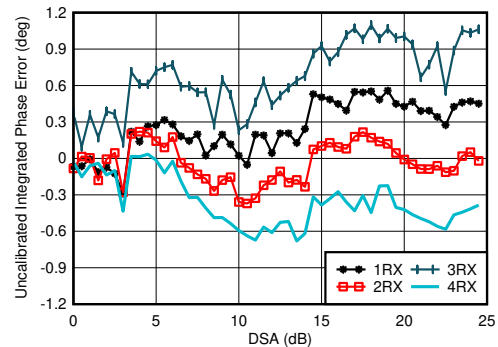
With 0.8GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 4-292. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8GHz**



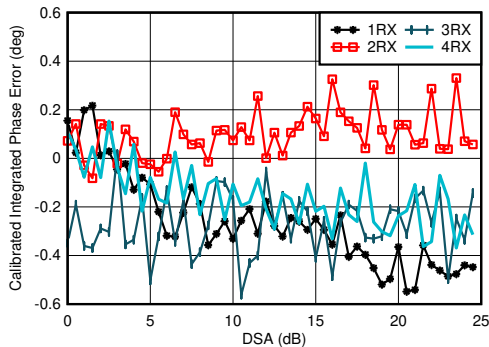
With 0.8GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 4-293. RX Calibrated Differential Phase Error vs DSA Setting at 0.8GHz**



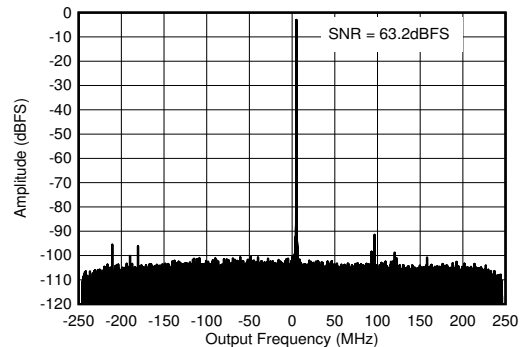
With 0.8GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-294. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8GHz**



With 0.8GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-295. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8GHz**

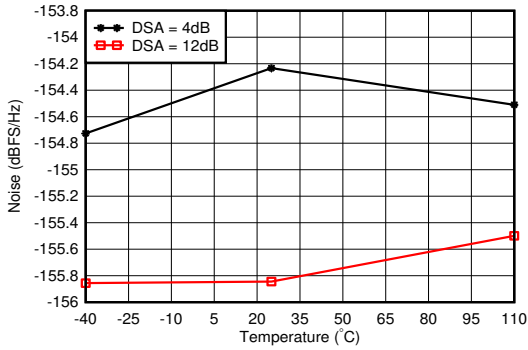


With 0.8GHz matching,  $f_{IN} = 840\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$

**Figure 4-296. RX Output FFT at 0.8GHz**

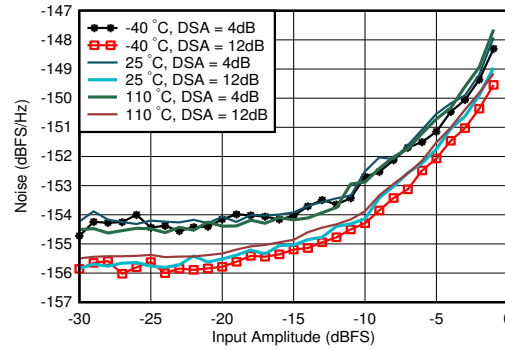
### 4.12.8 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



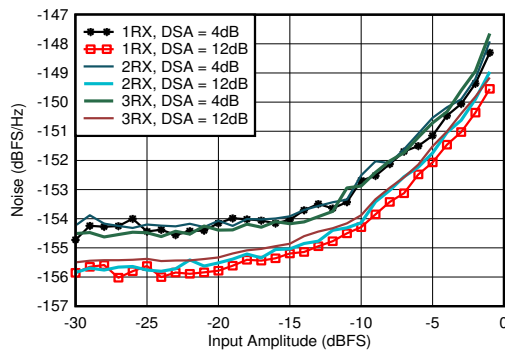
With 0.8GHz matching, 12.5MHz offset from tone

**Figure 4-297. RX Noise Spectral Density vs Temperature at 0.8GHz**



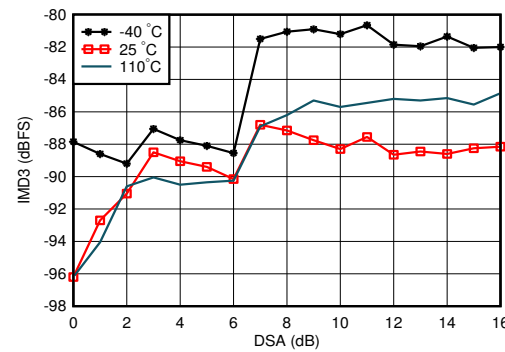
With 0.8GHz matching, DSA Setting = 12dB, 12.5MHz offset from tone

**Figure 4-298. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8GHz**



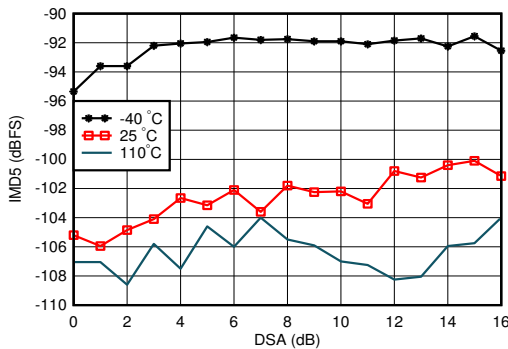
With 0.8GHz matching, 12.5MHz offset from tone

**Figure 4-299. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8GHz**



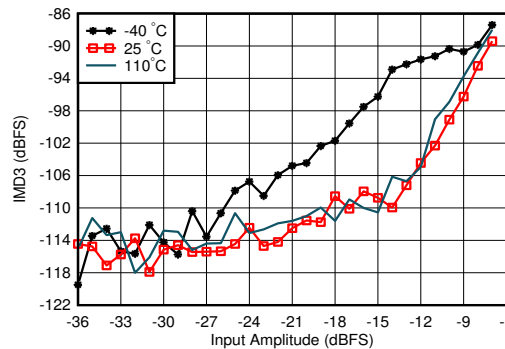
A. With 0.8GHz matching, each tone  $-7\text{dBFS}$ , tone spacing = 20MHz

**Figure 4-300. RX IMD3 vs DSA Setting and Temperature at 0.8GHz**



With 0.8GHz matching, each tone  $-7\text{dBFS}$ , tone spacing = 20MHz

**Figure 4-301. RX IMD5 vs DSA Setting and Temperature at 0.8GHz**

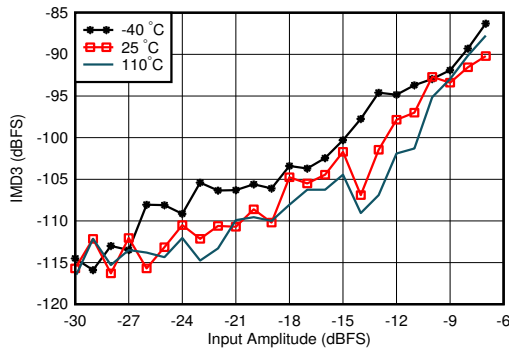


With 0.8GHz matching, tone spacing = 20MHz, DSA = 4dB

**Figure 4-302. RX IMD3 vs Input Level and Temperature at 0.8GHz**

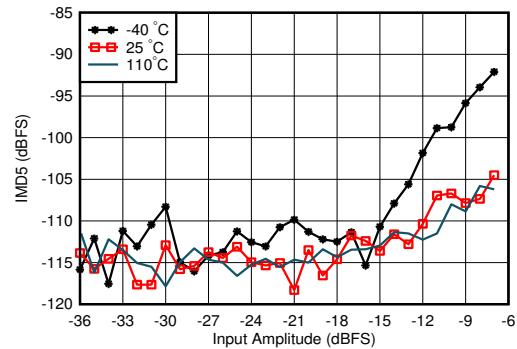
### 4.12.8 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



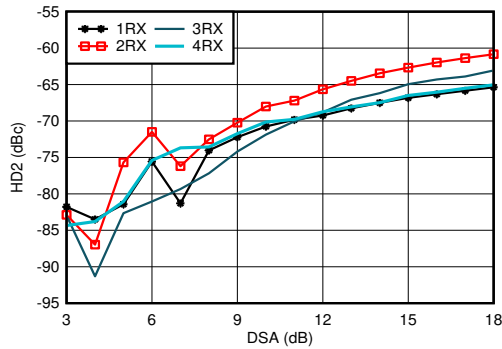
With 0.8GHz matching, tone spacing = 20MHz, DSA = 12dB

Figure 4-303. RX IMD3 vs Input Level and Temperature at 0.8GHz



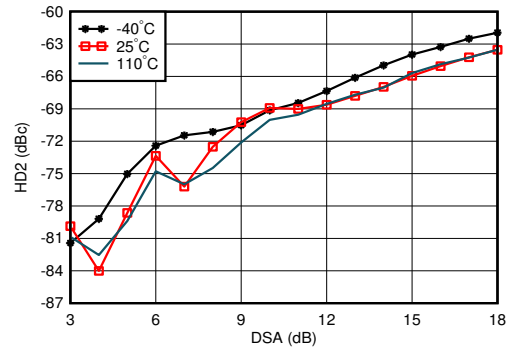
With 0.8GHz matching, tone spacing = 20MHz, DSA = 12dB

Figure 4-304. RX IMD5 vs Input Level and Temperature at 0.8GHz



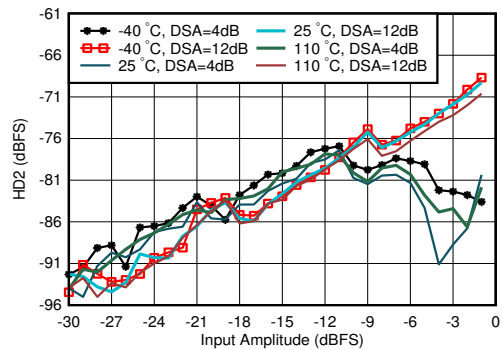
With 0.8GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-305. RX HD2 vs DSA Setting and Channel at 0.8GHz



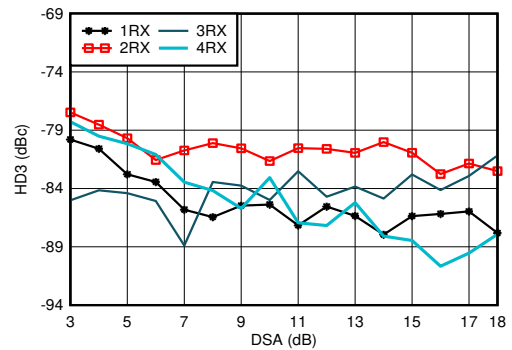
With 0.8GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-306. RX HD2 vs DSA Setting and Temperature at 0.8GHz



With 0.8GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-307. RX HD2 vs Input Level and Temperature at 0.8GHz

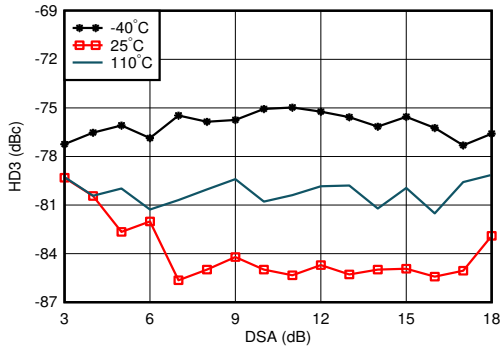


With 0.8GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-308. RX HD3 vs DSA Setting and Channel at 0.8GHz

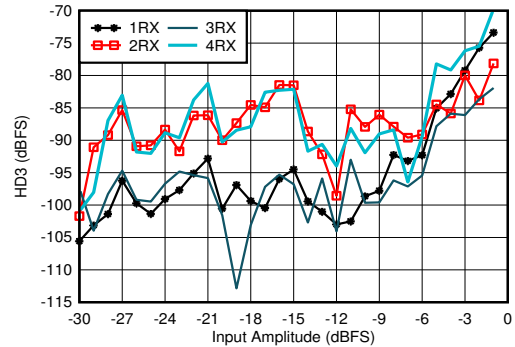
### 4.12.8 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



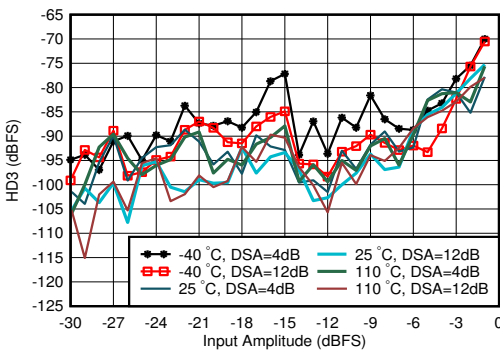
With 0.8GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-309. RX HD3 vs DSA Setting and Temperature at 0.8GHz



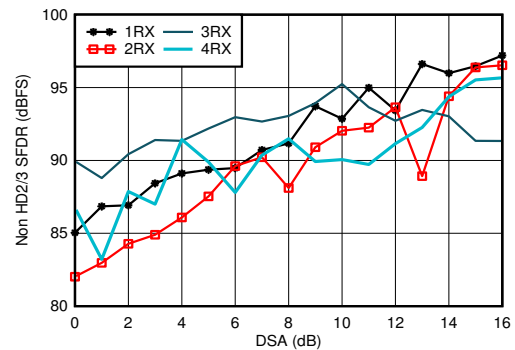
With 0.8GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-310. RX HD3 vs Input Level and Channel at 0.8GHz



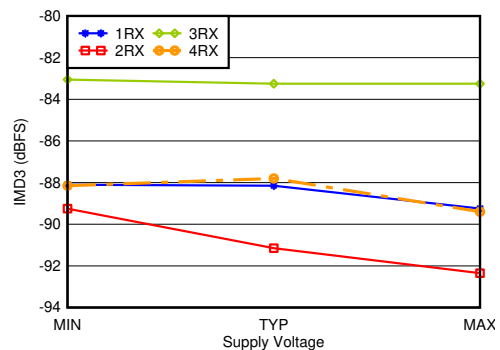
With 0.8GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-311. RX HD3 vs Input Level and Temperature at 0.8GHz



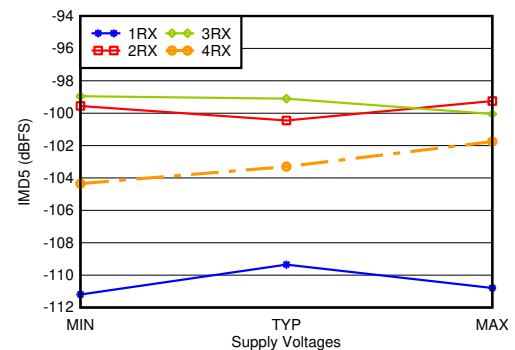
With 0.8GHz matching

Figure 4-312. RX Non-HD2/3 vs DSA Setting at 0.8GHz



With 0.8GHz matching,  $-7\text{dBFS}$  each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-313. RX IMD3 vs Supply and Channel at 0.8GHz



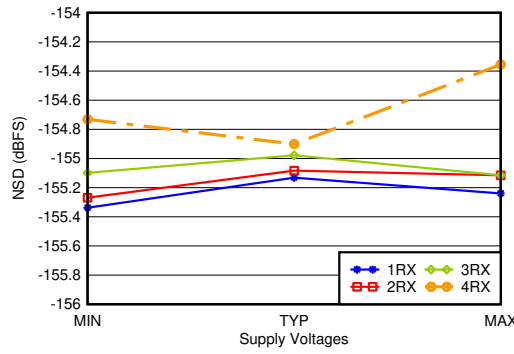
With 0.8GHz matching,  $-7\text{dBFS}$  each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-314. RX IMD5 vs Supply and Channel at 0.8GHz



**4.12.8 RX Typical Characteristics at 800MHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.

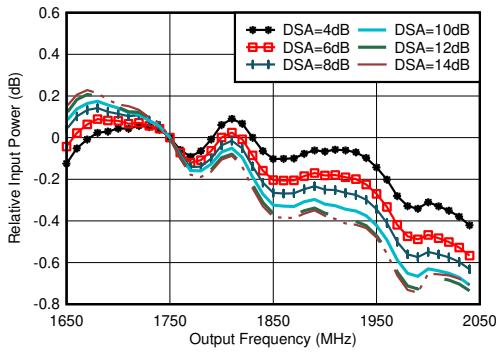


With 0.8GHz matching, 12.5MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 4-315. RX Noise Spectral Density vs Supply and Channel at 0.8GHz**

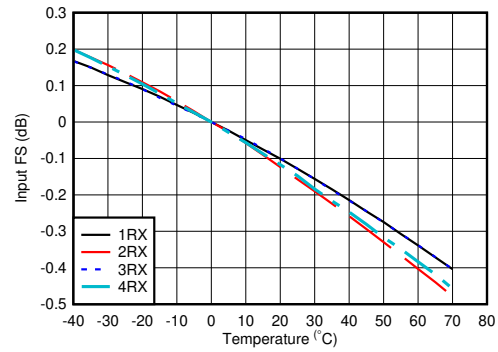
### 4.12.9 RX Typical Characteristics at 1.75-1.9GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



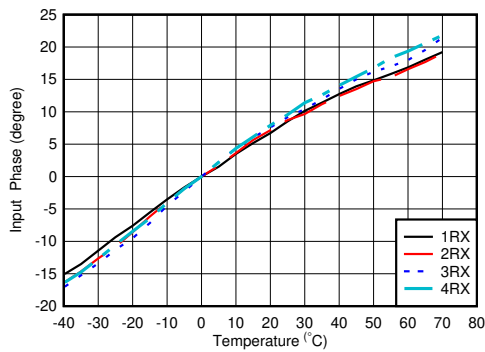
With 1.8GHz matching, normalized to 1.75GHz

**Figure 4-316. RX In-Band Gain Flatness,  $f_{IN} = 1750\text{MHz}$**



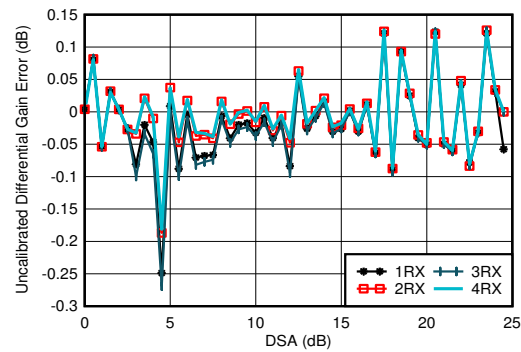
With 1.8GHz matching, normalized to fullscale at 25°C for each channel

**Figure 4-317. RX Input Fullscale vs Temperature and Channel at 1.75GHz**



With 2.6GHz matching, normalized to phase at 25°C

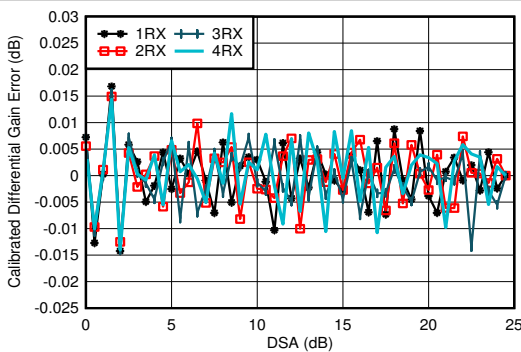
**Figure 4-318. RX Input Phase vs Temperature and DSA at  $f_{IN} = 1.75\text{GHz}$**



With 1.8GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

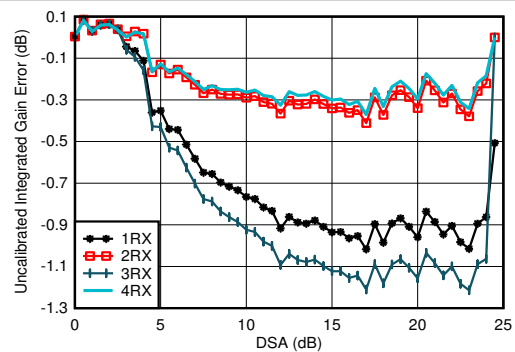
**Figure 4-319. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75GHz**



With 1.8GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

**Figure 4-320. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75GHz**



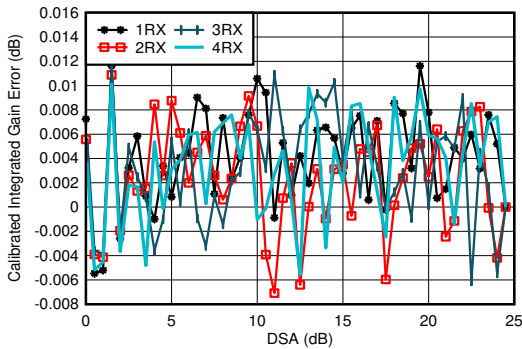
With 1.8GHz matching

Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-321. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75GHz**

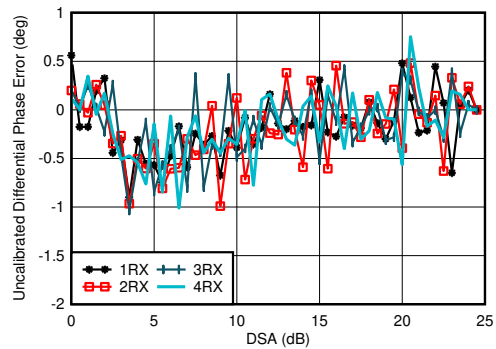
**4.12.9 RX Typical Characteristics at 1.75-1.9GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



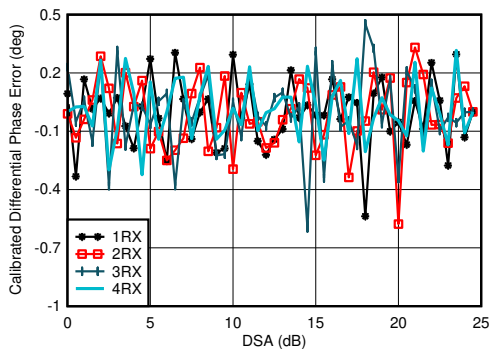
With 1.8GHz matching  
Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-322. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75GHz**



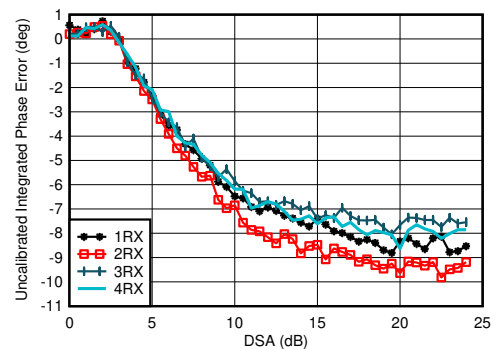
With 1.8GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 4-323. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75GHz**



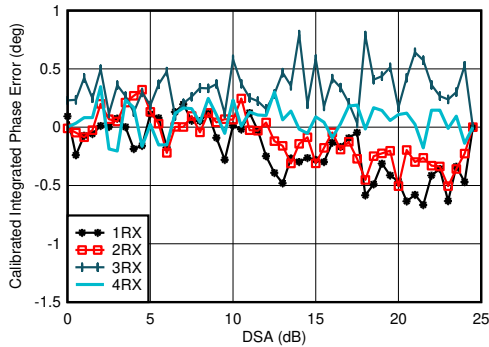
With 1.8GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 4-324. RX Calibrated Differential Phase Error vs DSA Setting at 1.75GHz**



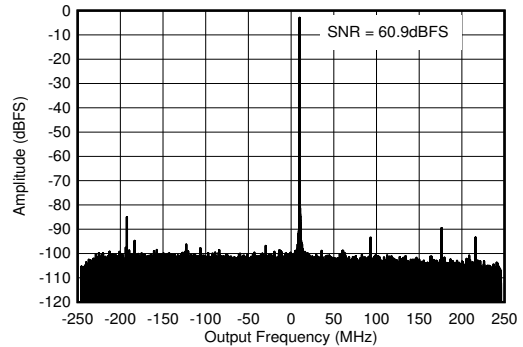
With 1.8GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-325. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75GHz**



With 1.8GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-326. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75GHz**

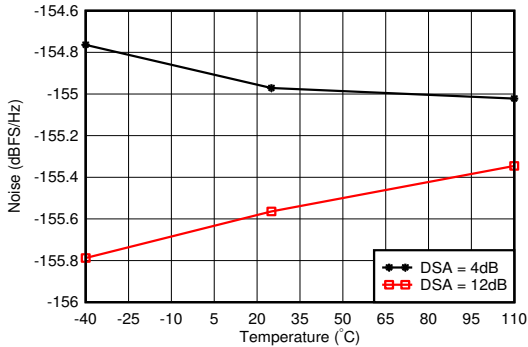


With 1.8GHz matching,  $f_{IN} = 2610\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$

**Figure 4-327. RX Output FFT at 1.75GHz**

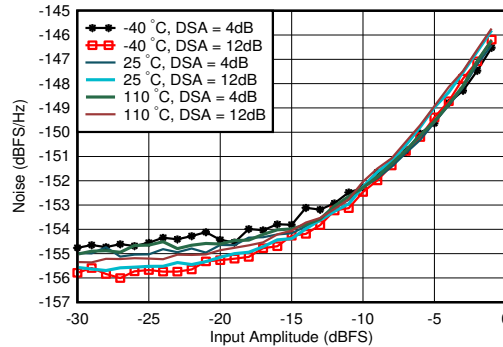
**4.12.9 RX Typical Characteristics at 1.75-1.9GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



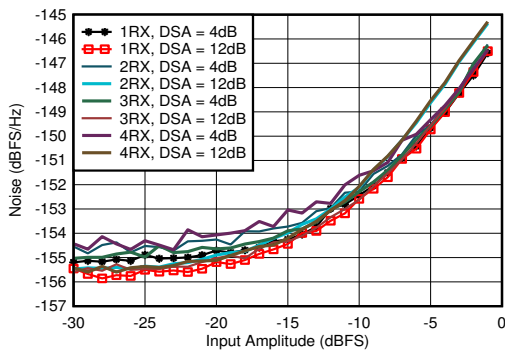
With 1.8GHz matching, 12.5MHz offset from tone

**Figure 4-328. RX Noise Spectral Density vs Temperature at 1.75GHz**



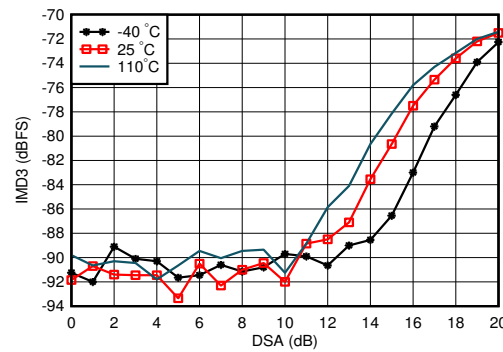
With 1.8GHz matching, DSA Setting = 12dB, 12.5MHz offset from tone

**Figure 4-329. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75GHz**



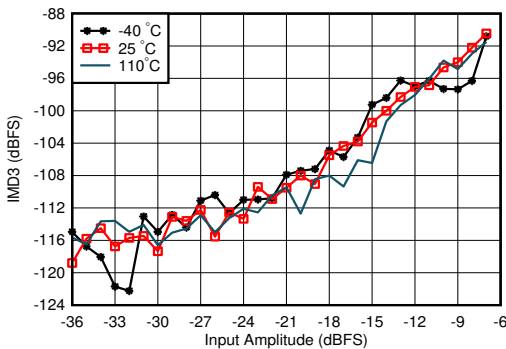
With 1.8GHz matching, 12.5MHz offset from tone

**Figure 4-330. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75GHz**



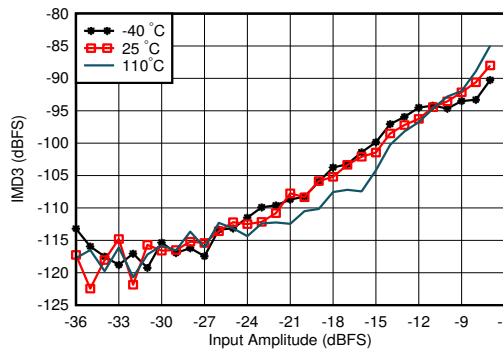
With 1.8GHz matching, each tone  $-7\text{dBFS}$ , tone spacing = 20MHz

**Figure 4-331. RX IMD3 vs DSA Setting and Temperature at 1.75GHz**



With 1.8GHz matching, tone spacing = 20MHz, DSA = 4dB

**Figure 4-332. RX IMD3 vs Input Level and Temperature at 1.75GHz**

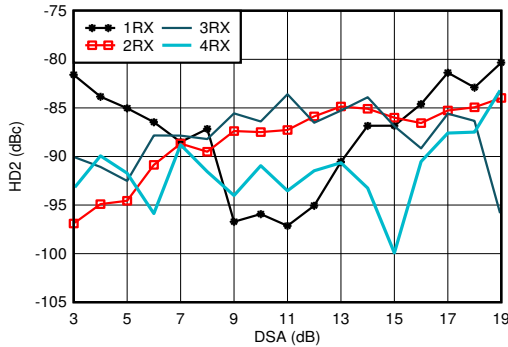


With 1.8GHz matching, tone spacing = 20MHz, DSA = 12dB

**Figure 4-333. RX IMD3 vs Input Level and Temperature at 1.75GHz**

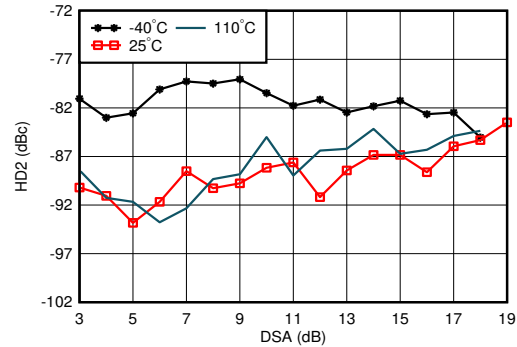
**4.12.9 RX Typical Characteristics at 1.75-1.9GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



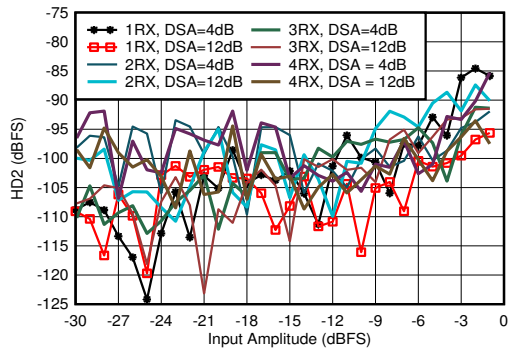
With 1.8GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 4-334. RX HD2 vs DSA Setting and Channel at 1.9 GHz**



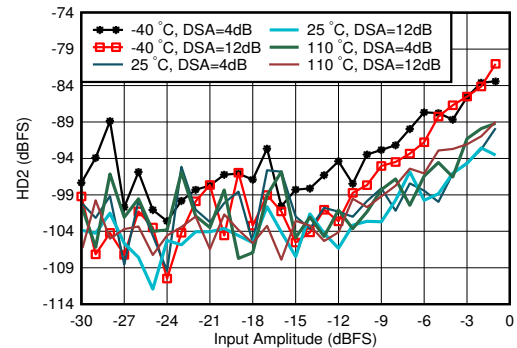
With 1.8GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 4-335. RX HD2 vs DSA Setting and Temperature at 1.9 GHz**



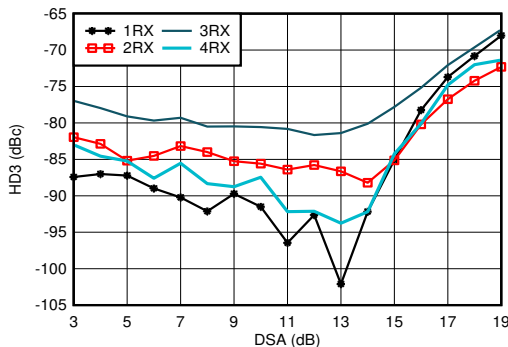
With 1.8GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 4-336. RX HD2 vs Input Amplitude and Channel at 1.9GHz**



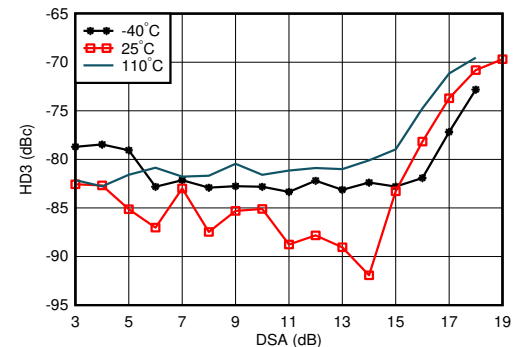
With 1.8GHz matching,  $f_{in} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 4-337. RX HD2 vs Input Amplitude and Temperature at 1.9GHz**



With 1.8GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

**Figure 4-338. RX HD3 vs DSA Setting and Channel at 1.9GHz**

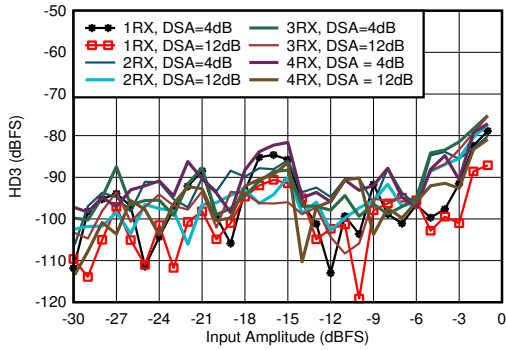


With 1.8GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

**Figure 4-339. RX HD3 vs DSA Setting and Temperature at 1.9GHz**

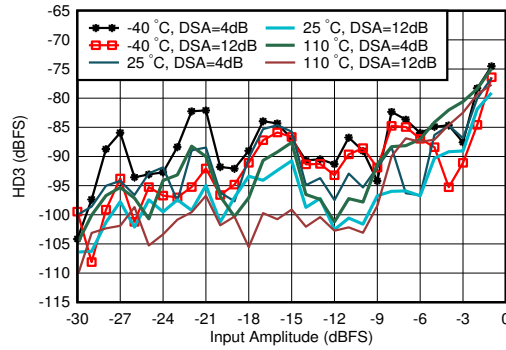
### 4.12.9 RX Typical Characteristics at 1.75-1.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



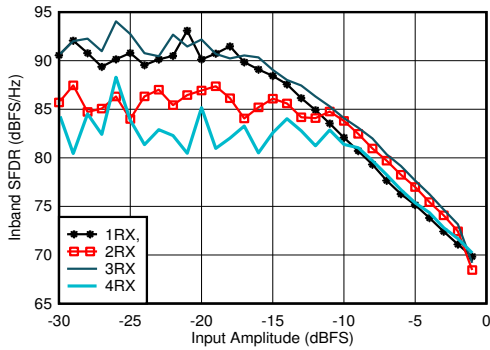
With 1.8GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

**Figure 4-340. RX HD3 vs Input Level and Channel at 1.9GHz**



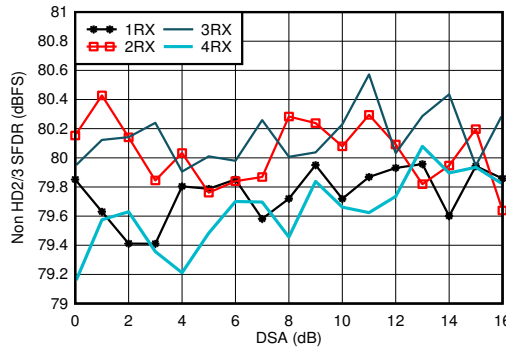
With 1.8GHz matching,  $f_{in} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

**Figure 4-341. RX HD3 vs Input Level and Temperature at 1.9GHz**



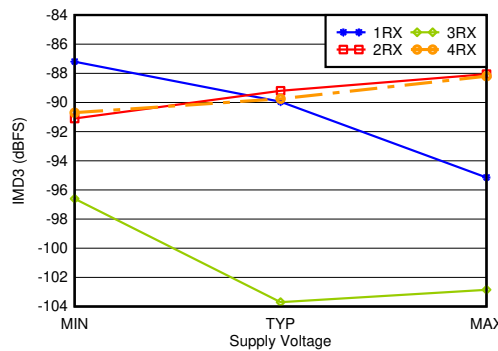
With 1.8GHz matching, decimated by 3

**Figure 4-342. RX In-Band SFDR ( $\pm 400\text{MHz}$ ) vs Input Amplitude at 1.75GHz**



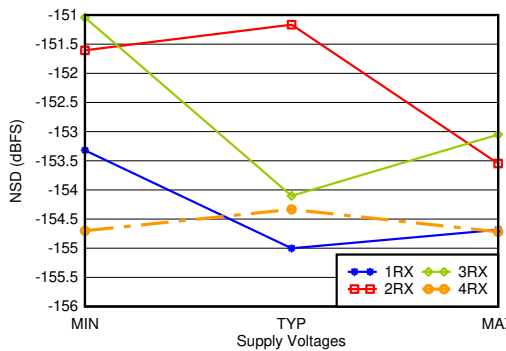
With 1.8GHz matching

**Figure 4-343. RX Non-HD2/3 vs DSA Setting at 1.75GHz**



With 1.8GHz matching,  $-7\text{dBFS}$  each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 4-344. RX IMD3 vs Supply and Channel at 1.75GHz**

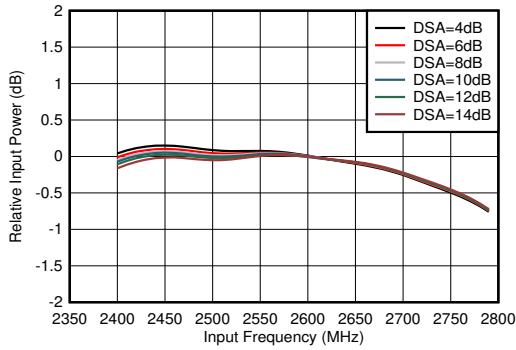


With 1.8GHz matching, 12.5MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 4-345. RX Noise Spectral Density vs Supply and Channel at 1.75GHz**

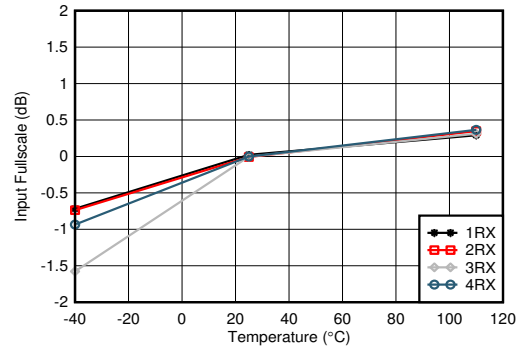
### 4.12.10 RX Typical Characteristics at 2.6GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



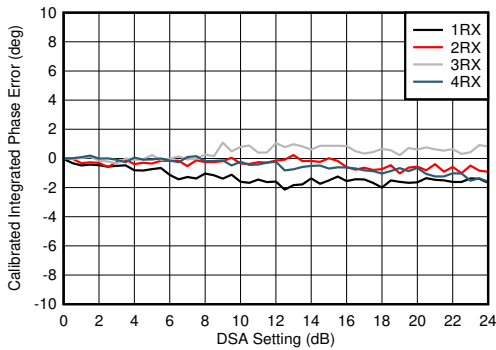
With matching, normalized to power at 2.6GHz for each DSA setting

**Figure 4-346. RX Inband Gain Flatness,  $f_{IN} = 2600\text{MHz}$**



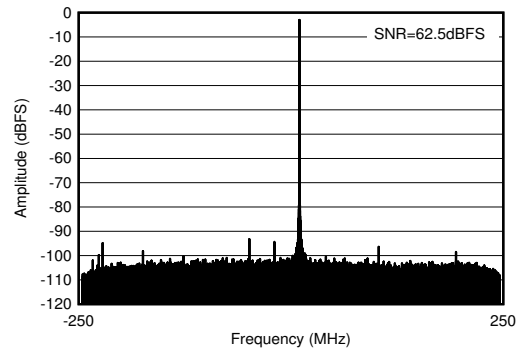
With 2.6GHz matching, normalized to fullscale at 25°C for each channel

**Figure 4-347. RX Input Fullscale vs Temperature and Channel at 2.6GHz**



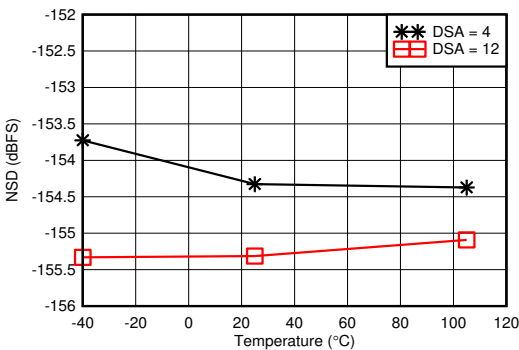
With 2.6GHz matching  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 4-348. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6GHz**



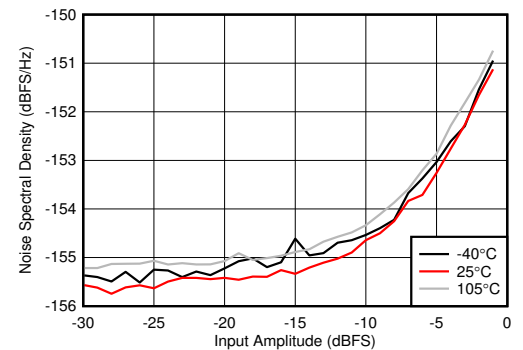
With 2.6GHz matching,  $f_{IN} = 2610\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$

**Figure 4-349. RX Output FFT at 2.6GHz**



With 2.6GHz matching, 12.5MHz offset from tone

**Figure 4-350. RX Noise Spectral Density vs Temperature at 2.6GHz**

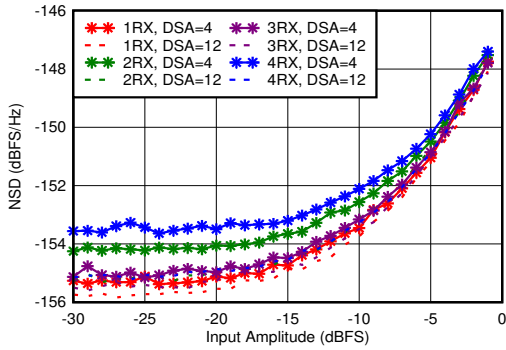


With 2.6GHz matching, DSA Setting = 12dB, 12.5MHz offset from tone

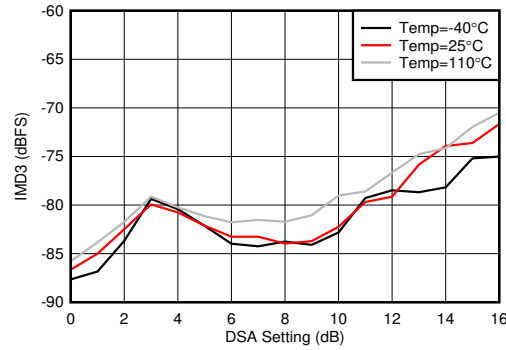
**Figure 4-351. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6GHz**

**4.12.10 RX Typical Characteristics at 2.6GHz (continued)**

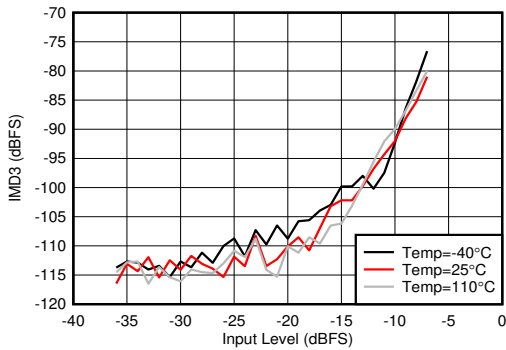
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



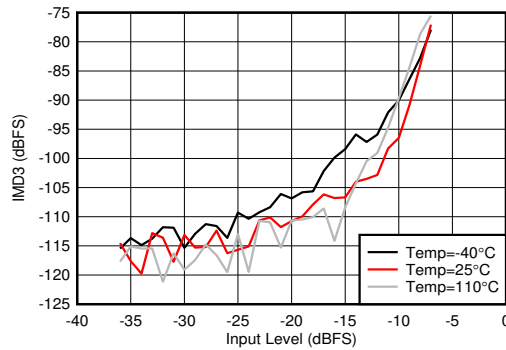
With 2.6GHz matching, 12.5MHz offset from tone  
**Figure 4-352. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6GHz**



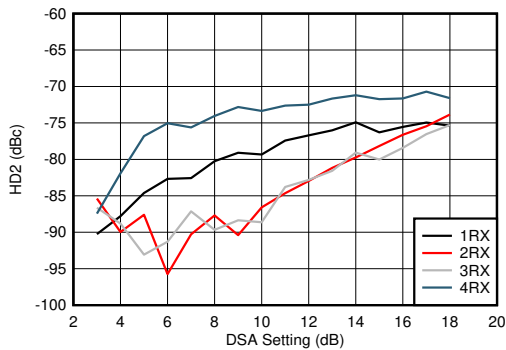
With 2.6GHz matching, each tone  $-7\text{dBFS}$ , tone spacing = 20MHz  
**Figure 4-353. RX IMD3 vs DSA Setting and Temperature at 2.6GHz**



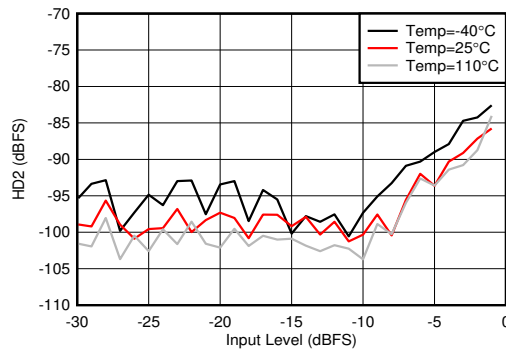
With 2.6GHz matching, tone spacing = 20MHz, DSA = 4dB  
**Figure 4-354. RX IMD3 vs Input Level and Temperature at 2.6GHz**



With 2.6GHz matching, tone spacing = 20MHz, DSA = 12dB  
**Figure 4-355. RX IMD3 vs Input Level and Temperature at 2.6GHz**



With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)  
**Figure 4-356. RX HD2 vs DSA Setting and Channel at 2.6GHz**

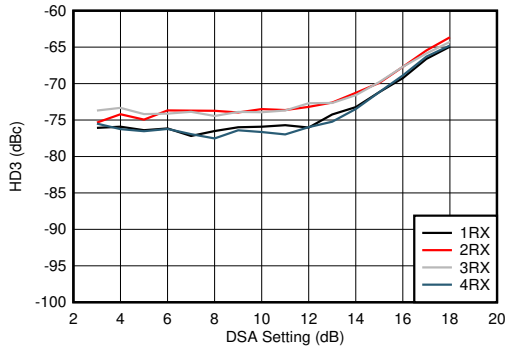


With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)  
**Figure 4-357. RX HD2 vs Input Level and Temperature at 2.6GHz**



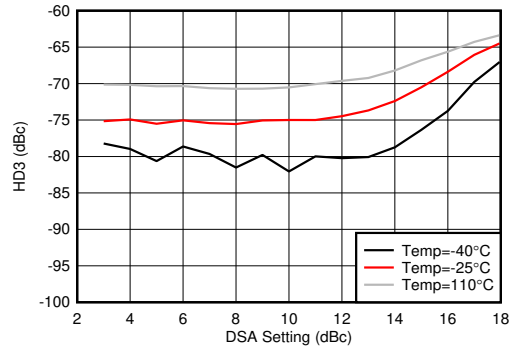
**4.12.10 RX Typical Characteristics at 2.6GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



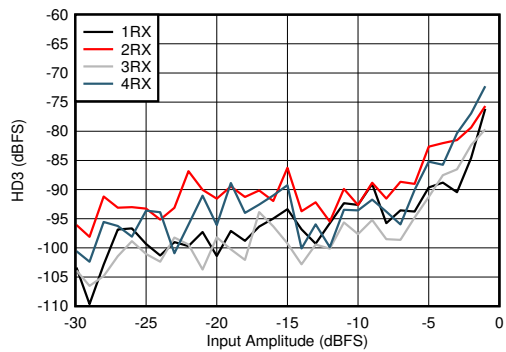
With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-358. RX HD3 vs DSA Setting and Channel at 2.6GHz**



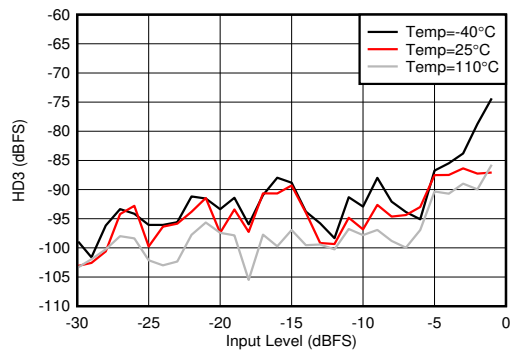
With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-359. RX HD3 vs DSA Setting and Temperature at 2.6GHz**



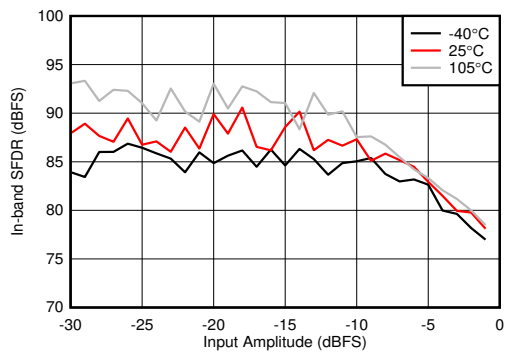
With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-360. RX HD3 vs Input Level and Channel at 2.6GHz**



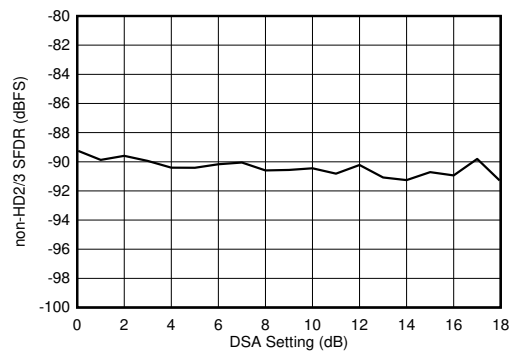
With 2.6GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 4-361. RX HD3 vs Input Level and Temperature at 2.6GHz**



With 2.6GHz matching, decimate by 4

**Figure 4-362. RX In-Band SFDR ( $\pm 300$  MHz) vs Input Amplitude and Temperature at 2.6GHz**

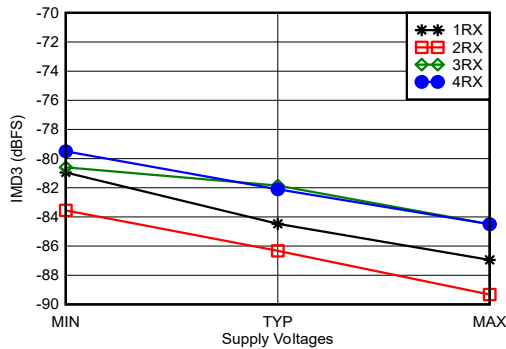


With 2.6GHz matching

**Figure 4-363. RX Non-HD2/3 vs DSA Setting at 2.6GHz**

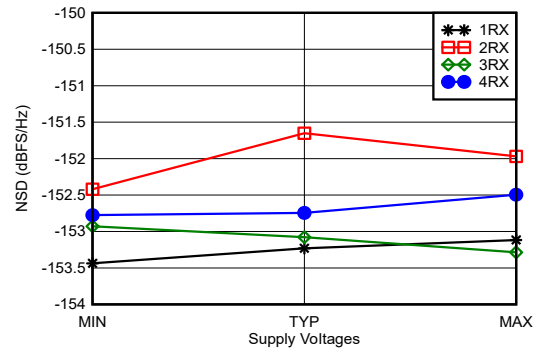
#### 4.12.10 RX Typical Characteristics at 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



With 2.6GHz matching, -7dBFS each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-364. RX IMD3 vs Supply and Channel at 2.6GHz

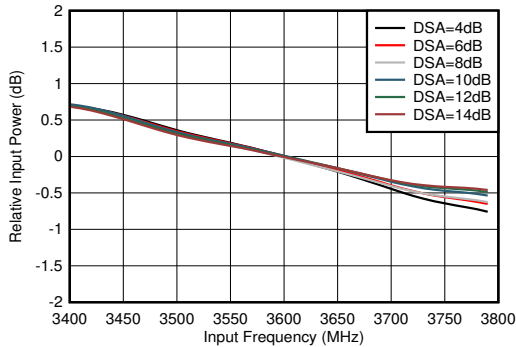


With 2.6GHz matching, 12.5MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-365. RX Noise Spectral Density vs Supply and Channel at 2.6GHz

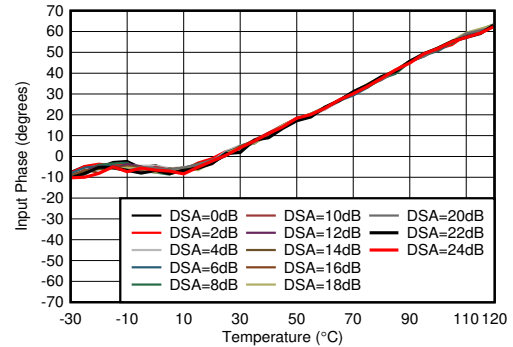
### 4.12.11 RX Typical Characteristics at 3.5GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



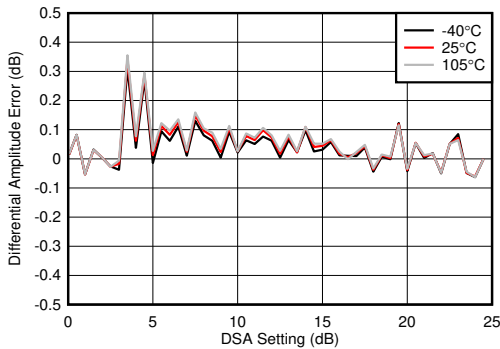
With 3.6GHz matching, normalized to 3.6GHz

**Figure 4-366. RX In-Band Gain Flatness,  $f_{IN} = 3600\text{MHz}$**



With 3.6GHz matching, normalized to phase at 25°C

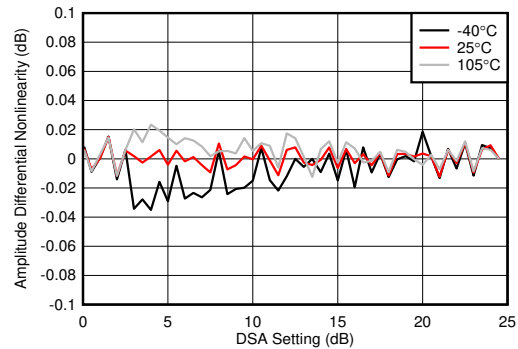
**Figure 4-367. RX Input Phase vs Temperature at 3.6GHz**



With 3.6GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

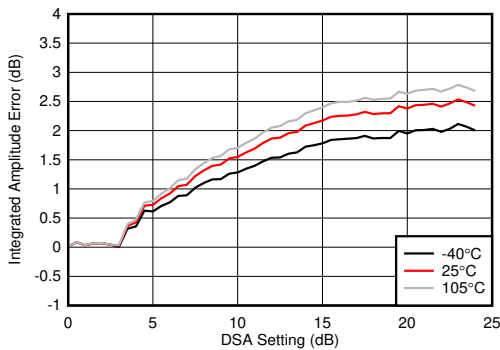
**Figure 4-368. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6GHz**



With 3.6GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

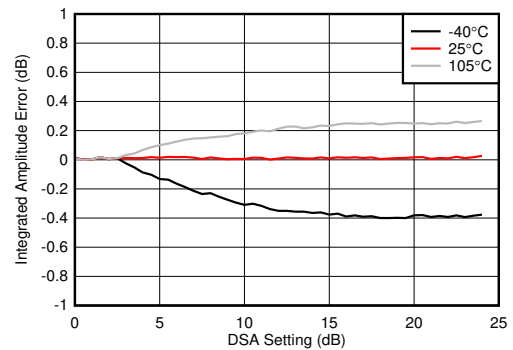
**Figure 4-369. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6GHz**



With 3.6GHz matching

Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-370. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6GHz**



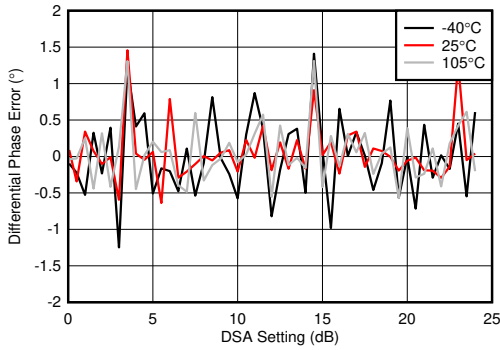
With 3.6GHz matching

Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-371. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6GHz**

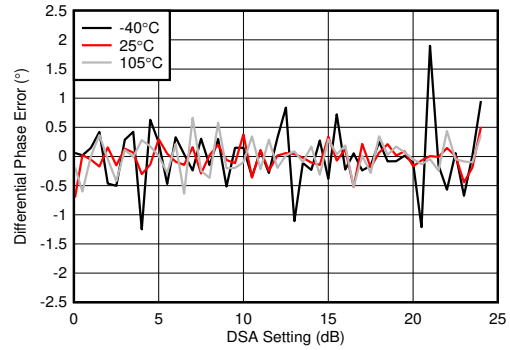
**4.12.11 RX Typical Characteristics at 3.5GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



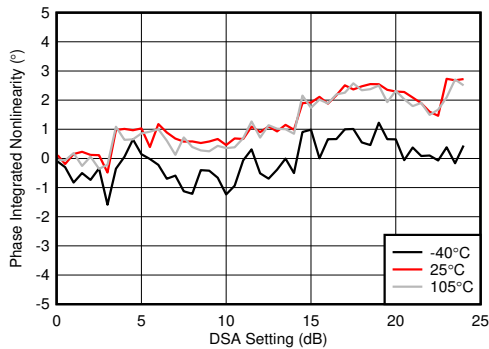
With 3.6GHz matching  
 Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 4-372. RX Uncalibrated Phase Error vs DSA Setting at 3.6GHz**



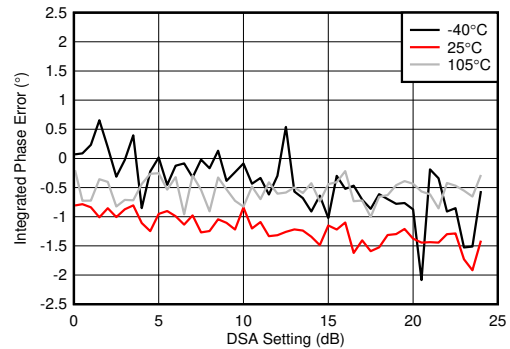
With 3.6GHz matching  
 Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 4-373. RX Calibrated Differential Phase Error vs DSA Setting at 3.6GHz**



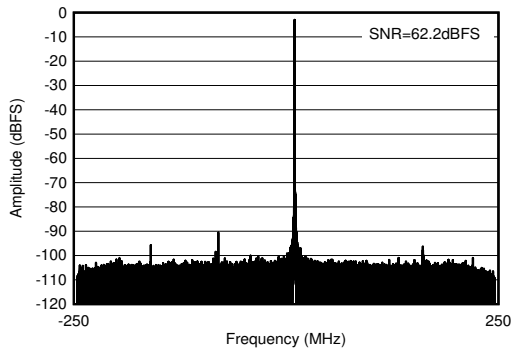
With 3.6GHz matching  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-374. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6GHz**



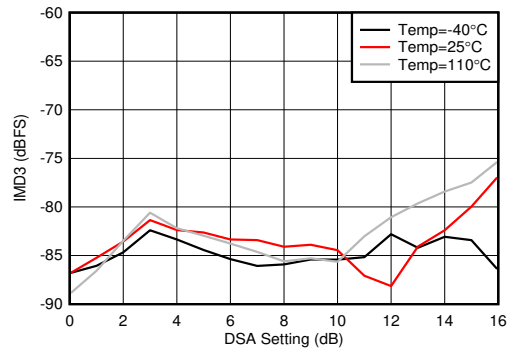
With 3.6GHz matching  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-375. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6GHz**



With 3.6GHz matching,  $f_{IN} = 3610\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$

**Figure 4-376. RX Output FFT at 3.6GHz**

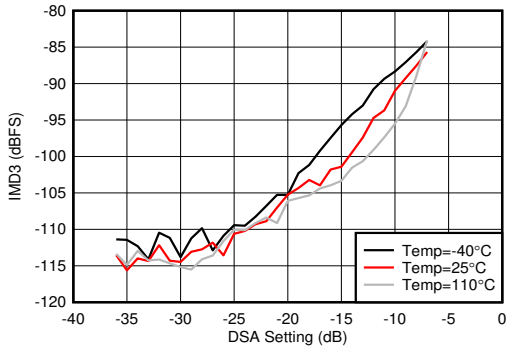


With 3.5 GHz matching, each tone at  $-7\text{dBFS}$ , 20MHz tone spacing

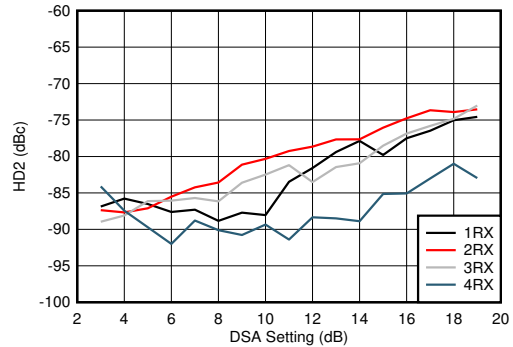
**Figure 4-377. RX IMD3 vs DSA Setting and Temperature at 3.6GHz**

**4.12.11 RX Typical Characteristics at 3.5GHz (continued)**

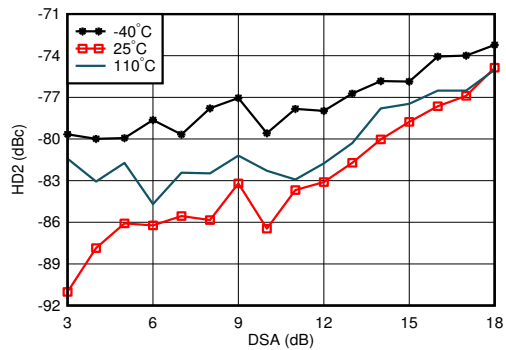
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



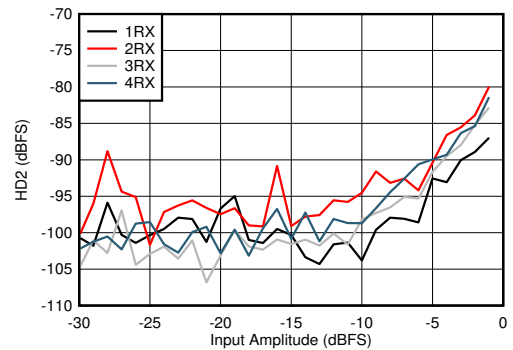
With 3.5GHz matching, 20MHz tone spacing  
**Figure 4-378. RX IMD3 vs Input Level and Temperature at 3.6GHz**



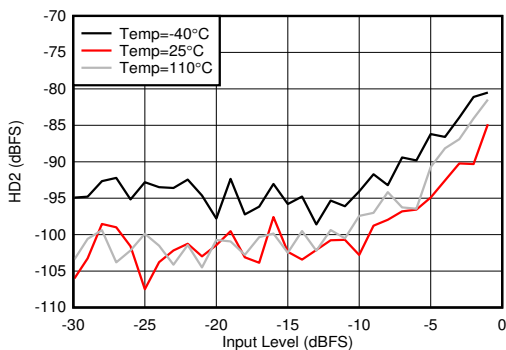
With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)  
**Figure 4-379. RX HD2 vs DSA Setting and Channel at 3.6GHz**



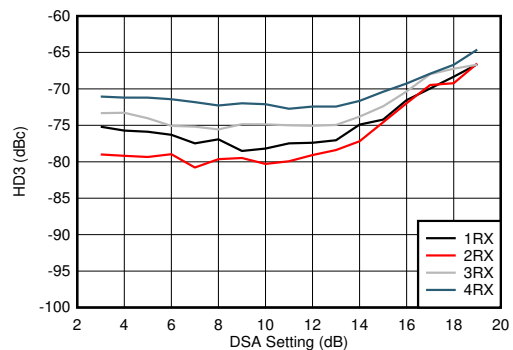
With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)  
**Figure 4-380. RX HD2 vs DSA Setting and Temperature at 3.6GHz**



With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)  
**Figure 4-381. RX HD2 vs Input Level and Channel at 3.6GHz**



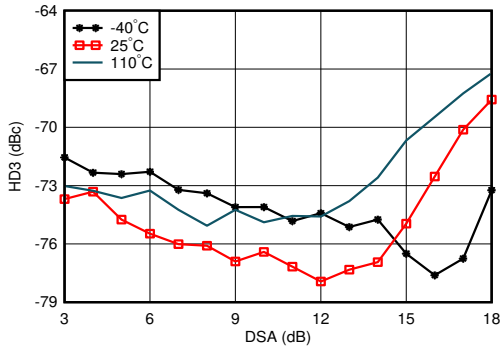
With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)  
**Figure 4-382. RX HD2 vs Input Level and Temperature at 3.6GHz**



With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)  
**Figure 4-383. RX HD3 vs DSA Setting and Channel at 3.6GHz**

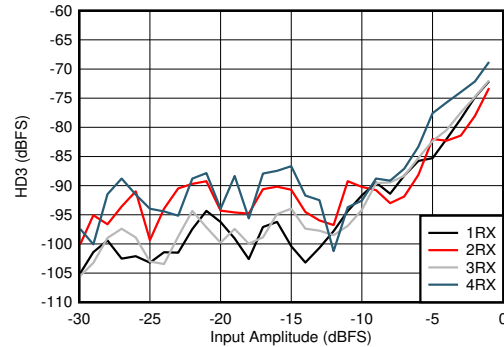
4.12.11 RX Typical Characteristics at 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



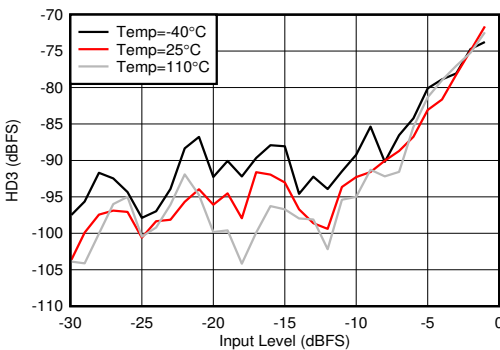
With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-384. RX HD3 vs DSA Setting and Temperature at 3.6GHz



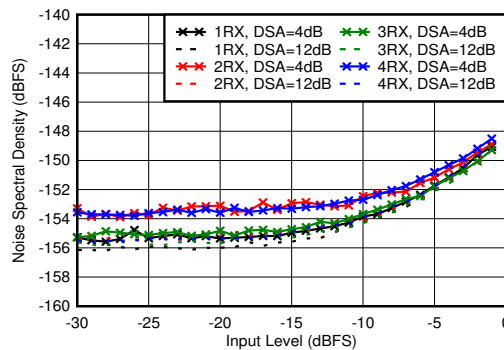
With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-385. RX HD3 vs Input Level and Channel at 3.6GHz



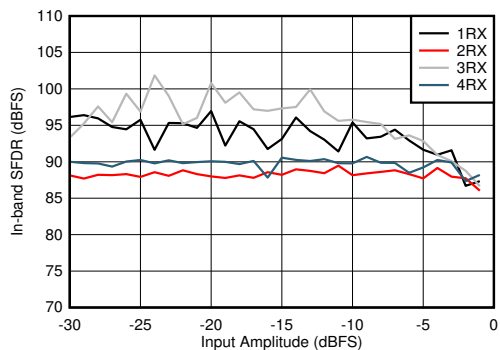
With 3.5GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-386. RX HD3 vs Input Level and Temperature at 3.6GHz



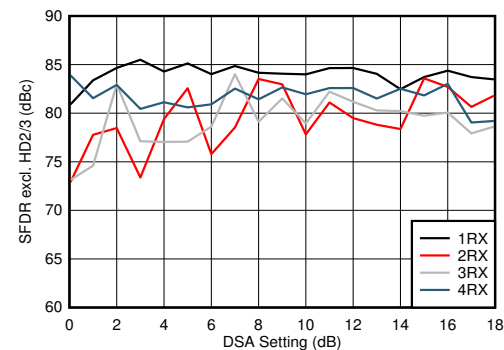
With 3.5GHz matching, 12.5-MHz offset from tone

Figure 4-387. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6GHz



With 3.5GHz matching

Figure 4-388. RX In-Band SFDR ( $\pm 200\text{MHz}$ ) vs Input Level and Channel at 3.6GHz

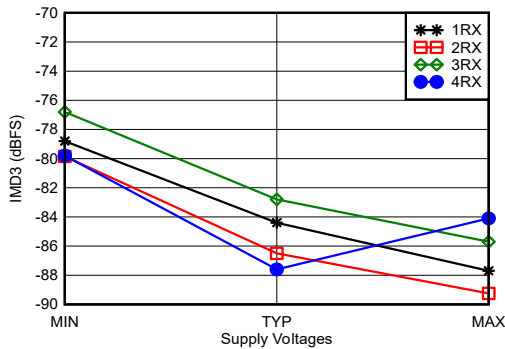


With 3.5GHz matching

Figure 4-389. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6GHz

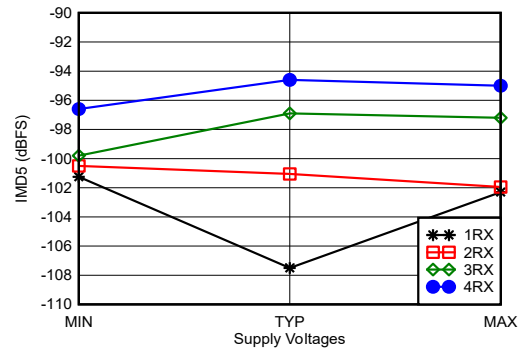
#### 4.12.11 RX Typical Characteristics at 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



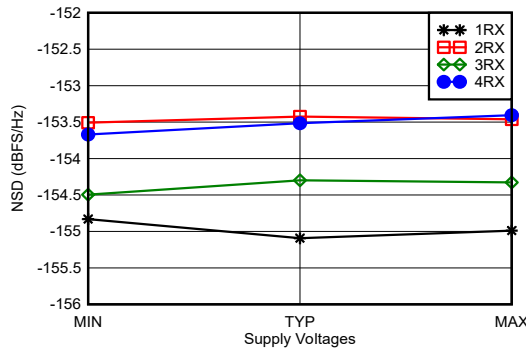
With 3.6GHz matching,  $-7\text{dBFS}$  each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-390. RX IMD3 vs Supply Voltage and Channel at 3.6GHz



With 3.6GHz matching,  $-7\text{dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-391. RX IMD5 vs Supply Voltage and Channel at 3.6GHz

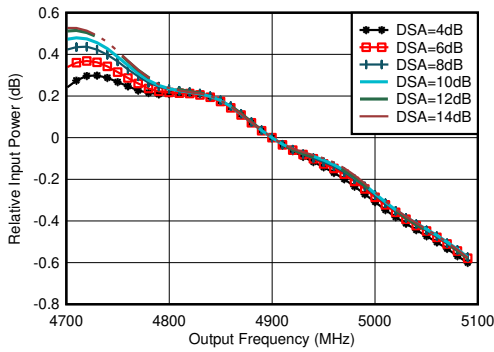


With 3.6GHz matching, tone at 20 dBFS, 12.5MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-392. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6GHz

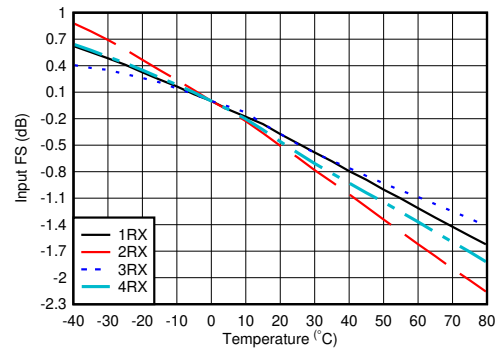
### 4.12.12 RX Typical Characteristics at 4.9GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



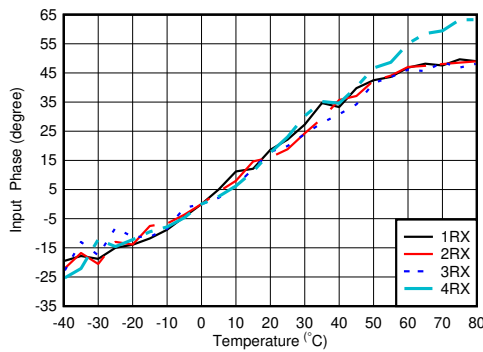
With matching, normalized to power at 4.9GHz for each DSA setting

Figure 4-393. RX Inband Gain Flatness,  $f_{IN} = 4900\text{MHz}$



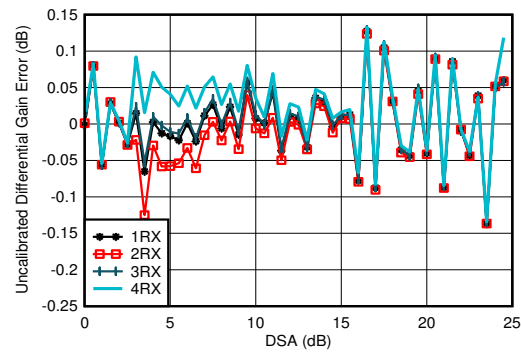
With 4.9GHz matching, normalized to fullscale at 25°C for each channel

Figure 4-394. RX Input Fullscale vs Temperature and Channel at 4.9GHz



With 4.9GHz matching, normalized to phase at 25°C

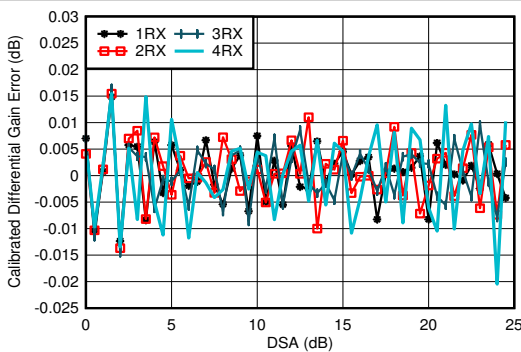
Figure 4-395. RX Input Phase vs Temperature and DSA at  $f_{OUT} = 4.9\text{GHz}$



With 4.9GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

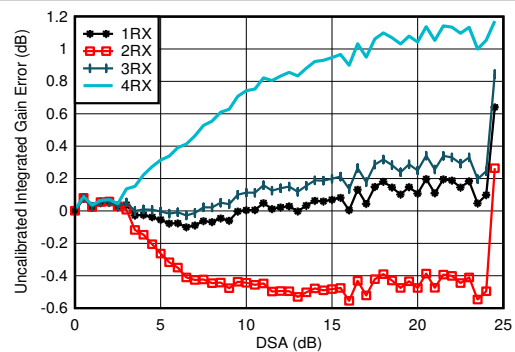
Figure 4-396. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9GHz



With 4.9GHz matching

$$\text{Differential Amplitude Error} = P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$$

Figure 4-397. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9GHz



With 4.9GHz matching

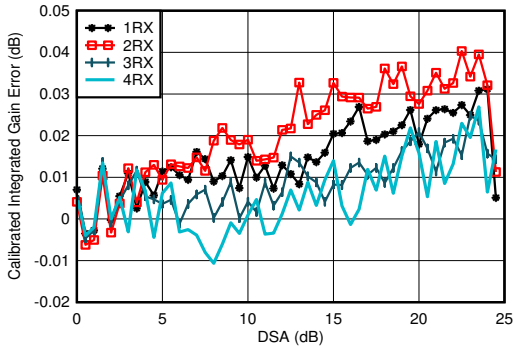
$$\text{Integrated Amplitude Error} = P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

Figure 4-398. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9GHz



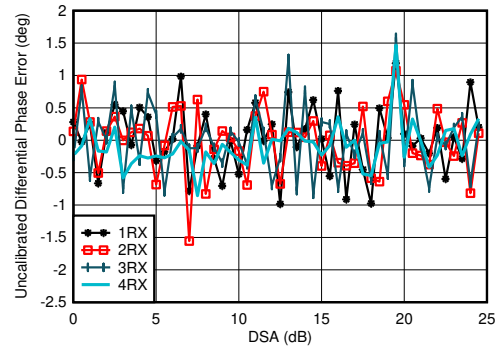
**4.12.12 RX Typical Characteristics at 4.9GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



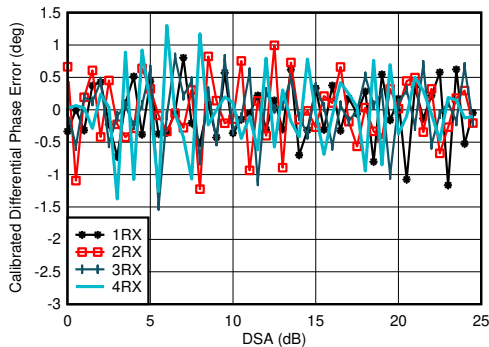
With 4.9GHz matching  
Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 4-399. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9GHz**



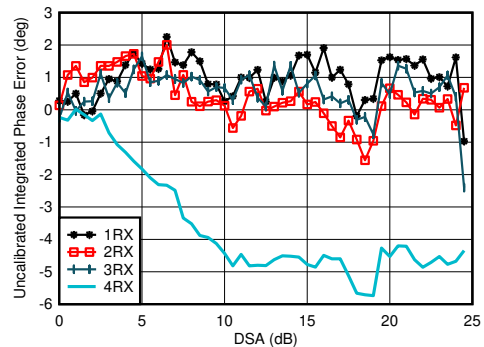
With 4.9GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 4-400. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9GHz**



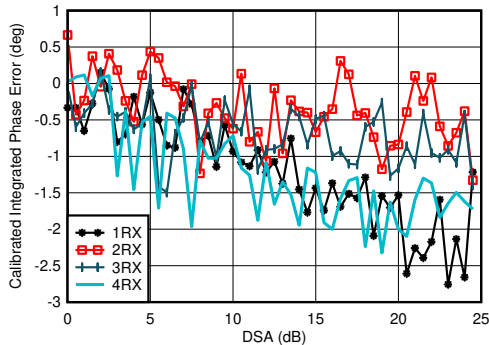
With 4.9GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 4-401. RX Calibrated Differential Phase Error vs DSA Setting at 4.9GHz**



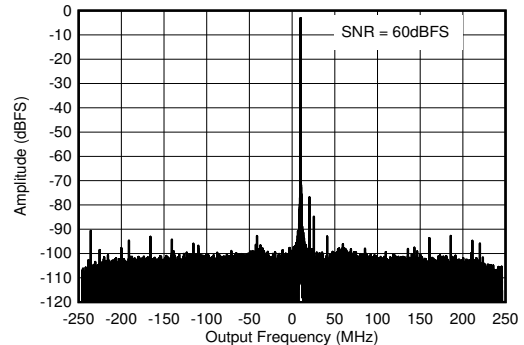
With 4.9GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-402. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9GHz**



With 4.9GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 4-403. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9GHz**

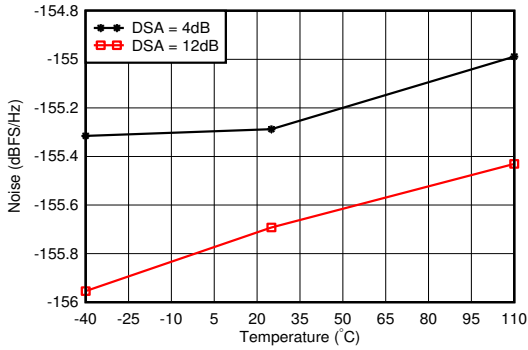


With 4.9GHz matching,  $f_{IN} = 4910\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$

**Figure 4-404. RX Output FFT at 4.9GHz**

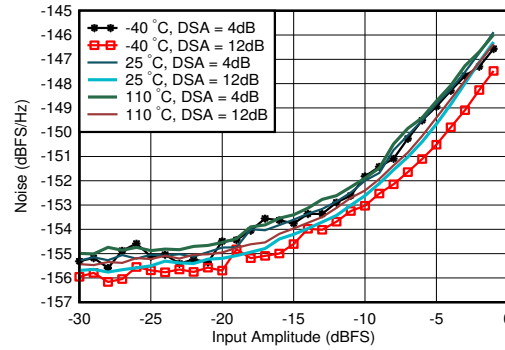
### 4.12.12 RX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



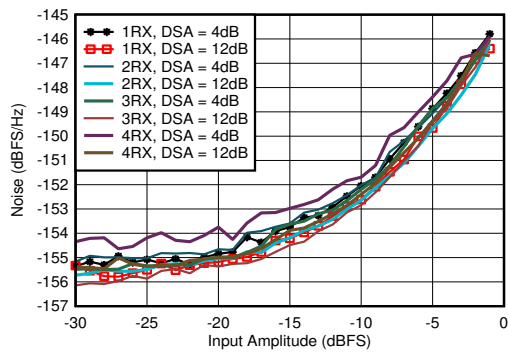
With 4.9GHz matching, 12.5-MHz offset from tone

**Figure 4-405. RX Noise Spectral Density vs Temperature at 4.9GHz**



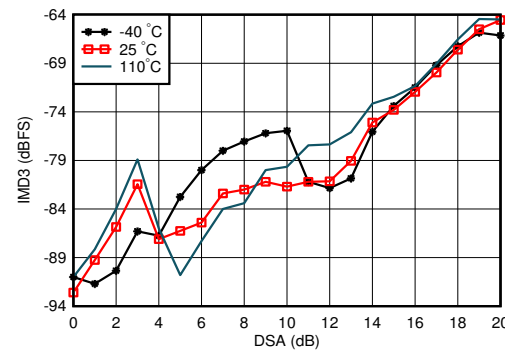
With 4.9GHz matching, DSA Setting = 12dB, 12.5MHz offset from tone

**Figure 4-406. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9GHz**



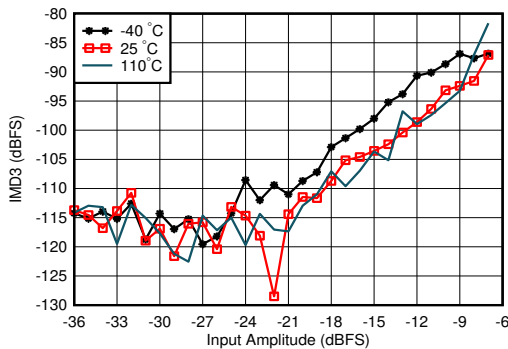
With 4.9GHz matching, 12.5MHz offset from tone

**Figure 4-407. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9GHz**



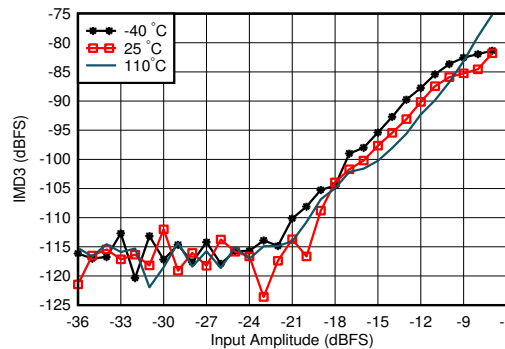
With 4.9GHz matching, each tone  $-7\text{dBFS}$ , tone spacing = 20MHz

**Figure 4-408. RX IMD3 vs DSA Setting and Temperature at 4.9GHz**



With 4.9GHz matching, tone spacing = 20MHz, DSA = 4dB

**Figure 4-409. RX IMD3 vs Input Level and Temperature at 4.9GHz**

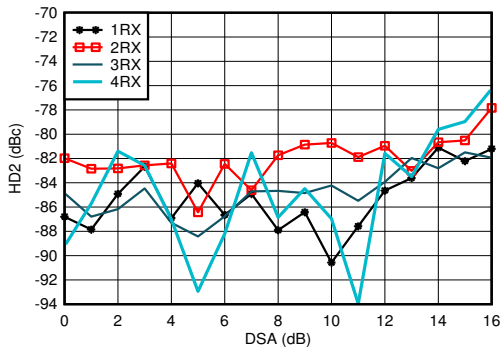


With 4.9GHz matching, tone spacing = 20MHz, DSA = 12dB

**Figure 4-410. RX IMD3 vs Input Level and Temperature at 4.9GHz**

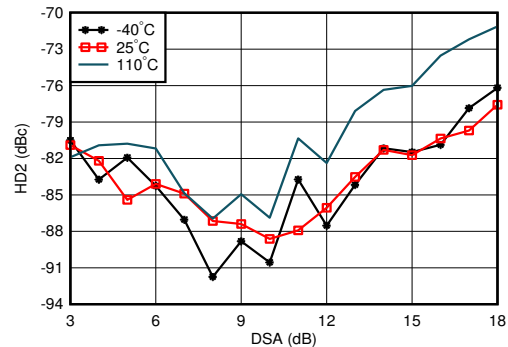
### 4.12.12 RX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



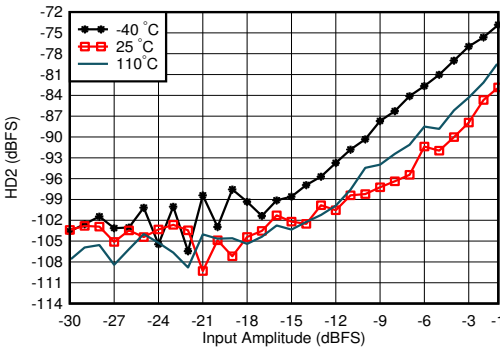
With 4.9GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-411. RX HD2 vs DSA Setting and Channel at 4.9GHz



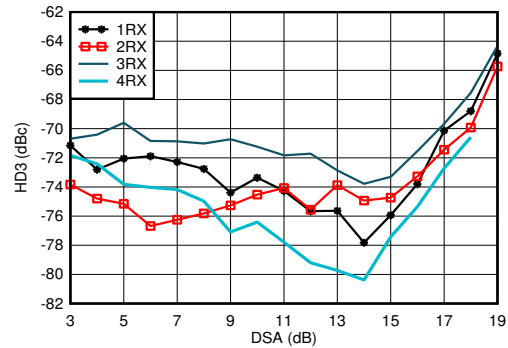
With 4.9GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-412. RX HD2 vs DSA and Temperature at 4.9GHz



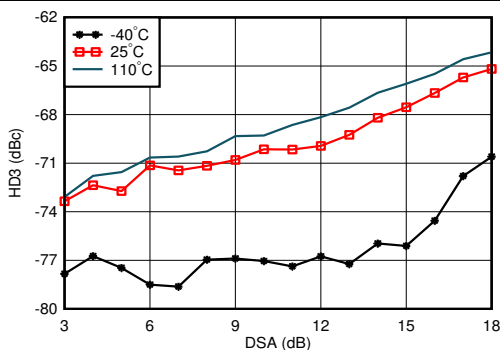
With 4.9GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 4-413. RX HD2 vs Input Level and Temperature at 4.9GHz



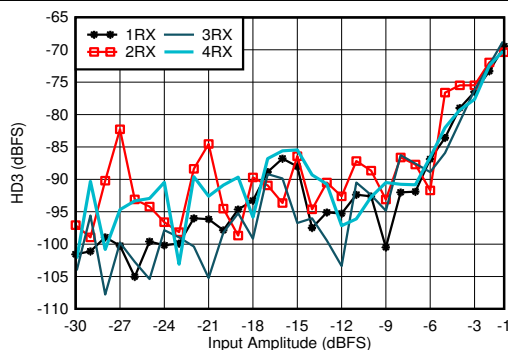
With 4.9GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-414. RX HD3 vs DSA Setting and Channel at 4.9GHz



With 4.9GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-415. RX HD3 vs DSA Setting and Temperature at 4.9GHz

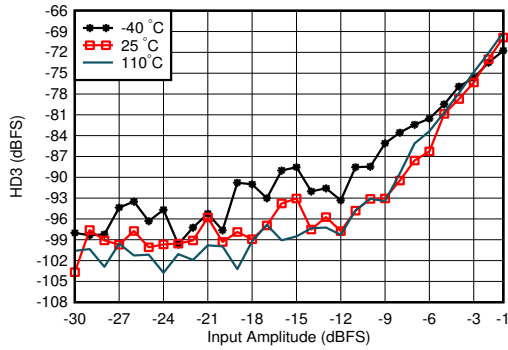


With 4.9GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-416. RX HD3 vs Input Level and Channel at 4.9GHz

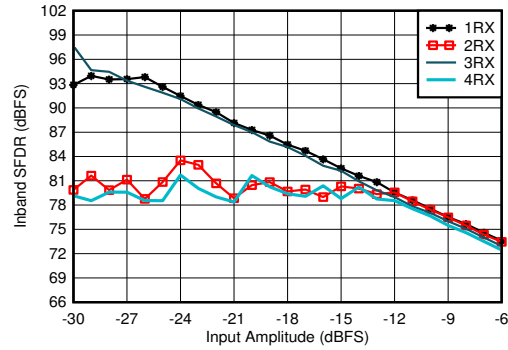
### 4.12.12 RX Typical Characteristics at 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{MHz}$ ,  $A_{IN} = -3\text{dBFS}$ , DSA setting = 4dB.



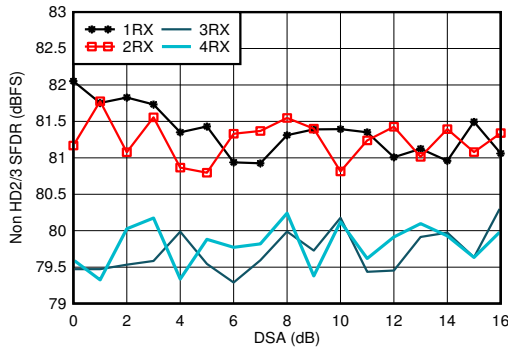
With 4.9GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 4-417. RX HD3 vs Input Level and Temperature at 4.9GHz



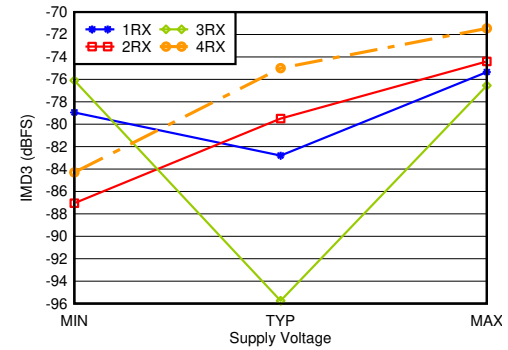
With 4.9GHz matching, decimate by 3

Figure 4-418. RX In-Band SFDR ( $\pm 400$  MHz) vs Input Amplitude and Channel at 4.9GHz



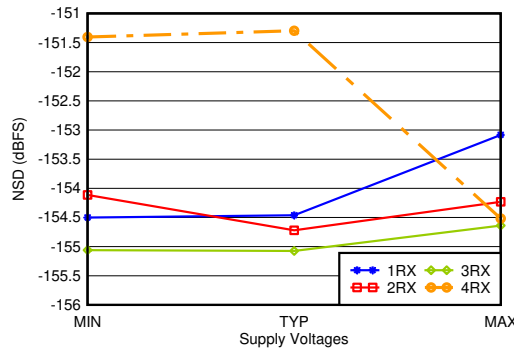
With 4.9GHz matching

Figure 4-419. RX Non-HD2/3 vs DSA Setting at 4.9GHz



With 4.9GHz matching,  $-7\text{dBFS}$  each tone, 20MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-420. RX IMD3 vs Supply and Channel at 4.9GHz



With 4.9GHz matching, 12.5MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 4-421. RX Noise Spectral Density vs Supply and Channel at 4.9GHz

### 4.12.13 RX Typical Characteristics at 8.1GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.

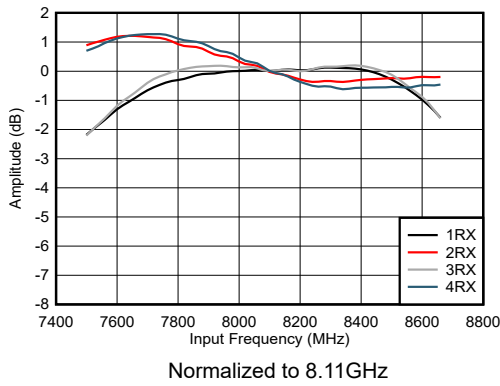


Figure 4-422. RX Amplitude vs Frequency and Channel

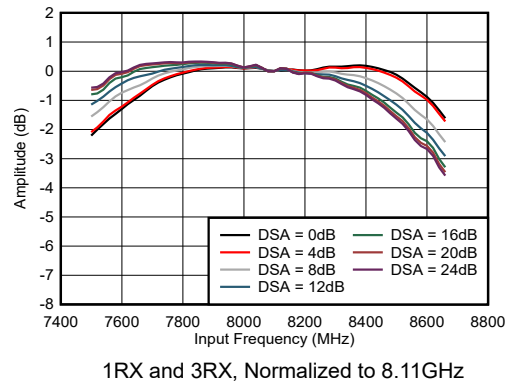


Figure 4-423. RX Amplitude vs Frequency and DSA Setting

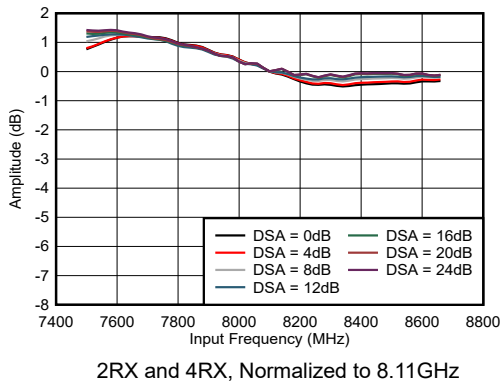


Figure 4-424. RX Amplitude vs Frequency and DSA Setting

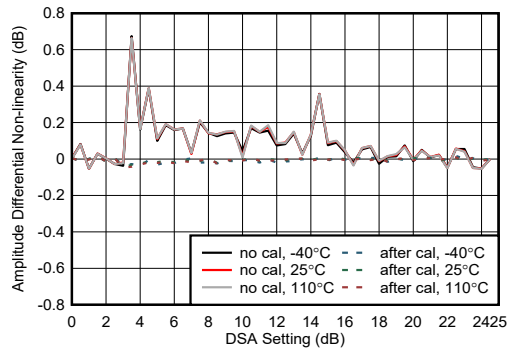


Figure 4-425. RX Amplitude Differential Nonlinearity at 8.1GHz

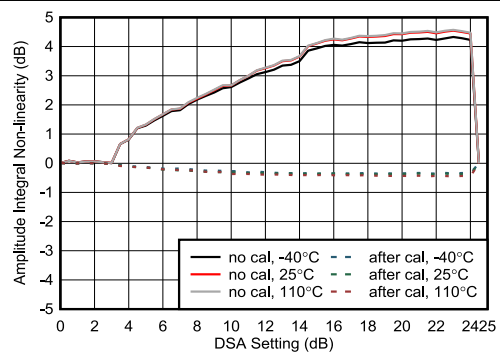


Figure 4-426. RX Amplitude Integrated Nonlinearity at 8.1GHz

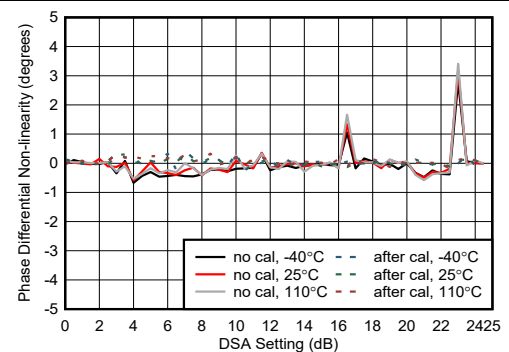
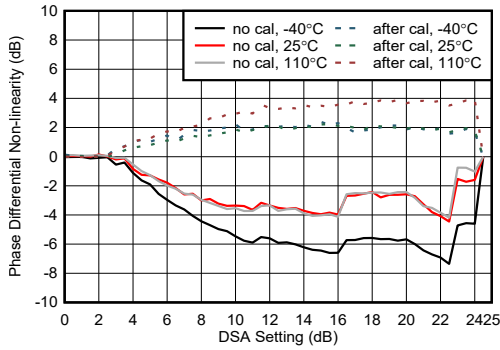


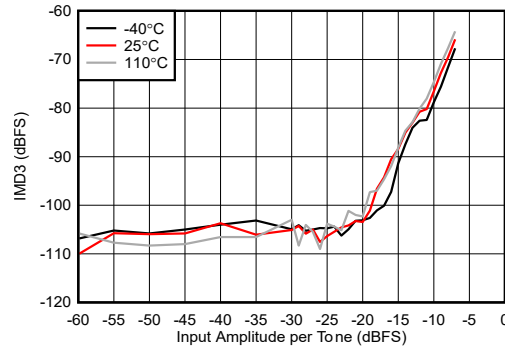
Figure 4-427. RX Phase Differential Nonlinearity at 8.1GHz

**4.12.13 RX Typical Characteristics at 8.1GHz (continued)**

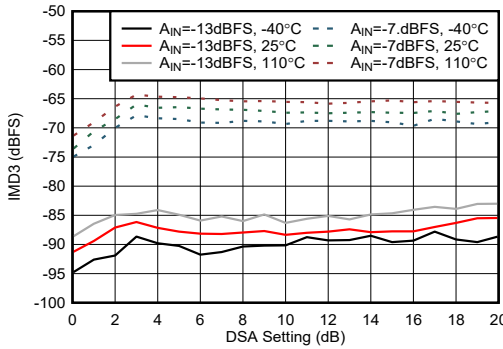
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.



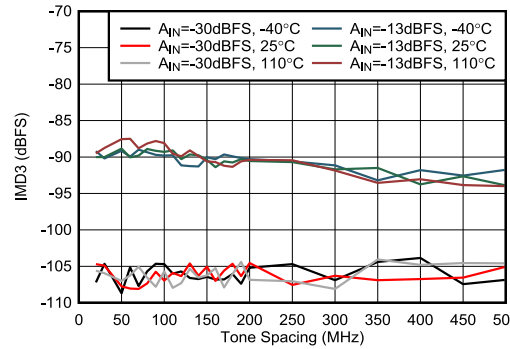
**Figure 4-428. RX Phase Differential Nonlinearity at 8.11GHz**



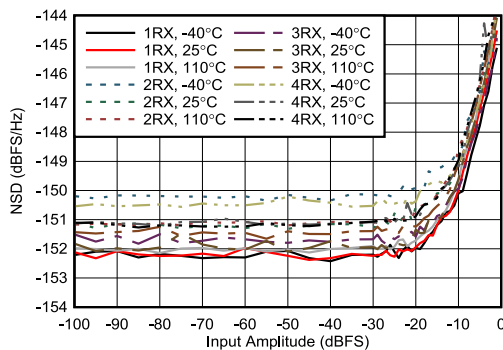
**Figure 4-429. RX IMD3 vs Input Amplitude at 8.11GHz**  
50MHz tone spacing



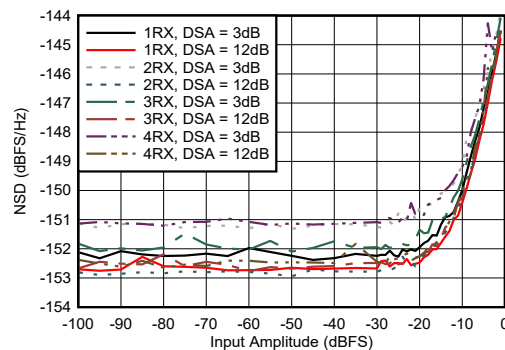
**Figure 4-430. RX IMD3 vs DSA Setting at 8.11GHz**  
50MHz tone spacing



**Figure 4-431. RX IMD3 vs Tone Spacing at 8.11GHz**



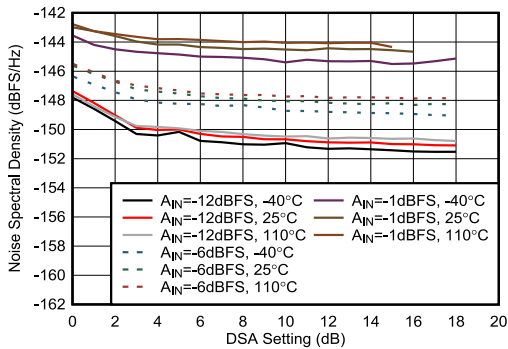
**Figure 4-432. RX NSD vs Digital Amplitude at 8.11GHz**



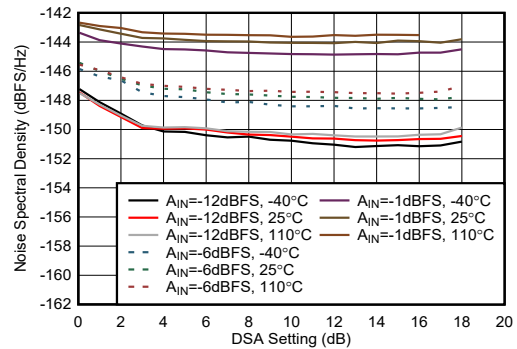
**Figure 4-433. RX NSD vs Digital Amplitude at 8.11GHz**

**4.12.13 RX Typical Characteristics at 8.1GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.

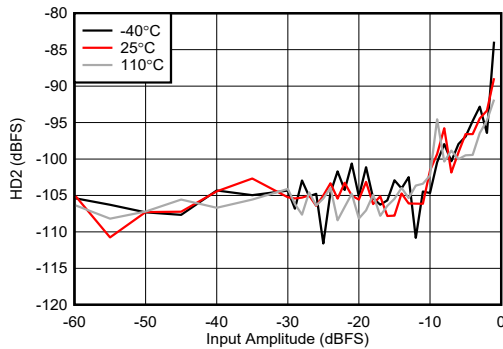


**Figure 4-434. RX NSD vs DSA Setting at 8.1GHz**

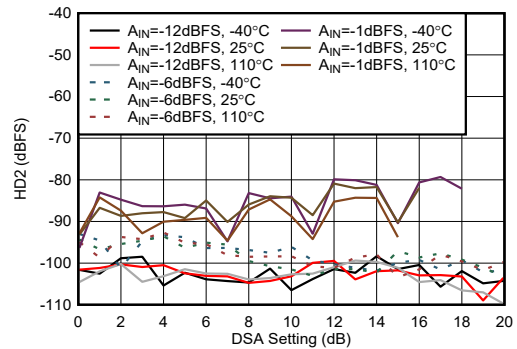


External clock mode

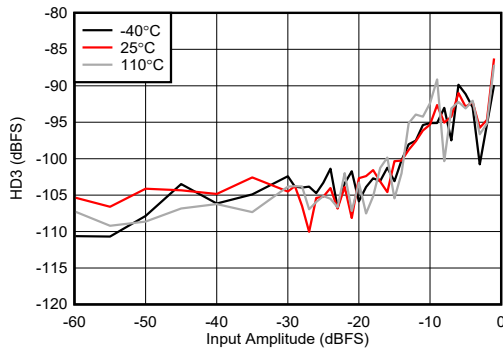
**Figure 4-435. RX NSD vs DSA Setting at 8.1GHz**



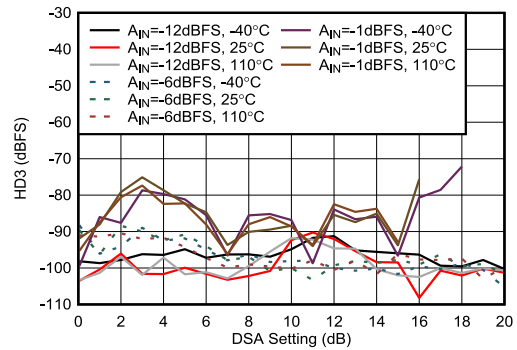
**Figure 4-436. RX HD2 vs Digital Amplitude at 8.1GHz**



**Figure 4-437. RX HD2 vs DSA Setting at 8.1GHz**



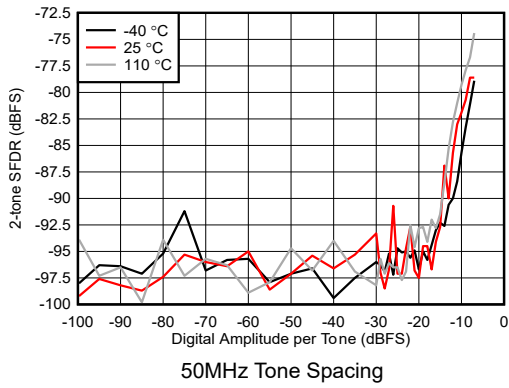
**Figure 4-438. RX HD3 vs Digital Amplitude at 8.1GHz**



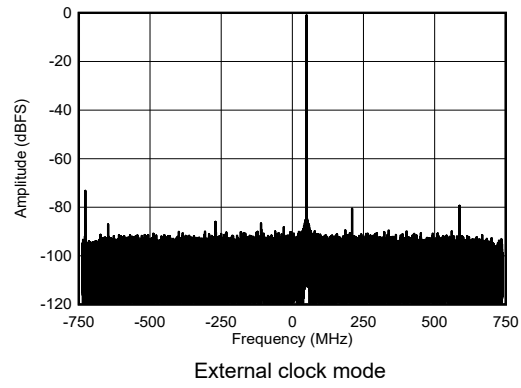
**Figure 4-439. RX HD3 vs DSA Setting at 8.1GHz**

**4.12.13 RX Typical Characteristics at 8.1GHz (continued)**

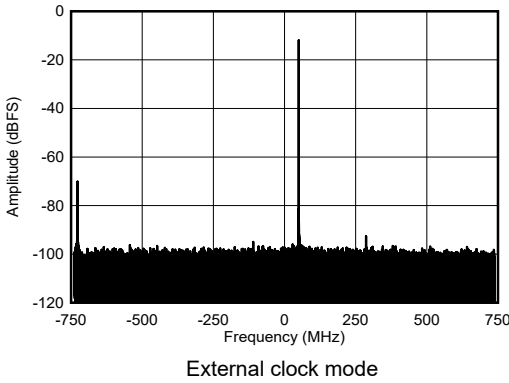
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.



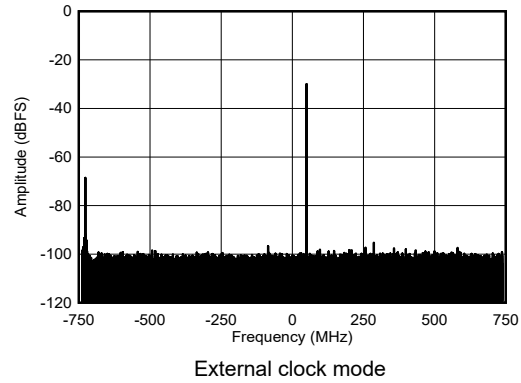
**Figure 4-440. RX 2-tone SFDR vs Digital Amplitude at 8.1GHz**



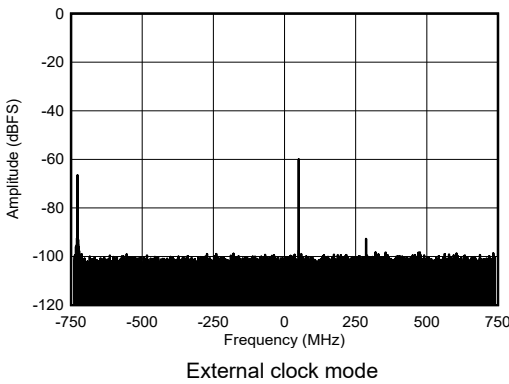
**Figure 4-441. RX Single Tone Output FFT at 8.1GHz, -1dBFS**



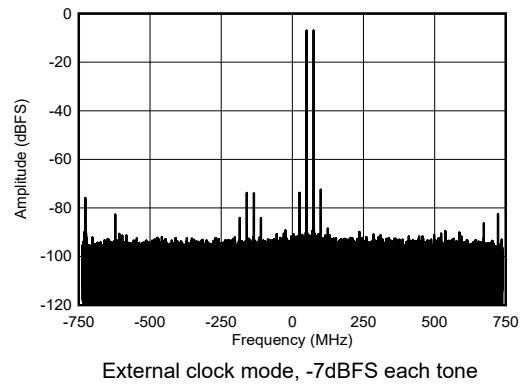
**Figure 4-442. RX Single Tone Output FFT at 8.1GHz, -12dBFS**



**Figure 4-443. RX Single Tone Output FFT at 8.1GHz, -30 dBFS**



**Figure 4-444. RX Single Tone Output FFT at 8.1GHz, -60 dBFS**

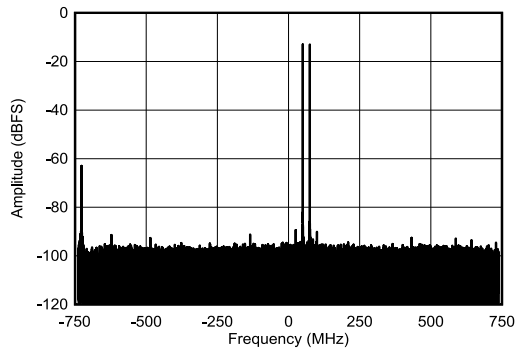


**Figure 4-445. RX Dual Tone Output FFT at 8.1GHz**



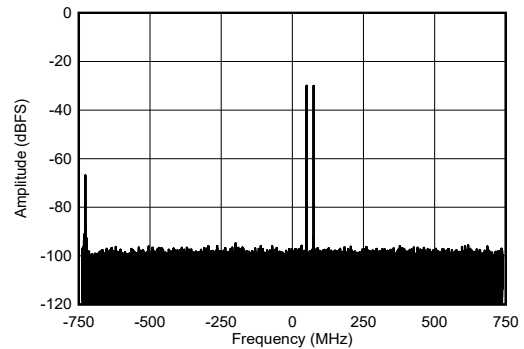
### 4.12.13 RX Typical Characteristics at 8.1GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 8.1GHz matching.



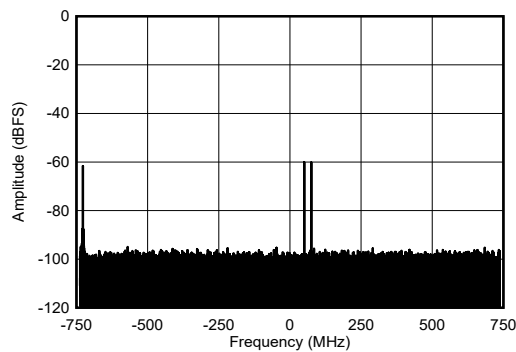
External clock mode, -13dBFS each tone

**Figure 4-446. RX Dual Tone Output FFT at 8.11GHz**



External clock mode, -30dBFS each tone

**Figure 4-447. RX Dual Tone Output FFT at 8.11GHz**



External clock mode, -60dBFS each tone

**Figure 4-448. RX Dual Tone Output FFT at 8.11GHz**

### 4.12.14 RX Typical Characteristics at 9.6GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 9.6GHz matching.

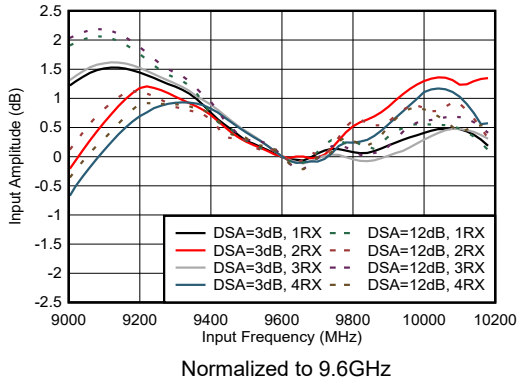


Figure 4-449. RX Input Amplitude vs Frequency

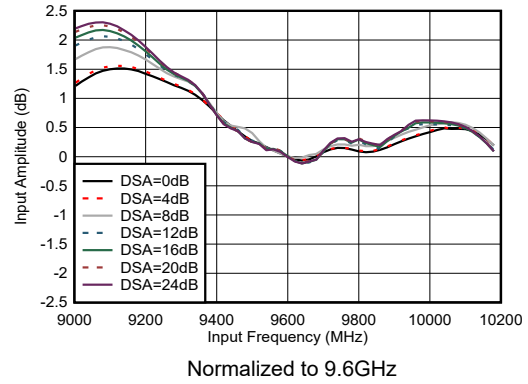


Figure 4-450. RX Input Amplitude vs Frequency at 9.6GHz

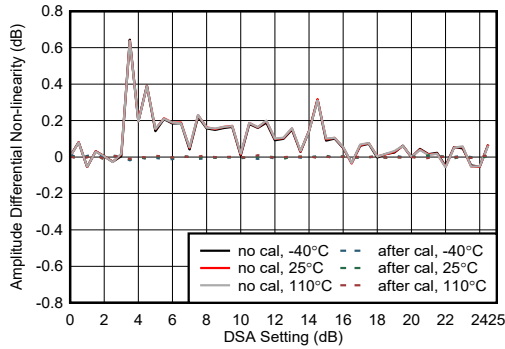


Figure 4-451. RX Amplitude Differential Non-linearity at 9.6GHz

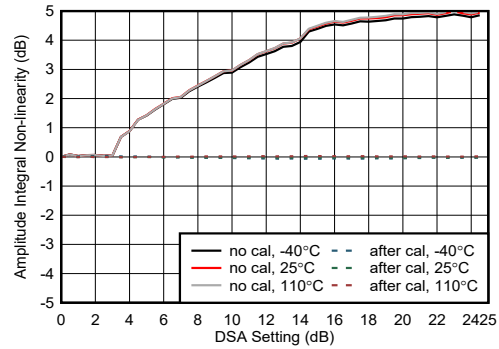


Figure 4-452. RX Amplitude Integrated Non-linearity at 9.6GHz

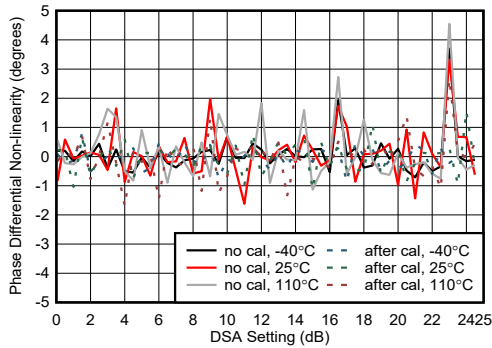


Figure 4-453. RX Phase Differential Non-linearity at 9.6GHz

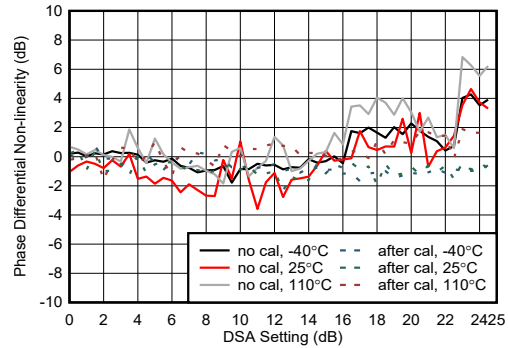
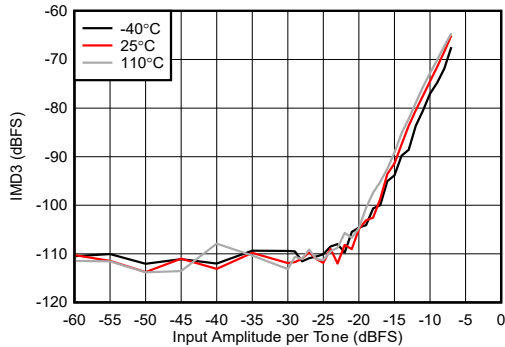


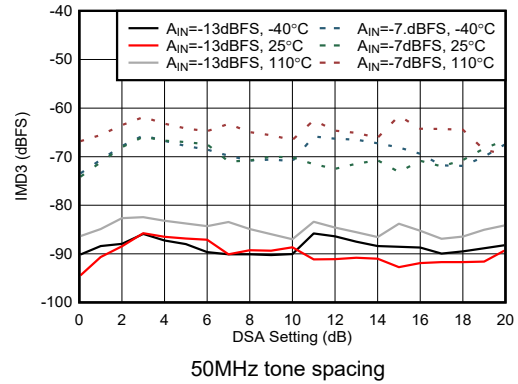
Figure 4-454. RX Phase Integrated Non-linearity at 9.6GHz

**4.12.14 RX Typical Characteristics at 9.6GHz (continued)**

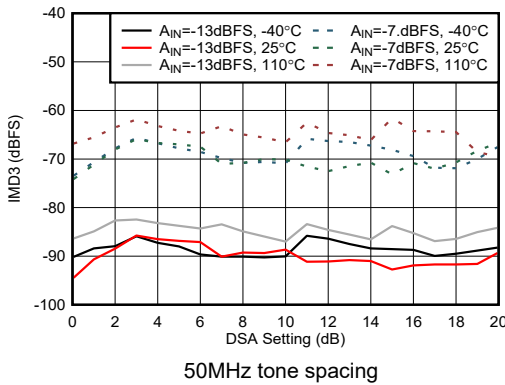
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 9.6GHz matching.



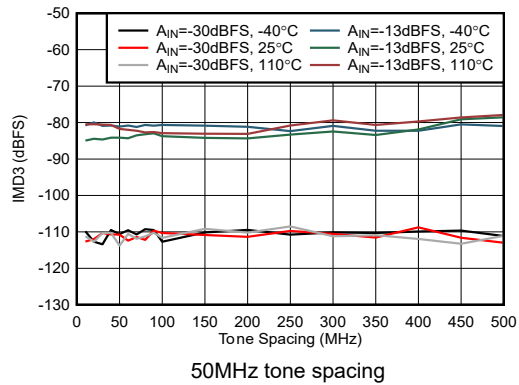
**Figure 4-455. RX IMD3 vs Digital Amplitude at 9.6GHz**



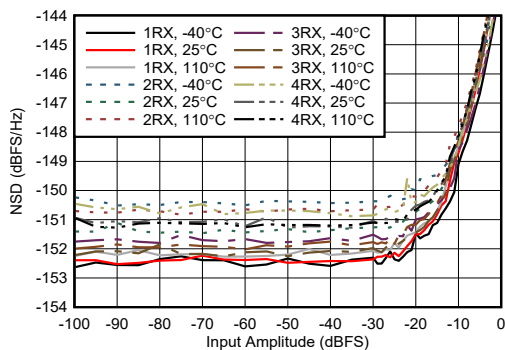
**Figure 4-456. RX IMD3 vs DSA Setting at 9.6GHz**



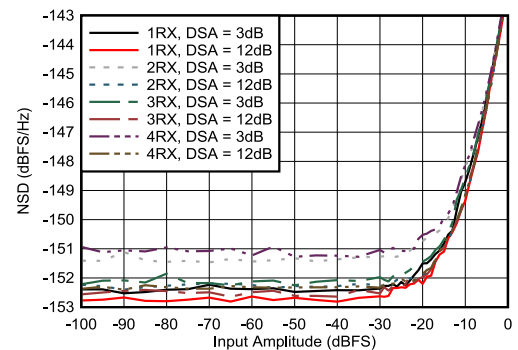
**Figure 4-457. RX IMD3 vs DSA Setting at 9.6GHz**



**Figure 4-458. RX IMD3 vs Tone Spacing at 9.6GHz**



**Figure 4-459. RX NSD vs Digital Amplitude at 9.6GHz**



**Figure 4-460. RX NSD vs Digital Amplitude at 9.6GHz**

### 4.12.14 RX Typical Characteristics at 9.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 9.6GHz matching.

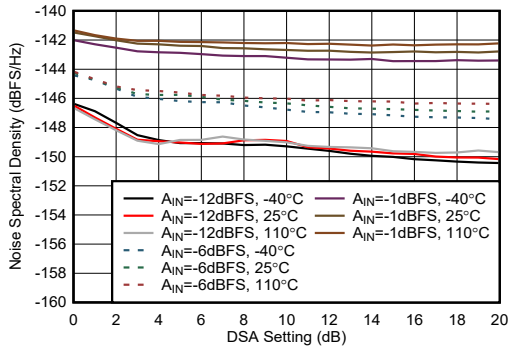


Figure 4-461. RX NSD vs DSA Setting at 9.6GHz

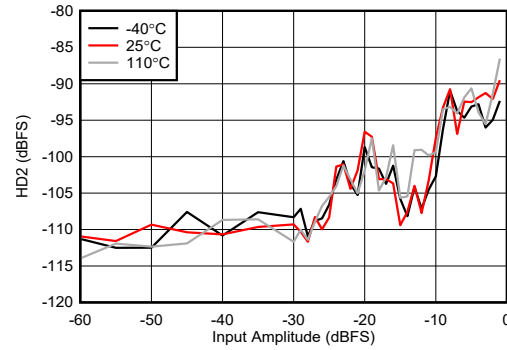


Figure 4-462. RX HD2 vs Digital Level at 9.6GHz

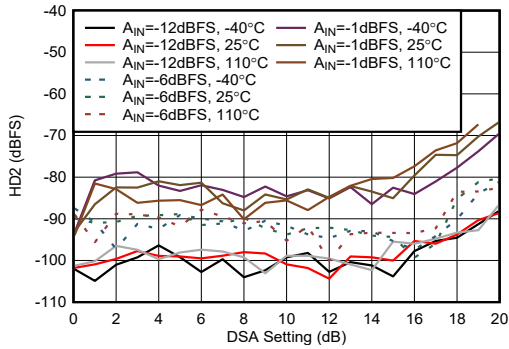


Figure 4-463. RX HD2 vs DSA Setting at 9.6GHz

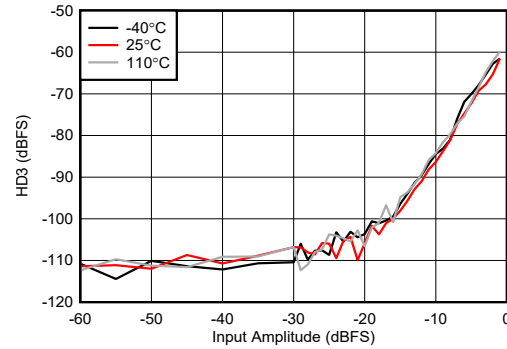


Figure 4-464. RX HD3 vs Digital Level at 9.6GHz

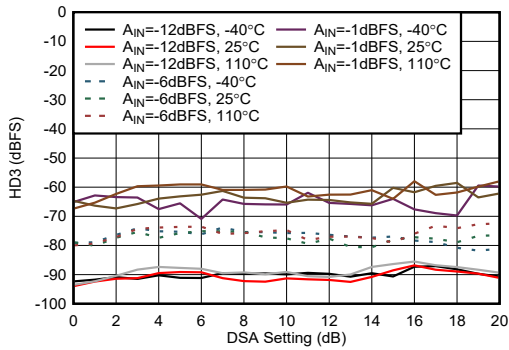
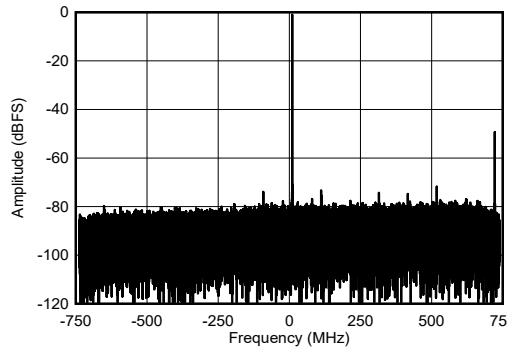


Figure 4-465. RX HD3 vs DSA Setting at 9.6GHz

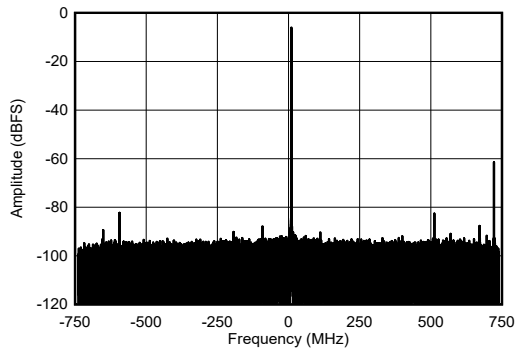


-1dBFS

Figure 4-466. RX Single Tone Output FFT at 9.61 GHz

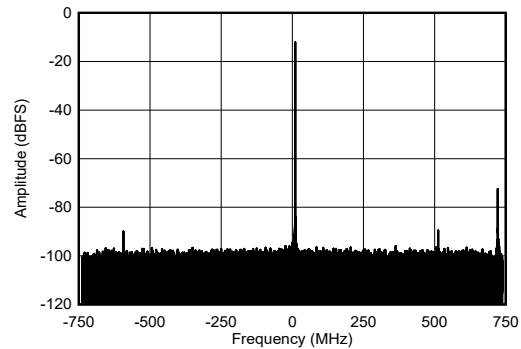
**4.12.14 RX Typical Characteristics at 9.6GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 9.6GHz matching.



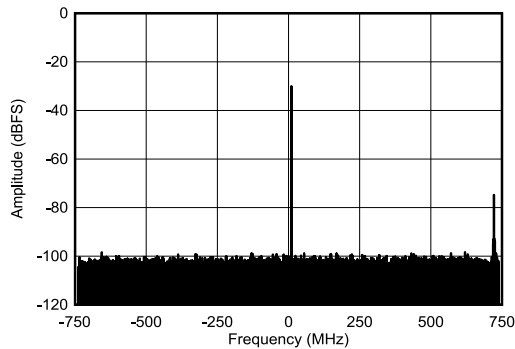
-6dBFS

**Figure 4-467. RX Single Tone Output FFT at 9.61GHz**



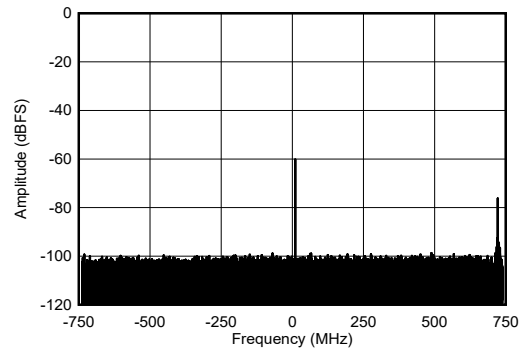
-12 dBFS.

**Figure 4-468. RX Single Tone Output FFT at 9.61GHz**



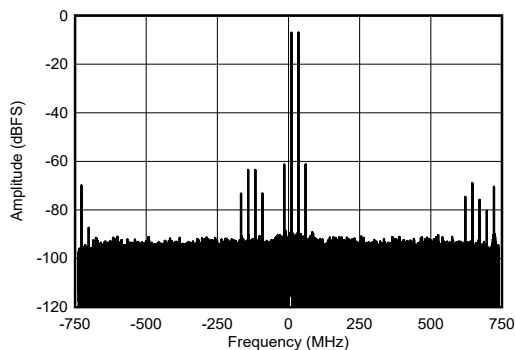
-30dBFS

**Figure 4-469. RX Single Tone Output FFT at 9.61GHz**



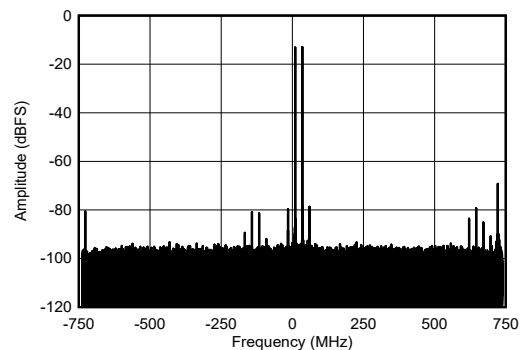
-60 dBFS

**Figure 4-470. RX Single Tone Output FFT at 9.61GHz**



9.61 and 9.635GHz, -7dBFS each tone

**Figure 4-471. RX Two Tone Output FFT at 9.61GHz**

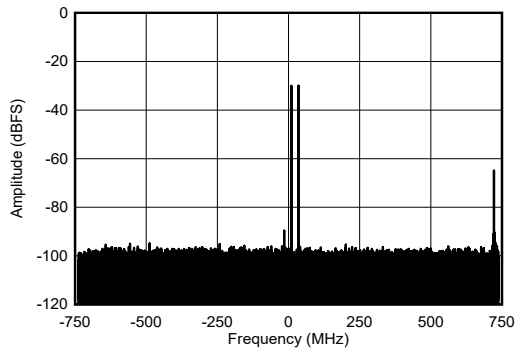


9.61 and 9.635GHz, -13dBFS each tone

**Figure 4-472. RX Two Tone Output FFT at 9.61GHz**

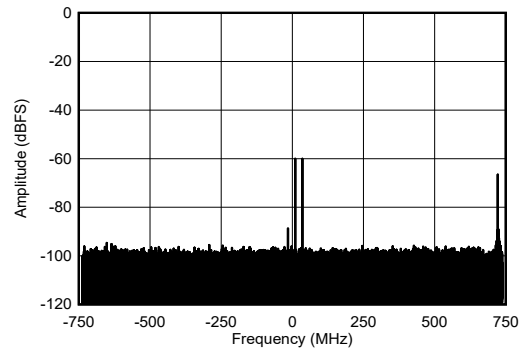
**4.12.14 RX Typical Characteristics at 9.6GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12MHz. Default conditions: output sample rate = 1474.56MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$ ,  $A_{\text{IN}} = -3\text{dBFS}$ , DSA setting = 3 dB, 9.6GHz matching.



9.61 and 9.635GHz, -30dBFS each tone

**Figure 4-473. RX Two Tone Output FFT at 9.61GHz**



9.61 and 9.635GHz, -60dBFS each tone

**Figure 4-474. RX Two Tone Output FFT at 9.61GHz**

## 5 Device and Documentation Support

### 5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 5.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 5.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 5.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 5.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from March 6, 2024 to August 1, 2024 (from Revision \* (March 2024) to Revision A (August 2024))

	<b>Page</b>
• Changed the RF frequency range from 10.2GHz to 12GHz (typical) in the <i>Features</i> .....	1
• Changed the RF frequency range from 10.2GHz to 12GHz in the <i>Description</i> .....	1
• Changed the RF frequency range to 12000MHz.....	6
• Changed the RF frequency range to 12000MHz.....	13

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE7950ALKSHP	ACTIVE	FCBGA	ALK	400	90	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 85	AFE7950SHP SNPB	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF AFE7950-SP :**

- Catalog : [AFE7950](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TRAY**

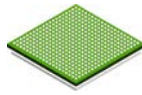


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE7950ALKSHP	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2

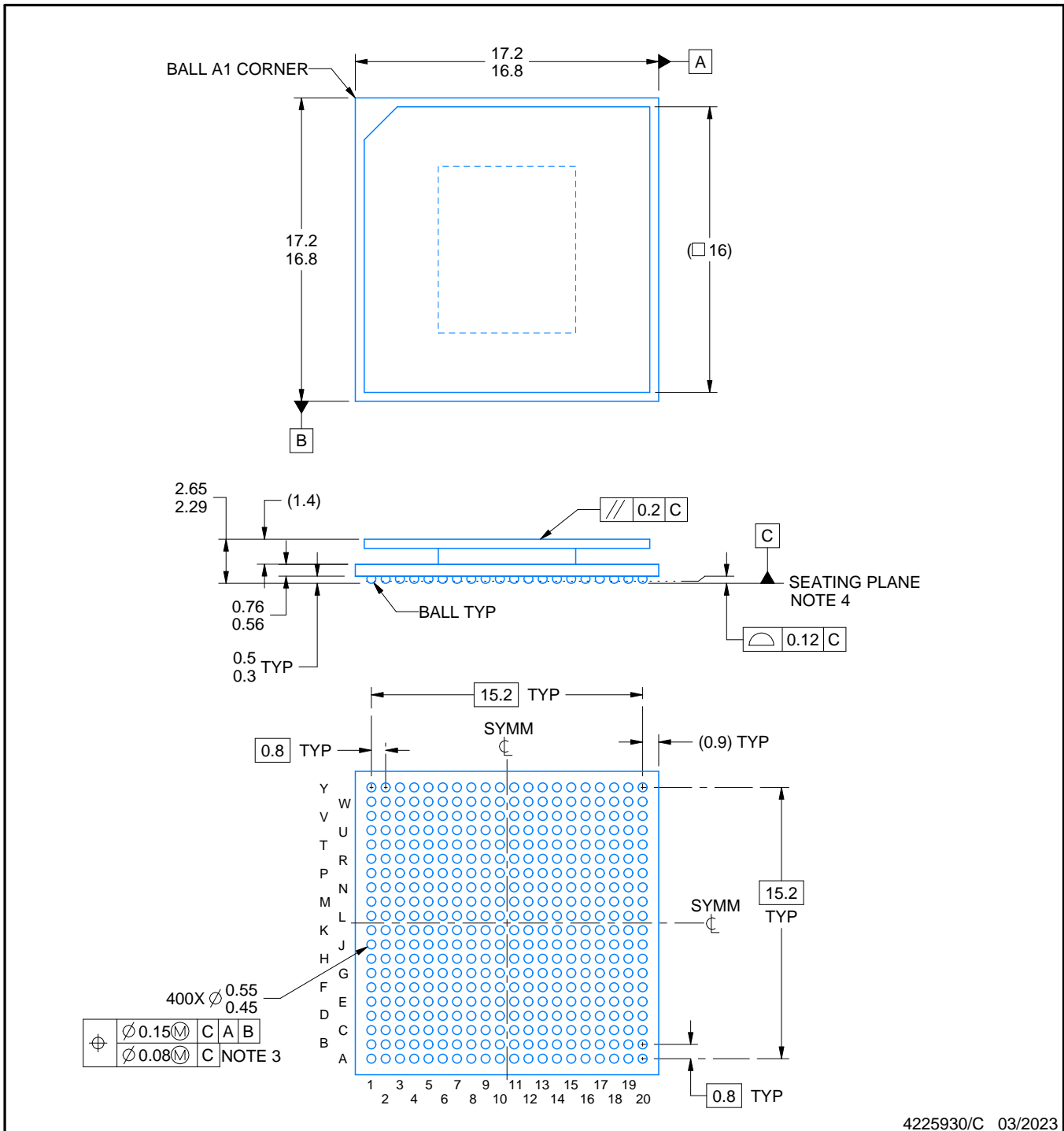
# ALK0400A



# PACKAGE OUTLINE

## FCBGA - 2.65 mm max height

BALL GRID ARRAY



4225930/C 03/2023

### NOTES:

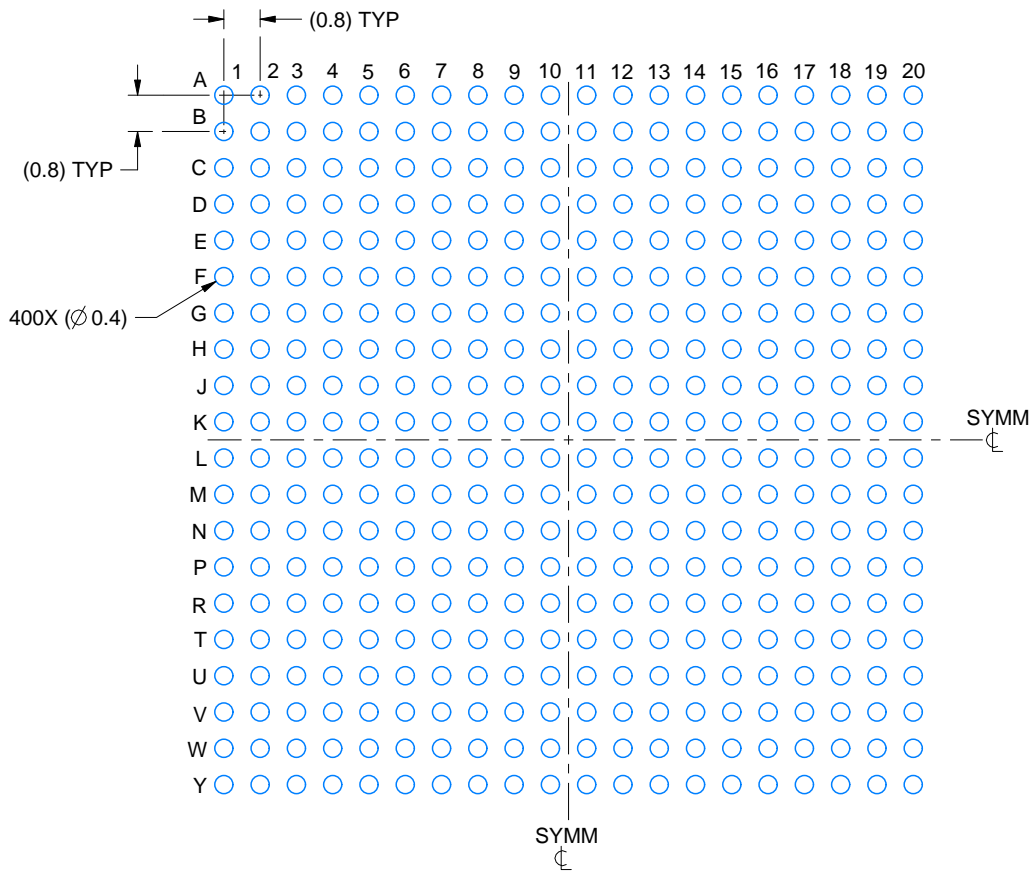
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).

# EXAMPLE BOARD LAYOUT

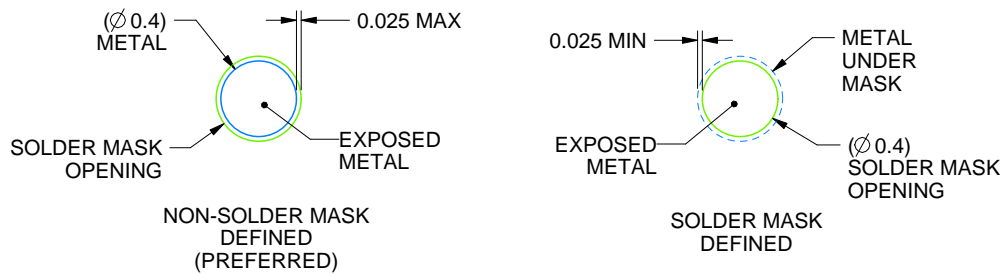
ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

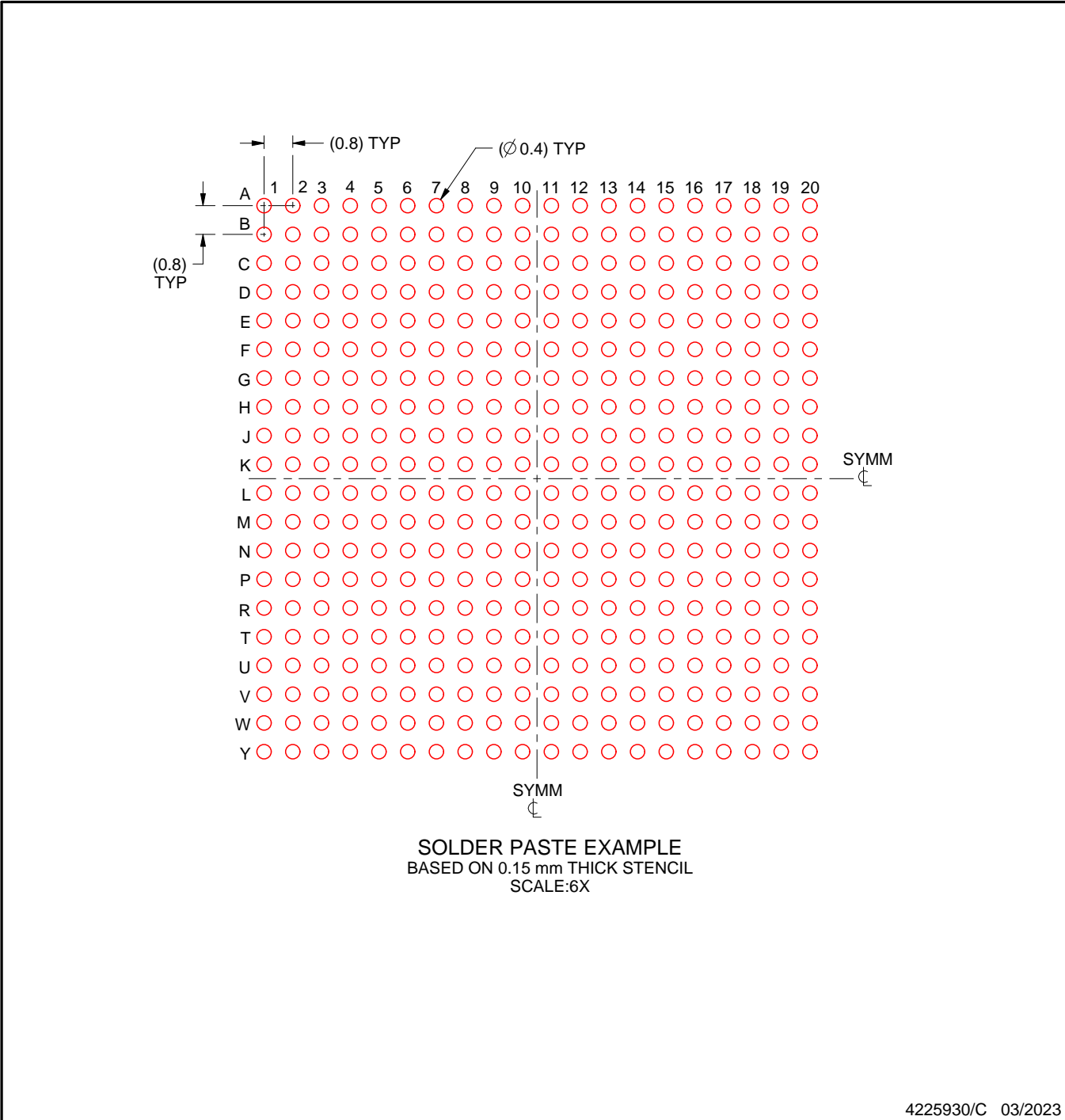
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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