CDx4HC4094, CD74HCT4094 High-Speed CMOS Logic 8-Stage Shift and Store Bus Register, Three-State

1 Features

- Buffered inputs
- Separate serial outputs synchronous to both positive and negative clock edges for cascading
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temp range: −55°C to 125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- HC types
  - 2- to 6-V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V
- HCT types
  - 4.5- to 5.5-V operation
  - Direct LSTTL input logic compatibility, V_{IL}= 0.8 V (Max), V_{IH} = 2 V (Min)
  - CMOS input compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

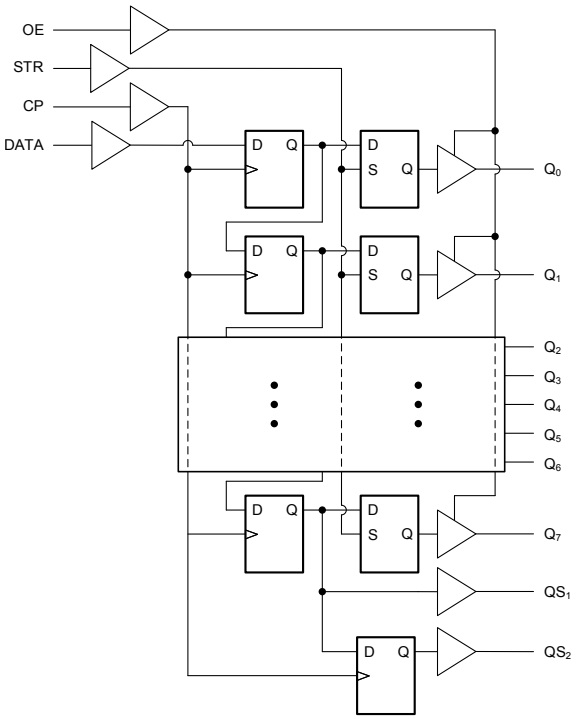
2 Description

The CDx4HC4094 and CD74HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input to parallel buffered tri-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the Strobe input is high. Data in the storage register appears at the outputs whenever the Output-Enable signal is high.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
CD54HC4094F3A	CDIP (16)	24.38 mm × 6.92 mm
CD74HC4094M	SOIC (16)	9.90 mm × 3.90 mm
CD74HC4094E	PDIP (16)	19.31 mm × 6.35 mm
CD74HC4094NSR	SO (16)	6.20 mm × 5.30 mm
CD74HC4094PW	TSSOP (16)	5.00 mm × 4.40 mm
CD74HCT4094M	SOIC (16)	9.90 mm × 3.90 mm
CD74HCT4094E	PDIP (16)	19.31 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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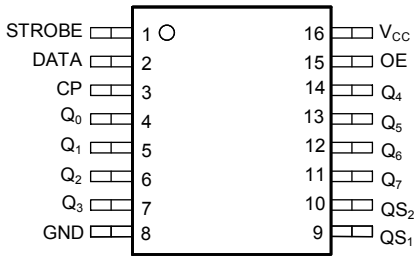
3 Revision History

Changes from Revision E (December 2010) to Revision F (March 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the doucment to reflect modern data sheet standards	1

4 Pin Configuration and Functions



J, N, D, NS, or PW package
16-Pin CDIP, PDIP, SOIC, SO, or TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input diode current	For V_I < –0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	Output diode current	For V_O < –0.5 V or V_O > V_{CC} + 0.5 V		±20	mA
I_O	Output source or sink current per output pin	For V_O > –0.5 V or V_O < V_{CC} + 0.5 V		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		– 65	150	°C
	Maximum lead temperature (Soldering 10s) (SOIC - lead tips only)			300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2		6	V
		HCT types	4.5		5.5	
V_I, V_O	Input or output voltage		0		V_{CC}	V
t_t	Input rise and fall time	2 V			1000	ns
		4.5 V			500	
		6 V			400	
T_A	Temperature range		–55		125	°C

5.3 Thermal Information

THERMAL METRIC		N (PDIP)	D (SOIC)(2)	NS (SOP)	PW (TSSOP)	UNIT
		PINS	PINS	PINS	PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	67	73	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.
(2) Lead tips only

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(2)	V_{CC} (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High-level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V_{IL}	Low-level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	V
			6			1.8		1.8		1.8	V
V_{OH}	High-level output voltage CMOS loads	I_{OH} = – 20μA	2	1.9			1.9		1.9		V
		I_{OH} = – 20μA	4.5	4.4			4.4		4.4		V
		I_{OH} = – 20μA	6	5.9			5.9		5.9		V
	High-level output voltage TTL loads	I_{OH} = – 6mA	4.5	3.98			3.84		3.7		V
		I_{OH} = – 7.8mA	6	5.48			5.34		5.2		V
V_{OL}	Low-level output voltage CMOS loads	I_{OL} = 20μA	2			0.1		0.1		0.1	V
		I_{OL} = 20μA	4.5			0.1		0.1		0.1	V
		I_{OL} = 20μA	6			0.1		0.1		0.1	V
	Low-level output voltage TTL loads	I_{OL} = 6mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 7.8mA	6			0.26		0.33		0.4	V
I_I	Input leakage current	V_{CC} or GND	6			±0.1		±1		±1	μA
I_{CC}	Supply current	V_{CC} or GND	6			8		80		160	μA
HCT TYPES											
V_{IH}	High-level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low-level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High-level output voltage CMOS loads	I_{OH} = – 20μA	4.5	4.4			4.4		4.4		V
	High-level output voltage TTL loads	I_{OH} = – 6mA	4.5	3.98			3.84		3.7		V
V_{OL}	Low-level output voltage CMOS loads	I_{OL} = 20μA	4.5			0.1		0.1		0.1	V
	Low-level output voltage TTL loads	I_{OL} = 6mA	4.5			0.26		0.33		0.4	V
I_I	Input leakage current	V_{CC} and GND	5.5			±0.1		±1		±1	μA
I_{CC}	Supply Current	V_{CC} and GND	5.5			8		80		160	μA
ΔI_{CC} (1) (3)	Additional quiescent device current per input pin: 1 unit load	D	4.5 to 5.5		40	144		180		196	μA
		CP, OE	4.5 to 5.5		150	540		675		735	μA
		STR	4.5 to 5.5		100	360		450		490	μA

(1) For dual−supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(2) $V_I = V_{IH}$ or V_{IL}, unless otherwise noted.
(3) Inputs held at V_{CC} – 2.1.

5.5 Prerequisite for Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		V_{CC} (V)	25°C		–40 to 85°C		–55 to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
t_W	CP pulse duration	2	80		100		120		ns
		4.5	16		20		24		
		6	14		17		20		
t_{WH}	STR pulse duration	2	80		100		120		ns
		4.5	16		20		24		
		6	14		17		20		
t_{SU}	Data set-up time	2	50		65		75		ns
		4.5	10		13		15		
		6	9		11		13		
t_H	Data hold time	2	3		3		3		ns
		4.5	3		3		3		
		6	3		3		3		
t_{SU}	STR set-up time	2	100		125		150		ns
		4.5	20		25		30		
		6	17		21		26		
t_H	STR hold time	2	0		0		0		ns
		4.5	0		0		0		
		6	0		0		0		
$f_{CL\ (MAX)}$	Maximum CP frequency	2	6		5		4		MHz
		4.5	30		24		20		
		6	35		28		24		
HCT TYPES									
t_W	CP pulse duration	4.5	16		20		24		ns
t_{WH}	STR pulse duration	4.5	16		20		24		ns
t_{SU}	Data set-up time	4.5	10		13		15		ns
t_H	Data hold time	4.5	4		4		4		ns
t_{SU}	STR set-up time	4.5	20		25		30		ns
t_H	STR hold time	4.5	0		0		0		ns
$f_{CL\ (MAX)}$	Maximum CP frequency	4.5	30		24		20		MHz

5.6 Switching Characteristics

Input t_r, t_f = 6 ns. Unless otherwise specified, CL = 50pF Parameter Measurement Information

PARAMETER		V_{CC} (V)	25°C			–40 to 85°C		–55 to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t_{pd}	Propagation delay time CP to QS_1	2			150		190		225	ns
		4.5		12[3]	30		38		45	
		6			26		33		38	
t_{pd}	CP to QS_2	2			135		170		205	ns
		4.5		11[3]	27		34		41	
		6			23		29		35	
t_{pd}	CP to Q_n	2			195		245		295	ns
		4.5		16[3]	39		49		59	
		6			33		42		50	
t_t	STR to Q_n	2			180		225		270	ns
		4.5			36		45		54	
		6			31		38		46	
t_{PZH}, t_{PZL}	Output enable to Q_n	2			175		220		265	ns
		4.5			35		44		53	
		6			30		37		45	
t_{PHZ}, t_{PLZ}	Output disable to Q_n	2			125		155		190	ns
		4.5			25		31		38	
		6			21		26		32	
t_{TLH}, t_{THL}	Output transition time	2			75		95		110	ns
		4.5			15		19		22	
		6			13		16		19	
t_{PHZ}, t_{PLZ}	Output disabling time	5		10[3]						ns
f_{MAX}	Maximum CP frequency	5		60[3]						MHz
C_{IN}	Input capacitance				10		10		10	pF
C_{PD}	Power dissipation capacitance[1], [2]	5		90[3]						pF
C_O	Tri-state output capacitance				15		15		15	pF
HCT TYPES										
t_{PLH}, t_{PHL}	Propagation delay time CP to QS_1	4.5		16[3]	39					ns
	CP to QS_2	4.5		15[3]	36					ns
	CP to Q_n	4.5		18[3]	43					ns
	STR to Q_n	4.5			39					ns
t_{PZH}, t_{PZL}	Output enable to Q_n	4.5			35					ns
t_{PHZ}, t_{PLZ}	Output disable to Q_n	4.5			35					ns
t_{TLH}, t_{THL}	Output transition time	4.5			15					ns
t_{PHZ}, t_{PLZ}	Output disabling time	5		14[3]						ns
f_{MAX}	Maximum CP frequency	5		60[3]						MHz
C_{IN}	Input capacitance				10		10		10	pF

Input t_r, t_f = 6 ns. Unless otherwise specified, CL = 50pF Parameter Measurement Information

PARAMETER		V_{CC} (V)	25°C			–40 to 85°C		–55 to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
C_{PD}	Power dissipation capacitance(1), (2)	5		110(3)						pF
C_O	Tri-state output capacitance				15		15		15	pF

(1) C_{PD} is used to determine the dynamic power consumption, per register.
(2) $P_D = V_{CC}{}^2 f_i$ (CPD + CL) where f_i = Input frequency, C_L = Output load capacitance, V_{CC} = Supply voltage.
(3) Typical value tested at 5V, CL = 15pF

6 Parameter Measurement Information

t_{PD} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

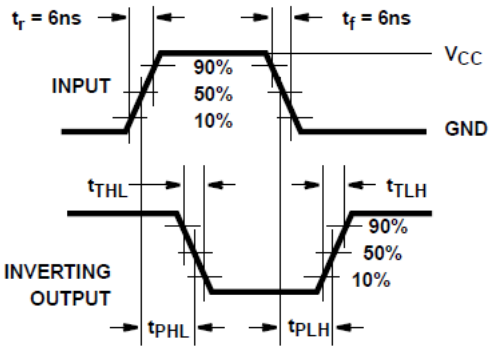


Figure 6-1. HC and HCT transition times and propagation delay times, combination logic

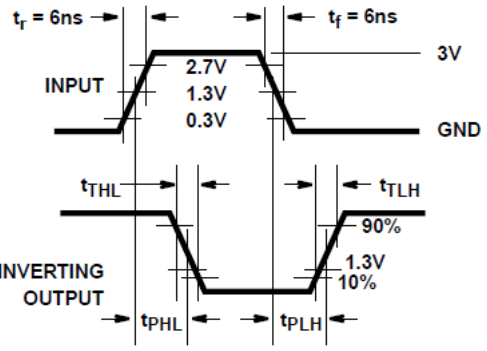


Figure 6-2. HCT transition times and tpopationg delay times, combination logic

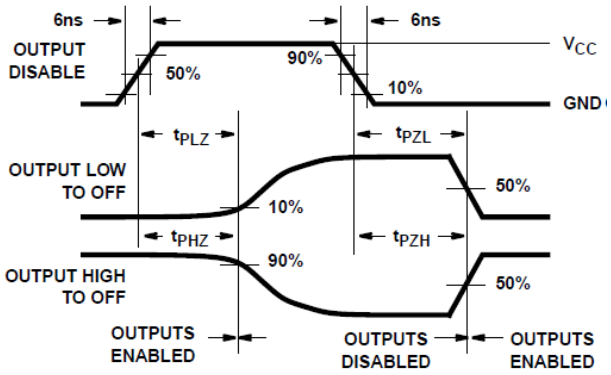


Figure 6-3. HC three-state propagation delay waveform

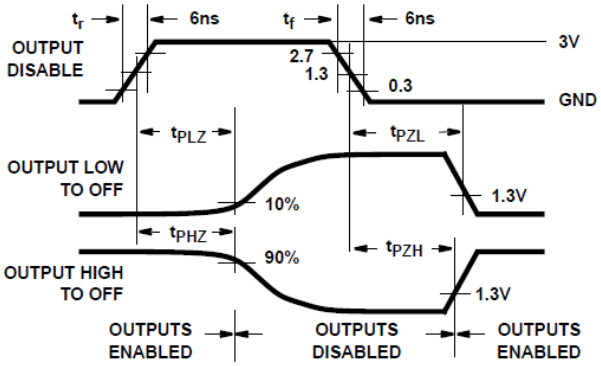
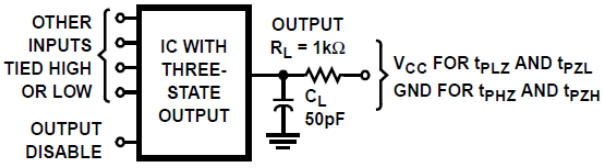


Figure 6-4. HCT three-state propagation delay waveform



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

Figure 6-5. HC and HCT three-state propagation delay test circuit

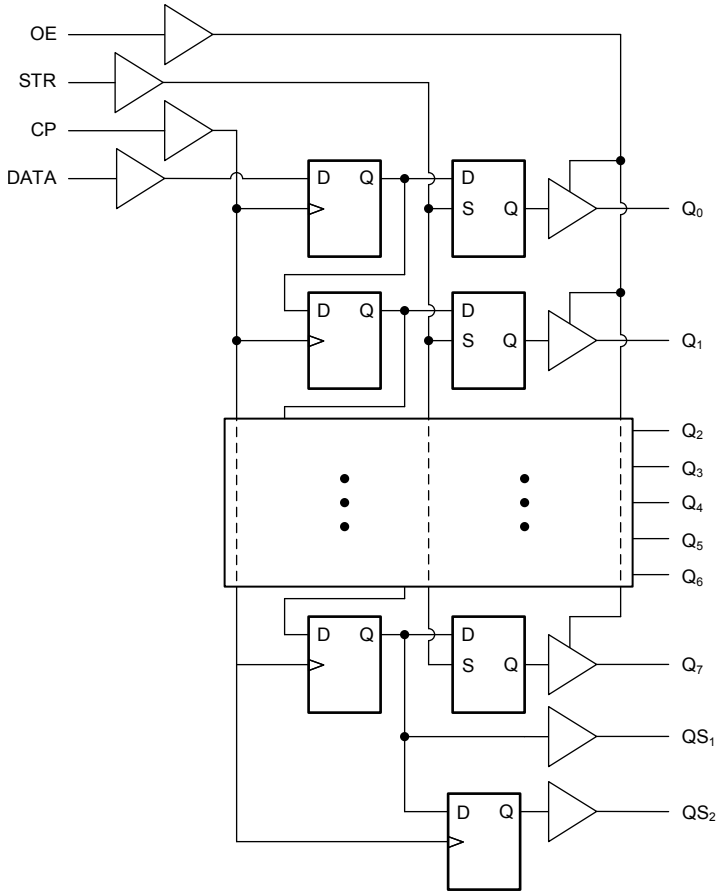
7 Detailed Description

7.1 Overview

The CDx4HC4094 and CD74HCT4094 are 8-stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input to parallel buffered tri-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the Strobe input is high. Data in the storage register appears at the outputs whenever the Output-Enable signal is high.

Two serial outputs are available for cascading a number of these devices. Data is available at the QS_1 serial output terminal on positive clock edges to allow for high-speed operation in cascaded system in which the clock rise time is fast. The same serial information, available at the QS_2 terminal on the next negative clock edge, provides a means for cascading these devices when the clock rise time is slow.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Truth Table

Inputs[2]				Parallel Outputs		Serial Outputs	
CP	OE	STR	D	Q_0	Q_n	QS_1 [1]	QS_2
↑	L	X	X	Z	Z	Q_6	NC
↓	L	X	X	Z	Z	NC	Q_7
↑	H	L	X	NC	NC	Q_6	NC
↑	H	H	L	L	$Q_n - 1$	Q_6	NC
↑	H	H	H	H	$Q_n - 1$	Q_6	NC
↓	H	H	H	NC	NC	NC	Q_7

(1) At the positive clock edge the information in the seventh register stage is transferred to the eighth register stage and QS_1 output.
(2) H = High voltage level, L = Low voltage level, X = Don't care, NC = No charge, Z = High-impedance off−state, ↑ = Transition from low-to-high level, ↓ = Transition from high to low.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HC4094F3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC4094F3A	Samples
CD74HC4094E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4094E	Samples
CD74HC4094M	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	HC4094M	
CD74HC4094M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC4094M	Samples
CD74HC4094M96G3	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	HC4094M	Samples
CD74HC4094M96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4094M	Samples
CD74HC4094MT	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	HC4094M	
CD74HC4094NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4094M	Samples
CD74HC4094NSRE4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4094M	Samples
CD74HC4094PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-55 to 125	HJ4094	
CD74HC4094PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HJ4094	Samples
CD74HC4094PWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4094	Samples
CD74HC4094PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4094	Samples
CD74HCT4094E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4094E	Samples
CD74HCT4094EE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4094E	Samples
CD74HCT4094M	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-55 to 125	HCT4094M	
CD74HCT4094M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HCT4094M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD54HC4094, CD74HC4094 :

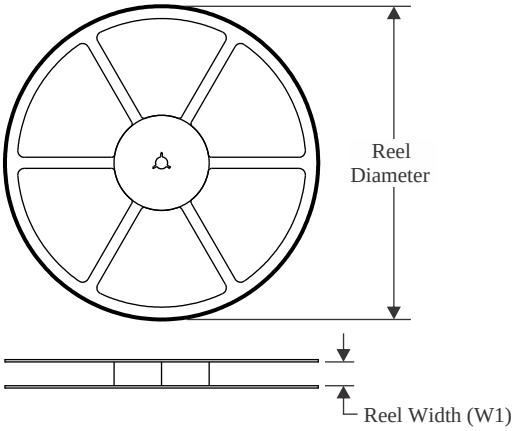
- Catalog : CD74HC4094
- Military : CD54HC4094

NOTE: Qualified Version Definitions:

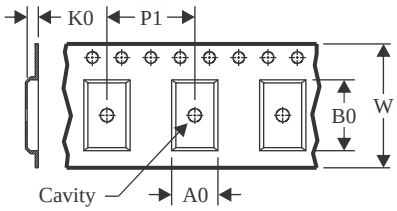
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

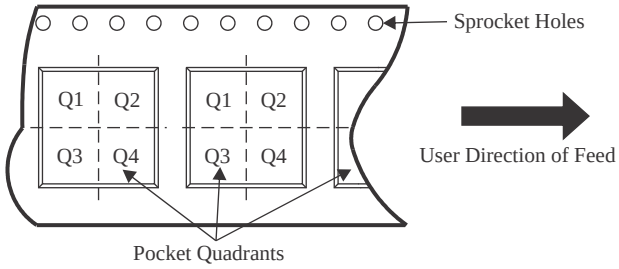


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

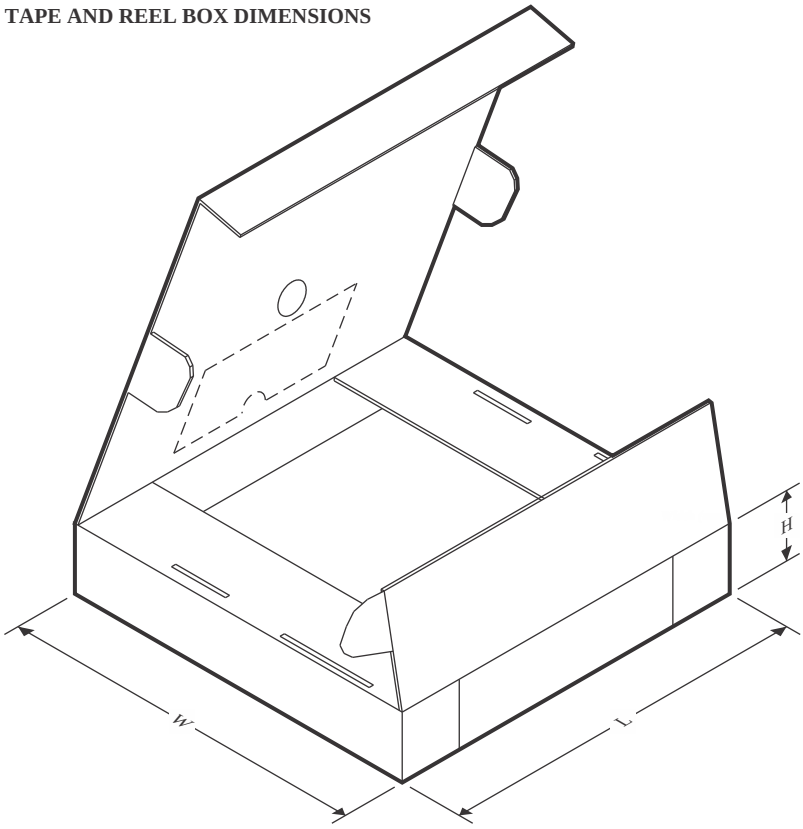
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4094M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4094M96G3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4094M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4094NSR	SO	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD74HC4094NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC4094PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4094PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4094PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT4094M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

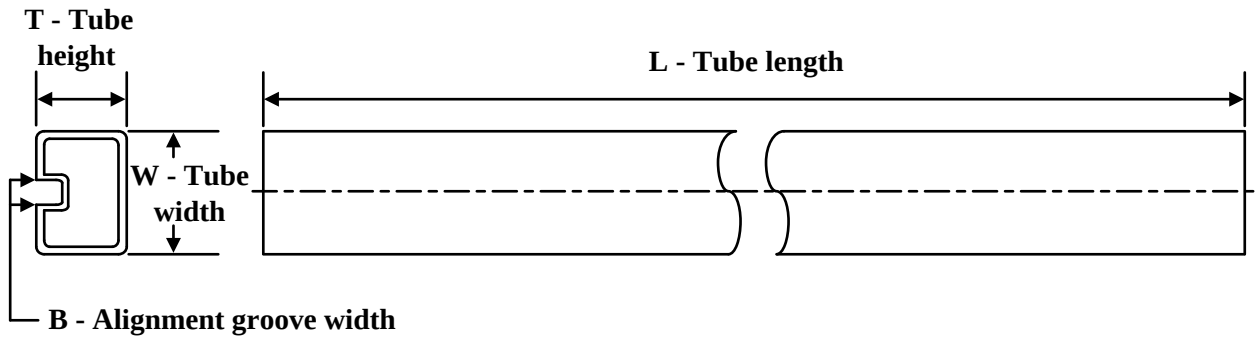
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4094M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HC4094M96G3	SOIC	D	16	2500	364.0	364.0	27.0
CD74HC4094M96G4	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC4094NSR	SO	NS	16	2000	356.0	356.0	35.0
CD74HC4094NSR	SO	NS	16	2000	356.0	356.0	35.0
CD74HC4094PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HC4094PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HC4094PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HCT4094M96	SOIC	D	16	2500	356.0	356.0	35.0

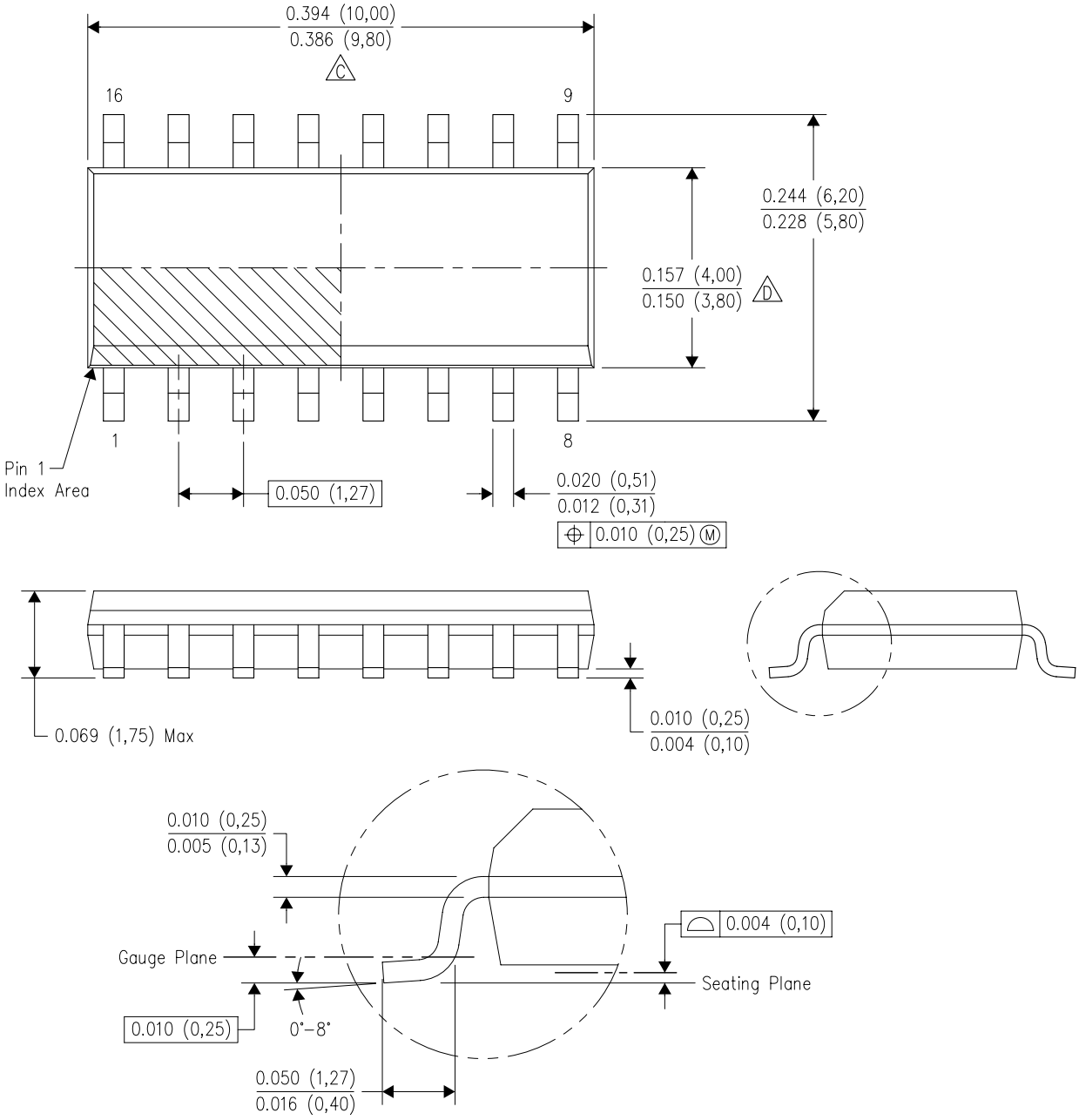
TUBE



*All dimensions are nominal

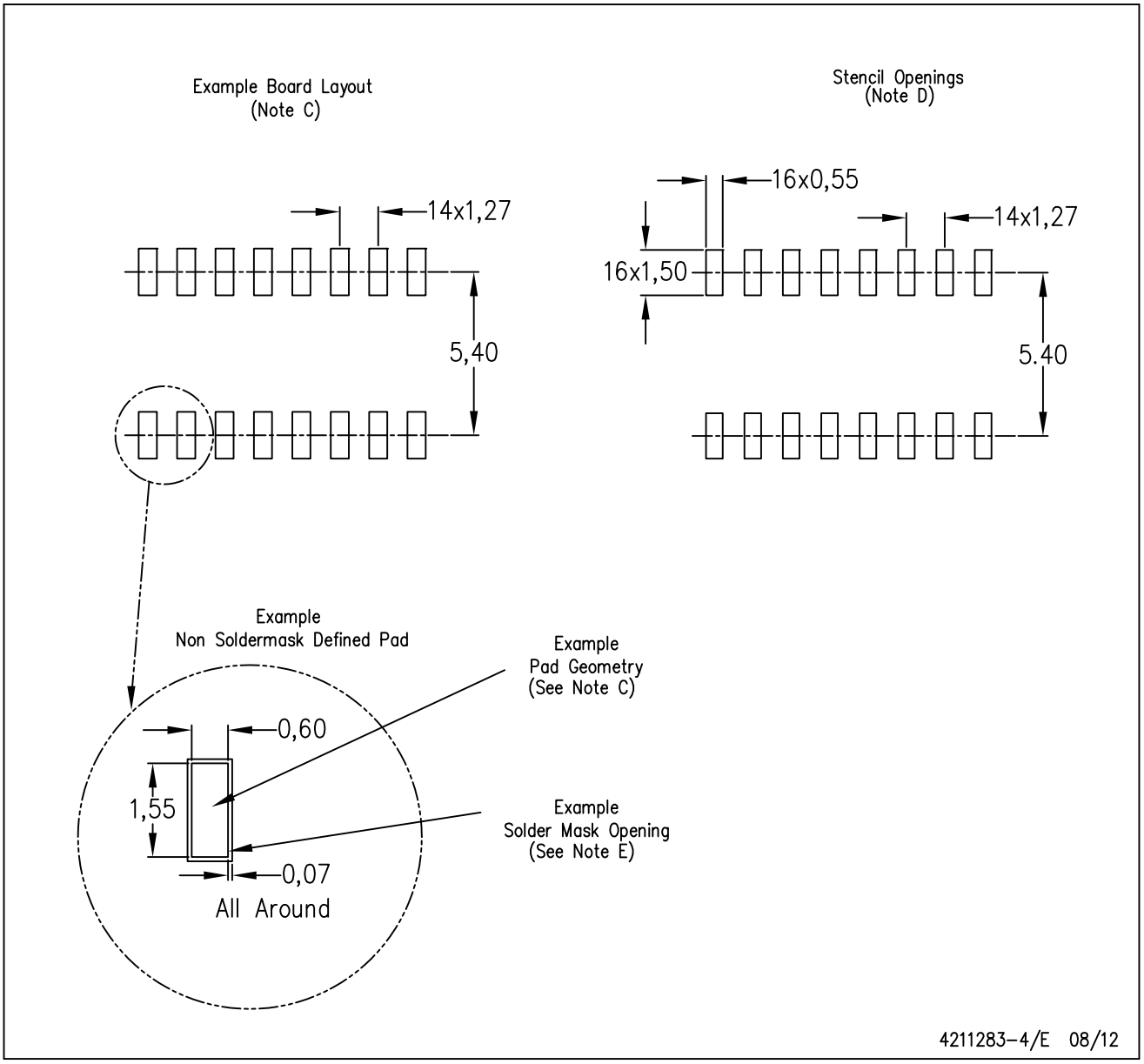
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC4094E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC4094E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4094E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4094E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4094EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT4094EE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



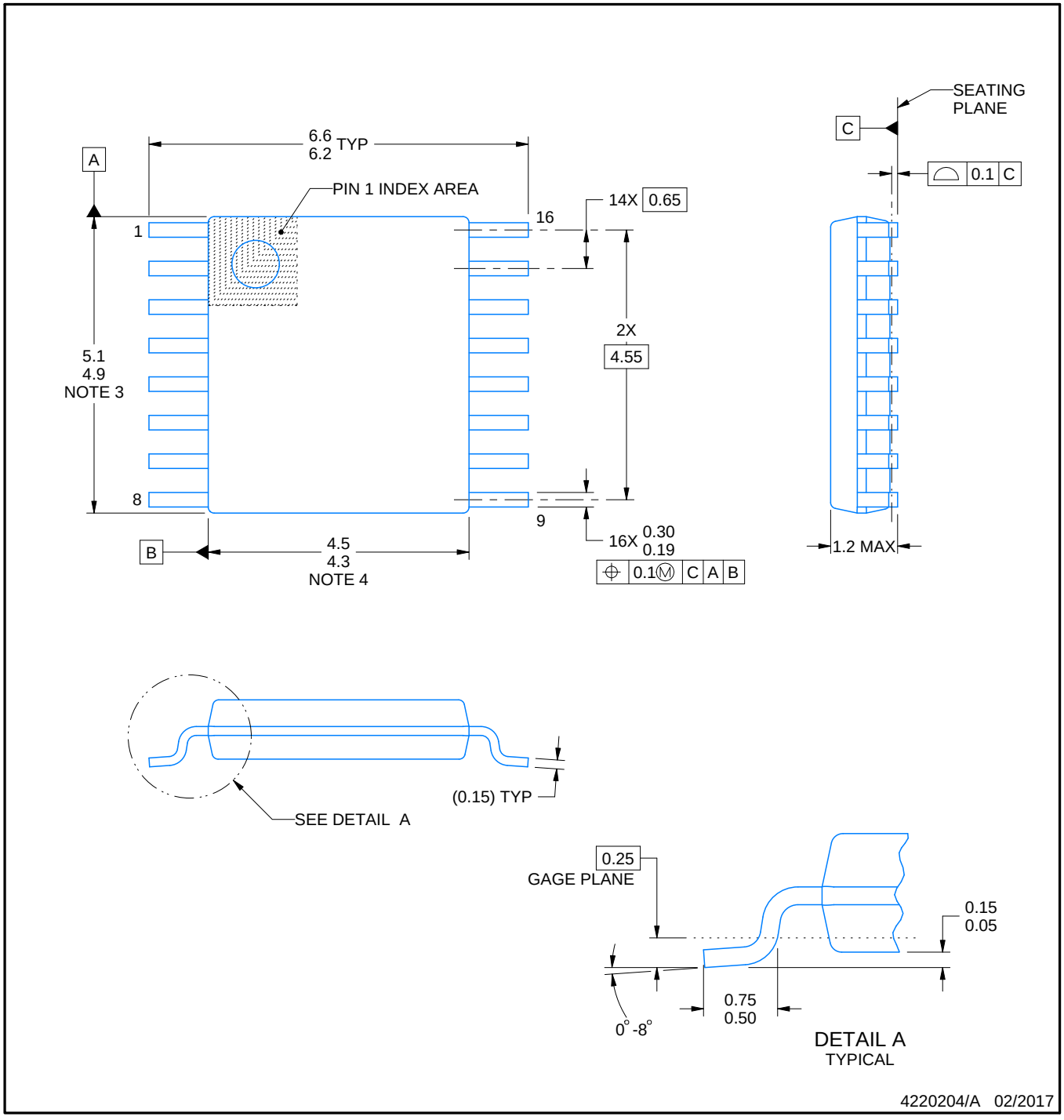
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

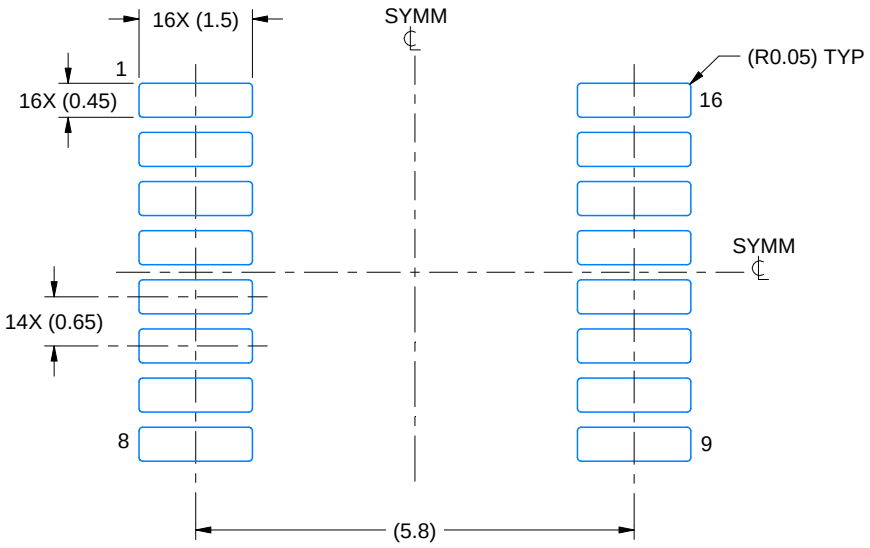
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

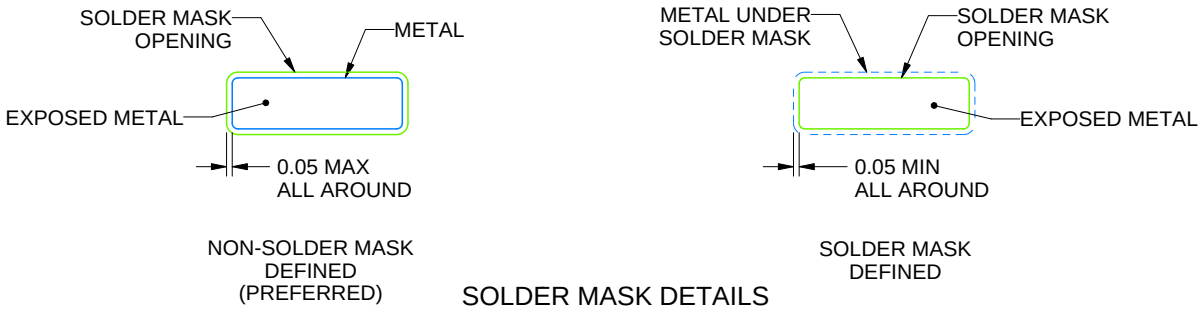


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

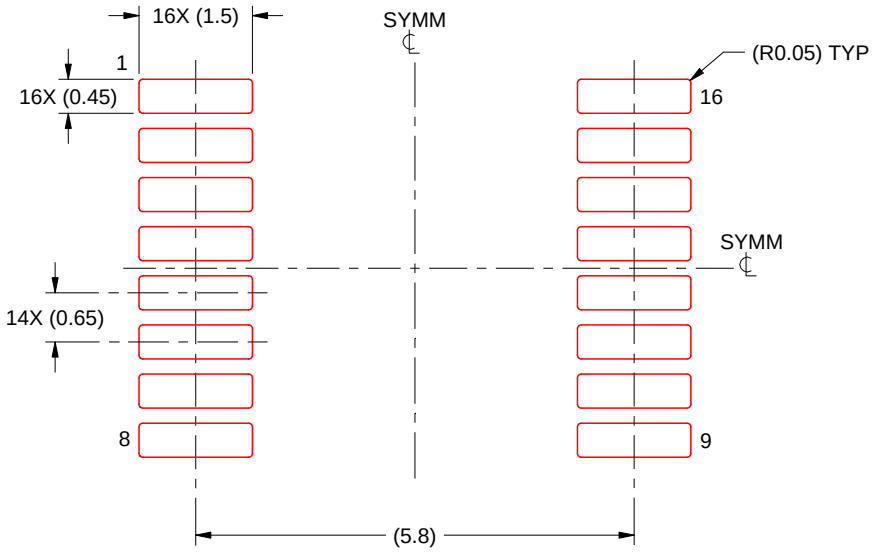


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

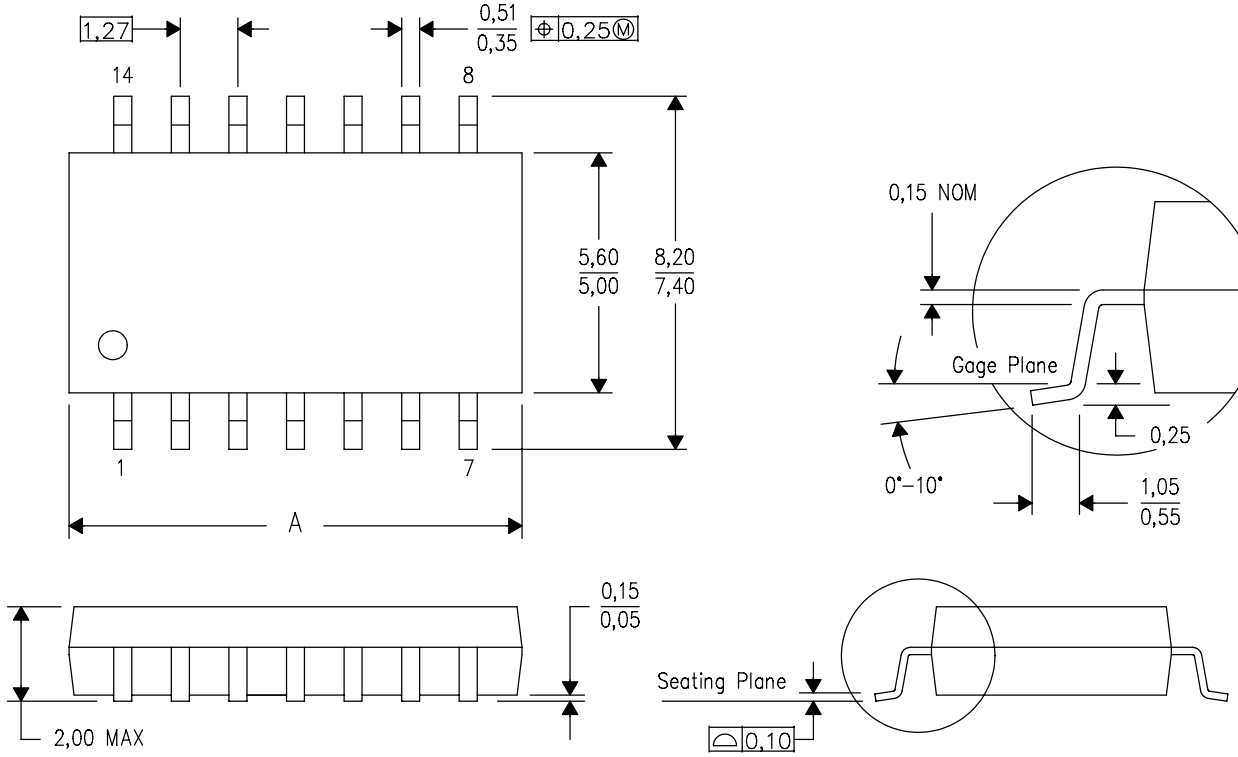
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

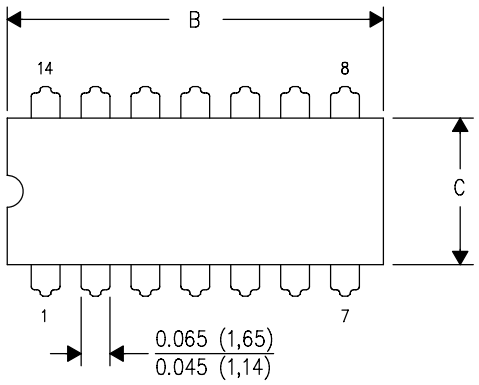
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

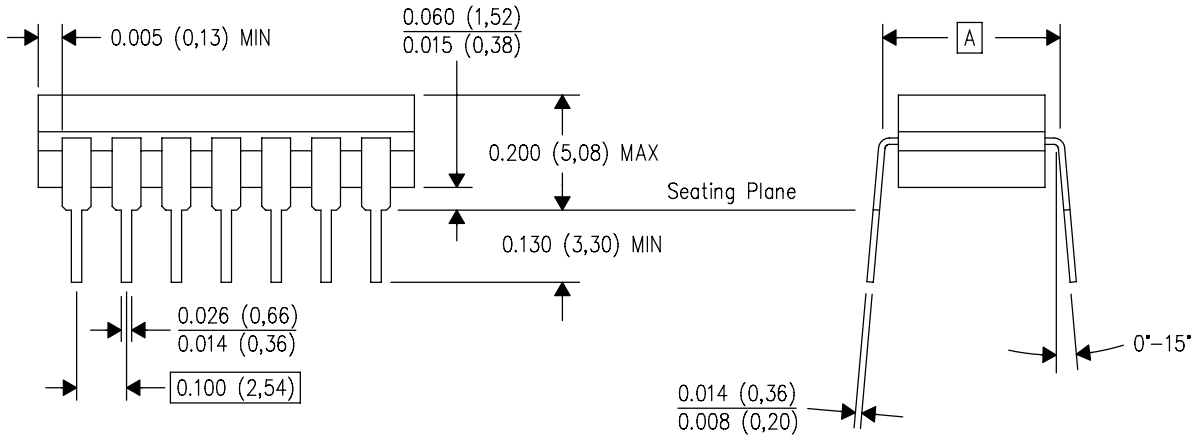
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



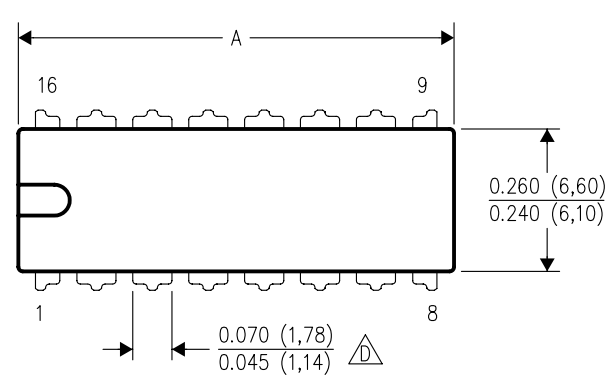
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

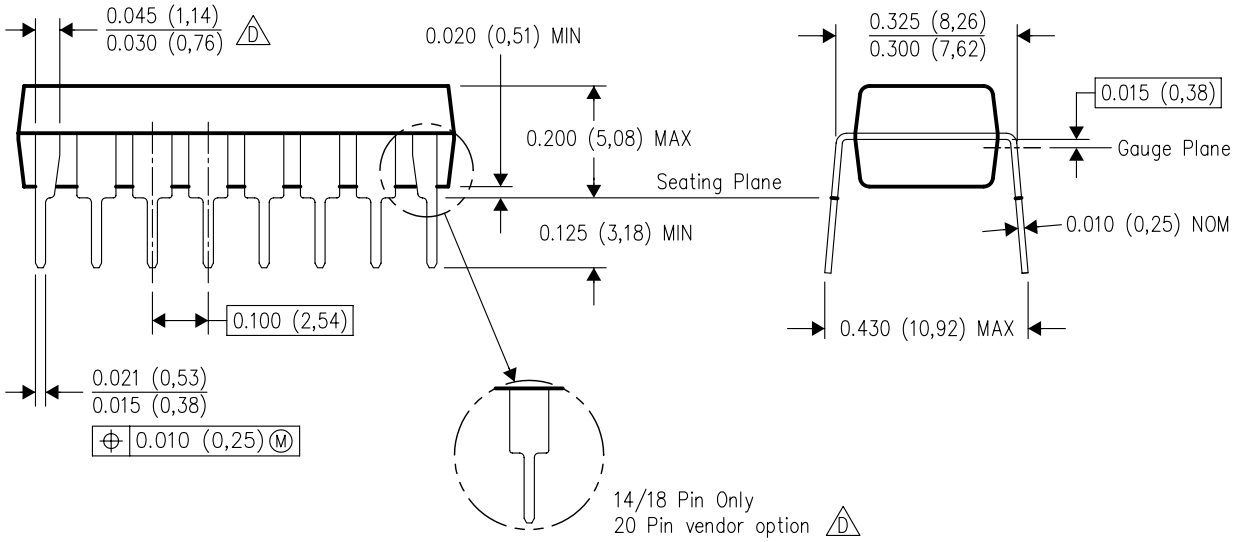
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

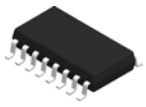


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

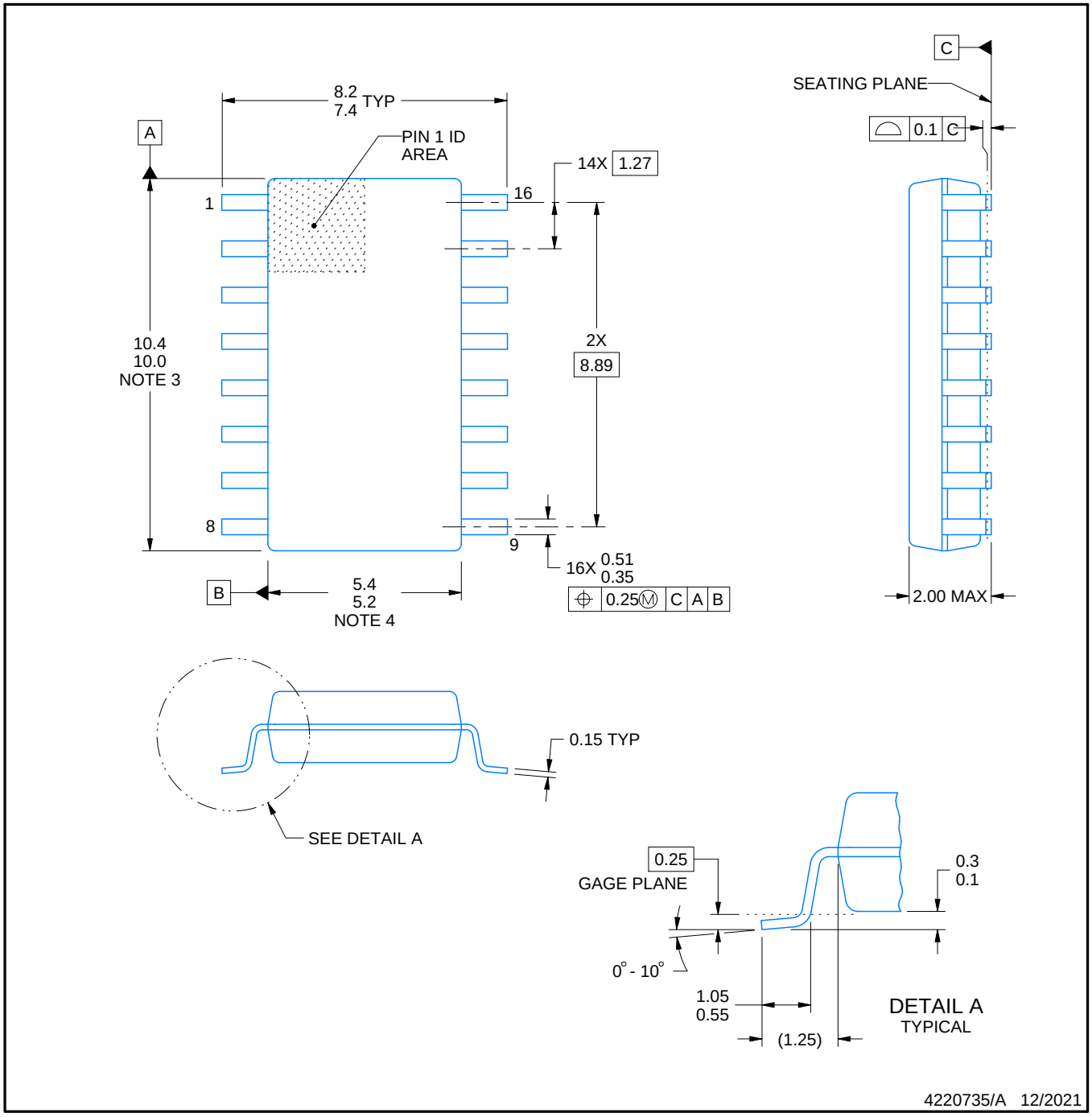


PACKAGE OUTLINE

NS0016A

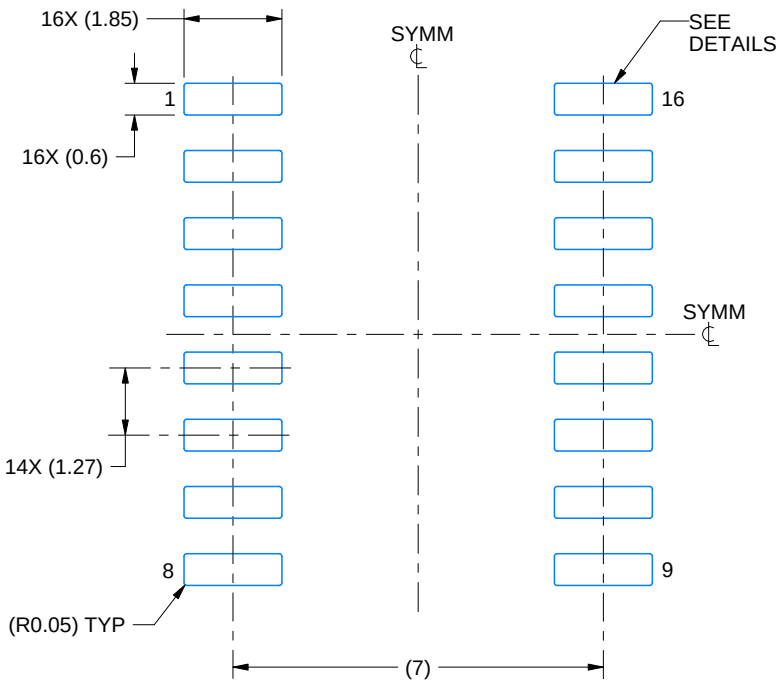
SOP - 2.00 mm max height

SOP

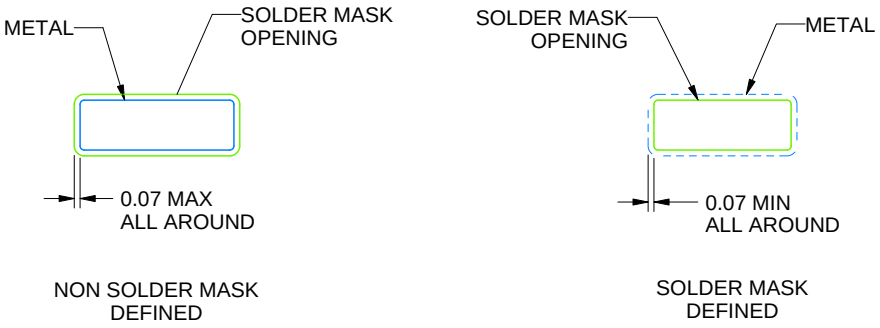


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

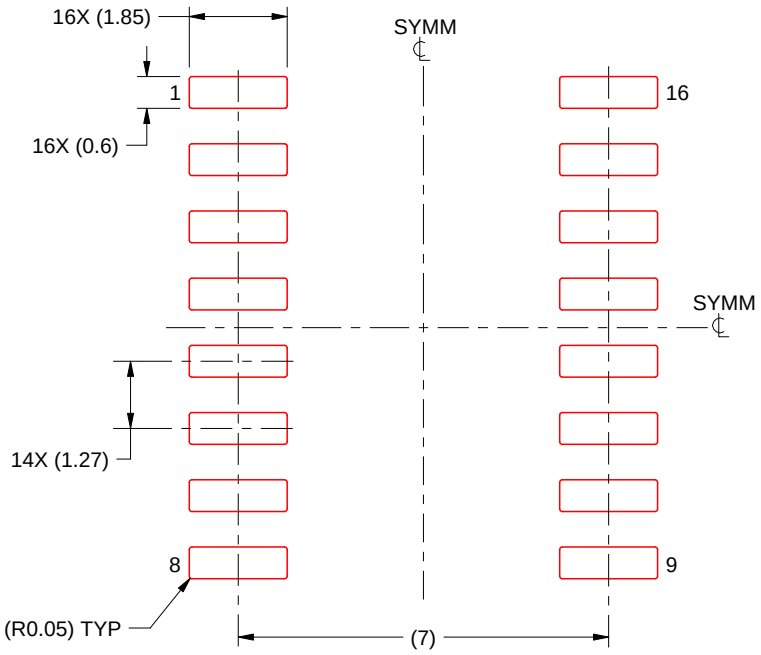
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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