

CD74HC4051-Q1 Automotive Analog Multiplexer or Demultiplexer

1 Features

- Qualified for automotive applications
- Wide analog input voltage range of $\pm 5V$ maximum
- Low ON resistance:
 - 70 Ω typical ($V_{CC} - V_{EE} = 4.5V$)
 - 40 Ω typical ($V_{CC} - V_{EE} = 9V$)
- Low crosstalk between switches
- Fast switching and propagation speeds
- Break-before-make switching
- Operation control voltage = 2V to 6V
- Switch voltage = 0V to 10V
- High noise immunity $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} , $V_{CC} = 5V$

2 Applications

- [Digital radio](#)
- Signal gating
- [Factory automation](#)
- [Televisions](#)
- [Appliances](#)
- Programmable logic circuits
- [Sensors](#)

3 Description

This device is a digitally controlled analog switch that utilizes silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

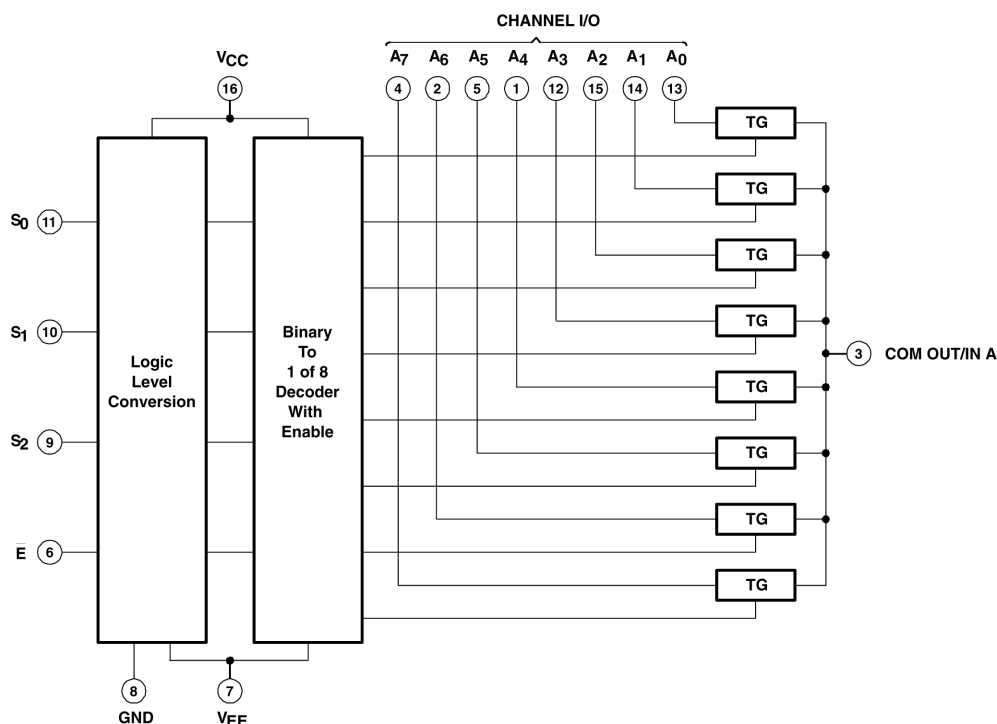
This analog multiplexer/demultiplexer controls analog voltages that may vary across the voltage supply range (for example, V_{CC} to V_{EE}). These bidirectional switches allow any analog input to be used as an output and vice versa. The switches have low ON resistance and low OFF leakages. In addition, the device has an enable control (\bar{E}) that, when high, disables all switches to their OFF state.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
CD74HC4051-Q1	PW (TSSOP, 16)	5mm × 6.4mm
	D (SOIC, 16)	9.9mm × 3.9mm

(1) For more information see, [Section 10](#)

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

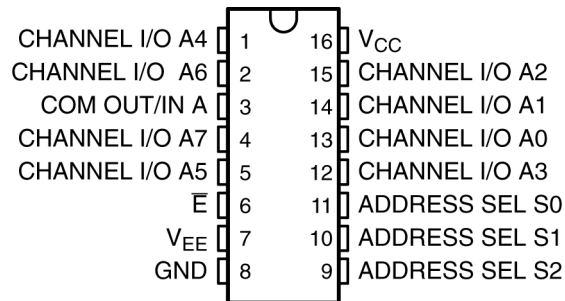


Figure 4-1. PW, D Package, 16-Pin TSSOP, SOIC (Top View)

Table 4-1. Function Table

INPUTS				ON CHANNEL(S)
E	S ₂	S ₁	S ₀	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT
$V_{CC} - V_{EE}$ (see ⁽²⁾)	Supply voltage range		-0.5	10.5	V
V_{CC}	Supply voltage range		-0.5	7	V
V_{EE}	Supply voltage range		+0.5	-7	V
I_{IK} ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$)	Input clamp current			±20	mA
I_{OK} ($V_O < V_{EE} - 0.5V$ or $V_O > V_{CC} + 0.5V$)	Output clamp current			±20	mA
($V_I > V_{EE} - 0.5V$ or $V_I < V_{CC} + 0.5V$)	Switch current			±25	mA
	Continuous current through V_{CC} or GND			±50	mA
I_{EE}	V_{EE} current			-20	mA
$R_{\theta JA}$	Package thermal impedance	D package		91.6	°C/W
		PW package		116.5	°C/W
T_J	Maximum junction temperature			150	°C
Lead temperature (during soldering):		At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max		300	°C
T_{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to GND unless otherwise specified.

5.2 Recommended Operating Conditions

(see ⁽¹⁾)

			MIN	MAX	UNIT
V_{CC}	Supply voltage (see ⁽²⁾)		2	6	V
	Supply voltage, $V_{CC} - V_{EE}$ (see Figure 5-1)		2	10	V
V_{EE}	Supply voltage, (see ⁽²⁾ and Figure 5-2)		0	-6	V
V_{IH}	High-level input voltage	$V_{CC} = 2V$	1.5		V
		$V_{CC} = 4.5V$	3.15		
		$V_{CC} = 6V$	4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2V$		0.5	V
		$V_{CC} = 4.5V$		1.35	
		$V_{CC} = 6V$		1.8	
V_I	Input control voltage		0	V_{CC}	V
V_{IS}	Analog switch I/O voltage		V_{EE}	V_{CC}	V
t_t	Input transition (rise and fall) time	$V_{CC} = 2V$	0	1000	ns
		$V_{CC} = 4.5V$	0	500	
		$V_{CC} = 6V$	0	400	
T_A	Operating free-air temperature		-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) In certain applications, the external load resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed

0.6V (calculated from r_{on} values shown in electrical characteristics table). No V_{CC} current flows through R_L if the switch current flows into the COM OUT/IN A terminal.

5.3 Recommended Operating Area as a Function of Supply Voltages

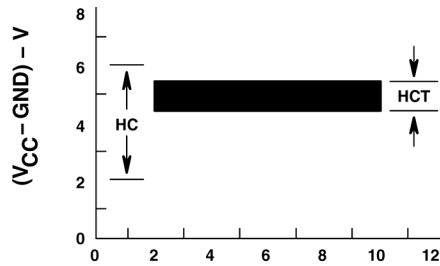


Figure 5-1. $(V_{CC} - V_{EE}) - V$

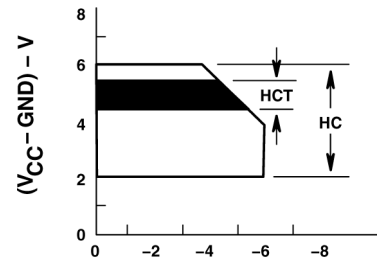


Figure 5-2. $(V_{EE} - GND) - V$

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{EE}	V_{CC}	$T_A = 25\text{ }^\circ\text{C}$			$T_A = -40\text{ }^\circ\text{C TO } 125\text{ }^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
r_{on}	$I_O = 1\text{ mA}$, $V_I = V_{IH}$ or V_{IL} . See Figure 5-3	$V_{IS} = V_{CC}$ or V_{EE}	0V	4.5V		70	160	240	Ω
			0V	6V		60	140	210	
			-4.5V	4.5V		40	120	180	
		$V_{IS} = V_{CC}$ to V_{EE}	0V	4.5V		90	180	270	
			0V	6V		80	160	240	
			-4.5V	4.5V		45	130	195	
Δr_{on}	Between any two channels	0V	4.5V		10			Ω	
		0V	6V		8.5				
		-4.5V	4.5V		5				
I_{IZ}	For switch OFF: When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$; When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$ For switch ON: All applicable combinations of V_{IS} and V_{OS} voltage levels, $V_I = V_{IH}$ or V_{IL}	0V	6V			± 0.2	± 2	μA	
		-5V	5V			± 0.4	± 4		
I_{IL}	$V_I = V_{CC}$ or GND	0V	6V			± 0.1	± 1	μA	
I_{CC}	$I_O = 0$, $V_I = V_{CC}$ or GND	When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$	0V	6V			12	160	μA
		When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$	-5V	5V			32	320	

5.5 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-5](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{EE}	V _{CC}	T _A = 25°C			T _A = -40 °C TO 125°C		UNIT	
						MIN	TYP	MAX	MIN	MAX		
t _{pd}	IN	OUT	C _L = 15pF		5V			4			ns	
			C _L = 50pF	0V	2V				60		90	ns
					4.5V				12		18	
					6V				10		15	
-4.5V	4.5V			8		12						
t _{en}	ADDRESS SEL or \bar{E}	OUT	C _L = 15pF		5V			19			ns	
			C _L = 50pF	0V	2V				325			490
					4.5V				45			68
					6V				38			57
-4.5V	4.5V			32		48						
t _{dis}	ADDRESS SEL or \bar{E}	OUT	C _L = 15pF		5V			27			ns	
			C _L = 50pF	0V	2V				250			400
					4.5V				50			68
					6V				44			57
-4.5V	4.5V			44		55						
C _I	Control		C _L = 50pF					10		10	pF	

5.6 Operating Characteristics

V_{CC} = 5V, T_A = 25°C, Input t_r, t_f = 6 ns

PARAMETER		TYP	UNIT
C _{pd}	Power dissipation capacitance (see ⁽¹⁾)	50	pF

(1) C_{pd} is used to determine the dynamic power consumption, per package.

- $P_D = C_{pd} V_{CC}^2 f_I + \Sigma (C_L + C_S) V_{CC}^2 f_O$
- f_O = output frequency
- f_I = input frequency
- C_L = output load capacitance
- C_S = switch capacitance
- V_{CC} = supply voltage

5.7 Analog Channel Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{EE}	V _{CC}	MIN	TYP	MAX	UNIT
C _I	Switch input capacitance					5		pF
C _{COM}	Common output capacitance					25		pF
f _{max}	Minimum switch frequency response at -3 dB	See Figure 6-1 and Figure 5-4 , and ⁽¹⁾ and ⁽²⁾	-2.25V	2.25V		145		MHz
			-4.5V	4.5V		180		

5.7 Analog Channel Characteristics (continued)

 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V_{EE}	V_{CC}	MIN	TYP	MAX	UNIT
THD	Sine-wave distortion	See Figure 6-2	-2.25V	2.25V	0.03	5		%
			-4.5V	4.5V	0.01	8		
O_{ISO}	Switch OFF signal feed through	See Figure 6-4 and Figure 5-5, and (2) and (3)	-2.25V	2.25V	-73			dB
			-4.5V	4.5V	-75			

- (1) Adjust input voltage to obtain 0 dBm at V_{OS} for $f_{IN} = 1\text{MHz}$.
- (2) V_{IS} is centered at $(V_{CC} - V_{EE})/2$.
- (3) Adjust input for 0 dBm.

5.8 Typical Characteristics

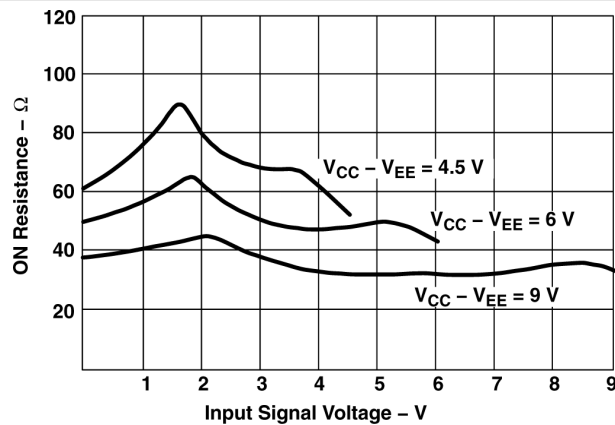


Figure 5-3. Typical on Resistance vs Input Signal Voltage

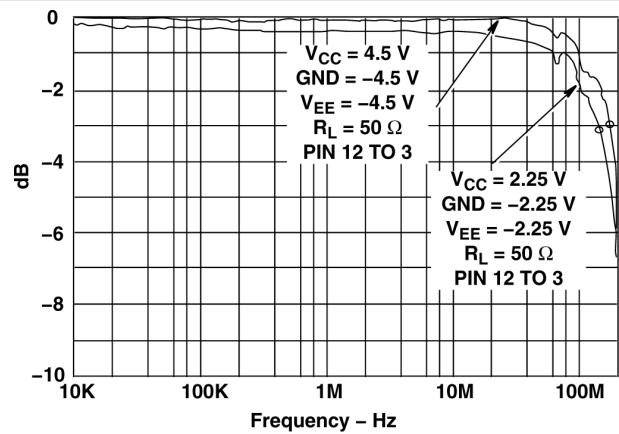


Figure 5-4. Channel on Bandwidth

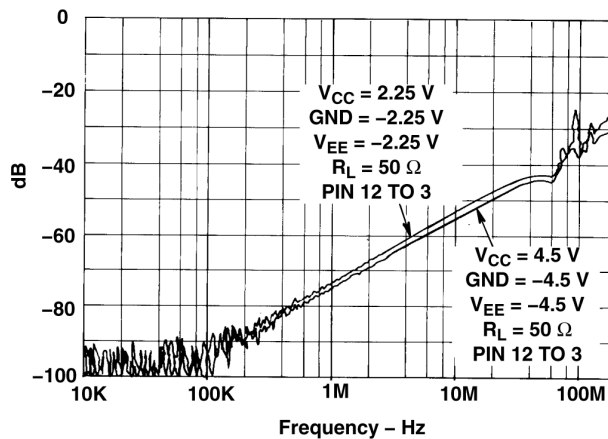


Figure 5-5. Channel off Feed-through

6 Parameter Measurement Information

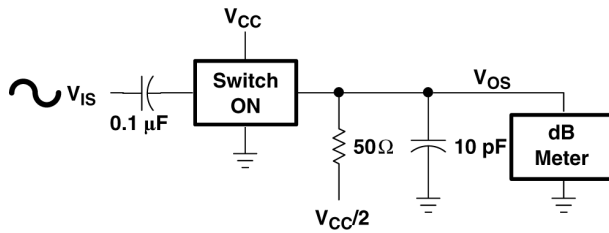
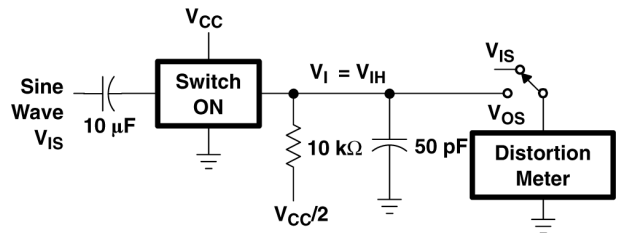


Figure 6-1. Frequency-Response Test Circuit



$f_{IS} = 1 \text{ kHz to } 10 \text{ kHz}$

Figure 6-2. Sine-Wave Distortion Test Circuit

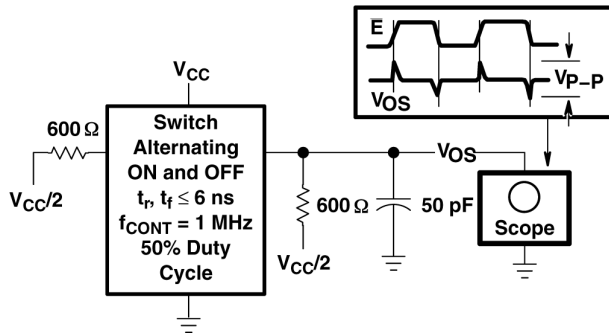


Figure 6-3. Control to Switch Feed-through Noise Test Circuit

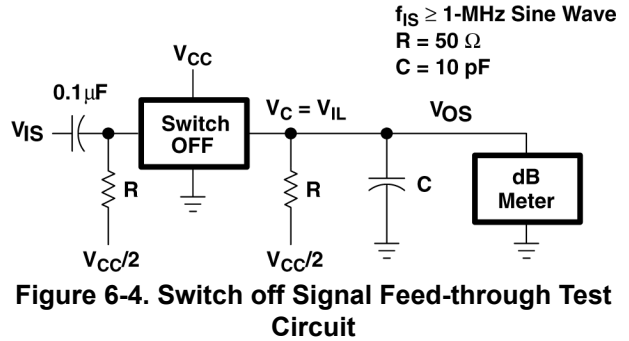
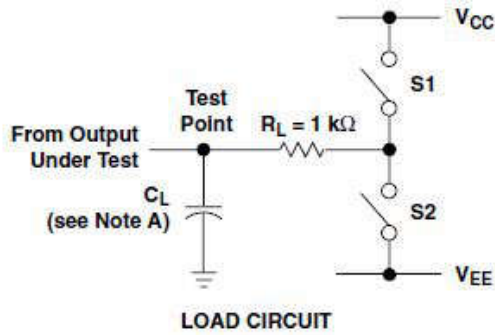
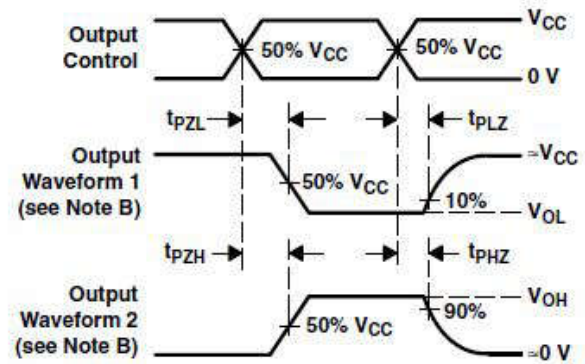
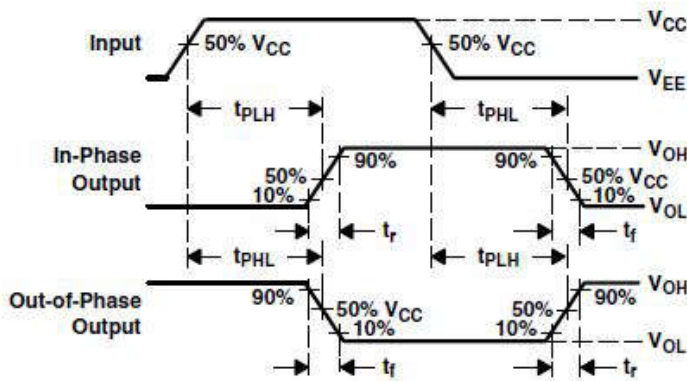


Figure 6-4. Switch off Signal Feed-through Test Circuit



PARAMETER	S1	S2	
t_{en}	t_{pZH}	Open	Closed
	t_{pZL}	Closed	Open
t_{dis}	t_{pHZ}	Open	Closed
	t_{pLZ}	Closed	Open
t_{pd}	Open	Open	



- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_r = 6\text{ns}$, $t_f = 6\text{ns}$.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. t_{pLZ} and t_{pHZ} are the same as t_{dis} .
- G. t_{pZL} and t_{pZH} are the same as t_{en} .
- H. t_{pLH} and t_{pHL} are the same as t_{pd} .

Figure 6-5. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

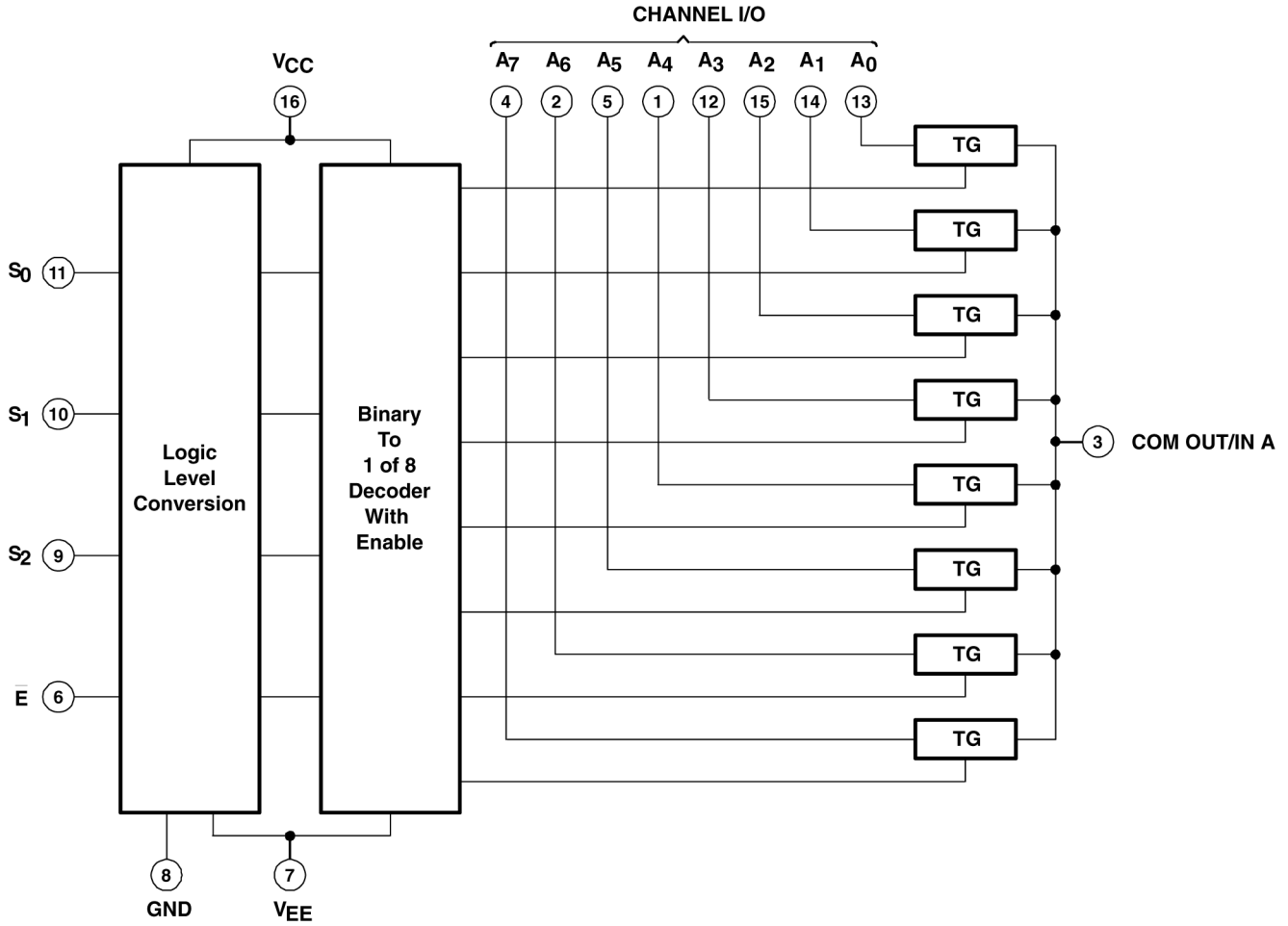


Figure 7-1. Logic Diagram (Positive Logic)

7.2 Device Functional Modes

Table 7-1. Function Table

INPUTS				ON CHANNEL(S)
\bar{E}	S_2	S_1	S_0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2008) to Revision B (April 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed M (SOIC, 16) to D (SOIC, 16) to accurately reflect the package drawing.....	1
• Changed the package thermal impedance for the D package from: 73°C/W to: 91.6°C/W	3
• Changed the package thermal impedance for the PW package from: 108°C/W to: 116.5°C/W	3
• Changed I _{CC} MAX from: 8μA to: 12μA when V _{IS} = V _{EE} , V _{OS} = V _{CC} at a TA = 25°C	4
• Changed I _{CC} MAX from: 16μA to: 32μA when V _{IS} = V _{CC} , V _{OS} = V _{EE} at a TA = 25°C	4
• Changed t _{en} MAX from: 225ns to: 325ns when C _L = 50pF at a TA = 25°C and from: 340ns to: 490ns when C _L = 50pF at a TA = -40°C to 125°C.....	5
• Changed t _{dis} TYP from: 19ns to: 27ns when C _L = 15pF at a TA = 25°C.....	5
• Changed t _{dis} MAX from: 225ns to: 250ns when C _L = 50pF, V _{EE} = 0V, and V _{CC} = 2V at a TA = 25°C, and from: 340ns to: 400ns at a TA = -40°C to 125°C.....	5
• Changed t _{dis} MAX from: 45ns to: 50ns when C _L = 50pF, V _{EE} = 0V, and V _{CC} = 4.5V at a TA = 25°C.....	5
• Changed t _{dis} MAX from: 38ns to: 44ns when C _L = 50pF, V _{EE} = 0V, and V _{CC} = 6V at a TA = 25°C.....	5
• Changed t _{dis} MAX from: 32ns to: 44ns when C _L = 50pF, V _{EE} = -4.5V, and V _{CC} = 4.5V at a TA = 25°C, and from: 48ns to: 55ns at a TA = -40°C to 125°C.....	5
• Removed the TBD \bar{E} or ADDRESS SEL to switch feed-through noise parameter.....	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4051QM96G4Q1	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125	HC4051Q	
CD74HC4051QM96Q1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4051Q	Samples
CD74HC4051QPWRG4Q1	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 125	HJ4051Q	
CD74HC4051QPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HJ4051Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD74HC4051-Q1 :

- Catalog : [CD74HC4051](#)
- Enhanced Product : [CD74HC4051-EP](#)
- Military : [CD54HC4051](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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