TEXAS INSTRUMENTS

# CD54HC174, CD74HC174, CD54HCT174, CD74HCT174

Data sheet acquired from Harris Semiconductor
SCHS159C

August 1997 - Revised October 2003

## High-Speed CMOS Logic Hex D-Type Flip-Flop with Reset

### Features

- **Buffered Positive Edge Triggered Clock**
- **Asynchronous Common Reset**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . . . . . . . . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . . . . . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55$^{o}$C to 125$^{o}$C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$**

### Description

The ’HC174 and ’HCT174 are edge triggered flip-flops which utilize silicon gate CMOS circuitry to implement D-type flip-flops. They possess low power and speeds comparable to low power Schottky TTL circuits. The devices contain six master-slave flip-flops with a common clock and common reset. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The $\overline{MR}$ input, when low, sets all outputs to a low state.

Each output can drive ten low power Schottky TTL equivalent loads. The ’HCT174 is functional as well as, pin compatible to the ’LS174.

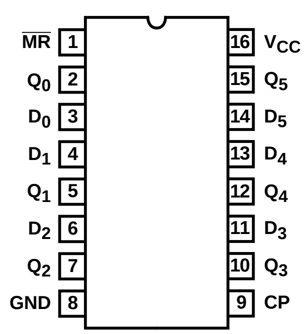
### Ordering Information

| PART NUMBER | TEMP. RANGE ($^{o}$C) | PACKAGE |
|---|---|---|
| CD54HC174F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT174F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC174E | -55 to 125 | 16 Ld PDIP |
| CD74HC174M | -55 to 125 | 16 Ld SOIC |
| CD74HC174MT | -55 to 125 | 16 Ld SOIC |
| CD74HC174M96 | -55 to 125 | 16 Ld SOIC |
| CD74HCT174E | -55 to 125 | 16 Ld PDIP |
| CD74HCT174M | -55 to 125 | 16 Ld SOIC |
| CD74HCT174MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT174M96 | -55 to 125 | 16 Ld SOIC |

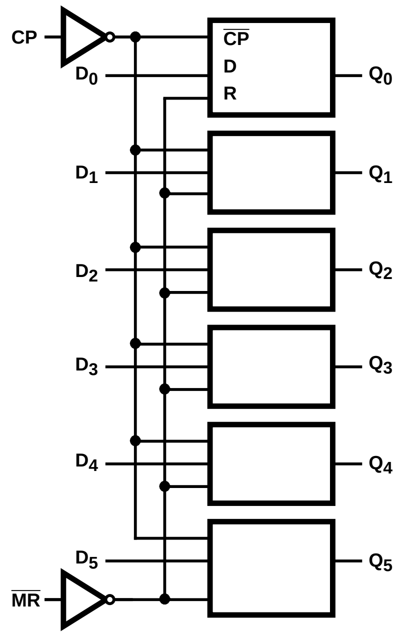
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout

**CD54HC174, CD54HCT174**
**(CERDIP)**
**CD74HC174, CD74HCT174**
**(PDIP, SOIC)**
TOP VIEW



## Functional Diagram

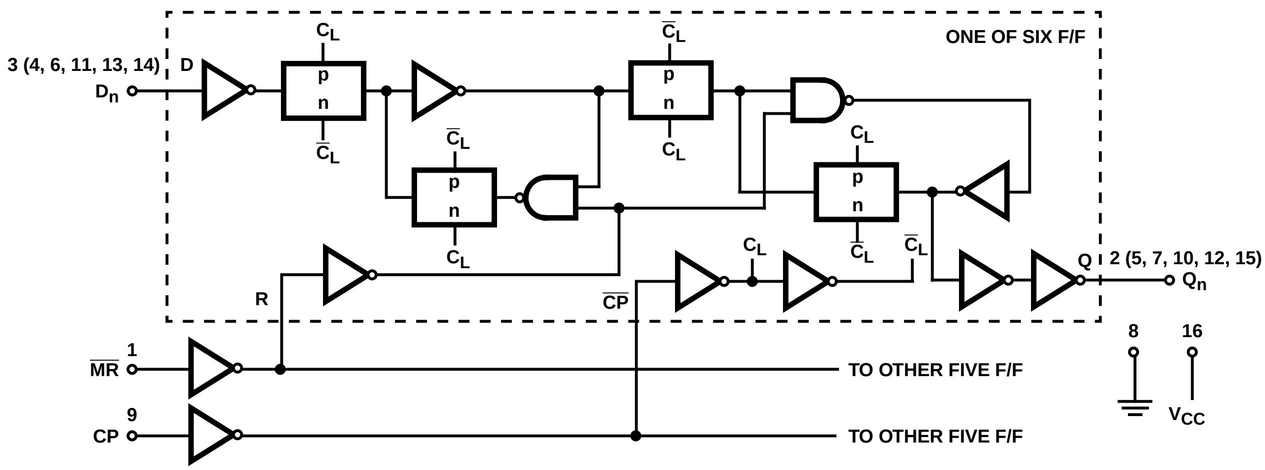



**TRUTH TABLE**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| RESET ($\overline{MR}$) | CLOCK CP | DATA $D_n$ | $Q_n$ |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | $Q_0$ |

H = High Voltage Level, L = Low Voltage Level, X = Irrelevant, ↑ = Transition from Low to High Level, $Q_0$ = Level Before the Indicated Steady-State Input Conditions Were Established

## Logic Diagram



## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . . . . . . . . . . . . . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . . . . . . . . . . . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . . . . . . . . . . . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ . . . . . . . . . . . . . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . . . . . . . . . . . . . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 2V to 6V
HCT Types . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . . . . . . . . . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1000ns (Max)
4.5V . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 500ns (Max)
6V . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 400ns (Max)

## Thermal Information

Thermal Resistance (Typical, Note 1) $\theta_{JA}$ (°C/W)
E (PDIP) Package . . . . . . . . . . . . . . . . . . . . . . . . . . 67
M (SOIC) Package . . . . . . . . . . . . . . . . . . . . . . . . . . 73
Maximum Junction Temperature . . . . . . . . . . . . . . . . . . . . . . . 150°C
Maximum Storage Temperature Range . . . . . . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . . . . . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO +85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO +85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ to GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 2) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE:

2. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

## HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| CP | 0.80 |
| $\overline{MR}$ | 0.55 |
| D | 0.15 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

## Prerequisite For Switching Function

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | |
| Clock Pulse Width | $t_W$ | - | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | 17 | - | 20 | - | ns |
| $\overline{MR}$ Pulse Width | $t_W$ | - | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | 17 | - | 20 | - | ns |

## Prerequisite For Switching Function (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C MIN | 25°C MAX | -40°C TO 85°C MIN | -40°C TO 85°C MAX | -55°C TO 125°C MIN | -55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| Setup Time, Data to Clock | $t_{SU}$ | - | 2 | 60 | - | 75 | - | 90 | - | ns |
| | | | 4.5 | 12 | - | 15 | - | 18 | - | ns |
| | | | 6 | 10 | - | 13 | - | 15 | - | ns |
| Hold Time, Data to Clock | $t_H$ | - | 2 | 5 | - | 5 | - | 5 | - | ns |
| | | | 4.5 | 5 | - | 5 | - | 5 | - | ns |
| | | | 6 | 5 | - | 5 | - | 5 | - | ns |
| Removal Time, $\overline{MR}$ to Clock | $t_{REM}$ | - | 2 | 5 | - | 5 | - | 5 | - | ns |
| | | | 4.5 | 5 | - | 5 | - | 5 | - | ns |
| | | | 6 | 5 | - | 5 | - | 5 | - | ns |
| Clock Frequency | $f_{MAX}$ | - | 2 | 6 | - | 5 | - | 4 | - | MHz |
| | | | 4.5 | 30 | - | 24 | - | 20 | - | MHz |
| | | | 6 | 35 | - | 28 | - | 24 | - | MHz |
| **HCT TYPES** | | | | | | | | | | |
| Clock Pulse Width | $t_W$ | - | 4.5 | 20 | - | 25 | - | 30 | - | ns |
| $\overline{MR}$ Pulse Width | $t_W$ | - | 6 | 25 | - | 31 | - | 38 | - | ns |
| Setup Time, Data to Clock | $t_{SU}$ | - | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| Hold Time, Data to Clock | $t_H$ | - | 6 | 5 | - | 5 | - | 5 | - | ns |
| Removal Time, $\overline{MR}$ to Clock | $t_{REM}$ | - | 4.5 | 12 | - | 15 | - | 18 | - | ns |
| Clock Frequency | $f_{MAX}$ | - | 6 | 25 | - | 20 | - | 17 | - | MHz |

## Switching Specifications Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C TYP | 25°C MAX | -40°C TO 85°C MAX | -55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **HC TYPES** | | | | | | | | |
| Propagation Delay, Clock to Q | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 165 | 205 | 250 | ns |
| | | | 4.5 | - | 33 | 41 | 50 | ns |
| | | | 6 | - | 28 | 35 | 43 | ns |
| | | $C_L$ = 15pF | 5 | 13 | - | - | - | ns |
| Propagation Delay, $\overline{MR}$ to Q | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | | 6 | - | 26 | 33 | 38 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| Output Transition Times | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | 75 | 95 | 110 | ns |
| | | | 4.5 | - | 15 | 19 | 22 | ns |
| | | | 6 | - | 13 | 16 | 19 | ns |
| Input Capacitance | $C_{IN}$ | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | - | 5 | 38 | - | - | - | pF |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C TYP | 25°C MAX | -40°C TO 85°C MAX | -55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **HCT TYPES** | | | | | | | | |
| Propagation Delay, Clock to Q | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 40 | 50 | 60 | ns |
| | | $C_L$ = 15pF | 5 | 17 | - | - | - | ns |
| Propagation Delay, $\overline{MR}$ to Q | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | 44 | 55 | 66 | ns |
| | | $C_L$ = 15pF | 5 | 18 | - | - | - | ns |
| Output Transition Times | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | 15 | 19 | 22 | ns |
| Input Capacitance | $C_{IN}$ | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$ | - | 5 | 44 | - | - | - | pF |

NOTES:

3. $C_{PD}$ is used to determine the dynamic power consumption, per flip-flop.
4. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_O)$ where $f_i$ = Input Frequency, $f_O$ = Input Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## *Test Circuits and Waveforms*

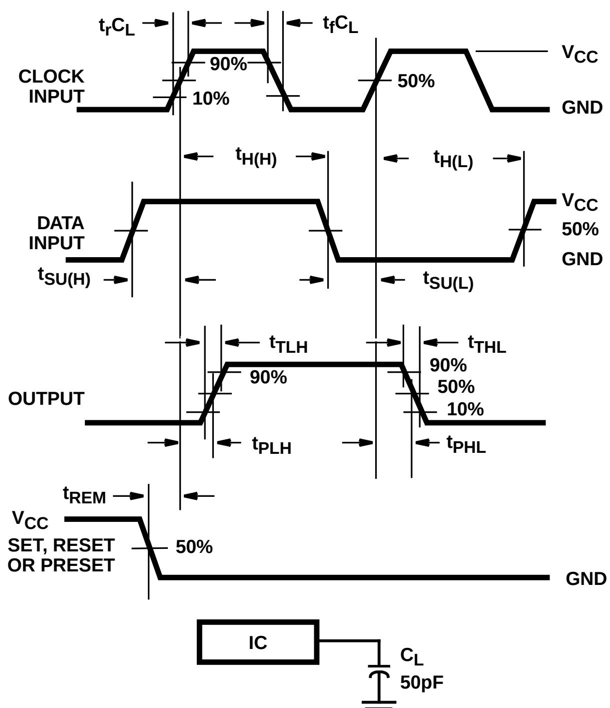



FIGURE 1. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

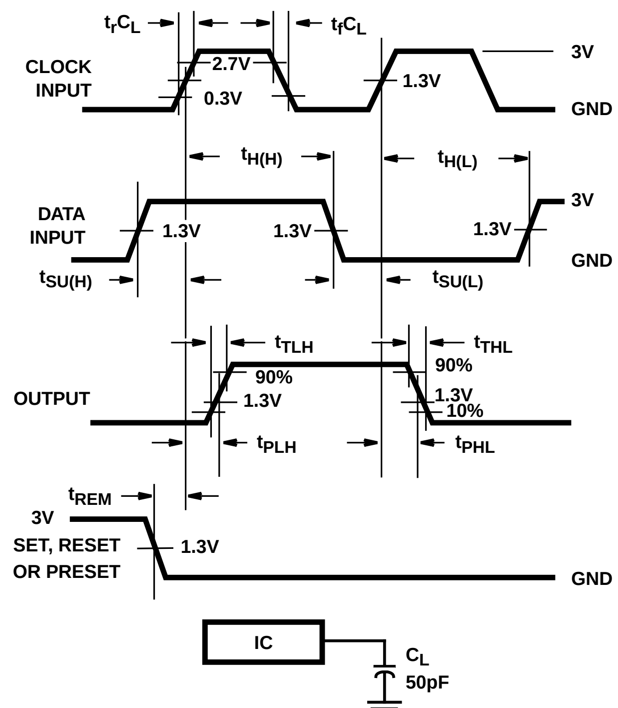



FIGURE 2. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8974301EA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8974301EA CD54HCT174F3A | Samples |
| CD54HC174F | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54HC174F | Samples |
| CD54HC174F3A | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 8407301EA CD54HC174F3A | Samples |
| CD54HCT174F | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54HCT174F | Samples |
| CD54HCT174F3A | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8974301EA CD54HCT174F3A | Samples |
| CD74HC174E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC174E | Samples |
| CD74HC174M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC174M | Samples |
| CD74HC174M96E4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC174M | Samples |
| CD74HCT174E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT174E | Samples |
| CD74HCT174M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT174M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



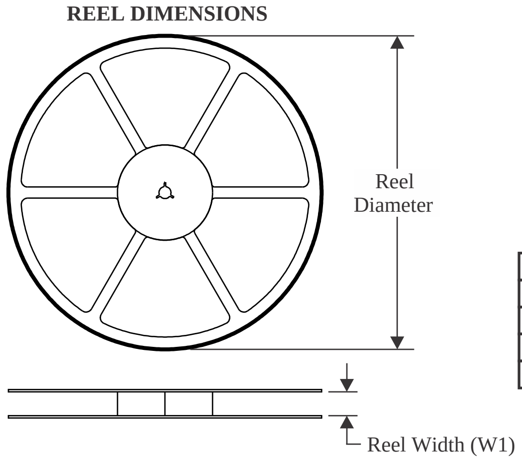
**OTHER QUALIFIED VERSIONS OF CD54HC174, CD54HCT174, CD74HC174, CD74HCT174 :**

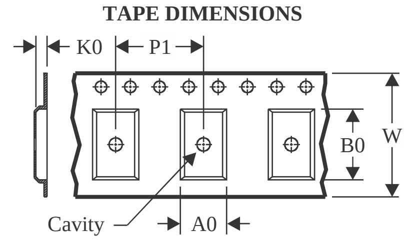
- Catalog : CD74HC174, CD74HCT174
- Military : CD54HC174, CD54HCT174

NOTE: Qualified Version Definitions:

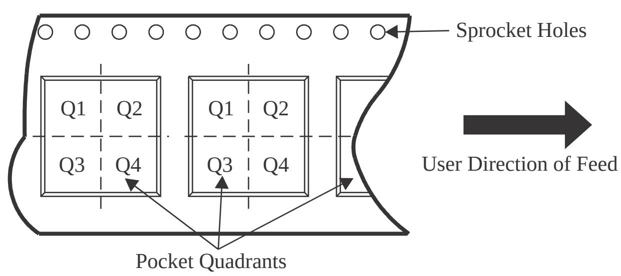
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



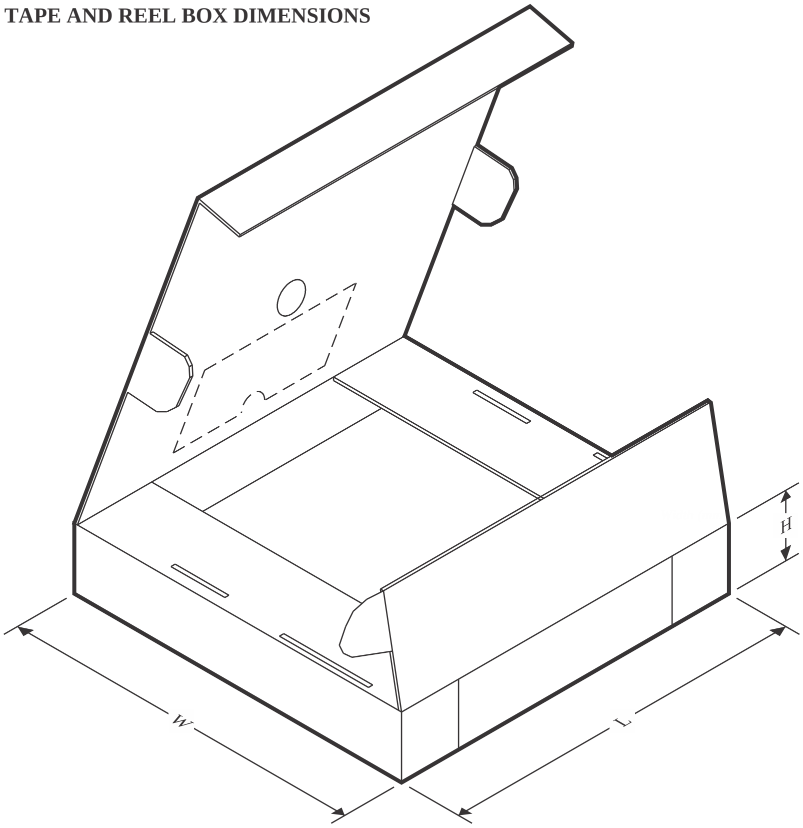

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC174M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT174M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

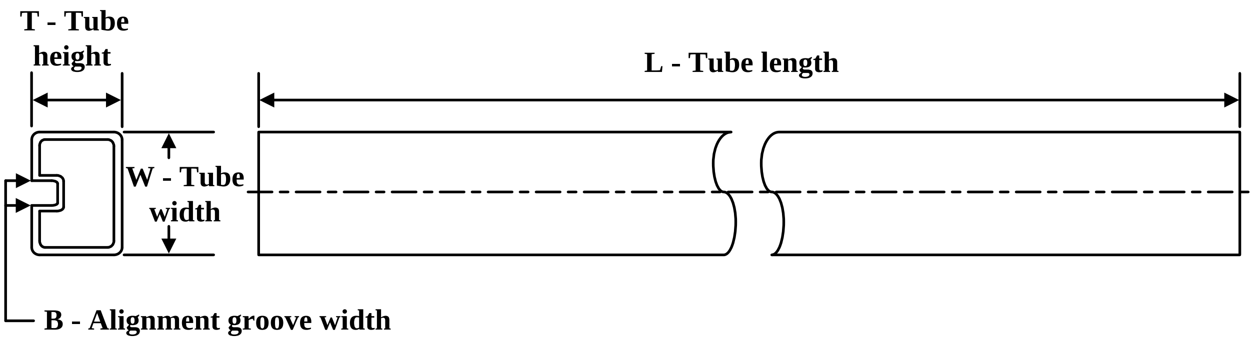
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC174M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| CD74HCT174M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |

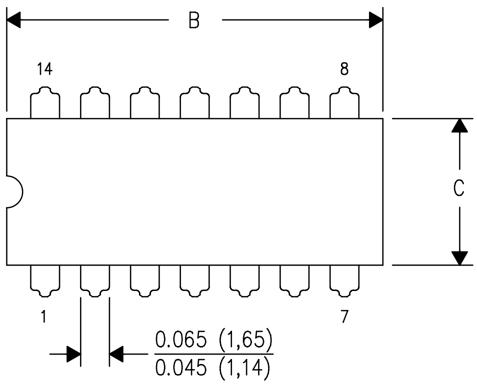
## TUBE



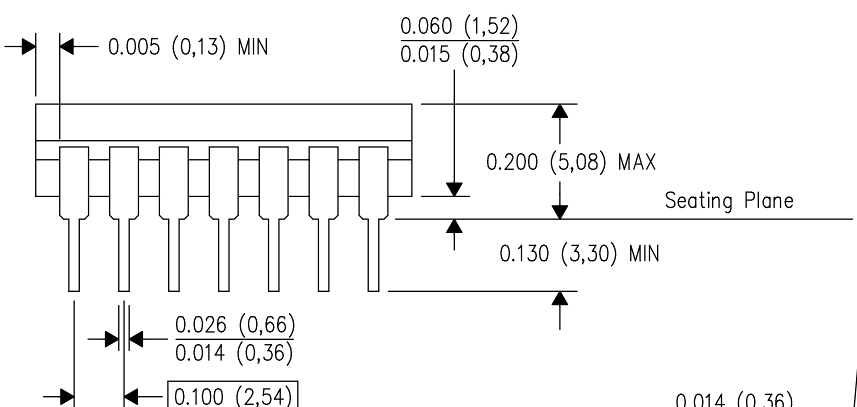

*All dimensions are nominal

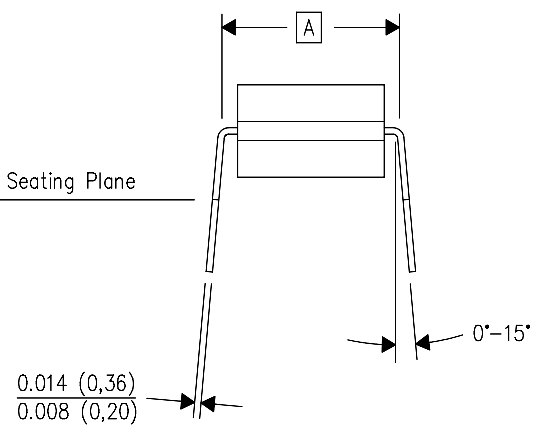
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74HC174E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC174E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT174E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT174E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

14 LEADS SHOWN




| PINS ** / DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



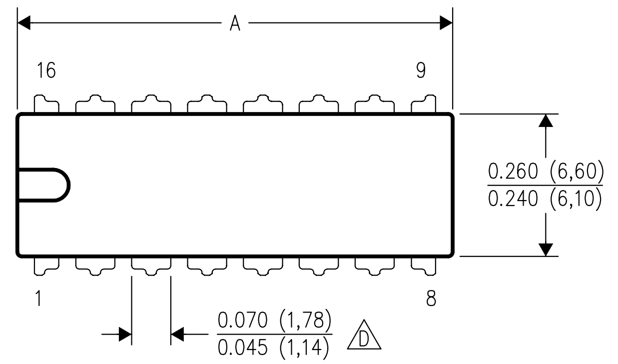




4040083/F 03/03

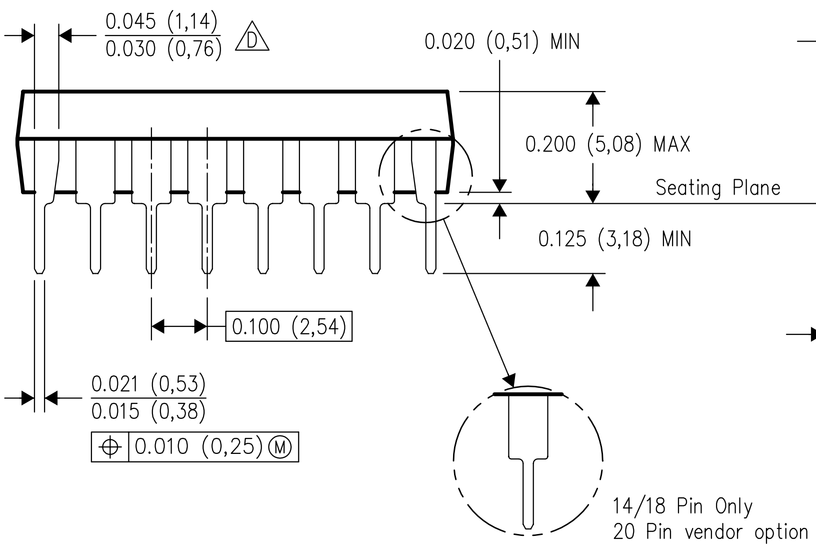
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

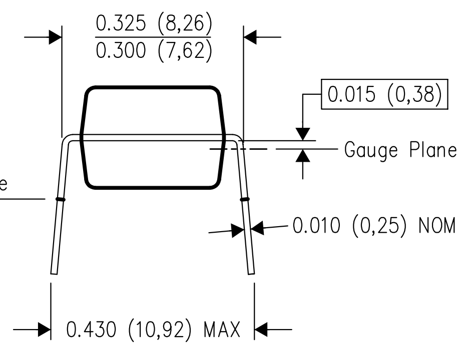
# N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| PINS ** / DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| C MS–001 VARIATION | AA | BB | AC | AD |

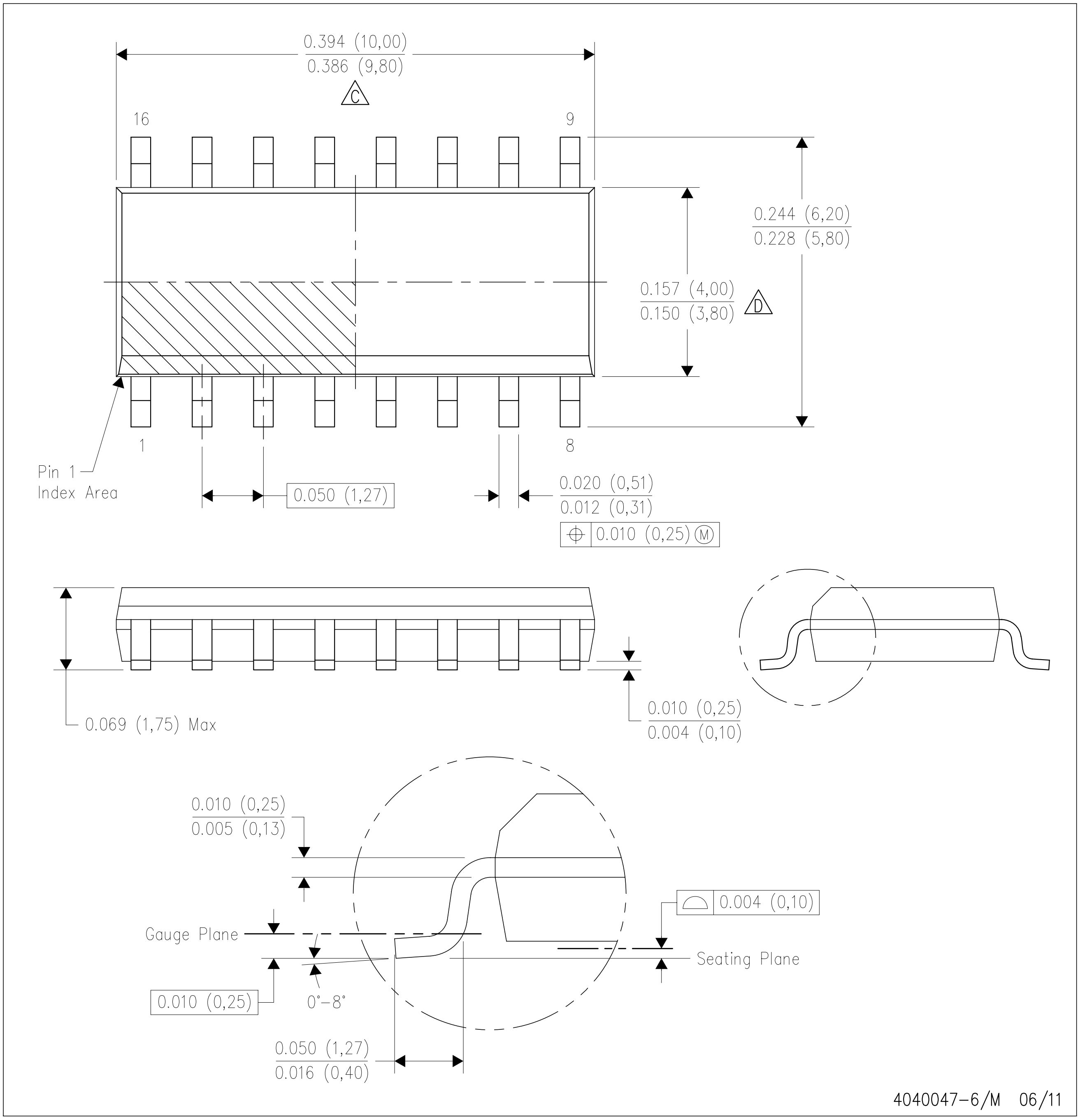



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

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