CDCM6208V2G 2:8 Clock Generator, Jitter Cleaner with Fractional Dividers

1 Features

- Superior Performance with Low Power:
  - Low Noise Synthesizer (265 fs-rms Typical Jitter) or Low Noise Jitter Cleaner (1.6 ps-rms Typical Jitter)
  - 0.5 W Typical Power Consumption
  - High Channel-to-Channel Isolation and Excellent PSRR
  - Device Performance Customizable Through Flexible 1.8 V, 2.5 V and 3.3 V Power Supplies, Allowing Mixed Output Voltages
- Flexible Frequency Planning:
  - 4x Integer Down-divided Differential Clock Outputs Supporting LVPECL-like, CML, or LVDS-like Signaling
  - 4x Fractional or Integer Divided Differential Clock Outputs Supporting HCSL, LVDS-like Signaling, or Eight CMOS Outputs
  - Fractional Output Divider Achieve 0 ppm to < 1 ppm Frequency Error and Eliminates need for Crystal Oscillators and Other Clock Generators
  - Output frequencies up to 800 MHz
- Two Differential Inputs, XTAL Support, Ability for Smart Switching
- SPI, I^{2}C™, and Pin Programmable
- Professional user GUI for Quick Design Turnaround
- 7 x 7 mm 48-QFN package (RGZ)
- -40 °C to 85 °C temperature range

2 Applications

- Base Band Clocking (Wireless Infrastructure)
- Networking and Data Communications
- Keystone C66x Multicore DSP Clocking
- Storage Server, Portable Test Equipment,
- Medical Imaging, High End A/V

3 Description

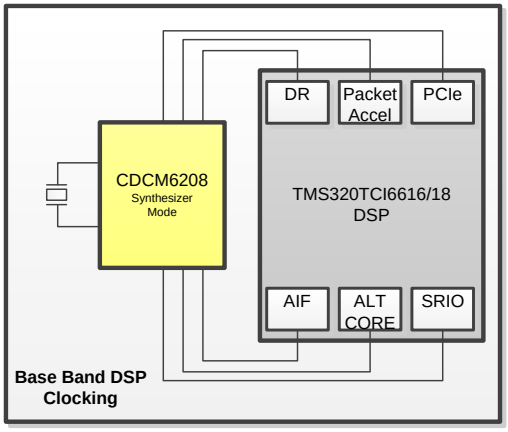
The CDCM6208V2G is a highly versatile, low jitter, low-power frequency synthesizer that can generate eight low jitter clock outputs, selectable between LVPECL-like high-swing CML, normal-swing CML, LVDS-like low-power CML, HCSL, or LVCMOS, from one of two inputs that can feature a low frequency crystal or CML, LVPECL, LVDS, or LVCMOS signals for a variety of wireless infrastructure baseband, wireline data communication, computing, low power medical imaging and portable test and measurement applications. The CDCM6208V2G also features an ***innovative*** fractional divider architecture for four of its outputs that can generate any frequency with better than 1ppm frequency accuracy. The CDCM6208V2G can be easily configured through I^{2}C or SPI programming interface and in the absence of serial interface, pin mode is also available that can set the device in 1 of 32 distinct pre-programmed configurations using control pins.

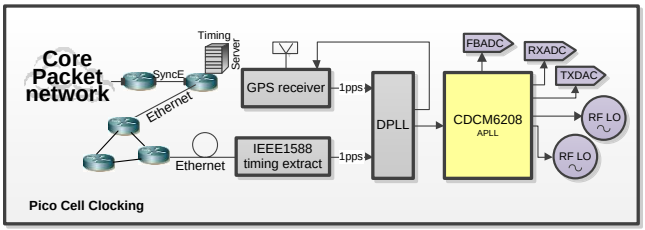
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCM6208V2G	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematics





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5 Revision History

DATE	REVISION	NOTES
March 2016	*	Initial release.

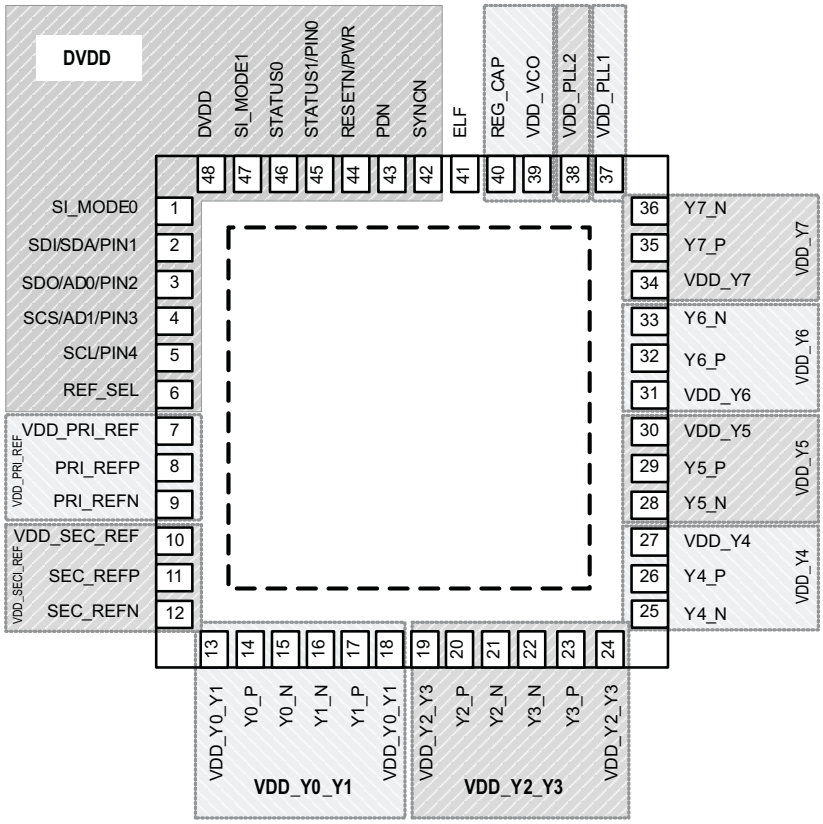
6 Description (continued)

In ***synthesizer mode***, the overall output jitter performance is less than 0.5 ps-rms (10 k - 20 MHz) or 20 ps-pp (unbound) on output using integer dividers and is between 50 to 220 ps-pp (10 k - 40 MHz) on outputs using fractional dividers depending on the prescaler output frequency.

In ***jitter cleaner mode***, the overall output jitter is less than 2.1 ps-rms (10 k - 20 MHz) or 40 ps-pp on output using integer dividers and is less than 70 ps to 240 ps-pp on outputs using fractional dividers. The CDCM6208V2G is packaged in a small 48-pin 7 mm x 7 mm QFN package.

7 Pin Configuration and Functions

RGZ Package
48 Pin VQFN
Top View



Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
PRI_REFP	8	Input	Universal	Primary Reference Input +
PRI_REFN	9	Input	Universal	Primary Reference Input –
VDD_PRI_REF	7	PWR	Analog	Supply pin for reference inputs to set between 1.8 V, 2.5 V, or 3.3 V or connect to VDD_SEC_REF.
SEC_REFP	11	Input	Universal	Secondary Reference Input +
SEC_REFN	12	Input	Universal	Secondary Reference Input –
VDD_SEC_REF	10	PWR	Analog	Supply pin for reference inputs to set between 1.8 V, 2.5 V, or 3.3 V or connect to VDD_PRI_REF(1).

(1) If Secondary input buffer is disabled (Register 4 Bit 5 = 0), it is possible to connect VDD_SEC_REF to GND.

Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
REF_SEL	6	Input	LVCMOS 50kΩ pull-up	Manual Reference Selection MUX for PLL. In SPI or I^{2}C mode the reference selection is also controlled through Register 4 bit 12. REF_SEL = 0 (≤ V_{IL}): selects PRI_REF REF_SEL = 1 (≥ V_{IH}): selects SEC_REF (when Reg 4.12 = 1). See Table 35 for detail.
ELF	41	Output	Analog	External loop filter pin for PLL
Y0_P	14	Output	Universal	Output 0 Positive Terminal
Y0_N	15	Output	Universal	Output 0 Negative Terminal
Y1_P	17	Output	Universal	Output 1 Positive Terminal
Y1_N	16	Output	Universal	Output 1 Negative Terminal
VDD_Y0_Y1 (2 pins)	13, 18	PWR	Analog	Supply pin for outputs 0, 1 to set between 1.8 V, 2.5 V or 3.3 V
Y2_P	20	Output	Universal	Output 2 Positive Terminal
Y2_N	21	Output	Universal	Output 2 Negative Terminal
Y3_P	23	Output	Universal	Output 3 Positive Terminal
Y3_N	22	Output	Universal	Output 3 Negative Terminal
VDD_Y2_Y3 (2 pins)	19, 24	PWR	Analog	Supply pin for outputs 2, 3 to set between 1.8 V, 2.5 V or 3.3 V
Y4_P	26	Output	Universal	Output 4 Positive Terminal
Y4_N	25	Output	Universal	Output 4 Negative Terminal
VDD_Y4	27	PWR	Analog	Supply pin for output 4 to set between 1.8 V, 2.5 V or 3.3 V
Y5_P	29	Output	Universal	Output 5 Positive Terminal
Y5_N	28	Output	Universal	Output 5 Negative Terminal
VDD_Y5	30	PWR	Analog	Supply pin for output 5 to set between 1.8 V, 2.5 V or 3.3 V
Y6_P	32	Output	Universal	Output 6 Positive Terminal
Y6_N	33	Output	Universal	Output 6 Negative Terminal
VDD_Y6	31	PWR	Analog	Supply pin for output 6 to set between 1.8 V, 2.5 V or 3.3 V
Y7_P	35	Output	Universal	Output 7 Positive Terminal
Y7_N	36	Output	Universal	Output 7 Negative Terminal
VDD_Y7	34	PWR	Analog	Supply pin for output 7 to set between 1.8 V, 2.5 V or 3.3 V
VDD_VCO	39	PWR	Analog	Analog power supply for PLL/VCO; This pin is sensitive to power supply noise; The supply of this pin and the VDD_PLL2 supply pin can be combined as they are both analog and sensitive supplies
VDD_PLL1	37	PWR	Analog	Analog Power Supply Connections
VDD_PLL2	38	PWR	Analog	Analog Power Supply Connections; This pin is sensitive to power supply noise; The supply of VDD_PLL2 and VDD_VCO can be combined as these pins are both power-sensitive, analog supply pins
DVDD	48	PWR	Analog	Digital Power Supply Connections; This is also the reference supply voltage for all control inputs and must match the expected input signal swing of control inputs.
GND	PAD	PWR	Analog	Power Supply Ground and Thermal Pad
STATUS0	46	Output	LVCMOS	Status pin 0 (see Table 6 for details)
STATUS1/PIN0	45	Output/ Input	LVCMOS no pull resistor	STATUS1: Status pin in SPI/I^{2}C modes. For details see Table 4 for pin modes and Table 6 for status mode. PIN0: Control pin 0 in pin mode.
SI_MODE1	47	Input	LVCMOS 50kΩ pull-up	Serial Interface Mode or Pin mode selection. SI_MODE[1:0]=00: SPI mode; SI_MODE[1:0]=01: I^{2}C mode; SI_MODE[1:0]=10: Pin Mode (No serial programming); SI_MODE[1:0]=11: RESERVED
SI_MODE0	1	Input	LVCMOS 50kΩ pull-down	
SDI/SDA/PIN1	2	Input/ Output	LVCMOS in Open drain out LVCMOS in no pull resistor	SDI: SPI Serial Data Input SDA: I^{2}C Serial Data (Read/Write bi-directional), open drain output; requires a pull-up resistor in I^{2}C mode; PIN1: Control pin 1 in pin mode

Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
SDO/AD0/PIN2	3	Output/ Input	LVCMOS out LVCMOS in LVCMOS in no pull resistor	SDO: SPI Serial Data AD0: I^2C Address Offset Bit 0 input PIN2: Control pin 2 in pin mode
SCS/AD1/PIN 3	4	Input	LVCMOS no pull resistor	SCS: SPI Latch Enable AD1: I^2C Address Offset Bit 1 input PIN3: Control pin 3 in pin mode
SCL/PIN4	5	Input	LVCMOS no pull resistor	SCL: SPI/I^2C Clock PIN4: Control pin 4 in pin mode
RESETN/PWR	44	Input	LVCMOS 50kΩ pull-up	In SPI/I^2C programming mode, external RESETN signal (active low). RESETN = V_{IL}: device in reset (registers values are retained) RESETN = V_{IH}: device active. The device can be programmed via SPI while RESETN is held low (this is useful to avoid any false output frequencies at power up). (2) In Pin mode this pin controls device core and I/O supply voltage setting. 0 = 1.8 V, 1 = 2.5/3.3 V for the device core and I/O power supply voltage. In pin mode, it is not possible to mix and match the supplies. All supplies should either be 1.8 V or 2.5/3.3 V.
REG_CAP	40	Output	Analog	Regulator Capacitor; connect a 10 µF cap with ESR below 1 Ω to GND at frequencies above 100 kHz
PDN	43	Input	LVCMOS 50kΩ pull-up	Power Down Active low. When PDN = V_{IH} is normal operation. When PDN = V_{IL}, the device is disabled and current consumption minimized. Exiting power down resets the entire device and defaults all registers. It is recommended to connect a capacitor to GND to hold the device in power-down until the digital and PLL related power supplies are stable. See section on power down in the application section.
SYNCN	42	Input	LVCMOS 50kΩ pull-up	Active low. Device outputs are synchronized on a low-to-high transition on the SYNCN pin. SYNCN held low disables all outputs.

(2) Note: the device cannot be programmed in I^2C while RESETN is held low.

8 Specifications

8.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	MAX	UNIT
Supply Voltage Range, VDD_PRI, VDD_SEC, VDD_Yx_Yy, VDD_PLL[2:1], DVDD	-0.5	4.6	V
Input Voltage Range CMOS control inputs, V_{IN}	-0.5	4.6 and V_{DVDD}+ 0.5	V
Input Voltage Range PRI/SEC inputs		4.6 and $V_{VDDPRI.SEC}$+ 0.5	V
Output Voltage Range, V_{OUT}	-0.5	V_{YxYy}+ 0.5	V
Input Current, I_{IN}		20	mA
Output Current, I_{OUT}		50	mA
Junction Temperature, T_J		125	°C
Storage temperature range, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute—maximum—rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VDD_Yx_Yy	Output Supply Voltage		1.71	1.8/2.5/3.3	3.465	V
VDD_PLL1 VDD_PLL2	Core Analog Supply Voltage		1.71	1.8/2.5/3.3	3.465	V
DVDD	Core Digital Supply Voltage		1.71	1.8/2.5/3.3	3.465	V
VDD_PRI, VDD_SEC	Reference Input Supply Voltage		1.71	1.8/2.5/3.3	3.465	V
ΔVDD/Δt	VDD power-up ramp time (0 to 3.3 V) PDN left open, all VDD tight together PDN low-high is delayed (1)				$50 < t_{PDN}$	ms
T_A	Ambient Temperature		-40		85	°C
SDA and SCL in I 2 C MODE (SI_MODE[1:0] = 01)						
V_I	Input Voltage	DVDD = 1.8 V	–0.5		2.45	V
		DVDD = 3.3 V	–0.5		3.965	V
d_R	Data Rate			100 400		kbps
V_{IH}	High-level input voltage		0.7 x DVDD			V
V_{IL}	Low-level input voltage				0.3 x DVDD	V
C_{BUS_I2C}	Total capacitive load for each bus line				400	pF

(1) For fast power up ramps under 50 ms and when all supply pins are driven from the same power supply source, PDN can be left floating. For slower power up ramps or if supply pins are sequenced with uncertain time delays, PDN needs to be held low until DVDD, VDD_PLLx, and VDD_PRI/SEC reach at least 1.45V supply voltage. See application section on mixing power supplies and particularly Figure 57 for details.

8.4 Thermal Information, Airflow = 0 LFM(1) (2) (3) (4)

THERMAL METRIC(1)		CDCM6208 RGZ 48 PINS VQFN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.27	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.58	
$R_{\theta JB}$	Junction-to-board thermal resistance	6.83	
ψ_{JT}	Junction-to-top characterization parameter	0.23	
ψ_{JB}	Junction-to-board characterization parameter	6.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.06	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(3) Connected to GND with 36 thermal vias (0.3 mm diameter).
(4) θ_{JB} (junction to board) is used for the QFN package, the main heat flow is from the junction to the GND pad of the QFN.

8.5 Thermal Information, Airflow = 150 LFM(1) (2) (3) (4)

THERMAL METRIC(1)		CDCM6208 RGZ 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		
$R_{\theta JB}$	Junction-to-board thermal resistance	6.61	
ψ_{JT}	Junction-to-top characterization parameter	0.37	
ψ_{JB}	Junction-to-board characterization parameter		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.06	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(3) Connected to GND with 36 thermal vias (0.3 mm diameter).
(4) θ_{JB} (junction to board) is used for the QFN package, the main heat flow is from the junction to the GND pad of the QFN.

8.6 Thermal Information, Airflow = 250 LFM(1) (2) (3) (4)

THERMAL METRIC(1)		CDCM6208 RGZ 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	19.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		
$R_{\theta JB}$	Junction-to-board thermal resistance	6.6	
ψ_{JT}	Junction-to-top characterization parameter	0.45	
ψ_{JB}	Junction-to-board characterization parameter		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.06	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(3) Connected to GND with 36 thermal vias (0.3 mm diameter).
(4) θ_{JB} (junction to board) is used for the QFN package, the main heat flow is from the junction to the GND pad of the QFN.

8.7 Thermal Information, Airflow = 500 LFM(1) (2) (3) (4)

THERMAL METRIC(1)		CDCM6208 RGZ 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	17.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		
$R_{\theta JB}$	Junction-to-board thermal resistance	6.58	
ψ_{JT}	Junction-to-top characterization parameter	0.58	
ψ_{JB}	Junction-to-board characterization parameter		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.05	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(3) Connected to GND with 36 thermal vias (0.3 mm diameter).
(4) θ_{JB} (junction to board) is used for the QFN package, the main heat flow is from the junction to the GND pad of the QFN.

8.8 Single Ended Input Characteristics

(SI_MODE[1:0], SDI/SDA/PIN1, SCL/PIN4, SDO/ADD0/PIN2, SCS/ADD1/PIN3, STATUS1/PIN0, RESETN/PWR, PDN, SYNCN, REF_SEL), DVDD = 1.71V to 1.89V, 2.375V to 2.625V, 3.135V to 3.465V, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage		0.8 x DVDD			V
V_{IL}	Input Low Voltage				0.2 x DVDD	V
I_{IH}	Input High Current	DVDD = 3.465V, V_{IH} = 3.465 V (pull-up resistor excluded)			30	µA
I_{IL}	Input Low Current	DVDD = 3.465V, V_{IL}= 0 V			-30	µA
ΔV/ΔT	PDN, RESETN, SYNCN, REF_SEL Input Edge Rate	20% - 80%	0.75			V/ns
minPulse	PDN, RESETN, SYNCN low pulse to trigger proper device reset		10			ns
C_{IN}	Input Capacitance			2.25		pF
RESETN, PWR, SYNCN, PDN, REF_SEL, SI_MODE[1:0]:						
R	Input Pullup and Pulldown Resistor		35	50	65	kΩ
SDA and SCL in I^2C Mode (SI_MODE[1:0]=01)						
V_{HYS_I2C}	Input hysteresis	DVDD = 1.8 V	0.1 V_{DVDD}			V
		DVDD = 2.5/3.3 V	0.05 V_{DVDD}			V
I_H	High-level input current	V_I = DVDD	–5		5	µA
V_{OL}	Output Low Voltage	I_{OL}= 3mA			0.2 x DVDD	V
C_{IN}	Input Capacitance terminal				5	pF

8.9 Single Ended Input Characteristics (PRI_REF, SEC_REF)

VDD_PRI, VDD_SEC = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IN}	Reference and Bypass Input Frequency	VDD_PRI/SEC = 1.8 V	0.008		200	MHz
		VDD_PRI/SEC = 3.3 V	0.008		250	MHz
V_{IH}	Input High Voltage		0.8 x VDD_PRI/VDD_SEC			V
V_{IL}	Input Low Voltage				0.2 x VDD_PRI/VDD_SEC	V
V_{HYST}	Input hysteresis		20	65	150	mV
I_{IH}	Input High Current	VDD_PRI/VDD_SEC = 3.465 V, V_{IH} = 3.465 V			30	µA
I_{IL}	Input Low Current	VDD_PRI/VDD_SEC = 3.465 V, V_{IL} = 0 V			-30	µA
ΔV/ΔT	Reference Input Edge Rate	20% - 80%	0.75			V/ns
IDC $_{SE}$	Reference Input Duty Cycle	f_{PRI} ≤ 200MHz	40%		60%	
		200 ≤ f_{PRI} ≤ 250 MHz	43%		60%	
C_{IN}	Input Capacitance			2.25		pF

8.10 Differential Input Characteristics (PRI_REF, SEC_REF)

VDD_PRI, VDD_SEC = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T_A = –40°C TO 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IN}	Reference and Bypass Input Frequency		0.008		250	MHz
V_I	Differential Input Voltage Swing, Peak-to-Peak	VDD_PRI/SEC = 2.5/3.3 V	0.2		1.6	V_{PP}
		VDD_PRI/SEC = 1.8 V	0.2		1	V_{PP}
V_{ICM}	Input Common Mode Voltage	CML input signaling, R4[7:6] = 00	VDD_PRI/VDD_SEC-0.4		VDD_PRI/VDD_SEC-0.1	V
V_{ICM}	Input Common Mode Voltage	LVDS, VDD_PRI/SEC = 1.8/2.5/3.3 V, R4[7:6] = 01, R4.1 = d.c., R4.0 = d.c.	0.8	1.2	1.5	V
V_{HYST}	Input hysteresis	LVDS (Q4[7:6,4:3] = 01)	15		65	mV_{pp}
		CML (Q4[7:6,4:3] = 00)	20		85	mV_{pp}
I_{IH}	Input High Current	VDD_PRI/SEC = 3.465 V, V_{IH} = 3.465 V			30	µA
I_{IL}	Input Low Current	VDD_PRI/SEC = 3.465V, V_{IL} = 0 V			-30	µA
ΔV/ΔT	Reference Input Edge Rate	20% - 80%	0.75			V/ns
IDC_{DIFF}	Reference Input Duty Cycle		30%		70%	
C_{IN}	Input Capacitance			2.7		pF

8.11 Crystal Input Characteristics (SEC_REF)

VDD_SEC = 1.71 to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V,T_A = –40°C to 85°C

PARAMETER		MIN	TYP	MAX	UNIT
MODE OF OSCILLATION		**FUNDAMENTAL**			
Frequency	See note (1)	10		30.72	MHz
	See note (2)	30.73		50	MHz
Equivalent Series Resistance (ESR)	10 MHz			150 (3)	Ω
	25 MHz			70 (4)	
	50 MHz			30 (5)	
On-chip load capacitance	1.8 V / 3.3 V SEC_REFP	3.5	4.5	5.5	pF
	1.8 V SEC_REFN	5.5	7.25	8.5	
	3.3 V SEC_REFN	6.5	7.34	8.5	
Drive Level	See note (6)			200	µW

(1) Verified with crystals specified for a load capacitance of CL=8pF, the pcb related capacitive load was estimated to be 2.3pF, and completed with a load capacitors of 4pF on each crystal terminal connected to GND. XTALs tested: NX3225GA 10MHz EXS00A-CG02813 CRG, NX3225GA 19.44MHz EXS00A-CG02810 CRG, NX3225GA 25MHz EXS00A-CG02811 CRG, and NX3225GA 30.72MHz EXS00A-CG02812 CRG.
(2) For 30.73 MHz to 50 MHz, it is recommended to verify sufficient negative resistance and initial frequency accuracy with the crystal vendor. The 50 MHz use case was verified with a NX3225GA 50MHz EXS00A-CG02814 CRG. To meet a minimum frequency error, the best choice of the XTAL was one with C_L = 7pF instead of C_L = 8pF.
(3) With NX3225GA_10M the measured remaining negative resistance on the EVM is 6430 Ω (43 x margin)
(4) With NX3225GA_25M the measured remaining negative resistance on the EVM is 1740 Ω (25 x margin)
(5) With NX3225GA_50M the measured remaining negative resistance on the EVM is 350 Ω (11 x margin)
(6) Maximum drive level measured was 145 µW; XTAL should at least tolerate 200 µW

8.12 Single Ended Output Characteristics (STATUS1, STATUS0, SDO, SDA)

VDD_Yx_Yy, VDD_PRI, VDD_SEC, VDD_PLLx, DVDD, VDD_VCO = 1.71V to 1.89V, 2.375V to 2.625V, 3.135V to 3.465V; T_A = –40°C to 85°C (Output load capacitance 10 pF unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output High Voltage	Status 1, Status 0, and SDO only; SDA is open drain and relies on external pullup for high output; I_{OH} = 1 mA	0.8 x DVDD			V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			0.2 x DVDD	V
V_{slew}	Output slew rate	30% - 70%	0.5			V/ns
I_{OZH}	3-stat Output High Current	DVDD = 3.465 V, V_{IH} = 3.465 V			5	µA
I_{OZL}	3-stat Output Low Current	DVDD = 3.465 V, V_{IL} = 0 V			-5	µA
t_{LOS}	Status Loss of Signal Detection Time	LOS_REFfvco		1	2	$1/f_{PFD}$
t_{LOCK}	Status PLL Lock Detection Time	Detect lock		2304		$1/f_{PFD}$
		Detect unlock		512		

8.13 PLL Characteristics

VDD_PLLx, VDD_VCO = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T_A = –40°C TO 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO}	VCO Frequency Range		2.39		2.55	GHz
K_{VCO}	VCO Gain	2.39 GHz		178		MHz/V
		2.50 GHz		204		
		2.55 GHz		213		
f_{PFD}	PFD Input Frequency		0.008		100	MHz
I_{CP-L}	High Impedance Mode Charge Pump Leakage			±700		nA
f_{FOM}	Estimated PLL Figure of Merit (FOM)	Measured in-band phase noise at the VCO output minus 20log(N-divider) at the flat region		–224		dBc/Hz
$t_{STARTUP}$	Startup time (see Figure 41)	Power supply ramp time of 1ms from 0 V to 1.7 V, final frequency accuracy of 10 ppm, f_{PFD} = 25 MHz, $C_{PDN\_to\_GND}$ = 22nF				
		w/ PRI input signal		12.8		ms
		w/ NDK 25 MHz crystal		12.85		ms

8.14 LVCMOS Output Characteristics

VDD_Yx_Yy = 1.71 V to 1.89V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T_A = –40°C TO 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT-F}	Output Frequency	Fract Out divVDD_Yx_Yy = 2.5/3.3 V	0.78		250	MHz
		Integer out divVDD_Yx_Yy = 2.5/3.3 V	1.55		250	
		Int or frac out divVDD_Yx_Yy = 1.8 V	0.78/1.5		200	
f_{ACC-F}	Output Frequency Error (1)	Fractional Output Divider	–1		1	ppm
V_{OH}	Output High Voltage (normal mode)	VDD_Yx = min to max, I_{OH} = -1 mA	0.8 x VDD_Yx_Yy			V
V_{OL}	Output Low Voltage(normal mode)	VDD_Yx = min to max, I_{OL} = 100 µA			0.2 x VDD_Yx_Yy	V
V_{OH}	Output High Voltage (slow mode)	VDD_Yx = min to max, I_{OH} = -100 µA	0.7 x VDD_Yx_Yy			V
V_{OL}	Output Low Voltage(slow mode)	VDD_Yx = min to max, I_{OL} = 100 µA			0.3 x VDD_Yx_Yy	V
I_{OH}	Output High Current	V_{OUT} = VDD_Yx_Yy/2				
		Normal mode	–50		-8	mA
		Slow mode	–45		-5	mA
I_{OL}	Output Low Current	V_{OUT} = VDD_Yx_Yy/2				
		Normal mode	10		55	mA
		Slow mode	5		40	mA
$t_{SLEW-RATE-N}$	Output Rise/Fall Slew Rate (normal mode)	20% to 80%, VDD_Yx_Yy = 2.5/3.3 V, C_L = 5 pF		5.37		V/ns
	Output Rise/Fall Slew Rate (normal mode)	20% to 80%, VDD_Yx_Yy = 1.8 V, C_L = 5 pF		2.62		V/ns
$t_{SLEW-RATE-S}$	Output Rise/Fall Slew Rate (slow mode)	20% to 80%, VDD_Yx_Yy = 2.5/3.3 V, C_L = 5 pF		4.17		V/ns
	Output Rise/Fall Slew Rate (slow mode)	20% to 80%, VDD_Yx_Yy = 1.8 V, C_L = 5 pF		1.46		V/ns
PN-floor	Phase Noise Floor	f_{OUT} = 122.88 MHz		–159.5	–154	dBc/Hz
ODC	Output Duty Cycle	Not in bypass mode	45%		55%	
R_{OUT}	Output Impedance	V_{OUT} = VDD_Yx/2				
		Normal mode Slow mode	30 45	50 74	90 130	Ω

(1) The User's GUI calculates exact frequency error. It is a fixed, static offset. If the desired output target frequency is with the exact reach of a multiple 1 over 2^{20}, the actual output frequency error is 0.
Note: In LVCMOS Mode, positive and negative outputs are in phase.

8.15 LVPECL (High-Swing CML) Output Characteristics

VDD_Yx_Yy = 1.71 V to 3.465 V, VDD_PRI, VDD_SEC, VDD_PLLx, DVDD, VDD_VCO = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T_A = –40°C TO 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OUT-I}	Output frequency	Integer Output Divider	1.55		800	MHz
V_{CM-DC}	Output DC coupled common mode voltage	DC coupled with 50 Ω external termination to VDD_Yx_Yy		VDD_Yx_Yy – 0.4		V
$\|V_{OD}\|$	Differential output voltage	100 Ω diff load AC coupling (See Figure 11), f_{OUT} ≤ 250 MHz				
		VDD_Yx_Yy ≤ 1.89 V	0.45	0.75	1.12	V
		VDD_Yx_Yy ≥ 2.375 V	0.6	0.8	1.12	V
		100 Ω diff load AC coupling (See Figure 11), f_{OUT} ≥ 250 MHz				
		VDD_Yx_Yy ≤ 1.89 V		0.73		V
		VDD_Yx_Yy ≥ 2.375 V	0.55	0.75	1.12	V
V_{OUT}	Differential output peak-to-peak voltage			2 x $\|V_{OD}\|$		V
t_R/t_F	Output rise/fall time	±200 mV around crossing point	109		217	ps
		20% to 80% V_{OD}		211		ps
t_{slew}	Output rise/fall slew rate		3.7	5.1	7.3	V/ns
PN-floor	Phase noise floor	VDD_Yx_Yy = 3.3 V (See Figure 53)		–161.4	–155.8	dBc/Hz
ODC	Output duty cycle	Not in bypass mode	47.5%		52.5%	
R_{OUT}	Output impedance	measured from pin to VDD_Yx_Yy		50		Ω

8.16 CML Output Characteristics

VDD_Yx_Yy, VDD_PRI, VDD_SEC, VDD_PLLx, DVDD, VDD_VCO = 1.71V to 1.89V, 2.375V to 2.625V, 3.135V to 3.465V, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{OUT-I}	Output frequency	Integer Output Divider		1.55		800	MHz
V_{CM-AC}	Output AC coupled common mode voltage	AC coupled with 50 Ω receiver termination			VDD_Yx_Yy – 0.46		V
V_{CM-DC}	Output DC coupled common mode voltage	DC coupled with 50 Ω on-chip termination to VDD_Yx_Yy			VDD_Yx_Yy – 0.2		V
$\|V_{OD}\|$	Differential output voltage	100 Ω diff load AC coupling, (See Figure 11)		0.3	0.45	0.58	V
V_{OUT}	Differential output peak-to-peak voltage				2 x $\|V_{OD}\|$		V
t_R/t_F	Output rise/fall time	20% to 80%	VDDYx = 1.8 V	100	151	300	ps
			VDDYx = 2.5 V/3.3 V	100	143	200	ps
PN-floor	Phase noise floor at > 5 Hz offset	f_{OUT} = 122.88 MHz	VDD_Yx_Yy = 1.8 V		–161.2	–155.8	dBc/Hz
			VDD_Yx_Yy = 3.3 V		–161.2	–153.8	dBc/Hz
ODC	Output duty cycle	Not in bypass mode		47.5%		52.5%	
R_{OUT}	Output impedance	measured from pin to VDD_Yx_Yy			50		Ω

8.17 LVDS (Low-Power CML) Output Characteristics

VDD_Yx_Yy, VDD_PRI, VDD_SEC, VDD_PLLx, DVDD, VDD_VCO = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135V to 3.465V, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{OUT-I}	Output frequency	Integer output divider		1.55		400	MHz
f_{OUT-F}		Fractional output divider		0.78		400	MHz
f_{ACC-F}	Output frequency error (1)	Fractional output divider		-1		1	ppm
V_{CM-AC}	Output AC coupled common mode voltage	AC coupled with 50 Ω receiver termination			VDD_Yx_Yy – 0.76		V
V_{CM-DC}	Output DC coupled common mode voltage	DC coupled with 50 Ω on-chip termination to VDD_Yx_Yy			VDD_Yx_Yy – 0.13		V
$\|V_{OD}\|$	Differential output voltage	100 Ω diff load AC coupling, (See Figure 11)		0.247	0.34	0.454	V
V_{OUT}	Differential output peak-to-peak voltage				2 x $\|V_{OD}\|$		V
t_R/t_F	Output rise/fall time	±100mV around crossing point				300	ps
PN-floor	Phase noise floor	f_{OUT}= 122.88 MHz	VDD_Yx = 1.8 V		–159.3	–154.5	dBc/Hz
			VDD_Yx = 2.5/3.3 V		–159.1	–154.9	dBc/Hz
ODC	Output duty cycle	Not in bypass mode	Y[3:0]	47.5%		52.5%	
			Y[7:4]	45%		55%	
R_{OUT}	Output impedance	Measured from pin to VDD_Yx_Yy			167		Ω

(1) The User's GUI calculates exact frequency error. It is a fixed, static offset. If the desired output target frequency is with the exact reach of a multiple of 1 over 2^{20}, the actual output frequency error is 0.

8.18 HCSL Output Characteristics

VDD_Yx_Yy, VDD_PRI, VDD_SEC, VDD_PLLx, DVDD, VDD_VCO = 1.71 to 1.89 V, 2.375 V to 2.625 V,3.135 V to 3.465 V, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{OUT-I}	Output frequency	Integer Output Divider		1.55		400	MHz
f_{OUT-F}		Fractional Output Divider		0.78		400	MHz
f_{ACC-F}	Output Frequency Error (1)	Fractional Output Divider		-1		1	ppm
V_{CM}	Output Common Mode Voltage	VDD_Yx_Yy = 2.5/3.3 V		0.2	0.34	0.55	V
		VDD_Yx_Yy = 1.8 V		0.2	0.33	0.55	V
$\|V_{OD}\|$	Differential Output Voltage	VDD_Yx_Yy = 2.5/3.3 V		0.4	0.67	1.0	V
		VDD_Yx_Yy = 1.8 V		0.4	0.65	1.0	V
V_{OUT}	Differential Output Peak-to-peak Voltage	VDD_Yx_Yy = 2.5/3.3 V		1.0		2.1	V
		VDD_Yx_Yy = 1.8 V			2 x$\|V_{OD}\|$		V
t_R/t_F	Output Rise/Fall Time	Measured from V_{DIFF}= –100 mV to V_{DIFF} = +100mV, VDD_Yx_Yy = 2.5/3.3 V		100	167	250	ps
		Measured from V_{DIFF}= –100 mV to V_{DIFF}= +100 mV, VDD_Yx_Yy = 1.8 V		120	192	295	
PN-floor	Phase Noise Floor	f_{OUT} = 122.88 MHz	VDD_Yx_Yy = 1.8 V		–158.8	–153	dBc/Hz
			VDD_Yx = 2.5/3.3 V		–157.6	–153	dBc/Hz
ODC	Output Duty Cycle	Not in bypass mode		45%		55%	

(1) The User's GUI calculates exact frequency error. It is a fixed, static offset. If the desired output target frequency is with the exact reach of A $1/2^{20}$ multiple, the actual output frequency error is 0.

8.19 Output Skew and Sync to Output Propagation Delay Characteristics

VDD_Yx_Yy = 1.71 to 1.89 V, 2.375 V to 2.625 V, 3.135V to 3.465 V, T_A = –40°C to 85°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PD-PS}	Propagation delay SYNCN↑ to output toggling high	f_{VCO} = 2.5 GHz	PS_A = 4	9	10.5	11	$1/f_{PS\_A}$
			PS_A = 5	9	10.2	11	$1/f_{PS\_A}$
			PS_A = 6	9	10.0	11	$1/f_{PS\_A}$
Δt_{PD-PS}	Part-to-Part Propagation delay variation SYNCN↑ to output toggling high(1)	Fixed supply voltage, temp, and device setting(1)			0	1	$1/f_{PS\_A}$
OUTPUT SKEW – ALL OUTPUTS USE IDENTICAL OUTPUT SIGNALING, INTEGER DIVIDERS ONLY; PS_A = PS_B = 6, OutDiv = 4							
$t_{SK,LVDS}$	Skew between Y[7:4] LVDS	Y[7:4] = LVDS				40	ps
$t_{SK,LVDS}$	Skew between Y[3:0] LVDS	Y[3:0] = LVDS				40	ps
$t_{SK,LVDS}$	Skew between Y[7:0] LVDS	Y[7:0] = LVDS				80	ps
$t_{SK,CML}$	Skew between Y[3:0] CML	Y[3:0] = CML				40	ps
$t_{SK,PECL}$	Skew between Y[3:0] PECL	Y[3:0] = LVPECL				40	ps
$t_{SK,HCSL}$	Skew between Y[7:4] HCSL	Y[7:4] = HCSL				40	ps
$t_{SK,SE}$	Skew between Y[7:4] CMOS	Y[7:4] = CMOS				50	ps
OUTPUT SKEW - MIXED SIGNAL OUTPUT CONFIGURATION, INTEGER DIVIDERS ONLY; PS_A = PS_B = 6, OutDiv = 4							
$t_{SK,CMOS-LVDS}$	Skew between Y[7:4] LVDS and CMOS mixed	Y[4] = CMOS, Y[7:5] = LVDS				2.5	ns
$t_{SK,CMOS-PECL}$	Skew between Y[7:0] CMOS and LVPECL mixed	Y[7:4] = CMOS, Y[3:0] = LVPECL				2.5	ns
$t_{SK,PECL-LVDS}$	Skew between Y[3:0] LVPECL and LVDS mixed	Y[0] = LVPECL, Y[3:1] = LVDS				120	ps
$t_{SK,PECL-CML}$	Skew between Y[3:0] LVPECL and CML mixed	Y[0] = LVPECL, Y[3:1] = CML				40	ps
$t_{SK,LVDS-PECL}$	Skew between Y[7:0] LVDS and LVPECL mixed	Y[7:4] = LVDS, Y[3:0] = LVPECL				180	ps
$t_{SK,LVDS-HCSL}$	Skew between Y[7:4] LVDS and HCSL mixed	Y[4] = LVDS, Y[7:5] = HCSL				250	ps
OUTPUT SKEW - USING FRACTIONAL OUTPUT DIVISION; PS_A = PS_B = 6, OutDiv = 3.125							
$t_{SK,DIFF,\ frac}$	Skew between Y[7:4] LVDS using all fractional divider with the same divider setting	Y[7:4] = LVDS				200	ps

(1) SYNC is toggled 10,000 times for each device. Test is repeated over process voltage and temperature (PVT).

8.20 Device Individual Block Current Consumption

VDD_Yx_Yy, VDD_PRI, VDD_SEC, VDD_PLLx, DVDD, VDD_VCO = 1.8 V, 2.5 V, or 3.3 V, T_A = –40°C to 85°C, Output Types = LVPECL/CML/LVDS/LVCMOS/HCSL

BLOCK	CONDITION	TYPICAL CURRENT CONSUMPTION (mA)
Core	CDCM6208V2G Core, active mode, PS_A = PS_B = 4	75
Output Buffer	CML output, AC coupled w/ 100 Ω diff load	24.25
	LVPECL, AC coupled w/ 100 Ω diff load	40
	LVCMOS output, transient, 'C_L' load, 'f' MHz output frequency, 'V' output swing	$1.8 + V \times f_{OUT} \times (C_L + 12 \times 10^{-12}) \times 10^3$
	LVDS output, AC coupled w/ 100 Ω diff load	19.7
	HCSL output, 50 Ω load to GND on each output pin	31
Output Divide Circuitry	Integer Divider Bypass (Divide = 1)	3
	Integer Divide Enabled, Divide > 1	8
	Fractional Divider Enabled	12
	additional current when PS_A differs from PS_B	15
Total Device, CDCM6208V2G	Device Settings (V2) 1. PRI input enabled, set to LVDS mode 2. SEC input XTAL 3. Input bypass off, PRI only sent to PLL 4. Reference clock 30.72 MHz 5. PRI input divider set to 1 6. Reference input divider set to 1 7. Charge Pump Current = 2.5 mA 8. VCO Frequency = 3.072 GHz 9. PS_A = PS_B divider ration = 4 10. Feedback divider ratio = 25 11. Output divider ratio = 5 12. Fractional divider pre-divider = 2 13. Fractional divider core input frequency = 384 MHz 14. Fractional divider value = 3.84, 5.76, 3.072, 7.68 15. CML outputs selected for CH0-3 (153.6 MHz) LVDS outputs selected for CH4-7 (100 MHz, 66.66 MHz, 125 MHz, 50 MHz)	(excl. $I_{termination\_resistors}$) (1.8 V: 251 mA 2.5 V: 254 mA 3.3 V: 257 mA) (incl. $I_{termination\_resistors}$) (1.8 V: 310 mA 2.5 V: 313 mA 3.3 V: 316 mA)
Total Device, CDCM6208V2G	Power Down (PDN = '0')	0.35

Helpful Note: The CDCM6208V2G User GUI does an excellent job estimating the total device current consumption based on the actual device configuration. Therefore, it is recommended to use the GUI to estimate device power consumption.

8.21 Worst Case Current Consumption

VDD_Yx_Yy, VDD_PRI, VDD_SEC, VDD_PLLx, DVDD, VDD_VCO = 3.45 V, T_A = T-40°C to 85°C, Output Types = maximum swing, all blocks including duty cycle correction and fractional divider enabled and operating at maximum operation

BLOCK	CONDITION	CURRENT CONSUMPTION TYP / MAX
Total Device, CDCM6208V2G	All conditions over PVT, AC coupled outputs with all outputs terminated, device configuration: Device Settings (V2) 1. PRI input enabled, set to LVDS mode 2. SEC input XTAL 3. Input bypass off, PRI only sent to PLL 4. Reference clock 30.72 MHz 5. PRI input divider set to 1 6. Reference input divider set to 1 7. Charge Pump Current = 2.5 mA 8. VCO Frequency = 3.072 GHz 9. PS_A = PS_B divider ration = 4 10. Feedback divider ratio = 25 11. Output divider ratio = 5 12. Fractional divider pre-divider = 2 13. Fractional divider core input frequency = 384 MHz 14. Fractional divider value = 3.84, 5.76, 3.072, 7.68 15. CML outputs selected for CH0-3 (153.6 MHz) LVDS outputs selected for CH4-7 (100MHz, 66.66 MHz, 125 MHz, 50 MHz)	1.8 V: 310 mA / +21% (excl term) 3.3 V: 318 mA / +21% (excl term)

8.22 I²C TIMING(1)

PARAMETER		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL Clock Frequency	0	100	0	400	kHz
$t_{su(START)}$	START Setup Time (SCL high before SDA low)	4.7		0.6		µs
$t_{h(START)}$	START Hold Time (SCL low after SDA low)	4.0		0.6		µs
$t_{w(SCLL)}$	SCL Low-pulse duration	4.7		1.3		µs
$t_{w(SCLH)}$	SCL High-pulse duration	4.0		0.6		µs
$t_{h(SDA)}$	SDA Hold Time (SDA valid after SCL low)	0 (2)	3.45	0	0.9	µs
$t_{su(SDA)}$	SDA Setup Time	250		100		ns
$t_{r\text{-}in}$	SCL / SDA input rise time		1000		300	ns
$t_{f\text{-}in}$	SCL / SDA input fall time		300		300	ns
$t_{f\text{-}out}$	SDA Output fall time from V_{IH} min to V_{IL} max with a bus capacitance from 10 pF to 400 pF		250		250	ns
$t_{su(STOP)}$	STOP Setup Time	4.0		0.6		µs
t_{BUS}	Bus free time between a STOP and START condition	4.7		1.3		µs
t_{glitch_filter}	Pulse width of spikes suppressed by the input glitch filter	75	300	75	300	ns

(1) For additional information, refer to the I²C-Bus specification, Version 2.1 (January 2000); the CDCM6208V2G meets the switching characteristics for standard mode and fast mode transfer.
(2) The I²C master must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

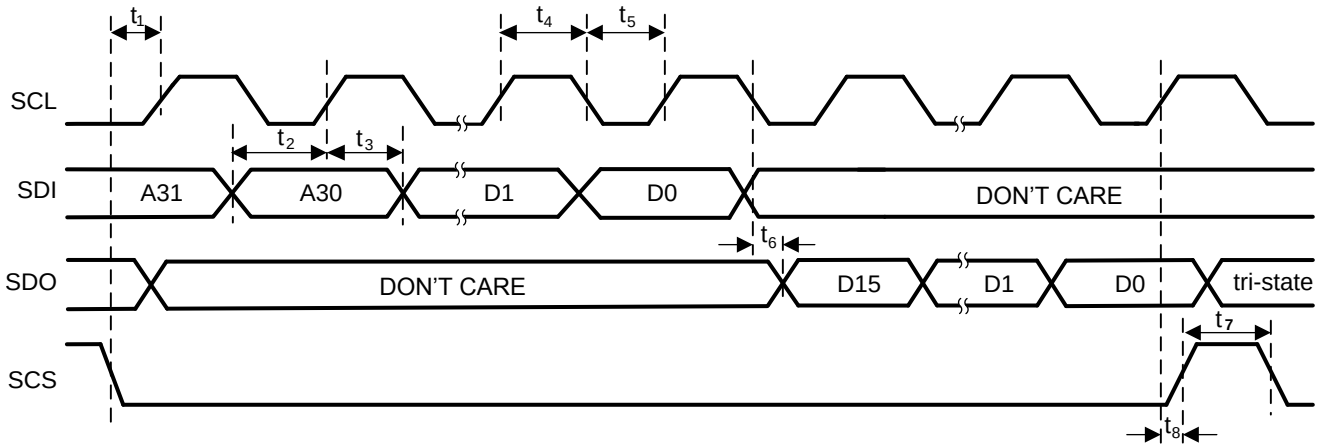


Figure 1. CDCM6208V2G SPI Port Timing

8.23 SPI Timing Requirements

PARAMETER		MIN	NOM	MAX	UNIT
f_{Clock}	Clock Frequency for the SCL			20	MHz
t_1	SPI_LE to SCL setup time	10			ns
t_2	SDI to SCL setup time	10			ns
t_3	SDO to SCL hold time	10			ns
t_4	SCL high duration	25			ns
t_5	SCL low duration	25			ns
t_6	SCL to SCS Setup time	10			ns
t_7	SCS Pulse Width	20			ns
t_8	SDI to SCL Data Valid (First Valid Bit after SCS)	10			ns

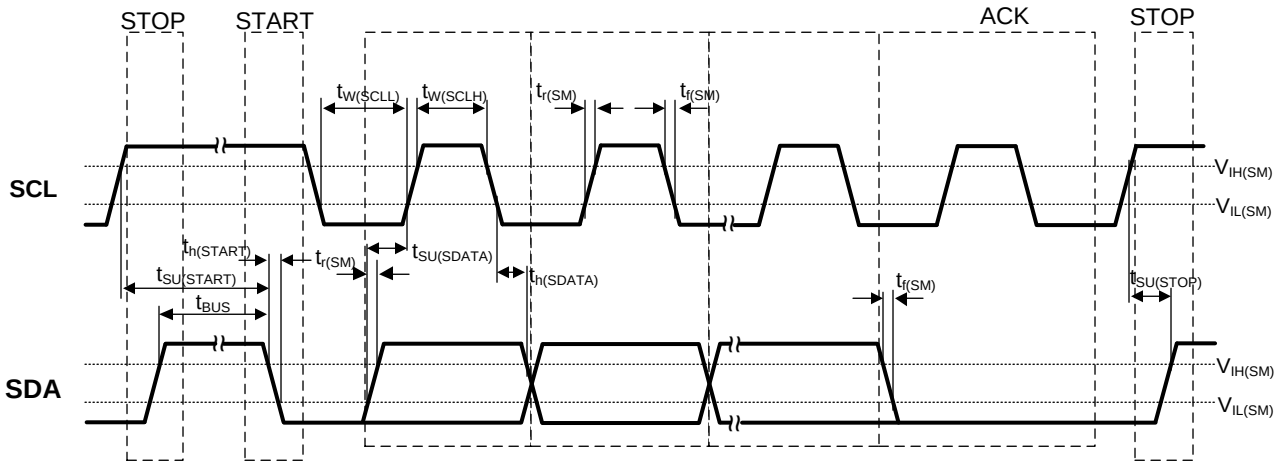
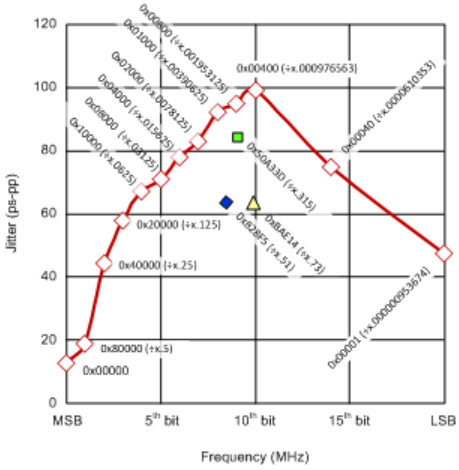


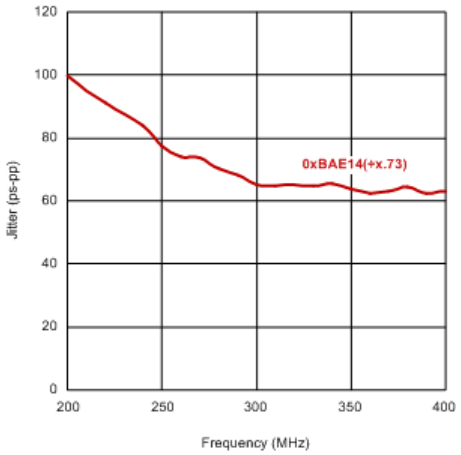
Figure 2. I^2C Timing Diagram

8.24 Typical Characteristics



f_{FRAC} = 300 MHz

Figure 3. Fractional Divider Bit Selection Impact on Jitter



Using Divide by x.73 Example

Figure 4. Fractional Divider Input Frequency Impact on Jitter

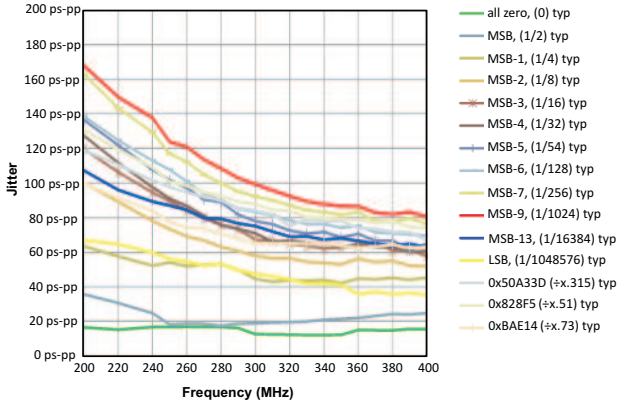


Figure 5. Fractional Divider Bit Selection Impact on T_J (Typical)

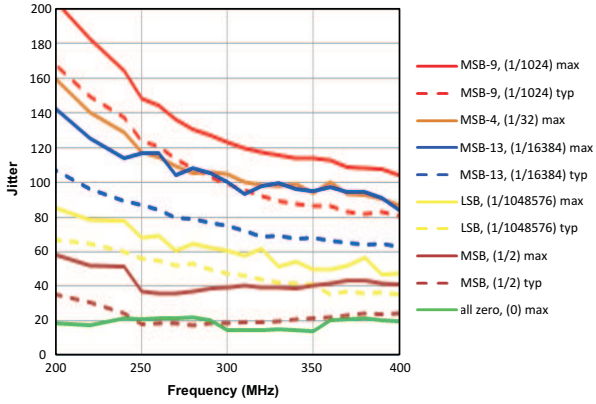
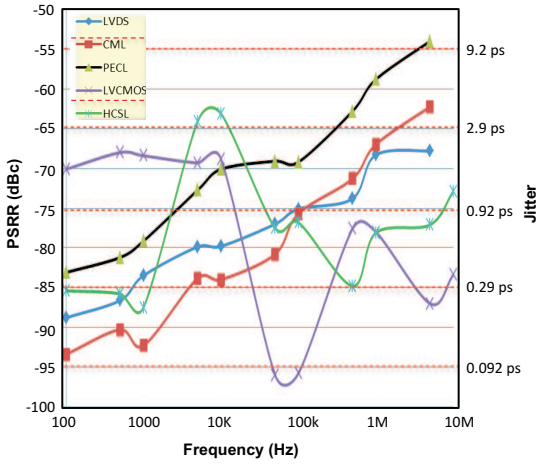


Figure 6. Fractional Divider Bit Selection Impact on T_J (Maximum Jitter Across Process, Voltage & Temperature)



f_{OUT} = 122 MHz

Figure 7. PSRR (in dBc and DJ [ps]) Over Frequency [Hz] and Output Signal Format

8.24.1 Fractional Output Divider Jitter Performance

The fractional output divider jitter performance is a function of the fraction output divider input frequency as well as actual fractional divide setting itself. To minimize the fractional output jitter, it is recommended to use the least number of fractional bits and the highest input frequency possible into the divider. As observable in Figure 3, the largest jitter contribution occurs when only one fractional divider bit is selected, and especially when the bits in the middle range of the fractional divider are selected. Tested using a LeCroy 40 Gbps RealTime scope over a time window of 200 ms. The R_J impact on T_J is estimated for a BERT $10^{(-12)}$ – 1. This measurement result is overly pessimistic, as it does not bandwidth limit the high-frequencies. In a real system, the SERDES TX will BW limit the jitter through its PLL roll-off above the TX PLL bandwidth of typically bit rate divided by 10.

8.24.2 Power Supply Ripple Rejection (PSRR) versus Ripple Frequency

See Figure 7 for reference.

Many system designs become increasingly more sensitive to power supply noise rejection. In order to simplify design and cost, the CDCM6208V2G has built in internal voltage regulation, improving the power supply noise rejection over designs with no regulators. As a result, the following output rejection is achieved:

The DJ due to PSRR can be estimated using Equation 1:

$$\text{Deterministic Jitter } (ps_{p\text{-}p}) = \frac{2 \times 10^{(spur/20)}}{\pi \times f_{CLK}} \times 10^{-12} \quad (1)$$

Example: *Therefore, if 100 mV noise with a frequency of 10 kHz were observed at the output supply, the according output jitter for a 122.88 MHz output signal with LVDS signaling could be estimated with DJ = 0.7ps.*

9 Parameter Measurement Information

9.1 Characterization Test Setup

This section describes the characterization test setup of each block in the CDCM6208V2G.

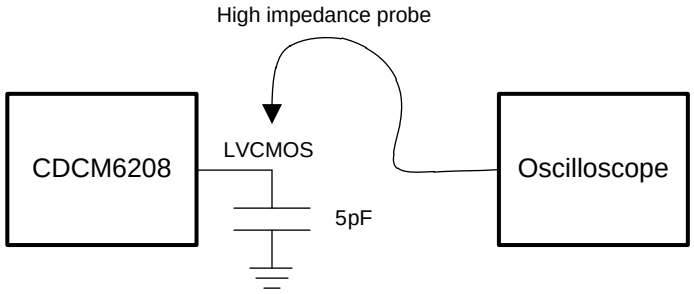


Figure 8. LVCMOS Output AC Configuration During Device Test (V_{OH}, V_{OL}, t_{SLEW})

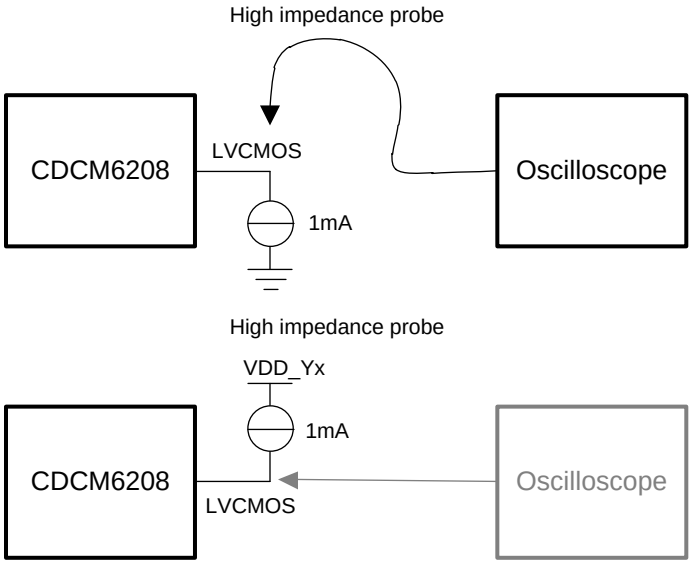


Figure 9. LVCMOS Output DC Configuration During Device Test

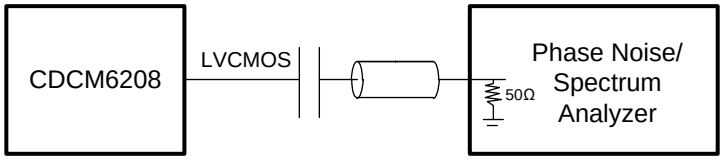


Figure 10. LVCMOS Output AC Configuration During Device Phase Noise Test

Characterization Test Setup (continued)

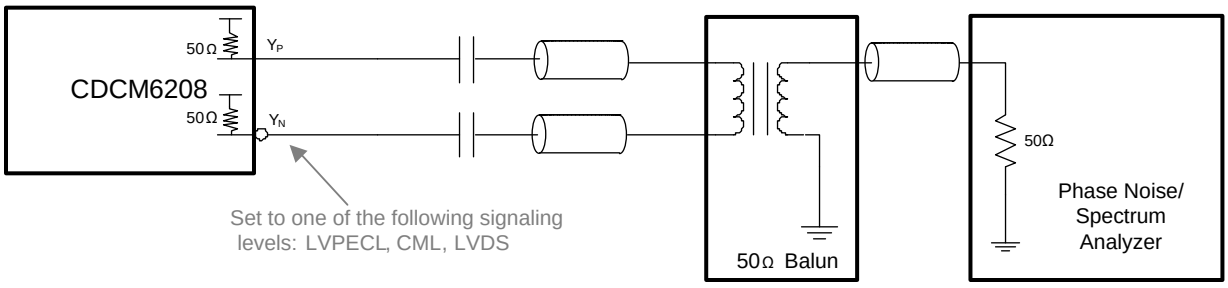


Figure 11. LVDS, CML, and LVPECL Output AC Configuration During Device Test

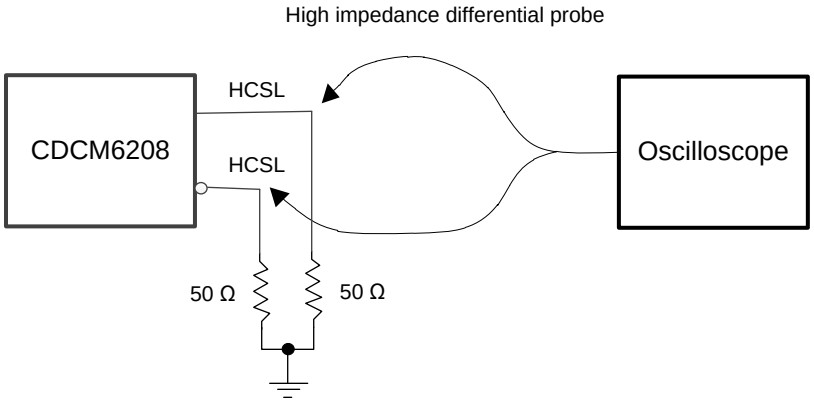


Figure 12. HCSL Output DC Configuration During Device Test

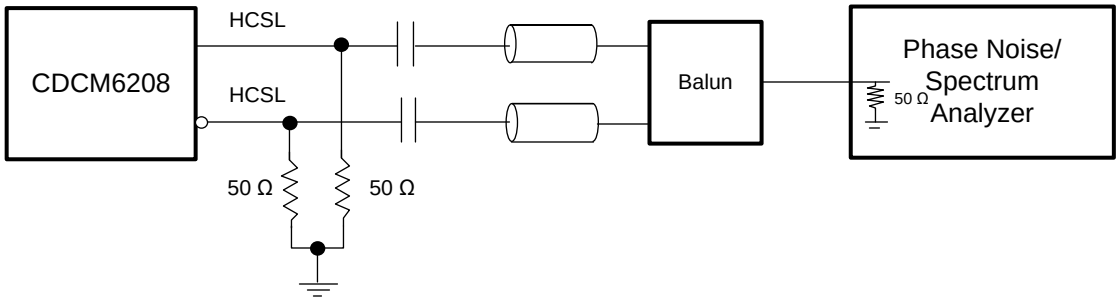


Figure 13. HCSL Output AC Configuration During Device Test

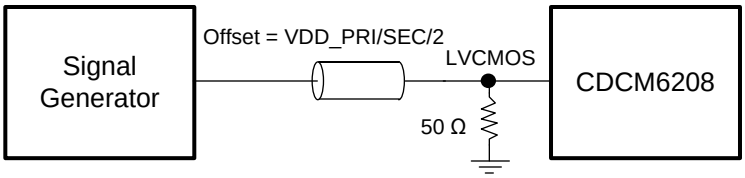


Figure 14. LVCMOS Input DC Configuration During Device Test

Characterization Test Setup (continued)

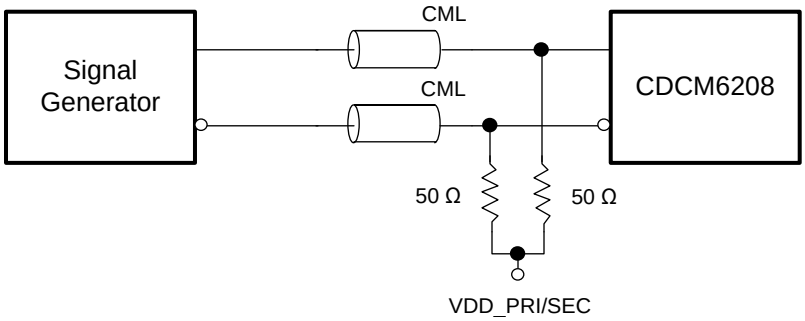


Figure 15. CML Input DC Configuration During Device Test

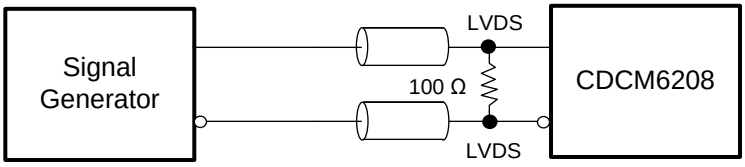


Figure 16. LVDS Input DC Configuration During Device Test

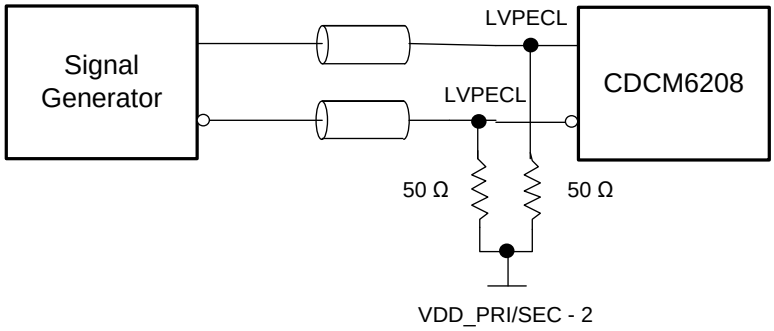


Figure 17. LVPECL Input DC Configuration During Device Test

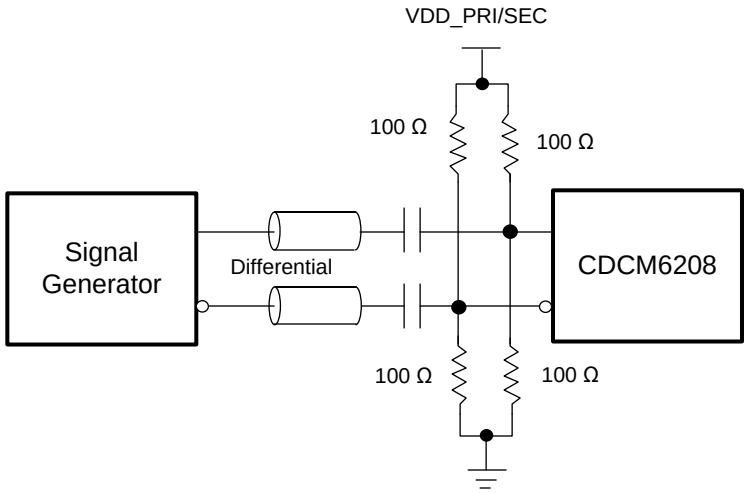


Figure 18. Differential Input AC Configuration During Device Test

Characterization Test Setup (continued)

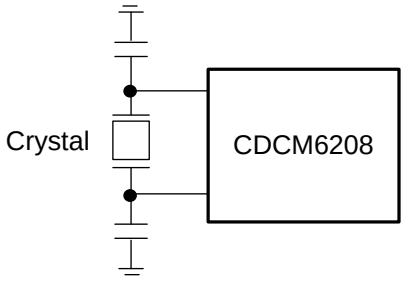


Figure 19. Crystal Reference Input Configuration During Device Test

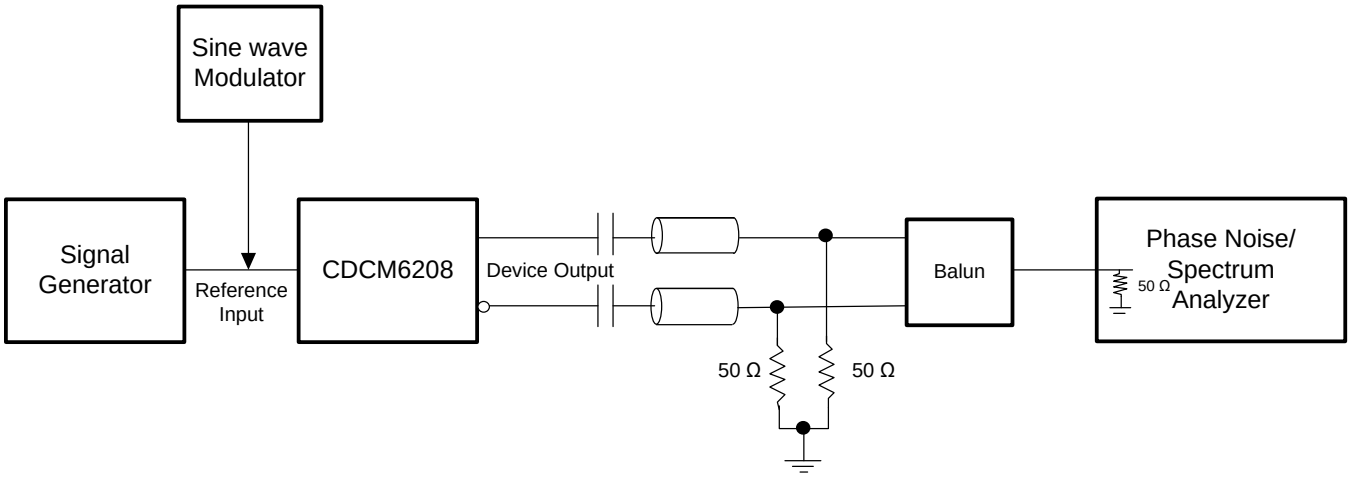


Figure 20. Jitter transfer Test Setup

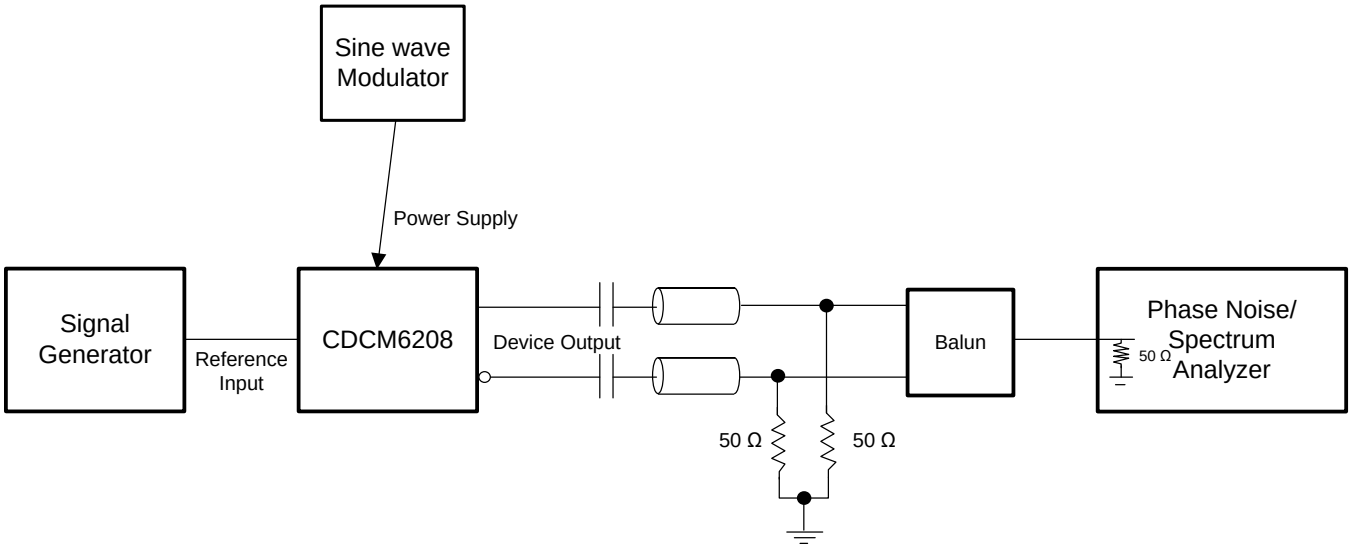


Figure 21. PSNR Test Setup

Characterization Test Setup (continued)

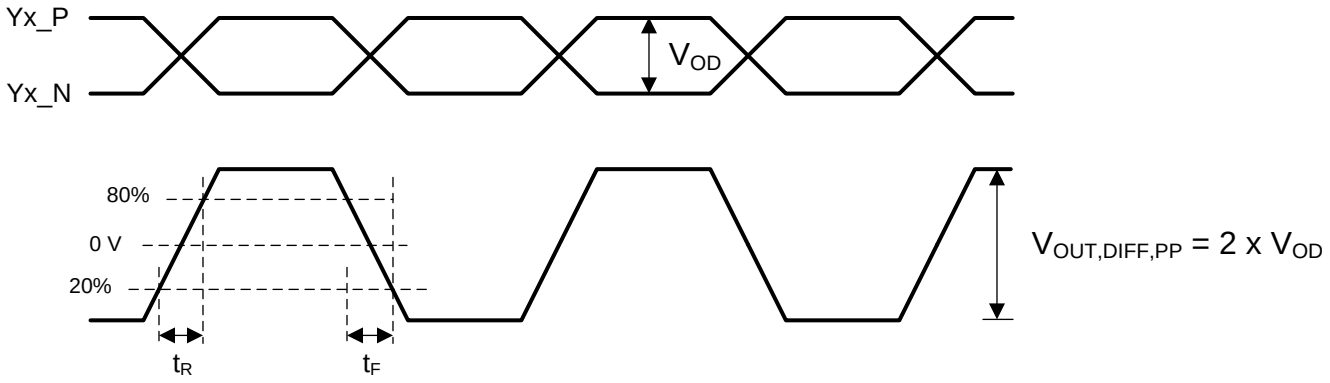


Figure 22. Differential Output Voltage and Rise and Fall Time

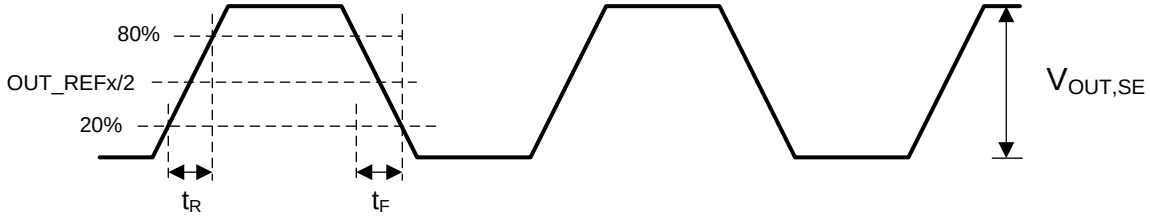


Figure 23. Single Ended Output Voltage and Rise and Fall Time

Characterization Test Setup (continued)

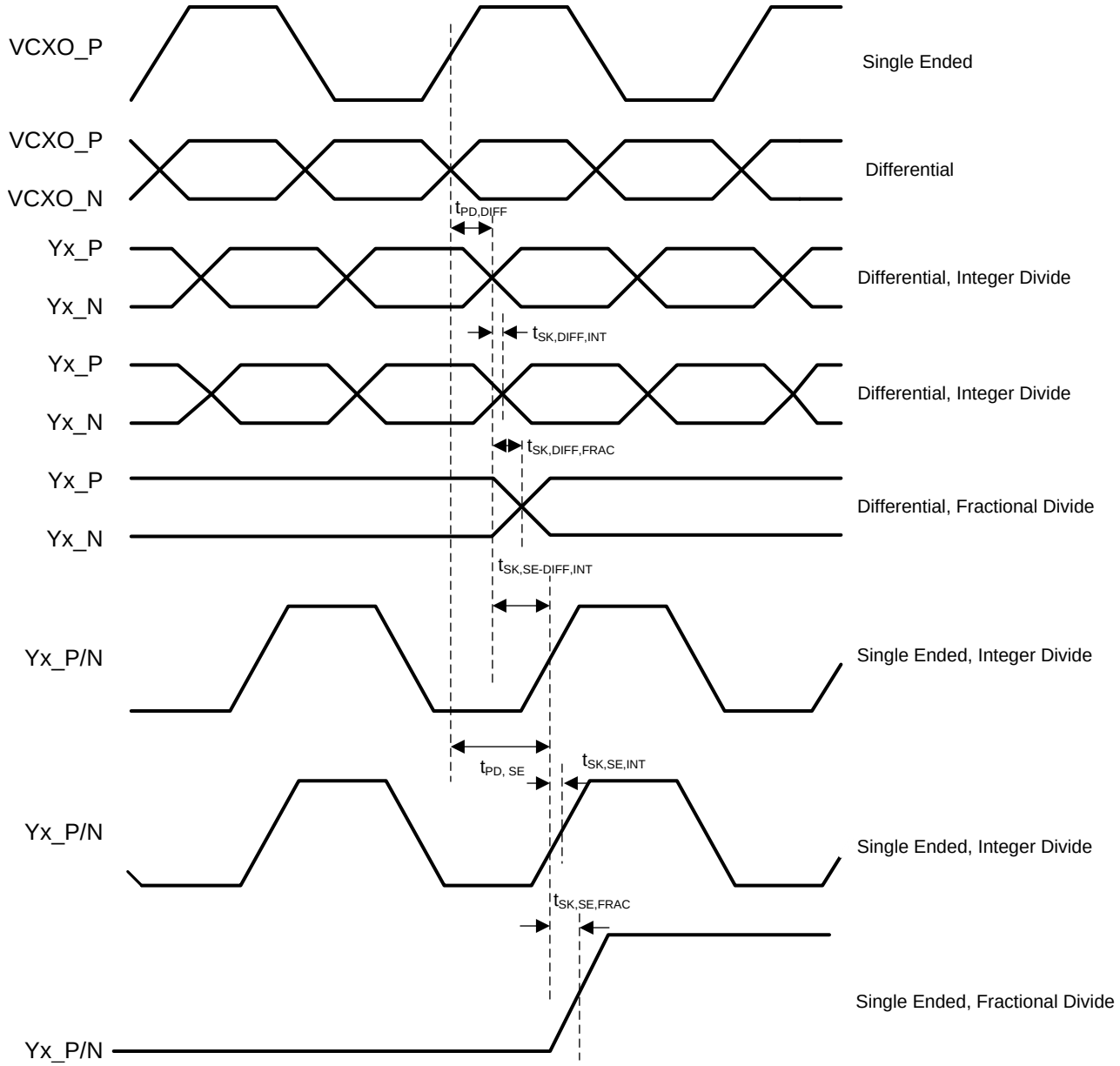


Figure 24. Differential and Single Ended Output Skew and Propagation Delay

10 Detailed Description

10.1 Overview

Supply Voltage: The CDCM6208V2G supply is internally regulated. Therefore each core and I/O supply can be mixed and matched in any order according to the application needs. The device jitter performance is independent of supply voltage.

Frequency Range: The PLL includes dual reference inputs with input multiplexer, charge pump, loop filter, and VCO that operates from 2.39 GHz to 2.55 GHz.

Reference inputs: The primary and secondary reference inputs support differential and single ended signals from 8 kHz to 250 MHz. The secondary reference input also supports crystals from 10 MHz to 50 MHz. There is a 4-bit reference divider available on the primary reference input. The input mux between the two references supports simply switching or can be configured as Smart MUX and supports glitchless input switching.

Divider and Prescaler: In addition to the 4-bit input divider of the primary reference a 14-b input divider at the output of input MUX and a cascaded 8-b and 10-b continuous feedback dividers are available. Two independent prescaler dividers offer divide by /4, /5 and /6 options of the VCO frequency of which any combination can then be chosen for a bank of 4 outputs (2 with fractional dividers and 2 that share an integer divider) through an output MUX. A total of 2 output MUXes are available.

Phase Frequency Detector and Charge Pump: The PFD input frequency can range from 8 kHz to 100 MHz. The charge pump gain is programmable and the loop filter consists of internal + partially external passive components and supports bandwidths from a few Hz up to 400kHz.

10.2 Functional Block Diagram

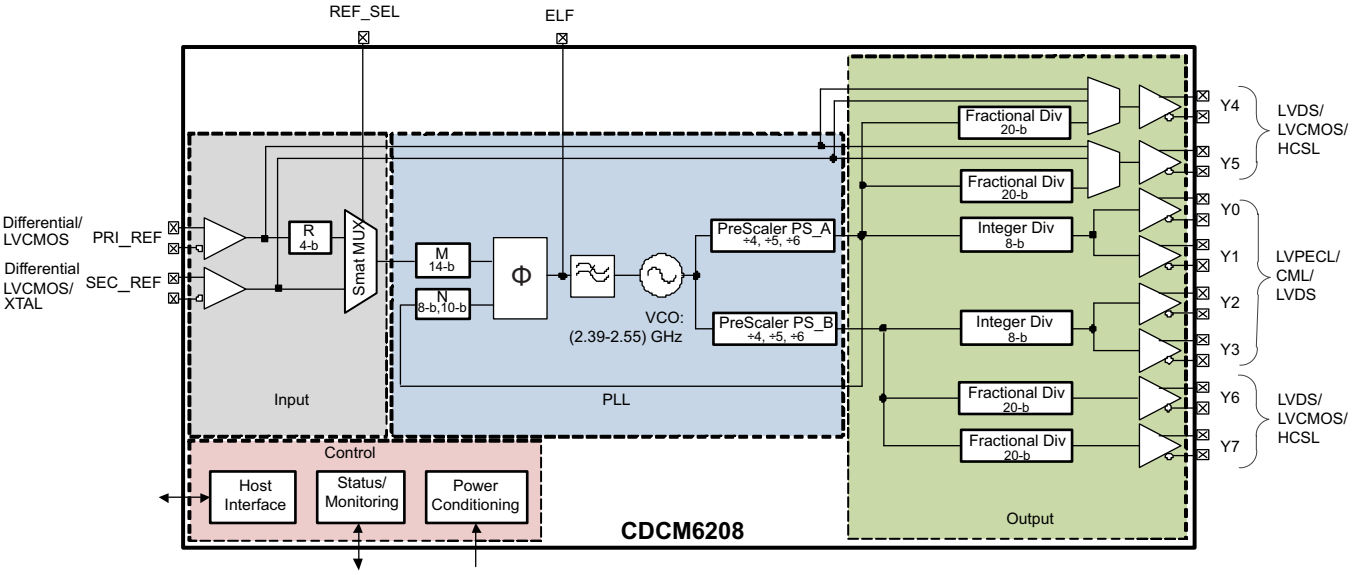


Figure 25. High-Level Block Diagram of CDCM6208V2G

10.3 Feature Description

Phase Noise: The Phase Noise performance of the device can be summarized to:

Table 1. Synthesizer Mode (Loop filter BW >250 kHz)

RANDOM JITTER (ALL OUTPUTS)			TOTAL JITTER	
TYPICAL	MAXIMUM		MAXIMUM	
10k-20MHz	12k-20MHz	10k-100MHz	Integer divider DJ-unbound RJ 10k-20MHz	Fractional divider DJ 10k-40MHz RJ 10k-20MHz
0.27 ps-rms (Integer division) 0.7ps-rms (fractional div)	0.3 ps-rms (int div) (1)	0.625 ps-rms (int div)	20 ps-pp (2)	50-220 ps-pp, see Figure 3

(1) Integrated Phase Noise (12kHz - 20 MHz) for 156.25 MHz output clock measured at room temperature using a 25 MHz Low Noise reference source
(2) T_J = 20 ps_{pp} applies for LVPECL, CML, and LVDS signaling. T_J lab characterization measured 8 ps_{pp}, (typical) and 12 ps_{pp} (max) over PVT.

Table 2. Jitter Cleaner Mode (Loop filter BW < 1 kHz)

RANDOM JITTER (ALL OUTPUTS)			TOTAL JITTER	
TYPICAL	MAXIMUM		MAXIMUM	
10k-20MHz	10k-20MHz	10k-100MHz	Integer divider DJ unbound RJ 10k-20MHz	Fractional divider DJ 10k-40MHz RJ 10k-20MHz
1.6 ps-rms (Integer division) 2.3 ps-rms (fractional div) 10k-20MHz	2.1 ps-rms (int div)	2.14 ps-rms (int div)	40 ps-pp	70-240 ps-pp, see Figure 3

Spurious Performance: The spurious performance is as follows:

- Less than -80 dBc spurious from PFD/reference clocks at 122.88 MHz output frequency in the Nyquist range.
- Less than -68 dBc spurious from output channel-to-channel coupling on the victim output at differential signaling level operated at 122.88 MHz output frequency in the Nyquist range.

Device outputs:

The Device outputs offer multiple signaling formats: high-swing CML (LVPECL like), normal-swing CML (CML), low-swing CML (LVDS like), HCSL, and LVCMOS signaling.

Table 3. Device Outputs

Outputs	LVPECL	CML	LVDS	HCSL	LVCMOS	OUTPUT DIVIDER	FREQUENCY RANGE
Y[3:0]	X	X	X			Integer only	1.55 - 800 MHz
Y[7:4]			X	X	X	Integer	1.55 - 800 MHz
						Fractional	1.00 - 400 MHz

Outputs [Y0:Y3] are driven by 8-b continuous integer dividers per pair. Outputs [Y4:Y7] are each driven by 20-b fractional dividers that can achieve any frequency with better than 1ppm frequency accuracy. The output skew is typically less than 40 ps for differential outputs. The LVCMOS outputs support adjustable slew rate control to control EMI. Pairs of 2 outputs can be operated at 1.8 V, 2.5 V or 3.3 V power supply voltage.

Device Configuration:32 distinct pin modes are available that cover many common use cases without the need for any serial programming of the device. For maximum flexibility the device also supports SPI and I^2C programming. I^2C offers 4 distinct addresses to support up to 4 devices on the same programming lines.

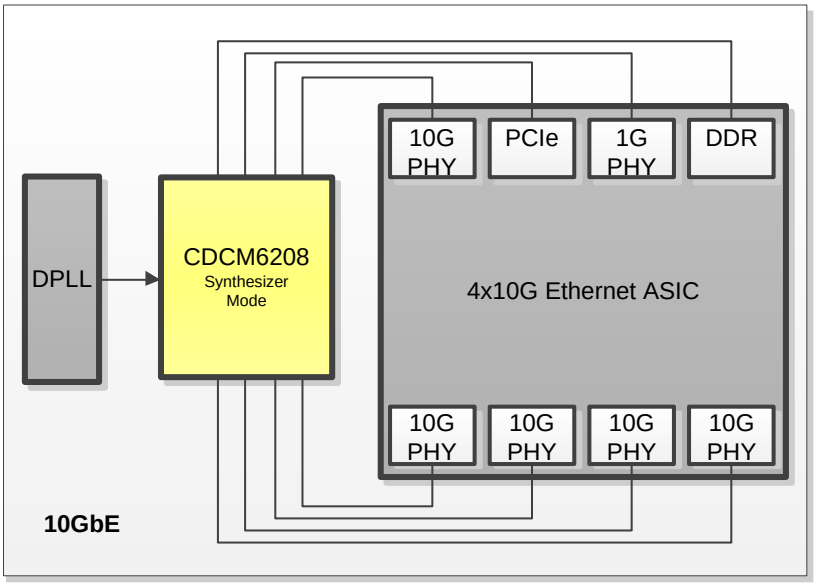


Figure 26. Typical Use Case: CDCM6208V2G Example in Wireless Infrastructure Baseband Application

10.4 Device Functional Modes

10.4.1 Control Pins Definition

In the absence of a host interface, the CDCM6208V2G can be powered up in one of 32 pre-configured settings when the pins are SI_MODE[1:0] = 10. The CDCM6208V2G has 5 control pins identified to achieve commonly used networking frequencies, and change output types. The Smart Input MUX for the PLL is set in most configurations to manual mode in pin mode. Based on the control pins settings for the on-chip PLL, the device generates the appropriate frequencies and appropriate output signaling types at start-up. In the case of the PLL loop filter, "JC" denotes PLL bandwidths of ≤ 1 kHz and "Synth" denotes PLL bandwidths of ≥ 100 kHz.

Table 4. Pre-Configured Settings of CDCM6208V2G Accessible by PIN[4:0](1) (2)

SI_MODE[1:0]	PIN[4:0]	Use Case	fin(PRI_REF)	Type	fin(SEC_REF)	Type2	REF_SEL	f(PFD)	f(VCO)	fout(Y0)	TYPE(Y0)	fout(Y1)	Type(Y1)	fout(Y2)	Type(Y2)	fout(Y3)	Type(Y3)	fout(Y4)	Type(Y4)	fout(Y5)	Type(Y5)	fout(Y6)	Type(Y6)	fout(Y7)	Type(Y7)
00	I/O	SPI Default	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	25	HCSL	125	HCSL	100	HCSL	133.333333	LVCMOS-P
01	I/O	I2C Default	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	25	HCSL	125	HCSL	100	HCSL	133.333333	LVCMOS-P
11	RESERVED																								
10	0x00	1-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	25	HCSL	125	HCSL	100	HCSL	133.333333	LVCMOS-P
10	0x01	2-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	100	HCSL	125	HCSL	100	HCSL	133.333333	LVCMOS-P
10	0x02	3-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	25	HCSL	125	HCSL	100	HCSL	133.333333	HCSL
10	0x03	4-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	100	HCSL	125	HCSL	100	HCSL	133.333333	HCSL
10	0x04	5-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	25	HCSL	125	HCSL	100	HCSL	133.333333	LVCMOS-P
10	0x05	6-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	25	HCSL	125	HCSL	100	HCSL	133.333333	LVCMOS-P
10	0x06	7-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	25	HCSL	125	HCSL	100	HCSL	133.333333	LVCMOS-P
10	0x07	8-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	25	HCSL	125	HCSL	100	HCSL	133.333333	LVCMOS-P
10	0x08	9-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	25	HCSL	125	HCSL	100	HCSL	133.333333	LVCMOS-P
10	0x09	10-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	25	HCSL	125	HCSL	100	HCSL	133.333333	LVCMOS-P
10	0x0A	11-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	3000	100	PECL	100	PECL	100	PECL	100	PECL	25	HCSL	125	HCSL	100	HCSL	133.333333	LVCMOS-P
10	0x0B	12-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	300	LVDS	300	LVDS	300	LVDS	X	Disable	X	Disable	X	Disable	X	Disable	X	Disable
10	0x0C	13-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	100	CML	100	CML	X	Disable	X	Disable	25	LVCMOS-PN	50	LVCMOS-P	148.499954	LVCMOS-PN	74.249 9773	LVDS
10	0x0D	14-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	100	CML	100	CML	X	Disable	X	Disable	25	LVCMOS-PN	50	LVCMOS-P	148.499954	LVCMOS-PN	74.249 9773	LVDS
10	0x0E	15-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	100	CML	100	CML	X	Disable	X	Disable	25	LVCMOS-P	19.2	LVCMOS-P	X	Disable	X	Disable
10	0x0F	16-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	X	Disable	100	CML	X	Disable	X	Disable	X	Disable	19.2	LVCMOS-P	32.768	LVCMOS-P	X	Disable

(1) The functionality of the status 0 and status 1 pins in SPI and I^2C mode is programmable.
(2) The REF_SEL input pin selects the primary or secondary input in MANUAL mode. That is: If the system only uses a XTAL on the secondary input, REF_SEL should be tied to VDD. The primary and secondary input stage power supply must be always connected.
For all pin modes, STATUS0 outputs the PLL_LOCK signal and STATUS1 the LOSS OF REFERENCE.
General Note: in all pin mode, all voltage supplies must either be 1.8 V or 2.5/3.3 V and the PWR pin number 44 must be set to 0 or 1 accordingly. In SPI and I2C mode, the supply voltages can be "mixed and matched" as long as the corresponding register bits reflect the supply voltage setting for each desired 1.8 V or 2.5/3.3 V supply. Exception: inputs configured for LVDS signaling (Type = LVDS) are supply agnostic, and therefore can be powered from 2.5 V/3.3 V or 1.8 V regardless of the supply select setting of pin number 44.

Table 4. Pre-Configured Settings of CDCM6208V2G Accessible by PIN[4:0](1) (2) (continued)

SI_MODE[1:0]	PIN[4:0]	Use Case	fin(PRI_REF)	Type	fin(SEC_REF)	Type2	REF_SEL	f(PFD)	f(VCO)	fout(Y0)	TYPE(Y0)	fout(Y1)	Type(Y1)	fout(Y2)	Type(Y2)	fout(Y3)	Type(Y3)	fout(Y4)	Type(Y4)	fout(Y5)	Type(Y5)	fout(Y6)	Type(Y6)	fout(Y7)	Type(Y7)
10	0x10	17-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	100	CML	100	CML	X	Disable	X	Disable	25	LVCM OS-PN	50	LVCM OS-P	148.49 9954	LVCM OS-PN	74.499 9874	LVDS
10	0x11	18-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	100	CML	100	CML	X	Disable	X	Disable	25	LVCM OS-PN	50	LVCM OS-P	148.49 9954	LVCM OS-PN	74.499 9874	LVDS
10	0x12	19-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	100	CML	X	Disable	X	Disable	X	Disable	X	Disable	24	LVCM OS-P	X	Disable	X	Disable
10	0x13	20-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	100	CML	X	Disable	X	Disable	X	Disable	25	LVCM OS-P	26.000 846	LVCM OS-P	12.000 0117	LVCM OS-P	X	Disable
10	0x14	21-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	X	Disable	X	Disable	X	Disable	X	Disable	25	LVCM OS-P	26.000 846	LVCM OS-P	48.000 0468	LVDS	X	Disable
10	0x15	22-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	100	CML	X	Disable	X	Disable	X	Disable	25	LVCM OS-P	26.000 846	LVCM OS-P	12.000 0117	LVCM OS-P	X	Disable
10	0x16	23-V2G	X	Disable	25	Crystal	MAN-SEC	25	3000	X	Disable	X	Disable	X	Disable	X	Disable	25	LVCM OS-P	26.000 846	LVCM OS-P	48.000 0468	LVDS	X	Disable
10	0x17	24-V2G	25	LVCM OS	25	Crystal	MAN-SEC	6.25	3125	156.25	LVDS	156.25	LVDS	156.25	LVDS	X	Disable	25	LVCM OS-PN	100	LVDS	100	LVDS	100	LVDS
10	0x18	25-V2G	125	CML	25	LVCM OS	MAN-SEC	6.25	3125	156.25	LVDS	156.25	LVDS	156.25	LVDS	X	Disable	52.992 415	LVDS	52.992 415	LVDS	52.992 415	LVDS	52.992 415	LVDS
10	0x19	26-V2G	35.328	LVCM OS	35.328	Crystal	MAN-SEC	35.328	2967.5 52	52.992	LVDS	52.992	LVDS	52.992	LVDS	X	Disable	24.999 7799	LVCM OS-PN	156.25 1195	LVDS	156.25 1195	LVDS	156.25 1195	LVDS
10	0x1A	27-V2G	35.328	LVCM OS	35.328	Crystal	MAN-SEC	35.328	2967.5 52	52.992	LVDS	52.992	LVDS	52.992	LVDS	52.992	LVDS	24.999 7799	LVCM OS-PN	156.25 1195	LVDS	156.25 1195	LVDS	156.25 1195	LVDS
10	0x1B	28-V2G	0.192	LVCM OS	0.192	LVCM OS	MAN-SEC	0.192	2967.5 52	52.992	LVDS	52.992	LVDS	52.992	LVDS	X	Disable	24.999 779913 1236	LVCM OS-PN	156.25 1195	LVDS	156.25 1195	LVDS	156.25 1195	LVDS
10	0x1C	29-V2G	25	LVCM OS	25	Crystal	MAN-SEC	25	3125	156.25	LVDS	156.25	LVDS	156.25	CML	X	Disable	X	Disable	125	LVCM OS-P	200	LVDS	25	LVCM OS-PN
10	0x1D	30-V2G	50	LVCM OS	50	Crystal	MAN-SEC	25	3125	156.25	LVDS	156.25	LVDS	156.25	CML	X	Disable	50	LVCM OS-P	125	LVCM OS-P	200	LVDS	25	LVCM OS-PN
10	0x1E	31-V2G	50	LVCM OS	25	Crystal	MAN-SEC	25	3125	156.25	LVDS	156.25	LVDS	156.25	CML	156.25	CML	156.25	HCSL	125	LVCM OS-P	200	LVDS	25	LVCM OS-PN
10	0x1F	32-V2G	50	LVCM OS	25	Crystal	MAN-SEC	25	3125	156.25	LVDS	156.25	LVDS	156.25	CML	156.25	CML	156.25	HCSL	125	LVCM OS-P	200	LVDS	25	LVCM OS-PN

10.4.2 Loop Filter Recommendations for Pin Modes

The following two tables provide the internal charge pump and R3/C3 settings for pin modes. The designer can either design their own optimized loop filter, or use the suggested loop filter in the Table 5.

Table 5. CDCM6208V2G Loop Filter Recommendation for Pin Mode

SI_MODE[1:0]	PIN[4:0]	Use Case	PRI_REF		SEC_REF		REF_SEL	f(PFD) (MHz)	ICP (mA)	Recommended External LPF Components C1 / R2 / C2	Internal LPF Components	
			Freq (MHz)	Type	Freq (MHz)	Type					R3 (Ω)	C3 (pF)
00	I/O	SPI Default	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
01	I/O	I2C Default	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
11	RESERVED											
10	0x00	1-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x01	2-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x02	3-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x03	4-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x04	5-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x05	6-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x06	7-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x07	8-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x08	9-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x09	10-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x0A	11-V2G	25	LVCMOS	25	LVCMOS	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x0B	12-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x0C	13-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x0D	14-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x0E	15-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x0F	16-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x10	17-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x11	18-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x12	19-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x13	20-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x14	21-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x15	22-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x16	23-V2G	X	Disable	25	Crystal	MAN-SEC	25	2.5	200pF / 400Ω / 22nF	100	242.5
10	0x17	24-V2G	25	LVCMOS	25	Crystal	MAN-SEC	6.25	4m	22pF / 860Ω / 22nF	100	242.5

Table 5. CDCM6208V2G Loop Filter Recommendation for Pin Mode (continued)

SI_MODE[1:0]	PIN[4:0]	Use Case	PRI_REF		SEC_REF		REF_SEL	f(PFD) (MHz)	ICP (mA)	Recommended External LPF Components C1 / R2 / C2	Internal LPF Components	
			Freq (MHz)	Type	Freq (MHz)	Type					R3 (Ω)	C3 (pF)
10	0x18	25-V2G	125	CML	25	LVCMOS	MAN-SEC	6.25	4m	22pF / 860Ω / 22nF	100	242.5
10	0x19	26-V2G	35.328	LVCMOS	35.328	Crystal	MAN-SEC	35.328	2.5m	22pF / 400Ω / 22nF	100	242.5
10	0x1A	27-V2G	35.328	LVCMOS	35.328	Crystal	MAN-SEC	35.328	2.5m	22pF / 400Ω / 22nF	100	242.5
10	0x1B	28-V2G	0.192	LVCMOS	0.192	LVCMOS	MAN-SEC	0.192	3.5m	100pF / 2.67kΩ / 6.8nF	100	242.5
10	0x1C	29-V2G	25	LVCMOS	25	Crystal	MAN-SEC	25	2.5m	100pF / 470Ω / 22nF	100	242.5
10	0x1D	30-V2G	50	LVCMOS	50	Crystal	MAN-SEC	25	2.5m	100pF / 470Ω / 22nF	100	242.5
10	0x1E	31-V2G	50	LVCMOS	50	Crystal	MAN-SEC	25	2.5m	100pF / 470Ω / 22nF	100	242.5
10	0x1F	32-V2G	50	LVCMOS	50	Crystal	MAN-SEC	25	2.5m	100pF / 470Ω / 22nF	100	242.5

10.4.3 Status Pins Definition

The device vitals such as input signal quality, smart mux input selection, and PLL lock can be monitored by reading device registers or at the status pins STATUS1, and STATUS0. Register 3[12:7] allows for customization of which vitals are mapped to these two pins. Table 6 lists the three events that can be mapped to each status pin and which can also be read in the register space.

Table 6. CDCM6208V2G Status Pin Definition List

STATUS SIGNAL NAME	SIGNAL TYPE	SIGNAL NAME	REGISTER BIT NO.	DESCRIPTION
SEL_REF	LVCMOS	STATUS0, 1	Reg 3.12 Reg 3.9	Indicates Reference Selected for PLL: 0 → Primary input selected to drive PLL 1 → Secondary input selected to drive PLL
LOS_REF	LVCMOS	STATUS0, 1	Reg 3.11 Reg 3.8	Loss of selected reference input observed at active input: 0 → Reference input present 1 → Loss of reference input Important Note 1: *For LOS_REF to operate properly, the secondary input SEC_IN must be enabled. Set register Q4.5=1. If register Q4.5 is set to zero, LOS_REF will output a static high signal regardless of the actual input signal status on PRI_IN.*
PLL_UNLOCK	LVCMOS	STATUS0, 1	Reg 3.10 Reg 3.7	Indicates unlock status for PLL (digital): PLL locked → Q21.02 = 0 and $V_{STATUS0/1}$= V_{IH} PLL unlocked → Q21.2 = 1 and $V_{STATUS0/1}$= V_{IL}See note (1) Note 2: I *f the smartmux is enabled and both reference clocks stall, the STATUSx output signal will 98% of the time indicate the LOS condition with a static high signal. However, in 2% of the cases, the LOS detection engine erroneously stalls at a state where the STATUSx output PLL lock indicator will signalize high for 511 out of every 512 PFD clock cycles.*

(1) The reverse logic between the register Q21.2 and the external output signal on STATUS0 or STATUS1.

NOTE

It is recommended to assert only one out of the three register bits for each of the status pins. For example, to monitor the PLL lock status on STATUS0 and the selected reference clock sources on STATUS1 output, the device register settings would be Q3.12 = Q3.7 = 1 and Q3.11 = Q3.10 = Q3.9 = Q3.8 = 0. If a status pin is unused, it is recommended to set the according 3 register bits to zero (e.g. Q3[12:9] = 0 for STATUS0 = 0). If more than one bit is enabled for each STATUS signal, the function becomes OR'ed. For example, if Q3.11 = Q3.10 = 1 and Q3.12 = 0, the STATUS0 output would be high either if the device goes out of lock or the selected reference clock signal is lost.

10.4.4 PLL Lock Detect

The PLL lock detection circuit is a digital detection circuit which detects any frequency error, even a single cycle slip. The PLL unlock is signalized when a certain number of cycle slips have been exceeded, at which point the counter is reset. A frequency error of 2% will cause PLL unlock to stay low. A 0.5% frequency error shows up as toggling the PLL lock output with roughly 50% duty cycle at roughly 1/1000 th of the PFD update frequency to the device. A frequency error of 1ppm would show up as rare toggling low for a duration of approximately 1000 PFD update clock cycles. If the system plans using PLL lock to toggle a system reset, then consider adding an RC filter on the PLL LOCK output (Status 1 or Status 0) to avoid rare cycle slips from triggering an entire system reset.

10.4.5 Interface and Control

The host (DSP, Microcontroller, FPGA, etc) configures and monitors the CDCM6208V2G via the SPI or I^{2}C port. The host reads and writes to a collection of control/status bits called the register file. Typically, a hardware block is controlled and monitored via a specific grouping of bits located within the register file. The host controls and monitors certain device-wide critical parameters directly, via control/status pins. In the absence of a host, the CDCM6208V2G can be configured to operate in pin mode where the control pins [PIN0-PIN4] can be set appropriately to generate the necessary clock outputs out of the device.

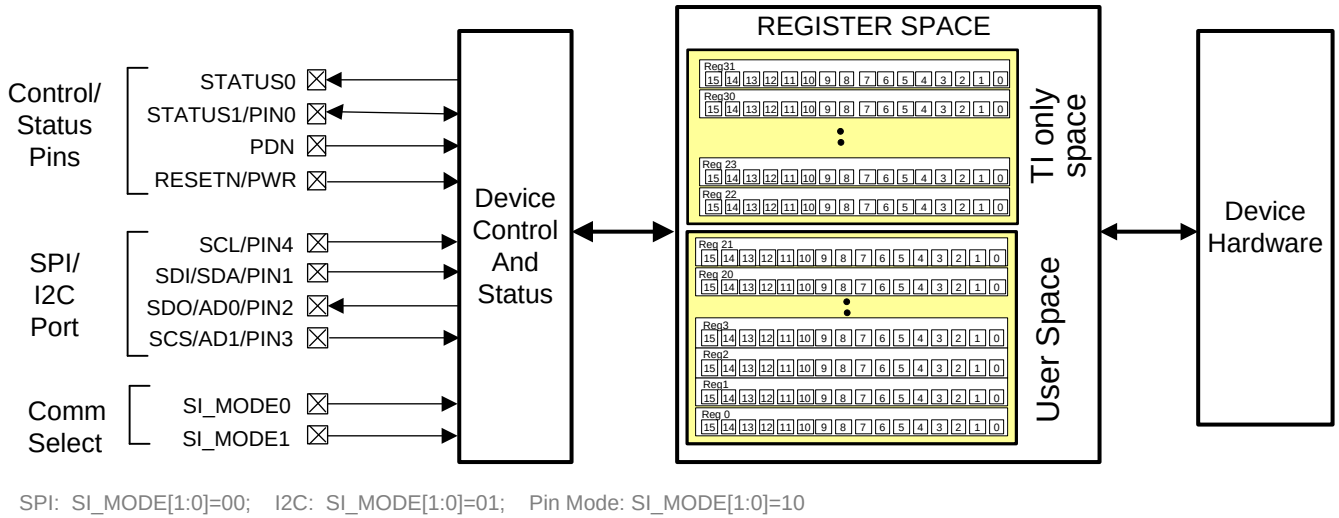


Figure 27. CDCM6208V2G Interface and Control Block

Within this register space, there are certain bits that have read/write access. Other bits are read-only (an attempt to write to a read only bit will not change the state of the bit).

10.4.5.1 Register File Reference Convention

Figure 28 shows the method this document employs to refer to an individual register bit or a grouping of register bits. If a drawing or text references an individual bit, the format is to specify the register number first and the bit number second. The CDCM6208V2G contains 21 registers that are 16 bits wide. The register addresses and the bit positions both begin with the number zero (0). A period separates the register address and bit address. The first bit in the register file is address 'R0.0' meaning that it is located in Register 0 and is bit position 0. The last bit in the register file is address R31.15 referring to the 16thbit of register address 31 (the 32ndregister in the device

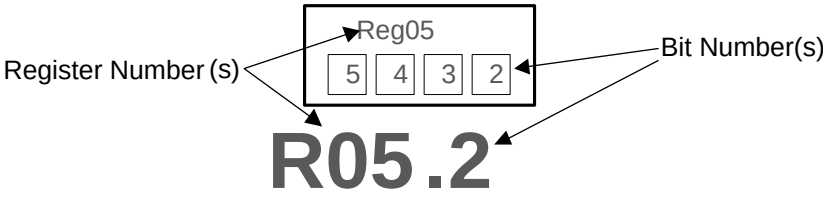


Figure 28. CDCM6208V2G Register Reference Format

10.4.5.2 SPI - Serial Peripheral Interface

To enable the SPI port, tie the communication select pins SI_MODE[1:0] to ground. SPI is a master/slave protocol in which the host system is always the master; therefore, the host always initiates communication to/from the device. The SPI interface consists of four signal pins. The device SPI address is 0000.

Table 7. Serial Port Signals in SPI Mode

PIN		I/O	DESCRIPTION
NAME	NUMBER		
SDI/SDA/PIN1	2	Input	SDI: SPI Serial Data Input
SDO/AD0/PIN2	3	Output	SDO: SPI Serial Data
SCS/AD1/PIN3	4	Input	SCS: SPI Latch Enable
SCL/PIN4	5	Input	SCL: SPI/I^{2}C Clock

The host must present data to the device MSB first. A message includes a transfer direction bit, an address field, and a data field as depicted in Figure 29

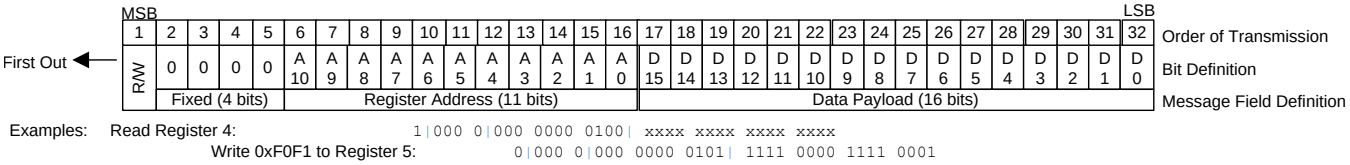


Figure 29. CDCM6208V2G SPI Message Format

10.4.5.2.1 Configuring the PLL

The CDCM6208V2G allows configuring the PLL to accommodate various input and output frequencies either through an I^{2}C or SPI programming interface or in the absence of programming, the PLL can be configured through control pins. The PLL can be configured by setting the Smart Input MUX, Reference Divider, PLL Loop Filter, Feedback Divider, Prescaler Divider, and Output Dividers.

For the PLL to operate in closed loop mode, the following condition in Equation 2 has to be met when using primary input for the reference clock, and the condition in Equation 3 has to be met when using secondary input for the reference clock.

$$\frac{f_{PRI\_REF}}{(M \times R)} = \frac{f_{VCO}}{(N \times PS\_A)} \quad (2)$$

$$\frac{f_{SEC\_REF}}{M} = \frac{f_{VCO}}{(N \times PS\_A)} \quad (3)$$

In Equation 2 and Equation 3, f_{PRI_REF} is the reference input frequency on the primary input and f_{SEC_REF} is the reference input frequency on the secondary input, *R* is the reference divider, *M* is the input divider, *N* is the feedback divider, and PS_A the prescaler divider A.

The output frequency, f_{OUT}, is a function of f_{VCO}, the prescaler A, and the output divider (O), and is given by Equation 4. (Use PS_B in for outputs 2, 3, 6, and 7).

$$f_{OUT} = \frac{f_{OSC}}{(O \times PS\_A)} \quad (4)$$

When the output frequency plan calls for the use of some output dividers as fractional values, the following steps are needed to calculate the closest achievable frequencies for those using fractional output dividers and the frequency errors (difference between the desired frequency and the closest achievable frequency).

- Based on system needs, decide the frequencies that need to have best possible jitter performance.
- Once decided, these frequencies need to be placed on integer output dividers.
- Then a frequency plan for these frequencies with strict jitter requirements can be worked out using the common divisor algorithm.
- Once the integer divider plans are worked out, the PLL settings (including VCO frequency, feedback divider, input divider and prescaler divider) can be worked out to map the input frequency to the frequency out of the prescaler divider.
- Then calculate the fractional divider values (whose values must be greater than 2) that are needed to support the output frequencies that are not part of the common frequency plan from the common divisor algorithm already worked out.
- For each fractional divider value, try to represent the fractional portion in a 20 bit binary scheme, where the first fractional bit is represented as 0.5, the second fractional bit is represented as 0.25, third fractional bit is represented as 0.125 and so on. Continue this process until the entire 20 bit fractional binary word is exhausted.
- Once exhausted, the fraction can be calculated as a cumulative sum of the fractional bit x fractional value of the fractional bit. Once this is done, the closest achievable output frequency can be calculated with the mathematical function of the frequency out of the prescaler divider divided by the achievable fractional divider.
- The frequency error can then be calculated as the difference between the desired frequency and the closest achievable frequency.

10.5 Programming

10.5.1 Writing to the CDCM6208V2G

To initiate a SPI data transfer, the host asserts the SCS (serial chip select) pin low. The first rising edge of the clock signal (SCL) transfers the bit presented on the SDI pin of the CDCM6208V2G. This bit signals if a read (first bit high) or a write (first bit low) will transpire. The SPI port shifts data to the CDCM6208V2G with each rising edge of SCL. Following the W/R bit are 4 fixed bits followed by 11 bits that specify the address of the target register in the register file. The 16 bits that follow are the data payload. If the host sends an incomplete message, (i.e. the host de-asserts the SCS pin high prior to a complete message transmission), then the CDCM6208V2G aborts the transfer, and device makes no changes to the register file or the hardware. Figure 31 shows the format of a write transaction on the CDCM6208V2G SPI port. The host signals the CDCM6208V2G of the completed transfer and disables the SPI port by de-asserting the SCS pin high.

Programming (continued)

10.5.2 Reading from the CDCM6208V2G

As with the write operation, the host first initiates a SPI transfer by asserting the SCS pin low. The host signals a read operation by shifting a logical high in the first bit position, signaling the CDCM6208V2G that the host is imitating a read data transfer from the device. During the portion of the message in which the host specifies the CDCM6208V2G register address, the host presents this information on the SDI pin of the device (for the first 15 clock cycles after the W/R bit). During the 16 clock cycles that follow, the CDCM6208V2G presents the data from the register specified in the first half of the message on the SDO pin. The SDO output is 3-stated anytime SCS is high, so that multiple SPI slave devices can be connected to the same serial bus. The host signals the CDCM6208V2G that the transfer is complete by de-asserting the SCS pin high.

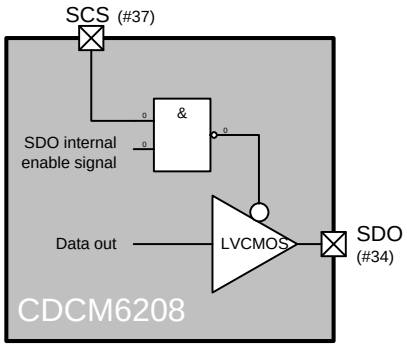


Figure 30.

10.5.3 Block Write/Read Operation

The device supports a block write and block read operation. The host need only specify the lowest address of the sequence of addresses that the host needs to access. The CDCM6208V2G will automatically increment the internal register address pointer if the SCS pin remains low after the SPI port finishes the initial 32-bit transmission sequence. Each transmission of 16 bits (a data payload width) results in the device automatically incrementing the address pointer (provided the SCS pin remains active low for all sequences).

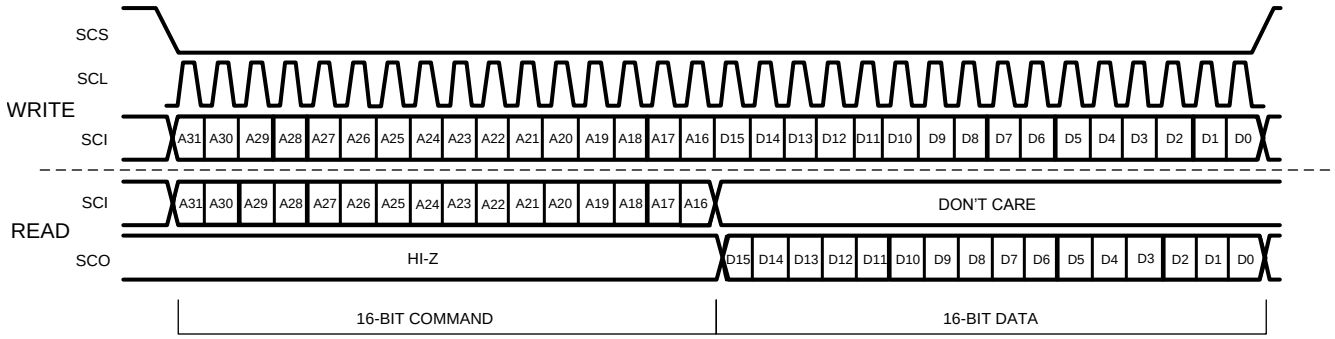


Figure 31. CDCM6208V2G SPI Port Message Sequencing

10.5.4 I^2C Serial Interface

With SI_MODE1=0 and SI_MODE0=1 the CDCM6208V2G enters I ^{2}C mode. The I^2C port on the CDCM6208V2G works as a slave device and supports both the 100 kHz standard mode and 400 kHz fast mode operations. Fast mode imposes a glitch tolerance requirement on the control signals. Therefore, the input receivers ignore pulses of less than 50 ns duration. The inputs of the device also incorporates a Schmitt trigger at the SDA and SCL inputs to provide receiver input hysteresis for increased noise robustness.

NOTE

Communication through I^2C is not possible while RESETN is held low.

Programming (continued)

In an I^{2}C bus system, the CDCM6208V2G acts as a slave device and is connected to the serial bus (data bus SDA and clock bus SCL). The SDA port is bidirectional and uses an open drain driver to permit multiple devices to be connected to the same serial bus. The CDCM6208V2G allows up to four unique CDCM6208V2G slave devices to occupy the I^{2}C bus in addition to any other I^{2}C slave device with a different I^{2}C address. These slave devices are accessed via a 7-bit slave address transmitted as part of an I^{2}C packet. Only the device with a matching slave address responds to subsequent I^{2}C commands. The device slave address is 10101xx (the two LSBs are determined by the AD1 and AD0 pins). The five MSBs are hard-wired, while the two LSBs are set through pins on device powerup.

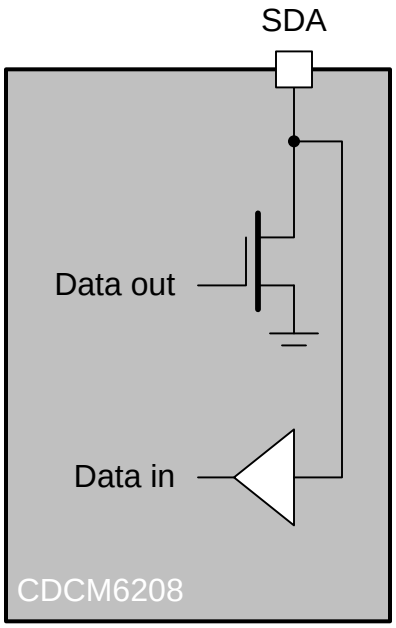


Figure 32.

During the data transfer through the I^{2}C port interface, one clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low. The start data transfer condition is characterized by a high-to-low transition on the SDA line while SCL is high. The stop data transfer condition is characterized by a low-to-high transition on the SDA line while SCL is high. The start and stop conditions are always initiated by the master. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit and bytes are sent MSB first.

The acknowledge bit (A) or non-acknowledge bit (A) is the 9thbit attached to any 8-bit data byte and is always generated by the receiver to inform the transmitter that the byte has been received (when A = 0) or not (when A = 1). A = 0 is done by pulling the SDA line low during the 9thclock pulse and A = 1 is done by leaving the SDA line high during the 9thclock pulse.

The I^{2}C master initiates the data transfer by asserting a start condition which initiates a response from all slave devices connected to the serial bus. Based on the 8-bit address byte sent by the master over the SDA line (consisting of the 7-bit slave address (MSB first) and an R/W bit), the device whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data transfer with the master. The CDCM6208V2G slave address bytes are given in below table.

After the data transfer has occurred, stop conditions are established. In write mode, the master asserts a stop condition to end data transfer during the 10 thclock pulse following the acknowledge bit for the last data byte from the slave. In read mode, the master receives the last data byte from the slave but does not pull SDA low during the 9thclock pulse. This is known as a non-acknowledge bit. By receiving the non-acknowledge bit, the slave knows the data transfer is finished and enters the idle mode. The master then takes the data line low during the low period before the 10 thclock pulse, and high during the 10 thclock pulse to assert a stop condition.

Programming (continued)

For "Register Write/Read" operations, the I^2C master can individually access addressed registers, that are made of two 8-bit data bytes.

Table 8. I^2C Slave Address Byte

A6	A5	A4	A3	A2	AD1	AD0	R/W
1	0	1	0	1	0	0	1/0
1	0	1	0	1	0	1	1/0
1	0	1	0	1	1	0	1/0
1	0	1	0	1	1	1	1/0

Table 9. Generic Programming Sequence

S	Start Condition
Sr	Repeated Condition
R/$\overline{W}$	1 = Read (Rd) from slave; 0 = Write (Wr) to slave
A	Acknowledge (ACK = 0 and NACK = 1)
P	Stop Condition
	Master to Slave Transmission
	Slave to Master Transmission

Figure 33. Register Write Programming Sequence

1	7	1	1	8	1	8	1	8	1	8	1	1
S	SLAVE Address	Wr	A	Register Address	A	Register Address	A	Data Byte	A	Data Byte	A	P

Figure 34. Register Read Programming Sequence

1	7	1	1	8	1	8	1	1	1	1	1	8	1	8	1	1
S	SLAVE Address	Wr	A	Register Address	A	Register Address	A	S	Slave Address	Rd	A	Data Byte	A	Data Byte	A	P

10.6 Register Maps

In SPI/I^{2}C mode the device can be configured through twenty registers. Register 4 configures the input, Reg 0-3 the PLL and dividers, and Register 5 - 20 configures the 8 different outputs.

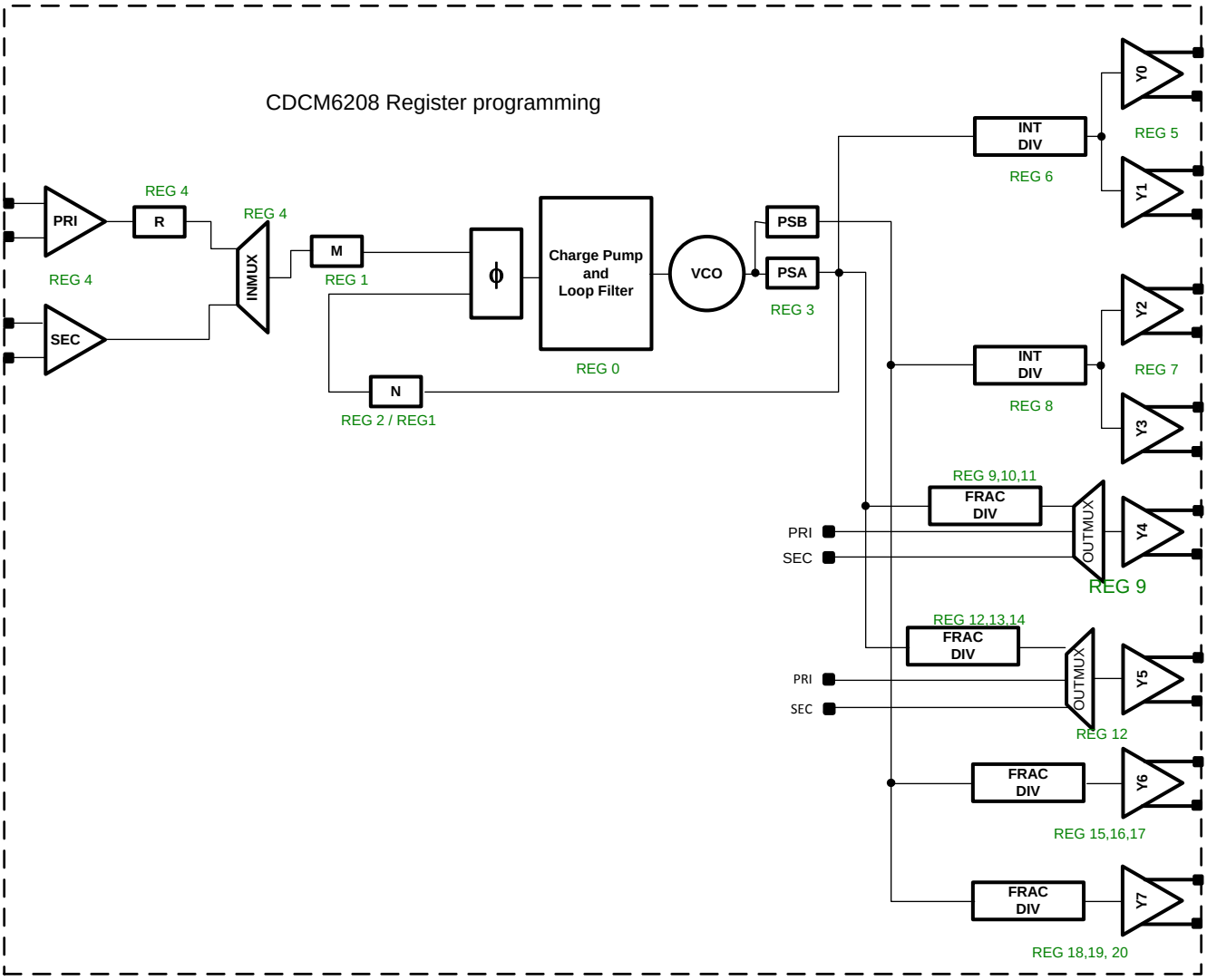


Figure 35. Device Register Map

Register Maps (continued)

Table 10. Register 0

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15:10	RESERVED		These bits must be set to 0
9:7	LF_C3[2:0]	PLL Internal Loop Filter (C3)	PLL Internal Loop Filter Capacitor (C3) Selection 000 → 35 pF 001→ 112.5 pF 010 → 177.5 pF 011 → 242.5 pF 100 → 310 pF 101 → 377.5 pF 110 → 445 pF 111 → 562.5 pF
6:4	LF_R3[2:0]	PLL Internal Loop Filter (R3)	PLL Internal Loop Filter Resistor (R3) Selection 000 → 10 Ω 001 → 30 Ω 010 → 60 Ω 011 → 100 Ω 100 → 530 Ω 101→ 1050 Ω 110 → 2080 Ω 111 → 4010 Ω
3:1	PLL_ICP[2:0]	PLL Charge Pump	PLL Charge Pump Current Setting 000 → 500 µA 001 → 1.0 mA 010 → 1.5 mA 011 → 2.0 mA 100 → 2.5 mA 101 → 3.0 mA 110 → 3.5 mA 111→ 4.0 mA
0	RESERVED		This bit is tied to zero statically, and it is recommended to set to 0 when writing to register.

Table 11. Register 1

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15:2	PLL_REFDIV[13:0]	PLL Reference Divider	PLL Reference 14-b Divider Selection (Divider value is register value +1)
1:0	PLL_FBDIV1[9:8]	PLL Feedback Divider 1	PLL Feedback 10-b Divider Selection, Bits 9:8

Table 12. Register 2

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15:8	PLL_FBDIV1[7:0]	PLL Feedback Divider 1	PLL Feedback 10-b Divider Selection, Bits 7:0 (Divider value is register value +1)
7:0	PLL_FBDIV0[7:0]	PLL Feedback Divider 0	PLL Feedback 8-b Divider Selection (Divider value is register value +1)

Table 13. Register 3

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15:13	RESERVED		These bits must be set to 0
12	ST1_SEL_REFCLK	Device Status	Reference clock status enable on Status 1 pin: 0 → Disable 1 → Enable (See Table 6 for full description)
11	ST1_LOR_EN		Loss-of-reference Enable on Status 1 pin: 0 → Disable" 1 → Enable (See Table 6 for full description)
10	ST1_PLLLOCK_EN		PLL Lock Indication Enable on Status 1 pin: 0 → Disable 1 → Enable (See Table 6 for full description)
9	ST0_SEL_REFCLK		Reference clock status enable on Status 0 pin: 0 → Disable 1 → Enable (See Table 6 for full description)
8	ST0_LOR_EN		Loss-of-reference Enable on Status 0 pin: 0 → Disable 1 → Enable (See Table 6 for full description)
7	ST0_PLLLOCK_EN		PLL Lock Indication Enable on Status 0 pin:" 0 → Disable 1 → Enable (See Table 6 for full description)
6	RSTN	Device Reset	Device Reset Selection: 0 → Device In Reset (retains register values) 1 → Normal Operation
5	SYNCN	Output Divider	Output Channel Dividers Synchronization Enable: 0 → Forces synchronization 1 → Exits synchronization
4	ENCAL	PLL/VCO	PLL/VCO Calibration Enable: 0 → Disable 1 → Enable
3:2	PS_B[1:0]	PLL Prescaler Divider B	PLL Prescaler 1 Integer Divider Selection: 00 → Divide-by-4 01→ Divide-by-5 10 → Divide-by-6 11 → RESERVED used for Y2, Y3, Y6, and Y7
1:0	PS_A[1:0]	PLL Prescaler Divider A	PLL Prescaler 0 Integer Divider Selection: 00 → Divide-by-4 01 → Divide-by-5 10 → Divide-by-6 11 → RESERVED used in PLL feedback, Y0, Y1, Y4, and Y5

Table 14. Register 4

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15:14	SMUX_PW[1:0]	Reference Input Smart MUX	Smart MUX Pulse Width Selection. This bit controls the Smart MUX delay and waveform reshaping. 00 → PLL Smart MUX Clock Delay and Reshape Disabled (default in all pin modes) 01 → PLL Smart MUX Clock Delay Enable 10 → PLL Smart MUX Clock Reshape Enable 11 → PLL Smart MUX Clock Delay and Reshape Enable
13	SMUX_MODE_SEL		Smart MUX Mode Selection: 0 → Auto select 1 → Manual select Note: in Auto select mode, both input buffers must be enabled. Set R4.5 = 1 and R4.2 = 1
12	SMUX_REF_SEL		Smart MUX Selection for PLL Reference: 0 → Primary 1 → Secondary (only if REF_SEL pin is high) This bit is ignored when smartmux is set to auto select (e.g. R4.13 = 0). See Table 6 for details.
11:8	CLK_PRI_DIV[3:0]	Primary Input Divider	Primary Input (R) Divider Selection: 0000 → Divide by 1 1111 → Divide by 16
7:6	SEC_SELBUF[1:0]	Secondary Input	Secondary Input Buffer Type Selection: 00 → CML 01 → LVDS 10 → LVCMOS 11 → Crystal
5	EN_SEC_CLK		Secondary input enable: 0 → Disable 1 → Enable
4:3	PRI_SELBUF[1:0]	Primary Input	Primary Input Buffer Type Selection: 00 → CML 01 → LVDS 10 → LVCMOS 11 → LVCMOS
2	EN_PRI_CLK		Primary input enable: 0 → Disable 1 → Enable
1	SEC_SUPPLY (1)	Secondary Input	Supply voltage for secondary input: 0 → 1.8 V 1 → 2.5/3.3 V
0	PRI_SUPPLY (2)	Primary Input	Supply voltage for primary input: 0 → 1.8 V 1 → 2.5/3.3 V

(1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0. To ensure best device performance this registers should be updated after power-up to reflect the true VDD_SEC supply voltage used.
(2) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0. To ensure best device performance this registers should be updated after power-up to reflect the true VDD_PRI supply voltage used.

Table 15. Register 5

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14	RESERVED		This bit must be set to 0
13	RESERVED		This bit must be set to 0
12	RESERVED		This bit must be set to 0
11	RESERVED		This bit must be set to 0
10	RESERVED		This bit must be set to 0
9	RESERVED		This bit must be set to 0
8:7	SEL_DRVR_CH1[1:0]	Output Channel 1	Output Channel 1 Type Selection: 00, 01 → LVDS 10 → CML 11 → PECL
6:5	EN _CH1[1:0]		Output channel 1 enable: 00 → Disable 01 → Enable 10 → Drive static 0 11 → Drive static 1
4:3	SEL_DRVR_CH0[1:0]	Output Channel 0	Output Channel 0 Type Selection: 00, 01 → LVDS 10 → CML 11 → PECL
2:1	EN_CH0[1:0]		Output channel 0 enable: 00 → Disable 01 → Enable 10 → Drive static 0 11 → Drive static 1
0	SUPPLY_CH0_1 (1)	Output Channels 0 and 1	Output Channels 0 and 1 Supply Voltage Selection: 0 → 1.8 V 1 → 2.5/3.3 V

(1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0 and to update this bit thereafter.

Table 16. Register 6

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14	RESERVED		This bit must be set to 0
13	RESERVED		This bit must be set to 0
12	RESERVED		This bit must be set to 0
11	RESERVED		This bit must be set to 0
10	RESERVED		This bit must be set to 0
9	RESERVED		This bit must be set to 0
8	RESERVED		This bit must be set to 0
7:0	OUTDIV0_1[7:0]	Output Channels 0 and 1	Output channels 0 and 1 8-b output integer divider setting (Divider value is register value +1)

Table 17. Register 7

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14	RESERVED		This bit must be set to 0
13	RESERVED		This bit must be set to 0
12	RESERVED		This bit must be set to 0
11	RESERVED		This bit must be set to 0
10	RESERVED		This bit must be set to 0
9	RESERVED		This bit must be set to 0
8:7	SEL_DRVR_CH3[1:0]	Output Channel 3	Output Channel 3 Type Selection: 00, 01 → LVDS 10 → CML 11 → PECL
6:5	EN_CH3[1:0]		Output channel 3 enable: 00 → Disable 01 → Enable 10 → Drive static 0 11 → Drive static 1
4:3	SEL_DRVR_CH2[1:0]	Output Channel 2	Output Channel 2 Type Selection: 00, 01 → LVDS 10 → CML" 11 → PECL
2:1	EN_CH2[1:0]		Output channel 2 enable: 00 → Disable 01 → Enable 10 → Drive static 0 11 → Drive static 1
0	SUPPLY_CH2_3 (1)	Output Channels 2 and 3	Output Channels 2 and 3 Supply Voltage Selection: 0 → 1.8 V 1 → 2.5/3.3 V

(1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0 and to update this bit thereafter.

Table 18. Register 8

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14	RESERVED		This bit must be set to 0
13	RESERVED		This bit must be set to 0
12	RESERVED		This bit must be set to 0
11	RESERVED		This bit must be set to 0
10	RESERVED		This bit must be set to 0
9	RESERVED		This bit must be set to 0
8	RESERVED		This bit must be set to 0
7:0	OUTDIV2_3[7:0]	Output Channels 2 and 3	Output channels 2 and 3 8-b output integer divider setting (Divider value is register value +1)

Table 19. Register 9

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14:13	OUTMUX_CH4[1:0]	Output Channel 4	Output MUX setting for output channel 4: 00 and 11 → PLL 01 → Primary input 10 → Secondary input
12:10	PRE_DIV_CH4[2:0]		Output channel 4 fractional divider's 3-b pre-divider setting (this pre-divider is bypassed if Q9.9 = 0) 000 → Divide by 2 001 → Divide by 3 111 → Divide by 1 All other combinations reserved
9	EN_FRACDIV_CH4		Output channel 4 fractional divider enable: 0 → Disable 1 → Enable
8	LVCMOS_SLEW_CH4		Output channel 4 LVCMOS output slew: 0 → Normal 1 → Slow
7	EN_LVCMOS_N_CH4		Output channel 4 negative-side LVCMOS enable: 0 → Disable 1 → Enable (Negative side can only be enabled if positive side is enabled)
6	EN_LVCMOS_P_CH4		Output channel 4 positive-side LVCMOS enable: 0 → Disable 1 → Enable
5	RESERVED		This bit must be set to 0
4:3	SEL_DRVR_CH4[2:0]		Output channel 4 type selection: 00 or 01 → LVDS 10 → LVCMOS 11 → HCSL
2:1	EN_CH4[1:0]		Output channel 4 enable: 00 → Disable 01 → Enable 10 → Drive static 0 11 → Drive static 1
0	SUPPLY_CH4 (1)		Output channel 4 Supply Voltage Selection: 0 → 1.8 V 1 → 2.5/3.3 V

(1) It is ok to power up the device with a 2.5 V / 3.3 V supply while this bit is set to 0 and to update this bit thereafter.

Table 20. Register 10

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14	RESERVED		This bit must be set to 0
13	RESERVED		This bit must be set to 0
12	RESERVED		This bit must be set to 0
11:4	OUTDIV4[7:0]	Output Channel 4	Output channel 4 8-b integer divider setting (Divider value is register value +1)
3:0	FRACDIV4[19:16]		Output channel 4 20-b fractional divider setting, bits 19 - 16

Table 21. Register 11

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15:0	FRACDIV4[15:0]	Output Channel 4	Output channel 4 20-b fractional divider setting, bits 15 - 0

Table 22. Register 12

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14:13	OUTMUX_CH5[1:0]	Output Channel 5	Output MUX setting for output channel 5: 00 and 11 → PLL 01 → Primary input 10 → Secondary input
12:10	PRE_DIV_CH5[2:0]		Output channel 5 fractional divider's 3-b pre-divider setting (this pre-divider is bypassed if Q12.9 = 0) 000 → Divide by 2 001 → Divide by 3 111 → Divide by 1 All other combinations reserved
9	EN_FRACDIV_CH5		Output channel 5 fractional divider enable: 0 → Disable 1 → Enable
8	LVCMOS_SLEW_CH5		Output channel 5 LVCMOS output slew: 0 → Normal 1 → Slow
7	EN_LVCMOS_N_CH5		Output channel 5 negative-side LVCMOS enable: 0 → Disable 1 → Enable (Negative side can only be enabled if positive side is enabled)
6	EN_LVCMOS_P_CH5		Output channel 5 positive-side LVCMOS enable: 0 → Disable 1 → Enable
5	RESERVED		This bit must be set to 0
4:3	SEL_DRVR_CH5[2:0]		Output channel 5 type selection: 00 or 01 → LVDS 10 → LVCMOS 11 → HCSL
2:1	EN_CH5[1:0]		Output channel 5 enable: 00 → Disable 01 → Enable 10 → Drive static 0 11 → Drive static 1
0	SUPPLY_CH5 (1)		Output channel 5Supply Voltage Selection: 0 → 1.8 V 1 → 2.5/3.3 V

(1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0 and to update this bit thereafter.

Table 23. Register 13

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14	RESERVED		This bit must be set to 0
13	RESERVED		This bit must be set to 0
12	RESERVED		This bit must be set to 0
11:4	OUTDIV5[7:0]	Output Channel 5	Output channel 5 8-b integer divider setting (Divider value is register value +1)
3:0	FRACDIV5[19:16]		Output channel 5 20-b fractional divider setting, bits 19-16

Table 24. Register 14

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15:0	FRACDIV5[15:0]	Output Channel 5	Output channel 5 20-b fractional divider setting, bits 15-0

Table 25. Register 15

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14	RESERVED		This bit must be set to 0
13	RESERVED		This bit must be set to 0
12:10	PRE_DIV_CH6[2:0]	Output Channel 6	Output channel 6 fractional divider's 3-b pre-divider setting (this pre-divider is bypassed if Q15.9 = 0) 000 → Divide by 2 001 → Divide by 3 111 → Divide by 1 All other combinations reserved
9	EN_FRACDIV_CH6		Output channel 6 fractional divider enable: 0 → Disable 1 → Enable
8	LVCMOS_SLEW_CH6		Output channel 6 LVCMOS output slew: 0 → Normal 1 → Slow
7	EN_LVCMOS_N_CH6		Output channel 6 negative-side LVCMOS enable: 0 → Disable 1 → Enable (Negative side can only be enabled if positive side is enabled)
6	EN_LVCMOS_P_CH6		Output channel 6 positive-side LVCMOS enable: 0 → Disable 1 → Enable
5	RESERVED		This bit must be set to 0
4:3	SEL_DRVR_CH6[1:0]		Output channel 6 type selection: 00 or 01 → LVDS 10 → LVCMOS 11 → HCSL
2:1	EN_CH6[1:0]		Output channel 6 enable: 00 → Disable 01 → Enable 10 → Drive static 0 11 → Drive static 1
0	SUPPLY_CH6 (1)		Output channel 6 Supply Voltage Selection: 0 → 1.8 V 1 → 2.5/3.3 V

(1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0 and to update this bit thereafter.

Table 26. Register 16

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14	RESERVED		This bit must be set to 0
13	RESERVED		This bit must be set to 0
12	RESERVED		This bit must be set to 0
11:4	OUTDIV6[7:0]	Output Channel 6	Output channel 6 8-b integer divider setting (Divider value is register value +1)
3:0	FRACDIV6[19:16]		Output channel 6 20-b fractional divider setting, bits 19-16

Table 27. Register 17

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15:0	FRACDIV6[15:0]	Output Channel 6	Output channel 6 20-b fractional divider setting, bits 15-0

Table 28. Register 18

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14	RESERVED		This bit must be set to 0
13	RESERVED		This bit must be set to 0
12:10	PRE_DIV_CH7[2:0]	Output Channel 7	Output channel 7 fractional divider's 3-b pre-divider setting (this pre-divider is bypassed if Q18.9 = 0) 000 → Divide by 2 001 → Divide by 3 111 → Divide by 1 All other combinations reserved
9	EN_FRACDIV_CH7		Output channel 7 fractional divider enable: 0 → Disable, 1 → Enable
8	LVCMOS_SLEW_CH7		Output channel 7 LVCMOS output slew: 0 → Normal, 1 → Slow
7	EN_LVCMOS_N_CH7		Output channel 7 negative-side LVCMOS enable: 0 → Disable, 1 → Enable (Negative side can only be enabled if positive side is enabled)
6	EN_LVCMOS_P_CH7		Output channel 7 positive-side LVCMOS enable: 0 → Disable, 1 → Enable
5	RESERVED		This bit must be set to 0
4:3	SEL_DRVR_CH7[2:0]		Output channel 7 type selection:00 or 01 → LVDS, 10 → LVCMOS, 11 → HCSL
2:1	EN_CH7[1:0]		Output channel 7 enable: 00 → Disable, 01 → Enable, 10 → Drive static low, 11 → Drive static high
0	SUPPLY_CH7 (1)		Output channel 7 Supply Voltage Selection: 0 → 1.8 V, 1 → 2.5/3.3 V

(1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0 and to update this bit thereafter.

Table 29. Register 19

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit must be set to 0
14	RESERVED		This bit must be set to 0
13	RESERVED		This bit must be set to 0
12	RESERVED		This bit must be set to 0
11:4	OUTDIV7[7:0]	Output Channel 7	Output channel 7 8-b integer divider setting (Divider value is register value +1)
3:0	FRACDIV7[19:16]		Output channel 7 20-b fractional divider setting, bits 19-16

Table 30. Register 20

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15:0	FRACDIV7[15:0]	Output Channel 7	Output channel 7 20-b fractional divider setting, bits 15-0

Table 31. Register 21 (Read Only)

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		This bit will read a 0
14	RESERVED		This bit will read a 0
13	RESERVED		This bit will read a 0
12	RESERVED		This bit will read a 0
11	RESERVED		This bit will read a 0
10	RESERVED		This bit will read a 0
9	RESERVED		This bit will read a 0
8	RESERVED		This bit will read a 0
7	RESERVED		This bit will read a 0
6	RESERVED		This bit will read a 0
5	RESERVED		This bit will read a 0
4	RESERVED		This bit will read a 0
3	RESERVED		This bit will read a 0
2	PLL_UNLOCK	Device Status Monitoring	Indicates unlock status for PLL (digital): 0 → PLL locked 1 → PLL unlocked Note: the external output signal on Status 0 or Status 1 uses a reversed logic, and indicates "lock" with a V_{OH} signal and unlock with a V_{OL} signaling level.
1	LOS_REF		Loss of reference input observed at input Smart MUX output in observation window for PLL: 0 → Reference input present 1 → Loss of reference input
0	SEL_REF		Indicates Reference Selected for PLL: 0 → Primary 1 → Secondary

Table 32. Register 40 (Read Only)

BIT	BIT NAME	RELATED BLOCK	DESCRIPTION/FUNCTION
15	RESERVED		Ignore
14	RESERVED		Ignore
13	RESERVED		Ignore
12	RESERVED		Ignore
11	RESERVED		Ignore
10	RESERVED		Ignore
9	RESERVED		Ignore
8	RESERVED		Ignore
7	RESERVED		Ignore
6	RESERVED		Ignore
5:3	VCO_VERSION	Device Information	Indicates the device version (Read only): 000 → CDCM6208V2G
2:0	DIE_REVISION		Indicates the silicon die revision (Read only): 00X --> Engineering Prototypes 010 --> Production Material

Table 33. Default Register Setting For SPI/I2C Modes

Register	CDCM6208V2G
0	0x01B9
1	0x0000
2	0x0013
3	0x08F6
4	0x30B4
5	0x01BA
6	0x0004
7	0x01BA
8	0x0005
9	0x001A
10	0x0130
11	0x0000
12	0x001A
13	0x0030
14	0x0000
15	0x001A
16	0x0050
17	0x0000
18	0x0652
19	0x0008
20	0x0000
.	.
.	.
.	.
40	0x00XX

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The CDCM6208 is a highly integrated clock generator and jitter cleaner. The CDCM6208 derives its output clocks from an on-chip oscillator which can be buffered through integer or fractional output dividers.

11.2 Typical Applications

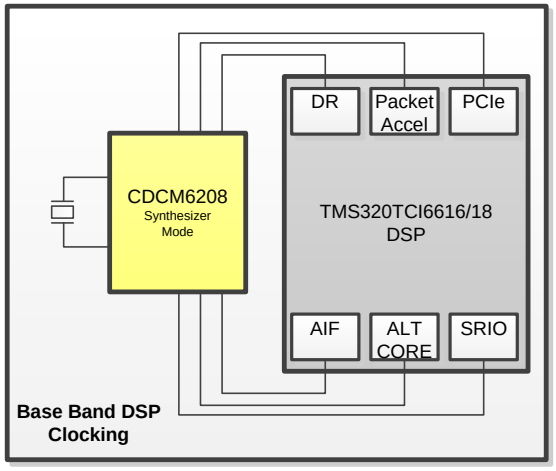


Figure 36. Typical Application Circuit

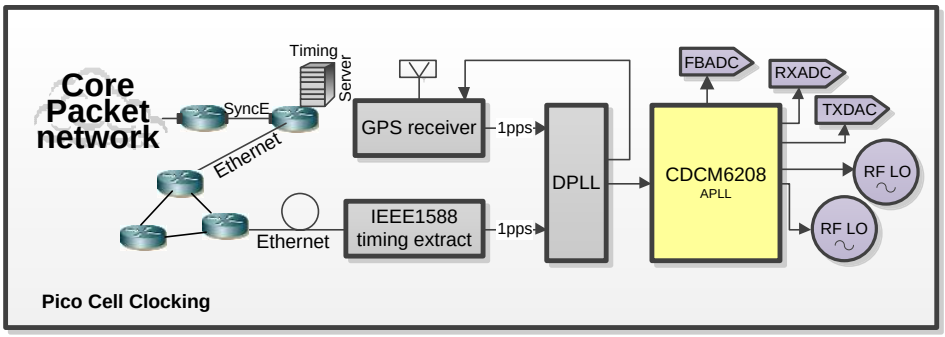


Figure 37. Typical Application Circuit

11.2.1 Design Requirements

The most jitter sensitive application besides driving A-to-D converters are systems deploying a serial link using Serializer and De-serializer implementation (for example, a 10 GigEthernet). Fully estimating the clock jitter impact on the link budget requires an understanding of the transmit PLL bandwidth and the receiver CDR bandwidth.

Typical Applications (continued)

11.2.1.1 Device Block-level Description

The CDCM6208V2G includes an on-chip PLL with an on-chip VCO. The PLL blocks consist of a universal input interface, a phase frequency detector (PFD), charge pump, partially integrated loop filter, and a feedback divider. Completing the CDCM6208V2G device are the combination of integer and fractional output dividers, and universal output buffers. The PLL is powered by on-chip low dropout (LDO), linear voltage regulators and the regulated supply network is partitioned such that the sensitive analog supplies are running from separate LDOs than the digital supplies which use their own LDO. The LDOs provide isolation of the PLL from any noise in the external power supply rail with a PSNR of better than -50 dB at all frequencies. The regulator capacitor pin REG_CAP should be connected to ground by a 10 µF capacitor with low ESR (e.g. below 1 Ω ESR) to ensure stability.

11.2.1.2 Device Configuration Control

Figure 39 illustrates the relationships between device states, the control pins, device initialization and configuration, and device operational modes. In pin mode, the state of the control pins determines the configuration of the device for all device states. In programming mode, the device registers are initialized to their default state and the host can update the configuration by writing to the device registers. A system may transition a device from pin mode to host connected mode by changing the state of the SI_MODE pins and then triggering a device reset (either via the RESETN pin or via setting the RESETN bit in the device registers). In reset, the device disables the outputs so that unwanted sporadic activity associated with device initialization does not appear on the device outputs.

Typical Applications (continued)

11.2.1.3 Configuring the RESETN Pin

Figure 38 shows two typical applications examples of the RESETN pin.

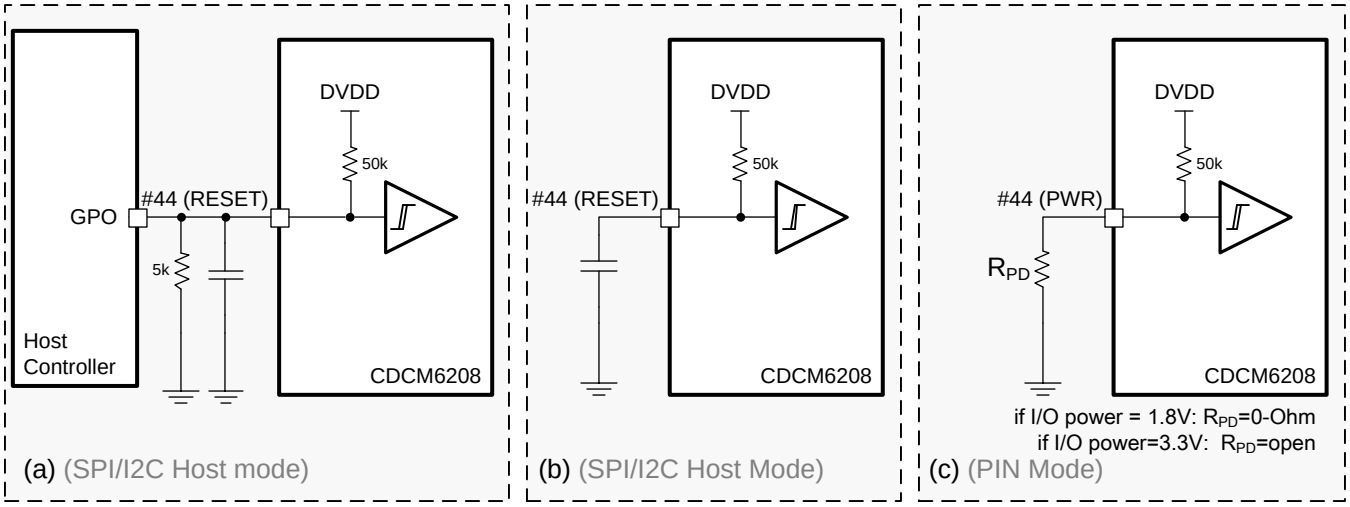


Figure 38. RESETN/PWR Pin Configurations

Figure 38 *(a) SPI / I2C* mode only: shows the RESETN pin connected to a digital device that controls device reset. The resistor and capacitor combination ensure reset is held low even if the CDCM6208V2G is powered up before the host controller output signal is valid.

Figure 38 *(b) SPI / I2C mode only:*shows a configuration in which the user wishes to introduce a delay between the time that the system applies power to the device and the device exiting reset. If the user does not use a capacitor, then the device effectively ignores the state of the RESETN pin.

Figure 38 *(c) Pin mode only:* shows a configuration useful if the device is used in Pin Mode. Here device pin number 44 becomes the PWR input. An external pull down resistor can be used to pull this pin down. If the resistor is not installed, the pin is internally pulled high.

Typical Applications (continued)

Figure 39 shows how the different possible device configurations and when the VCO becomes calibrated and the outputs turn on and off.

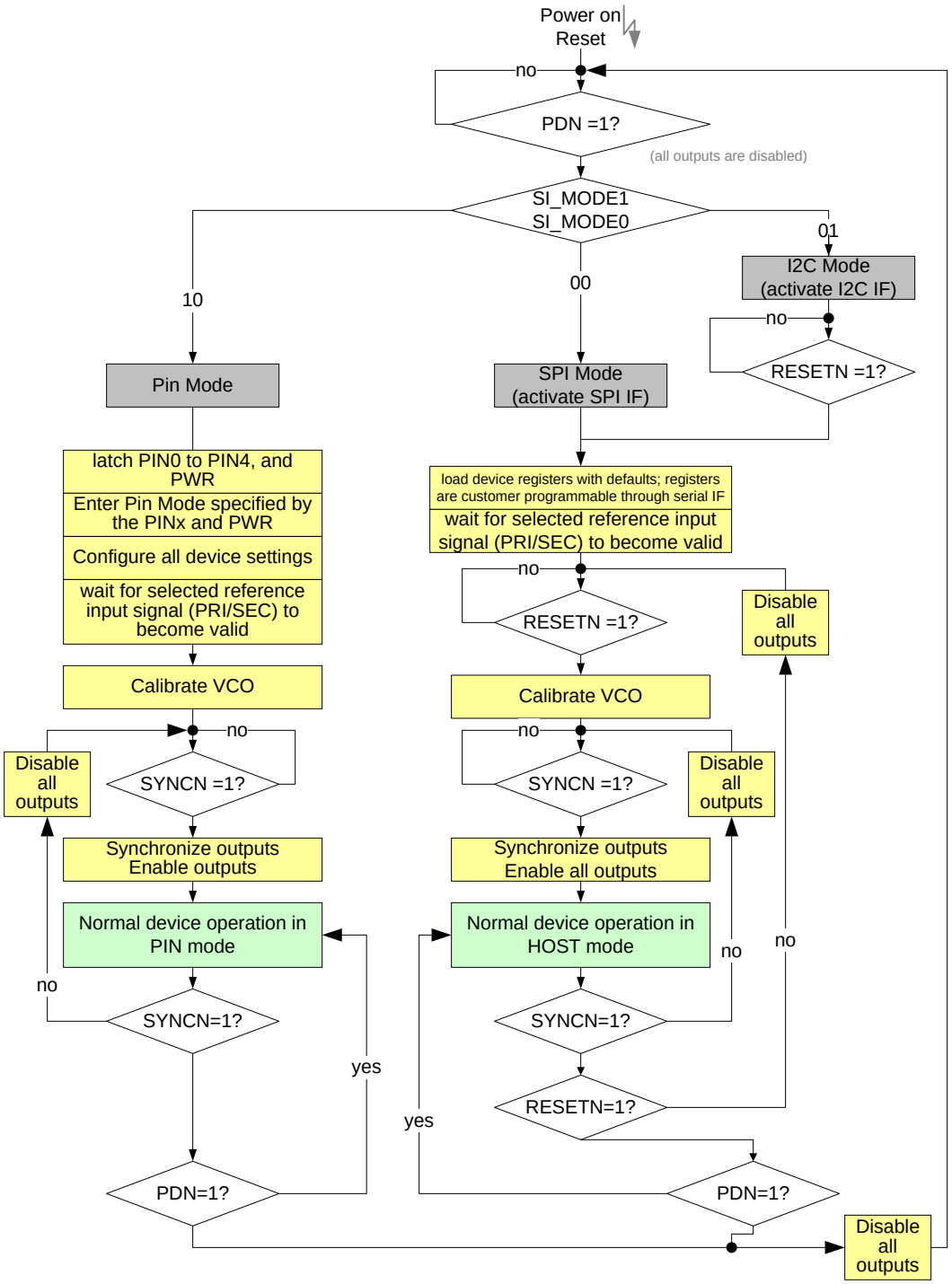


Figure 39. Device Power up and Configuration

Typical Applications (continued)

11.2.1.4 Preventing False Output Frequencies in SPI/I2C Mode at Startup:

Some systems require a custom configuration and cannot tolerate any output to start up with a wrong frequency. Holding RESET low at power-up until the device is fully configured keeps all outputs disabled. The device calibrates automatically after RESET becomes released and starts out with the desired output frequency.

NOTE

The RESETN pin cannot be held low during I^2C communication. Instead, use the SYNC pin to disable the outputs during an I^2C write operation, and toggle RESETN pin afterwards. Alternatively, other options exist such as using the RESETN bit in the register space to disable outputs until the write operation is complete.

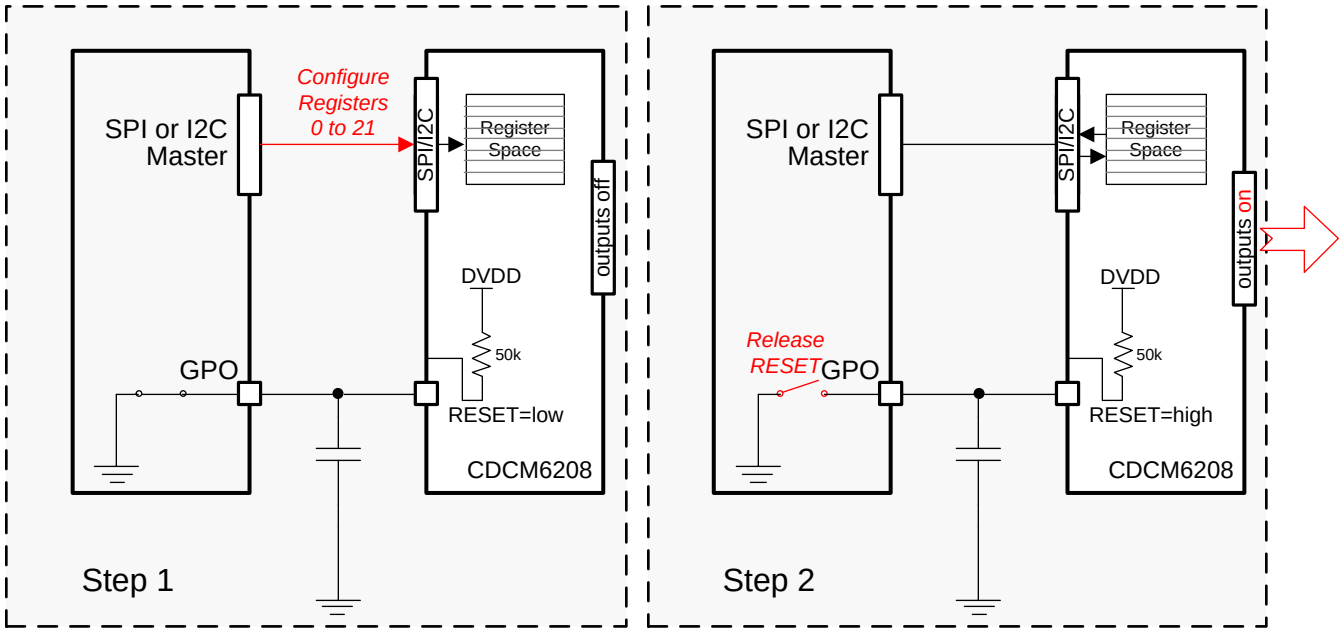


Figure 40. Reset Pin Control During Register Loading

11.2.1.5 Power Down

When the PDN pin = 0, the device enters a complete power down mode with a current consumption of no more than 1 mA from the entire device.

11.2.1.6 Device Power Up Timing:

Before the device outputs turn on after power up, the device goes through the following initialization routine:

Table 34. Initialization Routine

STEP	DURATION	COMMENTS
Step 1: Power up ramp	Depends on customer supply ramp time	The POR monitor holds the device in power-down or reset until the VDD supply voltage reaches 1.06 V (min) to 1.26 V (max)
Step 2: XO startup (if crystal is used)	Depends on XTAL. Could be several ms; For NX3225GA 25 MHz typical XTAL startup time measures 200 µs.	This step assumes RESETN = 1 and PDN = 1.The XTAL startup time is the time it takes for the XTAL to oscillate with sufficient amplitude. The CDCM6208V2G has a built-in amplitude detection circuit, and holds the device in reset until the XTAL stage has sufficient swing.

Typical Applications (continued)

Table 34. Initialization Routine (continued)

STEP	DURATION	COMMENTS
Step 3: Ref Clock Counter	64k Reference clock cycles at PFD input	This counter of 64 k clock cycles needs to expire before any further power-up step is done inside the device. This counter ensures that the input to the PFD from PRI or SEC input has stabilized in frequency. The duration of this step can range from 640 µs (f_{PFD}= 100 MHz) to 8 sec (8 kHz PFD).
Step 4: FBCLK counter	64k FBCLK cycles with CW=32; The duration is similar to Step 3, or can be more accurately estimated as: Approximately 64k x PS_A x N/2.48 GHz	The Feedback counter delays the startup by another 64k PFD clock cycles. This is so that all counters are well initialized and also ensure additional timing margin for the reference clock to settle. This step can range from 640 µs (f_{PFD}= 100 MHz) to 8 sec (f_{PFD}= 8kHz).
Step 5: VCO calibration	128k PFD reference clock cycles	This step calibrates the VCO to the exact frequency range, and takes exactly 128k PFD clock cycles. The duration can therefore range from 1280 µs (f_{PFD}= 100 MHz) to 16 sec (f_{PFD}= 8 KHz).
Step 6: PLL lock time	approximately 3 x LBW	The Outputs turn on immediately after calibration. A small frequency error remains for the duration of approximately 3 x LBW (so in synthesizer mode typically 10 µs). The initial output frequency will be lower than the target output frequency, as the loop filter starts out initially discharged.
Step 7: PLL Lock indicator high	approximately 2305 PFD clock cycles	The PLL lock indicator if selected on output STATUS0 or STATUS1 will go high after approximately 2048 to 2560 PFD clock cycles to indicate PLL is now locked.

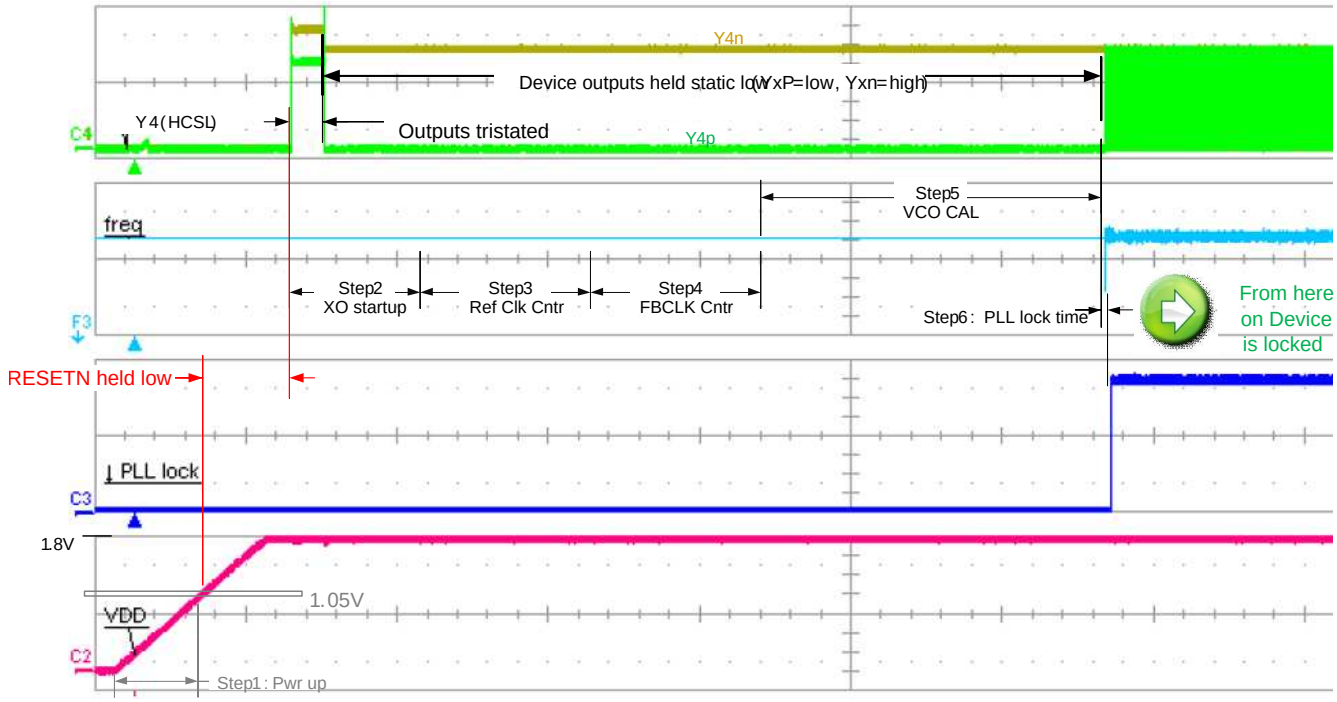


Figure 41. Powerup Time

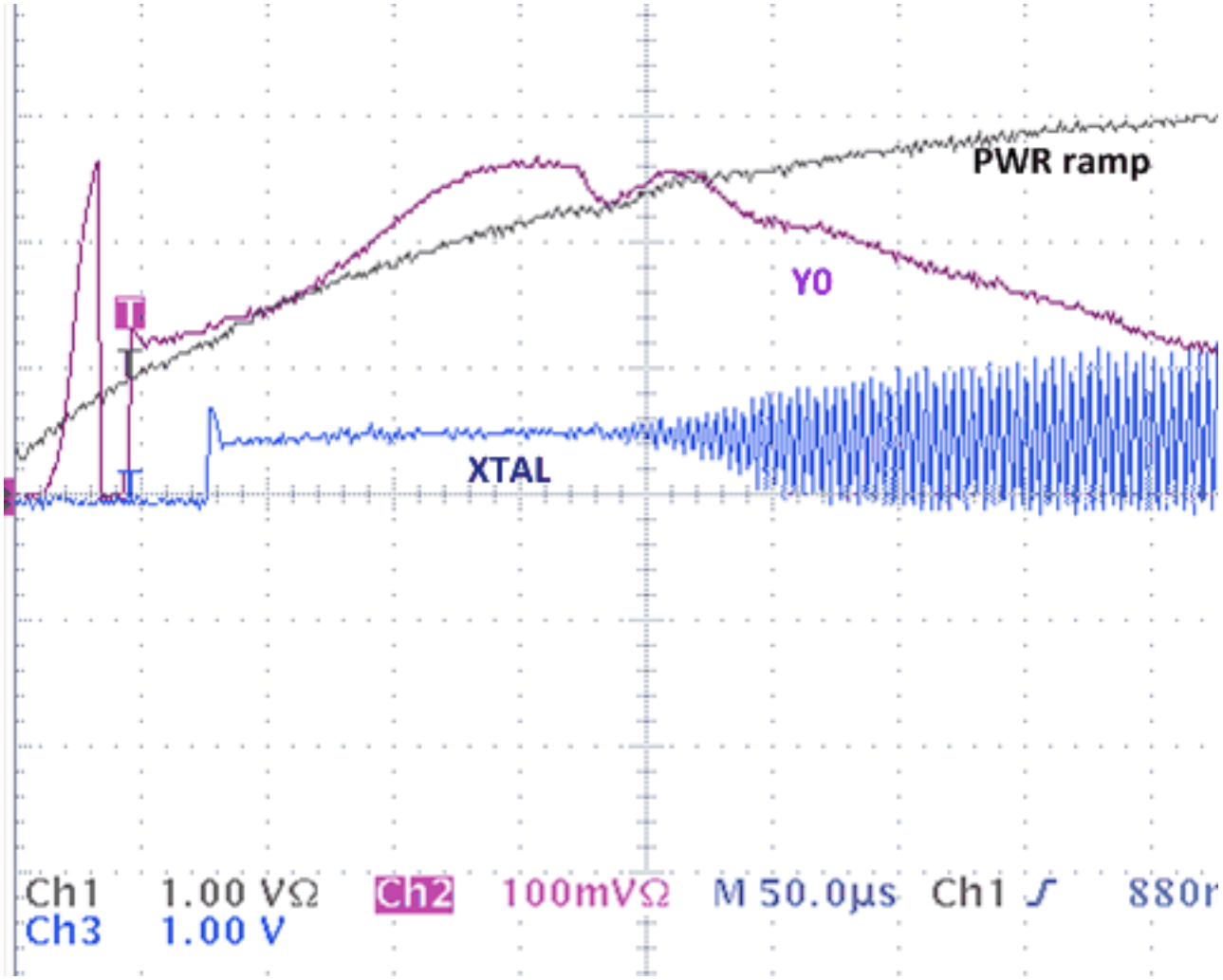


Figure 42. XTAL Startup Using NX3225GA 25 MHz (Step 2)

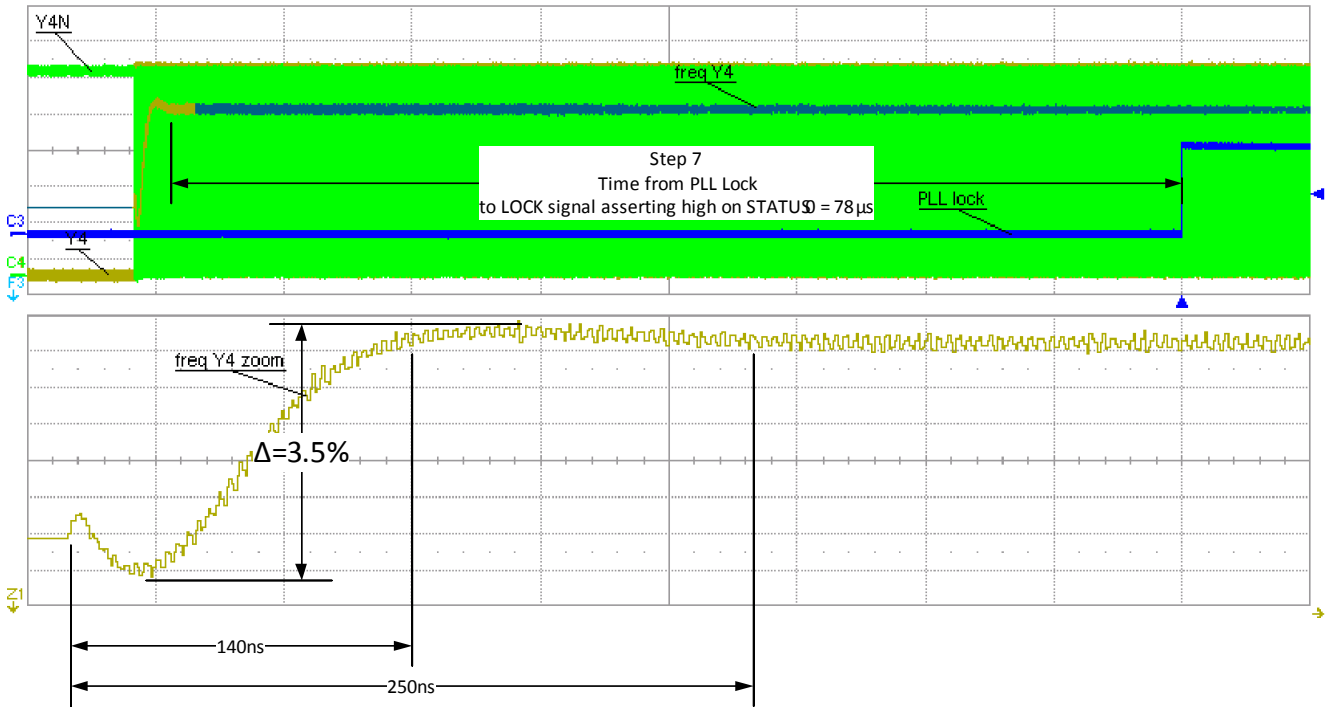


Figure 43. PLL Lock Behavior (Step 6)

11.2.1.7 Input Mux and Smart Input Mux

The Smart Input MUX supports auto-switching and manual-switching using control pin (and through register). The Smart Input MUX is designed such that glitches created during switching in both auto and manual modes are suppressed at the MUX output.

Table 35. Input Mux Selection

SI_MODE1 PIN NO. 47	REGISTER 4 BIT 13SMUX_MODE_SEL	REGISTER 4 BIT 12 SMUX_REF_SEL	REF_SEL PIN NO. 6	SELECTED INPUT	
0 (SPI/I2C mode)	0	X	X	Auto Select Priority is given to Primary Reference input.	
	1	0	1	Primary input	input select through SPI/I^{2}C
		1		Secondary input	
		1	0	Primary input	input select through external pin
			1	Secondary input	
1 (pin mode)	not available		0	Primary or Auto (see Table 4)	
			1	Secondary or Auto (see Table 4)	

Example 1:An application desired to auto-select the clock reference in SPI/I2C mode. During production testing however, the system needs to force the device to use the primary followed by the secondary input. The settings would be as follows:

1. Tie REF_SEL pin always high
2. For primary clock input testing, use R4[13:12] = 10
3. For secondary clock input testing, set R4[13:12] = 11.
4. For the auto-mux setting in the final product shipment, set R3[13:12]=01 or 00

Example 2: The application wants to select the clock input manually without programming SPI/I2C. In this case, program R4[13:12] = 11, and select primary or secondary input by toggling REF_SEL low or high.

SmartMux input frequency limitation: In the automatic mode, the frequencies of both inputs to the smart mux (PRI_REF divided by R and SEC_REF) need to be similar; however, they can vary by up to 20%.

Switching behavior: The input clocks can have any phase. When switching happens between one input clock to the other, the phase of the output clock slowly transitions to the phase of the newly selected input clock. There will be no-phase jump at the output. The phase transition time to the new reference clock signal depends on the PLL loop filter bandwidth. Auto-switch assigns higher priority to PRI_REF and lower priority to SEC_REF. The timing diagram of an auto-switch at the input MUX is shown in Figure 44.

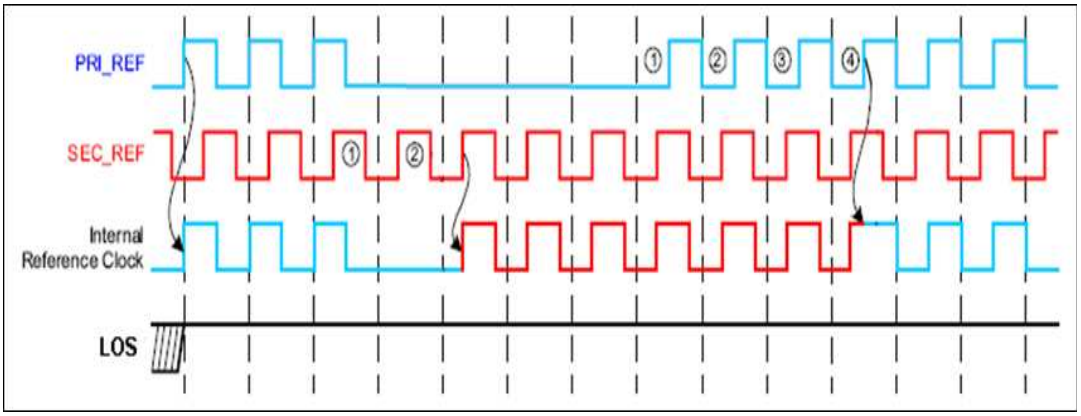


Figure 44. Smart Input MUX Auto-Switch Mode Timing Diagram

11.2.1.8 Universal INPUT Buffer (PRI_REF, SEC_REF)

The universal input buffers support multiple signaling formats (LVDS, CML or LVCMOS) and these require external termination schemes. The secondary input buffer also supports crystal inputs and Table 28 provides the characteristics of the crystal that can be used. Both inputs incorporate hysteresis.

11.2.1.9 VCO Calibration

The LC VCO is designed using high-Q monolithic inductors and has low phase noise characteristics. The VCO of the CDCM6208V2G must be calibrated to ensure that the clock outputs deliver optimal phase noise performance. Fundamentally, a VCO calibration establishes an optimal operating point within the tuning range of the VCO. While transparent to the user, the CDCM6208V2G and the host system perform the following steps comprising a VCO calibration sequence:

1. **Normal Operation**- When the CDCM6208V2G is in normal (operational) mode, the state of both the power down pin (PDN) and reset pin (RESETN) is high.
2. **Entering the reset state** – If the user wishes to restore all device defaults and initiate a VCO calibration sequence, then the host system must place the device in reset via the PDN pin, via the RESETN pin, or by removing and restoring device power. Pulling either of these pins low places the device in the reset state. Holding either pin low holds the device in reset.
3. **Exiting the reset state** – The device calibrates the VCO either by exiting the device reset state or through the device reset command initiated via the host interface. Exiting the reset state occurs automatically after power is applied and/or the system restores the state of the PDN or RESETN pins from the low to high state. Exiting the reset state using this method causes the device defaults to be loaded/reloaded into the device register bank. Invoking a device reset via the register bit does not restore device defaults; rather, the device retains settings related to the current clock frequency plan. Using this method allows for a VCO calibration for a frequency plan other than the default state (i.e. the device calibrates the VCO based on the settings contained within the register bank at the time that the register bit is accessed). The nominal state of this bit is low. Writing this bit to a high state and then returning it to the low state invokes a device reset without restoring device defaults.

4. **Device stabilization** – After exiting the reset state as described in Step 3, the device monitors internal voltages and starts a reset timer. Only after internal voltages are at the correct level and the reset time has expired will the device initiate a VCO calibration. This ensures that the device power supplies and phase locked loops have stabilized prior to calibrating the VCO.
5. **VCO Calibration** – The CDCM6208V2G calibrates the VCO. During the calibration routine, the device holds all outputs in reset so that the CDCM6208V2G generates no spurious clock signals.

11.2.1.10 Reference Divider (R)

The reference (R) divider is a continuous 4-b counter (1 – 16) that is present on the primary input before the Smart Input MUX. It is operational in the frequency range of 8 kHz to 250 MHz. The output of the R divider sets the input frequency for the Smart MUX, and the auto switch capability of the Smart MUX can then be employed as long as the secondary input frequency is no more than ± 20% different from the output of the R divider.

11.2.1.11 Input Divider (M)

The input (M) divider is a continuous 14-b counter (1 – 16384) that is present after the Smart Input MUX. It is operational in the frequency range of 8 kHz to 250 MHz. The output of the M divider sets the PFD frequency to the PLL and should be in the range of 8 kHz to 100 MHz.

11.2.1.12 Feedback Divider (N)

The feedback (N) divider is made up of cascaded 8-b counter divider (1 – 256) followed by a 10-b counter divider (1 – 1024) that are present on the feedback path of the PLL. It is operational in the frequency range of 8 kHz to 800 MHz. The output of the N divider sets the PFD frequency to the PLL and should be in the range of 8 kHz to 100 MHz. The frequency out of the first divider is required to be less than or equal to 200 MHz to ensure proper operation.

11.2.1.13 Prescaler Dividers (PS_A, PS_B)

The prescaler (PS) dividers are fed by the output of the VCO and are distributed to the output dividers (PS_A to the dividers for Outputs 0, 1, 4, and 5 and PS_B to the dividers for Outputs 2, 3, 6, and 7. PS_A also completes the PLL as it also drives the input of the Feedback Divider (N).

11.2.1.14 Phase Frequency Detector (PFD)

The PFD takes inputs from the Smart Input MUX output and the feedback divider output and produces an output that is dependent on the phase and frequency difference between the two inputs. The allowable range of frequencies at the inputs of the PFD is from 8 kHz to 100 MHz.

11.2.1.15 Charge Pump (CP)

The charge pump is controlled by the PFD which dictates either to pump up or down in order to charge or discharge the integrating section of the on-chip loop filter. The integrated and filtered charge pump current is then converted to a voltage that drives the control voltage node of the internal VCO through the loop filter. The range of the charge pump current is from 500 µA to 4 mA.

11.2.1.16 Programmable Loop Filter

The on-chip PLL supports a partially internal and partially external loop filter configuration for all PLL loop bandwidths where the passive external components C1, C2, and R2 are connected to the ELF pin as shown in Figure 45 to achieve PLL loop bandwidths from 400 kHz down to 10 Hz.

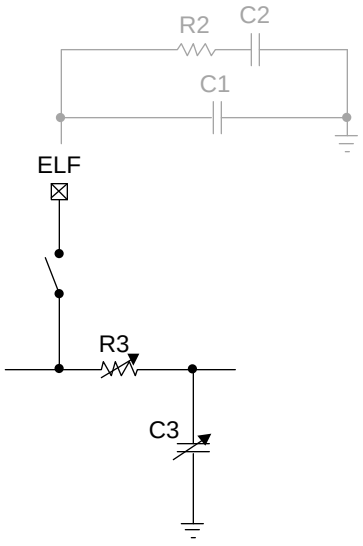


Figure 45. CDCM6208V2G PLL Loop Filter Topology

11.2.1.16.1 Loop Filter Component Selection

The loop filter setting and external resistor selection is important to set the PLL to best possible bandwidth and to minimize jitter. A high bandwidth (≥ 100 kHz) provides best input signal tracking and is therefore desired with a clean input reference (synthesizer mode). A low bandwidth (≤ 1 kHz) is desired if the input signal quality is unknown (jitter cleaner mode). TI provides a software tool that makes it easy to select the right loop filter components. C1, R2, and C2 are external loop filter components, connected to the ELF pin. The 3 rd pole of the loop filter is device internal with R3 and C3 register selectable.

11.2.1.16.2 Device Output Signaling

LVDS-like: All outputs Y[7:0] support LVDS-like signaling. The actual output stage uses a CML structure and drives a signal swing identical to LVDS (~350mV). The output slew rate is faster than standard LVDS for best jitter performance. The LVDS-like outputs should be AC-coupled when interfacing to a LVDS receiver. See reference schematic Figure 63 for an example. The supply voltage for outputs configured LVDS can be selected freely between 1.8 V and 3.3 V.

LVPECL-like: Outputs Y[3:0] support LVPECL-like signaling. The actual output stage uses a CML structure but drives the same signal amplitude and rise time as true emitter coupled logic output stages. The LVPECL-like outputs should be AC-coupled, and contrary to standard PECL designs, no external termination resistor to VCC-2V is used (fewer components for lowest BOM cost). See reference schematic Figure 63 for an example. The supply voltage for outputs configured LVPECL-like is recommended to be 3.3 V, though even 1.8 V provides nearly the same output swing and performance at much lower power consumption.

CML: Outputs Y[3:0] support standard CML signaling. The supply voltage for outputs configured CML can be selected freely between 1.8 V and 3.3 V. A true CML receiver can be driven DC coupled. All other differential receiver should connected using AC coupling. See reference schematic Figure 63 for a circuit example.

HCSL: Outputs Y[7:4] support HCSL signaling. The supply voltage for outputs configured HCSL can be selected freely between 1.8 V and 3.3 V. HCSL is referenced to GND, and requires external 50 Ω termination to GND. See reference schematic for an example.

CMOS: Outputs Y[7:4] support 1.8 V, 2.5 V, and 3.3 V CMOS signaling. A fast or reduced slew rate can be selected through register programming. Each differential output port can drive one or two CMOS output signals. Both signals are “in-phase”, meaning their phase offset is zero degrees, and not 180˚. The output swing is set by providing the according supply voltage (for example, if VDD_Y4=2.5 V, the output swing on Y4 will be 2.5 V CMOS). Outputs configured for CMOS should only be terminated with a series-resistor near the device output to preserve the full signal swing. Terminating CMOS signals with a 50 Ω resistor to GND would reduce the output signal swing significantly.

11.2.1.16.3 Integer Output Divider (IO)

Each integer output divider is made up of a continuous 10-b counter. The output buffer itself contributes only little to the total device output jitter due to a low output buffer phase noise floor. The typical output phase noise floor at an output frequency of 122.88 MHz, 20 MHz offset from the carrier measures as follows: LVCMOS: -157.8 dBc/Hz, LVDS: -158 dBc/Hz, LVPECL: -158.25 dBc/Hz, HCSL: -160 dBc/Hz. Therefore, the overall contribution of the output buffer to the total jitter is approximately 50 fs-rms (12 k - 20 MHz). An actual measurement of phase noise floor with different output frequencies for one nominal until yielded the following:

Table 36. Integer Output Divider (IO)

f_{OUT}	LVDS (Y0)	PECL (Y0)	CML (Y0)	HCSL (Y4)	CMOS 3p3V (Y7)
737.28 MHz	-154.0 dBc/Hz	-154.8 dBc/Hz	-154.4 dBc/Hz	-153.1 dBc/Hz	-150.9 dBc/Hz
368.64 MHz	-157.0 dBc/Hz	-155.8 dBc/Hz	-156.4 dBc/Hz	-153.9 dBc/Hz	-153.1 dBc/Hz
184.32 MHz	-157.3 dBc/Hz	-158.6 dBc/Hz	158.1 dBc/Hz	-154.7 dBc/Hz	-156.2 dBc/Hz
92.16 MHz	-161.2 dBc/Hz	-161.6 dBc/Hz	-161.4 dBc/Hz	-155.2 dBc/Hz	-159.4 dBc/Hz
46.08 MHz	-162.2 dBc/Hz	-165.0 dBc/Hz	-163.0 dBc/Hz	-154.0 dBc/Hz	-162.8 dBc/Hz

11.2.1.16.4 Fractional Output Divider (FOD)

The CDCM6208V2G incorporates a fractional output divider on Y[7:4], allowing these outputs to run at non-integer output divide ratios of the PLL frequencies. This feature is useful when systems require different, unrelated frequencies. The fractional output divider architecture is shown in Figure 46.

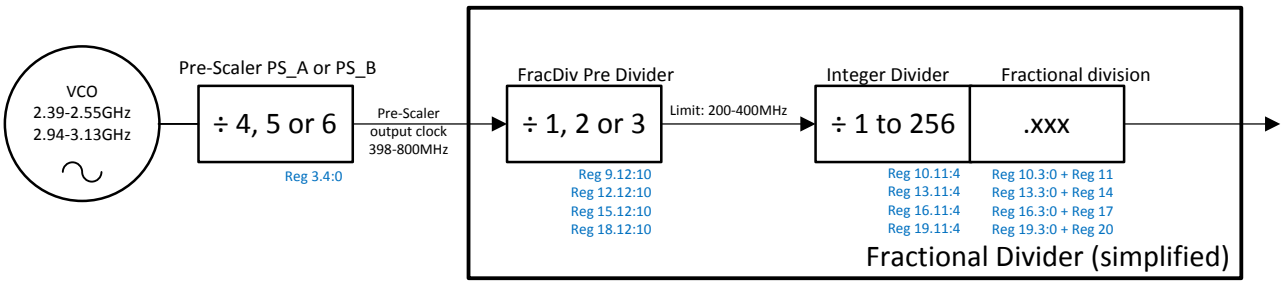


Figure 46. Fractional Output Divider Principle Architecture (Simplified Graphic, not Showing Output Divider Bypass Options)

The fractional output divider requires an input frequency between 400 MHz and 800 MHz, and outputs any frequency equal or less than 400 MHz (the minimum fractional output divider setting is 2). The fractional divider block has a first stage integer pre-divider followed by a fractional sigma-delta output divider block that is deep enough such as to generate any output frequency in the range of 0.78 MHz to 400 MHz from any input frequency in the range of 400 MHz to 800 MHz with a worst case frequency accuracy of no more than ±1ppm. The fractional values available are all possible 20-b representations of fractions within the following range:

- $1.0 \le fracDIV \le 1.9375$
- $2.0 \le fracDIV \le 3.875$
- $4.0 \le fracDIV \le 5.875$
- $x.0 \le fracDIV \le (x + 1) + 0.875$ with x being all even numbers from x = 2, 4, 6, 8, 10, ..., 254
- $254.0 \le fracDIV \le 255.875$
- $256.0 \le fracDIV \le 256.99999$

The CDCM6208V2G user GUI comprehends the fractional divider limitations; therefore, using the GUI to comprehend frequency planning is recommended.

The fractional divider output jitter is a function of fractional divider input frequency and furthermore depends on which bits are exercised within the fractional divider. Exercising only MSB or LSB bits provides better jitter than exercising bits near the center of the fractional divider. Jitter data are provided in this document, and vary from 50 ps-pp to 200 ps-pp, when the device is operated as a frequency synthesizer with high PLL bandwidths (approximately 100 kHz to 400 kHz). When the device is operated as a jitter cleaner with low PLL bandwidths (< 1 kHz), its additive total jitter increases by as much as 30 ps-pp. The fractional divider can be used in integer mode. However, if only an integer divide ratio is needed, it is important to disable the corresponding fractional divider enable bit, which engages the higher performing integer divider.

11.2.1.16.5 Output Synchronization

Both types of output dividers can be synchronized using the SYNCN signal. For the CDCM6208V2G, this signal comes from the SYNCN pin or the soft SYNCN register bit R3.5. The most common way to execute the output synchronization is to toggle the SYNCN pin. When SYNC is asserted ($V_{SYNCN} \leq V_{IL}$), all outputs are disabled (high-impedance) and the output dividers are reset. When SYNC is de-asserted ($V_{SYNCN} \geq V_{IH}$), the device first internally latches the signal, then retimes the signal with the pre-scaler, and finally turns all outputs on simultaneously. The first rising edge of the outputs is therefore approximately 15 ns to 20 ns delayed from the SYNC pin assertion. For one particular device configuration, the uncertainty of the delay is ±1 PS_A clock cycles. For one particular device and one particular configuration, the delay uncertainty is one PS_A clock cycle.

The SYNC feature is particularly helpful in systems with multiple CDCM6208V2G. If SYNC is released simultaneously for all devices, the total remaining output skew uncertainty is ±1 clock cycles for all devices configured to identical pre-scaler settings. For devices with varying pre-scaler settings, the total part-to-part skew uncertainty due to sync remains ±2 clock cycles.

Outputs Y0, Y1, Y4, and Y5 are aligned with the PS_A output while outputs Y2, Y3, Y6, and Y7 are aligned with the PS_B output). All outputs Y[7:0] turn on simultaneously, if PS_B and PS_A are set to identical divide values (PS_A=PS_B).

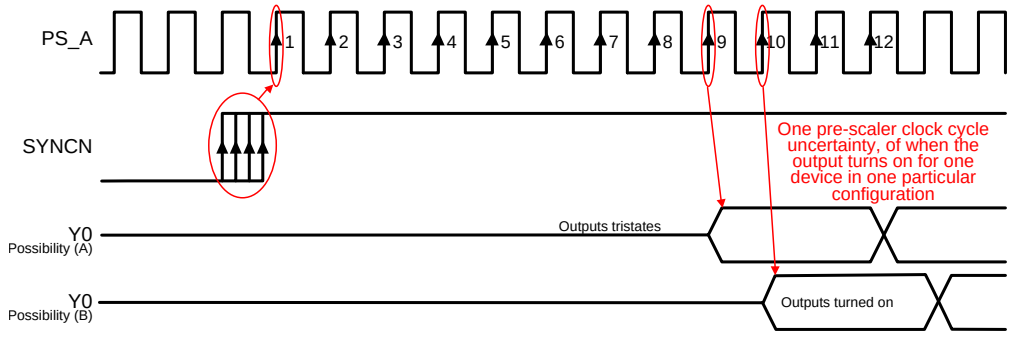


Figure 47. SYNCN to Output Delay Uncertainty

11.2.1.16.6 Output MUX on Y4 and Y5

The CDCM6208V2G device outputs Y4 and Y5 can either be used as independent fractional outputs or allow bypassing of the PLL in order to output the primary or secondary input signal directly.

11.2.1.16.7 Staggered CLK Output Powerup for Power Sequencing of a DSP

DSPs are sensitive to any kind of voltage swing on unpowered input rails. To protect the DSP from long-term reliability problems, it is recommended to avoid any clock signal to the DSP until the DSP power rail is also powered up. This can be achieved in two ways using the CDCM6208V2G:

1. ***Digital control***: Initiating a configuration of all registers so that all outputs are disabled, and then turning on outputs one by one through serial interface after each DSP rail becomes powered up accordingly.
2. ***Output Power supply domain control***: An even easier scheme might be to connect the clock output power supply VDD_Yx to the corresponding DSP input clock supply domain. In this case, the CDCM6208V2G output will remain disabled until the DSP rails ramps up as well. Figure 48 shows the turn-on behavior.

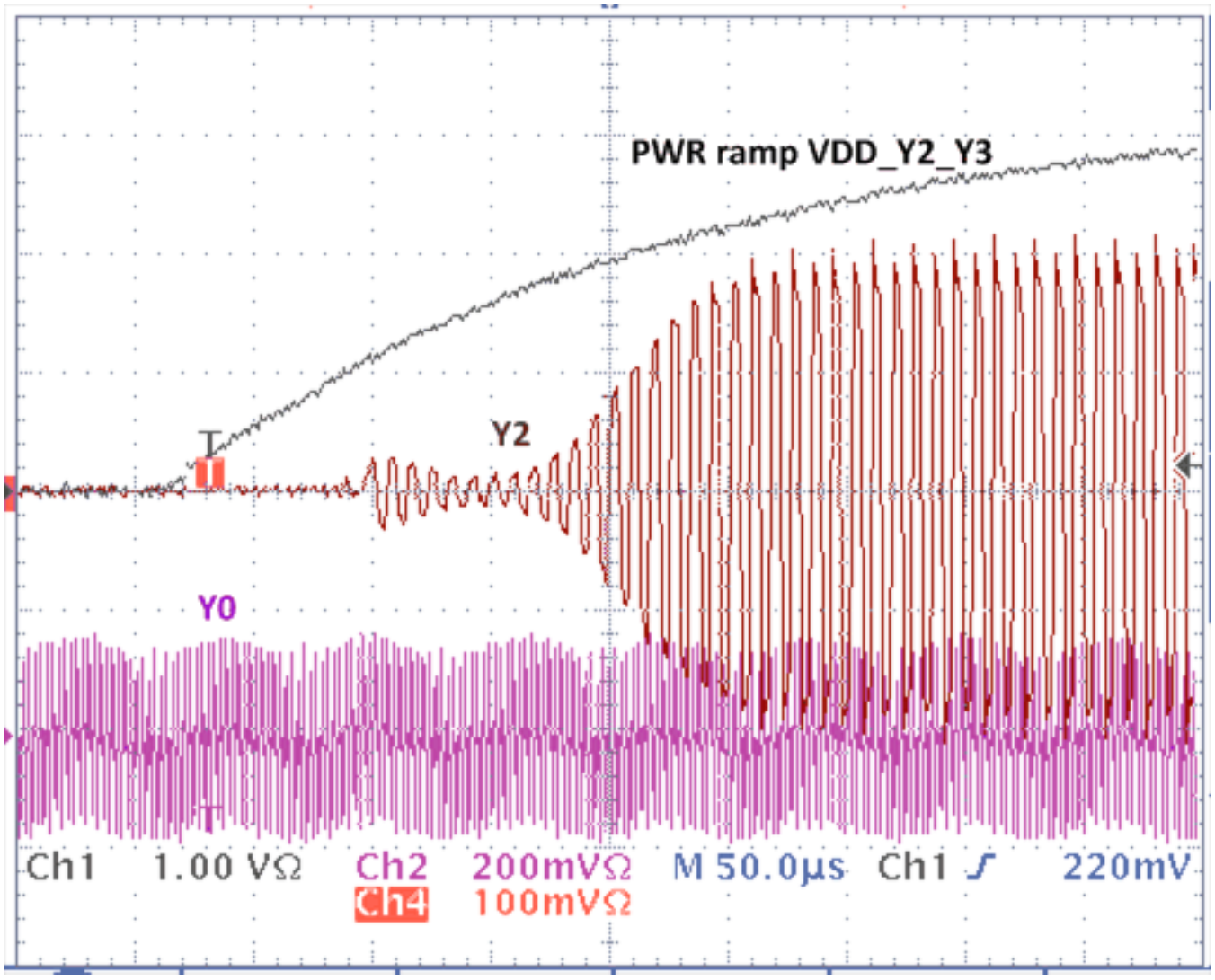


Figure 48. Sequencing the Output Turn-on Through Sequencing the Output Supplies. Output Y2 Powers Up While Output Y0 is Already Running.

11.2.2 Detailed Design Procedure

11.2.2.1 Jitter Considerations in SERDES Systems

The most jitter sensitive application besides driving A-to-D converters are systems deploying a serial link using Serializer and De-serializer implementation (for example, 10 GigEthernet). Fully estimating the clock jitter impact on the link budget requires an understanding of the transmit PLL bandwidth and the receiver CDR bandwidth. As can be seen in Figure 49, the bandwidth of TX and RX is the frequency range in which clock jitter adds without any attenuation to the jitter budget of the link. Outside of these frequencies, the SERDES link will attenuate clock jitter with a 20 dB/dec or even steeper roll-off.

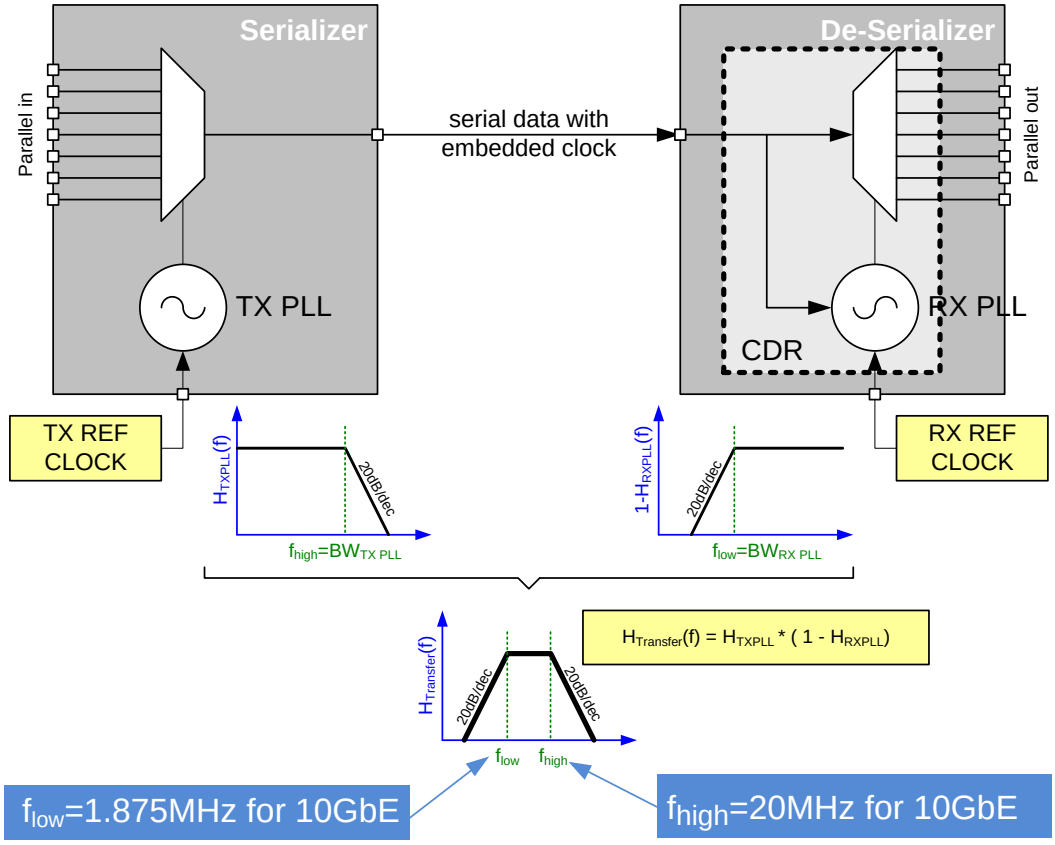


Figure 49. Serial Link Jitter Budget Explanation

Example: SERDES link with KeyStone™ I DSP

The SERDES TX PLL of the TI KeyStone™ I DSP family (see SPRABI2) for the SRIO interface, has a 13 MHz PLL bandwidth (Low Pass Characteristic, see Figure 49). The CDCM6208V2, pin-mode 27, was characterized in this example over Process, Voltage and Temperature (PVT) with a low pass filter of 13 MHz to simulate the TX PLL. The attenuation is higher or equal to 20 dB/dec; therefore, the characterization used 20 dB/dec as worst case.

Table 37 shows the maximum Total Jitter(1) over PVT with and without Low Pass Filter.

Table 37. Maximum Total Jitter Over PVT With and Without Low Pass Filter

OUTPUT	FREQUENCY [MHz]	MAX T_J [ps] DSP SPEC	MAX T_J [ps] without LOW PASS FILTER	MAX T_J [ps] with 13 MHz LOW PASS FILTER
Y0	122.88	56	9.43	8.19
Y2	30.72	56	9.60	7.36
Y3	30.72	56	9.47	7.42
Y4	156.25 (6 bit fraction)	56	57.66	17.48
Y5	156.25 (20 bit fraction)	56	76.87	32.32
Y6	100.00	56	86.30	33.86
Y7	66.667	300	81.71	35.77

(1) Input signal: 250fs RMS (Integration Range 12kHz to 5MHz)

Figure 50 shows the maximum Total Jitter with, without Low Pass Filter characteristic and the maximum TI KeyStone™ I specification.

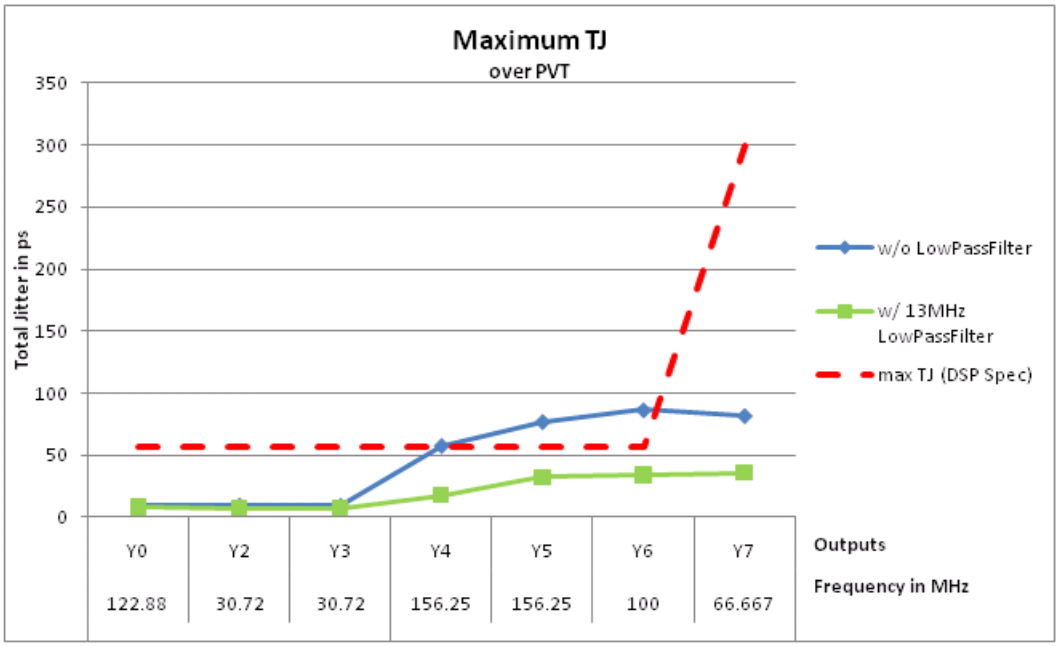


Figure 50. Maximum Jitter Over PVT

NOTE

Due to the damping characteristic of the DSP SERDES PLLs, the actual T_J data can be worse.

11.2.2.2 Jitter Considerations in ADC and DAC Systems

A/D and D/A converters are sensitive to clock jitter in two ways: They are sensitive to phase noise in a particular frequency band, and also have maximum spur level requirements to achieve maximum noise floor sensitivity. The following test results were achieved connecting the CDCM6208V2G to ADC and DACs:

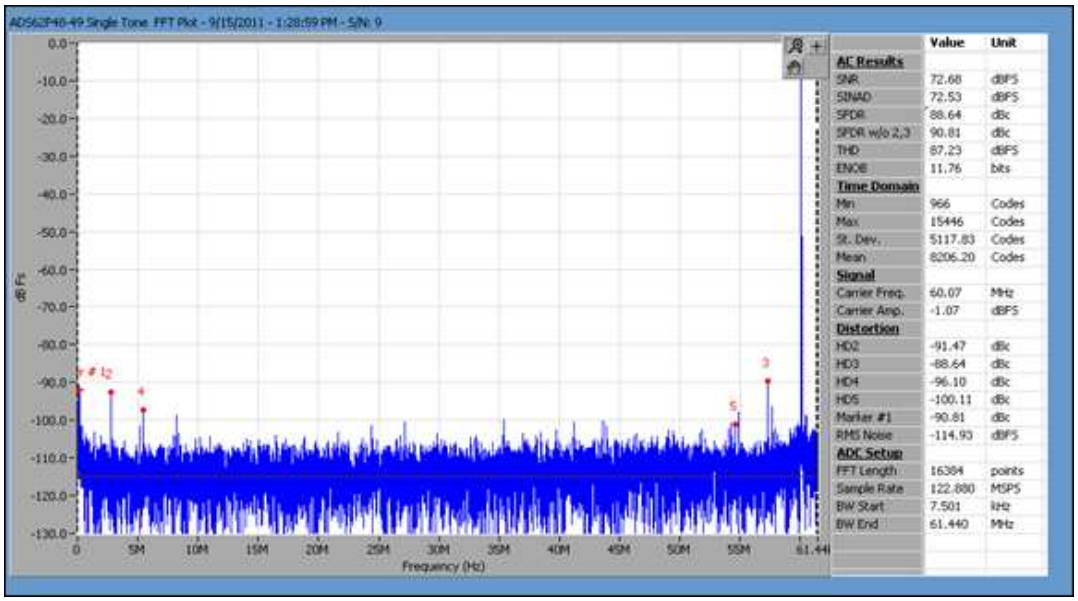


Figure 51. IF = 60 MHz Fclk = 122.88 MHz Baseline (Lab Clk Generator) ADC: ADS62P48-49

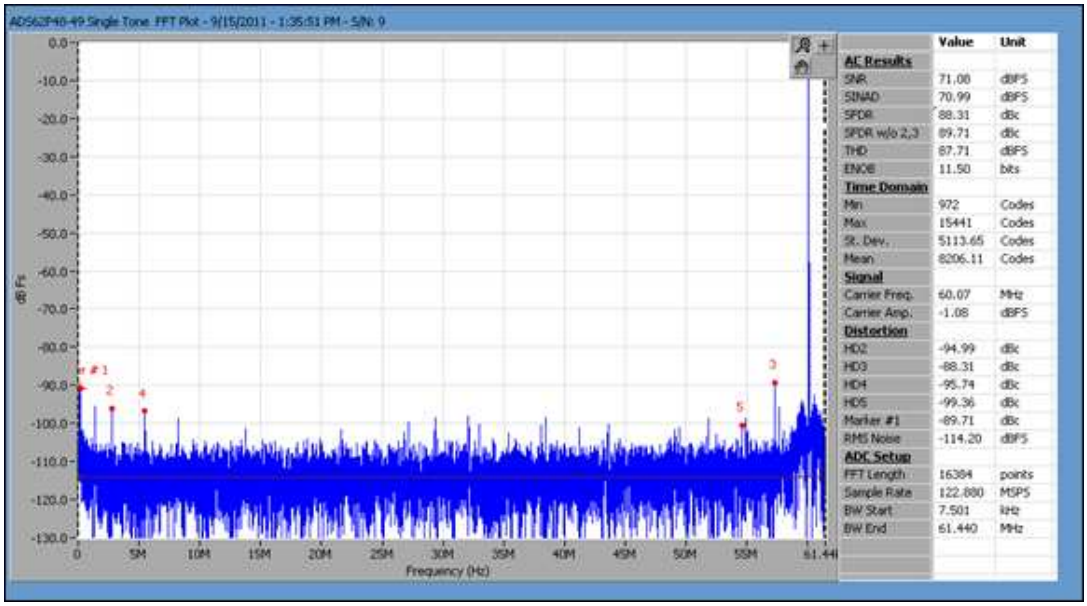


Figure 52. IF = 60 MHz Fclk = 122.88 MHz CDCM6208V2G driving ADC

Observation: up to an IF = 100 MHz, The ADC performance when driven by the CDCM6208V2G (Figure 52) is similar to when the ADC is driven by an expensive lab signal generator with additional passive source filtering (Figure 51).

Conclusion Therefore, the CDCM6208V2G is usable for applications up to 100 MHz IF. For IF above 100 MHz, the SNR starts degrading in our experiments. Measurements were conducted with ADC connected to Y0 and other outputs running at different integer frequencies.

Important note on crosstalk: it is highly recommended that both pre-dividers are configured identically, as otherwise SFDR and SNR suffer due to crosstalk between the two pre-divider frequencies.

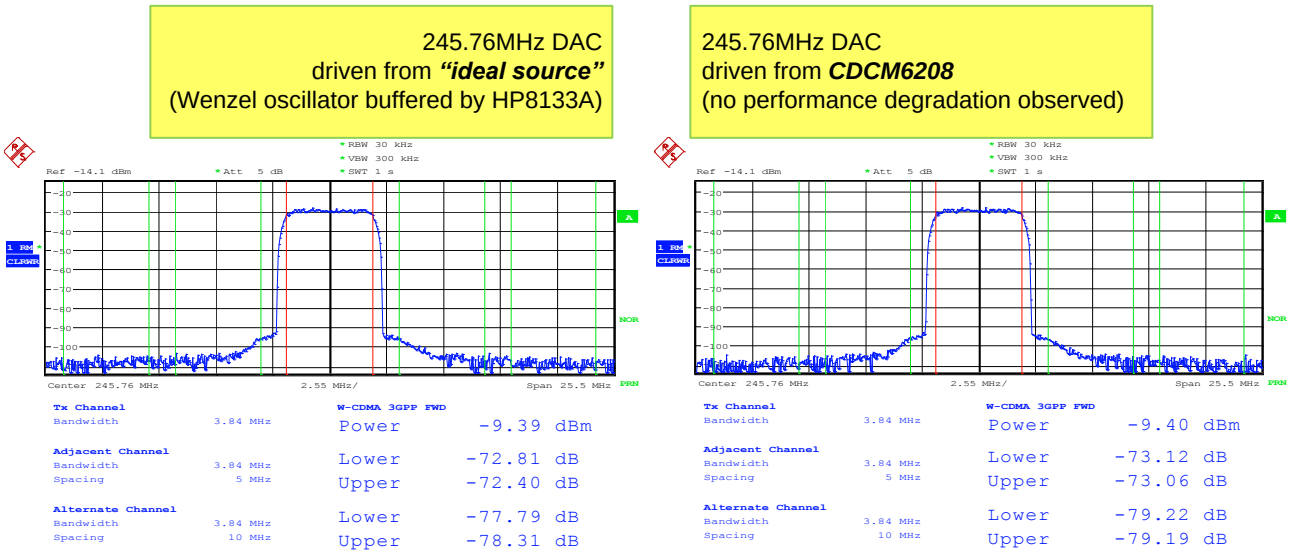


Figure 53. DAC Driven by Lab Source and CDCM6208V2G in Comparison (Performance Identical)

Observation/Conclusion: The DAC performance was not degraded at all by the CDCM6208V2G compared to driving the DAC with a perfect lab source. Therefore, the CDCM6208V2G provides sufficient low noise to drive a 245.76 MHz DAC.

11.2.3 Application Performance Plots

11.2.3.1 Typical Device Jitter

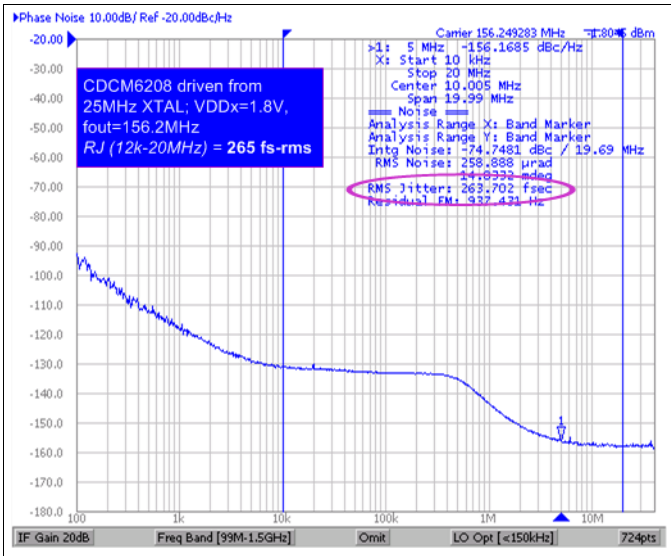


Figure 54. Typical Device Output Phase Noise and Jitter for 25 MHz

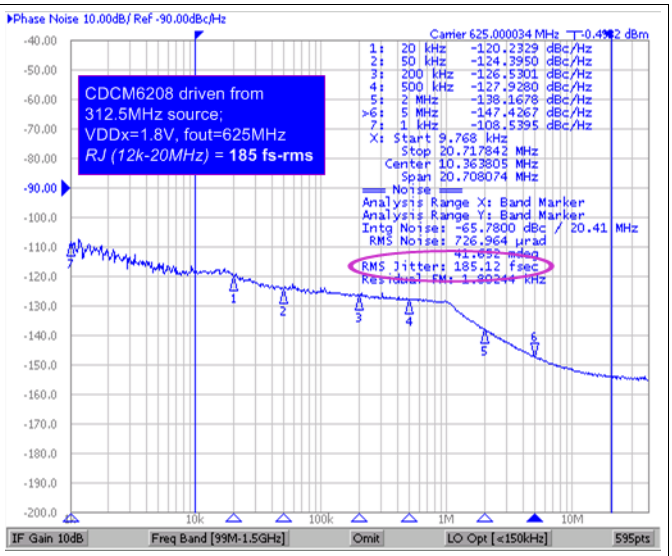


Figure 55. Typical Device Output Phase Noise and Jitter for 312.5 MHz

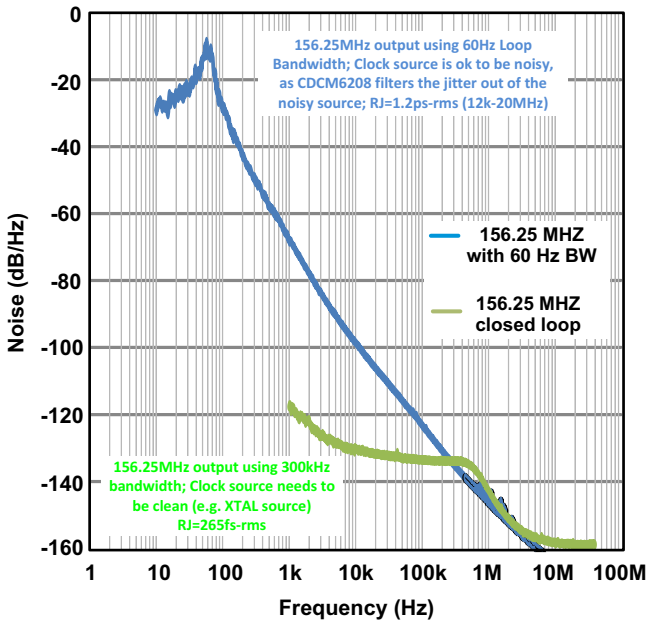


Figure 56. Phase Noise Plot for Jitter Cleaning Mode (blue) and Synthesizer Mode (green)

12 Power Supply Recommendations

12.1 Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains

Mixing Supplies: The CDCM6208V2G incorporates a very flexible power supply architecture. Each building block has its own power supply domain, and can be driven independently with 1.8 V, 2.5 V, or 3.3 V . This is especially of advantage to minimize total system cost by deploying multiple low-cost LDOs instead of one, more-expensive LDO. This also allows mixed IO supply voltages (e.g. one CMOS output with 1.8 V, another with 3.3 V) or interfacing to a SPI/I2C controller with 3.3 V supply while other blocks are driven from a lower supply voltage to minimize power consumption. The CDCM6208V2G current consumption is practically independent of the supply voltage, and therefore a lower supply voltage consumes lower device power. Also note that outputs Y3:0 if used for PECL swing will provide higher output swing if the according output domains are connected to 2.5 V or 3.3 V.

Power-on Reset: The CDCM6208V2G integrates a built-in POR circuit, that holds the device in powerdown until all input, digital, and PLL supplies have reached at least 1.06 V (min) to 1.24 V (max). After this power-on release, device internal counters start (see previous section on device power up timing) followed by device calibration. While the device digital circuit resets properly at this supply voltage level, the device is not ready to calibrate at such a low voltage. Therefore, for slow power up ramps, the counters expire before the supply voltage reaches the minimum voltage of 1.71 V. Hence for slow power-supply ramp rates, it is necessary to delay calibration further using the PDN input.

Slow power-up supply ramp: No particular power supply sequence is required for the CDCM6208V2G. However, it is necessary to ensure that device calibration occurs AFTER the DVDD supply as well as the VDD_PLL1, VDD_PLL2, VDD_PRI, and VDD_SEC supply are all operational, and the voltage on each supply is higher than 1.45. This is best realized by delaying the PDN low-to-high transition. The PDN input incorporates a 50 kΩ resistor to DVDD. Assuming the DVDD supply ramp has a fixed time relationship to the slowest of all PLL and input power supplies, a capacitor from PDN to GND can delay the PDN input signal sufficiently to toggle PDN low-to-high AFTER all other supplies are stable. However, if the DVDD supply ramps much sooner than the PLL or input supplies, additional means are necessary to prevent PDN from toggling too early. A premature toggling of PDN would possibly result in failed PLL calibration, which can only be corrected by re-calibrating the PLL by either toggling PDN or RESET high-low-high.

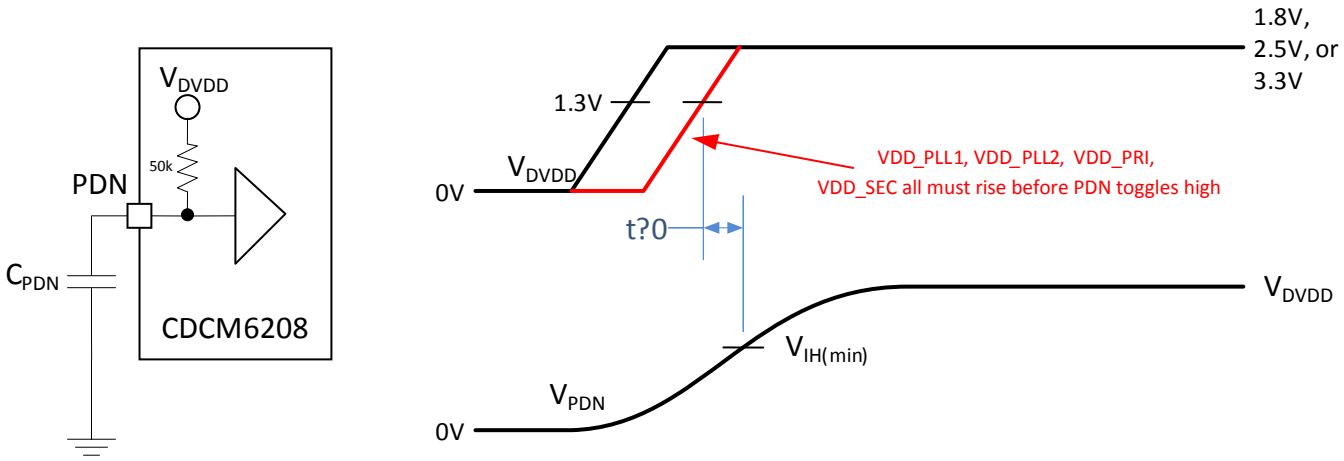


Figure 57. PDN Delay When Using Slow Ramping Power Supplies (Supply Ramp > 50 ms)

12.1.1 Fast Power-up Supply Ramp

If the supply ramp time for DVDD, VDD_PLL1, VDD_PLL2, VDD_PRI, and VDD_SEC are faster than 50 ms from 0 V to 1.8 V, no special provisions are necessary on PDN; the PDN pin can be left floating. Even an external capacitor to GND can be omitted in this circumstance, as the device delays calibration sufficiently by internal means.

Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains (continued)

12.1.2 Delaying VDD_Yx_Yy to Protect DSP IOs

DSPs and other highly integrated processors sometimes do not permit any clock signal to be present until the DSP power supply for the corresponding IO is also present. The CDCM6208V2G allows to either sequence output clock signals by writing to the corresponding output enable bit through SPI/I2C, or alternatively it is possible to connect the DSP IO supply and the CDCM6208V2G output supply together, in which case the CDCM6208V2G output will not turn on until the DSP supply is also valid. This second implementation avoids SPI/I2C programming.

13 Layout

13.1 Layout Guidelines

Employing the thermally enhanced printed circuit board layout shown in Figure 58 insures good thermal performance of the solution. Observing good thermal layout practices enables the thermal pad on the backside of the QFN-48 package to provide a good thermal path between the die contained within the package and the ambient air. This thermal pad also serves as the ground connection the device; therefore, a low inductance connection to the ground plane is essential.

13.2 Layout Example

Figure 58 shows a layout optimized for good thermal performance and a good power supply connection as well. The 7×7 filled via pattern facilitates both considerations.

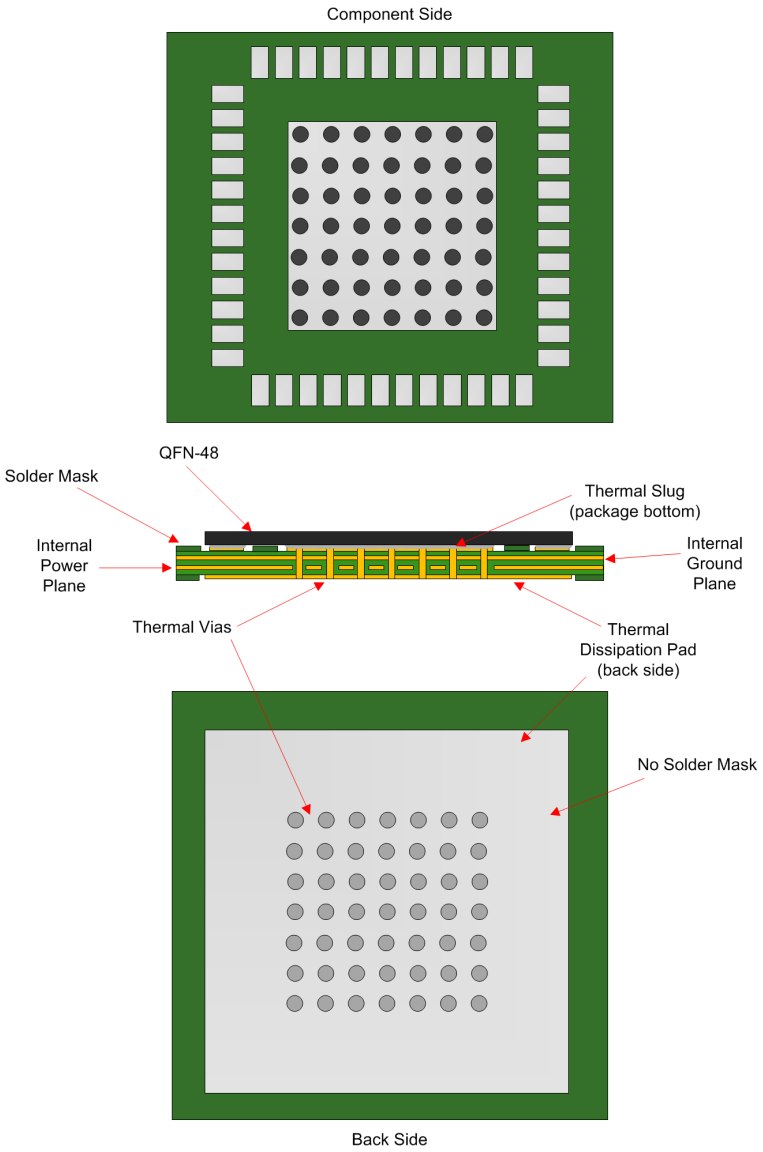


Figure 58. Recommended PCB layout of CDCM6208

Layout Example (continued)

Figure 59 shows two conceptual layouts detailing recommended placement of power supply bypass capacitors. If the capacitors are mounted on the back side, 0402 components can be employed; however, soldering to the Thermal Dissipation Pad can be difficult. For component side mounting, use 0201 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane.

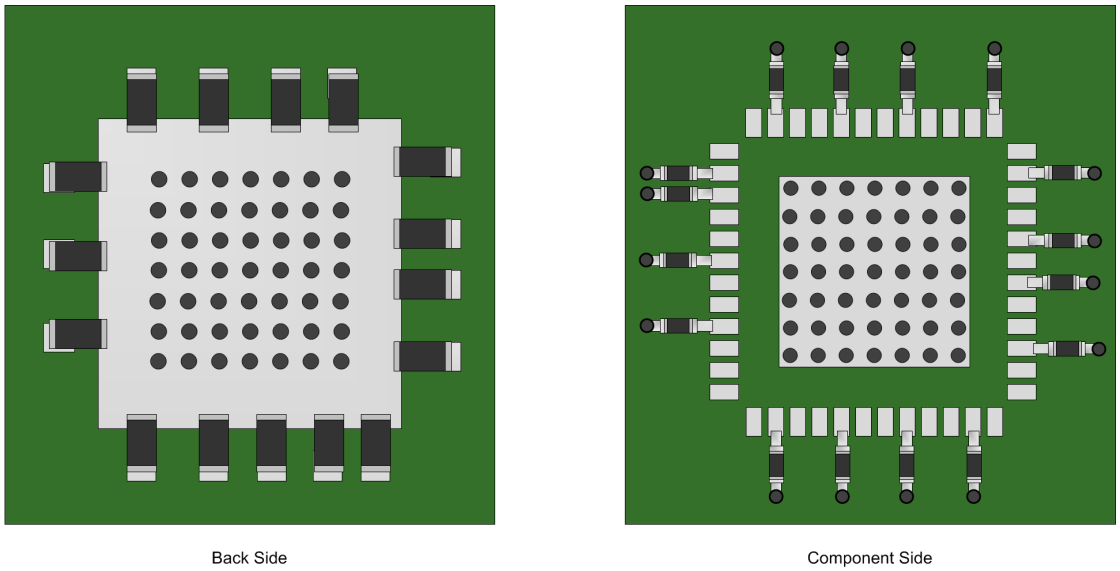


Figure 59. PCB Conceptual Layouts

13.2.1 Reference Schematic

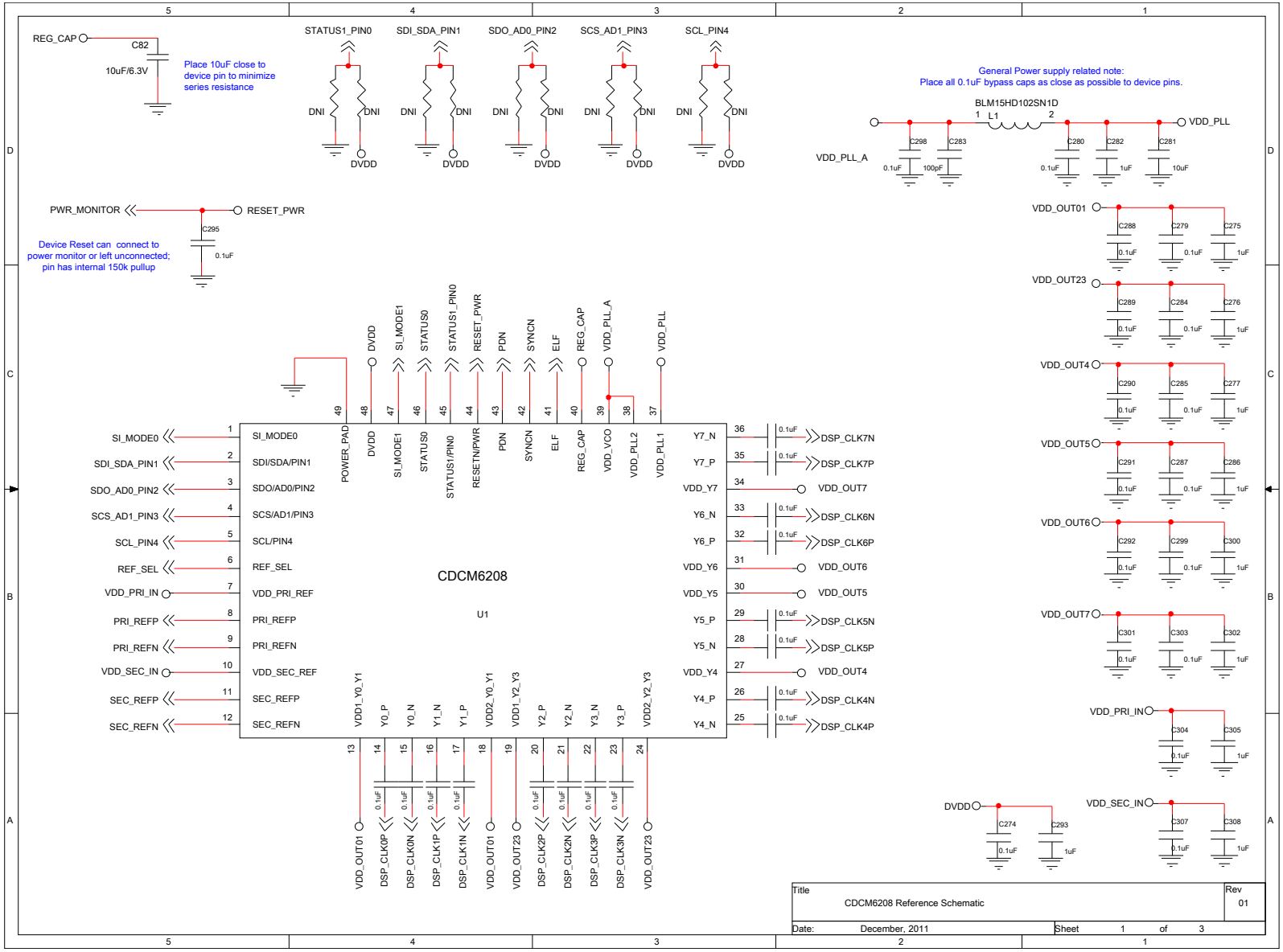


Figure 60. Schematic Page 1

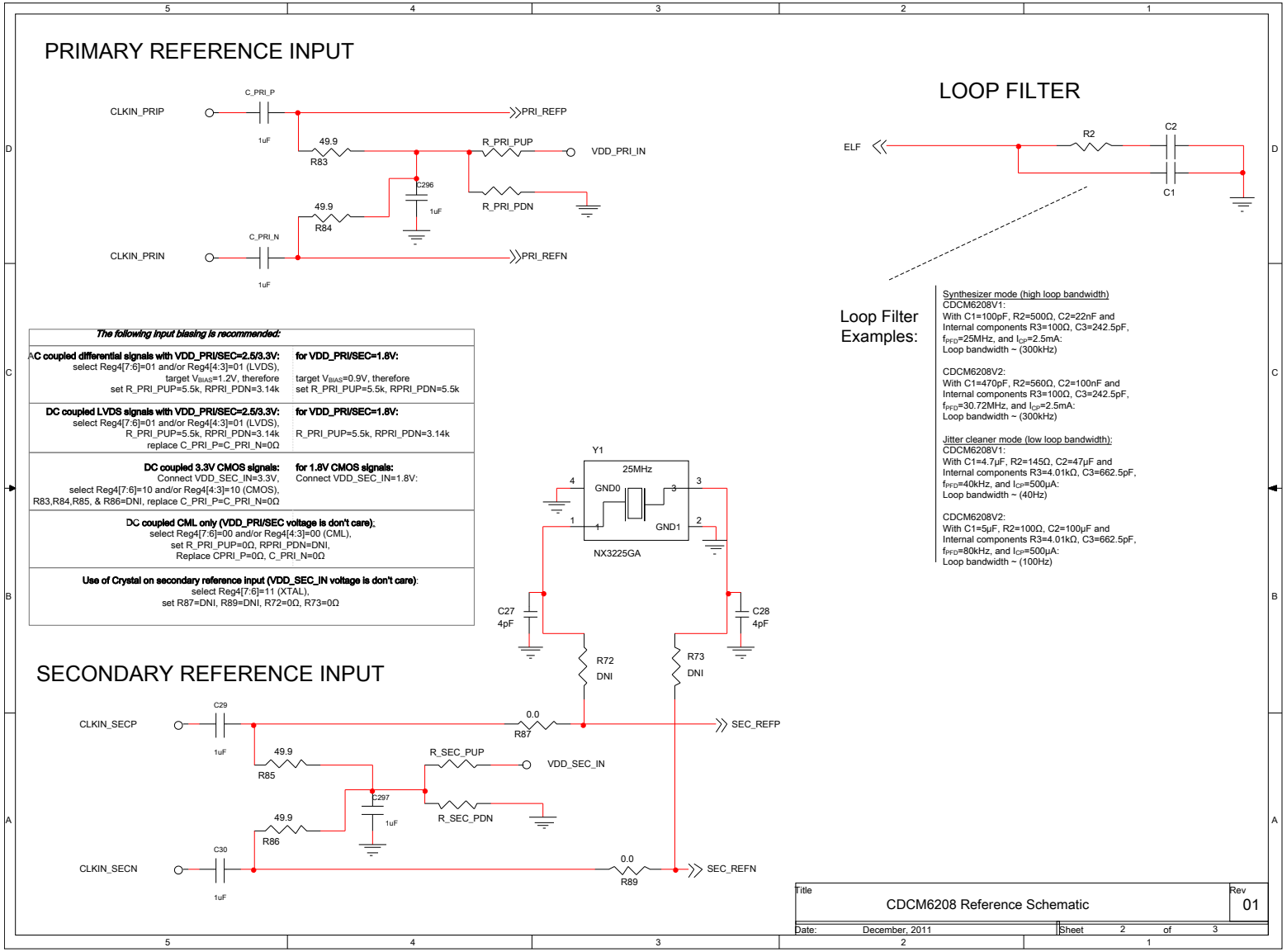


Figure 61. Schematic Page 2

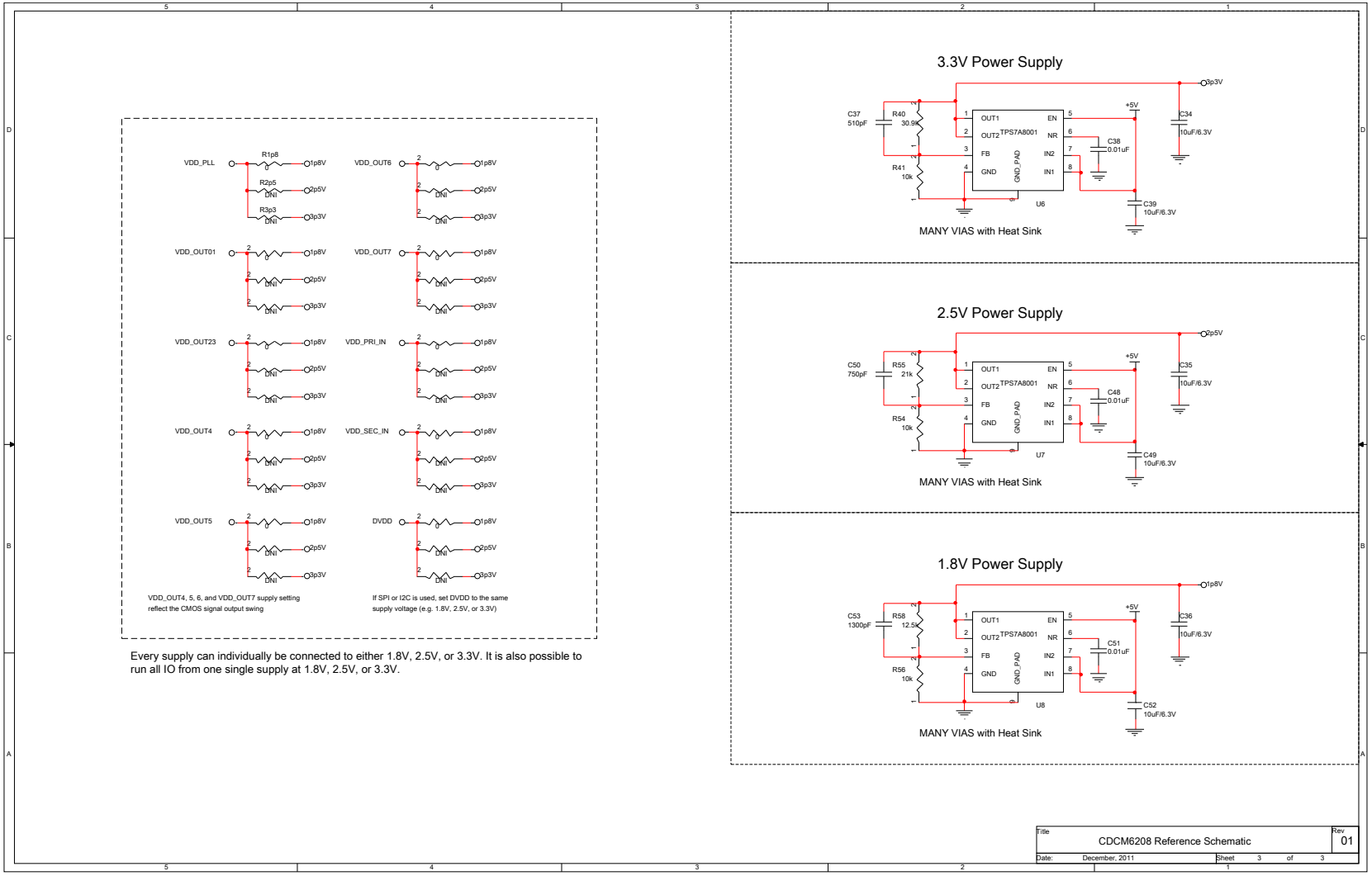


Figure 62. Schematic Page 3

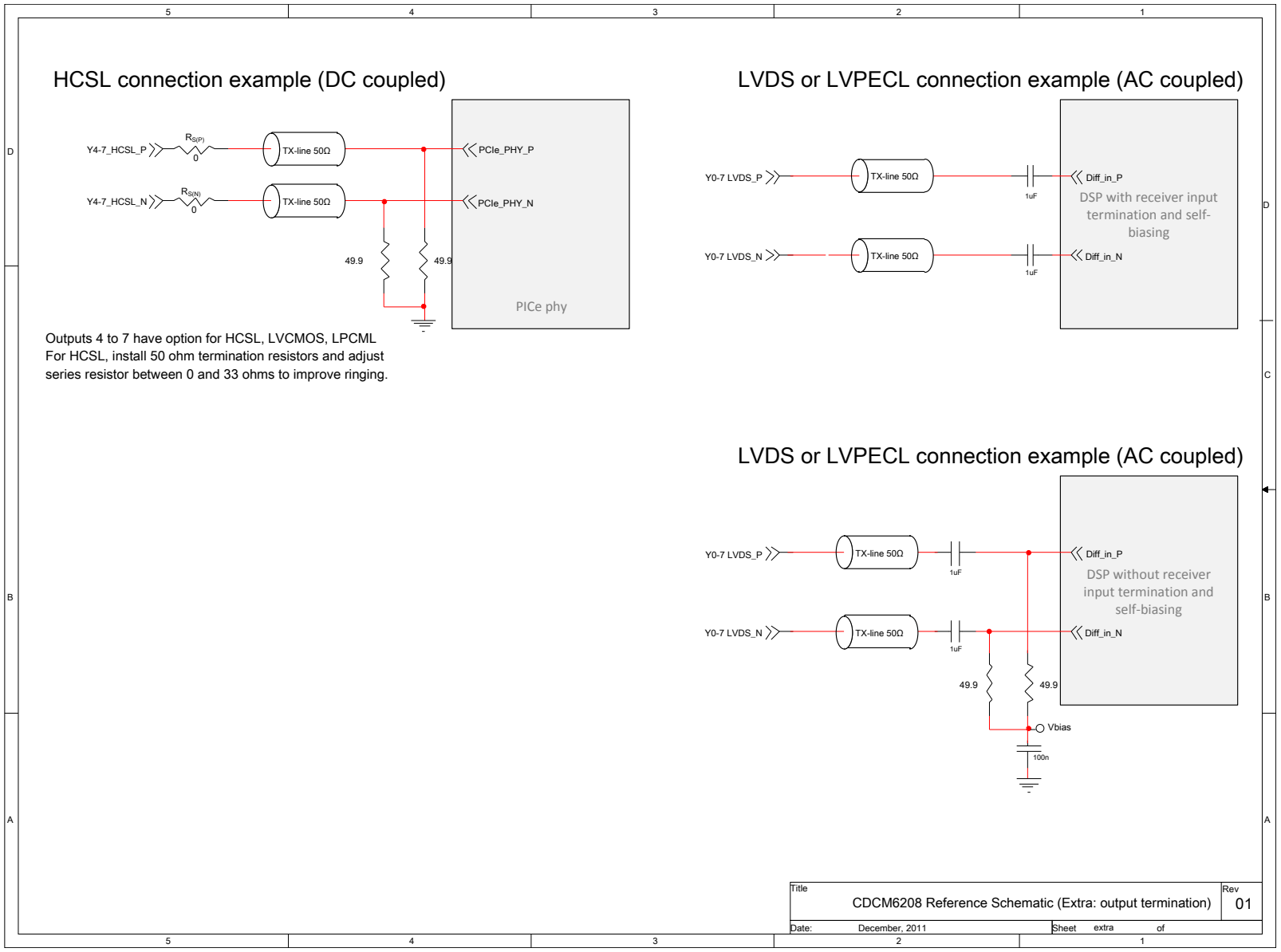


Figure 63. Schematic Page 4

14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Related Documentation

IC Package Thermal Metrics application report, SPRA953.

Hardware Design Guide for KeyStone Devices SPRABI2 for the SRIO interface.

14.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.3 Trademarks

KeyStone, E2E are trademarks of Texas Instruments.
I^2C is a trademark of NXP B.V. Corporation.
All other trademarks are the property of their respective owners.

14.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCM6208V2GRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CM6208V2G	Samples
CDCM6208V2GRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CM6208V2G	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

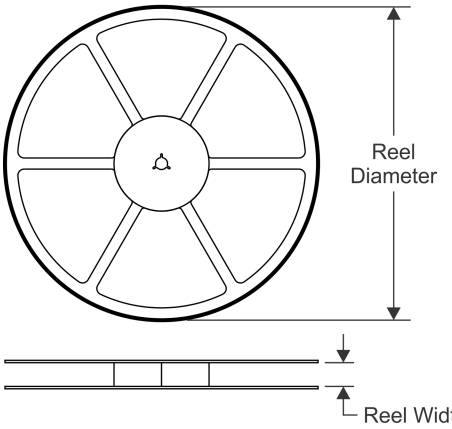
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

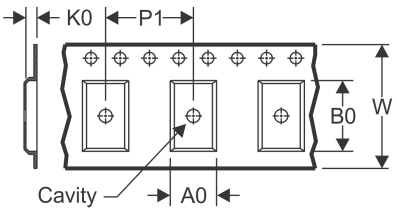
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

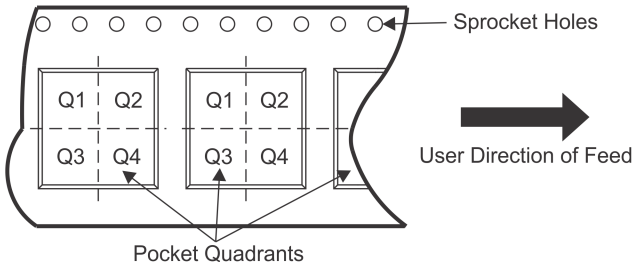


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

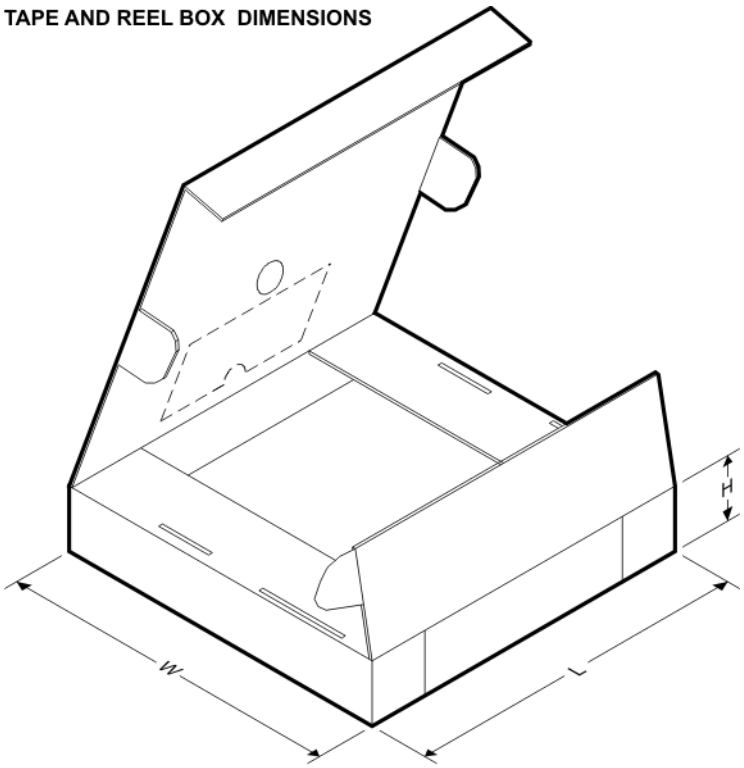
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCM6208V2GRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CDCM6208V2GRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCM6208V2GRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
CDCM6208V2GRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

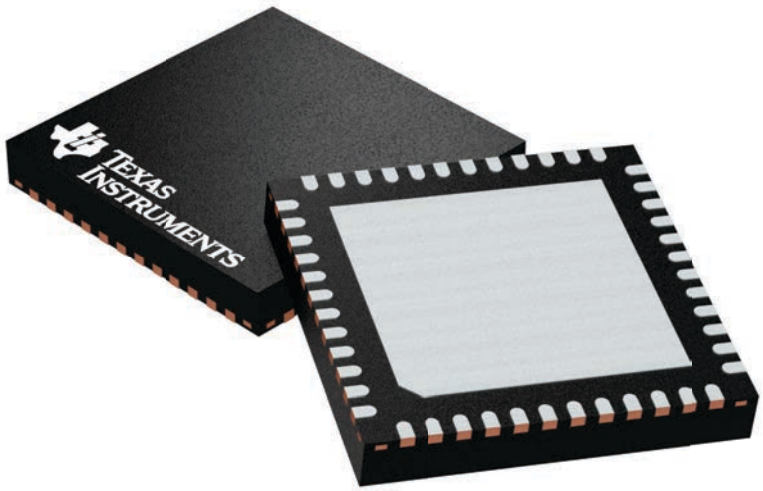
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

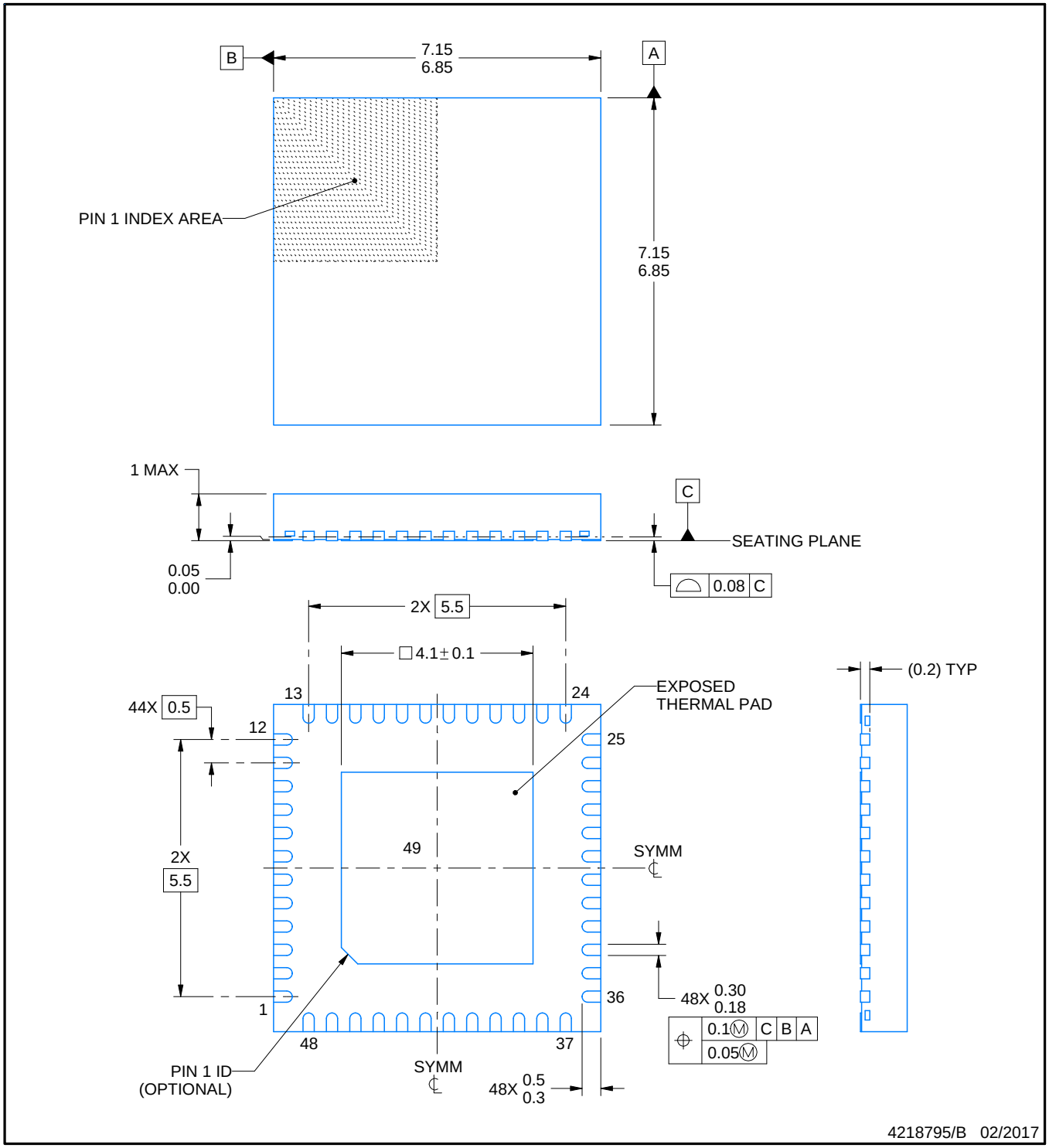
4224671/A

RGZ0048B

PACKAGE OUTLINE

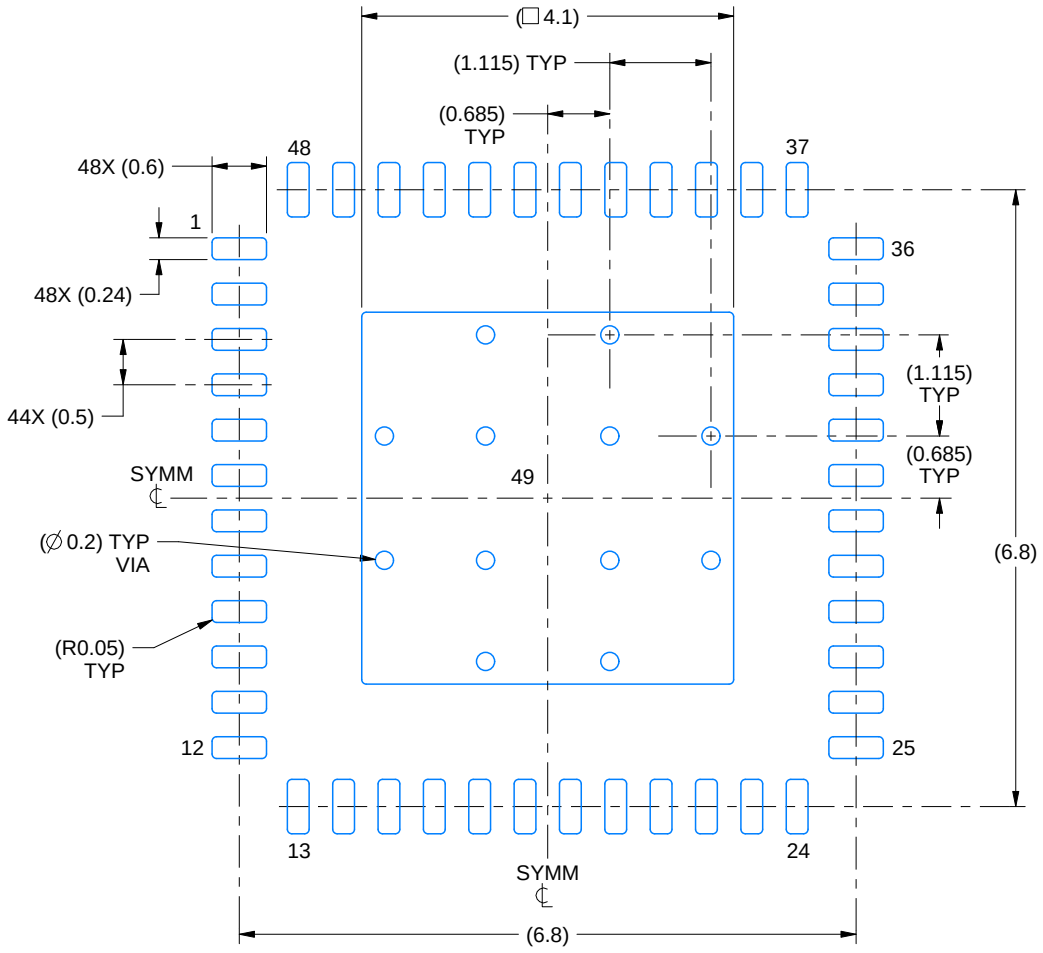
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

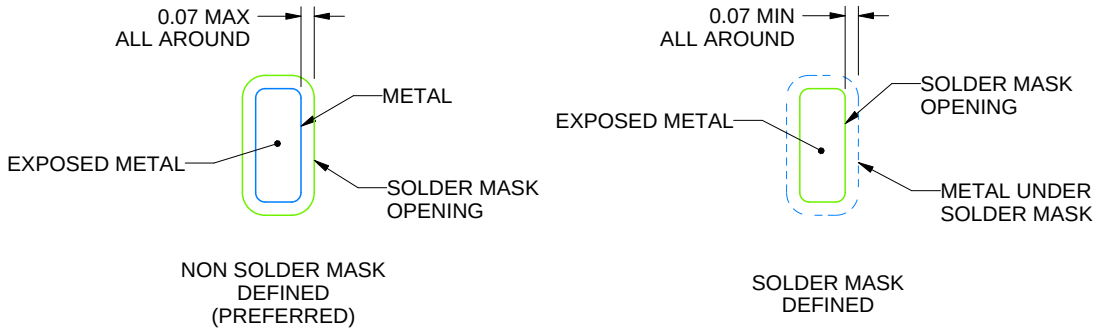


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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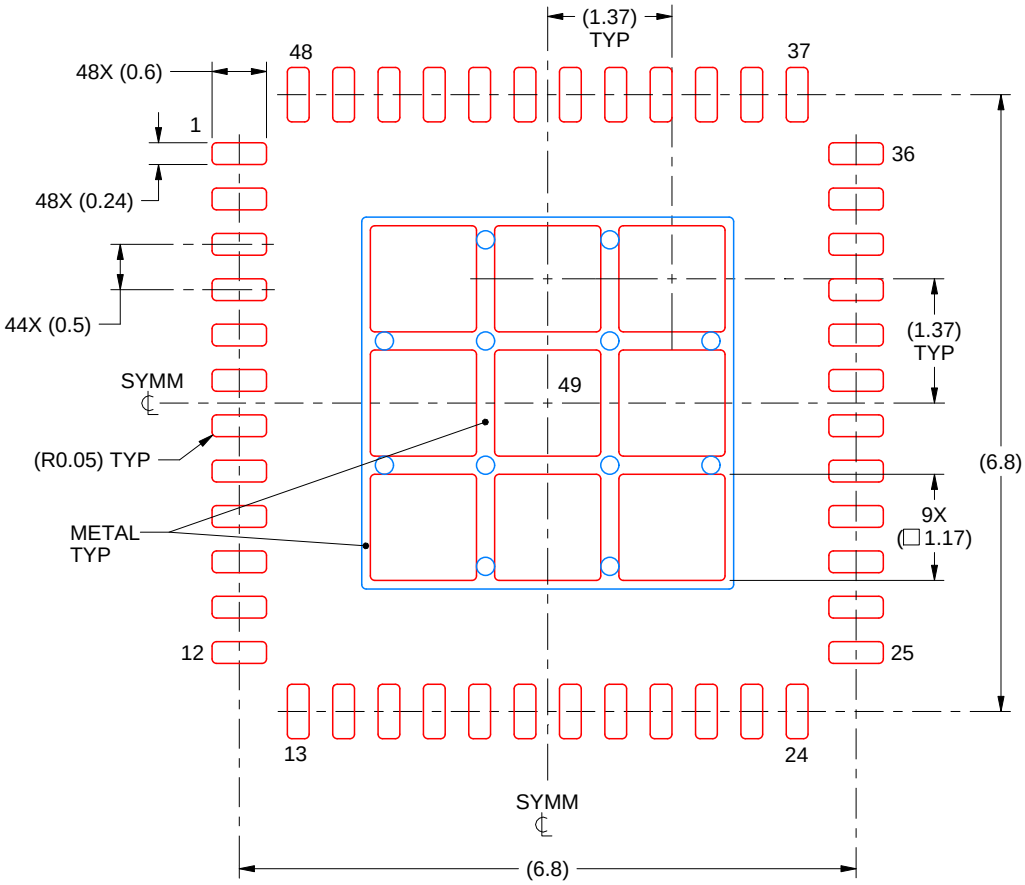
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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