TEXAS INSTRUMENTS

CSD16408Q5

SLPS228B – OCTOBER 2009 – REVISED OCTOBER 2023

N-Channel NexFET™ Power MOSFET

1 Features

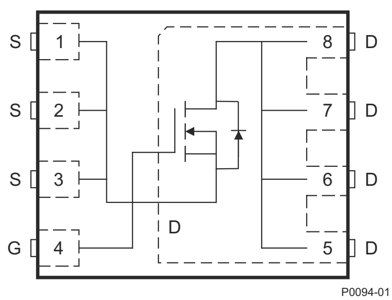
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- SON 5-mm × 6-mm Plastic Package

2 Applications

- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

3 Description

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.



Top View

Product Summary

V_{DS}	Drain-to-source voltage	25		V
Q_g	Gate charge, total (4.5 V)	6.7		nC
Q_{gd}	Gate charge, gate-to-drain	1.9		nC
$r_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V	5.4	mΩ
		V_{GS} = 10 V	3.6	mΩ
$V_{GS(th)}$	Threshold voltage	1.8		V

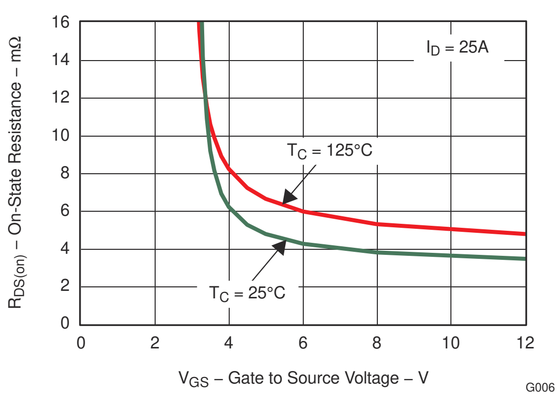
Ordering Information

Device	Package	Media	Qty	Ship
CSD16408Q5	SON 5-mm × 6-mm plastic package	13-inch (33-cm) reel	2500	Tape and reel

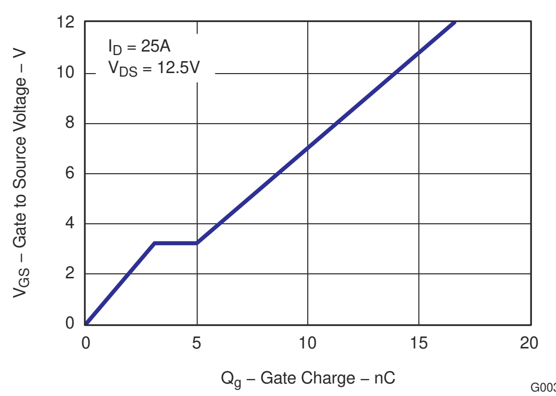
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-source voltage	25	V
V_{GS}	Gate-to-source voltage	–12 to 16	V
I_D	Continuous drain current, T_C = 25°C	113	A
	Continuous drain current(1)	22	A
I_{DM}	Pulsed drain current, T_A = 25°C(2)	141	A
P_D	Power dissipation(1)	3.1	W
T_J, T_{STG}	Operating junction and storage temperature range	–55 to 150	°C
E_{AS}	Avalanche energy, single-pulse I_D = 23 A, L = 0.1 mH, R_G = 25 Ω	126	mJ

(1) Typical $R_{\theta JA}$ = 41°C/W on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.
(2) Pulse duration ≤300 µs, duty cycle ≤2%



$R_{DS(on)}$ vs V_{GS}



GATE CHARGE

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2010) to Revision B (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (October 2009) to Revision A (September 2010)	Page
• Deleted environmental bullets from features list	1

5 Electrical Characteristics

T_A = 25°C unless otherwise stated

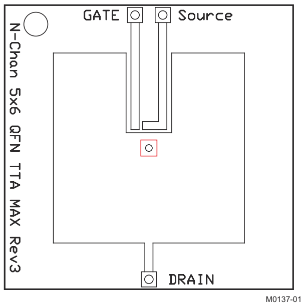
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	25			V
I_{DSS}	Drain-to-source leakage	V_{GS} = 0 V, V_{DS} = 20 V			1	μA
I_{GSS}	Gate-to-source leakage	V_{DS} = 0 V, V_{GS} = –12 V to 16 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.4	1.8	2.1	V
$r_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_D = 25 A		5.4	6.8	mΩ
		V_{GS} = 10 V, I_D = 25 A		3.6	4.5	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 25 A		60		S
Dynamic Characteristics						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V , f = 1 MHz		990	1300	pF
C_{OSS}	Output capacitance			760	1000	pF
C_{RSS}	Reverse transfer capacitance			75	100	pF
R_g	Series gate resistance			0.8	1.6	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 12.5 V, I_D = 25 A		6.7	8.9	nC
Q_{gd}	Gate charge, gate-to-drain			1.9		nC
Q_{gs}	Gate charge, gate-to-source			3.1		nC
$Q_{g(th)}$	Gate charge at Vth			1.8		nC
Q_{OSS}	Output charge	V_{DS} = 13 V, V_{GS} = 0 V		15.7		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 20 A, R_G = 2 Ω		11.3		ns
t_r	Rise time			25		ns
$t_{d(off)}$	Turnoff delay time			11		ns
t_f	Fall time			10.8		ns
Diode Characteristics						
V_{SD}	Diode forward voltage	I_S = 25 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 13 V, I_F = 2 5A, di/dt = 300 A/μs		17		nC
t_{rr}	Reverse recovery time	V_{DD} = 13 V, I_F = 25 A, di/dt = 300 A/μs		21		ns

6 Thermal Characteristics

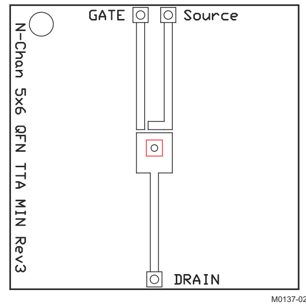
T_A = 25°C unless otherwise stated

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			1.9	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			51	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 51°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

7 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated

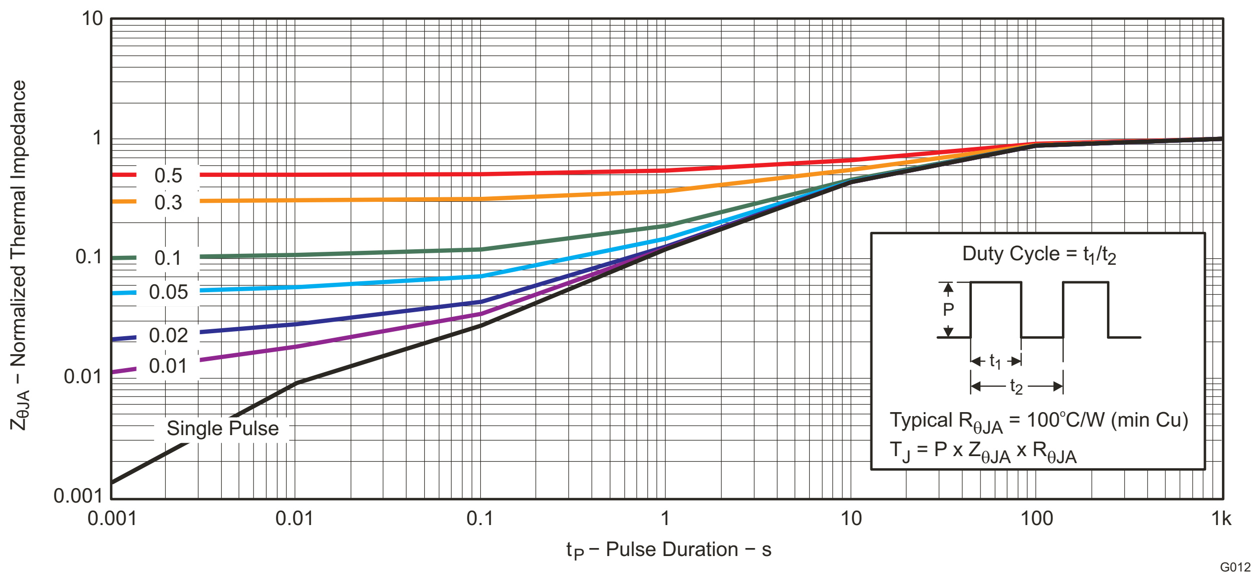


Figure 7-1. Transient Thermal Impedance

7 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated

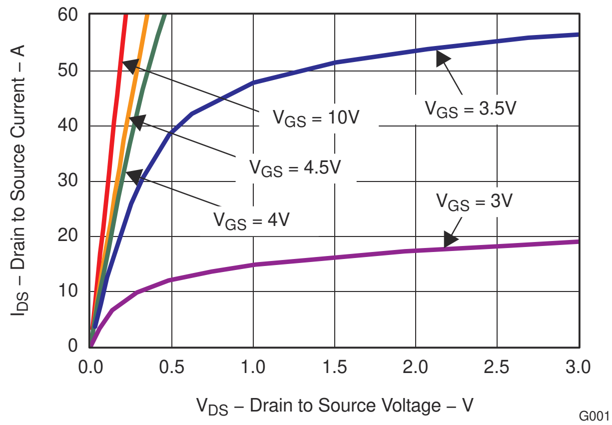


Figure 7-2. Saturation Characteristics

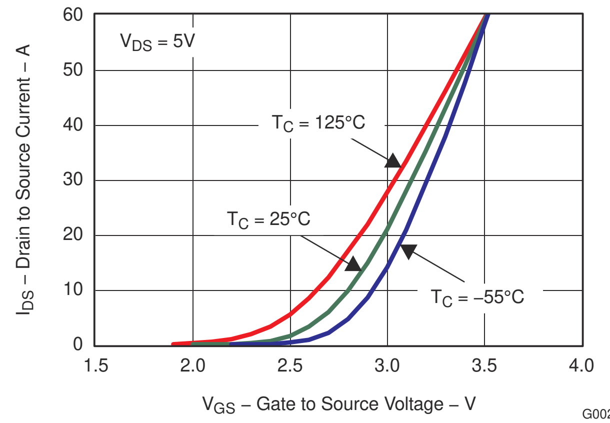


Figure 7-3. Transfer Characteristics

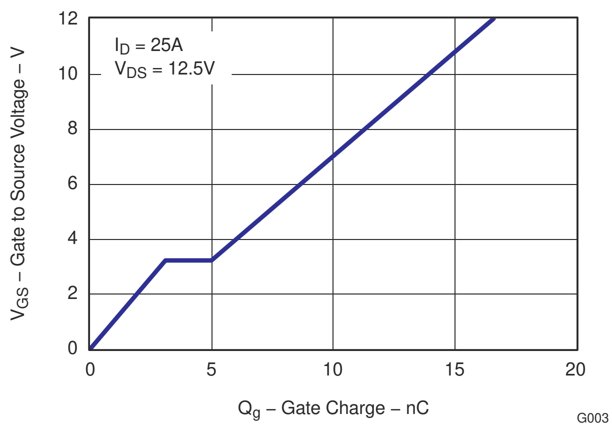


Figure 7-4. Gate Charge

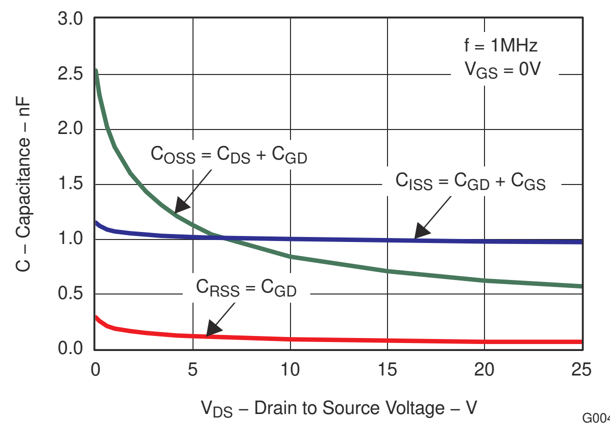


Figure 7-5. Capacitance

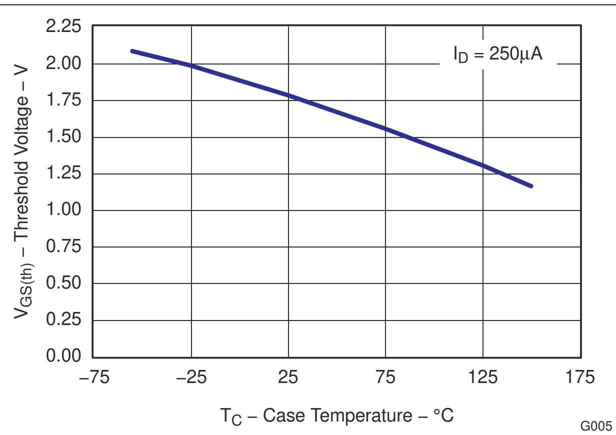


Figure 7-6. Threshold Voltage vs. Temperature

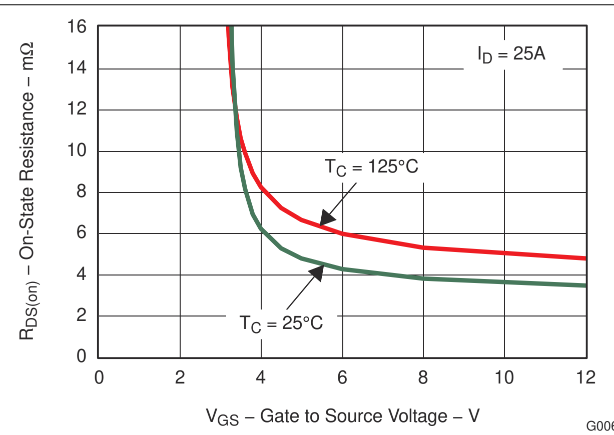


Figure 7-7. On-State Resistance vs. Gate-to-Source Voltage

7 Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

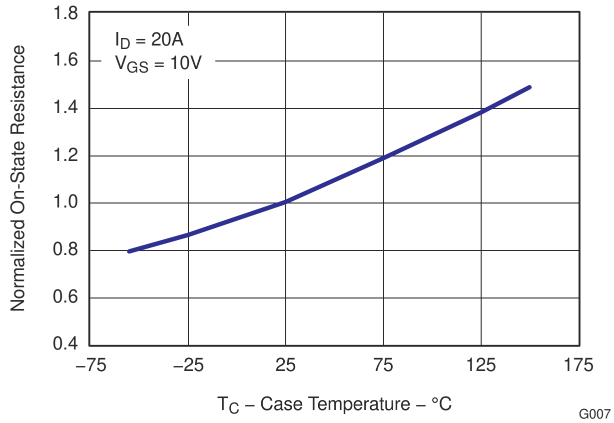


Figure 7-8. Normalized On-State Resistance vs. Temperature

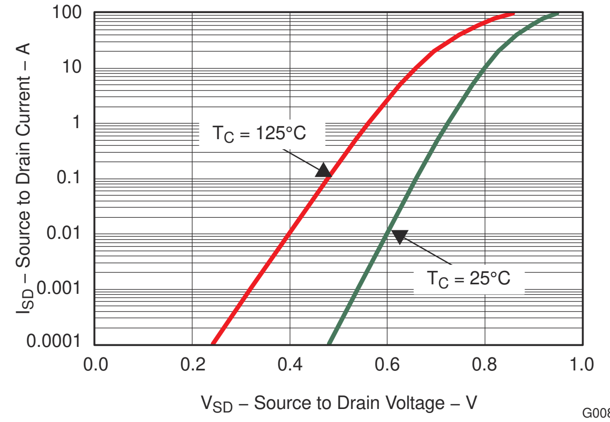


Figure 7-9. Typical Diode Forward Voltage

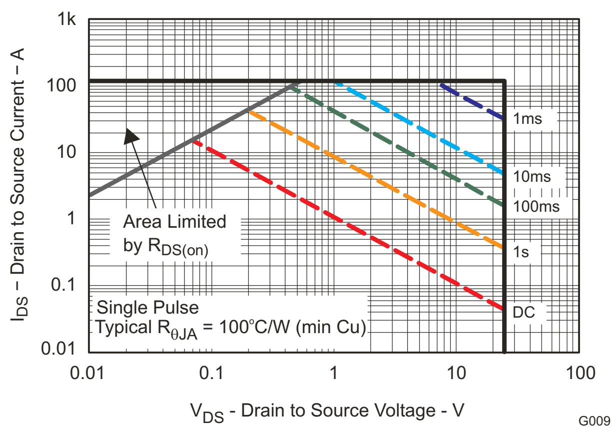


Figure 7-10. Maximum Safe Operating Area

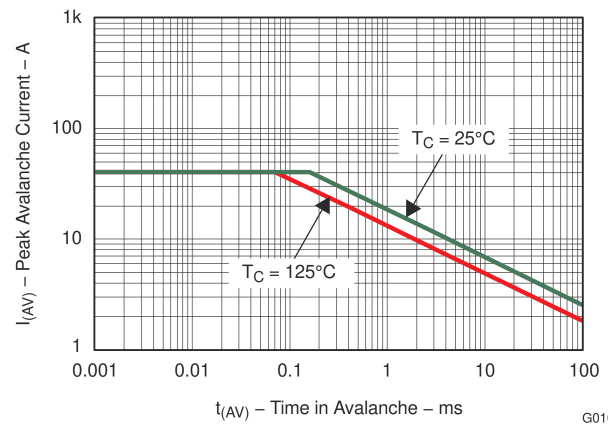


Figure 7-11. Single-Pulse Unclamped Inductive Switching

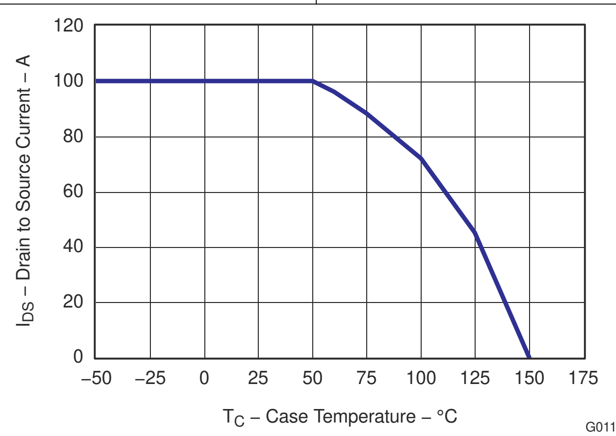


Figure 7-12. Maximum Drain Current vs. Temperature

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16408Q5	ACTIVE	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16408	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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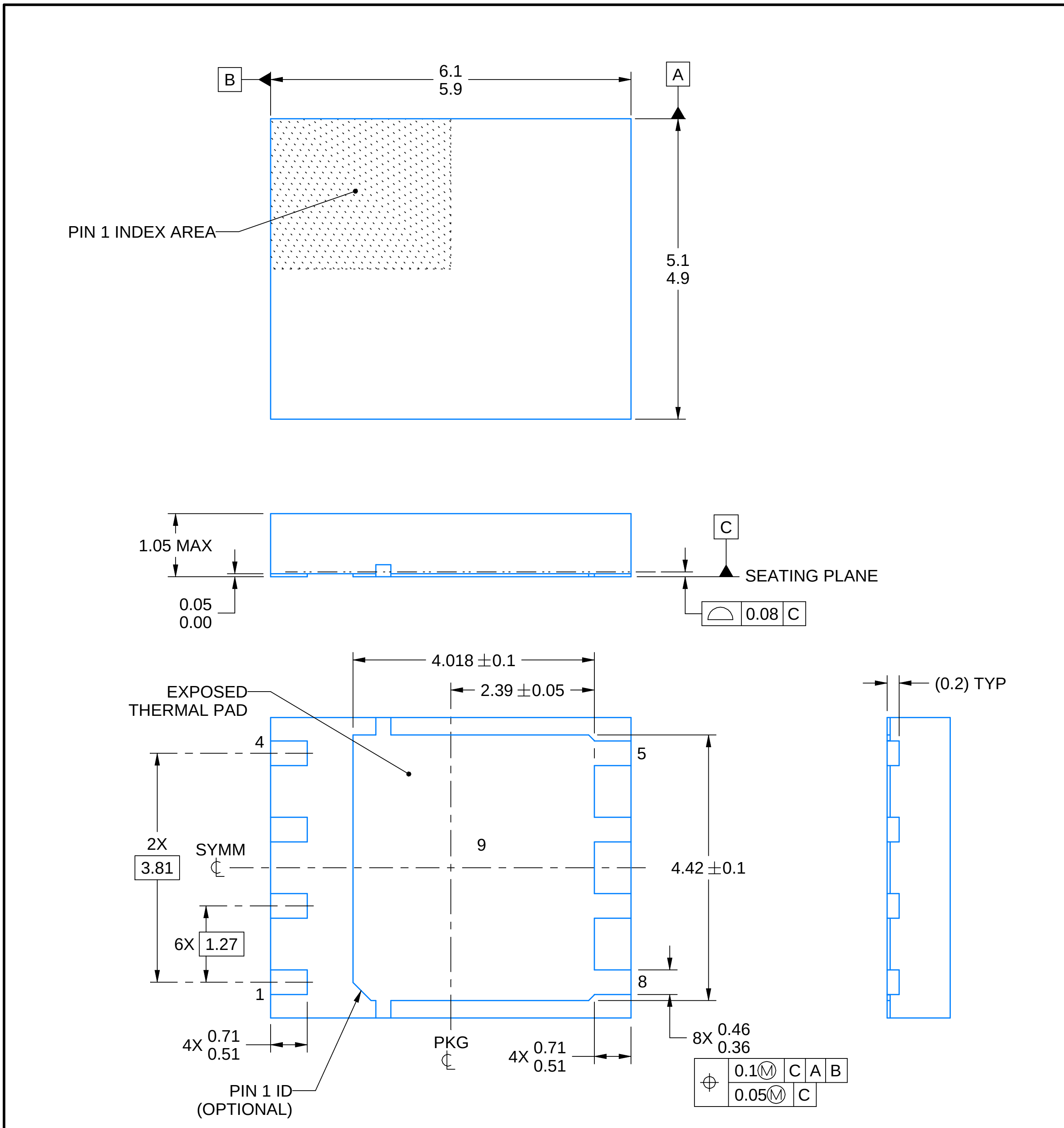

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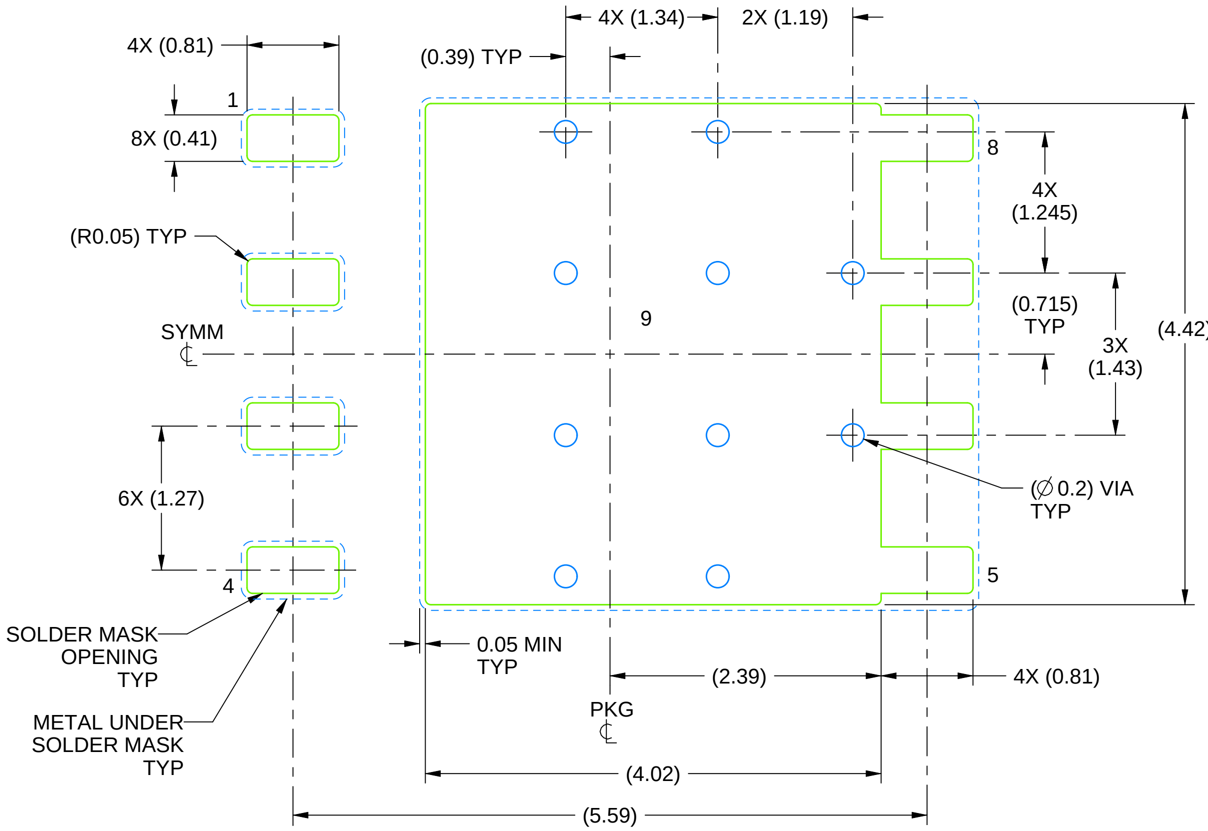
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:15X

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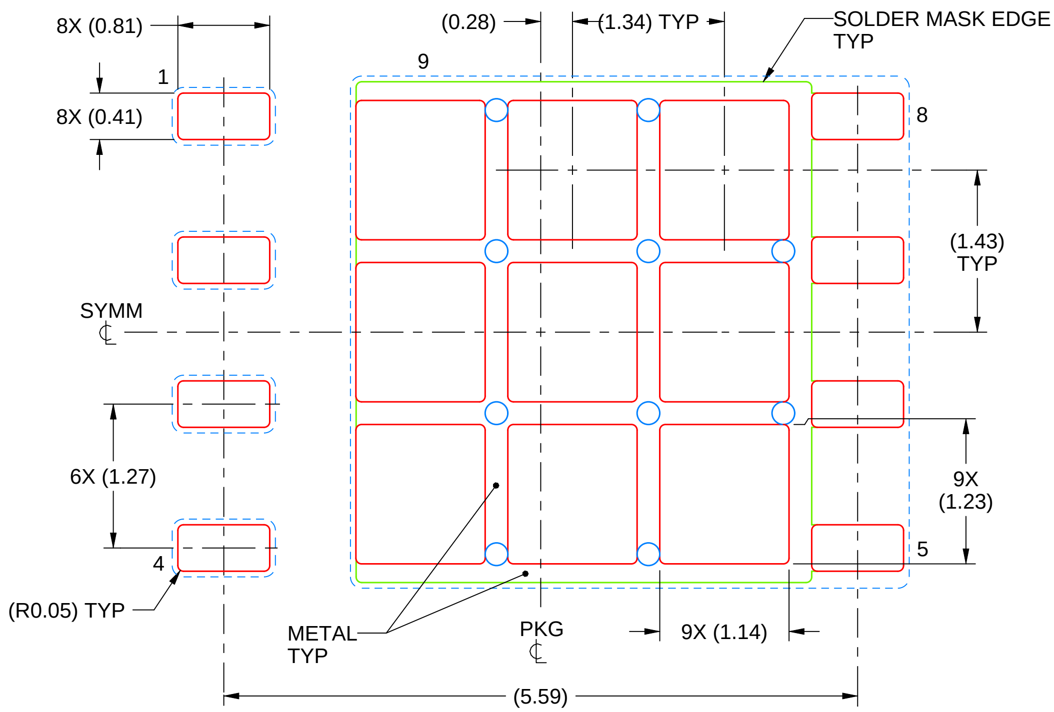
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.