

# CSD25483F4 20-V P-Channel FemtoFET™ MOSFET

## 1 Features

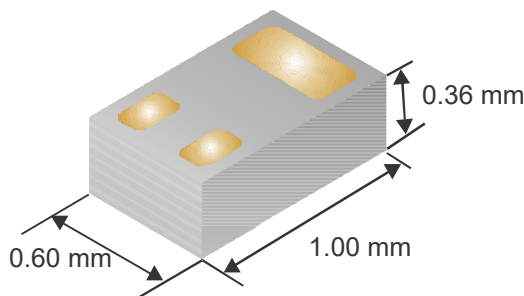
- Ultra-low on-resistance
- Ultra-low  $Q_g$  and  $Q_{gd}$
- High operating drain current
- Ultra-small footprint (0402 case size)
  - 1.0 mm × 0.6 mm
- Ultra-low profile
  - Maximum height: 0.36-mm
- Integrated ESD protection diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

## 2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

## 3 Description

This 210-m $\Omega$ , 20-V P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.



Typical Device Dimensions

## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
$V_{DS}$	Drain-to-source voltage	-20	V
$Q_g$	Gate charge total (-4.5 V)	959	pC
$Q_{gd}$	Gate charge gate-to-drain	161	pC
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = -1.8\text{ V}$	530 m $\Omega$
		$V_{GS} = -2.5\text{ V}$	338 m $\Omega$
		$V_{GS} = -4.5\text{ V}$	210 m $\Omega$
$V_{GS(th)}$	Threshold voltage	-0.95	V

## Ordering Information<sup>(1)</sup>

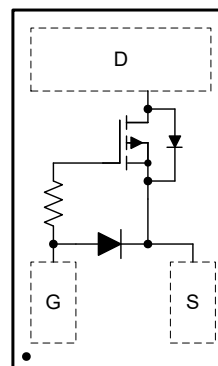
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD25483F4	3000	7-Inch Reel	Femto (0402) 1.0-mm × 0.6-mm Land Grid Array (LGA)	Tape and Reel
CSD25483F4T	250			

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-source voltage	-20	V
$V_{GS}$	Gate-to-source voltage	-12	V
$I_D$	Continuous drain current <sup>(1)</sup>	-1.6	A
$I_{DM}$	Pulsed drain current <sup>(2)</sup>	-6.5	A
$I_G$	Continuous gate clamp current	-35	mA
	Pulsed gate clamp current <sup>(2)</sup>	-350	
$P_D$	Power dissipation <sup>(1)</sup>	500	mW
$V_{(ESD)}$	Human body model (HBM)	4	kV
	Charged device model (CDM)	2	
$T_J, T_{stg}$	Operating junction and storage temperature range	-55 to 150	$^\circ\text{C}$

- (1) Typical  $R_{\theta JA} = 85^\circ\text{C}/\text{W}$  on 1-inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2-oz. (0.071 mm thick) Cu pad on a 0.06-inch (1.52 mm) thick FR4 PCB.
- (2) Pulse duration  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$



Top View



## Table of Contents

<b>1 Features</b> .....	1	6.1 Trademarks.....	6
<b>2 Applications</b> .....	1	6.2 Electrostatic Discharge Caution.....	6
<b>3 Description</b> .....	1	6.3 Glossary.....	6
<b>4 Revision History</b> .....	2	<b>7 Mechanical Data</b> .....	7
<b>5 Specifications</b> .....	3	7.1 Mechanical Dimensions.....	7
5.1 Electrical Characteristics.....	3	7.2 Recommended Minimum PCB Layout.....	8
5.2 Thermal Information.....	3	7.3 Recommended Stencil Pattern.....	8
5.3 Typical MOSFET Characteristics.....	4	7.4 CSD25483F4 Embossed Carrier Tape Dimensions....	9
<b>6 Device and Documentation Support</b> .....	6		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision E (October 2021) to Revision F (January 2022)</b>	<b>Page</b>
• Changed Maximum height from "0.35 mm" to "0.36 mm" in <i>Features</i> .....	1
• Changed height dimension from "0.35 mm" to "0.36 mm" in <i>Typical Device Dimensions</i> .....	1
• Changed maximum height dimension from "0.35 mm" to "0.36 mm" in <i>Mechanical Dimensions</i> .....	7
<b>Changes from Revision D (October 2014) to Revision E (October 2021)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added footnote with link to support document.....	8
<b>Changes from Revision C (July 2014) to Revision D (October 2014)</b>	<b>Page</b>
• Corrected timing $V_{DS}$ to read $-10\text{ V}$ .....	3
<b>Changes from Revision B (February 2014) to Revision C (July 2014)</b>	<b>Page</b>
• Corrected capacitance units to read pF in <a href="#">Figure 5-5</a> .....	4
<b>Changes from Revision A (December 2013) to Revision B (February 2014)</b>	<b>Page</b>
• Updated lead and halogen free in features .....	1
• Added $I_G$ parameter.....	1
• Lowered $I_{DSS}$ limit.....	3
• Lowered $I_{GSS}$ limit.....	3
<b>Changes from Revision * (October 2013) to Revision A (December 2013)</b>	<b>Page</b>
• Fixed resistance typo.....	1
• Added small reel.....	1

## 5 Specifications

### 5.1 Electrical Characteristics

(T<sub>A</sub> = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
B <sub>V</sub> DSS	Drain-to-Source Voltage	V <sub>GS</sub> = 0 V, I <sub>DS</sub> = -250 μA	-20			V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -16 V			-100	nA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -12 V			-50	nA
V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = -250 μA	-0.70	-0.95	-1.2	V
R <sub>DS(on)</sub>	Drain-to-Source On-Resistance	V <sub>GS</sub> = -1.8 V, I <sub>DS</sub> = -0.1 A		530	1070	mΩ
		V <sub>GS</sub> = -2.5 V, I <sub>DS</sub> = -0.5 A		338	390	mΩ
		V <sub>GS</sub> = -4.5 V, I <sub>DS</sub> = -0.5 A		210	245	mΩ
		V <sub>GS</sub> = -8 V, I <sub>DS</sub> = -0.5 A		175	205	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = -10 V, I <sub>DS</sub> = -0.5 A		1.4		S
<b>DYNAMIC CHARACTERISTICS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -10 V, f = 1 MHz		198		pF
C <sub>oss</sub>	Output Capacitance			82		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			5.8		pF
R <sub>G</sub>	Series Gate Resistance			20		Ω
Q <sub>g</sub>	Gate Charge Total (4.5 V)	V <sub>DS</sub> = -10 V, I <sub>DS</sub> = -0.5 A		959		pC
Q <sub>gd</sub>	Gate Charge Gate-to-Drain			160		pC
Q <sub>gs</sub>	Gate Charge Gate-to-Source			252		pC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>			122		pC
Q <sub>oss</sub>	Output Charge	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V		1081		pC
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>DS</sub> = -0.5 A, R <sub>G</sub> = 2 Ω		4.3		ns
t <sub>r</sub>	Rise Time			3.7		ns
t <sub>d(off)</sub>	Turn Off Delay Time			17.4		ns
t <sub>f</sub>	Fall Time			7		ns
<b>DIODE CHARACTERISTICS</b>						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>SD</sub> = -0.5 A, V <sub>GS</sub> = 0 V		-0.75		V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DS</sub> = -10 V, I <sub>F</sub> = -0.5 A, di/dt = 100 A/μs		1060		pC
t <sub>rr</sub>	Reverse Recovery Time			7.5		ns

### 5.2 Thermal Information

(T<sub>A</sub> = 25°C unless otherwise stated)

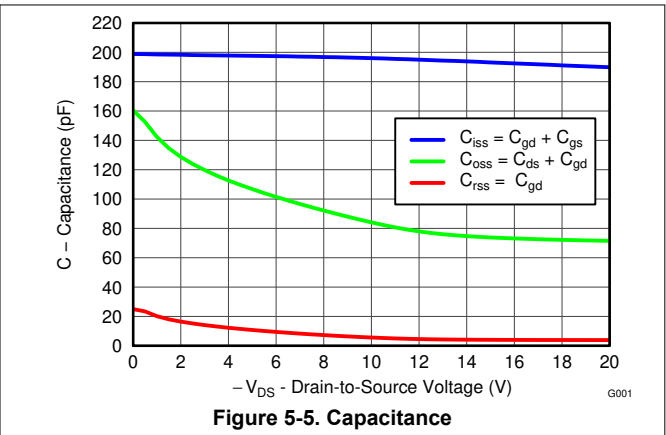
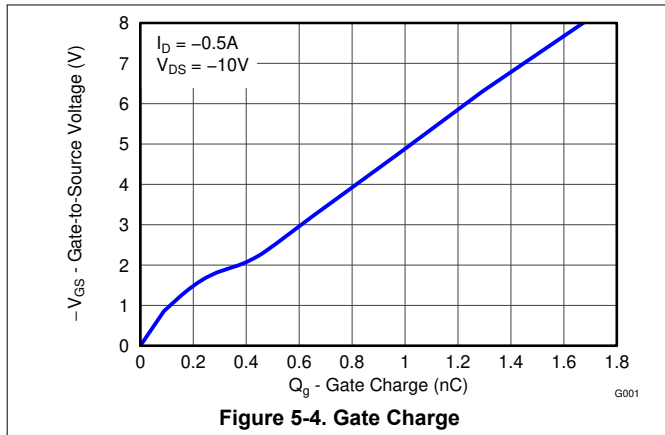
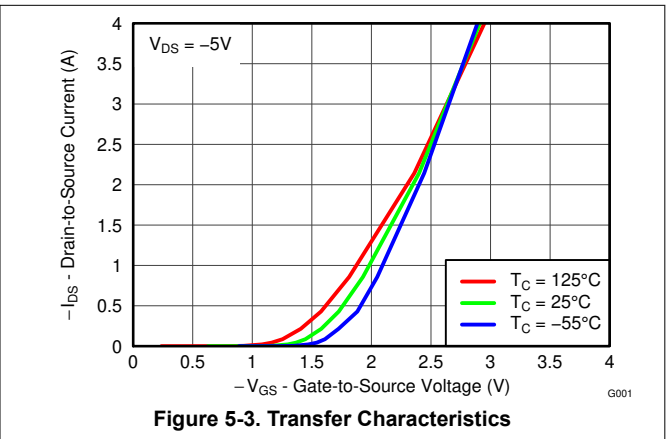
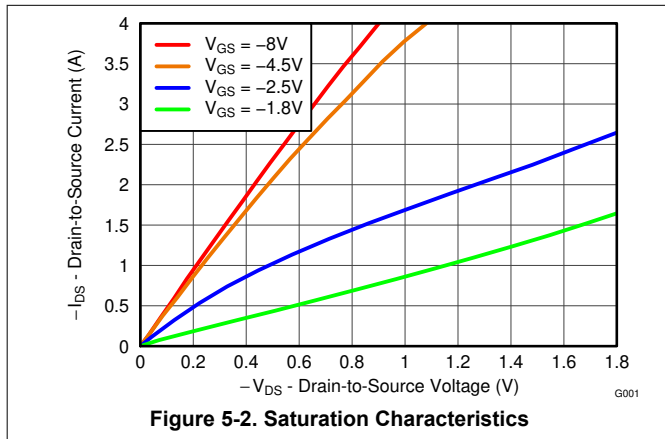
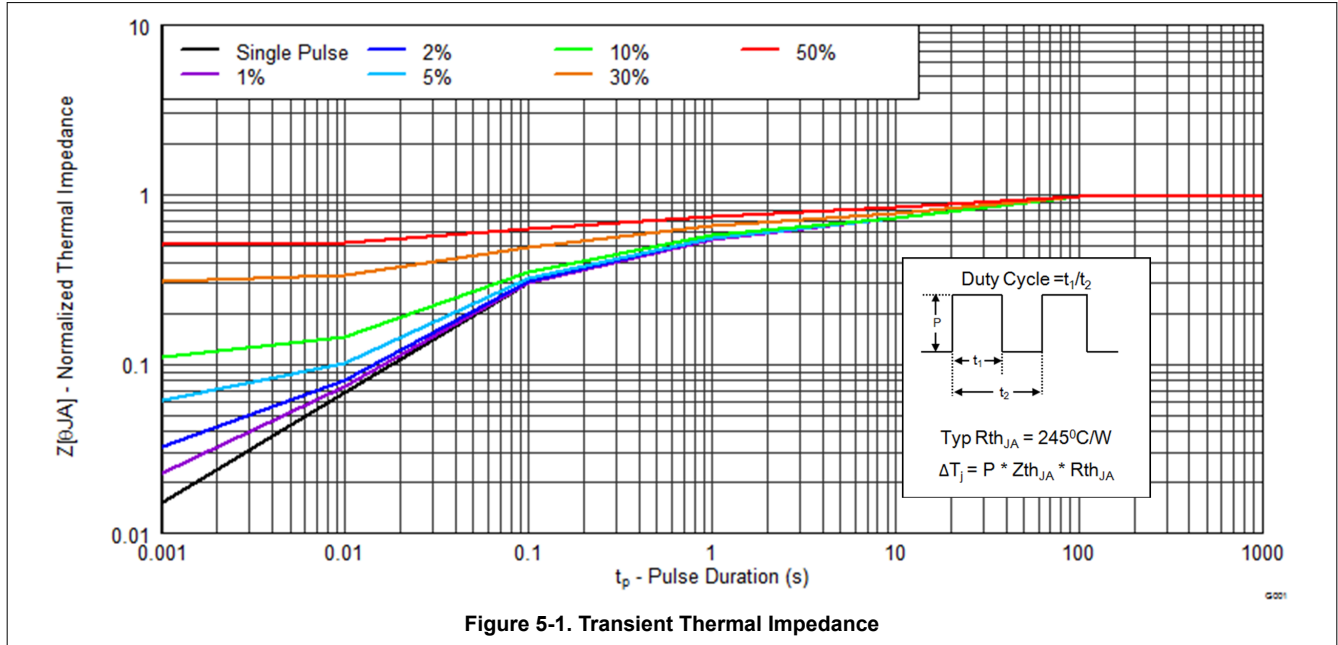
THERMAL METRIC		TYPICAL VALUES	UNIT
R <sub>θJA</sub>	Junction-to-Ambient Thermal Resistance <sup>(1)</sup>	85	°C/W
	Junction-to-Ambient Thermal Resistance <sup>(2)</sup>	245	

(1) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

### 5.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



### 5.3 Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

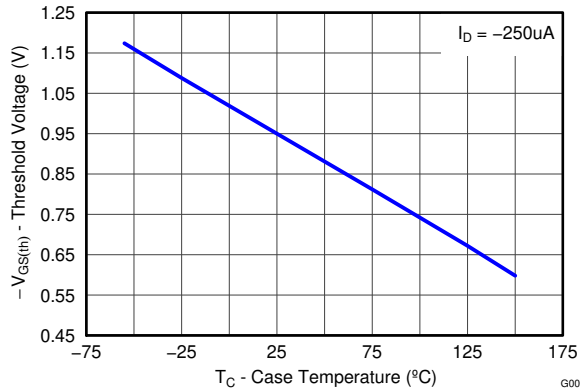


Figure 5-6. Threshold Voltage vs Temperature

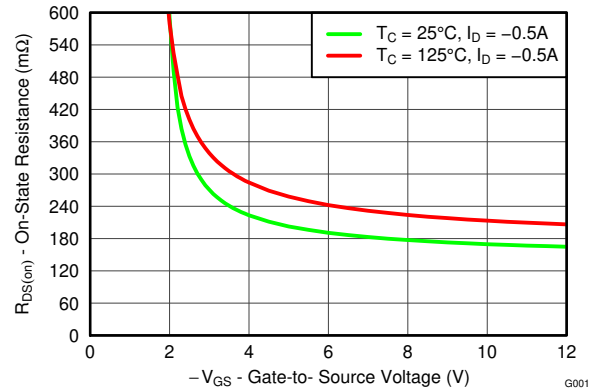


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage

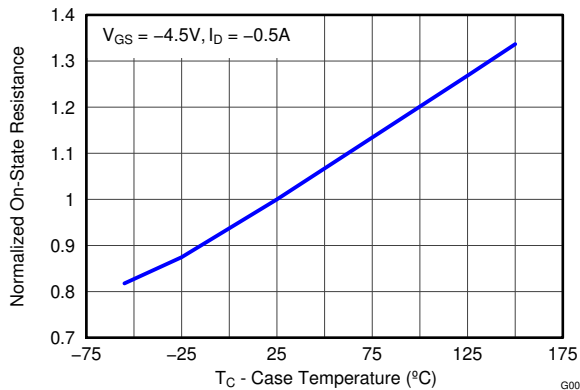


Figure 5-8. Normalized On-State Resistance vs Temperature

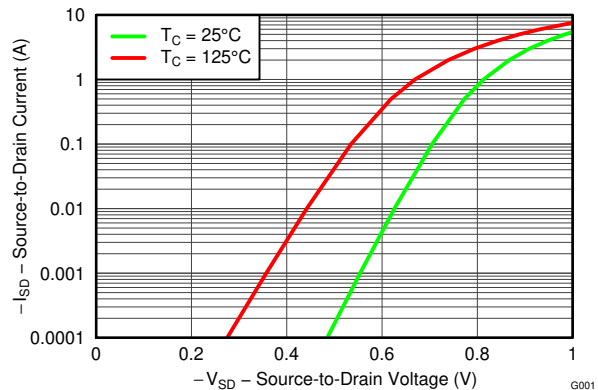


Figure 5-9. Typical Diode Forward Voltage

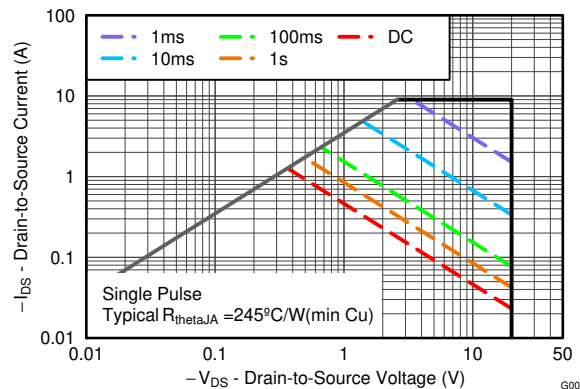


Figure 5-10. Maximum Safe Operating Area

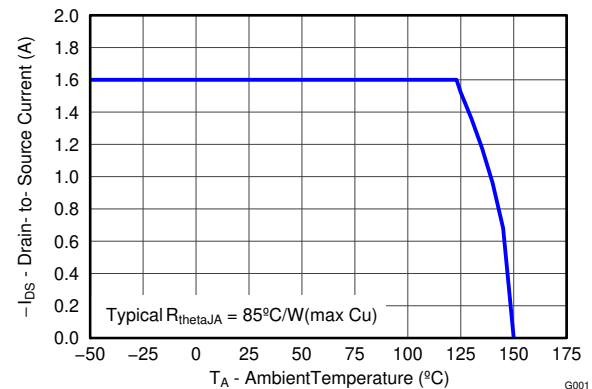


Figure 5-11. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Trademarks

FemtoFET™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 6.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

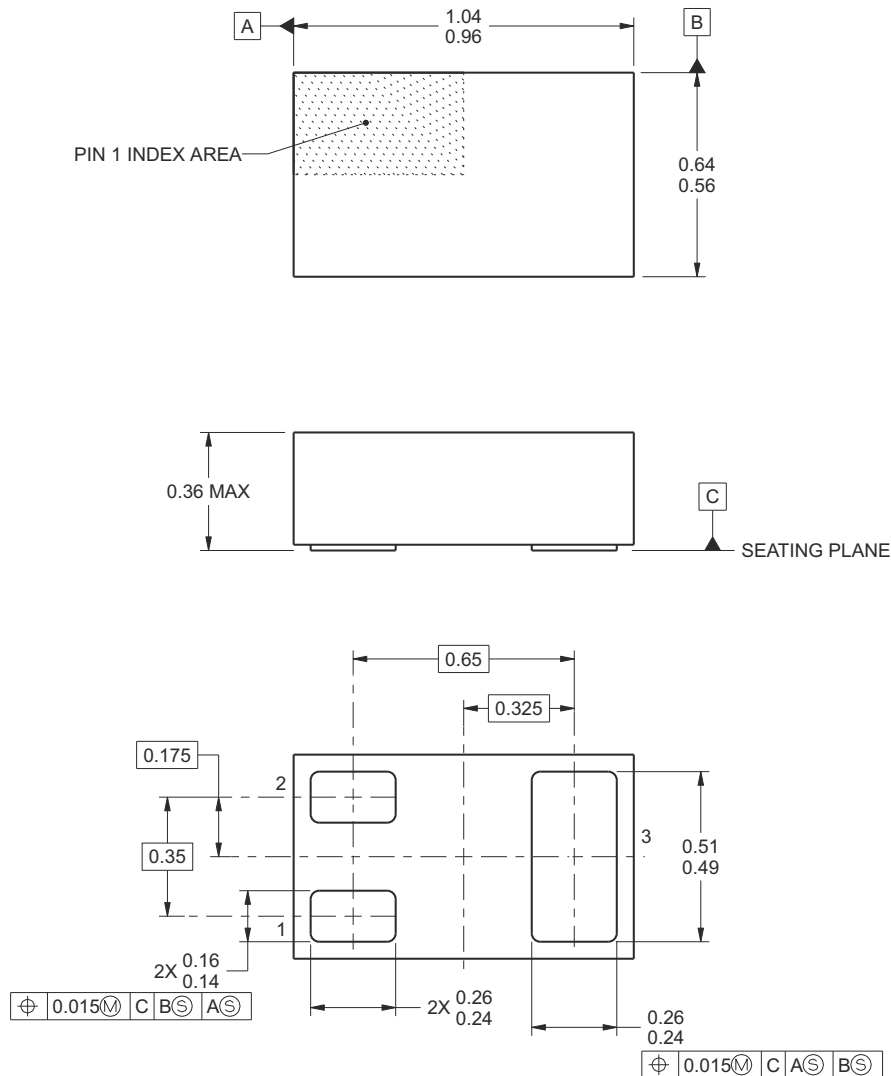
### 6.3 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical Data

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Mechanical Dimensions

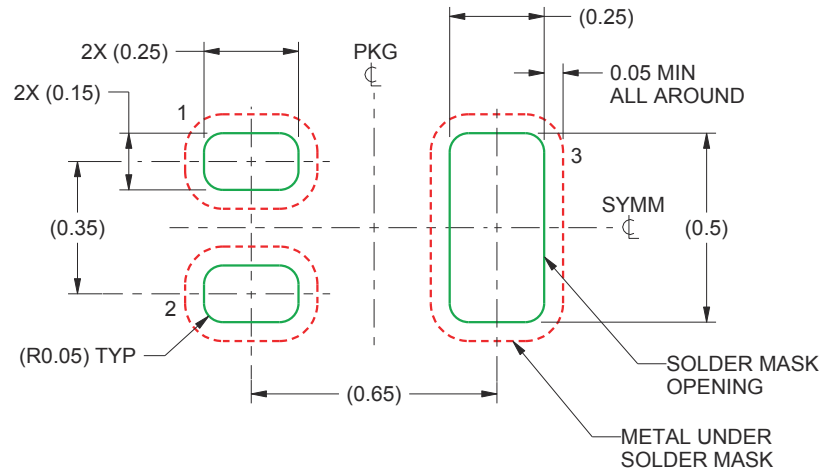


- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a PB-free solder land design.

#### Pin Configuration

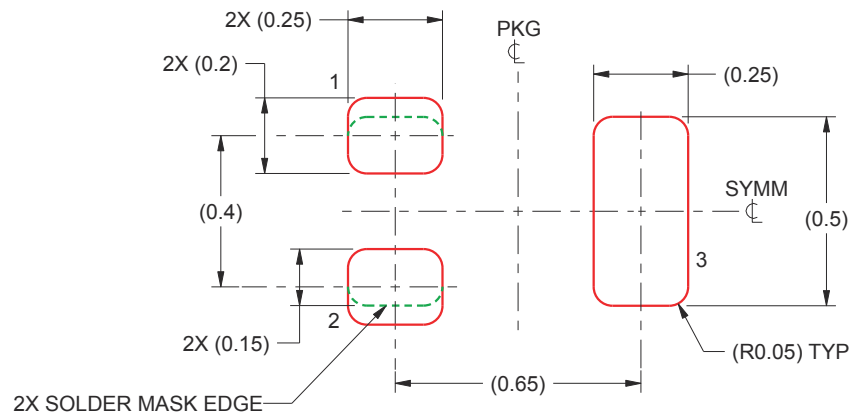
Position	Designation
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

## 7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

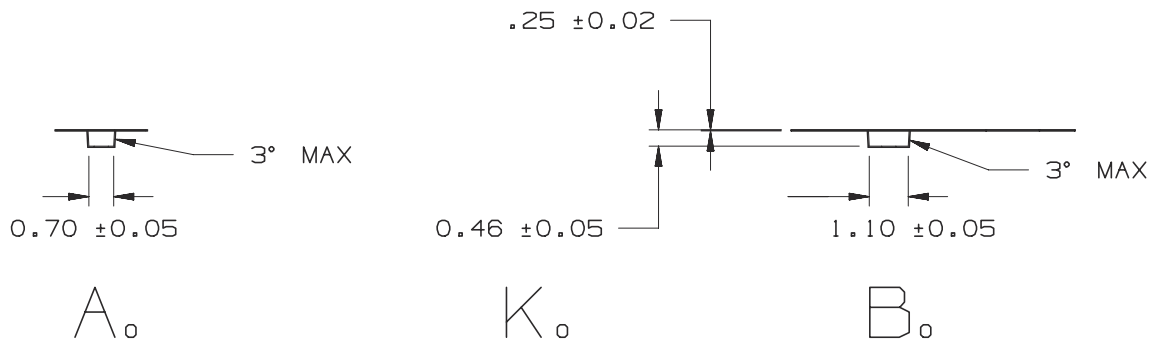
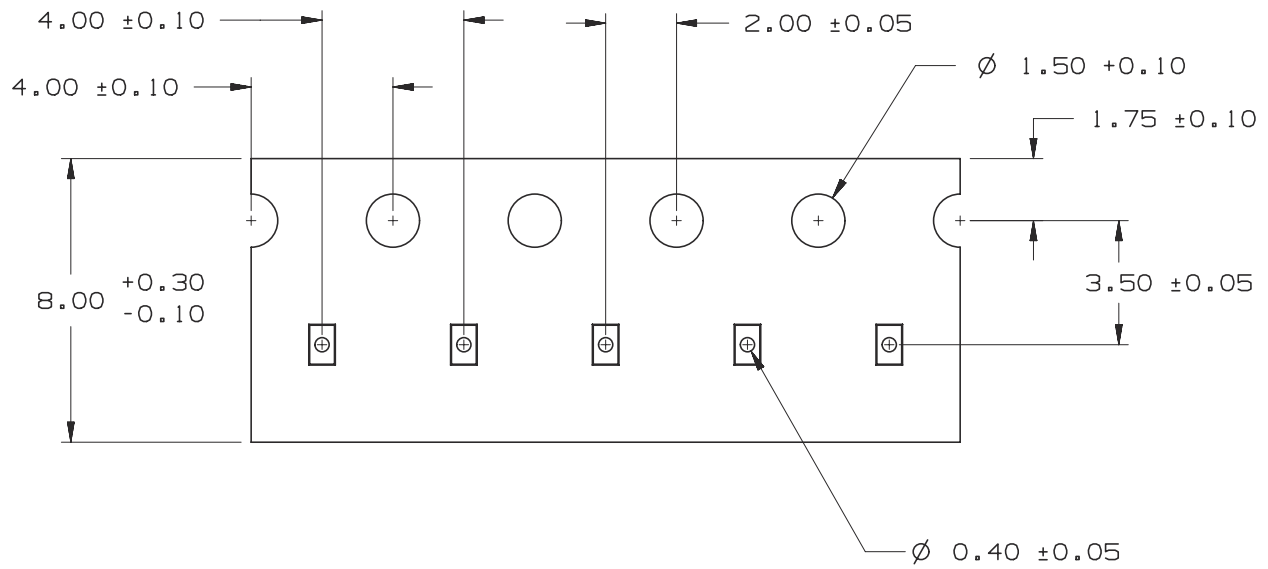
## 7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.



### 7.4 CSD25483F4 Embossed Carrier Tape Dimensions



A. Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25483F4	ACTIVE	PICOSTAR	YJC	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	DR	<a href="#">Samples</a>
CSD25483F4T	ACTIVE	PICOSTAR	YJC	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	DR	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

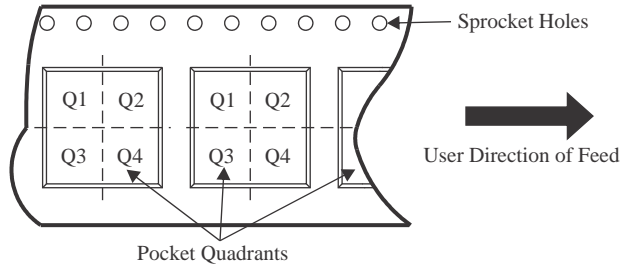
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25483F4	PICOSTAR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2
CSD25483F4T	PICOSTAR	YJC	3	250	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25483F4	PICOSTAR	YJC	3	3000	182.0	182.0	20.0
CSD25483F4T	PICOSTAR	YJC	3	250	182.0	182.0	20.0

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated