DAC5681Z 16-Bit, 1.0 GSPS 2x to 4x Interpolating Digital-To-Analog Converter (DAC)

1 Features

- 16-Bit Digital-to-Analog Converter (DAC)
- 1.0 GSPS Update Rate
- 16-Bit Wideband Input LVDS Data Bus
  - 8 Sample Input FIFO
- High Performance
  - 73-dBc ACLR WCDMA TM1 at 180 MHz
- 2x to 32x Clock Multiplying PLL/VCO
- 2x or 4x Interpolation Filters
  - Stopband Transition 0.4–0.6 Fdata
  - Filters Configurable in Either Low-Pass or High-Pass Mode
    - Allows Selection of Higher Order Image
- On-Chip 1.2-V Reference
- 2 to 20-mA Differential Scalable Output
- 64-Pin 9-mm × 9-mm VQFN Package

2 Applications

- Cellular Base Stations
- Broadband Wireless Access (BWA)
- WiMAX 802.16
- Fixed Wireless Backhaul
- Cable Modem Termination System (CMTS)

3 Description

The DAC5681Z is a 16-bit 1.0 GSPS digital-to-analog converter (DAC) with wideband LVDS data input, integrated 2x to 4x interpolation filters, on-board clock multiplier, and internal voltage reference. The DAC5681Z offers superior linearity, noise, crosstalk, and PLL phase noise performance.

The DAC5681Z integrates a wideband LVDS port with on-chip termination. Full-rate input data can be transferred to a single DAC channel, or half-rate and 1/4-rate input data can be interpolated by on-board 2x or 4x FIR filters. Each interpolation FIR is configurable in either low-pass or high-pass mode, allowing selection of a higher order output spectral image. An on-chip delay lock loop (DLL) simplifies LVDS interfacing by providing skew control for the LVDS input data clock.

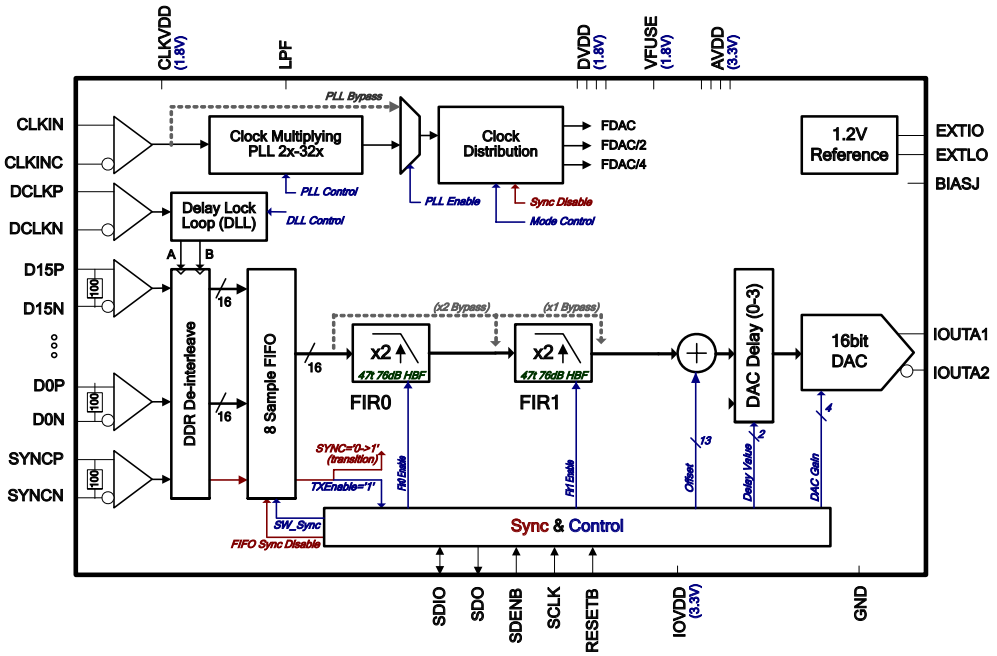
The DAC5681Z is characterized for operation over the industrial temperature range of –40°C to 85°C and is available in a 64-pin VQFN package. Other members of the family include the dual-channel, interpolating DAC5682Z and the single-channel, non-interpolating DAC5681.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC5681z	VQFN (64)	9.00 mm × 9.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2012) to Revision G — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1

Changes from Revision E (March 2011) to Revision F — **Page**

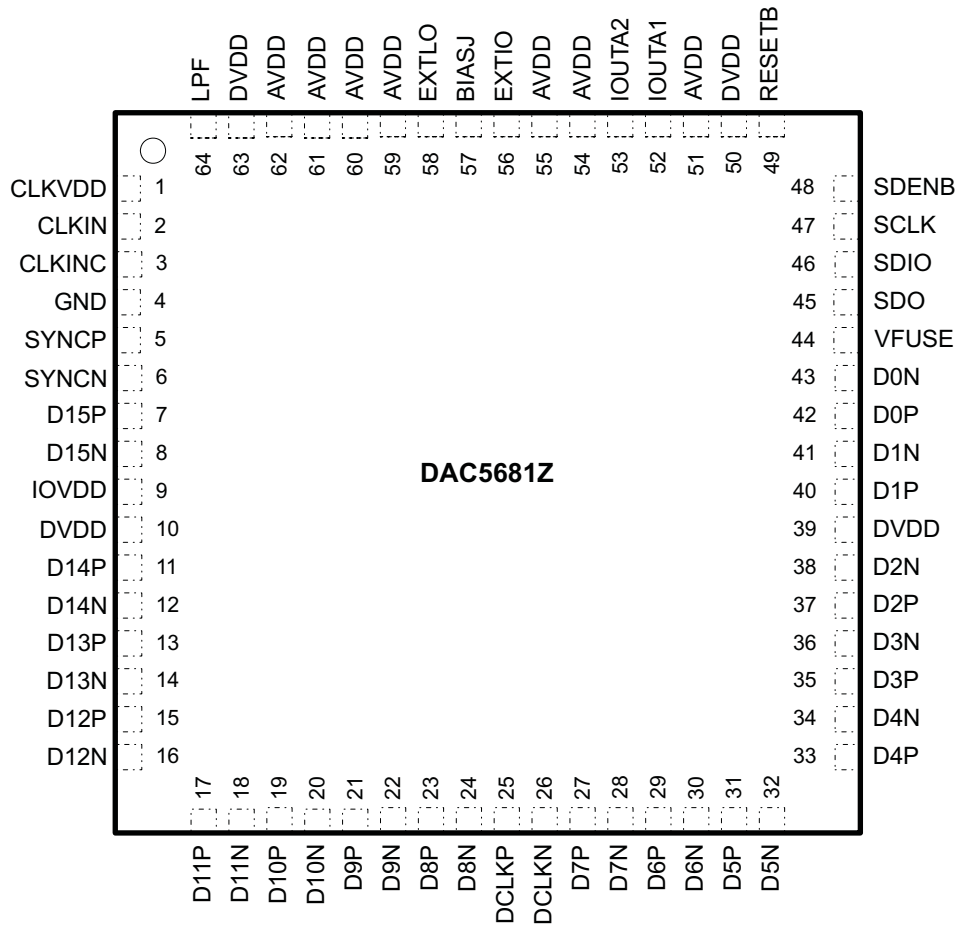
- Changed the Revision to F, August 2012 ... 1
- Changed the first paragraph of ANALOG CURRENT OUTPUTS section for clarification. ... 27
- Changed graphic entity of Figure 46 for clarification. ... 36

Changes from Revision D (September 2009) to Revision E — **Page**

- Changed defined by ..... registers CONFIG1, CONFIG5 and CONFIG6 to defined by .....registers CONFIG1 and CONFIG5. ... 22
- Changed in RECOMMENDED...PROCEDURE section, second sentence from "clkdiv_sync_dis and FIFO_sync_dis bits as well .....input." to "clkdiv_sync_dis as well....input." ... 33
- Deleted "CONFIG5 FIFO_sync_dis = 0" from first and second ordered lists under RECMMENDED.....PROCEDURE section. ... 33

5 Pin Configuration and Functions

RGC Package
64-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	51, 54, 55, 59–62	I	Analog supply voltage. (3.3 V)
BIASJ	57	O	Full-scale output current bias. For 20-mA full-scale output current, connect a 960-Ω resistor to GND.
CLKIN	2	I	Positive external clock input with a self-bias of approximately CLKVDD/2. With the clock multiplier PLL enabled, CLKIN provides lower frequency reference clock. If the PLL is disabled, CLKIN directly provides clock for DAC up to 1 GHz.
CLKINC	3	I	Complementary external clock input. (See the CLKIN description)
CLKVDD	1	I	Internal clock buffer supply voltage. (1.8 V)
D[15..0]P	7, 11, 13, 15, 17, 19, 21, 23, 27, 29, 31, 33, 35, 37, 40, 42	I	LVDS positive input data bits 0 through 15. Each positive/negative LVDS pair has an internal 100-Ω termination resistor. Order of bus can be reversed via **rev_bus** bit in CONFIG5 register. Data format relative to DCLKP/N clock is double data rate (DDR) with two data samples input per DCLKP/N clock. In dual-channel mode, data for the A-channel is input while DCLKP is high. D15P is most significant data bit (MSB) – pin 7 D0P is least significant data bit (LSB) – pin 42

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
D[15..0]N	8, 12, 14, 16, 18, 20, 22, 24, 28, 30, 32, 34, 36, 38, 41, 43	I	LVDS negative input data bits 0 through 15. (See D[15:0]P description) D15N is most significant data bit (MSB) – pin 8 D0N is least significant data bit (LSB) – pin 43
DCLKP	25	I	LVDS positive input clock. Unlike the other LVDS inputs, the DCLKP/N pair is self-biased to approximately DVDD/2 and does not have an internal termination resistor in order to optimize operation of the DLL circuit. See *DLL Operation*. For proper external termination, connect a 100-Ω resistor across LVDS clock source lines followed by series 0.01-µF capacitors connected to each of DCLKP and DCLKN pins (see Figure 65). For best performance, the resistor and capacitors should be placed as close as possible to these pins.
DCLKN	26	I	LVDS negative input clock. (See the DCLKP description)
DVDD	10, 39, 50, 63	I	Digital supply voltage. (1.8 V)
EXTIO	56	I/O	Used as external reference input when internal reference is disabled (that is, EXTLO connected to AVDD). Used as 1.2-V internal reference output when EXTLO = GND, requires a 0.1-µF decoupling capacitor to AGND when used as reference output.
EXTLO	58	O	Connect to GND for internal reference, or AVDD for external reference.
GND	4, Thermal Pad	I	Pin 4 and the Thermal Pad located on the bottom of the VQFN package is ground for AVDD, DVDD and IOVDD supplies.
IOUTA1	52	O	DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current sink and the least positive voltage on the IOUTA1 pin. Similarly, a 0xFFFF data input results in a 0-mA current sink and the most positive voltage on the IOUTA1 pin.
IOUTA2	53	O	DAC complementary current output. The IOUTA2 has the opposite behavior of the IOUTA1 described above. An input data value of 0x0000 results in a 0-mA sink and the most positive voltage on the IOUTA2 pin.
IOVDD	9	I	Digital I/O supply voltage (3.3 V) for pins RESETB, SCLK, SDENB, SDIO, SDO.
LPF	64	I	PLL loop filter connection. If not using the clock multiplying PLL, the LPF pin may be left open. Set both **PLL_bypass** and **PLL_sleep** control bits for reduced power dissipation.
RESETB	49	I	Resets the chip when low. Internal pullup.
SCLK	47	I	Serial interface clock. Internal pulldown.
SDENB	48	I	Active low serial data enable, always an input to the DAC5681Z. Internal pullup.
SDIO	46	I/O	Bi-directional serial interface data in 3-pin mode (default). In 4-pin interface mode (CONFIG5 **sif4**), the SDIO pin is an input only. Internal pulldown.
SDO	45	O	Uni-directional serial interface data in 4-pin mode (CONFIG5 **sif4**). The SDO pin is in high-impedance state in 3-pin interface mode (default), but can optionally be used as a status output pin via CONFIG14 **SDO_func_sel(2:0)**. Internal pulldown.
SYNCP	5	I	LVDS SYNC positive input data. The SYNCP/N LVDS pair has an internal 100-Ω termination resistor. By default, the **SYNCP/N input must be logic 1 to enable a DAC analog output**. See *LVDS SYNCP/N Operation*.
SYNCN	6	I	LVDS SYNC negative input data.
VFUSE	44	I	Digital supply voltage. (1.8 V) **Connect to DVDD pins for normal operation**. This supply pin is also used for factory fuse programming.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	DVDD(2)	–0.5	2.3	V
	VFUSE(2)	–0.5	2.3	V
	CLKVDD(2)	–0.5	2.3	V
	AVDD(2)	–0.5	4	V
	IOVDD(2)	–0.5	4	V
Terminal voltage	AVDD to DVDD	–2	2.6	V
	CLKVDD to DVDD	–0.5	0.5	V
	IOVDD to AVDD	–0.5	0.5	V
	D[15..0]P ,D[15..0]N, SYNCP, SYNCN (2)	–0.5	DVDD + 0.5	V
	DCLKP, DCLKN(2)	–0.3	2.1	V
	CLKIN, CLKINC(2)	–0.5	CLKVDD + 0.5	V
	SDO, SDIO, SCLK, SDENB, RESETB (2)	–0.5	IOVDD + 0.5	V
	IOUTA1, IOUTA2 (2)	–0.5	AVDD + 0.5	V
	LPF, EXTIO, EXTLO, BIASJ(2)	–0.5	AVDD + 0.5	V
Peak input current (any input)			20	mA
Peak total input current (all inputs)			–30	mA
Operating free-air temperature, T_A: DAC5681Z		–40	85	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to GND.

6.2 Esd Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
SUPPLIES				
AVDD	3	3.3	3.6	V
DVDD	1.7	1.8	1.9	V
CLKVDD	1.7	1.8	1.9	V
IOVDD	3	3.3	3.6	V
ANALOG OUTPUT				
IOUTA1, IOUTA2, IOUTB1, IOUTB2	0	20	20	mA
V IOUTA1, IOUTA2, IOUTB1, IOUTB2 Compliance voltage	AVDD – 0.5		AVDD + 0.5	V

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
CLOCK INPUT				
CLKIN ECL/PECL Frequency			1000	MHz
CLKIN Amplitude Differential	0.4	1	CLKVDD	V
CLKIN Duty Cycle		50%		
CLKIN common mode voltage		CLKDVDD / 2		V
DCLK LVDS Frequency			500	MHz
DIGITAL INPUTS				
SYNC LVDS	1	1.2	1.4	V
D15..D0 LVDS	1	1.2	1.4	V
LVDS Common mode		1.2		V
LVDS Differential Swing		0.4		V
SCLK, SDIO, SDENB, SDO CMOS SPI	GND		IOVDD	V

6.4 Thermal Information

THERMAL METRIC[1]		DAC5681Z RGC (VQFN) 64 PINS	UNIT
T_J	Maximum junction temperature [2][3]	125	°C
θ_{JA}	Theta junction-to-ambient (still air)	22	°C/W
	Theta junction-to-ambient (200 lfm)	15	
Ψ_{JT}	Psi junction-to-top of package	0.2	°C/W
θ_{JB}	Theta junction-to-board	3.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Air flow or heat sinking reduces θ_{JA} and may be required for sustained operation at 85°C under maximum operating conditions.
(3) It is strongly recommended to solder the device thermal pad to the board ground plane.

6.5 Electrical Characteristics — DC Specification

over operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 1.8 V, IOVDD = 3.3 V, DVDD = 1.8 V, $Iout_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION			16			Bits
DC ACCURACY(1)						
INL	Integral nonlinearity	1 LSB = IOUTFS / 2^{16}		±4		LSB
DNL	Differential nonlinearity			±2		
ANALOG OUTPUT						
	Coarse gain linearity			±0.04		LSB
	Offset error	Mid code offset		0.01%		FSR
	Gain error	With external reference		1%		FSR
	Gain error	With internal reference		0.7%		FSR
	Minimum full scale output current(2)			2		mA
	Maximum full scale output current(2)			20		
	Output Compliance range(3)	IOUTFS = 20 mA	AVDD –0.5		AVDD + 0.5	V
	Output resistance			300		kΩ
	Output capacitance			5		pF
REFERENCE OUTPUT						
V_{ref}	Reference voltage		1.14	1.2	1.26	V
	Reference output current(4)			100		nA
REFERENCE INPUT						
V_{EXTIO}	Input voltage range		0.1		1.25	V
	Input resistance			1		MΩ
	Small signal bandwidth	CONFIG6: BiasLPF_A = 0		95		kHz
		CONFIG6: BiasLPF_A = 1		472		
	Input capacitance			100		pF
TEMPERATURE COEFFICIENTS						
	Offset drift			±1		ppm of FSR/°C
	Gain drift	With external reference		±15		ppm of FSR/°C
		With internal reference		±30		
	Reference voltage drift			±8		ppm/°C
POWER SUPPLY						
	Analog supply voltage, AVDD		3	3.3	3.6	V
	Digital supply voltage, DVDD		1.7	1.8	1.9	V
	Clock supply voltage, CLKVDD		1.7	1.8	1.9	V
	I/O supply voltage, IOVDD		3	3.3	3.6	V
$I_{(AVDD)}$	Analog supply current	Mode 4 (below)		68		mA
$I_{(DVDD)}$	Digital supply current			271		mA
$I_{(CLKVDD)}$	Clock supply current			41		mA
$I_{(IOVDD)}$	IO supply current			13		mA

(1) Measured differential across IOUTA1 and IOUTA2 with 25 Ω each to AVDD.
(2) Nominal full-scale current, IoutFS, equals 16 × IBIAS current.
(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5681Z device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.
(4) Use an external buffer amplifier with high impedance input to drive any external load.

Electrical Characteristics — DC Specification (continued)

over operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 1.8 V, IOVDD = 3.3 V, DVDD = 1.8 V, $Iout_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (continued)						
$I_{(AVDD)}$	Sleep mode, AVDD supply current	Mode 6 (below)		1		mA
$I_{(DVDD)}$	Sleep mode, DVDD supply current			4		mA
$I_{(CLKVDD)}$	Sleep mode, CLKVDD supply current			2		mA
$I_{(IOVDD)}$	Sleep mode, IOVDD supply current			2		mA
P	AVDD + IOVDD current, 3.3 V	Mode 1: 1X2, PLL = OFF, CLKIN = 983.04 MHz FDAC = 983.04 MHz, IF = 184.32 MHz 4 carrier WCDMA		71		mA
	DVDD + CLKVDD current, 1.8 V			267		mA
	Power Dissipation			715		mW
	AVDD + IOVDD current, 3.3 V	Mode 2: 1X2, PLL = ON (8X), CLKIN = 122.88 MHz FDAC = 983.04 MHz, IF = 184.32 MHz 4 carrier WCDMA		81		mA
	DVDD + CLKVDD current, 1.8 V			292		mA
	Power Dissipation			790		mW
	AVDD + IOVDD current, 3.3 V	Mode 3: 1X4, HP/HP, PLL = OFF, CLKIN = 983.04 MHz, FDAC = 983.04MHz, IF = 215.04 MHz 4 carrier WCDMA		71		mA
	DVDD + CLKVDD current, 1.8 V			278		mA
	Power Dissipation			735		mW
	AVDD + IOVDD current, 3.3 V	Mode 4: 1X4, HP/HP, PLL = ON (8X), CLKIN = 122.88 MHz FDAC = 983.04 MHz, IF = 215.04 MHz DACA on, 4 carrier WCDMA		81		mA
	DVDD + CLKVDD current, 1.8 V			312		mA
	Power Dissipation			830	910	mW
	AVDD + IOVDD current, 3.3 V	Mode 5: PLL = OFF, CLKIN = 983.04 MHz, FDAC = 983.04MHz, Digital Logic Disabled, DAC on SLEEP, Static Data Pattern		3		mA
	DVDD + CLKVDD current, 1.8 V			117		mA
	Power Dissipation			220		mW
	AVDD + IOVDD current, 3.3 V	Mode 6: PLL = OFF, CLKIN = OFF FDAC = OFF, Digital Logic Disabled DAC on SLEEP, Static Data Pattern		3		mA
	DVDD + CLKVDD current, 1.8 V			6		mA
	Power Dissipation			20	30	mW
PSRR	Power supply rejection ratio	DC tested	–0.2%		0.2	FSR/V
T	Operating range		–40		85	°C

6.6 Electrical Characteristics — AC Specification(1)

Over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA, 4:1 transformer output termination, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SFDR	Spurious free dynamic	1X1, PLL off, CLKIN = 500 MHz, IF = 5.1 MHz, First Nyquist Zone < f_{DATA} / 2		81		dBc
		1X2, PLL off, CLKIN = 1000 MHz, IF = 5.1 MHz, First Nyquist Zone < f_{DATA} / 2		80		
		1X2, PLL off, CLKIN = 1000 MHz, IF = 20.1 MHz, First Nyquist Zone < f_{DATA} / 2		77		

(1) Measured single-ended into 50-Ω load.

Electrical Characteristics — AC Specification(1) (continued)

Over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA, 4:1 transformer output termination, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE (continued)						
SNR	Signal-to-noise ratio	1X2, PLL off, CLKIN = 500 MHZ, Single tone, 0 dBFS, IF = 20.1 MHz		75		dBc
		1X2, PLL off, CLKIN = 1000 MHZ, Single tone, 0 dBFS, IF = 20.1 MHz		70		
		1X2, PLL off, CLKIN = 1000 MHZ, Single tone, 0 dBFS, IF = 70.1 MHz		66		
		1X4, PLL off, CLKIN = 1000 MHZ, Single tone, 0 dBFS, IF = 180 MHz		60		
		1X2 , PLL off, CLKIN = 1000 MHZ, Single tone, 0 dBFS, IF = 300.2 MHz		60		
		1X2, PLL off, CLKIN = 1000 MHZ, Four tone, each – 12 dBFS, IF = 24.7, 24.9, 25.1 and 25.3 MHz		73		
IMD3	Third-order two-tone intermodulation (each tone at –6 dBFS)	1X2, PLL off, CLKIN = 1000 MHZ, IF = 20.1 and 21.1 MHz		88		dBc
		1X2, PLL off, CLKIN = 1000 MHZ, IF = 70.1 and 71.1 MHz		75		
		1X2, PLL off, CLKIN = 1000 MHZ, IF = 150.1 and 151.1 MHz		67		
IMD	Four-tone intermodulation (each tone at –12 dBFS)	1X2, PLL off, CLKIN = 1000 MHz, IF = 298.4, 299.2, 300.8 and 301.6 MHz		64		dBc
ACLR(2)	Adjacent channel leakage ratio	Single carrier, baseband, 1X2, PLL off, CLKIN = 983.04 MHz	80	83		dBc
		Single carrier, IF = 180 MHz, 1X2, PLL off, CLKIN = 983.04 MHz		73		
		Four carrier, IF = 180 MHz, 1X2, PLL off, CLKIN = 983.04 MHz		68		
		Four carrier, IF = 275 MHz, 1X2, PLL off, CLKIN = 983.04 MHz		66		
	Noise floor(3)	50-MHz offset, 1-MHz BW, Single Carrier, baseband, 1X2, PLL off, CLKIN = 983.04		93		dBc
		50-MHz offset, 1-MHz BW, Four Carrier, baseband, 1X2, PLL off, CLKIN = 983.04		85		
ANALOG OUTPUT						
f_{CLK}	Maximum output update rate		1000			MSPS
$t_{s(DAC)}$	Output settling time to 0.1%	Transition: Code 0x0000 to 0xFFFF		10.4		ns
t_{pd}	Output propagation delay	DAC output is updated on falling edge of DAC clock. Does not include Digital Latency		2.5		ns
$t_{r(IOUT)}$	Output rise time 10% to 90%			220		ps
$t_{f(IOUT)}$	Output fall time 90% to 10%			220		ps
	Digital Latency	No interpolation, PLL Off		76		DAC clock cycles
		x2 interpolation, PLL Off		158		
		x4 interpolation, PLL Off		289		
Power-up Time	DAC Wake-up Time	IOUT current settling to 1% of $IOUT_{FS}$. Measured from SDENB; Register 0x06, toggle Bit 4 from 1 to 0.		80		µs
	DAC Sleep Time	IOUT current settling to less than 1% of $IOUT_{FS}$. Measured from SDENB; Register 0x06, toggle Bit 4 from 0 to 1.		80		µs

(2) W-CDMA with 3.84-MHz BW, 5-MHz spacing, centered at IF. TESTMODEL 1, 10 ms
(3) Carrier power measured in 3.84-MHz BW.

6.7 Electrical Characteristics – Digital Specifications

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8-V.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
LVDS INTERFACE: D[15:0]P/N, SYNCP/N, DCLKP/N (1)								
$V_{A,B+}$	Logic high differential input voltage threshold				175			mV
$V_{A,B-}$	Logic low differential input voltage threshold				–175			mV
V_{COM1}	Input Common Mode	SYNCP/N, D[15:0]P/N only			1.0			V
V_{COM2}	Input Common Mode	DCLKP/N only				DVDD ÷2		V
Z_T	Internal termination	SYNCP/N, D[15:0]P/N only			85	110	135	Ω
C_L	LVDS Input capacitance					2		pF
t_S, t_H	DCLK to Data	DCLKP/N: 0 to 125MHz (see Figure 42) DLL Disabled, CONFIG5 **DLL_bypass** = 1, CONFIG10 = 00000000		Setup_min		1100		ps
				Hold_min		–600		
$t_{SKEW(A)}$, $t_{SKEW(B)}$	DCLK to Data Skew(2)	DLL Enabled, CONFIG5 **DLL_bypass** = 0, DDR format	DCLKP/N = 150 MHz	Positive		1000		ps
				Negative		–1800		
			DCLKP/N = 200 MHz	Positive		800		
				Negative		–1300		
			DCLKP/N = 250 MHz	Positive		600		
				Negative		–1000		
			DCLKP/N = 300 MHz	Positive		450		
				Negative		–800		
			DCLKP/N = 350 MHz	Positive		400		
				Negative		–700		
			DCLKP/N = 400 MHz	Positive		300		
				Negative		–600		
			DCLKP/N = 450 MHz	Positive		300		
				Negative		–500		
			DCLKP/N = 500 MHz	Positive		350		
				Negative		–300		
f_{DATA}	Input data rate supported	DLL Disabled, CONFIG5 **DLL_bypass** = 1, DDR format, DCLKP frequency: <125 MHz					250	MSPS
		DLL Enabled, CONFIG5 **DLL_bypass** = 0, DDR format, DCLKP frequency: 125 to 500 MHz			250		1000	
	DLL Operating Frequency (DCLKP/N Frequency)	DLL Enabled, CONFIG5 **DLL_bypass** = 0, DDR format	CONFIG10 = 11001101 = 0xCD			125–150		MHz
			CONFIG10 = 11001110 = 0xCE			150–175		
			CONFIG10 = 11001111 = 0xCF			175–200		
			CONFIG10 = 11001000 = 0xC8			200–325		
			CONFIG10 = 11000000 = 0xC0			325–500		

(1) See *LVDS INPUTS* for terminology.
(2) Positive skew: Clock ahead of data.
Negative skew: Data ahead of clock.

Electrical Characteristics – Digital Specifications (continued)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8-V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS INTERFACE: SDO, SDIO, SCLK, SDENB, RESETB						
V_{IH}	High-level input voltage		2	3		V
V_{IL}	Low-level input voltage		0	0	0.8	V
I_{IH}	High-level input current			±20		µA
I_{IL}	Low-level input current			±20		µA
CI	CMOS Input capacitance			5		pF
V_{OH}	SDO, SDIO	I_{load} = –100 µA	IOVDD –0.2			V
		I_{load} = –2mA	0.8 x IOVDD			V
V_{OL}	SDO, SDIO	I_{load} = 100 µA			0.2	V
		I_{load} = 2 mA			0.5	V
$t_{s(SDENB)}$	Set-up time, SDENB to rising edge of SCLK		20			ns
$t_{s(SDIO)}$	Set-up time, SDIO valid to rising edge of SCLK		10			ns
$t_{h(SDIO)}$	Hold time, SDIO valid to rising edge of SCLK		5			ns
$t_{(SCLK)}$	Period of SCLK		100			ns
$t_{(SCLKH)}$	High time of SCLK		40			ns
$t_{(SCLKL)}$	Low time of SCLK		40			ns
$t_{d(Data)}$	Data output delay after falling edge of SCLK			10		ns
t_{RESET}	Minimum RESETB pulse width			25		ns
CLOCK INPUT (CLKIN/CLKINC)						
	Duty cycle			50%		
	Differential voltage(3)		0.4	1		V
	CLKIN/CLKINC input common mode			CLKVDD ÷2		V

(3) Driving the clock input with a differential voltage lower than 1 V will result in degraded performance.

Electrical Characteristics – Digital Specifications (continued)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, CLKVDD, DVDD = 1.8-V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PHASE LOCKED LOOP					
Phase noise	DAC output at 600 kHz offset, 100 MHz, 0-dBFS tone, 1X4, f_{DATA} = 250 MSPS, CLKIN/C = 250 MHz, PLL_m = 00111, PLL_n = 001, VCO_div2 = 0, PLL_range = 1111, PLL_gain = 00		–125		dBc/ Hz
	DAC output at 6 MHz offset, 100 MHz, 0-dBFS tone, 1X4, f_{DATA} = 250 MSPS, CLKIN/C = 250 MHz, PLL_m = 00111, PLL_n = 001, VCO_div2 = 0, PLL_range = 1111, PLL_gain = 00		–146		
PLL/VCO Operating Frequency, Typical VCO Gain	**PLL_gain** = 00, **PLL_range** = 0000 (0)	160		290	MHz
			220		MHz/V
	PLL_gain = 01, **PLL_range** = 0001 (1)	290		460	MHz
			300		MHz/V
	PLL_gain = 01, **PLL_range** = 0010 (2)	400		520	MHz
			260		MHz/V
	PLL_gain = 01, **PLL_range** = 0011 (3)	480		570	MHz
			240		MHz/V
	PLL_gain = 01, **PLL_range** = 0100 (4)	560		620	MHz
			210		MHz/V
	PLL_gain = 10, **PLL_range** = 0101 (5)	620		740	MHz
			270		MHz/V
	PLL_gain = 10, **PLL_range** = 0110 (6)	690		780	MHz
			250		MHz/V
	PLL_gain = 10, **PLL_range** = 0111 (7)	740		820	MHz
			240		MHz/V
	PLL_gain = 10, **PLL_range** = 1000 (8)	790		850	MHz
			220		MHz/V
	PLL_gain = 10, **PLL_range** = 1001 (9)	840		880	MHz
			210		MHz/V
	PLL_gain = 11, **PLL_range** = 1010 (A)	880		940	MHz
			250		MHz/V
	PLL_gain = 11, **PLL_range** = 1011 (B)	920		990	MHz
			230		MHz/V
	PLL_gain = 11, **PLL_range** = 1100 (C)	960		1000	MHz
			220		MHz/V
PFD Maximum Frequency			160		MHz

6.8 Typical Characteristics

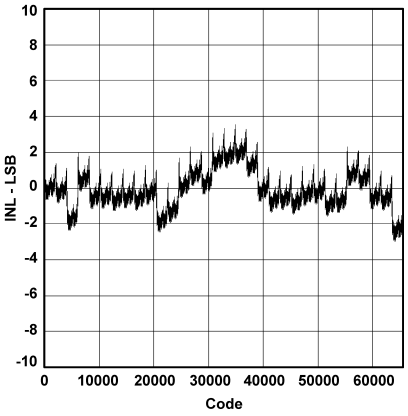


Figure 1. Integral Nonlinearity

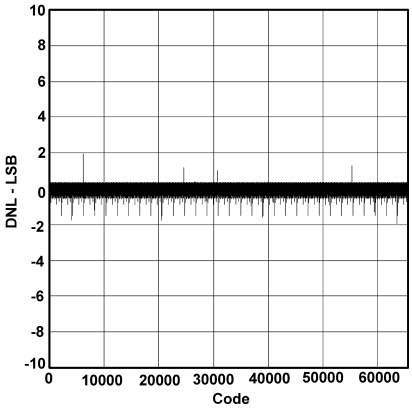


Figure 2. Differential Nonlinearity

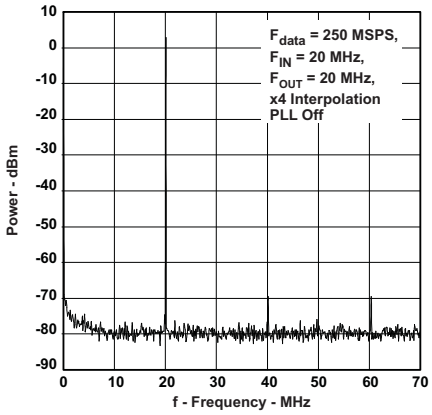


Figure 3. Single-Tone Spectral Plot

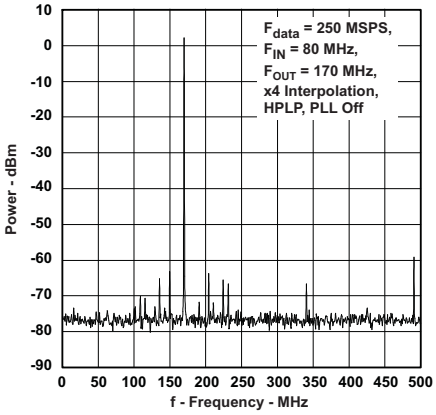


Figure 4. Single-Tone Spectral Plot

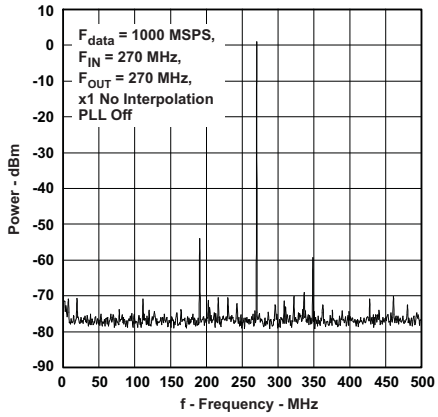


Figure 5. Single-Tone Spectral Plot

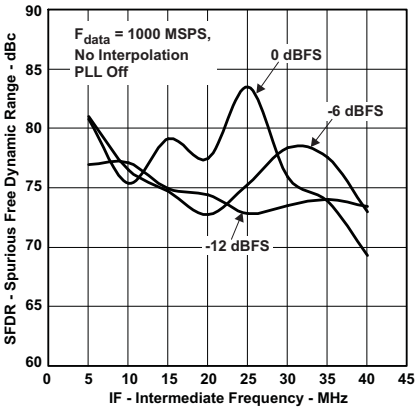


Figure 6. In-Band SFDR vs IF

Typical Characteristics (continued)

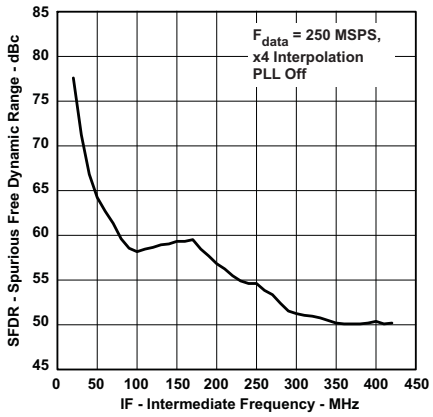


Figure 7. Out-of-Band SFDR vs IF

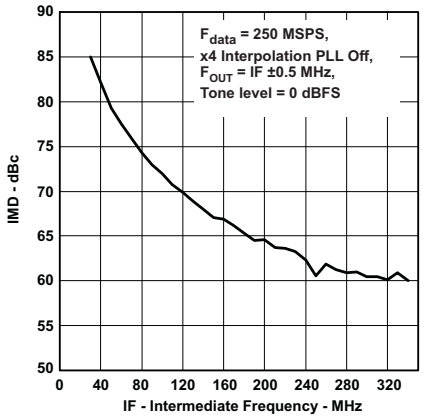


Figure 8. Two-Tone IMD vs Output Frequency

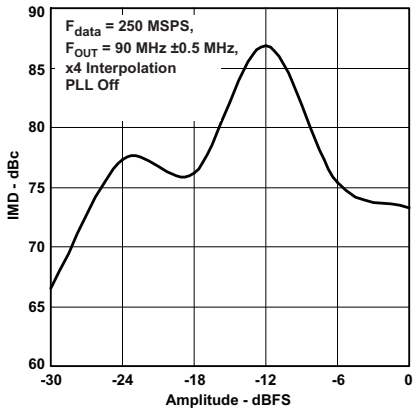


Figure 9. Two-Tone IMD vs Amplitude

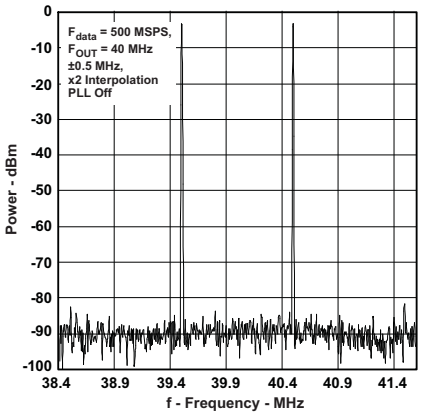


Figure 10. Two-Two-Tone IMD Spectral Plot

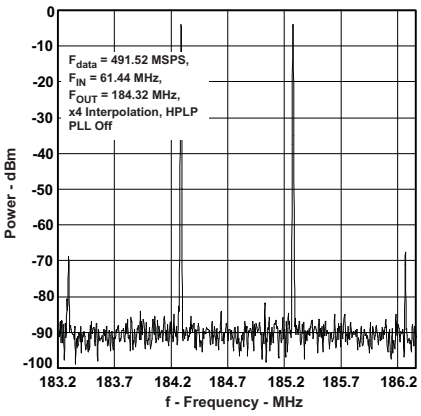


Figure 11. Two-Tone IMD Spectral Plot

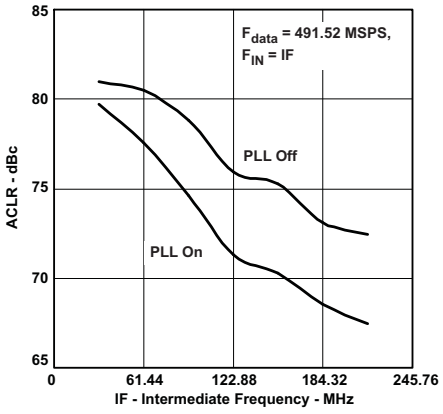


Figure 12. Single Carrier W-CDMA Test Model 1

Typical Characteristics (continued)

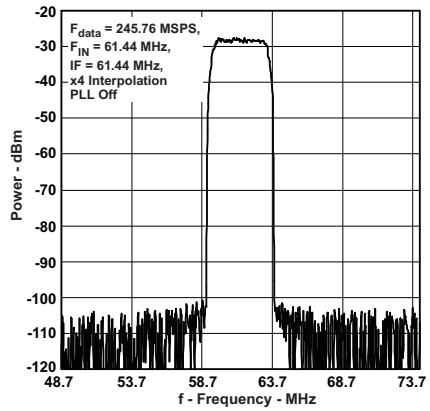


Figure 13. Single Carrier W-CDMA Test Model 1 Carrier Power: –7.8 dBm, ACLR: 79.3 dB

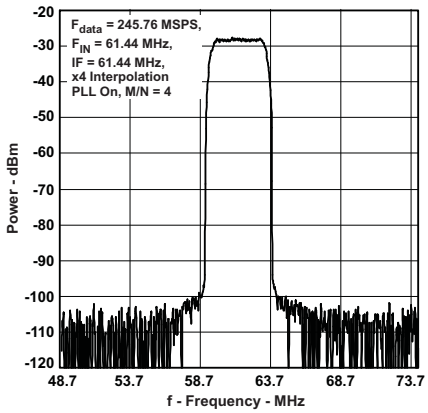


Figure 14. Single Carrier W-CDMA Test Model 1 Carrier Power: –7.8 dBm, ACLR: 76.9 dB

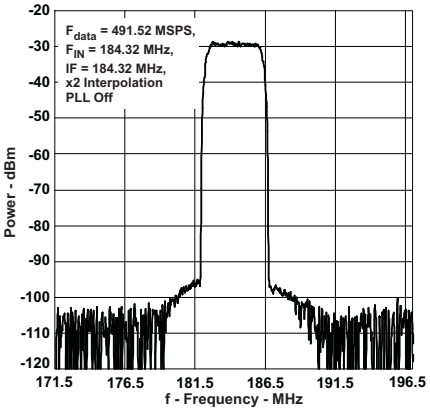


Figure 15. Single Carrier W-CDMA Test Model 1 Carrier Power: –8.9 dBm, ACLR: 72 dB

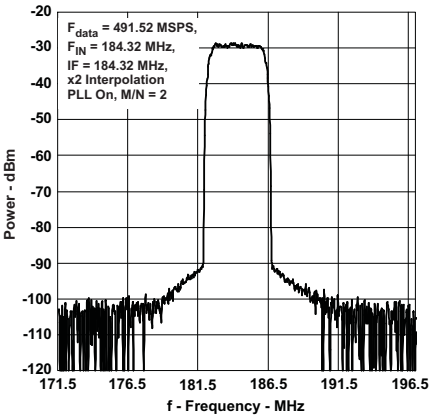


Figure 16. Single Carrier W-CDMA Test Model 1 Carrier Power: –8.9 dBm, ACLR: 68 dB

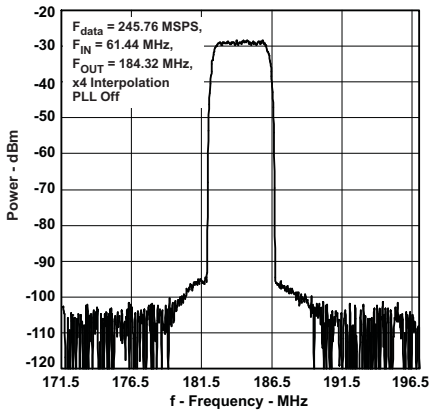


Figure 17. Single Carrier W-CDMA Test Model 1 Carrier Power: –8.5 dBm, ACLR: 71.8 dB

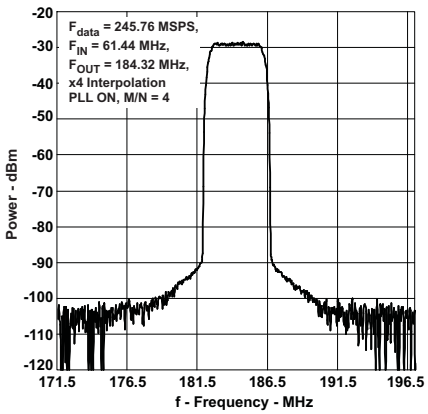


Figure 18. Single Carrier W-CDMA Test Model 1 Carrier Power: –8.5 dBm, ACLR: 68.2 dB

Typical Characteristics (continued)

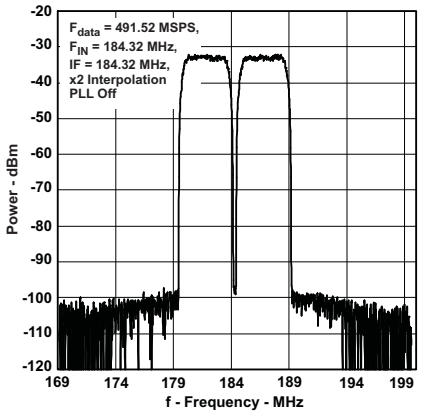


Figure 19. Two Carrier W-CDMA Test Model 1
Carrier Power: –12.5 dBm, ACLR: 68.3 dB

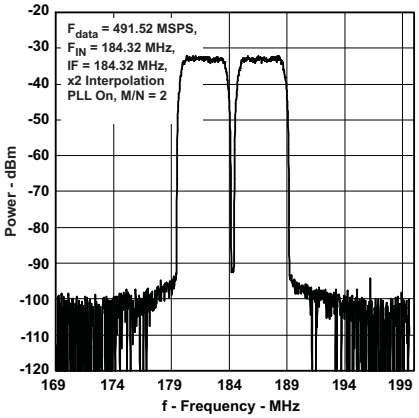


Figure 20. Two Carrier W-CDMA Test Model 1
Carrier Power: –12.5 dBm, ACLR: 65.9 dB

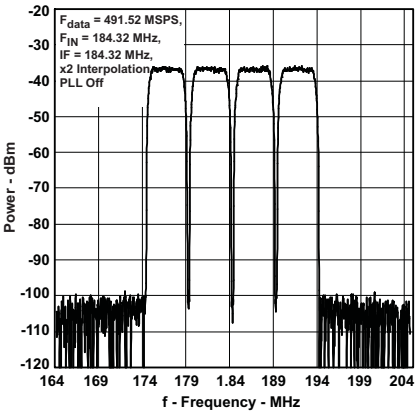


Figure 21. Four Carrier W-CDMA Test Model 1
Carrier Power: –16.3 dBm, ACLR: 66.7 dB

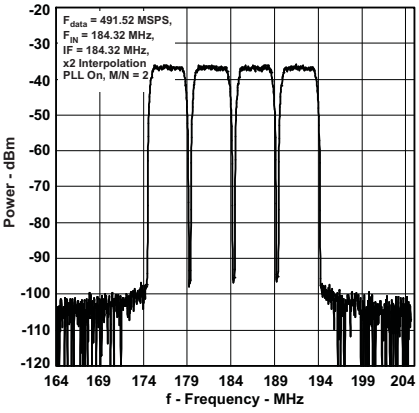


Figure 22. Four Carrier W-CDMA Test Model 1
Carrier Power: –16.3 dBm, ACLR: 64.5 dB

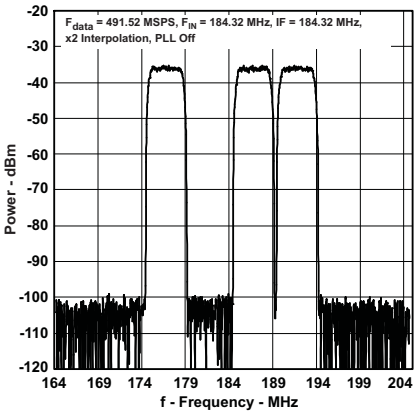


Figure 23. Three Carrier W-CDMA Test Model 1 With Gap
Carrier Power: –15.7 dBm, ACLR: 67.5 dB

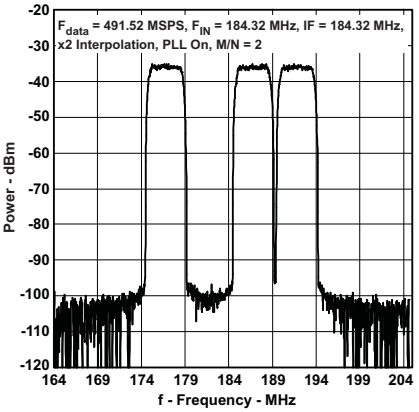


Figure 24. Three Carrier W-CDMA Test Model 1 With Gap
Carrier Power: –15.7 dBm, ACLR: 65.9 dB

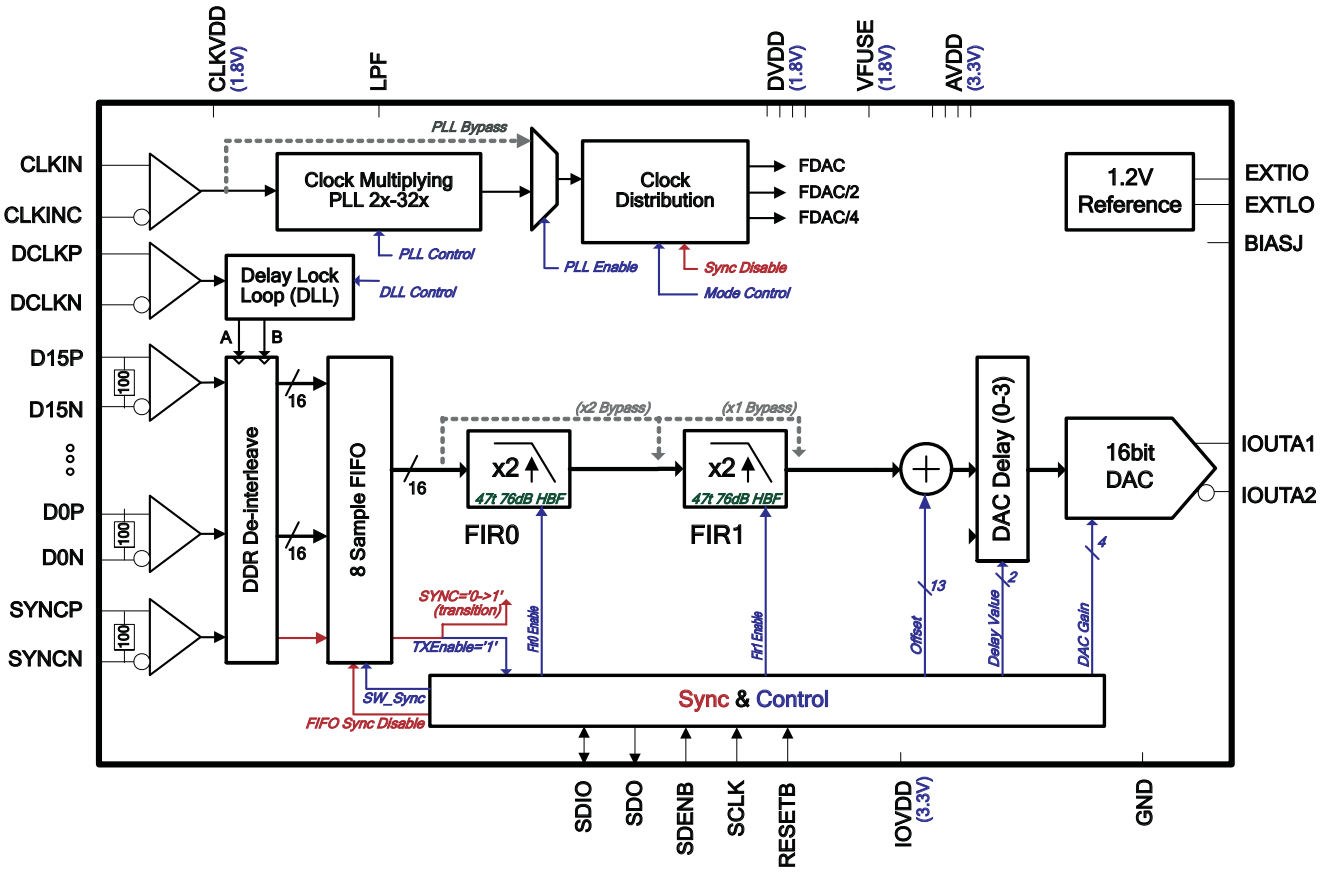
7 Detailed Description

7.1 Overview

The DAC5681Z is a single-channel 16-bit 1.0 GSPS DAC with wideband LVDS data input, integrated 2x to 4x interpolation filters, onboard clock multiplier and internal voltage reference. The DAC5681Z offers superior linearity, noise, crosstalk, and PLL phase noise performance.

The DAC5681Z integrates a wideband LVDS port with on-chip termination. Full-rate input data can be transferred to a single DAC channel, or half-rate and 1/4-rate input data can be interpolated by onboard 2x or 4x FIR filters. Each interpolation FIR is configurable in either lowpass or highpass mode, allowing selection of a higher order output spectral image. An on-chip delay lock loop (DLL) simplifies LVDS interfacing by providing skew control for the LVDS input data clock.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 FIR Filters

Figure 25 shows the magnitude spectrum response for the identical 47-tap FIR0 and FIR1 filters. The transition band is from 0.4 to 0.6 × F_{IN} (the input data rate for the FIR filter) with <0.002 dB of pass-band ripple and approximately 76 dB of stop-band attenuation. Figure 26 shows the region from 0.35 to 0.45 × F_{IN} – up to 0.44x FIN there is less than 0.4 dB attenuation. The composite spectrum for x4 interpolation mode, the cascaded response of FIR0 and FIR1, is shown in Figure 27. The filter taps for both FIR0 and FIR1 are listed in Table 1.

Feature Description (continued)

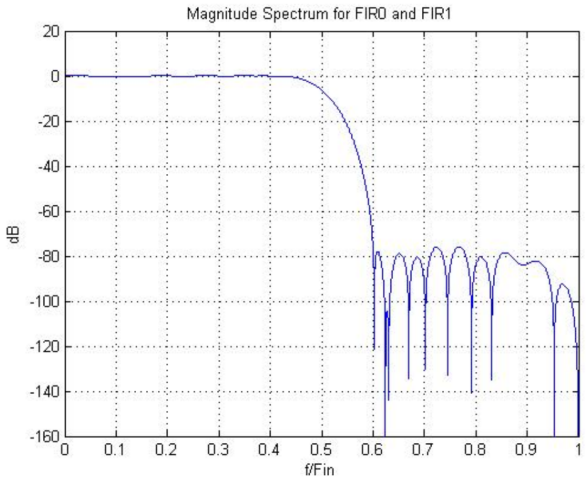


Figure 25. Magnitude Spectrum For FIR0 and FIR1

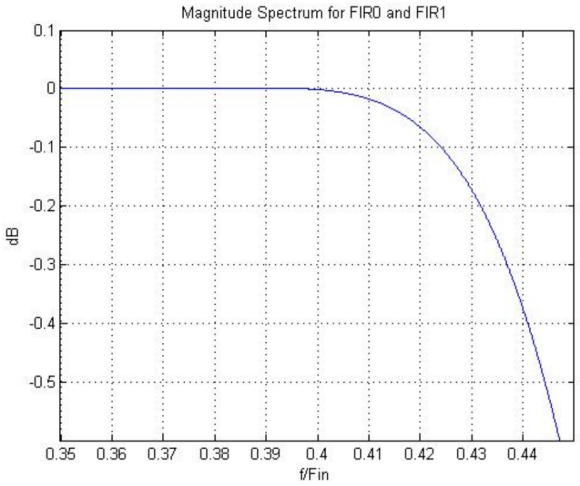


Figure 26. FIR0 and FIR1 Transition Band

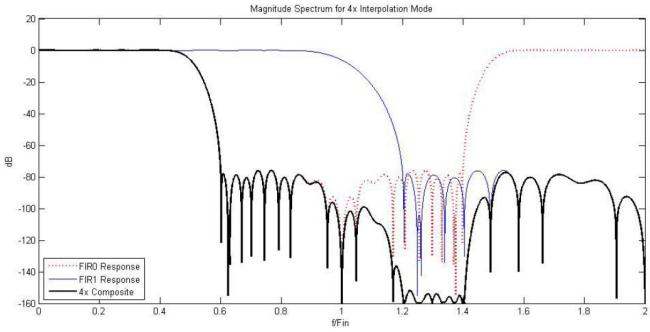


Figure 27. Magnitude Composite Spectrum for 4x Interpolation Mode

Table 1. FIR0 and FIR1 Digital Filter Taps

TAP NO.	COEFF	TAP NO.	COEFF
1, 47	–5	2, 46	0
3, 45	18	4, 44	0
5, 43	–42	6, 42	0
7, 41	85	8, 40	0
9, 39	–158	10, 38	0
11, 37	272	12, 36	0
13, 35	–444	14, 34	0
15, 33	704	16, 32	0
17, 31	–1106	18, 30	0
19, 29	1795	20, 28	0
21, 27	–3295	22, 26	0
23, 25	10368	—	—
24	16384	—	—

7.3.2 Dual-Channel Real Upconversion

Each DAC5681Z digital filter has a normal Low Pass (LP) characteristic, but can be configured to perform a High Pass (HP) function by mixing a 1 –1....sequence at the output of the FIR to invert the spectrum. The mixing mode for each filter is controlled by FIR0_HP and FIR1_HP bits in register CONFIG2. With 1X4 interpolation and cascaded combinations of HP and LP filter modes, the output frequency response will be digitally shifted or upconverted. The wide bandwidths of both FIR0 and FIR1 (40% bandpass) provide options for setting six different frequency ranges, listed in Table 2. With the High Pass (1X2 HP mode), High Pass/Low Pass (1X4 HP/LP mode) and Low Pass/High Pass (1X4 LP/HP mode) settings, the upconverted signal is spectrally inverted.

Table 2. Dual-Channel Real Upconversion Options

MODE NAME	INTERP. FACTOR	FIR0, CMIX0 MODE	FIR1, CMIX1 MODE	INPUT FREQUENCY	OUTPUT FREQUENCY	SIGNAL BANDWIDTH	SPECTRUM INVERTED?
1X2	X2	—	LP	0.0 to 0.4 × f_{DATA}	0.0 to 0.4 × f_{DATA}	0.4 × f_{DATA}	No
1X2 HP	X2	—	HP	0.0 to 0.4 × f_{DATA}	0.6 to 1.0 × f_{DATA}	0.4 × f_{DATA}	Yes
1X4	X4	LP	LP	0.0 to 0.4 × f_{DATA}	0.0 to 0.4 × f_{DATA}	0.4 × f_{DATA}	No
1X4 HP/LP	X4	HP	LP	0.2 to 0.4 × f_{DATA}	0.6 to 0.8 × f_{DATA}	0.2 × f_{DATA}	Yes
1X4 HP/HP	X4	HP	HP	0.2 to 0.4 × f_{DATA}	1.2 to 1.4 × f_{DATA}	0.2 × f_{DATA}	No
1X4 LP/HP	X4	LP	HP	0.0 to 0.4 × f_{DATA}	1.6 to 2.0 × f_{DATA}	0.4 × f_{DATA}	Yes

7.3.3 LVDS Data Interfacing

Interfacing very high-speed LVDS data and clocks presents a big challenge to system designers as they have unique constraints and are often implemented with specialized circuits to increase bandwidth. One such specialized LVDS circuit used in many FPGAs and ASICs is a SERializer-DESerializer (SERDES) block. For interfacing to the DAC5681Z, only the SERializer functionality of the SERDES block is required. SERDES drivers accept lower rate parallel input data and output a serial stream using a shift register at a frequency multiple of the data bit width. For example, a 4-bit SERDES block can accept parallel 4-bit input data at 250 MSPS and output serial data 1000 MSPS.

External clock distribution for FPGA and ASIC SERDES drivers often have a chip-to-chip system constraint of a limited input clock frequency compared to the desired LVDS data rate. In this case, an internal clock multiplying PLL is often used in the FPGA or ASIC to drive the high-rate SERDES outputs. Due to this possible system clocking constraint, the DAC5681Z accommodates a scheme where a toggling LVDS SERDES data bit can provide a “data driven” half-rate clock (DCLK) from the data source. A DLL on-board the DAC is used to shift the DCLK edges relative to LVDS data to maintain internal set-up and hold timing.

To increase bandwidth of a single 16-bit input bus, the DAC5681Z assumes Double Data Rate (DDR) style interfacing of data relative to the half-rate DCLK. Refer to Figure 28 and Figure 29 providing an example implementation using FPGA-based LVDS data and clock interfaces to drive the DAC5681Z. In this example, an assumed system constraint is that the FPGA can only receive a 250 MHz maximum input clock while the desired DAC clock is 1000 MHz. A clock distribution chip such as the CDCM7005 or the CDCE62005 is useful in this case to provide frequency and phase locked clocks at 250 MHz and 1000 MHz.

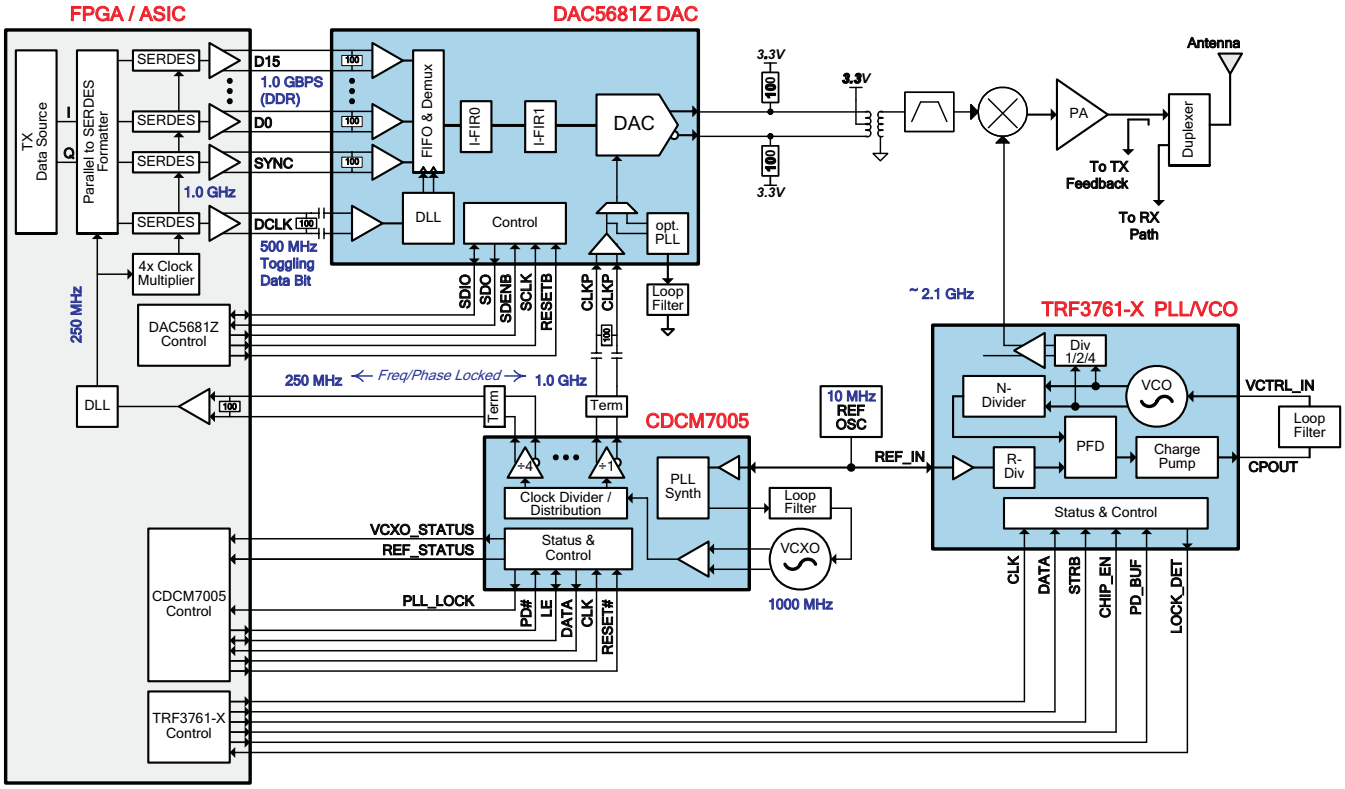


Figure 28. Example Real If System Diagram

From the example provided by Figure 29, driving LVDS data into the DAC using SERDES blocks requires a parallel load of 4 consecutive data samples to shift registers. Color is used in the figure to indicate how data and clocks flow from the FPGA to the DAC5681Z. The figure also shows the use of the SYNCP/N input, which along with DCLK, requires 18 individual SERDES data blocks to drive the DAC's input data FIFO that provides an elastic buffer to the DAC5681Z digital processing chain.

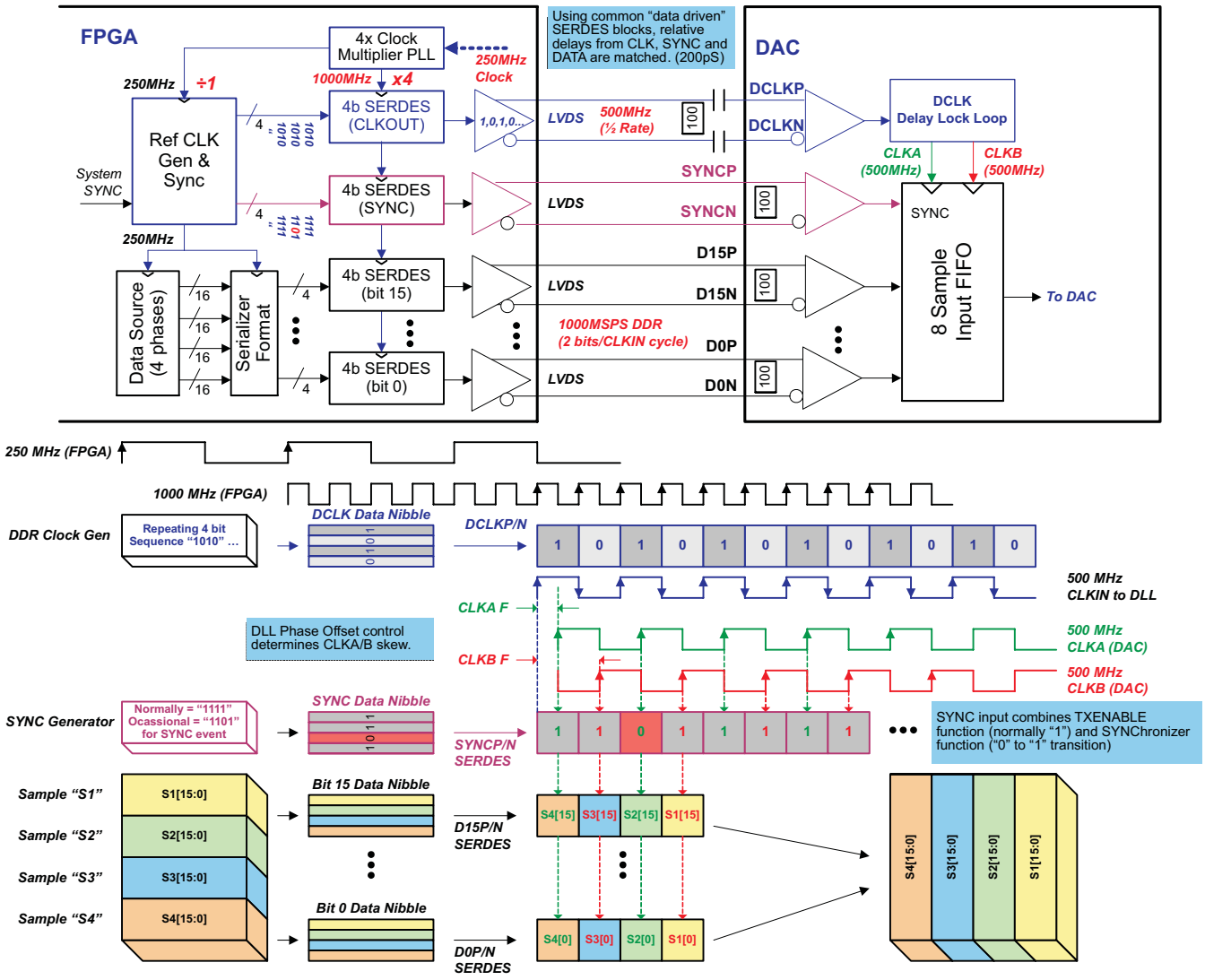


Figure 29. Example FPGA-Based LVDS Data Flow to DAC

7.3.4 LVDS Inputs

The D[15:0]P/N and SYNCP/N LVDS pairs have the input configuration shown in Figure 30. Figure 31 shows the typical input levels and common-mode voltage used to drive these inputs.

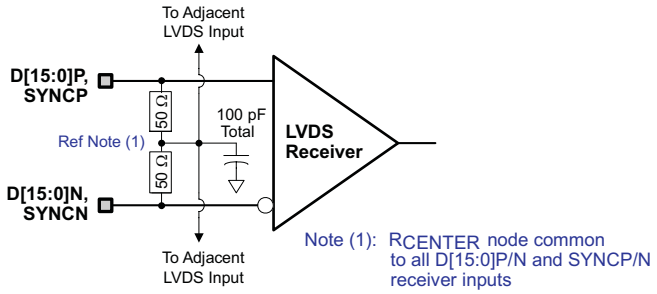


Figure 30. D[15:0]P/N and SYNCP/N LVDS Input Configuration

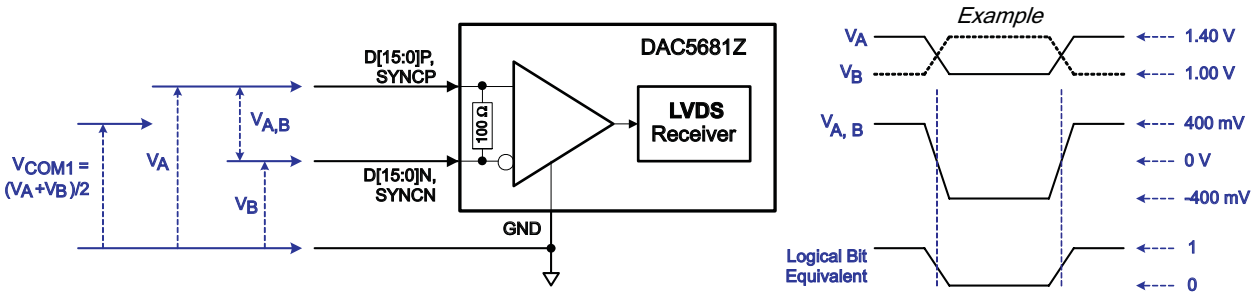


Figure 31. LVDS Data (D[15:0]P/N, SYNCP/N Pairs) Input Levels

Table 3. Example LVDS Data Input Levels

APPLIED VOLTAGES		RESULTING DEFERENTIAL VOLTAGE	RESULTING COMMON-MODE VOLTAGE	LOGICAL BIT BINARY EQUIVALENT
V_A	V_B	$V_{A,B}$	V_{COM1}	
1.4 V	1.0 V	400 mV	1.2 V	1
1.0 V	1.4 V	–400 mV		0
1.2 V	0.8 V	400 mV	1.0 V	1
0.8 V	1.2 V	–400 mV		0

Figure 32 shows the DCLKP/N LVDS clock input levels. Unlike the D[15:0]P/N and SYNCP/N LVDS pairs, the DCLKP/N pair does not have an internal resistor and the common-mode voltage is self-biased to approximately DVDD/2 in order to optimize the operation of the DLL circuit. For proper external termination a 100-Ω resistor needs to be connected across the LVDS clock source lines followed by series 0.01-µF capacitors connected to each of the DCLKP and DCLKN pairs. For best performance, the resistor and capacitors should be placed as close as possible to these pins.

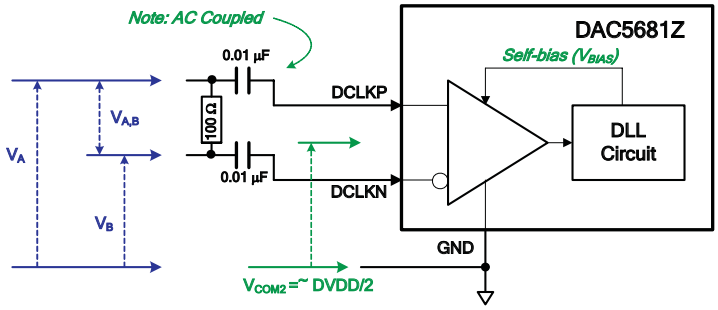


Figure 32. LVDS Clock (DCLKP/N) Input Levels

7.3.5 LVDS SYNCP/N Operation

The SYNCP/N LVDS input control functions as a combination of Transmit Enable (TXENABLE) and Synchronization trigger. If SYNCP is low, the transmit chain is disabled so input data from the FIFO is ignored while zeros are inserted into the data path. If SYNCP is raised from low to high, a synchronization event occurs with behavior defined by individual control bits in registers CONFIG1 and CONFIG5. The SYNCP/N control is sampled and input into the FIFO along with the other LVDS data to maintain timing alignment with the data bus. See Figure 29.

The software_sync_sel and software_sync controls in CONFIG3 provide a substitute for external SYNCP/N control; however, since the serial interface is used no timing control is provided with respect to the DAC clock.

7.3.6 Dll Operation

The DAC5681Z provides a digital Delay Lock Loop (DLL) to skew the LVDS data clock (DCLK) relative to the data bits, D[15:0] and SYNC, in order to maintain proper set-up and hold timing. Since the DLL operates closed-loop, it requires a stable DCLK to maintain delay lock. Refer to the description of DLL_ifixed(2:0) and DLL_delay(3:0) control bits in the *CONFIG10 register*. Prior to initializing the DLL, the DLL_ifixed value should be programmed to match the expected DCLK frequency range. To initialize the DLL, refer to the DLL_Restart programming bit in the*CONFIG8 register*. After initialization, the status of the DLL can be verified by reading the DLL_Lock bit from STATUS0. See *Startup Sequence*.

7.3.7 Reference Operation

The DAC5681Z uses a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS} to pin BIASJ. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The default full-scale output current equals 16 times this bias current and can thus be expressed as Equation 1:

$$IOUT_{FS} = 16 \times I_{BIAS} = 16 \times V_{EXTIO} / R_{BIAS} \quad (1)$$

The DAC has a 4-bit coarse gain control via DACA_gain(3:0) in the CONFIG7 register so the $IOUT_{FS}$ can expressed as Equation 2:

$$IOUTA_{FS} = (DACA\_gain + 1) \times I_{BIAS} = (DACA\_gain + 1) \times V_{EXTIO} / R_{BIAS}$$

where

- V_{EXTIO} is the voltage at terminal EXTIO (2)

The bandgap reference voltage delivers an accurate voltage of 1.2 V. This reference is active when terminal EXTLO is connected to AGND. An external decoupling capacitor C_{EXT} of 0.1 µF should be connected externally to terminal EXTIO for compensation. The bandgap reference can additionally be used for external reference operation. In that case, an external buffer with high impedance input should be applied in order to limit the bandgap load current to a maximum of 100 nA. The internal reference can be disabled and overridden by an external reference by connecting EXTLO to AVDD. Capacitor CEXT may hence be omitted. Terminal EXTIO thus serves as either input or output node.

The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor R_{BIAS} or changing the externally applied reference voltage. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20 dB.

7.3.8 DAC Transfer Function

The CMOS DACs consist of a segmented array of NMOS current sinks, capable of sinking a full-scale output current up to 20 mA. Differential current switches direct the current to either one of the complementary output nodes IOUT1 or IOUT2. Complementary output currents enable differential operation, thus canceling out common-mode noise sources (digital feed-through, on-chip and PCB noise), DC offsets, even order distortion components, and increasing signal output power by a factor of two.

The full-scale output current is set using external resistor R_{BIAS} in combination with an on-chip bandgap voltage reference source (+1.2 V) and control amplifier. Current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a maximum full-scale output current equal to 16 times I_{BIAS}.

The relation between IOUT1 and IOUT2 can be expressed as Equation 3:

$$IOUT1 = – IOUT_{FS} – IOUT2 \quad (3)$$

We will denote current flowing into a node as – current and current flowing out of a node as + current. Since the output stage is a current sink the current can only flow from AVDD into the IOUT1 and IOUT2 pins. The output current flow in each pin driving a resistive load can be expressed as Equation 4 and Equation 5:

$$IOUT1 = IOUT_{FS} \times (65535 – CODE) / 65536 \quad (4)$$

$$IOUT2 = IOUT_{FS} \times CODE / 65536$$

where

- CODE is the decimal representation of the DAC data input word. (5)

For the case where IOUT1 and IOUT2 drive resistor loads R_L directly, this translates into single ended voltages at IOUT1 and IOUT2 as Equation 6 and Equation 7 respectively:

$$VOUT1 = AVDD – | IOUT1 | \times R \quad (6)$$

$$VOUT2 = AVDD – | IOUT2 | \times R \quad (7)$$

Assuming that the data is full scale (65536 in offset binary notation) and the R_L is 25 Ω, the differential voltage between pins IOUT1 and IOUT2 can be expressed in Equation 8 through Equation 10:

$$VOUT1 = AVDD – | –0\ mA | \times 25\ \Omega = 3.3\ V \quad (8)$$

$$VOUT2 = AVDD – | –20\ mA | \times 25\ \Omega = 2.8\ V \quad (9)$$

$$VDIFF = VOUT1 – VOUT2 = 0.5\ V \quad (10)$$

NOTE

Take care to not exceed the compliance voltages at node IOUT1 and IOUT2, which would lead to increased signal distortion.

7.3.9 DAC Output SINC Response

Due to the sampled nature of a high-speed DAC, the well known sin(x)/x (or SINC) response can significantly attenuate higher frequency output signals. Figure 33 shows the unitized SINC attenuation roll-off with respect to the final DAC sample rate in 4 Nyquist zones. For example, if the final DAC sample rate F_S = 1.0 GSPS, then a tone at 440 MHz is attenuated by 3.0 dB. Although the SINC response can create challenges in frequency planning, one side benefit is the natural attenuation of Nyquist images. The increased over-sampling ratio of the input data provided by the 2x and 4x digital interpolation modes of the DAC5681Z improves the SINC roll-off (droop) within the original signal's band of interest.

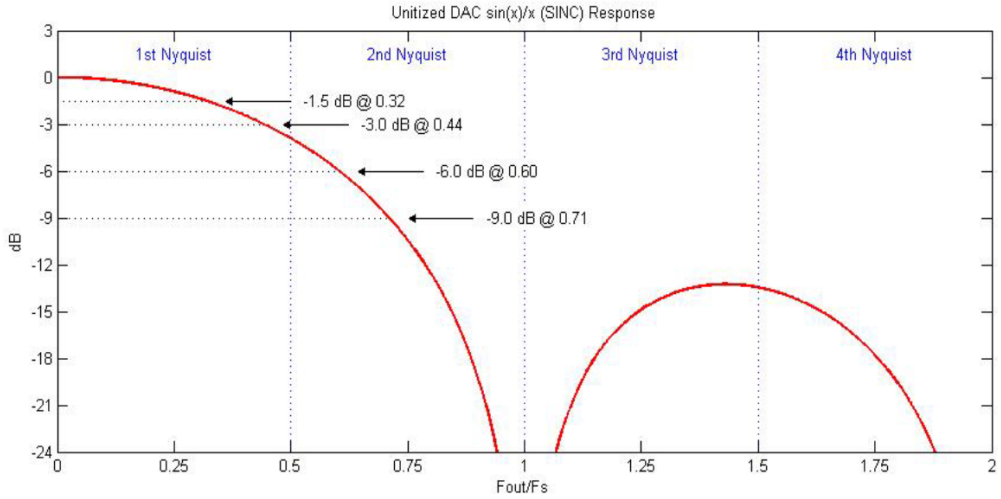


Figure 33. Unitized DAC sin(x)/x (SINC) Response

7.3.10 Test Methodology

Typical AC specifications were characterized with the DAC5681ZEVM using the test configuration shown in Figure 34. A sinusoidal master clock frequency is generated by an HP8665B signal generator and into a splitter. One output drives an Agilent 8133A pulse generator, and the other drives the CDCM7005 clock driver. The 8133A converts the sinusoidal frequency into a square wave output clock and drives an Agilent ParBERT 81250A pattern-generator clock. On the EVM, the DAC5681Z CLKIN/C input clock is driven by an CDCM7005 clock distribution chip that is configured to simply buffer the external 8665B clock or divide it down for PLL test configurations.

The DAC5681Z output is characterized with a Rohde and Schwarz FSU spectrum analyzer. For WCDMA signal characterization, it is important to use a spectrum analyzer with high IP3 and noise subtraction capability so that the spectrum analyzer does not limit the ACPR measurement.

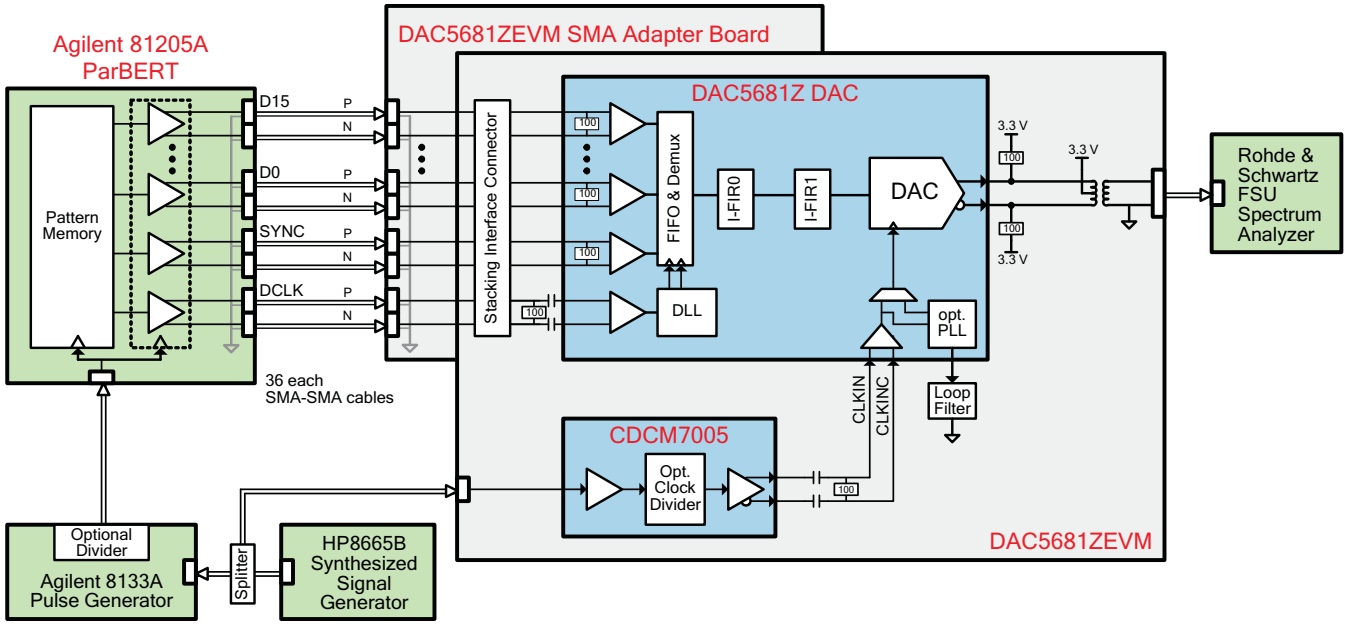


Figure 34. DAC5681Z Test Configuration for Normal Clock Mode

7.3.11 CMOS Digital Inputs

Figure 35 shows a schematic of the equivalent CMOS digital inputs of the DAC5681Z. SDIO and SCLK have pulldown resistors while RESETB and SDENB have pullup resistors internal the DAC5681Z. See *Specifications*. The pullup and pulldown circuitry is approximately equivalent to 100 kΩ.

Figure 35. CMOS/TTL Digital Equivalent Input

7.3.12 Digital Self Test Mode

The DAC5681Z has a Digital Self Test (SLFTST) mode to designed to enable board level testing without requiring specific input data test patterns. The SLFTST mode is enabled via the CONFIG1 **SLFTST_ena** bit and results are only valid when CONFIG3 **SLFTST_err_mask** bit is cleared. An internal Linear Feedback Shift Register (LFSR) is used to generate the input test patterns for the full test cycle while a checksum result is computed on the digital signal chain outputs. The LVDS input data bus is ignored in SLFTST mode. After the test cycle completes, if the checksum result does not match a hardwired comparison value, the STATUS4 **SLFTST_err** bit is set and will remain set until cleared by writing a 0 to the **SLFTST_err** bit. A full self test cycle requires no more than 400,000 CLKIN/C clock cycles to complete and will automatically repeat until the **SLFTEST_ena** bit is cleared.

To initiate a the Digital Self Test, use the following steps:

1. Provide a normal CLKIN/C input clock. (The PLL is not used in SLFTST mode.)
2. Provide a RESETB pulse to perform a hardware reset on device.
3. Program the registers with the values shown in Table 4. These register values contain the settings to properly configure the SLFTST including **SLFTST_ena** and **SLFTST_err_mask** bits
4. Provide a 1 on the SYNCP/N input to initiate TXENABLE.
5. Wait at a minimum of 400,000 CLKIN/C cycles for the SLFTST to complete. Example: If CLKIN = 1 GHz, then the wait period is 400,000 × 1 / 1 GHz = 400 µSec.
6. Read STATUS4 **SLFTST_err** bit. If set, a self test error has occurred. The **SLFTST_err** status may optionally be programmed to output on the SDO pin if using the 3-bit SIF interface. See Table 4 Note (1).
7. (Optional) The SLFTST function automatically repeats until **SLFTST_ena** bit is cleared. To the loop the test, write a 0 to STATUS4 **SLFTST_err** to clear previous errors and continue at Step 5.
8. To continue normal operating mode, provide another RESETB pulse and reprogram registers to the desired normal settings.

Table 4. Digital Self Test (SLFTST) Register Values

REGISTER	ADDRESS (hex)	VALUE (Binary)	VALUE (Hex)
CONFIG1	01	00011000	18
CONFIG2	02	11101010	EA
CONFIG3	03	10110000	B0
STATUS4	04	00000000	00
CONFIG5	05	00000110	06
CONFIG6	06	00001111	0F
CONFIG12	0C	00001010	0A
CONFIG13	0D	01010101	55
CONFIG14(1)	0E	00001010	0A
CONFIG15	0F	10101010	AA
All others	–	Default	Default

(1) If using a 3-bit SIF interface, the SDO pin can be programmed to report **SLFTST_err** status via the **SDO_fun_sel(2:0)** bits. In this case, set CONFIG14 = 10101010 or AA hex.

7.3.13 Analog Current Outputs

Figure 36 shows a simplified schematic of the current source array output with corresponding switches in a current sink configuration. Differential switches direct the current into either the positive output node, IOUT1, or its complement, IOUT2, then through the individual NMOS current sources. The output impedance is determined by the stack of the current sources and differential switches, and is typically >300 kΩ in parallel with an output capacitance of 5 pF.

The external output resistors are referenced to an external ground. The minimum output compliance at nodes IOUT1 and IOUT2 is limited to AVDD – 0.5 V, determined by the CMOS process. Beyond this value, transistor breakdown may occur resulting in reduced reliability of the DAC5681Z device. The maximum output compliance voltage at nodes IOUT1 and IOUT2 equals AVDD + 0.5 V. Exceeding the minimum output compliance voltage adversely affects distortion performance and integral non-linearity. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUT1 and IOUT2 does not exceed 0.5 V.

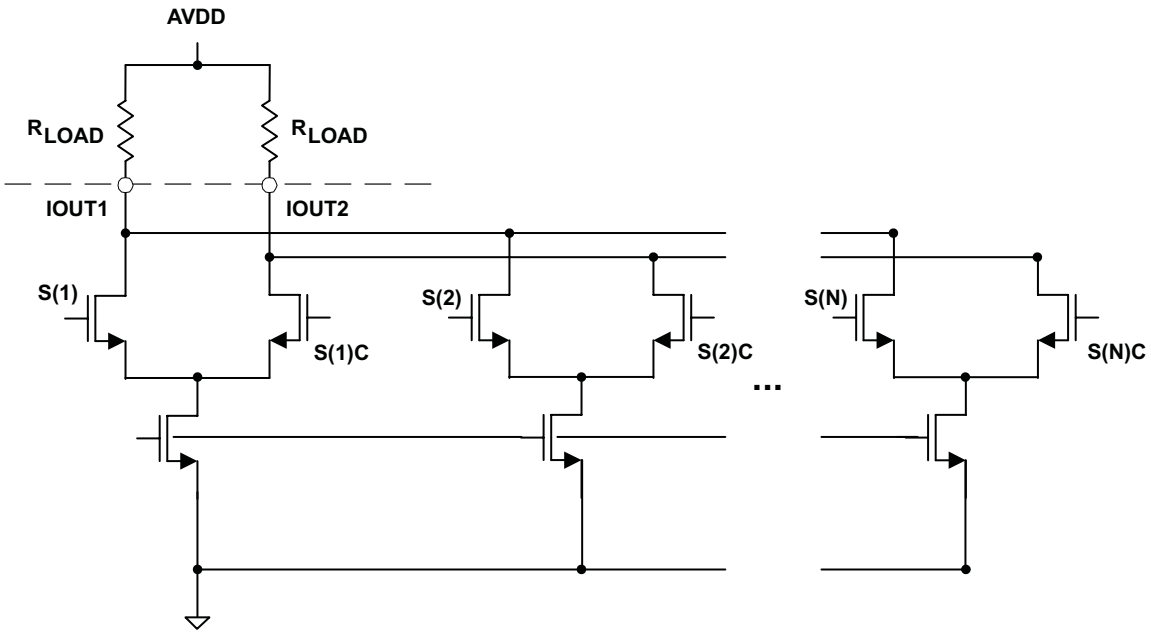


Figure 36. Equivalent Analog Current Output

The DAC5681Z can be easily configured to drive a doubly terminated 50-Ω cable using a properly selected RF transformer. Figure 37 and Figure 38 show the 50-Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratio, respectively. The center tap of the primary input of the transformer has to be connected to AVDD to enable a DC current flow. Applying a 20-mA full-scale output current would lead to a 0.5 V_{PP} for a 1:1 transformer, and a 1-V_{PP} output for a 4:1 transformer. The low DC-impedance between IOUT1 or IOUT2 and the transformer center tap sets the center of the ac-signal at AVDD, so the 1-V_{PP} output for the 4:1 transformer results in an output between AVDD + 0.5 V and AVDD – 0.5 V.

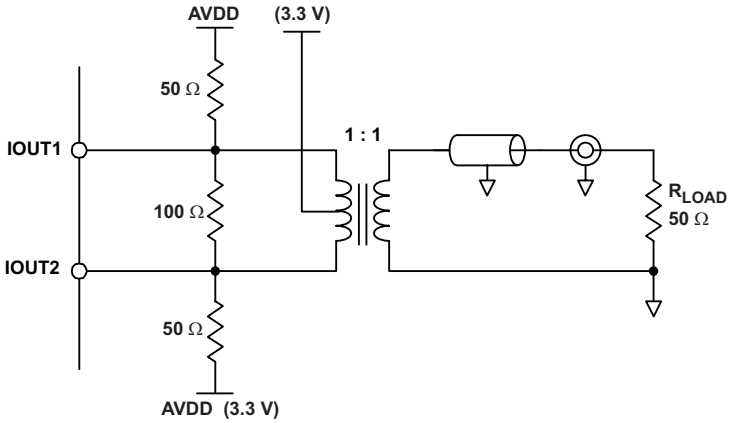


Figure 37. Driving a Doubly-Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

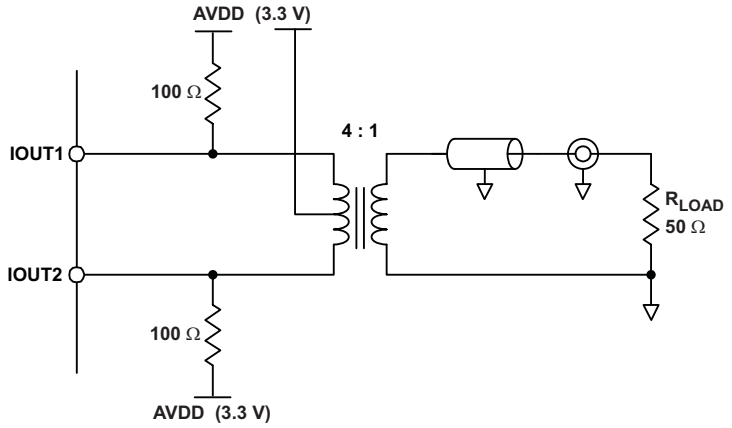


Figure 38. Driving a Doubly-Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

7.3.14 Designing the PLL Loop Filter

To minimize phase noise given for a given fDAC and M/N, the values of **PLL_gain** and **PLL_range** are selected so that G_{VCO} is minimized and within the MIN and MAX frequency for a given setting.

The external loop filter components C1, C2, and R1 are set by the G_{VCO}, M/N, the loop phase margin φ_d and the loop bandwidth ω_d. Except for applications where abrupt clock frequency changes require a fast PLL lock time, it is suggested that φ_d be set to at least 80 degrees for stable locking and suppression of the phase noise side lobes. Phase margins of 60 degrees or less can be sensitive to board layout and decoupling details.

See Figure 39, the recommend external loop filter topology. C1, C2, and R1 are calculated by Equation 11 and Equation 12:

$$C1 = \tau1\left(1 - \frac{\tau2}{\tau3}\right) \qquad C2 = \frac{\tau1 \times \tau2}{\tau3} \qquad R1 = \frac{\tau3^2}{\tau1(\tau3 - \tau2)} \tag{11}$$

where,

$$\tau 1 = \frac{K_d K_{VCO}}{\omega_d^2}\left(\tan \Phi_d + \sec \Phi_d\right) \quad \tau 2 = \frac{1}{\omega_d\left(\tan \Phi_d + \sec \Phi_d\right)} \quad \tau 3 = \frac{\tan \Phi_d + \sec \Phi_d}{\omega_d}$$

where

- charge pump current: iqp = 1 mA
  vco gain: $K_{VCO} = 2\pi \times G_{VCO}$ rad/V
  PFD Frequency: $\omega_d \leq 160$ MHz
  phase detector gain: $K_d = iqp \div (2 \times \pi \times M)$ A/rad (12)

The Excel spreadsheet (SLAC169) is available from Texas Instruments for automatically calculating the values for C1, R1 and C2.

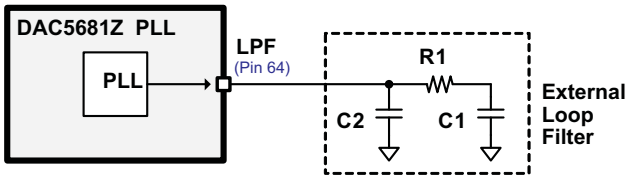


Figure 39. Recommended External Loop Filter Topology

7.3.15 System Examples

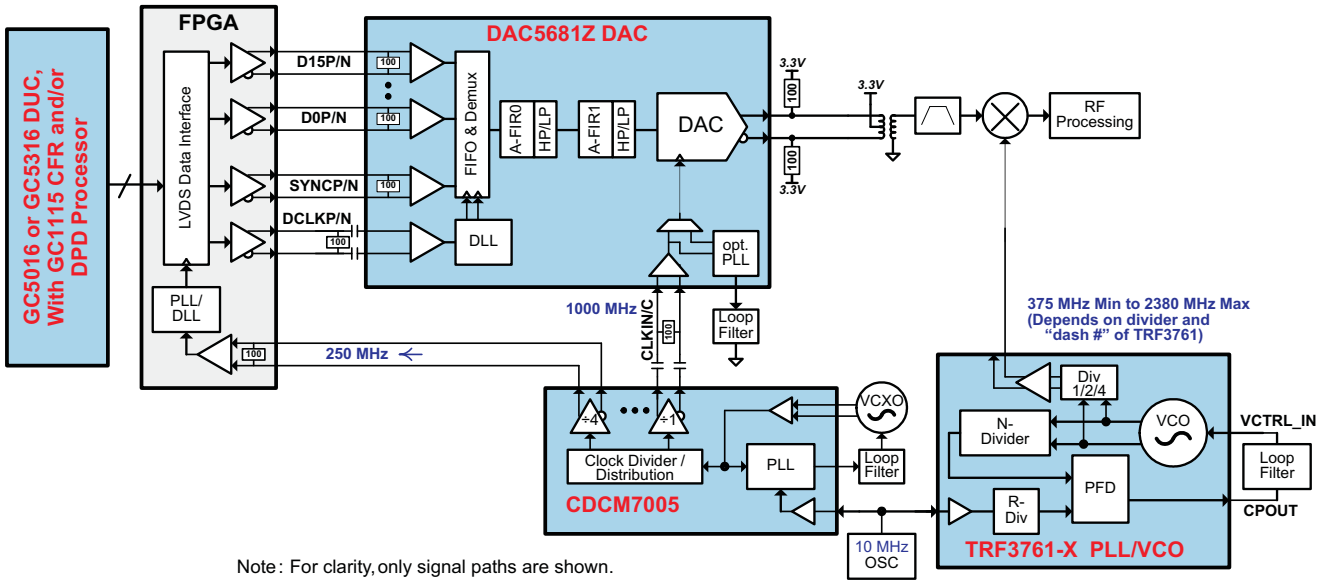
7.3.15.1 Digital Interface and Clocking Considerations for Application Examples

The LVDS digital input bus of the DAC5681Z can be driven by an FPGA or digital ASIC. This input signal can be generated directly by the FPGA, or fed by a Texas Instruments Digital Up Converter (DUC) such as the GC5016 or GC5316. Optionally, a GC1115 Crest Factor Reduction (CFR) or Digital Pre-Distortion (DPD) processor may be inserted in the digital signal chain for improving the efficiency of high-power RF amplifiers. For the details on the DAC's high-rate digital interface, refer to the *LVDS Data Interfacing* section.

A low phase noise clock for the DAC at the final sample rate can be generated by a VCXO and a Clock Synchronizer/PLL such as the Texas Instruments CDCM7005 or CDCE62005, which can also provide other system clocks. An optional system clocking solution can use the DAC in clock multiplying PLL mode in order to avoid distributing a high-frequency clock at the DAC sample rate; however, the internal VCO phase noise of the DAC in PLL mode may degrade the quality of the DAC output signal.

7.3.15.2 Digital IF Output Radio

Refer to Figure 40 for an example Digital IF Output Radio. The DAC5681Z receives a real digital input data stream and increases the sample rate through interpolation by a factor of 2 or 4. By performing digital interpolation on the input data, undesired images of the original signal can be pushed out of the band of interest and more easily suppressed with analog filters. Real mixing is available at each stage of interpolation using the LP/HP filter modes to upconvert the signal. (See *Digital Real Upconversion*) The DAC output signal would typically be terminated with a transformer (see the *Analog Current Outputs* section). An IF filter, either LC or SAW, is used to suppress the DAC Nyquist zone images and other spurious signals before being mixed to RF with a mixer. The TRF3671 Frequency Synthesizer, with integrated VCO, may be used to drive a common LO input of the mixers for frequencies between 375 and 2380 MHz.



Note: For clarity, only signal paths are shown.

Figure 40. System Diagram of a Digital IF Output Radio

7.3.15.3 CMTS/VOD Transmitter

The exceptional SNR of the DAC5681Z enables a cable modem termination system (CMTS) or video on demand (VOD) QAM transmitter in excess of the stringent DOCSIS specification, with >74 dBc and 75 dBc in the adjacent and alternate channels.

See Figure 40 for an example IF Output Radio – this signal chain is nearly identical to a typical system using the DAC5681Z for a cost optimized two QAM transmitter. A GC5016 would accept two separate symbol rate inputs and provide pulse shaping and interpolation to ≈128 MSPS. The two QAM carriers would be combined into two groups of two QAM carriers with intermediate frequencies of approximately 30 MHz to 40 MHz. The GC5016 would output data to the DAC5681Z through an FPGA for CMOS to LVDS translation. The DAC5681Z would provide 2x or 4x interpolation to increase the frequency of the 2nd Nyquist zone image. The signal is then output through a transformer and to an RF upconverter.

7.3.15.4 High-Speed Arbitrary Waveform Generator

The 1GSPS bandwidth input data bus combined with the 16-bit DAC resolution of the DAC5681Z allows wideband signal generation for test and measurement applications. In this case, interpolation is not desired by the FPGA-based waveform generator as it can make use of the full Nyquist bandwidth of up to 500 MHz.

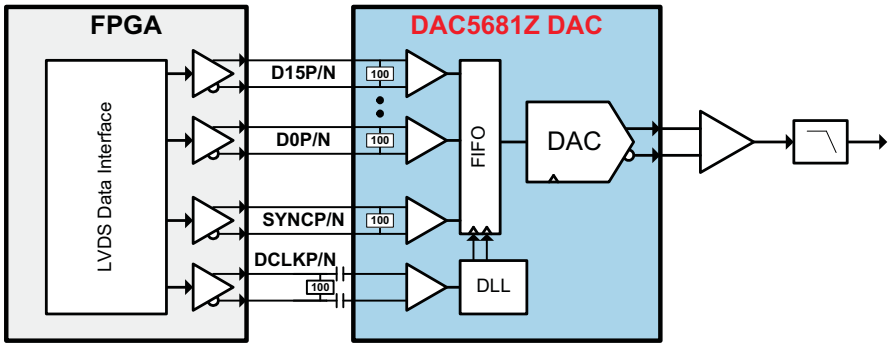


Figure 41. System Diagram of Arbitrary Waveform Generator

7.3.16 Initialization Set-Up

7.3.16.1 Recommended Start-Up Sequence

The following start-up sequence is recommended to initialize the DAC5681Z:

1. Supply all 1.8-V (CLKVDD, DVDD, VFUSE) voltages simultaneously followed by all 3.3-V (AVDD and IOVDD) voltages.
2. Provide stable CLKIN/C clock.
3. Toggle RESETB pin for a minimum 25-nSec active low pulse width.
4. Program all desired SIF registers. Set **DLL_Restart** bit during this write cycle. The CONFIG10 register value should match the corresponding DCLKP/N frequency range in the *Electrical Characteristics – Digital Specifications* table.
5. Provide stable DCLKP/N clock. (This can also be provided earlier in the sequence)
6. Clear the **DLL_Restart** bit when the DCLKP/N clock is expected to be stable.
7. Verify the status of **DLL_Lock** and repeat until set to 1. **DLL_Lock** can be monitored by reading the STATUS0 register or by monitoring the SDO pin in 3-wire SIF mode. (See *CONFIG14 SDO_func_sel*.)
8. Enable transmit of data by asserting the LVDS SYNCP/N input or setting CONFIG3 **SW_sync** bit. (See *CONFIG3 SW_sync* and *CONFIG3 SW_sync_sel*.) The SYNC source must be held at a logic 1 to enable data flow through the DAC. If multiple DAC devices require synchronization, refer to the *Recommended Multi-DAC Synchronization Procedure*.
9. Provide data flow to LVDS D[15:0]P/N pins. If using the LVDS SYNCP/N input, data can be input simultaneous with the logic 1 transition of SYNCP/N.

7.3.16.2 Recommended Multi-Dac Synchronization Procedure

The DAC5681Z provides a mechanism to synchronize multiple DAC devices in a system. The procedure has two steps involving control of the CONFIG5 **clkdiv_sync_dis** bits as well as external control of the LVDS SYNCP/N input. (All DACs involved need to be configured to accept the external SYNCP/N input and not *software* sync mode).

1. Synchronize Clock Dividers (for each DAC):
   (a) Set CONFIG5 **clkdiv_sync_dis** = 0.
   (b) Toggle SYNCP/N input to all DACs simultaneously (same input to all DACs).
2. Synchronize FIFO pointers (for each DAC):
   (a) Set CONFIG5 **clkdiv_sync_dis** = 1 (Disable clock divider re-sync).
   (b) Wait a minimum of 50 CLKIN cycles from previous SYNCP/N toggle. In practice, the time required to write the above register value will typically occupy more than 50 cycles.
   (c) Assert SYNCP/N input and hold at 1 to all DACs simultaneously. Holding this at 1 is effectively the TXENABLE for the chip so data will be output on the analog pins.
3. After the normal pipeline delay of the device, the outputs of all DACs will be synchronized to within ±1 DAC clock cycle.

7.4 Device Functional Modes

The primary modes of operation, listed in Table 5, are selected by registers CONFIG1, CONFIG2 and CONFIG3.

Table 5. DAC5681Z Modes of Operation

MODE NAME	NO. OF DACS OUT	INTERP. FACTOR	FIR0, CMIX0 MODE	FIR1, CMIX1 MODE	DEVICE CONFIG.	LVDS INPUT DATA MODE	MAX CLKIN FREQ (MHz)(1)	MAX DCLK FREQ [DDR] (MHZ)	MAX TOTAL INPUT BUS RATE (MSPS)	MAX INPUT DATA RATE PER CHAN (#CH @ MSPS)	MAX SIGNAL BW PER DAC (MHz) (2)
1X1 (Bypass)	1	X1	–	–	Single Real	A	1000	500	1000	1 at 1000	500
1X2	1	X2	–	LP	Single Real	A	1000	250	500	1 at 500	200
1X2 HP	1	X2	–	HP	Single Real	A	1000	250	500	1 at 500	200
1X4	1	X4	LP	LP	Single Real	A	1000	125	250	1 at 250	100
1X4 LP/HP	1	X4	LP	HP	Single Real	A	1000	125	250	1 at 250	100
1X4 HP/LP	1	X4	HP	LP	Single Real	A	1000	125	250	1 at 250	50
1X4 HP/HP	1	X4	HP	HP	Single Real	A	1000	125	250	1 at 250	50

(1) Also the final DAC sample rate in MSPS.
(2) Assumes a 40% passband for FIR0 and/or FIR1 filters in all modes except 1X1 and 2X1 where simple Nyquist frequency is listed. Slightly wider bandwidths may be achievable depending on filtering requirements. Refer to *FIR Filters* section for more detail on filter characteristics. Also refer to Table 6 for IF placement and upconversion considerations.

7.4.1 Clock and Data Modes

There are two modes of operation to drive the internal clocks on the DAC5681Z. Timing diagrams for both modes are shown in Figure 42. EXTERNAL CLOCK MODE accepts an external full-rate clock input on the CLKIN/CLKINC pins to drive the DACs and final logic stages while distributing an internally divided down clock for lower speed logic such as the interpolating FIRs. PLL CLOCK MODE uses an internal clock multiplying PLL to derive the full-rate clock from an external lower rate reference frequency on the CLKIN/CLKINC pins. In both modes, an LVDS half-rate data clock (DCLKP/DCLKN) is provided by the user and is typically generated by a *toggling data bit* to maintain LVDS data to DCLK timing alignment. LVDS data relative to DCLK is input using Double Data Rate (DDR) switching using both rising and falling edges as shown in *Clock Inputs*. The CONFIG10 register contains user controlled settings for the DLL to adjust for the DCLK input frequency and various t_{SKEW} timing offsets between the LVDS data and DCLK. The CDCM7005 and CDCE62005 from Texas Instruments are recommended for providing phase aligned clocks at different frequencies for device-to-device clock distribution and multiple DAC synchronization.

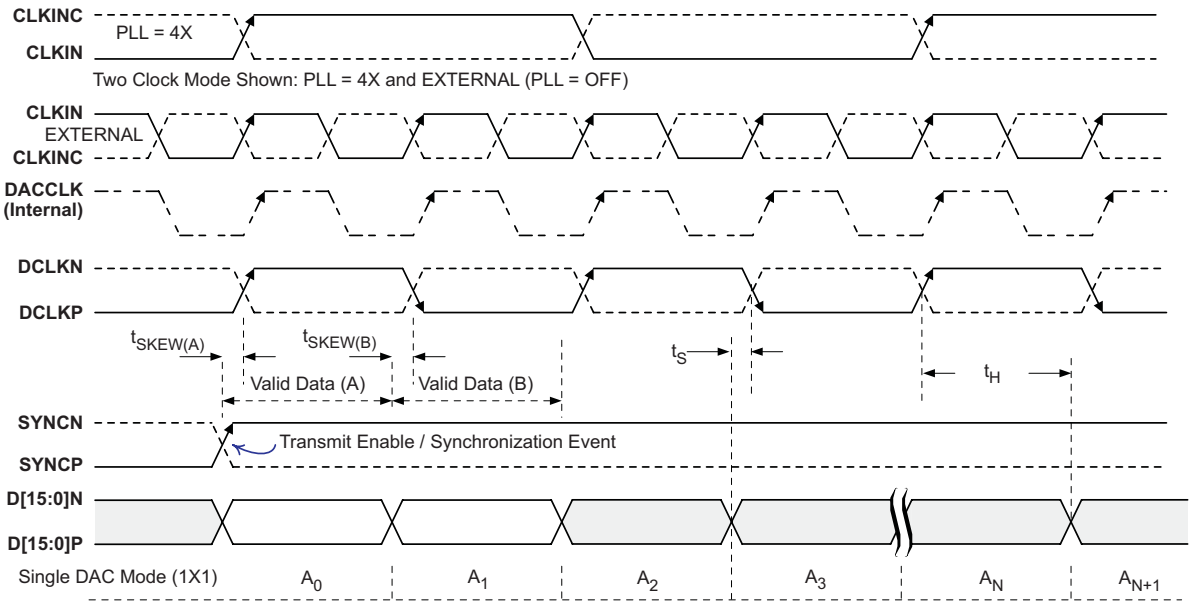


Figure 42. Clock and Data Timing Diagram

7.4.2 PLL Clock Mode

In PLL Clock Mode, the user provides an external reference clock to the CLKIN/C input pins. Refer to Figure 43. An internal clock multiplying PLL uses the lower-rate reference clock to generate a high-rate clock for the DAC. This function is very useful when a high-rate clock is not already available at the system level; however, the internal VCO phase noise in PLL Clock Mode may degrade the quality of the DAC output signal when compared to an external low jitter clock source.

The internal PLL has a type four phase-frequency detector (PFD) comparing the CLKIN/C reference clock with a feedback clock to drive a charge pump controlling the VCO operating voltage and maintaining synchronization between the two clocks. An external lowpass filter is required to control the loop response of the PLL. See the Table 7 section for the filter setting calculations. This is the only mode where the LPF filter applies.

The input reference clock N-Divider is selected by CONFIG9 PLL_n(2:0) for values of ÷1, ÷2, ÷4 or ÷8. The VCO feedback clock M-Divider is selected by CONFIG9 PLL_m(4:0) for values of ÷1, ÷2, ÷4, ÷8, ÷16 or ÷32. The combination of M-Divider and N-Divider form the clock multiplying ratio of M/N. If the reference clock frequency is greater than 160 MHz, use a N-Divider of ÷2, ÷4 or ÷8 to avoid exceeding the maximum PFD operating frequency.

For DAC sample rates less than 500MHz, the phase noise of DAC clock signal can be improved by programming the PLL for twice the desired DAC clock frequency, and setting the CONFIG11 VCO_div2 bit. If not using the PLL, set CONFIG5 PLL_bypass and CONFIG6 PLL_sleep to reduce power consumption. In some cases, it may be useful to reset the VCO control voltage by toggling CONFIG11 PLL_LPF_reset.

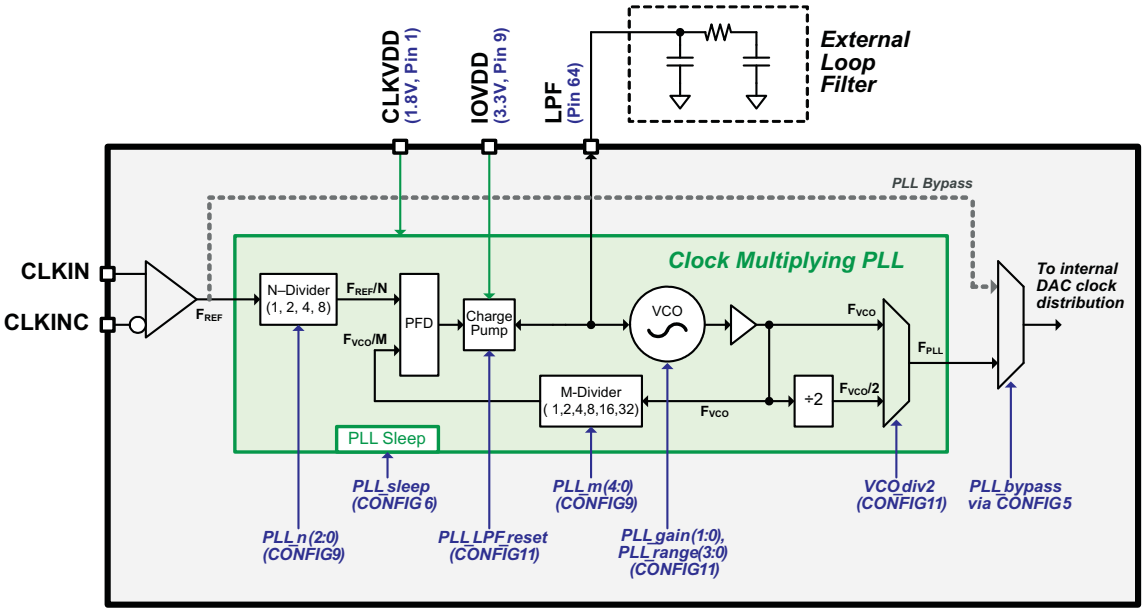


Figure 43. Functional Block Diagram for PLL

7.4.3 Clock Inputs

Figure 44 shows an equivalent circuit for the LVDS data input clock (DCLKP/N).

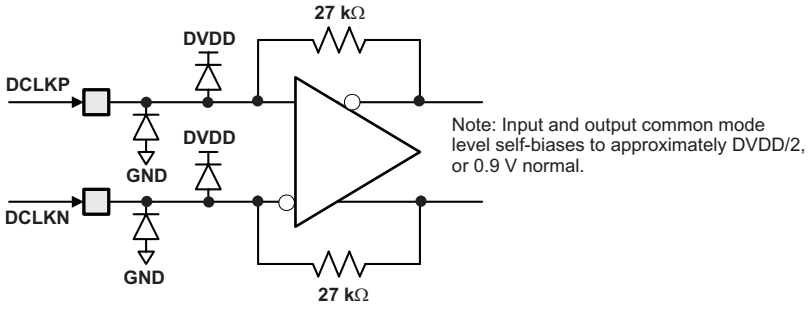


Figure 44. DCLKP/N Equivalent Input Circuit

Figure 45 shows an equivalent circuit for the DAC input clock (CLKIN/C).

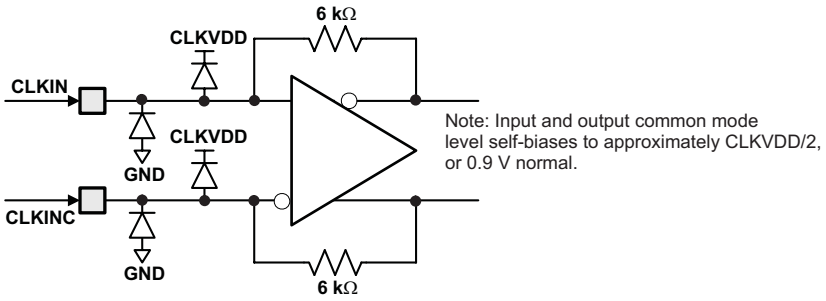


Figure 45. CLKIN/C Equivalent Input Circuit

Figure 46 shows the preferred configuration for driving the CLKIN/CLKINC input clock with a differential ECL/PECL source.

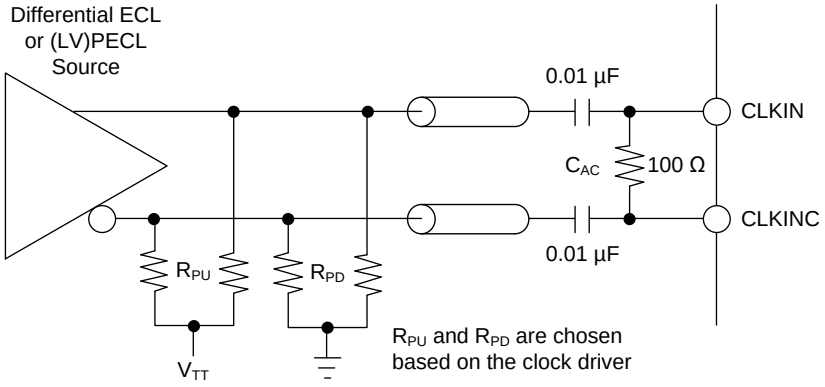


Figure 46. Preferred Clock Input Configuration With a Differential ECL/PECL Clock Source

7.5 Programming

7.5.1 Serial Interface

The serial port of the DAC5681Z is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of DAC5681Z. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 pin interface by **SIF4** in register **CONFIG5**. In both configurations, **SCLK** is the serial interface input clock and **SDENB** is serial interface enable. For 3 pin configuration, **SDIO** is a bidirectional pin for both data in and data out. For 4 pin configuration, **SDIO** is data in only and SDO is data out only. Data is input into the device with the rising edge of SCLK. Data is output from the device on the falling edge of **SCLK**.

Each read/write operation is framed by signal **SDENB** (Serial Data Enable Bar) asserted low for 2 to 5 bytes, depending on the data length to be transferred (1–4 bytes). The first frame byte is the instruction cycle which identifies the following data transfer cycle as read or write, how many bytes to transfer, and what address to transfer the data.

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/W	N1	N0	A4	A3	A2	A1	A0

R/W Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from DAC5681Z and a low indicates a write operation to DAC5681Z.

[N1 : N0] Identifies the number of data bytes to be transferred per Table 5. Data is transferred MSB first.

Table 6. Number of Transferred Bytes Within One Communication Frame

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

[A4 : A0] Identifies the address of the register to be accessed during the read or write operation. For multi-byte transfers, this address is the starting address. The address is written to the DAC5681Z MSB first and counts down for each byte.

Figure 47 shows the serial interface timing diagram for a DAC5681Z write operation. **SCLK** is the serial interface clock input to DAC5681Z. Serial data enable **SDENB** is an active low input to DAC5681Z. **SDIO** is serial data in. Input data to DAC5681Z is clocked on the rising edges of **SCLK**.

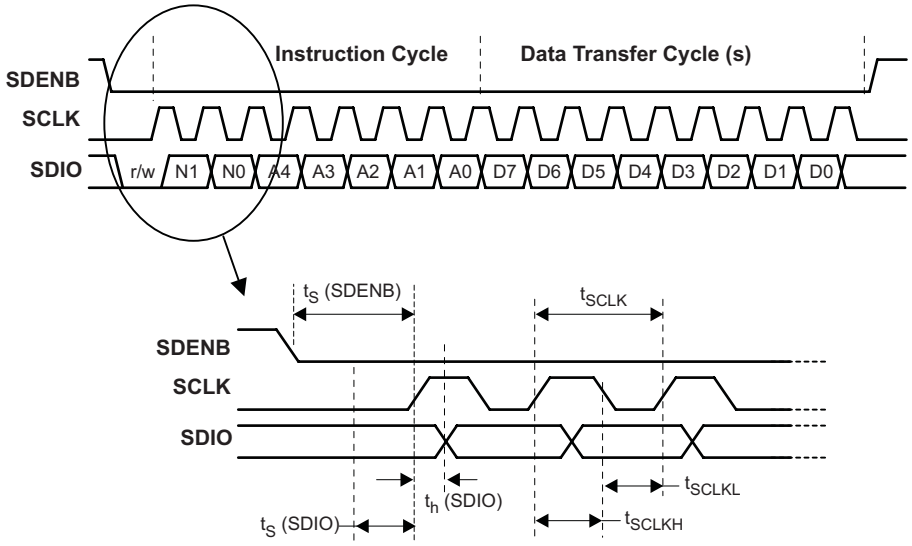


Figure 47. Serial Interface Write Timing Diagram

Figure 48 shows the serial interface timing diagram for a DAC5681Z read operation. **SCLK** is the serial interface clock input to DAC5681Z. Serial data enable **SDENB** is an active low input to DAC5681Z. **SDIO** is serial data in during the instruction cycle. In 3-pin configuration, **SDIO** is data out from DAC5681Z during the data transfer cycles, while **SDO** is in a high-impedance state. In 4 pin configuration, **SDO** is data out from DAC5681Z during the data transfer cycles. At the end of the data transfer, SDO will output low on the final falling edge of SCLK until the rising edge of SDENB when it will enter 3-state output.

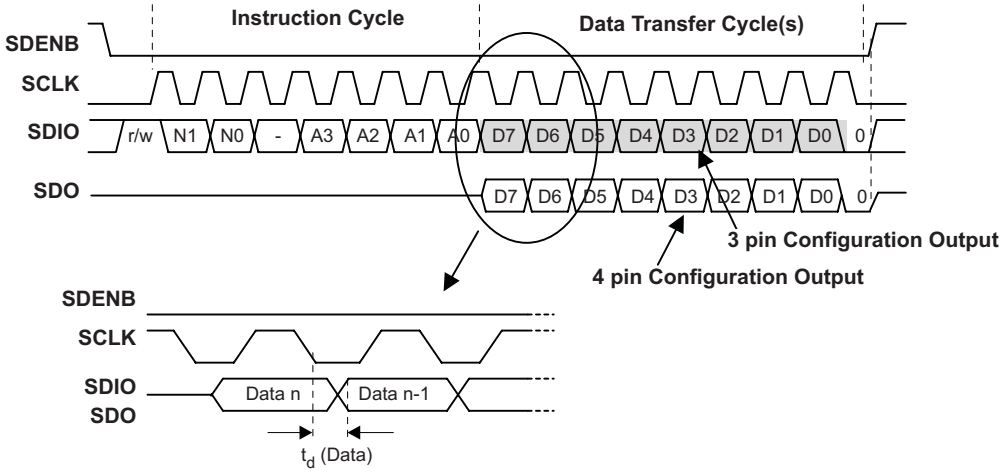


Figure 48. Serial Interface Read Timing Diagram

7.6 Register Maps

Table 7. Register Map

NAME	ADDRESS	DEFAULT	(MSB) BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	(LSB) BIT 0
STATUS0	0x00	0x0B	PLL_lock	DLL_lock	Unused	device_ID(2:0)			version(1:0)	
CONFIG1	0x01	0x10	DAC_delay(1:0)		Unused	fir_ena	SLFTST _ena	FIFO_offset(2:0)		
CONFIG2	0x02	0xC0	Twos_ comp	Reserved	FIR2x4x	Unused	Reserved	FIR1_HP	Reserved	FIR0_HP
CONFIG3	0x03	0x70	DAC_offset _ena	SLFTST_err _mask	FIFO_err_ mask	Pattern_err _mask	Reserved	Reserved	SW_sync	SW_sync _sel
STATUS4	0x04	0x00	Unused	SLFTST_err	FIFO_err	Pattern_ err	Unused	Unused	Unused	Unused
CONFIG5	0x05	0x00	SIF4	rev_bus	clkdiv_ sync_dis	Reserved	Reserved	DLL_ bypass	PLL_ bypass	Reserved
CONFIG6	0x06	0x0C	Reserved	Unused	Reserved	Sleep_A	BiasLPF_A	Reserved	PLL_ sleep	DLL_ sleep
CONFIG7	0x07	0xFF	DACA_gain(3:0)				Reserved			
CONFIG8	0x08	0x00	Reserved					DLL_ restart	Reserved	
CONFIG9	0x09	0x00	PLL_m(4:0)					PLL_n(2:0)		
CONFIG10	0x0A	0x00	DLL_delay(3:0)				DLL_invclk	DLL_ifixed(2:0)		
CONFIG11	0x0B	0x00	PLL_LPF _reset	VCO_div2	PLL_gain(1:0)		PLL_range(3:0)			
CONFIG12	0x0C	0x00	Reserved		Offset_sync	OffsetA(12:8)				
CONFIG13	0x0D	0x00	OffsetA(7:0)							
CONFIG14	0x0E	0x00	SDO_func_sel(2:0)			Reserved				
CONFIG15	0x0F	0x00	Reserved							

7.6.1 STATUS0 – Address: 0x00, Default = 0x0B

Figure 49. STATUS0 Register

7	6	5	4	3	2	1	0
PLL_lock	DLL_lock	Unused		device_ID(2:0)		version(1:0)	
0	0	0	0	1	0	1	1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

PLL_lock: Asserted when the internal PLL is locked. (**Read Only**)

DLL_lock: Asserted when the internal DLL is locked. Once the DLL is locked, this bit should remain a 1 unless the DCLK input clock is removed or abruptly changes frequency causing the DLL to fall out of lock. (**Read Only**)

device_ID(2:0): Returns 010 for DAC5681Z Device_ID code. (**ReadOnly**)

version(1:0): A hardwired register that contains the register set version of the chip. (**ReadOnly**)

version (1:0)	Identification
01	PG1.0 Initial Register Set
10	PG1.1 Register Set
11	Production Register Set

7.6.2 CONFIG1 – Address: 0x01, Default = 0x10

Figure 50. CONFIG1 Register

7	6	5	4	3	2	1	0
DAC_delay(1:0)		Unused	FIR_ena	SLFTST_ena	FIFO_offset(2:0)		
0	0	0	1	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

DAC_delay(1:0): DAC data delay adjustment. (0–3 periods of the DAC clock) This can be used to adjust system level output timing. The same delay is applied to DACA data paths.

FIR_ena: When set, the interpolation filters are enabled.

SLFTST_ena: When set, a Digital Self Test (SLFTST) of the core logic is enabled. Refer to *Digital Self Test Mode* section for details on SLFTST operation.

FIFO_offset(2:0): Programs the FIFO's output pointer location, allowing the input pointer to be shifted –4 to +3 positions upon SYNC. Default offset is 0 and is updated upon each sync event. **The recommended setting is 001**.

FIFO_offset(2:0)	Offset
011	+3
010	+2
001	+1
000	0
111	–1
110	–2
101	–3
100	–4

7.6.3 CONFIG2 – Address: 0x02, Default = 0xC0

Figure 51. CONFIG2 Register

7	6	5	4	3	2	1	0
Twos_comp	Reserved	FIR2x4x	Unused	Reserved	FIR1_HP	Reserved	FIR0_HP
1	1	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Twos_comp: When set (default) the input data format is expected to be 2s complement, otherwise offset binary format is expected.

Reserved (Bit 6): Set to 1 for proper operation.

FIR2x4x: When set, 4X interpolation of the input data is performed, otherwise 2X interpolation.

FIR1_HP: When set, the FIR1 functions in High Pass (HP) mode; otherwise, the Low Pass (LP) filter mode is used. In 1X4 mode, the cascaded combination of HP and LP modes of FIR0 and FIR1 can be used to perform real upconversion. See Dual-Channel Real Upconversion.

FIR0_HP: When set, the FIR0 functions in High Pass (HP) mode; otherwise, the Low Pass (LP) filter mode is used. In 1X4 mode, the cascaded combination of HP and LP modes of FIR0 and FIR1 can be used to perform real upconversion. See Dual-Channel Real Upconversion.

7.6.4 CONFIG3 – Address: 0x03, Default = 0x70

Figure 52. CONFIG3 Register

7	6	5	4	3	2	1	0
DAC_offset_ena	SLFTST_err_mask	FIFO_err_mask	Pattern_err_mask	Reserved	Reserved	SW_sync	SW_sync_sel
0	1	1	1	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

DAC_offset_ena: When set, the values of **OffsetA(12 :0)** in CONFIG12 through CONFIG13 registers are summed into the DAC-A data path. This provides a system-level offset adjustment capability that is independent of the input data.

SLFTST_err_mask: When set, masks out the **SLFTST_err** bit in STATUS4 register. Refer to Digital Self Test Mode section for details on SLFTST operation.

FIFO_err_mask: When set, masks out the **FIFO_err** bit in STATUS4 register.

Pattern_err_mask: When set, masks out the **Pattern err** bit in STATUS4 register.

Reserved (Bit 3): Set to 0 for proper operation.

Reserved (Bit 2): Set to 0 for proper operation.

SW_sync: This bit can be used as a substitute for the LVDS external SYNC input pins for both synchronization and transmit enable control.

SW_sync_sel: When set, the SW_sync bit is used as the only synchronization input and the LVDS external SYNC input pins are ignored.

7.6.5 STATUS4 – Address: 0x04, Default = 0x00

Figure 53. STATUS4 Register

7	6	5	4	3	2	1	0
Unused	SLFTST_err	FIFO_err	Pattern_err	Unused	Unused	Unused	Unused
0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

SLFTST_err: Asserted when the Digital Self Test (SLFTST) fails. To clear the error, write a 0 to this register bit. This bit is also output on the SDO pin when the Self Test is enabled via **SLFTST_ena** control bit in CONFIG1. Refer to *Digital Self Test Mode* section for details on SLFTST operation.

FIFO_err: Asserted when the FIFO pointers over run each other causing a sample to be missed. To clear the error, write a 0 to this register bit.

Pattern_err: A digital checkerboard pattern compare function is provided for board level confidence testing and DLL limit checks. If the **Pattern_err_mask** bit via CONFIG3 is cleared, logic is enabled to continuously monitor input FIFO data. Any received data pattern other than 0xAAAA or 0x5555 causes this bit to be set. To clear the error, flush out the previous pattern error by inputting at least 8 samples of the 0xAAAA and/or 0x5555, then write a 0 to this register bit.

7.6.6 CONFIG5 – Address: 0x05, Default = 0x00

Figure 54. CONFIG5 Register

7	6	5	4	3	2	1	0
SIF4	rev_bus	clkdiv_sync_dis	Reserved	Reserved	DLL_bypass	PLL_bypass	Reserved
0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

SIF4: When set, the serial interface is in 4 pin mode, otherwise it is in 3 pin mode. Refer to **SDO_func_sel (2:0)** bits in Table 7 for options available to output status indicator data on the SDO pin.

rev_bus: Reverses the LVDS input data bus so that the MSB to LSB order is swapped. This function is provided to ease board level layout and avoid wire crossovers in case the LVDS data source output bus is mirrored with respect to the DAC's input data bus.

clkdiv_sync_dis: Disables the clock divider sync when this bit is set.

Reserved (Bit 4): Set to 0 for proper operation.

Reserved (Bit 3): Set to 0 for proper operation.

DLL_bypass: When set, the DLL is bypassed and the LVDS data source is responsible for providing correct set-up and hold timing.

PLL_bypass: When set, the PLL is bypassed.

Reserved (Bit 0): Set to 0 for proper operation.

7.6.7 CONFIG6 – Address: 0x06, Default = 0x0C

Figure 55. CONFIG6 Register

7	6	5	4	3	2	1	0
Reserved	Unused	Reserved	Sleep_A	BiasLPF_A	Reserved	PLL_sleep	DLL_sleep
0	0	0	0	1	1	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Reserved (Bit 7): Reserved (Bit 7): Set to 0 for proper operation.

Reserved (Bit 5): Set to 0 for proper operation.

Sleep_A: When set, DACA is put into sleep mode.

BiasLPF_A: Enables a 95-kHz lowpass filter corner on the DACA current source bias when cleared. If this bit is set, a 472-kHz filter corner is used.

Reserved (Bit 2): Set to 1 for proper operation.

PLL_sleep: When set, the PLL is put into sleep mode.

DLL_sleep: When set, the DLL is put into sleep mode.

7.6.8 CONFIG7 – Address: 0x07, Default = 0xFF

Figure 56. CONFIG7 Register

7	6	5	4	3	2	1	0
DACA_gain(3:0)				Reserved			
1	1	1	1	1	1	1	1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

DACA_gain(3:0): Scales DACA output current in 16 equal steps.

$$\frac{VEXTIO}{R_{bias}} \times (DACA\_gain + 1)$$

Reserved (3:0): Set to 1111 for proper operation.

7.6.9 CONFIG8 – Address: 0x08, Default = 0x00

Figure 57. CONFIG8 Register

7	6	5	4	3	2	1	0
Reserved					DLL_restart	Reserved	
0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Reserved (7:3): Set to 00000 for proper operation.

DLL_restart: This bit is used to restart the DLL. When this bit is set, the internal DLL loop filter is reset to zero volts, and the DLL delay line is held at the center of its bias range. When cleared, the DLL will acquire lock to the DCLK signal. A DLL restart is accomplished by setting this bit with a serial interface write, and then clearing this bit with another serial interface write. Any interruption in the DCLK signal or changes to the DLL programming in the CONFIG10 register must be followed by this DLL restart sequence. Also, when this bit is set, the **DLL_lock** indicator in the STATUS0 register is cleared.

Reserved (1:0): Set to 00 for proper operation

7.6.10 CONFIG9 – Address: 0x09, Default = 0x00

Figure 58. CONFIG9 Register

7	6	5	4	3	2	1	0
PLL_m(4:0)					PLL_n(2:0)		
0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

PLL_m: M portion of the M/N divider of the PLL thermometer encoded:

PLL_m(4:0)	M value
00000	1
00001	2
00011	4
00111	8
01111	16
11111	32
All other values	Invalid

PLL_n: N portion of the M/N divider of the PLL thermometer encoded. If supplying a high rate CLKIN frequency, the PLL_n value should be used to divide down the input CLKIN to maintain a maximum PFD operating of 160 MHz.

PLL_n(2:0)	N value
000	1
001	2
011	4
111	8
All other values	Invalid

PLL Function:

$$f_{vco} = \left[\frac{(M)}{(N)}\right] \times f_{ref}$$

where f_{ref} is the frequency of the external DAC clock input on the CLKIN/CLKINC pins.

7.6.11 CONFIG10 – Address: 0x0A, Default = 0x00

Figure 59. CONFIG10 Register

7	6	5	4	3	2	1	0
DLL_delay(3:0)				DLL_invclk	DLL_ifixed(2:0)		
0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

DLL_delay(3:0): The DCLKP/N LVDS input data clock has a DLL to automatically skew the clock to LVDS data timing relationship, providing proper set-up and hold times. **DLL_delay(3:0)** is used to manually adjust the DLL delay ± from the fixed delay set by **DLL_ifixed(2:0)**. Adjustment amounts are approximate.

DLL_delay(3:0)	Delay Adjust (degrees)
1000	50°
1001	55°
1010	60°
1011	65°
1100	70°
1101	75°
1110	80°
1111	85°
0000	90° (Default)
0001	95°
0010	100°
0011	105°
0100	110°
0101	115°
0110	120°
0111	125°

DLL_invclk: When set, used to invert an internal DLL clock to force convergence to a different solution. This can be used in the case where the DLL delay adjustment has exceeded the limits of its range.

DLL_ifixed(2:0): Adjusts the DLL delay line bias current. Refer to the *Electrical Characteristics* table. Used in conjunction with the DLL_invclk bit to select appropriate delay range for a given DCLK frequency:
011 – maximum bias current and minimum delay range
000 – mid scale bias current
101 – minimum bias current and maximum delay range
100 – do not use.

7.6.12 CONFIG11 – Address: 0x0B, Default = 0x00

Figure 60. CONFIG11 Register

7	6	5	4	3	2	1	0
PLL_LPF_ reset	VCO_div2	PLL_gain(1:0)		PLL_range(3:0)			
0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

PLL_LPF_reset: When a logic high, the PLL loop filter (LPF) is pulled down to 0 V. Toggle from 1 to 0 to restart the PLL if an over-speed lock-up occurs. Over-speed can happen when the process is fast, the supplies are higher than nominal, and so on, resulting in the feedback dividers missing a clock.

VCO_div2: When set, the PLL CLOCK output is 1/2 the PLL VCO frequency. Used to run the VCO at 2X the needed clock frequency to reduce phase noise for lower input clock rates.

PLL_gain(1:0): Used to adjust the PLL's Voltage Controlled Oscillator (VCO) gain, K_{VCO}. Refer to *Electrical Characteristics*. By increasing the **PLL_gain**, the VCO can cover a broader range of frequencies; however, the higher gain also increases the phase noise of the PLL. In general, lower **PLL_gain** settings result in lower phase noise. The K_{VCO} of the VCO can also affect the PLL stability and is used to determine the loop filter components. See *Designing the PLL Loop Filter*.

PLL_range(3:0): Programs the PLL VCO fixed bias current. Refer to *Electrical Characteristics*. This setting, in conjunction with the PLL_gain(1:0), sets the achievable frequency range of the PLL VCO:
000 – minimum bias current and lowest VCO frequency range
111 – maximum bias current and highest VCO frequency range

7.6.13 CONFIG12 – Address: 0x0C, Default = 0x00

Figure 61. CONFIG12 Register

7	6	5	4	3	2	1	0
Reserved		Offset_sync	OffsetA(12:8)				
0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Reserved (1:0): Set to 00 for proper operation.

Offset_sync: On a change from 0 to 1 the values of the OffsetA(12:0) and OffsetB(12:0) control registers are transferred to the registers used in the DAC-A and DAC-B offset calculations. This double buffering allows complete control by the user as to when the change in the offset value occurs. This bit does not auto-clear. Prior to updating new offset values, it is recommended that the user clear this bit.

OffsetA(12:8): Upper 5 bits of the offset adjustment value for the A data path. (**SYNCED via Offset_sync**)

7.6.14 CONFIG13 – Address: 0x0D, Default = 0x00

Figure 62. CONFIG13 Register

7	6	5	4	3	2	1	0
OffsetA(7:0)							
0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

OffsetA(7:0): Lower 8 bits of the offset adjustment value for the A data path. (**SYNCED via Offset_sync**)

7.6.15 CONFIG14 – Address: 0x0E, Default = 0x00

Figure 63. CONFIG14 Register

7	6	5	4	3	2	1	0
SDO_func_sel(2:0)			Reserved				
0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

SDO_func_sel(2:0): Selects the signal for output on the SDO pin. When using the 3 pin serial interface mode, this allows the user to multiplex several status indicators onto the SDO pin. In 4 pin serial interface mode, programming this register to view one of the 5 available status indicators will override normal SDO serial interface operation.

SDO_func_sel (2:0)	Output to SDO
000, 110, 111	Normal SDO function
001	PLL_lock
010	DLL_lock
011	Pattern_err
100	FIFO_err
101	SLFTST_err

Reserved (4:0): Set to 00000 for proper operation.

7.6.16 CONFIG15 – Address: 0x0F, Default = 0x00

Figure 64. CONFIG15 Register

7	6	5	4	3	2	1	0
Reserved							
0	0	0	0	0	0	0	0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Reserved (7:0): Set to 0x00 for proper operation.

8 Application And Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

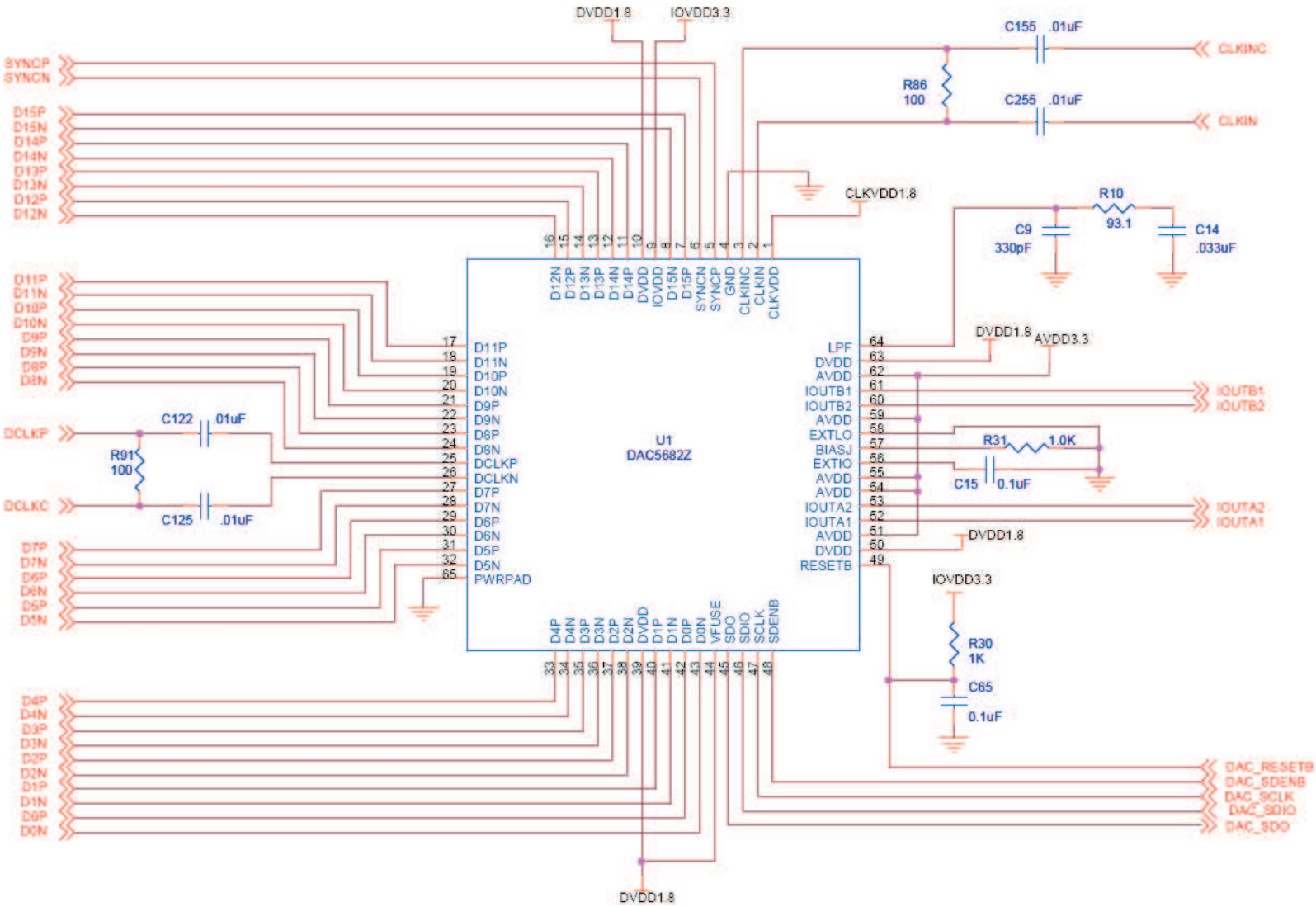
8.1 Application Information

The DAC5681z is a high-speed, wide bandwidth Digital-to-Analog converter. The DAC output can sample at 1Gsps allowing synthesis of real signal from 0 to 400 MHz with bandwidth of up to 400 MHz. When the DAC is operated in bypass mode, the maximum data rate is 1 Gsps and can sustain a signal bandwidth of 500 MHz. The interpolation modes of the DAC allow the input baseband rates to be 2-4 times slower than the DAC output rate reducing the processing requirements of the digital baseband processor and simplify the DAC image filtering requirements. The coarse mixing blocks within the DAC allow power efficient placement of the final carrier at the DAC output. Typically this DAC with its digital features is very well equipped communications applications; however it is also suitable for use in applications that require arbitrary waveform generation.

8.2 Typical Application

A typical application for the DAC5681Z is a wideband transmitter. The DAC is provided with some input digital baseband signal and it outputs an analog carrier. A typical configuration is described in the following:

- Datarate = 491.52 Msps (DCLK LVPECL or LVDS)
- 2x Interpolation
- External clock mode = 983.04 MHz (CLKIN LVPECL or LVDS)
- Input data = 4C WCDMA with IF frequency at 184.32 MHz
- AVDD/IOVDD = 3.3 V
- DVDD/CLKVDD=1.8 V
- SYNCP/N = LVDS 1
- IOUTAP/N to transformer



(1) Power supply decoupling capacitors not shown.

(2) Internal Reference configuration shown.

Figure 65. Typical Application Schematic

8.2.1 Design Requirements

The requirements for this design were to generate a 4-carrier WCDMA signal at an intermediate frequency of 184.32 MHz. The ACPR needs to be better than 65 dBc.

8.2.2 Detailed Design Procedure

The 4-carrier signal with an intermediate frequency of 184.32 MHz must be created in the digital processor at a sample rate of 491.52 Msps. These 16-bit samples are placed on the 16b LVDS input port of the DAC.

A differential DAC clock must be generated from a clock source at 983.04 MHz and a data clock at 491.52 MHz. This must be provided to the CLKIN and DCLK pins of the DAC respectively. The DAC register map must be reset, then programmed for 2x interpolation and external clock mode as per the data sheet. The digital sample format (2s complement or offset binary) must match the incoming data from the processor. The SYNC signal must he held high for the DAC to have an analog output.

The IOUOTA differential connections must be connected to a transformer to provide a single ended output. A typical 2:1 impedance transformer is used on the device EVM. The DAC5681Z EVM provides a good reference for this design example.

8.2.3 Application Curve

The spectrum analyzer plot in Figure 66 shows the ACPR for the transformer output using x2 interpolation, PLL Off mode. The results meet the system requirements for a minimum of 65-dBc ACPR.

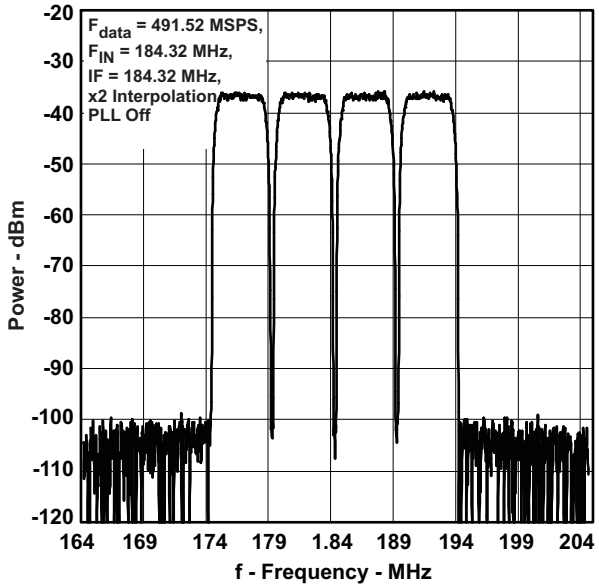


Figure 66. Four Carrier W-CDMA Test Model 1
Carrier Power: –16.3 dBm, ACLR: 66.7 dB

9 Power Supply Recommendations

TI recommends that the device be powered with the nominal supply voltages as indicated in the *Recommended Operating Conditions*.

In most instances the best performance is achieved with LDO supplies. However the supplies may be driven with direct outputs from a DC-DC switcher as long as the noise performance of the switcher is acceptable.

For an LDO power supply reference, it is best to refer to the SLAU236.

10 Layout

10.1 Layout Guidelines

The DAC5681Z EVM layout should be used as a reference for the layout to obtain the best performance. A sample layout is shown in *Layout Example*. Some important layout recommendations are the following:

- Use a single ground plane. Keep the digital and analog signals on distinct separate sections of the board. This may be virtually divided down the middle of the device package when doing placement and layout.
- Keep the analog outputs as far away from the switching clocks and digital signals as possible. This will keep coupling from the digital circuits to the analog outputs to a minimum.
- Decoupling caps should be kept close to the power pins of the device.

10.2 Layout Example

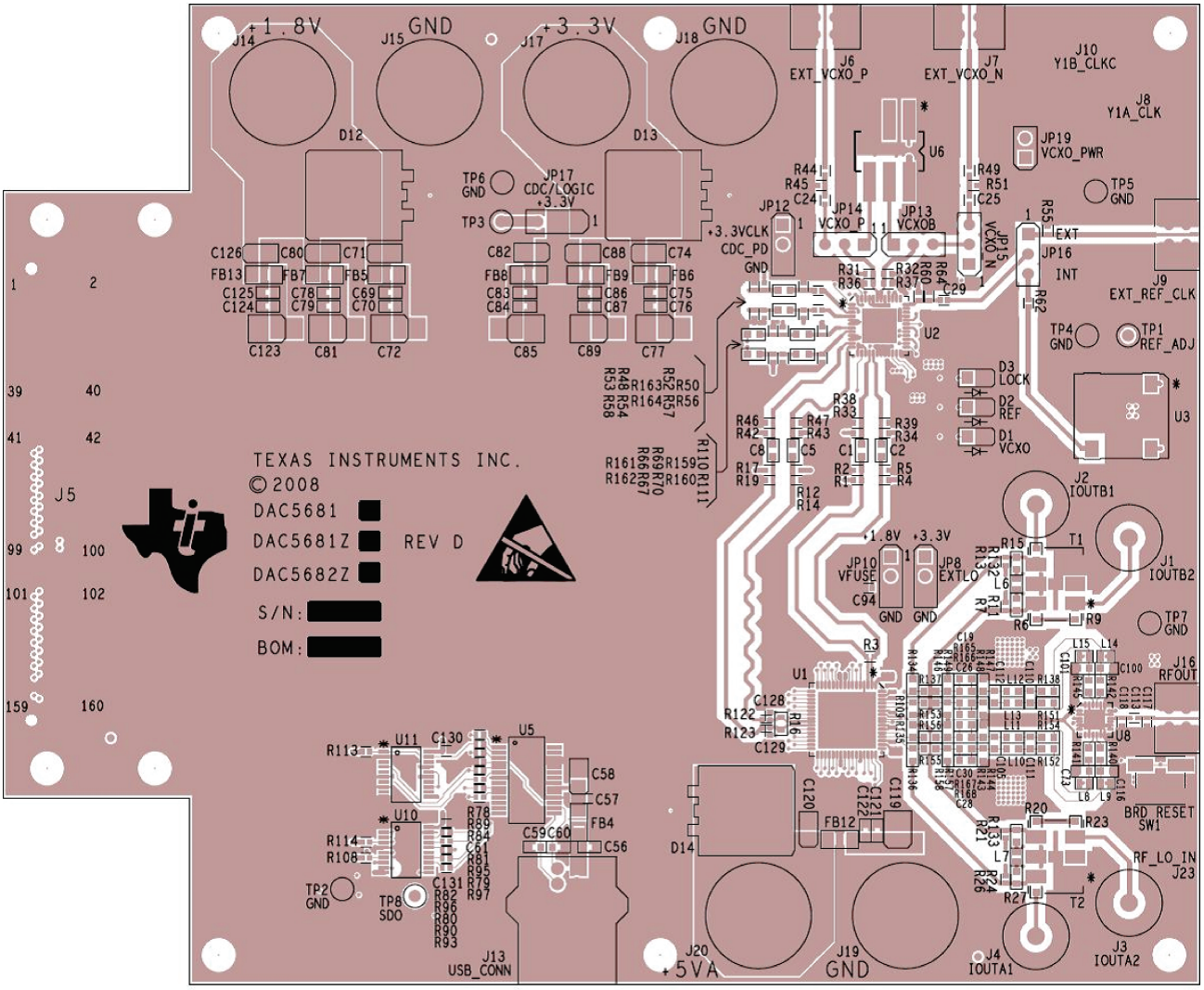


Figure 67. Top Layer of DAC5681Z EVM Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Device Nomenclature

11.1.2.1 Definition Of Specifications

Adjacent Carrier Leakage Ratio (ACLR): Defined for a 3.84-Mcps 3-GPP W-CDMA input signal measured in a 3.84-MHz bandwidth at a 5-MHz offset from the carrier with a 12-dB peak-to-average ratio.

Analog and Digital Power Supply Rejection Ratio (APSSR, DPSSR): Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

Differential Nonlinearity (DNL): Defined as the variation in analog output associated with an ideal 1 LSB change in the digital input code.

Gain Drift: Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Gain Error: Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

Integral Nonlinearity (INL): Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Intermodulation Distortion (IMD3, IMD): The two-tone IMD3 or four-tone IMD is defined as the ratio (in dBc) of the worst 3rd-order (or higher) intermodulation distortion product to either fundamental output tone.

Offset Drift: Defined as the maximum change in DC offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

Offset Error: Defined as the percentage error (in FSR%) for the ratio of the differential output current (IOUT1–IOUT2) and the mid-scale output current.

Output Compliance Range: Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result reduced reliability of the device or adversely affecting distortion performance.

Reference Voltage Drift: Defined as the maximum change of the reference voltage in ppm per degree Celsius from value at ambient (25°C) to values over the full operating temperature range.

Spurious Free Dynamic Range (SFDR): Defined as the difference (in dBc) between the peak amplitude of the output signal and the peak spurious signal.

Signal to Noise Ratio (SNR): Defined as the ratio of the RMS value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and DC.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

DAC5681/81z/82z EVM User's Guide, SLAU236

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC5681ZIRGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	DAC5681ZI	Samples
DAC5681ZIRGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	DAC5681ZI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

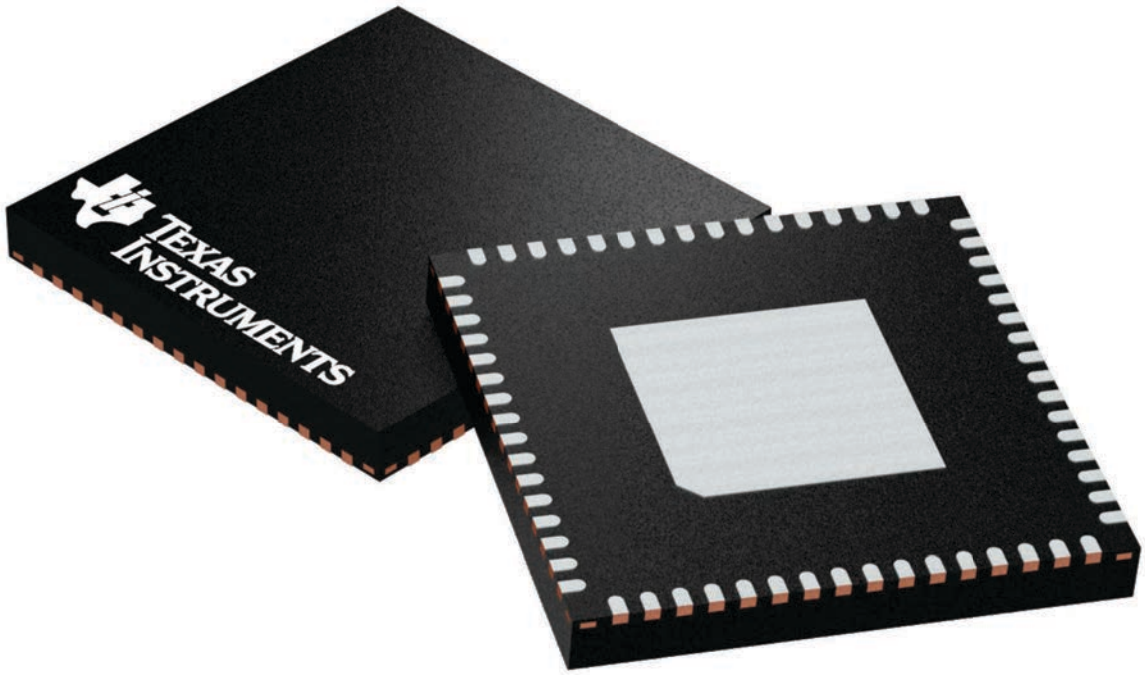
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

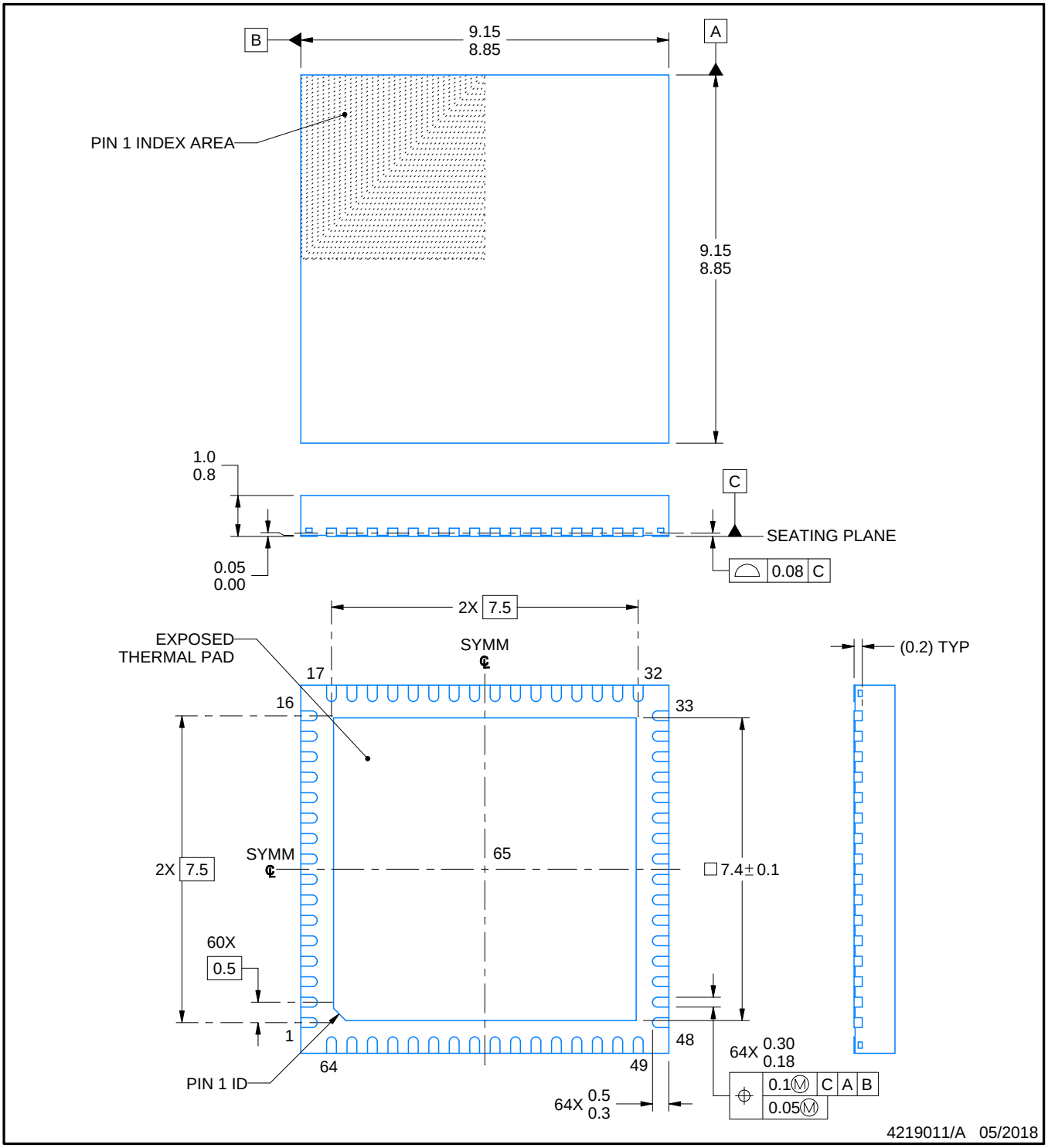
4224597/A

RGC0064H

PACKAGE OUTLINE

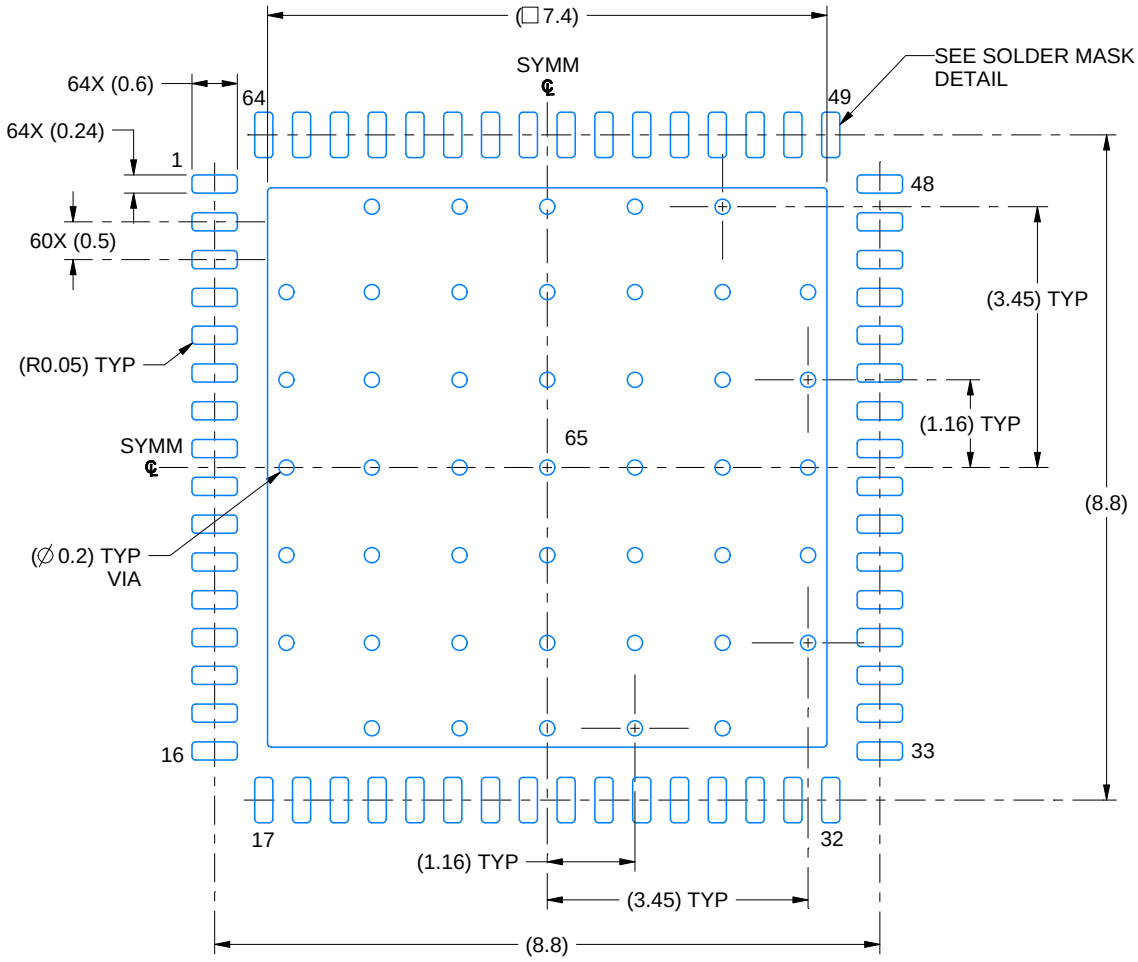
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

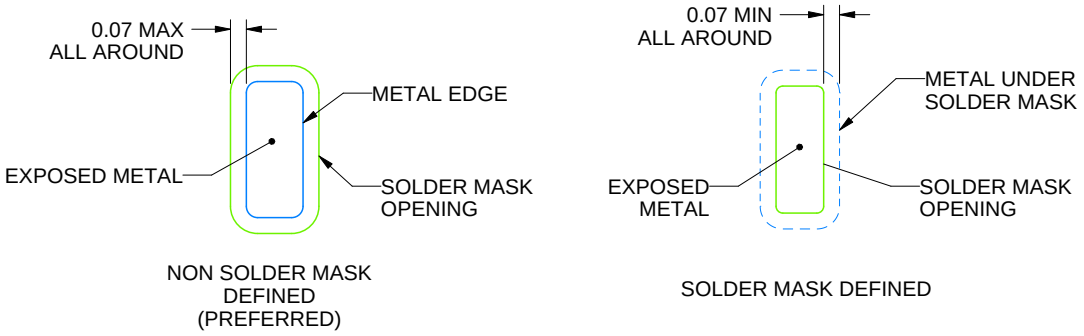


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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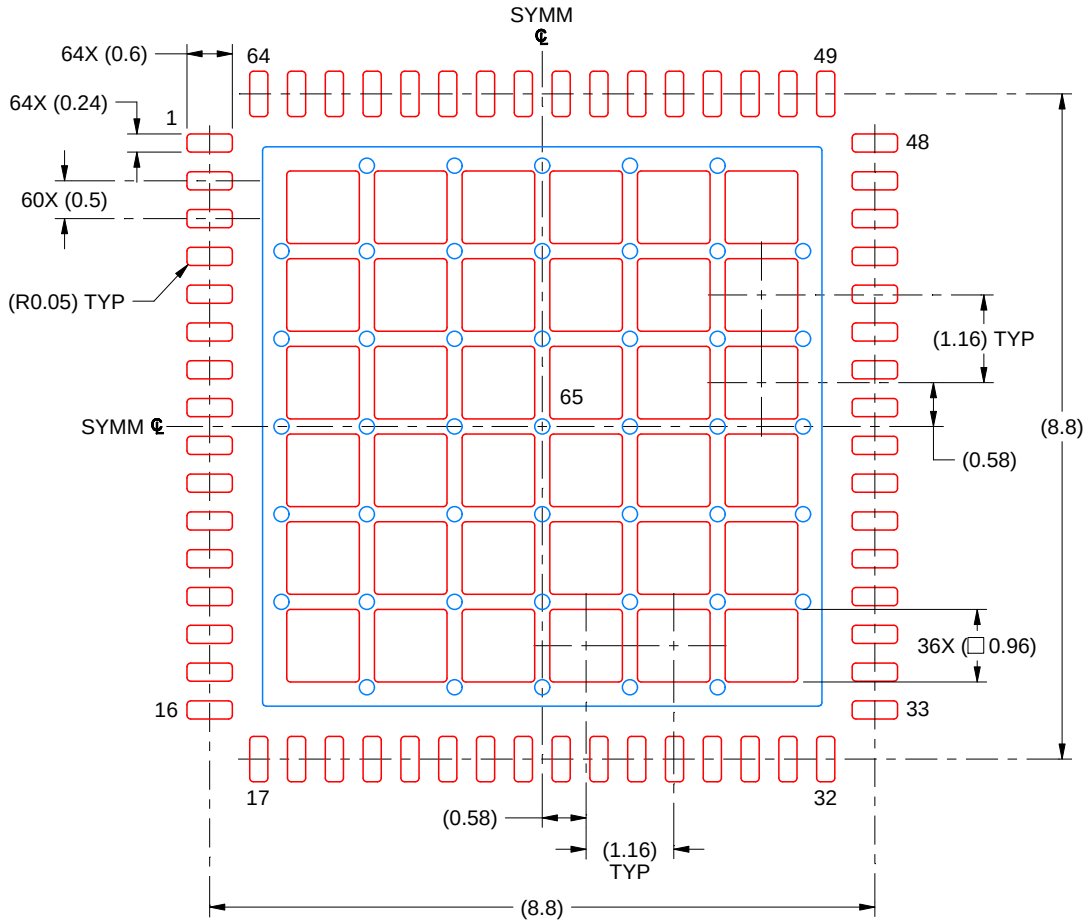
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219011/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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