DS26C32AMQML Quad Differential Line Receiver

Check for Samples: DS26C32AMQML

FEATURES

- **CMOS Design for Low Power**
- **±0.2V Sensitivity Over Input Common Mode Voltage Range**
- **Input Fail-Safe Circuitry**
- **Inputs Won't Load Line When V_{CC} = 0V**
- **Meets the Requirements of EIA Standard RS-422**
- **TRI-STATE Outputs for Connection to System Buses**

DESCRIPTION

The DS26C32A is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

The DS26C32A has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. The DS26C32A features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

The DS26C32A provides an enable and disable function common to all four receivers, and features TRI-STATE outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

CONNECTION DIAGRAMS

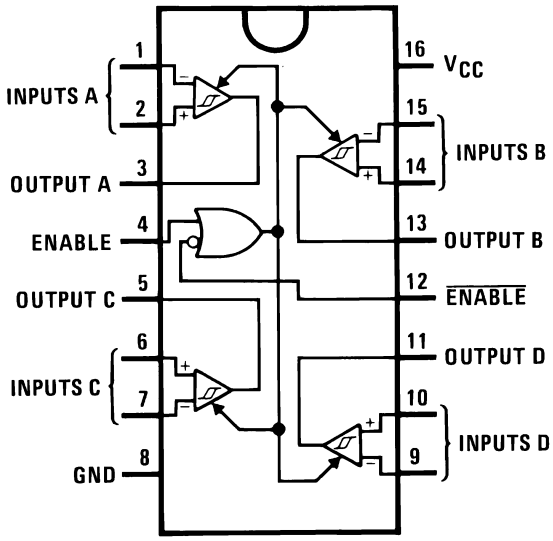

Figure 1. CDIP and CLGA Packages-Top View
See Package Numbers NFE0016A, NAC0016A, or NAD0016A

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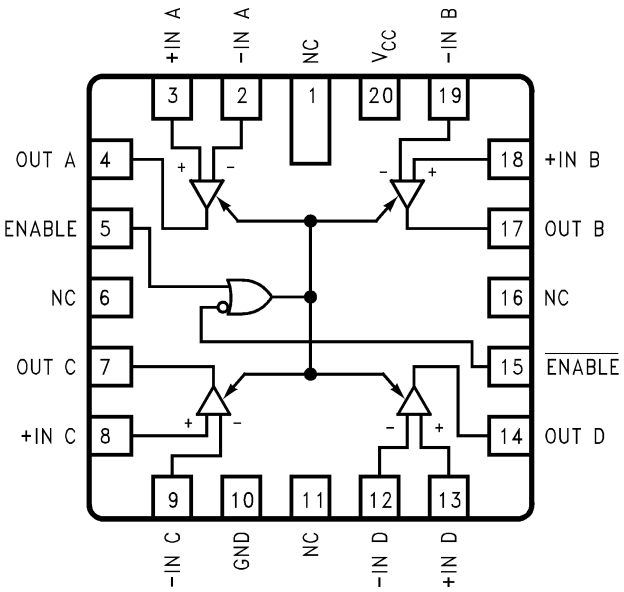
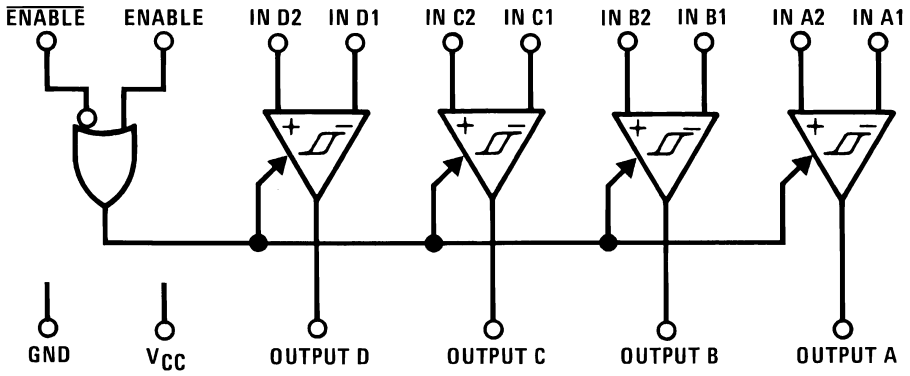


Figure 2. 20-Lead LCCC Package-Top View
See Package Number NAJ0020A

Logic Diagram



Truth Table (1)

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
L	H	X	Z
All Other Combinations of Enable Inputs		$V_{ID} \geq V_{Th}$ (Max)	H
		$V_{ID} \leq V_{Th}$ (Min)	L
		Open	H

(1) Z = TRI-STATE

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{Diff})	±14V
Enable Input Voltage (V_I)	7V
Storage Temperature Range (T_{Stg})	−65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering 4 sec.)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not verify specific performance limits. For verified specifications and test conditions, see the Electrical Characteristics. The verified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Unless otherwise specified, all voltages are referenced to ground.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)	−55	+125	°C

Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

DS26C32AM Electrical Characteristics DC Parameters

Parameter		Test Conditions	Notes	Min	Max	Unit	Sub-groups
V_{TH}	Minimum Differential Input Voltage	V_{CC} = 5V, V_O = V_{OH} or V_{OL}, -7 < V_{CM} < +7		-200	+200	mV	1, 2, 3
R_I	Input Resistance	V_{CC} = 5V, -7 < V_{CM} < +7, One input AC Gnd		4.5	11	KΩ	1, 2, 3
I_I	Input Current	V_{CC} = 5V, V_I = +10V, Other Input = Gnd			+1.8	mA	1, 2, 3
		V_{CC} = 5V, V_I = -10V, Other Input = Gnd			-2.7	mA	1, 2, 3
V_{OH}	Logical "1" Output Voltage	V_{CC} = 4.5V, V_{Diff} = +1V, I_O = -6.0mA		3.8		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage	V_{CC} = 5.5V, V_{CC} = Max, V_{Diff} = -1V, I_O = 6.0mA			0.3	V	1, 2, 3

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DS26C32AM Electrical Characteristics DC Parameters (continued)

Parameter		Test Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IH}	Minimum Enable High Level Voltage		(1)	2.0		V	1, 2, 3
V_{IL}	Maximum Enable Low Level Voltage		(1)		0.8	V	1, 2, 3
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_O = V_{CC}$ or Gnd, Enable = V_{IL}, $\overline{\text{Enable}} = V_{IH}$			±5.0	µA	1, 2, 3
I_I	Maximum Enable Input Current	$V_I = V_{CC}$ or Gnd			±1.0	µA	1, 2, 3
I_{CC}	Quiescent Power Supply Current	V_{Diff} = +1V, V_{CC} = 5.5V			25	mA	1, 2, 3

(1) Parameter tested Go-No-Go only.

DS26C32AM Electrical Characteristics AC Parameters - Propagation Delay Time

The following conditions apply, unless otherwise specified. V_{CC} = 5V ±10%, C_{CL} = 50pF, V_{Diff} = 2.5V

Parameter		Test Conditions	Notes	Min	Max	Unit	Sub-groups
t_{PLH}	Input to Output Prop Delay	V_{CM} = 0V			35	ns	9, 10, 11
t_{PHL}	Input to Output Prop Delay	V_{CM} = 0V			35	ns	9, 10, 11
t_{Rise}	Output Rise Time	V_{CM} = 0V			9	ns	9, 10, 11
t_{Fall}	Output Fall Time	V_{CM} = 0V			9	ns	9, 10, 11
t_{PLZ}	Output Disable Time	R_L = 1000Ω			29	ns	9, 10, 11
t_{PZL}	Output Enable Time	R_L = 1000Ω			29	ns	9, 10, 11
t_{PHZ}	Output Disable Time	R_L = 1000Ω			29	ns	9, 10, 11
t_{PZH}	Output Enable Time	R_L = 1000Ω			29	ns	9, 10, 11

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Typical Performance Characteristics

Differential Propagation Delay vs Temperature

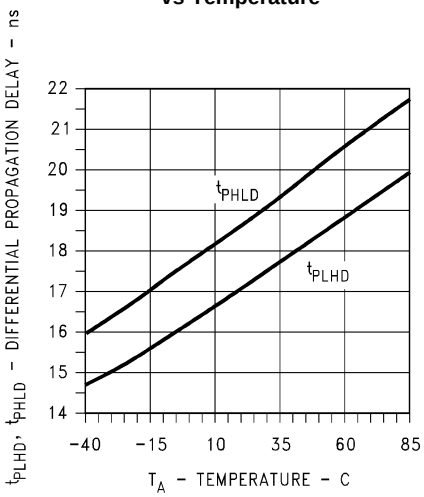

Figure 3.

Differential Propagation Delay vs Power Supply Voltage

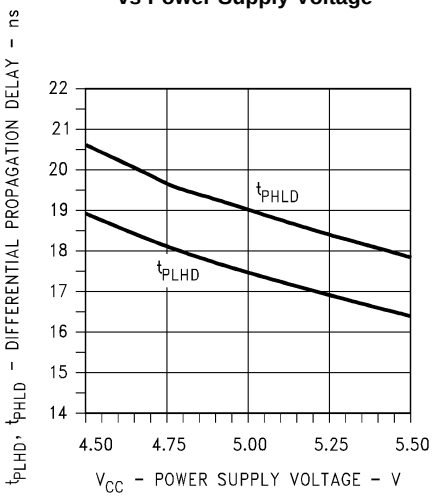

Figure 4.

Differential Skew vs Temperature

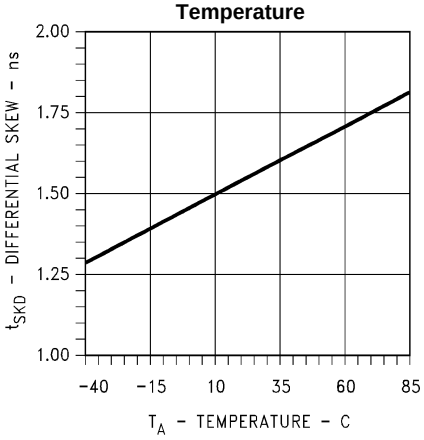

Figure 5.

Differential Skew vs Power Supply Voltage

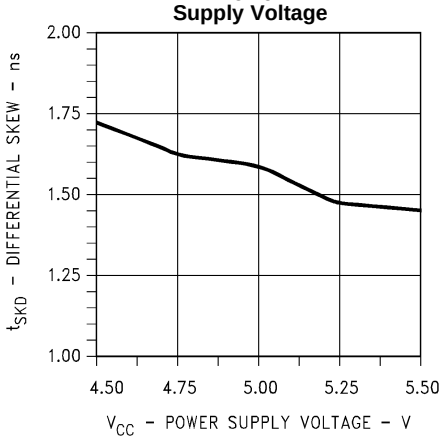

Figure 6.

Output High Voltage vs Output High Current

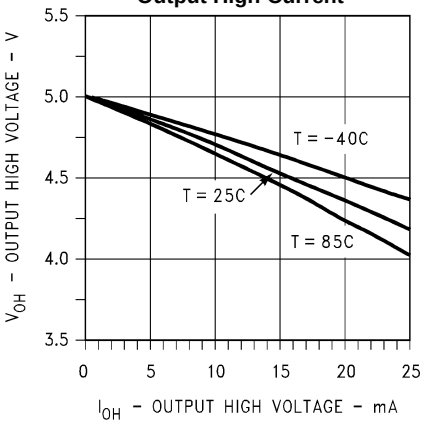

Figure 7.

Output High Voltage vs Output High Current

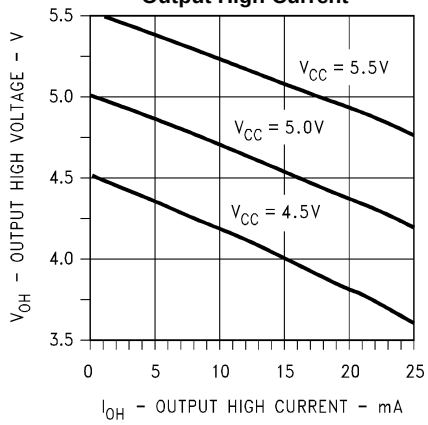

Figure 8.

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Typical Performance Characteristics (continued)

Output Low Voltage vs Output Low Current

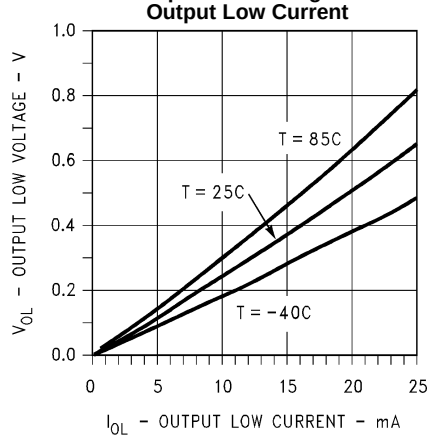

Figure 9.

Output Low Voltage vs Output Low Current

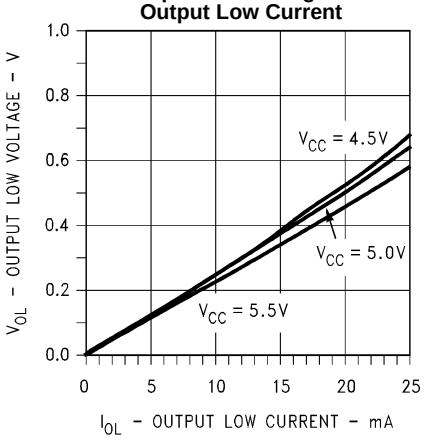

Figure 10.

Input Resistance vs Input Voltage

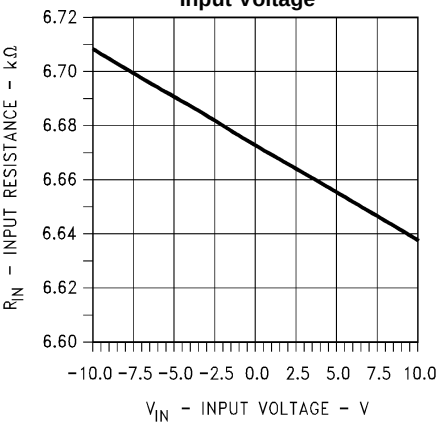

Figure 11.

Input Current vs Power Supply Voltage

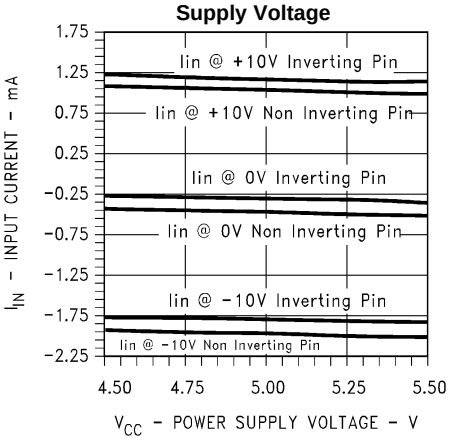

Figure 12.

Hysteresis & Differential Transition Voltage vs Temperature

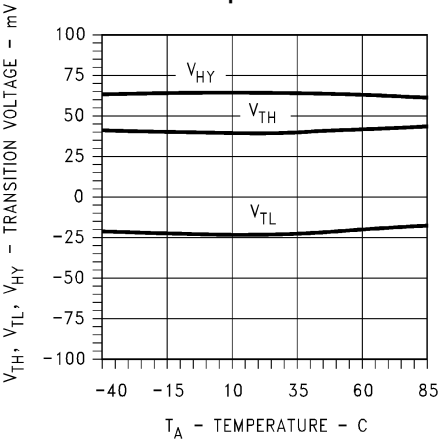

Figure 13.

Hysteresis & Differential Transition Voltage vs Power Supply Voltage

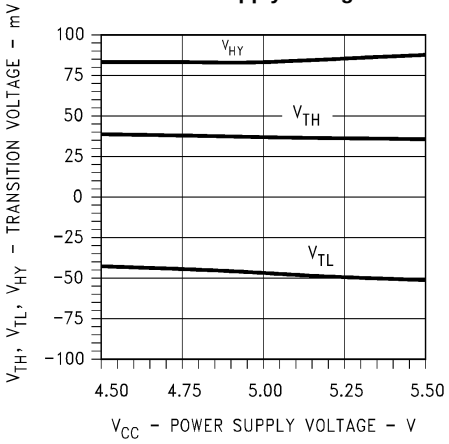

Figure 14.

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Typical Performance Characteristics (continued)

Supply Current vs Temperature

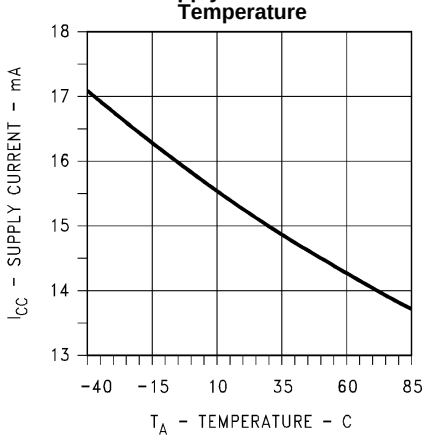


Figure 15.

Disabled Supply Current vs Power Supply Voltage

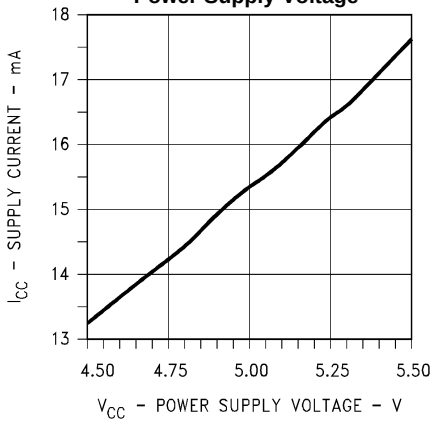


Figure 16.

Supply Current vs Data Rate

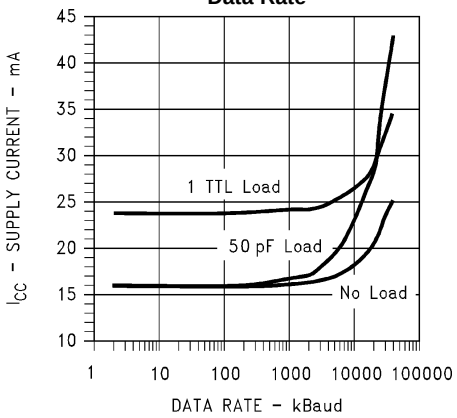
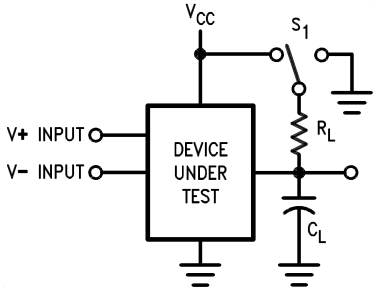


Figure 17.

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS



C_L includes load and test jig capacitance.
$S_1 = V_{CC}$ for t_{PZL}, and t_{PLZ} measurements.
S_1 = Gnd for t_{PZH}, and t_{PHZ} measurements.

Figure 18. Test Circuit for TRI-STATE Output Tests

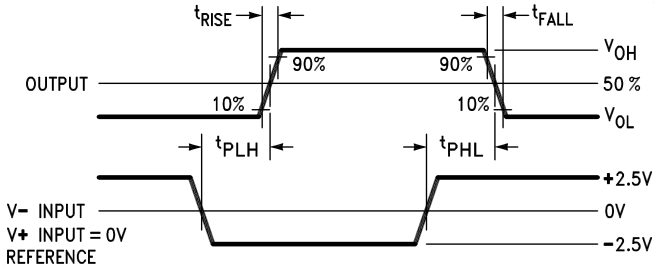


Figure 19. Propagation Delay

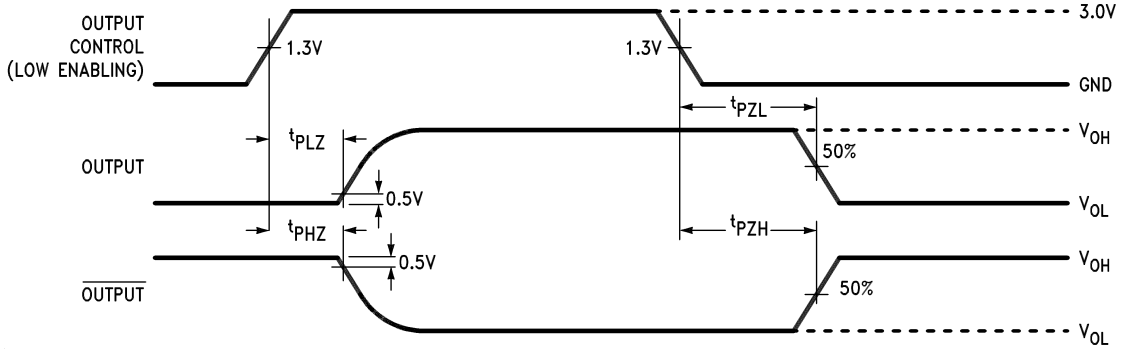
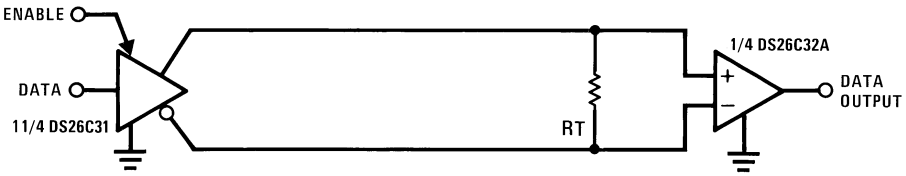


Figure 20. TRI-STATE Output Enable and Disable Waveforms

TYPICAL APPLICATIONS

Figure 21. Two-Wire Balanced Systems, RS-422



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REVISION HISTORY

Released	Revision	Section	Changes
10/26/2010	*	New Release, Corporate format	MDS data sheets converted into one Corp. data sheet format. MNDS26C32AM-X Rev 0B0 will be archived.
4/15/2013	A		Changed layout of National Data Sheet to TI format

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9164001M2A	ACTIVE	LCCC	NAJ	20	50	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C32AME /883 Q 5962-91640 01M2A ACO 01M2A >T	Samples
5962-9164001MEA	ACTIVE	CDIP	NFE	16	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C32AMJ/883 5962-9164001MEA Q	Samples
5962-9164001MFA	ACTIVE	CFP	NAD	16	19	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C32AMW /883 Q 5962-91640 01MFA ACO 01MFA >T	Samples
5962-9164001MXA	ACTIVE	CFP	NAC	16	88	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C32AMWG /883 Q 5962-91640 01MXA ACO 01MXA >T	Samples
DS26C32A MD8	ACTIVE	DIESALE	Y	0	100	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
DS26C32AME/883	ACTIVE	LCCC	NAJ	20	50	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C32AME /883 Q 5962-91640 01M2A ACO 01M2A >T	Samples
DS26C32AMJ/883	ACTIVE	CDIP	NFE	16	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C32AMJ/883 5962-9164001MEA Q	Samples
DS26C32AMW/883	ACTIVE	CFP	NAD	16	19	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C32AMW /883 Q 5962-91640 01MFA ACO 01MFA >T	Samples
DS26C32AMWG/883	ACTIVE	CFP	NAC	16	88	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C32AMWG /883 Q 5962-91640 01MXA ACO 01MXA >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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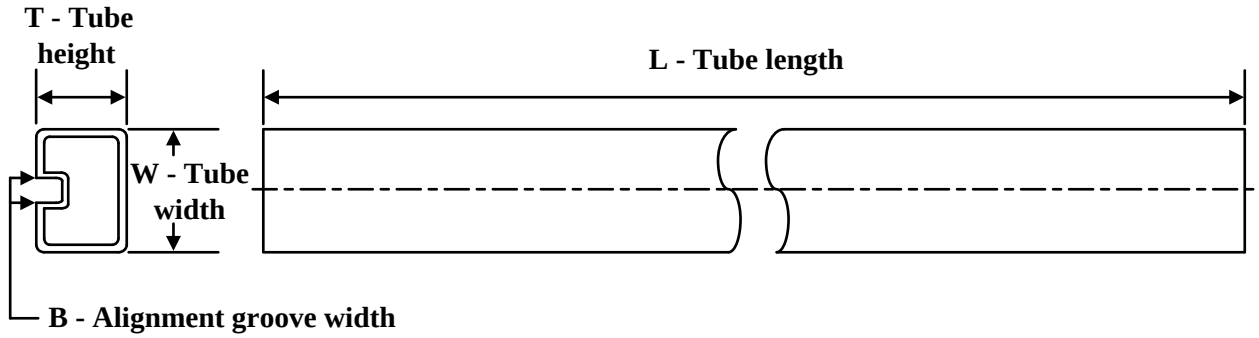
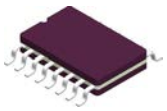
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9164001M2A	NAJ	LCCC	20	50	470	11	3810	0
5962-9164001MEA	NFE	CDIP	16	25	506.98	15.24	13440	NA
5962-9164001MFA	NAD	CFP	16	19	502	23	9398	9.78
DS26C32AME/883	NAJ	LCCC	20	50	470	11	3810	0
DS26C32AMJ/883	NFE	CDIP	16	25	506.98	15.24	13440	NA
DS26C32AMW/883	NAD	CFP	16	19	502	23	9398	9.78

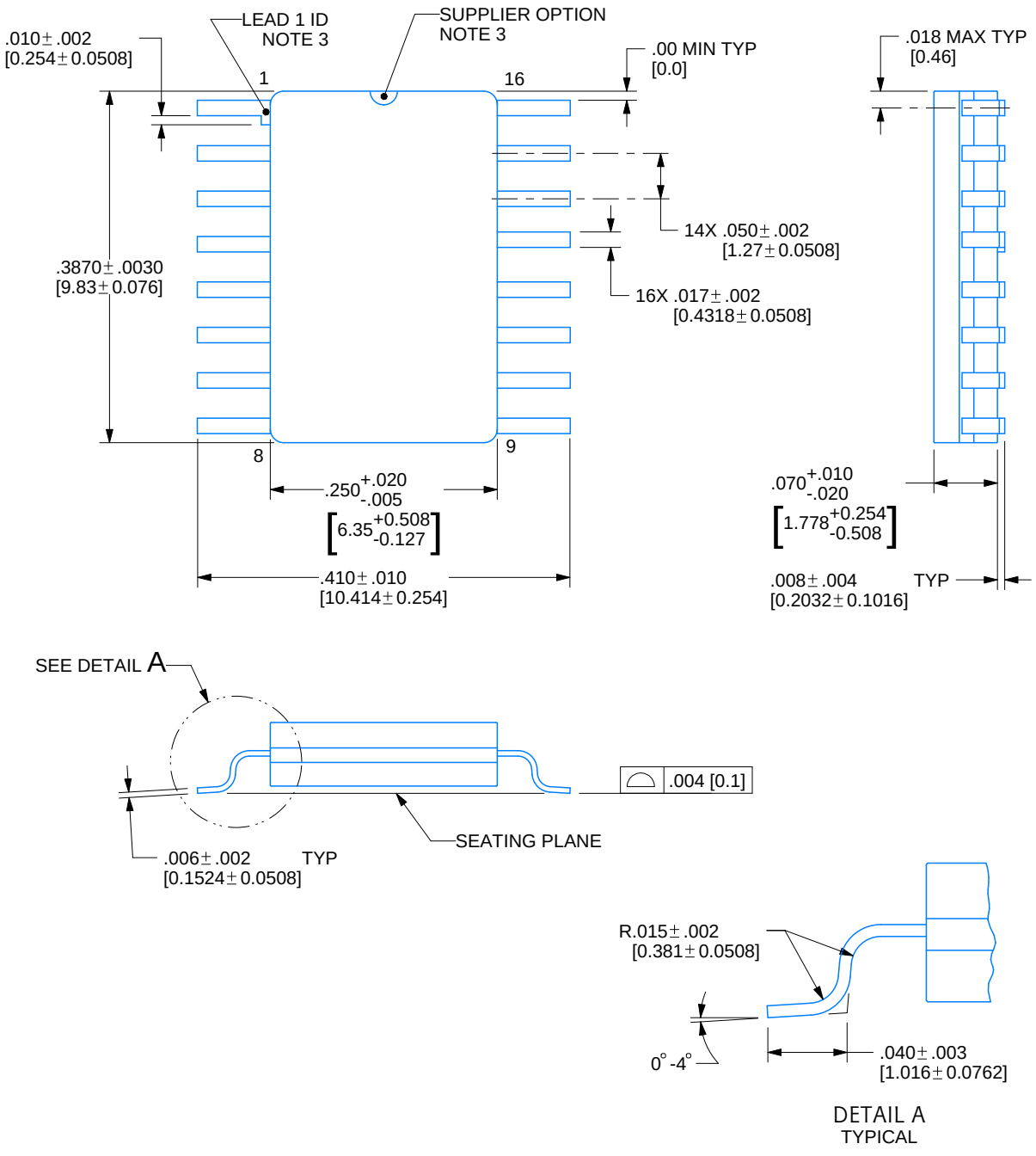


PACKAGE OUTLINE

NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



4215198/C 08/2022

NOTES:

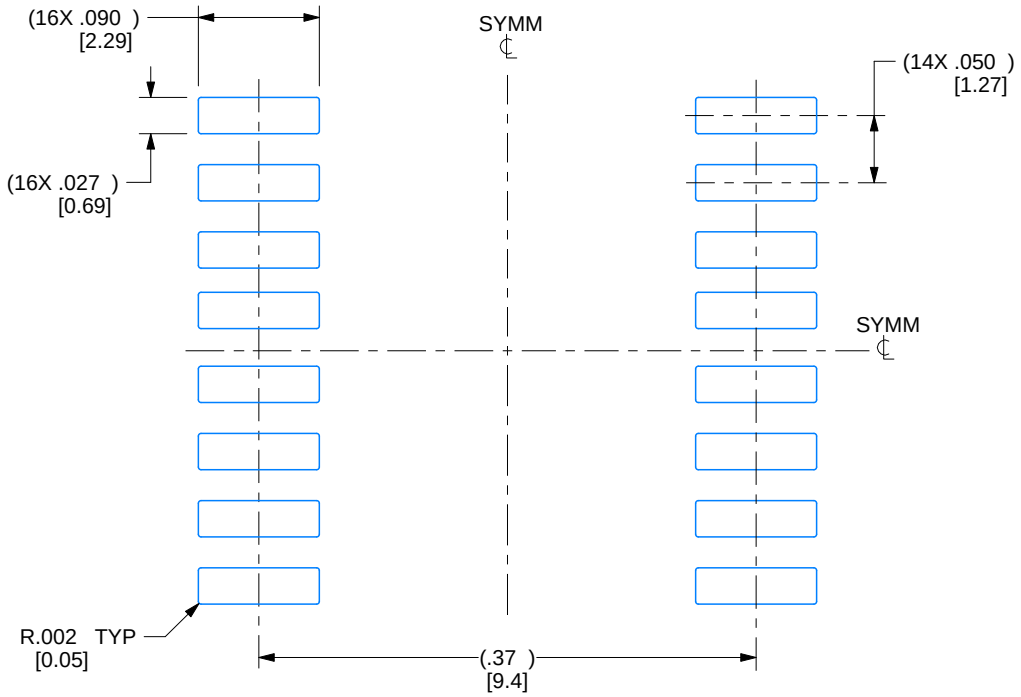
1. Controlling dimension is Inch. Values in [ ] are milimeters. Dimensions in ( ) for reference only.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

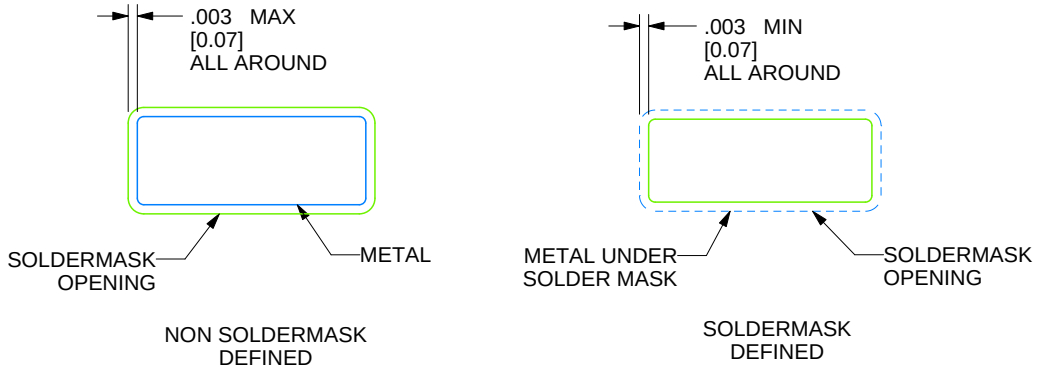
NAC0016A

CFP - 2.33mm max height

CERAMIC FLATPACK



RECOMMENDED LAND PATTERN

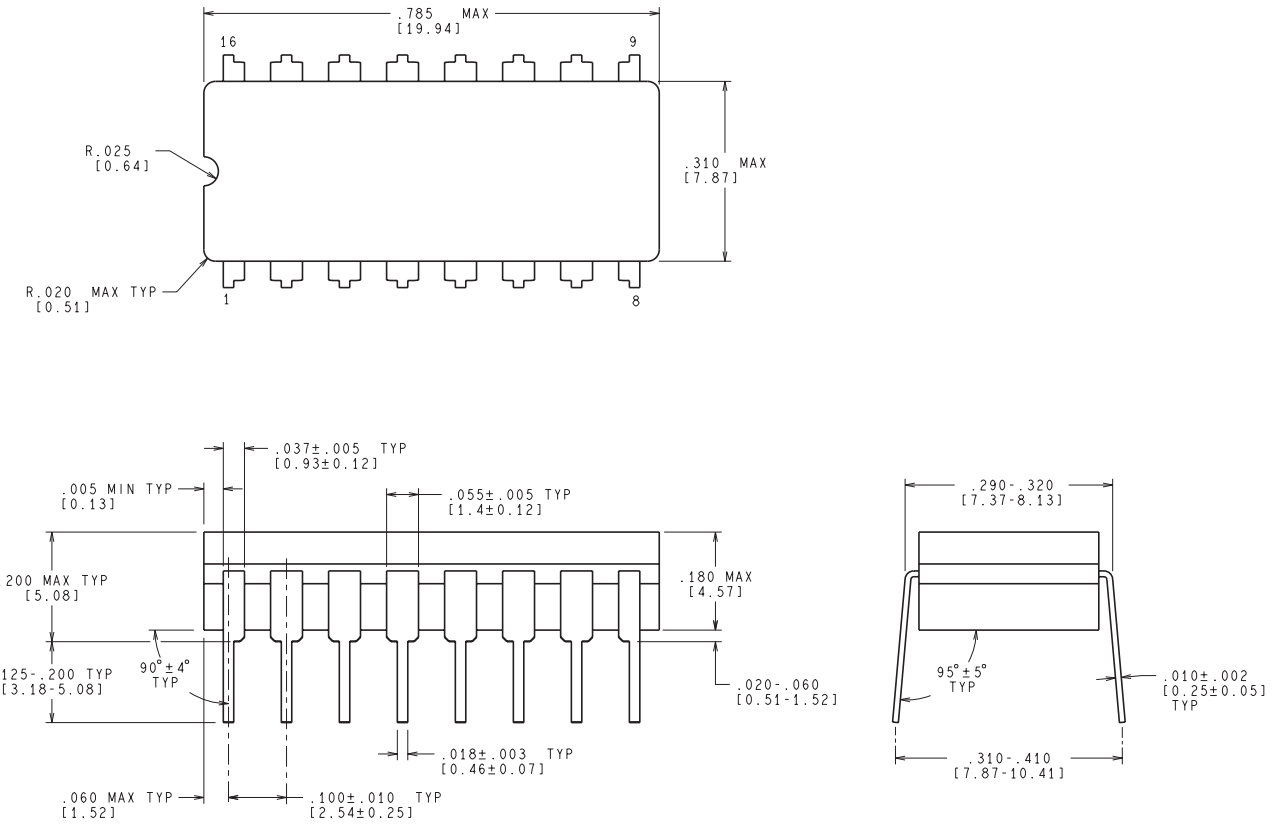


4215198/C 08/2022

REVISIONS

REV	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	2197879	12/30/2021	TINA TRAN / ANIS FAUZI
B	NO CHANGE TO DRAWING; REVISION FOR YODA RELEASE;	2198832	02/15/2022	K. SINCERBOX
C	.387± .003 WAS .39000± .00012;	2200917	08/08/2022	D. CHIN / K. SINCERBOX

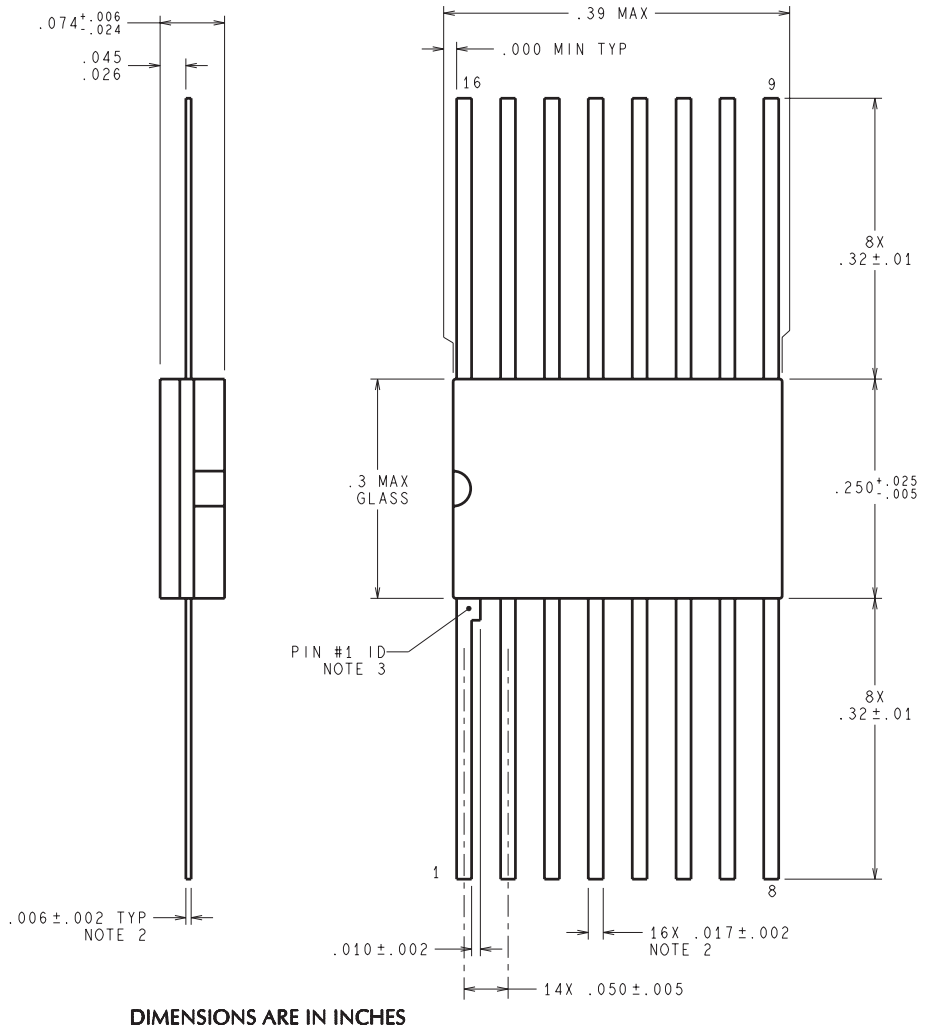
NFE0016A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

J16A (REV L)

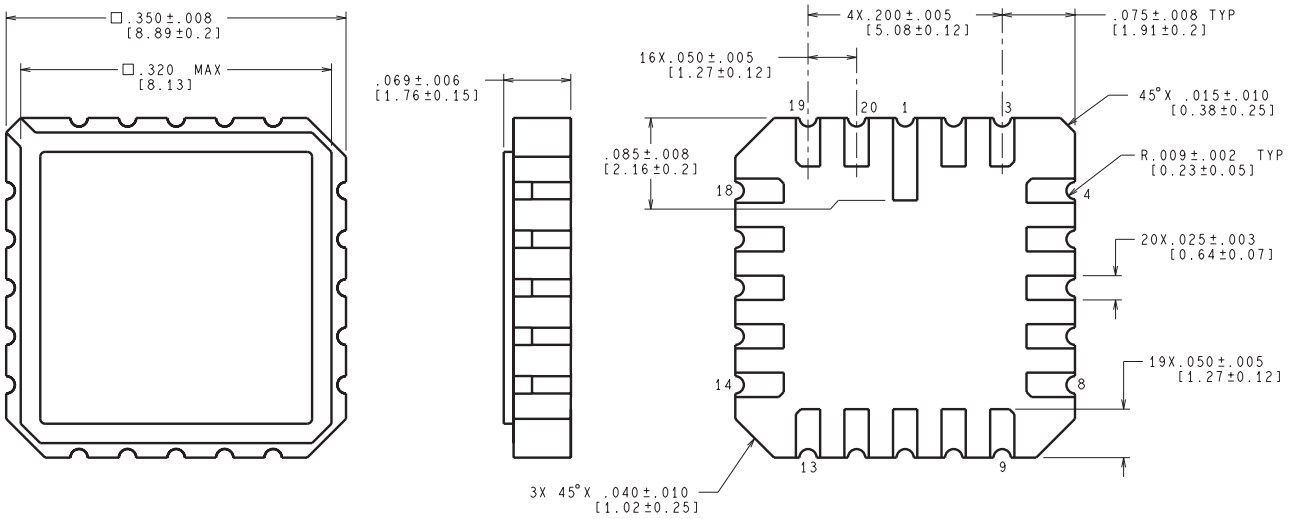
NAD0016A



DIMENSIONS ARE IN INCHES

W16A (Rev T)

NAJ0020A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

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