DS26LS31C/DS26LS31M Quad High Speed Differential Line Driver

Check for Samples: DS26LS31C, DS26LS31M

FEATURES

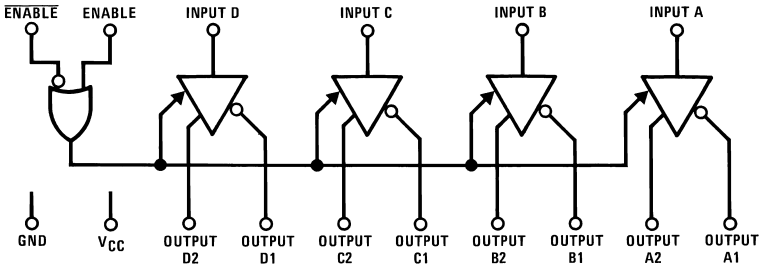
- **Output Skew—2.0 ns Typical**
- **Input to output delay—10 ns Typical**
- **Operation from Single 5V Supply**
- **Outputs Won't Load Line when V_{CC} = 0V**
- **Four Line Drivers in One Package for Maximum Package Density**
- **Output Short-Circuit Protection**
- **Complementary Outputs**
- **Meets the Requirements of EIA Standard RS-422**
- **Pin Compatible with AM26LS31**
- **Available in Military and Commercial Temperature Range**

DESCRIPTION

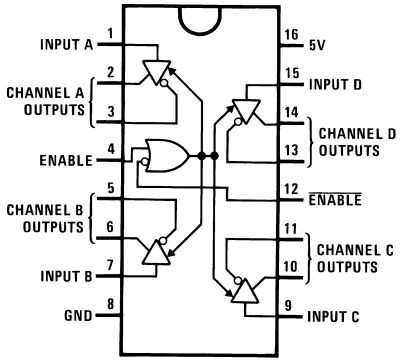
The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE outputs and logically ANDed complementary outputs. The inputs are all LS compatible and are all one unit load.

Logic and Connection Diagrams



Top View



For Complete Military Product Specifications, refer to the appropriate SMD or MDS.

Figure 1. PDIP Package
See Package D0016A or NFG0016E
See Package Numbers NAJ0020A, NFE0016A or NAD0016A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	5.5V
Output Voltage (Power OFF)	−0.25 to 6V
Maximum Power Dissipation (3) at 25°C	
Cavity Package	1509 mW
NFG0016E Package	1476 mW
D0016A Package	1051 mW

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics provide conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.9 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS26LS31M	4.5	5.5	V
DS26LS31	4.75	5.25	V
Temperature, T_A			
DS26LS31M	−55	+125	°C
DS26LS31	0	+70	°C

Electrical Characteristics(1)(2)(3)

Parameter		Test Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	I_{OH} = −20 mA	2.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20 mA			0.5	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.4V		−40	−200	μA
I_{IH}	Input High Current	V_{IN} = 2.7V			20	μA
I_I	Input Reverse Current	V_{IN} = 7V			0.1	mA
I_O	TRI-STATE Output Current	V_O = 2.5V			20	μA
		V_O = 0.5V			−20	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.5	V
I_{SC}	Output Short-Circuit Current		−30		−150	mA
I_{CC}	Power Supply Current	All Outputs Disabled or Active		35	60	mA

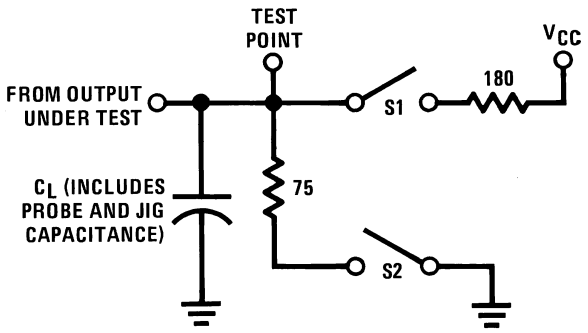
(1) Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS726LS31M and across the 0°C to +70°C range for the DS26LS31. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.
(3) Only one output at a time should be shorted.

Switching Characteristics

V_{CC} = 5V, T_A = 25°C

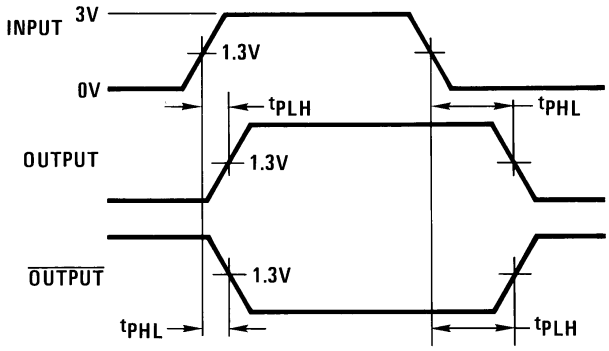
Parameter		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Input to Output	C_L = 30 pF		10	15	ns
t_{PHL}	Input to Output	C_L = 30 pF		10	15	ns
Skew	Output to Output	C_L = 30 pF		2.0	6.0	ns
t_{LZ}	Enable to Output	C_L = 10 pF, S2 Open		15	35	ns
t_{HZ}	Enable to Output	C_L = 10 pF, S1 Open		15	25	ns
t_{ZL}	Enable to Output	C_L = 30 pF, S2 Open		20	30	ns
t_{ZH}	Enable to Output	C_L = 30 pF, S1 Open		20	30	ns

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS



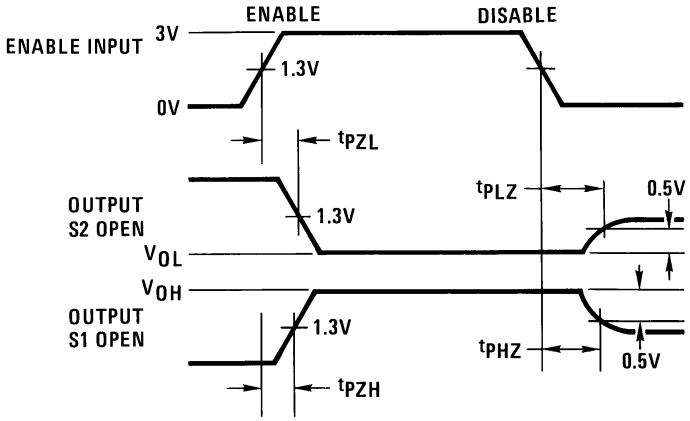
S1 and S2 of load circuit are closed except where shown.

Figure 2. AC Test Circuit



f = 1 MHz, $t_r \leq 15$ ns, $t_f \leq 6$ ns

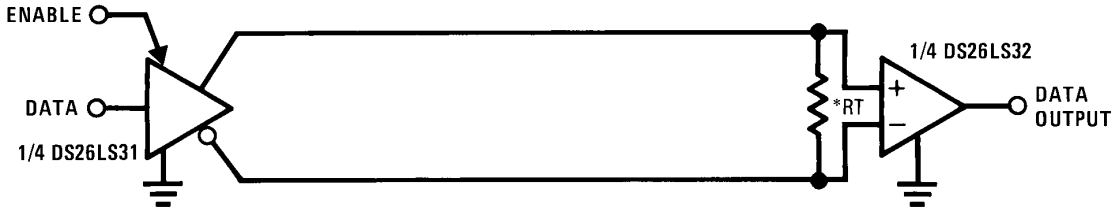
Figure 3. Propagation Delays



f = 1 MHz, $t_r \leq 15$ ns, $t_f \leq 6$ ns

Figure 4. Enable and Disable Times

TYPICAL APPLICATIONS



R_T is optional although highly recommended to reduce reflection.

Figure 5. Two-Wire Balanced System, RS-422

Typical Performance Characteristics

DS26LS31CN Unloaded I_C vs Frequency vs T_A

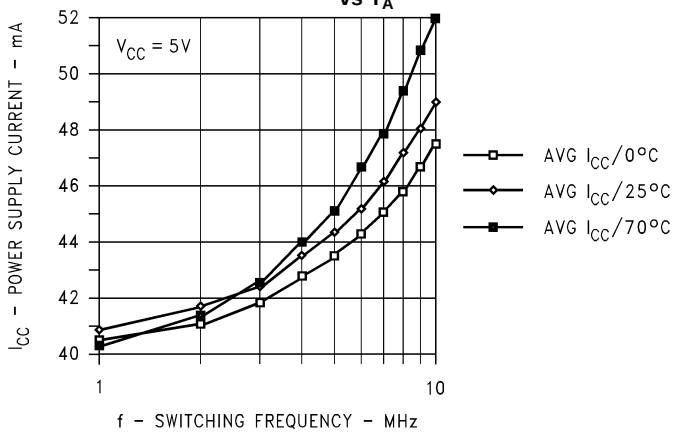


Figure 6.

DS26LS31 I_{CC} vs V_{CC} vs T_A

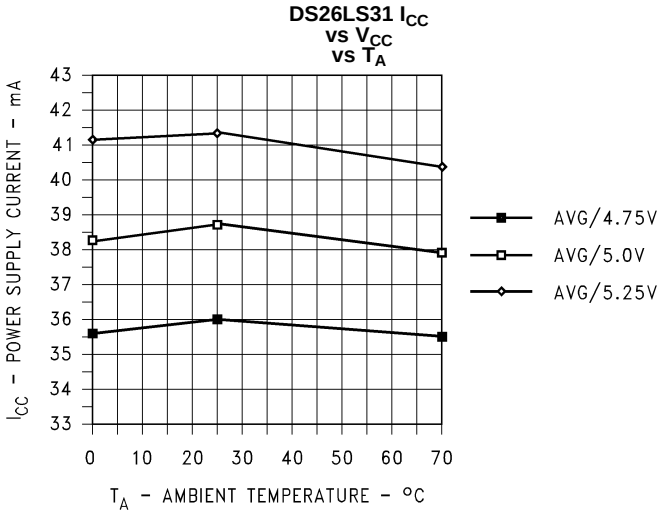


Figure 7.

DS26LS31CN V_{OH} vs I_{OH} vs T_A

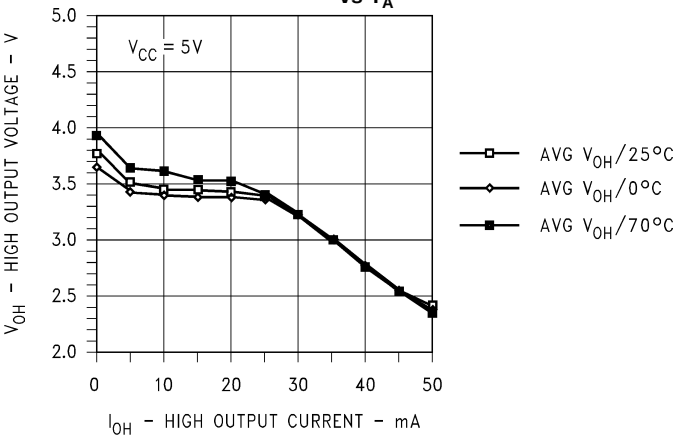


Figure 8.

DS26LS31CN V_{OL} vs I_{OL} vs T_A

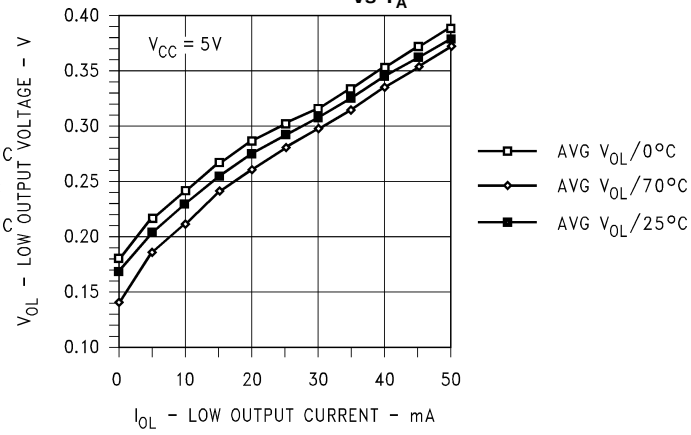


Figure 9.

DS26LS31CN V_{OD} vs I_O vs T_A

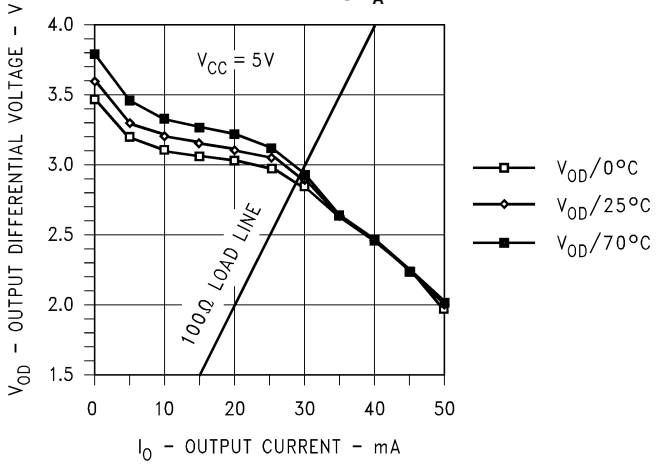
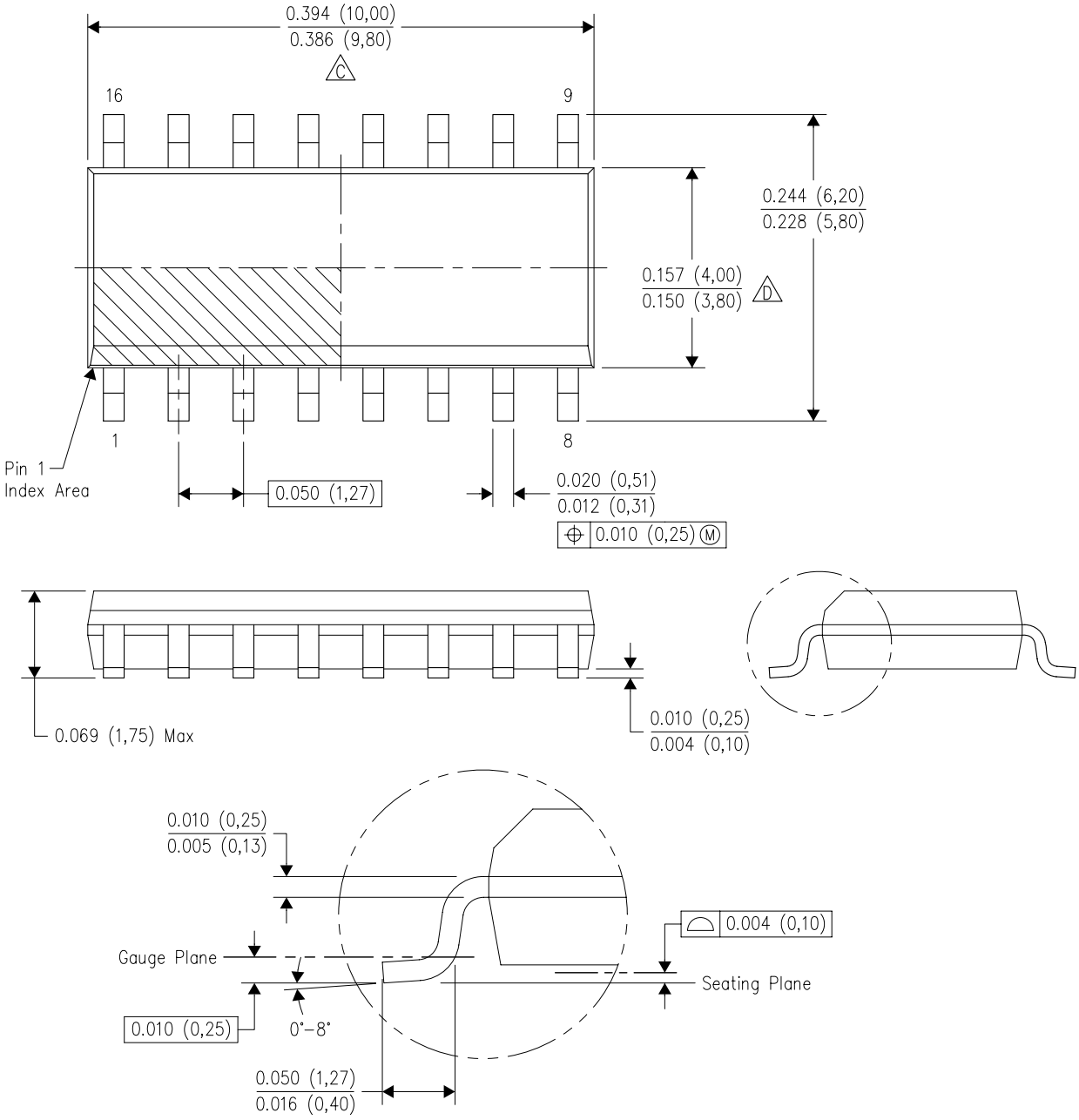


Figure 10.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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