TEXAS INSTRUMENTS

LF198-N, LF298, LF398-N
LF198A-N, LF398A-N

SNOSBI3C – JULY 2000 – REVISED OCTOBER 2018

LFx98x Monolithic Sample-and-Hold Circuits

1 Features

- Operates from ±5-V to ±18-V Supplies
- Less than 10-μs Acquisition Time
- Logic Input Compatible With TTL, PMOS, CMOS
- 0.5-mV Typical Hold Step at Ch = 0.01 μF
- Low Input Offset
- 0.002% Gain Accuracy
- Low Output Noise in Hold Mode
- Input Characteristics Do Not Change During Hold Mode
- High Supply Rejection Ratio in Sample or Hold
- Wide Bandwidth
- Space Qualified, JM38510

2 Applications

- Ramp Generators With Variable Reset Level
- Integrators With Programmable Reset Level
- Synchronous Correlators
- 2-Channel Switches
- DC and AC Zeroing
- Staircase Generators

3 Description

The LFx98x devices are monolithic sample-and-hold circuits that use BI-FET technology to obtain ultrahigh DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity-gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6 μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LFx98x to be included inside the feedback loop of 1-MHz operational amplifiers without having stability problems. Input impedance of 10^{10} Ω allows high-source impedances to be used without degrading accuracy.

P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1-μF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design ensures no feedthrough from input to output in the hold mode, even for input signals equal to the supply voltages.

Logic inputs on the LFx98x are fully differential with low input current, allowing for direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4 V. The LFx98x will operate from ±5-V to ±18-V supplies.

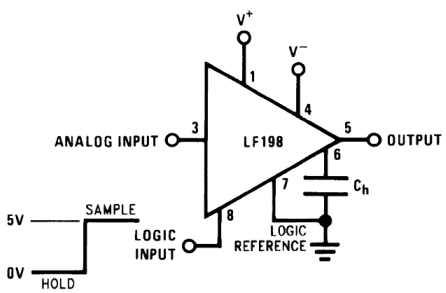
An A version is available with tightened electrical specifications.

Device Information(1)

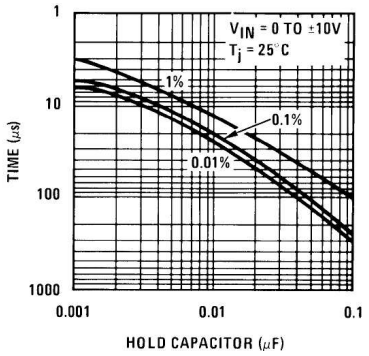
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LF298, LF398-N	SOIC (14)	8.65 mm × 3.91 mm
LFx98x	TO-99 (8)	9.08 mm × 9.08 mm
LF398-N	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Connection



Acquisition Time



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2015) to Revision C — **Page**

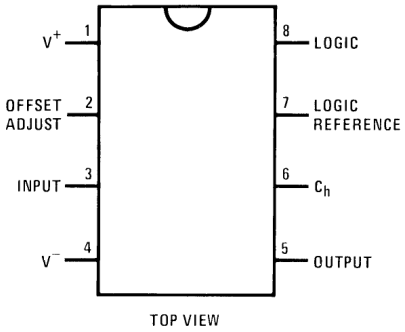
- Updated *Device Information* and *Pin Functions* tables ... 1
- Separated *Electrical Characteristics* into four tables: LF198-N and LF298; LF198A-N; LF398-N; and LF398A-N (OBSOLETE) ... 5

Changes from Revision A (July 2000) to Revision B — **Page**

- Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

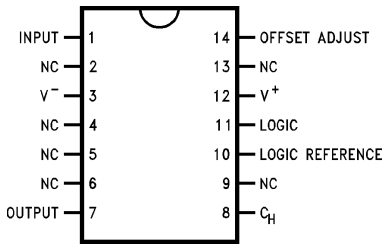
5 Pin Configuration and Functions

P Package
8-Pin PDIP
Top View

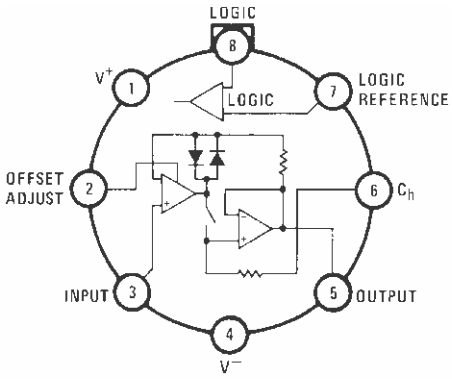


TOP VIEW

D Package
14-Pin SOIC
Top View



LMC Package
8-Pin TO-99
Top View



TOP VIEW

A military RETS electrical test specification is available on request. The LF198-N may also be procured to Standard Military Drawing #5962-8760801GA or to MIL-STD-38510 part ID JM38510/12501SGA.

Pin Functions

PIN				TYPE(1)	DESCRIPTION
NAME	LF298, LF398-N	LFx98x	LF398-N		
	SOIC-14	TO-99	PDIP-8		
V^+	12	1	1	P	Positive supply
OFFSET ADJUST	14	2	2	A	DC offset compensation pin
INPUT	1	3	3	A	Analog Input
V^-	3	4	4	P	Negative supply
OUTPUT	7	5	5	O	Output
C_h	8	6	6	A	Hold capacitor
LOGIC REFERENCE	10	7	7	I	Reference for LOGIC input
LOGIC	11	8	8	I	Logic input for Sample and Hold modes
NC	2, 4, 5, 6, 9, 13	—	—	NA	No connect

(1) P = Power, G = Ground, I = Input, O = Output, A = Analog

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage			±18	V
Power dissipation	(Package limitation, see (3))		500	mW
Operating ambient temperature	LF198-N, LF198A-N	–55	125	°C
	LF298	–25	85	°C
	LF398-N, LF398A-N	0	70	°C
Input voltage			±18	V
Logic-to-logic reference differential voltage (see (4))		7	−30	V
Output short circuit duration		Indefinite		
Hold capacitor short circuit duration			10	sec
Lead temperature	H package (soldering, 10 sec.)		260	°C
	N package (soldering, 10 sec.)		260	°C
	M package: vapor phase (60 sec.)		215	°C
	Infrared (15 sec.)		220	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A) / R_{\theta JA}$, or the number given in the Absolute Maximum Ratings, whichever is lower. The maximum junction temperature, T_{JMAX}, for the LF198-N and LF198A-N is 150°C; for the LF298, 115°C; and for the LF398-N and LF398A-N, 100°C.
(4) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2 V below the positive supply and 3 V above the negative supply.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply voltage			±15		V
T_J	Ambient temperature	LF198-N, LF198A-N	–55		125	°C
		LF298	–25		85	
		LF398-N, LF398A-N	0		70	

6.3 Thermal Information

THERMAL METRIC(1)		LF398-N	LF298, LF398-N	LFx98x	UNIT
		P (PDIP)	D (SOIC)	LMC (TO-99)	
		8 PINS	14 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.9	80.6	85(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.3	38.1	20	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.2	35.4	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.3	5.8	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.0	35.1	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Board mount in 400 LF/min air flow.

6.4 Electrical Characteristics, LF198-N and LF298

The following specifications apply for $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$, $+V_S = +15\ V$, $-V_S = -15\ V$, $T_A = T_J = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0 V, LOGIC HIGH = 2.5 V, LOGIC LOW = 0 V unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage(1)	$T_J = 25°C$		1	3	mV
	Full temperature range			5	mV
Input bias current(1)	$T_J = 25°C$		5	25	nA
	Full temperature range			75	nA
Input impedance	$T_J = 25°C$		10		GΩ
Gain error	$T_J = 25°C$, $R_L = 10\ k$		0.002%	0.005%	
	Full temperature range			0.02%	
Feedthrough attenuation ratio at 1 kHz	$T_J = 25°C$, $C_h = 0.01\ \mu F$	86	96		dB
Output impedance	$T_J = 25°C$, "HOLD" mode		0.5	2	Ω
	Full temperature range			4	Ω
HOLD step(2)	$T_J = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		0.5	2	mV
Supply current(1)	$T_J \ge 25°C$		4.5	5.5	mA
Logic and logic reference input current	$T_J = 25°C$		2	10	µA
Leakage current into hold capacitor(1)	$T_J = 25°C$, hold mode(3)		30	100	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10\ V$, $C_h = 1000\ pF$		4		µs
	$C_H = 0.01\ \mu F$		20		µs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2\ V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		dB
Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	V

(1) These parameters ensured over a supply voltage range of ±5 to ±18 V, and an input range of $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$.
(2) Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5-mV step with a 5-V logic swing and a 0.01-µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
(3) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

6.5 Electrical Characteristics, LF198A-N

The following specifications apply for $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$, $+V_S = +15\ V$, $-V_S = -15\ V$, $T_A = T_J = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0 V, LOGIC HIGH = 2.5 V, LOGIC LOW = 0 V unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage(1)	$T_J = 25°C$		1	1	mV
	Full temperature range			2	mV
Input bias current(1)	$T_J = 25°C$		5	25	nA
	Full temperature range			75	nA
Input impedance	$T_J = 25°C$		10		GΩ
Gain error	$T_J = 25°C$, $R_L = 10\ k$		0.002%	0.005%	
	Full temperature range			0.01%	
Feedthrough attenuation ratio at 1 kHz	$T_J = 25°C$, $C_h = 0.01\ \mu F$	86	96		dB
Output impedance	$T_J = 25°C$, "HOLD" mode		0.5	1	Ω
	Full temperature range			4	Ω
HOLD step(2)	$T_J = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		0.5	1	mV
Supply current(1)	$T_J \ge 25°C$		4.5	5.5	mA
Logic and logic reference input current	$T_J = 25°C$		2	10	µA
Leakage current into hold capacitor(1)	$T_J = 25°C$, hold mode(3)		30	100	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10\ V$, $C_h = 1000\ pF$		4	6	µs
	$C_H = 0.01\ \mu F$		20	25	µs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2\ V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	90	110		dB
Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	V

(1) These parameters ensured over a supply voltage range of ±5 to ±18 V, and an input range of $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$.
(2) Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5-mV step with a 5-V logic swing and a 0.01-µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
(3) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

6.6 Electrical Characteristics, LF398-N

The following specifications apply for $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$, $+V_S = +15\ V$, $-V_S = -15\ V$, $T_A = T_J = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0 V, LOGIC HIGH = 2.5 V, LOGIC LOW = 0 V unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage(1)	$T_J = 25°C$		2	7	mV
	Full temperature range			10	mV
Input bias current(1)	$T_J = 25°C$		10	50	nA
	Full temperature range			100	nA
Input impedance	$T_J = 25°C$		10		GΩ
Gain error	$T_J = 25°C$, $R_L = 10\ k$		0.004%	0.01%	
	Full temperature range			0.02%	
Feedthrough attenuation ratio at 1 kHz	$T_J = 25°C$, $C_h = 0.01\ \mu F$	80	90		dB
Output impedance	$T_J = 25°C$, "HOLD" mode		0.5	4	Ω
	Full temperature range			6	Ω
HOLD step(2)	$T_J = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		1	2.5	mV
Supply current(1)	$T_J \ge 25°C$		4.5	6.5	mA
Logic and logic reference input current	$T_J = 25°C$		2	10	µA
Leakage current into hold capacitor(1)	$T_J = 25°C$, hold mode(3)		30	200	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10\ V$, $C_h = 1000\ pF$		4		µs
	$C_H = 0.01\ \mu F$		20		µs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2\ V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		dB
Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	V

(1) These parameters ensured over a supply voltage range of ±5 to ±18 V, and an input range of $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$.
(2) Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5-mV step with a 5-V logic swing and a 0.01-µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
(3) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

6.7 Electrical Characteristics, LF398A-N (OBSOLETE)

The following specifications apply for $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$, $+V_S = +15\ V$, $-V_S = -15\ V$, $T_A = T_J = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0 V, LOGIC HIGH = 2.5 V, LOGIC LOW = 0 V unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage(1)	$T_J = 25°C$		2	2	mV
	Full temperature range			3	mV
Input bias current(1)	$T_J = 25°C$		10	25	nA
	Full temperature range			50	nA
Input impedance	$T_J = 25°C$		10		GΩ
Gain error	$T_J = 25°C$, $R_L = 10\ k$		0.004%	0.005%	
	Full temperature range			0.01%	
Feedthrough attenuation ratio at 1 kHz	$T_J = 25°C$, $C_h = 0.01\ \mu F$	86	90		dB
Output impedance	$T_J = 25°C$, "HOLD" mode		0.5	1	Ω
	Full temperature range			6	Ω
HOLD step(2)	$T_J = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		1	1	mV
Supply current(1)	$T_J \ge 25°C$		4.5	6.5	mA
Logic and logic reference input current	$T_J = 25°C$		2	10	µA
Leakage current into hold capacitor(1)	$T_J = 25°C$, hold mode(3)		30	100	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10\ V$, $C_h = 1000\ pF$		4	6	µs
	$C_H = 0.01\ \mu F$		20	25	µs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2\ V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	90	110		dB
Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	V

(1) These parameters ensured over a supply voltage range of ±5 to ±18 V, and an input range of $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$.
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(3) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

6.8 Typical Characteristics

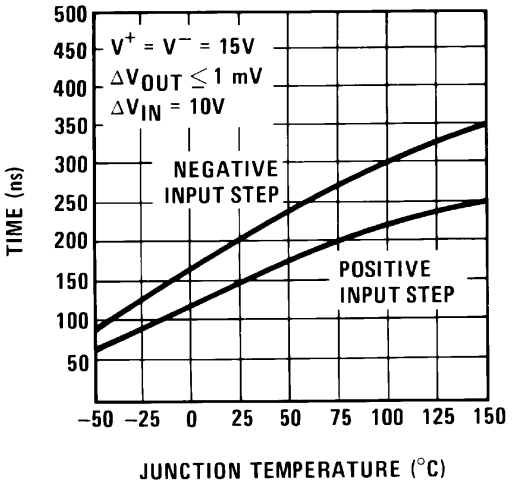


Figure 1. Aperture Time

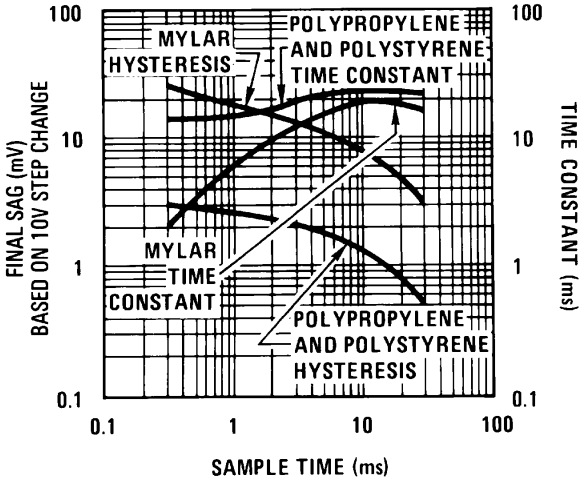


Figure 2. Dielectric Absorption Error in Hold Capacitor

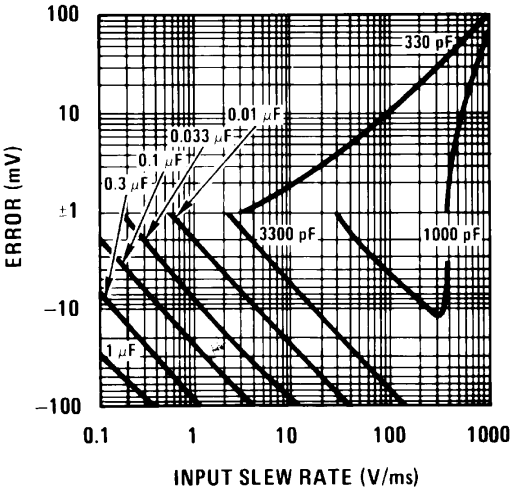


Figure 3. Dynamic Sampling Error

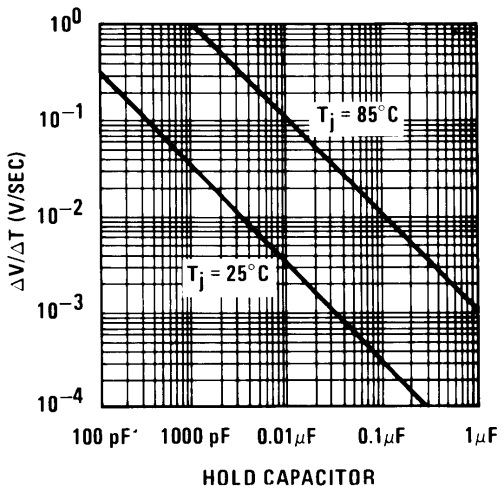


Figure 4. Output Droop Rate

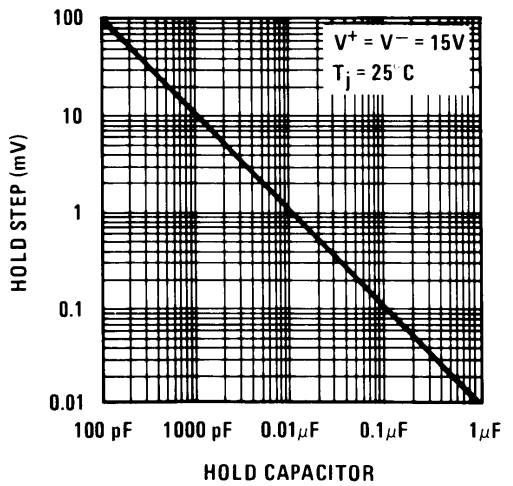


Figure 5. Hold Step

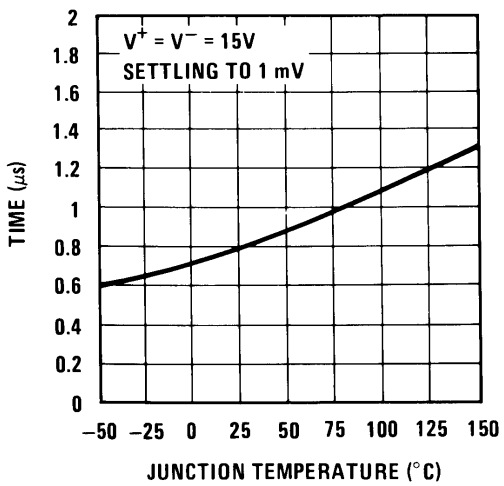


Figure 6. Hold Settling Time

Typical Characteristics (continued)

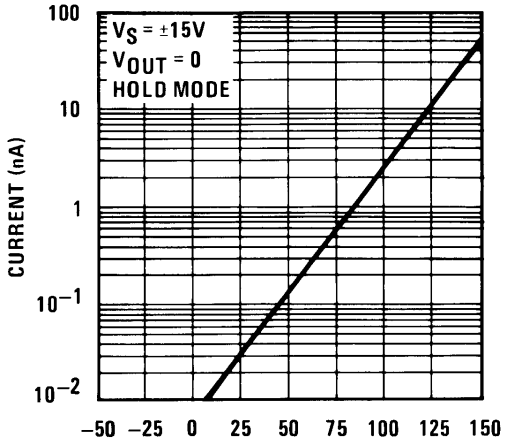


Figure 7. Leakage Current into Hold Capacitor

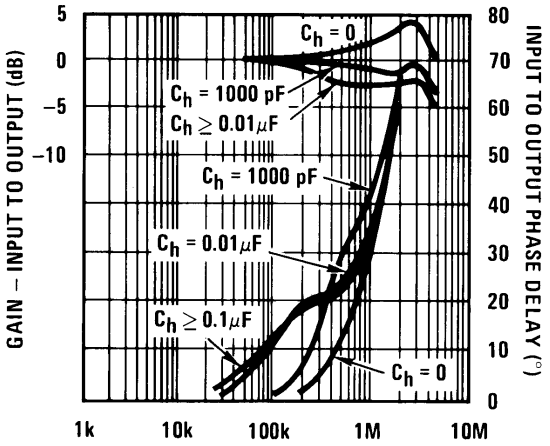


Figure 8. Phase and Gain (Input to Output, Small Signal)

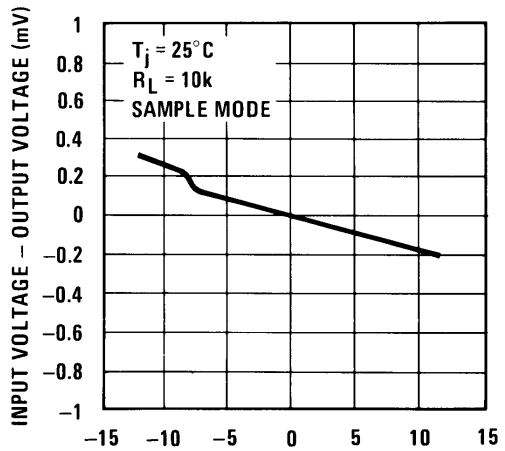


Figure 9. Gain Error

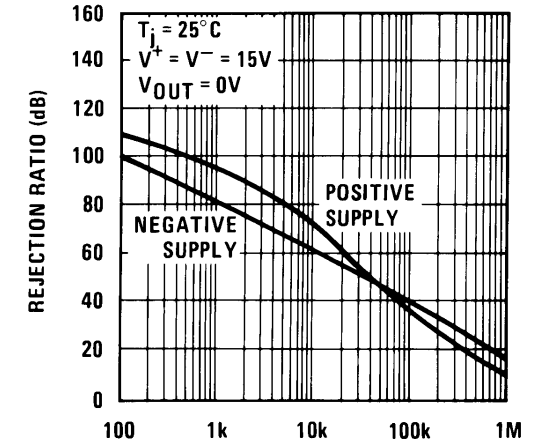


Figure 10. Power Supply Rejection

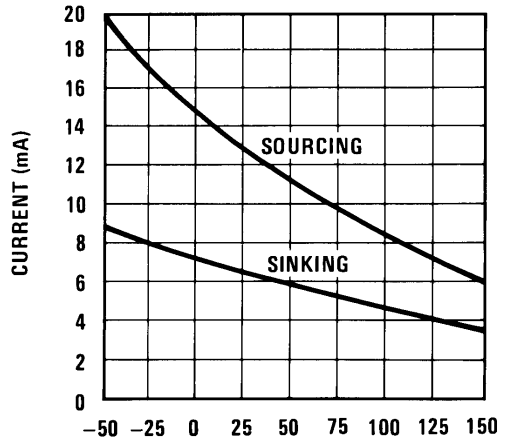


Figure 11. Output Short Circuit Current

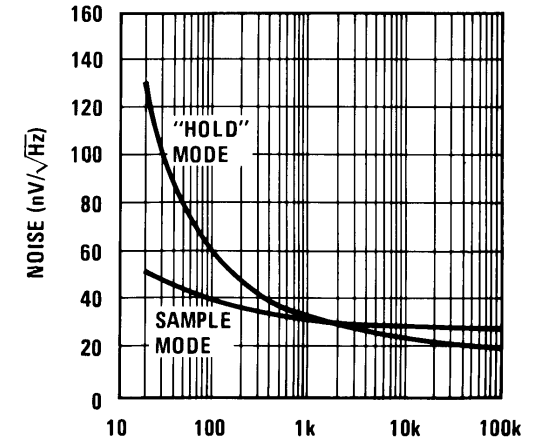


Figure 12. Output Noise

Typical Characteristics (continued)

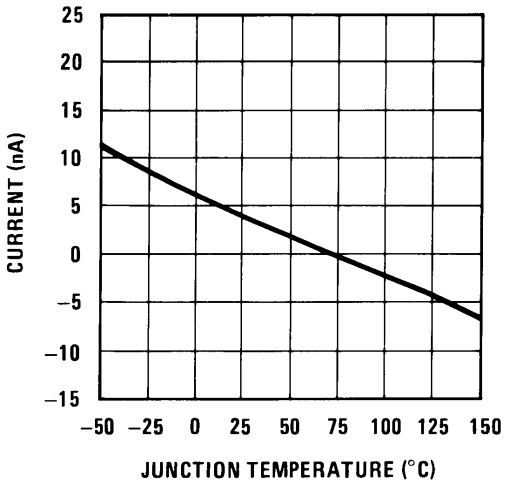


Figure 13. Input Bias Current

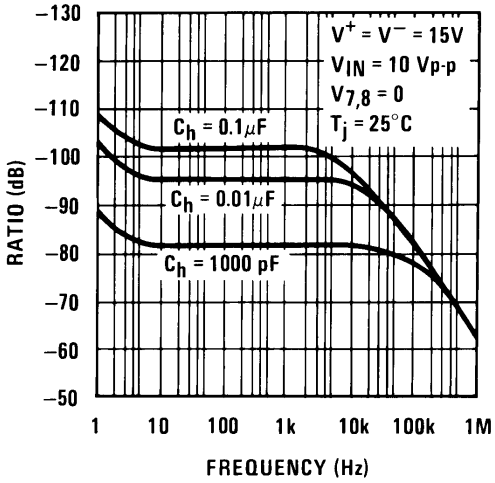


Figure 14. Feedthrough Rejection Ratio (Hold Mode)

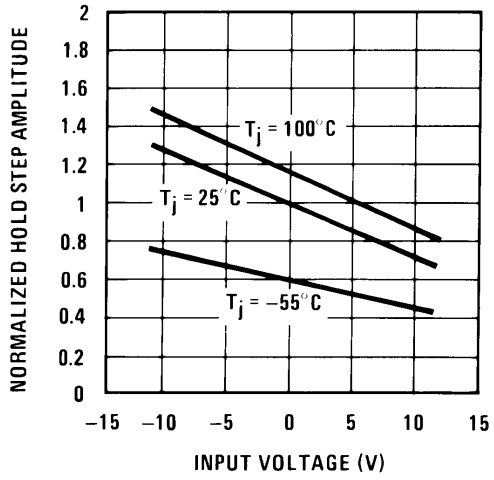


Figure 15. Hold Step vs Input Voltage

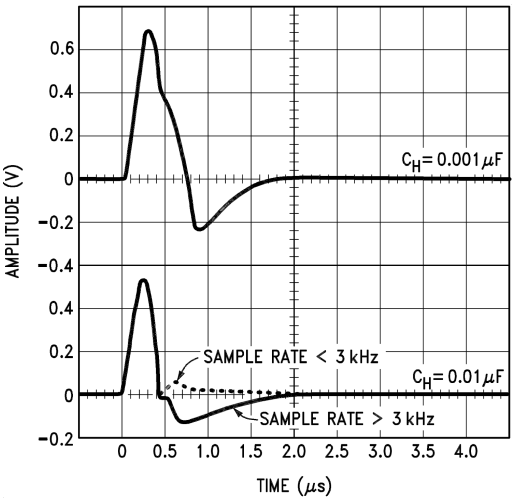


Figure 16. Output Transient at Start of Sample Mode

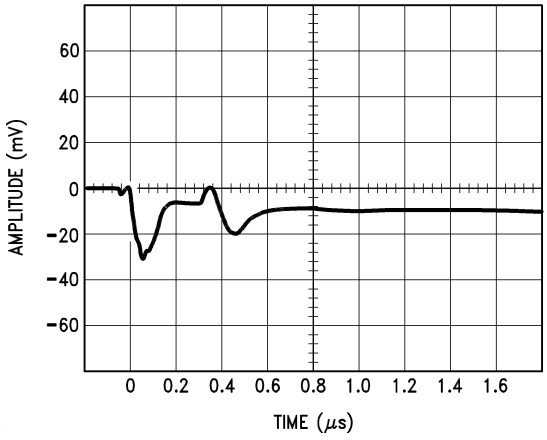
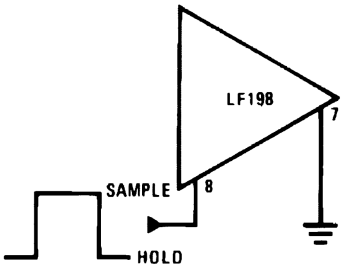


Figure 17. Output Transient at Start of Hold Mode

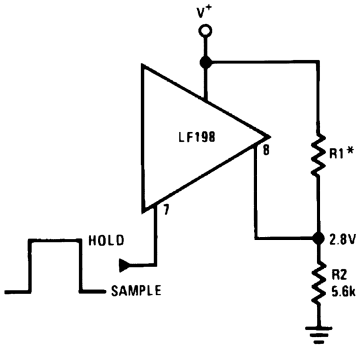
7 Parameter Measurement Information

7.1 TTL and CMOS 3 V ≤ V_{LOGIC} (Hi State) ≤ 7 V



Threshold = 1.4 V

Figure 18. Sample When Logic High With TTL and CMOS Biasing

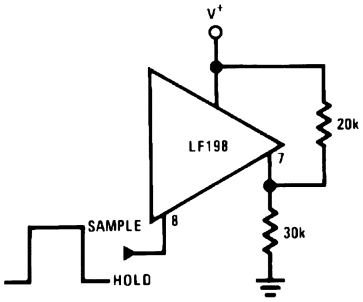


Threshold = 1.4 V

Select for 2.8 V at pin 8

Figure 19. Sample When Logic Low With TTL and CMOS Biasing

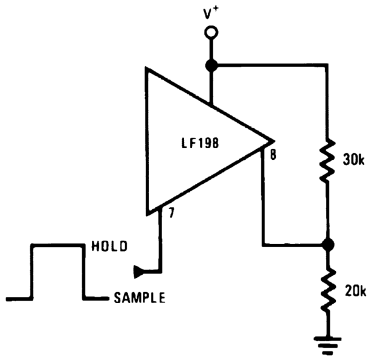
7.2 CMOS 7 V ≤ V_{LOGIC} (Hi State) ≤ 15 V



Threshold = 0.6 (V^+) + 1.4 V

Figure 20. Sample When Logic High With CMOS Biasing

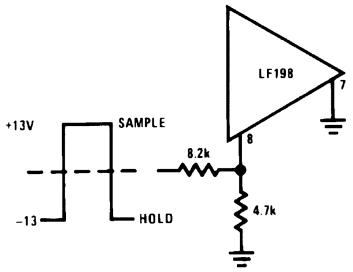
CMOS 7 V ≤ V_{LOGIC} (Hi State) ≤ 15 V (continued)



Threshold = 0.6 (V^+) –1.4V

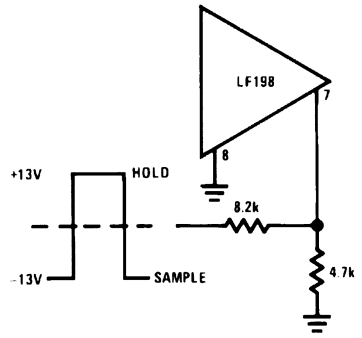
Figure 21. Sample When Logic Low With CMOS Biasing

7.3 Operational Amplifier Drive



Threshold ≈ +4 V

Figure 22. Sample When Logic High With Operational Amplifier Biasing



Threshold = −4 V

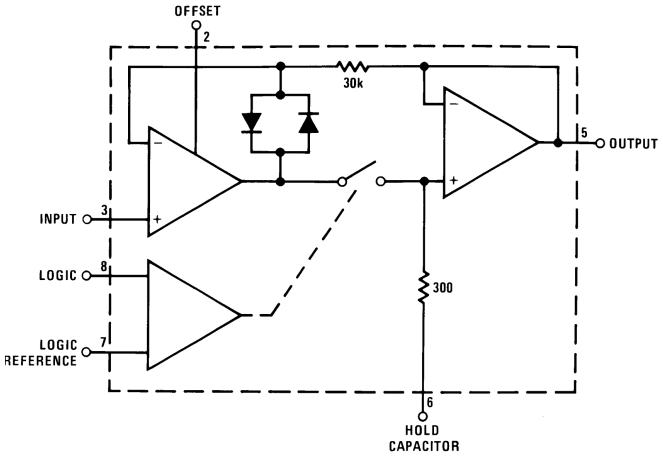
Figure 23. Sample When Logic Low With Operational Amplifier Biasing

8 Detailed Description

8.1 Overview

The LFx98x devices are monolithic sample-and-hold circuits that utilize BI-FET technology to obtain ultrahigh DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity-gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6 µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198-N to be included inside the feedback loop of 1-MHz operational amplifier without having stability problems. Input impedance of 10^{10} Ω allows high-source impedances to be used without degrading accuracy.

8.2 Functional Block Diagram



8.3 Feature Description

The LFx98x OUTPUT tracks the INPUT signal by charging and discharging the hold capacitor. The OUTPUT can be held at any given time by pulling the LOGIC input low relative to the LOGIC REFERENCE voltage and resume sampling when LOGIC returns high. Additionally, the OFFSET pin can be used to zero the offset voltage present at the INPUT.

8.4 Device Functional Modes

The LFx98x devices have a *sample* mode and *hold* mode controlled by the LOGIC voltage relative to the LOGIC REFERENCE voltage. The device is in *sample* mode when the LOGIC input is pulled high relative to the LOGIC REFERENCE voltage and in *hold* mode when the LOGIC input is pulled low relative to the LOGIC REFERENCE. In *sample* mode, the output is tracking the input signal by charging and discharging the hold capacitor. Smaller values of hold capacitance will allow the output to track faster signals. In *hold* mode the input signal is disconnected from the signal path and the output retains the value on the hold capacitor. Larger values of capacitance will have a smaller droop rate as shown in Figure 4.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Hold Capacitor

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198-N.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may *sag back* up to 0.2% after a quick change in voltage. A long sample time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. Most ceramic capacitors are unusable with > 1% hysteresis. Ceramic NPO or COG capacitors are now available for 125°C operation and also have low dielectric absorption. For more exact data, see Figure 2. The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198-N is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10 to 50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

9.1.2 DC and AC Zeroing

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1-kΩ potentiometer, which has one end tied to V+ and the other end tied through a resistor to ground. The resistor should be selected to give approximately 0.6 mA through the 1-kΩ potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10-pF capacitor from the wiper to the hold capacitor will give ±4-mV hold step adjustment with a 0.01-µF hold capacitor and 5-V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

9.1.3 Logic Rise Time

For proper operation, logic signals into the LF198-N must have a minimum dV/dt of 1.0 V/µs. Slower signals will cause excessive hold step. If a R/C network is used in front of the logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/µs.

9.1.4 Sampling Dynamic Signals

Sample error to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300-Ω series resistor on the chip. This means that at the moment the *hold* command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp–p at 10 kHz. Maximum dV/dt is 0.6 V/µs. With no analog phase delay and 100-ns logic delay, one could expect up to (0.1 µs) (0.6V/µs) = 60 mVerror if the hold signal arrived near maximum dV/dt of the input. A positive-going input would give a

Application Information (continued)

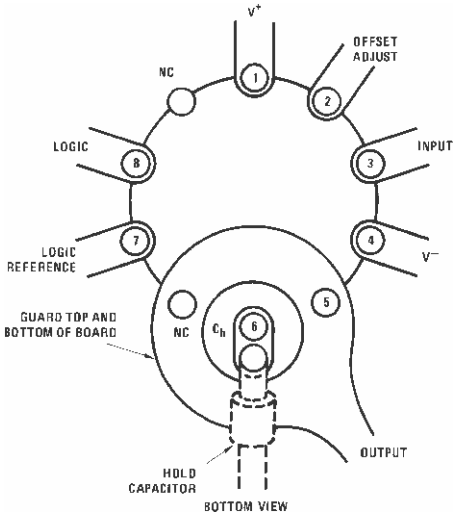
60-mV error. Now assume a 1-MHz (3-dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16 µs) (0.6 V/µs) = –96 mV. Total output error is 60 mV (digital) –96 mV (analog) for a total of –36 mV. To add to the confusion, analog delay is proportioned to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

Figure 1 has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the hold command. This curve is based on a 1-mV error fed into the output.

Figure 6 indicates the time required for the output to settle to 1 mV after the hold command.

9.1.5 Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input and the C_h pin. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5 V will also help.



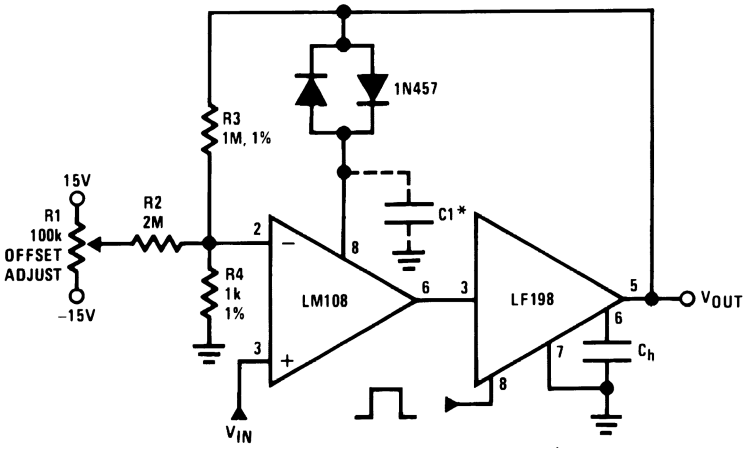
Use 10-pin layout. Guard around C_H is tied to output.

Figure 24. Guarding Technique

9.2 Typical Applications

9.2.1 X1000 Sample and Hold

The circuit configuration in Figure 25 shows how to incorporate an amplification factor of 1000 into the sample and hold stage. This may be particularly useful if the input signal has a very low amplitude. Equation 1 provides the appropriate value of capacitance for the COMP 2 pin capacitance of the LM108.



*For lower gains, the LM108 must be frequency compensated

Figure 25. X1000 Sample and Hold

$$\text{Use} \approx \frac{100}{A_V}\text{pF from comp 2 to ground} \tag{1}$$

9.2.1.1 Design Requirements

Assume an unbuffered analog to digital converter with 1-Vpp dynamic range is used in a system which needs to sample an input signal with only 1-mVpp amplitude. Using the LF198-N and LM108 connect the input signal so that the maximum dynamic range is used by the 1-Vpp data converter.

9.2.1.2 Detailed Design Procedure

Connect the LFx98x and LM108 as shown in Figure 25. To maximize the dynamic range of 1 Vpp a gain factor of 1000x is needed. Set R3 to 1 MΩ and R4 to 1 kΩ to give a noninverting gain of 1001. The calculated value of C1 is 0.1 pF according to Equation 1, which is negligibly small and may be left off of the design.

Typical Applications (continued)

9.2.1.3 Application Curves

The feedthrough rejection ratio of the LF198-N is extremely good and provides good isolation for a wide variety of hold capacitors as Figure 26 shows. Additionally, the output transient settles almost completely after 0.8 µs and would be ready to sample as shown in Figure 27.

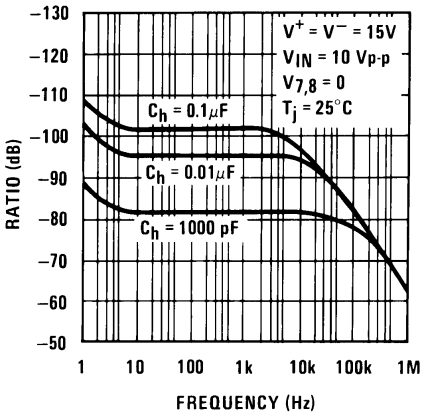


Figure 26. Feedthrough Rejection Ratio (Hold Mode)

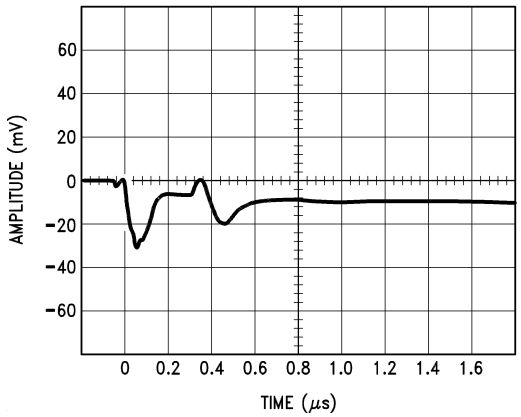
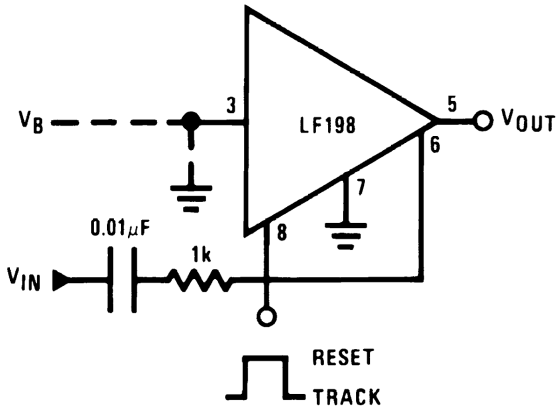


Figure 27. Output Transient at Start of Hold Mode

9.2.2 Sample and Difference Circuit

The LFx98x may be used as a sample and difference circuit as shown in Figure 28 where the output follows the input in hold mode.



$V_{OUT} = V_B + \Delta V_{IN}$ (HOLD MODE)

Figure 28. Sample and Difference Circuit

Typical Applications (continued)

9.2.3 Ramp Generator With Variable Reset Level

The circuit configuration shown in Figure 29 generates a ramp signal with variable reset level. The rise or fall time may be computed by Equation 2.

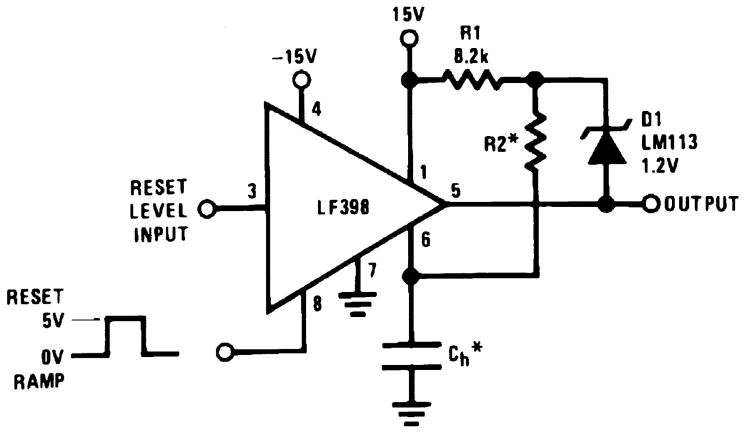


Figure 29. Ramp Generator With Variable Reset Level

$$\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)(C_h)} \tag{2}$$

9.2.4 Integrator With Programmable Reset Level

The LFx98x may be used with LM308 to create an integrator circuit with programmable reset level as shown in Figure 30. The integrated output voltage in hold mode is computed with Equation 3.

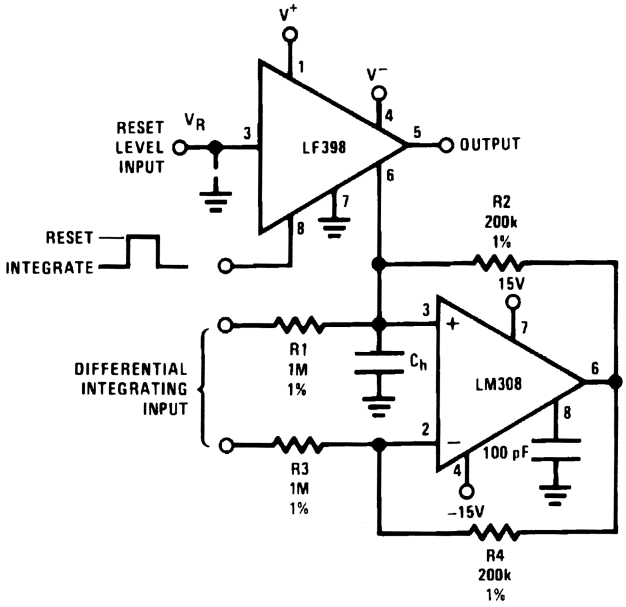


Figure 30. Integrator With Programmable Reset Level

$$V_{OUT}\ (\text{Hold Mode}) = \left[\frac{1}{(R1)(C_h)}\int_0^t V_{IN}\ dt\right] + \left[V_R\right] \tag{3}$$

Typical Applications (continued)

9.2.5 Output Holds at Average of Sampled Input

The LFx98x can be used to identify the average value of the input signal and hold the corresponding voltage on the output. Connect R_h and C_h as shown in Figure 31. The corresponding values may be calculated with Equation 4.

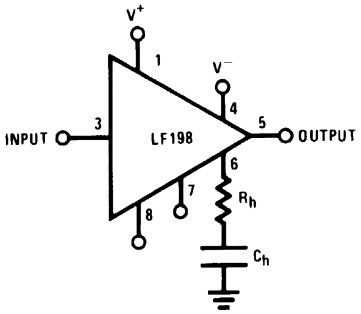


Figure 31. Output Holds at Average of Sampled Input

$$\text{Select } (R_h)\,(C_h) \gg \frac{1}{2\pi f_{IN}\,(\text{Min})} \tag{4}$$

9.2.6 Increased Slew Current

The slew current can be increased by connecting opposing diodes from the OUTPUT to the HOLD CAPACITOR pins as shown in Figure 32.

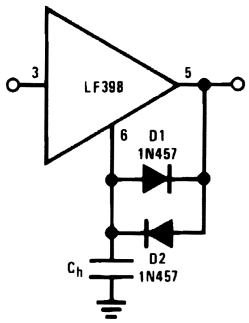
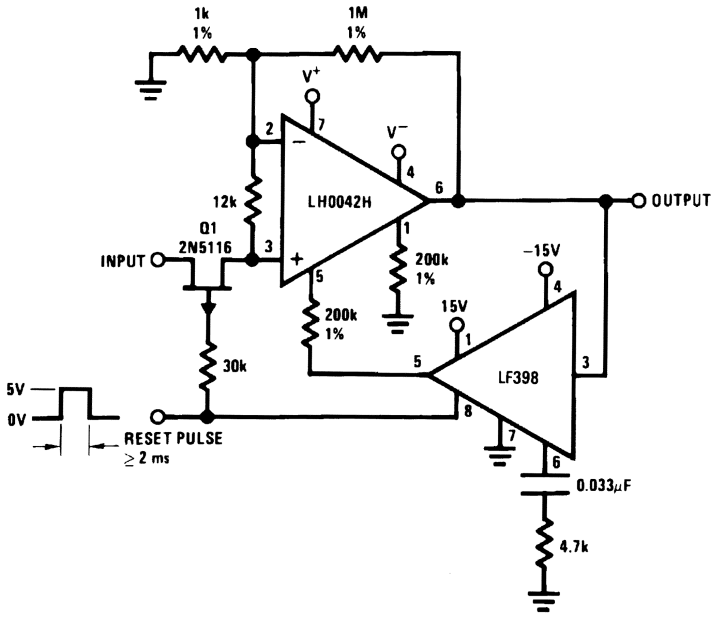


Figure 32. Increased Slew Current

Typical Applications (continued)

9.2.7 Reset Stabilized Amplifier

The LFx98x may be used with LH0042H to create a reset stabilized amplifier with a gain of 1000 as shown in Figure 33.



$V_{OS} \leq 20\ \mu V$ (No trim) $Z_{IN} \approx 1\ M\Omega$

Figure 33. Reset Stabilized Amplifier

$$\frac{\Delta V_{OS}}{\Delta t} \approx 30\mu V / sec \quad (5)$$

$$\frac{\Delta V_{OS}}{\Delta T} \approx 0.1\mu V/^{\circ}C \quad (6)$$

Typical Applications (continued)

9.2.8 Fast Acquisition, Low Droop Sample and Hold

Two LFx98x devices may be used along with LM3905 TIMER to create a fast acquisition, low droop sample and hold circuit as shown in Figure 34.

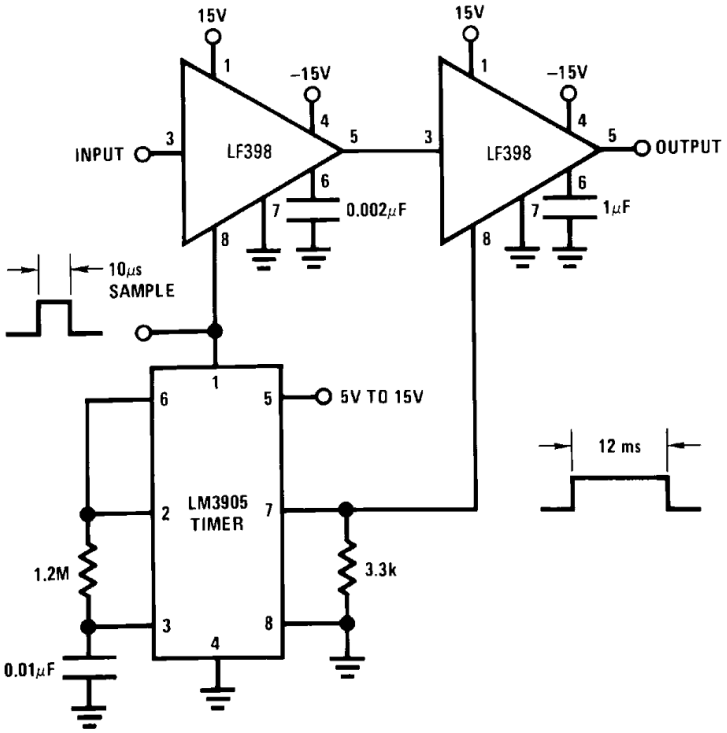


Figure 34. Fast Acquisition, Low Droop Sample and Hold

Typical Applications (continued)

9.2.9 Synchronous Correlator for Recovering Signals Below Noise Level

The LFx98x may be used with two LM122H TIMER devices to create a synchronous correlator for recovering signals below noise level as shown in Figure 35.

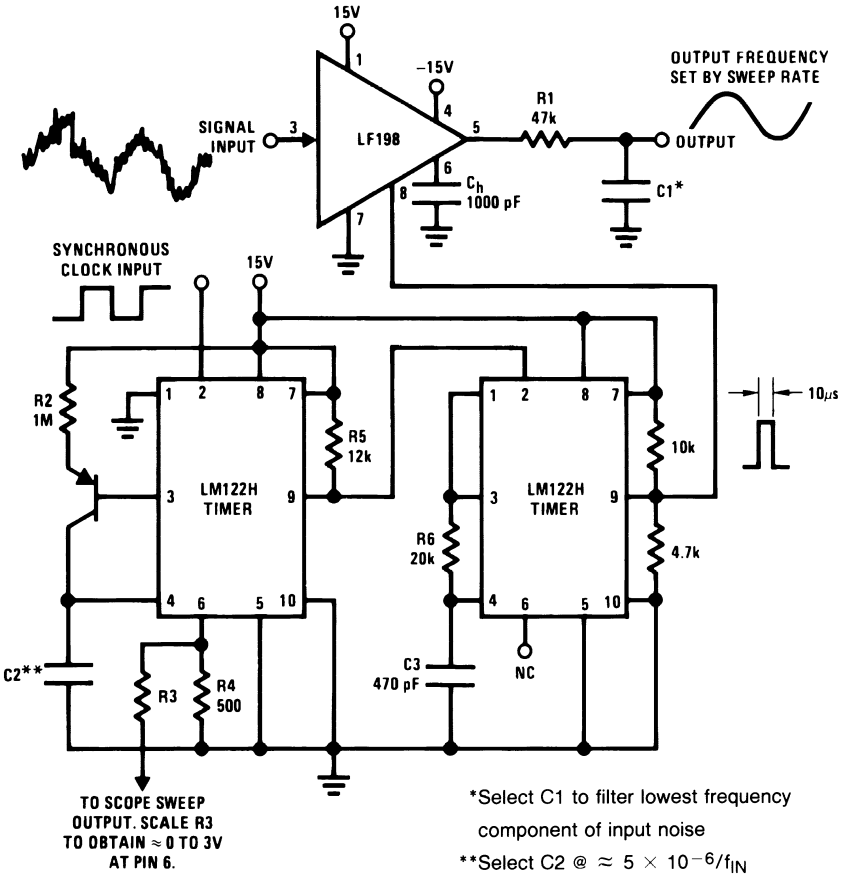


Figure 35. Synchronous Correlator for Recovering Signals Below Noise Level

9.2.10 2-Channel Switch

The HOLD CAPACITOR pin could be alternatively used as a second input to create a 2-channel switch shown Figure 36

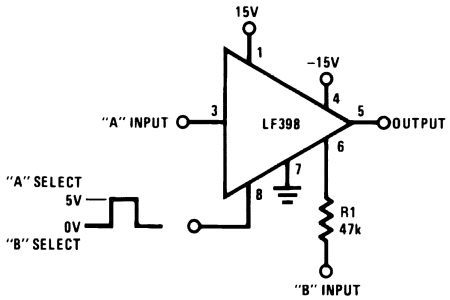


Figure 36. 2-Channel Switch

In the configuration of Figure 36, input signal A and input signal B have the characteristics listed in Table 1.

Typical Applications (continued)

Table 1. 2-Channel Switch Characteristics

	A	B
Gain	1 ± 0.02%	1 ± 0.2%
ZIN	10^{10} Ω	47 kΩ
BW	≈1 MHz	≈400 kHz
Crosstalk @ 1 kHz	–90 dB	–90 dB
Offset	≤ 6 mV	≤ 75 mV

9.2.11 DC and AC Zeroing

The LFLFx98x features an OFFSET ADJUST pin which can be connected to a potentiometer to zero the DC offset. Additionally, an inverter may be connected with an AC-coupled potentiometer to the HOLD CAPACITOR pin to create a DC- and AC-zeroing circuit as shown in Figure 37.

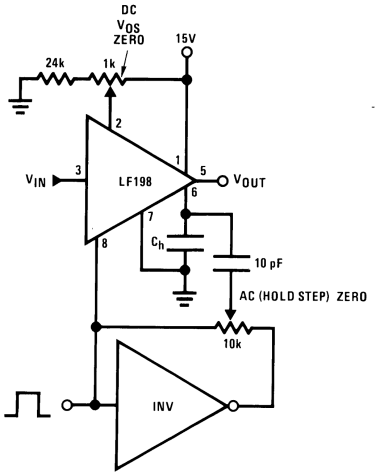
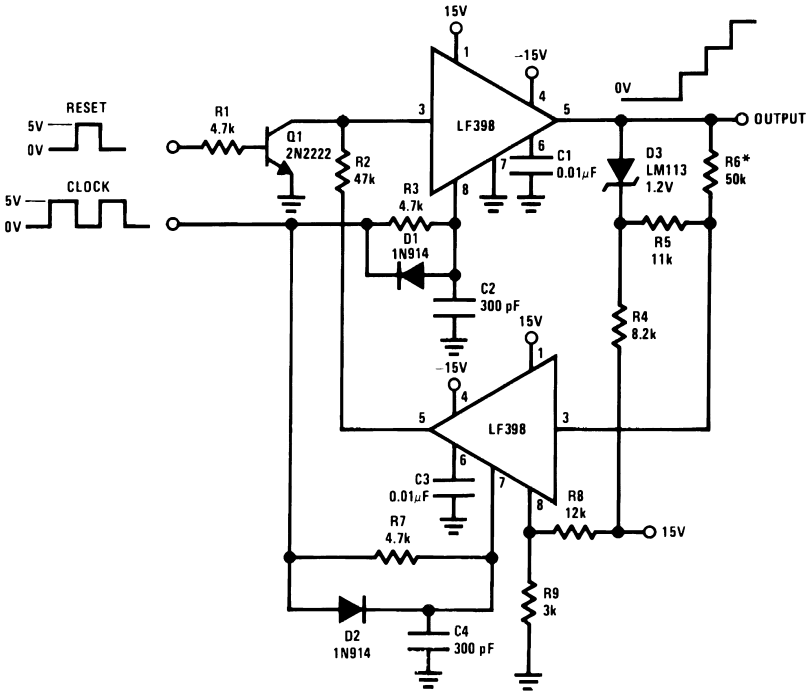


Figure 37. DC and AC Zeroing

9.2.12 Staircase Generator

The LFx98x can be connected as shown in Figure 38 to create a staircase generator.



*Select for step height: 50 kΩ → 1-V Step.

Figure 38. Staircase Generator

9.2.13 Differential Hold

Two LFx98x devices may be connected as shown in Figure 39 to create a differential hold circuit.

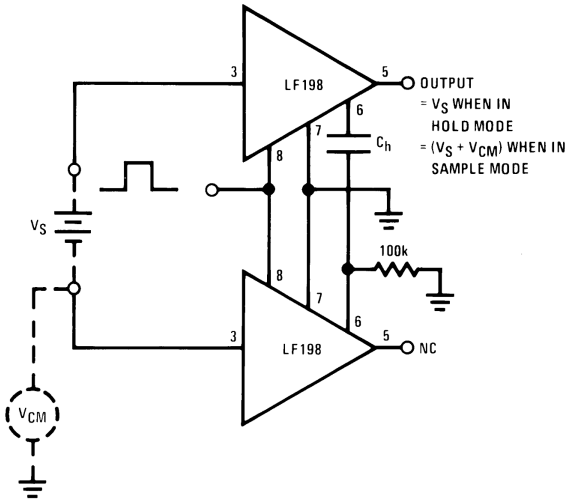
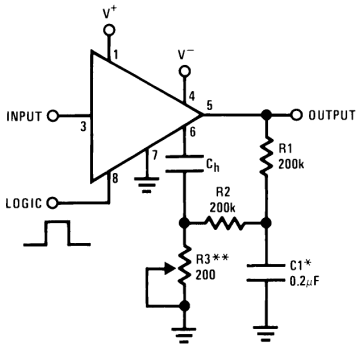


Figure 39. Differential Hold

9.2.14 Capacitor Hysteresis Compensation

The LFx98x devices may be used for capacitor hysteresis compensation as shown in Figure 40.



*Select for time constant C1 = τ/100 kΩ

**Adjust for amplitude

Figure 40. Capacitor Hysteresis Compensation

10 Power Supply Recommendations

The LFx98x devices are rated for a typical supply voltage of ±15 V. To achieve noise immunity as appropriate to the application, it is important to use good printed-circuit-board layout practices for power supply rails and planes, as well as using bypass capacitors connected between the power supply pins and ground. All bypass capacitors must be rated to handle the supply voltage and be decoupled to ground. TI recommends to decouple each supply with two capacitors; a small value ceramic capacitor (approximately 0.1 μF) placed close to the supply pin in addition to a large value Tantalum or Ceramic (≥ 10 μF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at higher frequencies while the large capacitor will act as the charge bucket for fast load current spikes at the op amp output. The combination of these capacitors will provide supply decoupling and will help maintain stable operation for most loading conditions.

11 Layout

11.1 Layout Guidelines

Take care to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. A ground plane underneath the device is recommended; any bypass components to ground should have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins will lower the power supply inductance and provide a more stable power supply. The feedback components should be placed as close to the device as possible to minimize stray parasitics.

11.2 Layout Example

Figure 41 shows an example schematic and layout for the LFx98x 8-pin PDIP package.

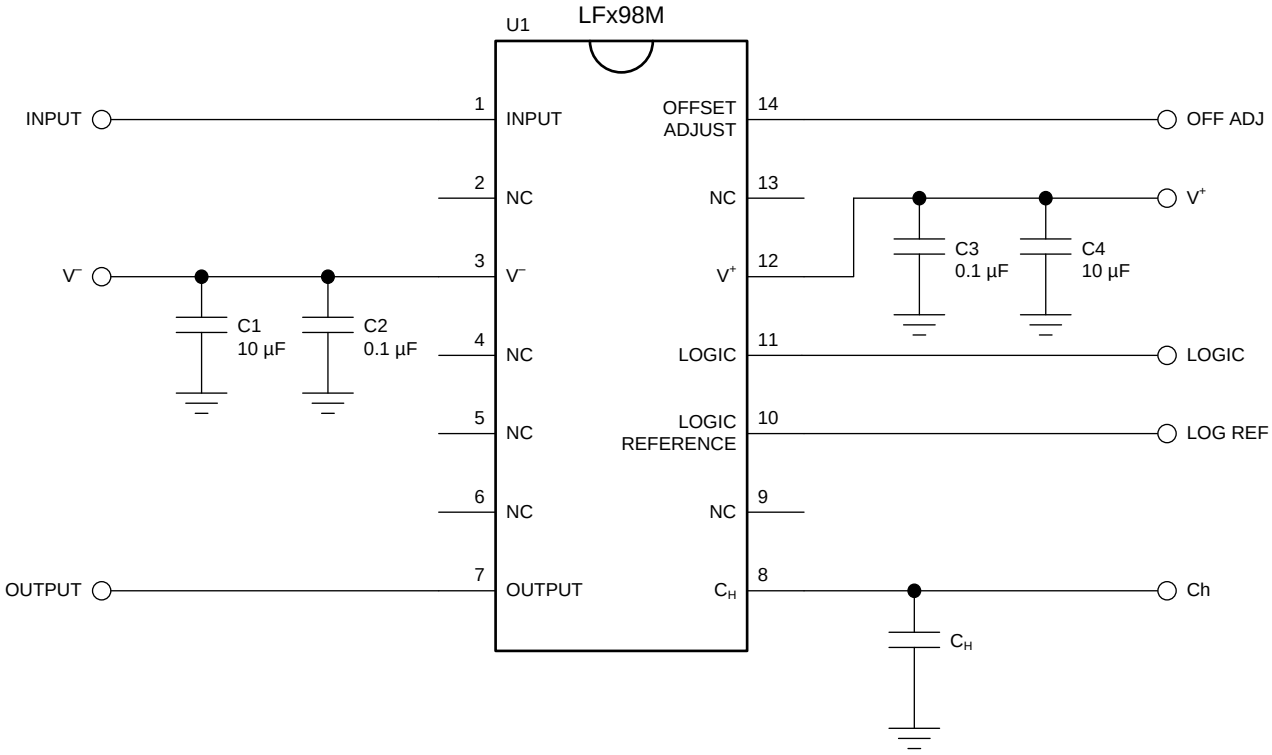


Figure 41. Schematic Example

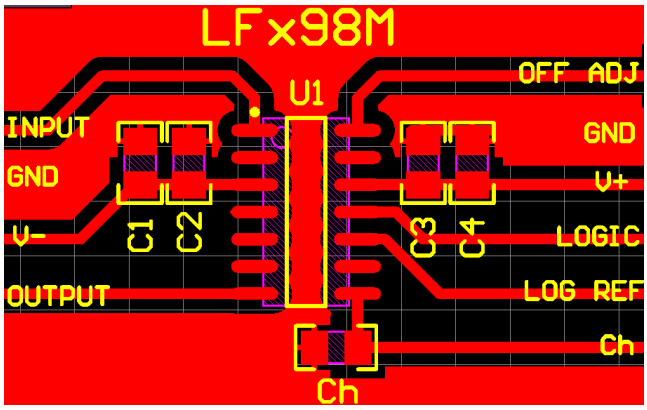


Figure 42. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

- **Hold Step:** The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is 5 V.
- **Acquisition Time:** The time required to acquire a new analog input voltage with an output step of 10 V. Acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.
- **Gain Error:** The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.
- **Hold Settling Time:** The time required for the output to settle within 1 mV of final value after the *hold* logic command.
- **Dynamic Sampling Error:** The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. This error term occurs even for long sample times.
- **Aperture Time:** The delay required between *hold* command and an input analog transition, so that the transition does not affect the held output.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LF198-N	Click here	Click here	Click here	Click here	Click here
LF298	Click here	Click here	Click here	Click here	Click here
LF398-N	Click here	Click here	Click here	Click here	Click here
LF198A-N	Click here	Click here	Click here	Click here	Click here
LF398A-N (Obsolete)	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LF198AH/NOPB	ACTIVE	TO-99	LMC	8	500	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	(LF198AH, LF198AH)	Samples
LF198H	ACTIVE	TO-99	LMC	8	500	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	(LF198H, LF198H)	Samples
LF198H/NOPB	ACTIVE	TO-99	LMC	8	500	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	(LF198H, LF198H)	Samples
LF298M/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-25 to 85	LF298M	Samples
LF298MX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-25 to 85	LF298M	Samples
LF398AN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	0 to 70	LF 398AN	Samples
LF398H	ACTIVE	TO-99	LMC	8	500	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	0 to 70	LF398H	Samples
LF398H/NOPB	ACTIVE	TO-99	LMC	8	500	RoHS & Green	Call TI	Level-1-NA-UNLIM	0 to 70	(LF398H, LF398H)	Samples
LF398M/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LF398M	Samples
LF398MX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LF398M	Samples
LF398N/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	0 to 70	LF 398N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

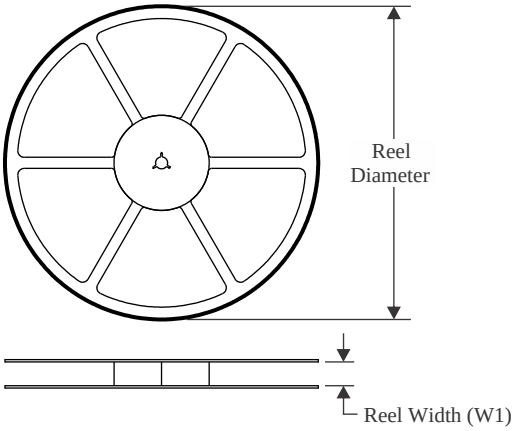
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

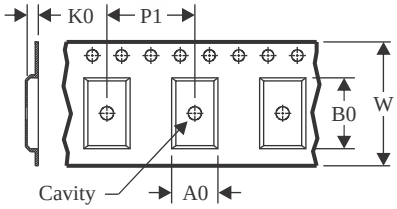
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

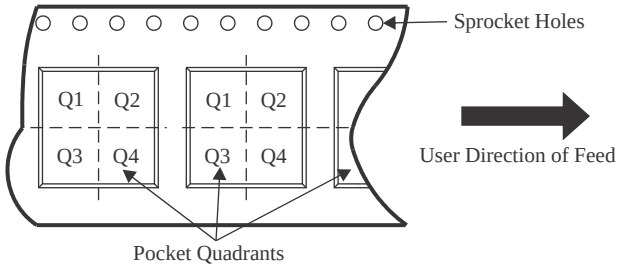


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

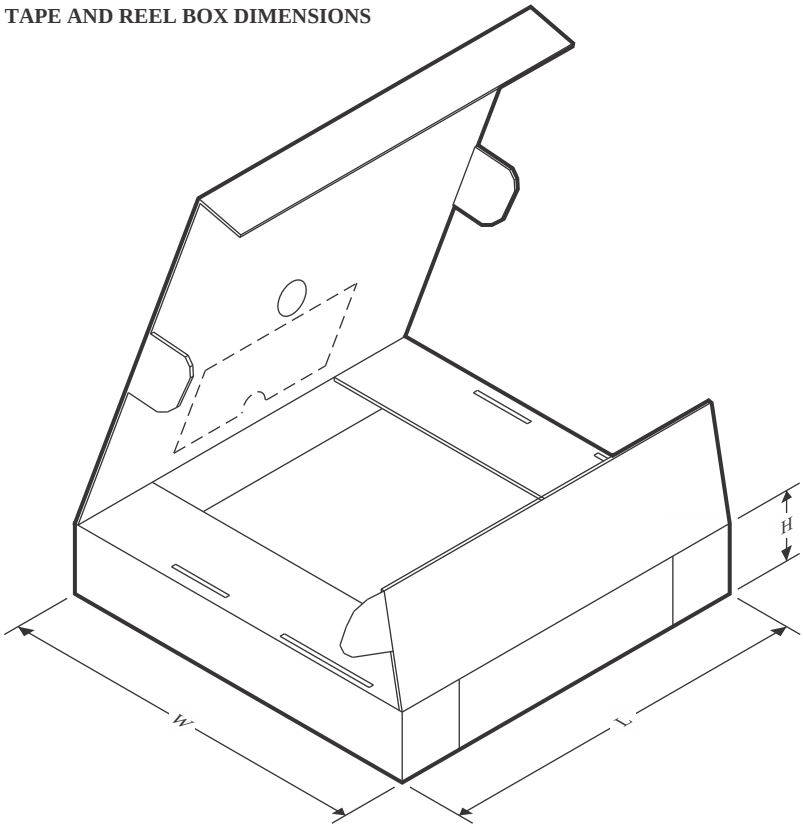
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF298MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LF398MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

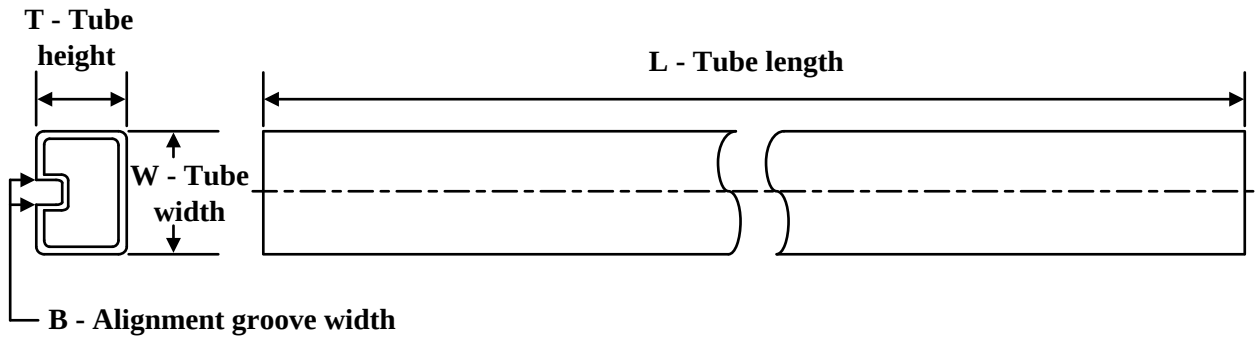
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

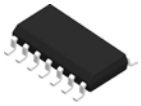
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF298MX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LF398MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LF298M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LF398AN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LF398M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LF398N/NOPB	P	PDIP	8	40	502	14	11938	4.32

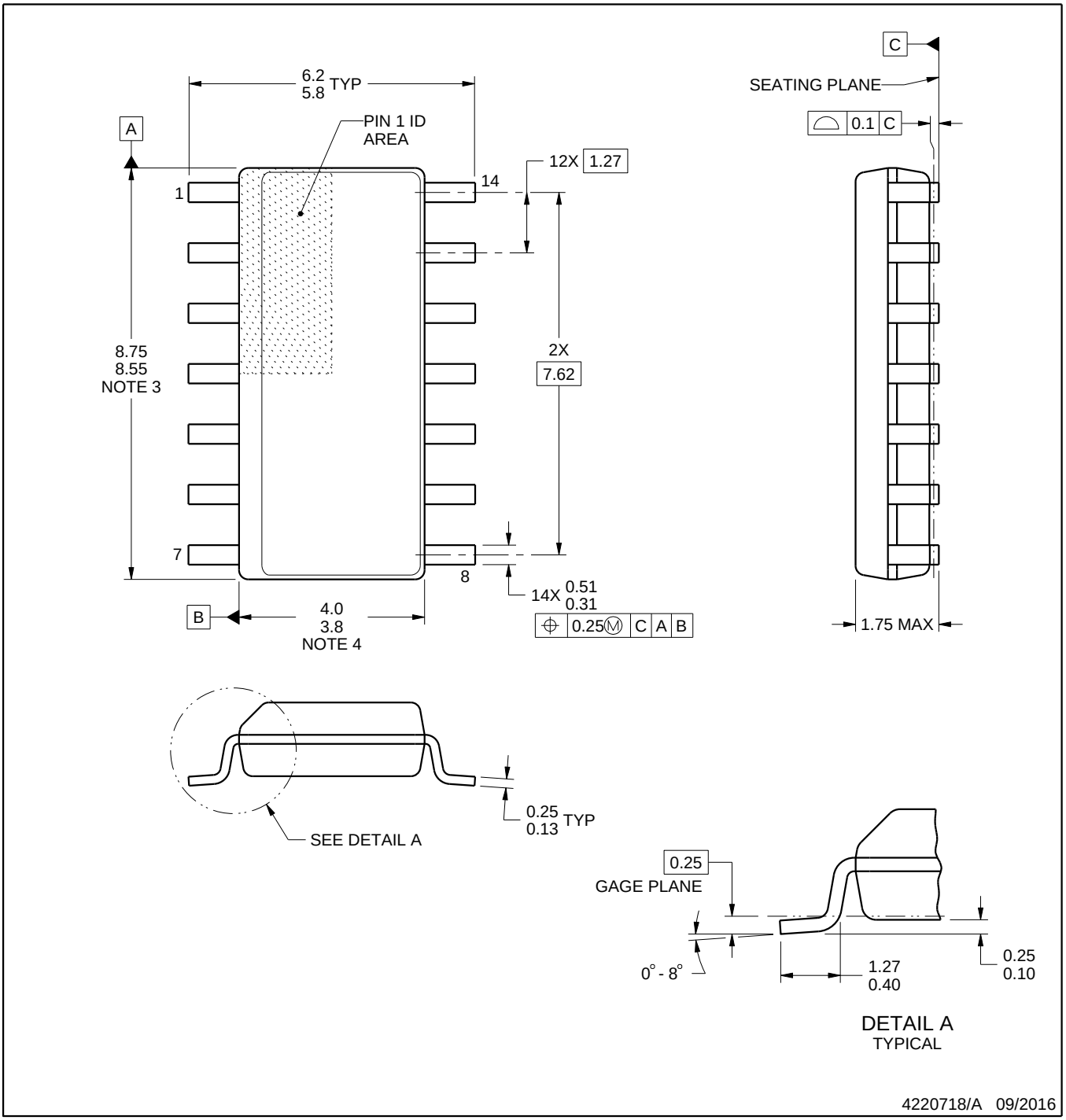


PACKAGE OUTLINE

D0014A

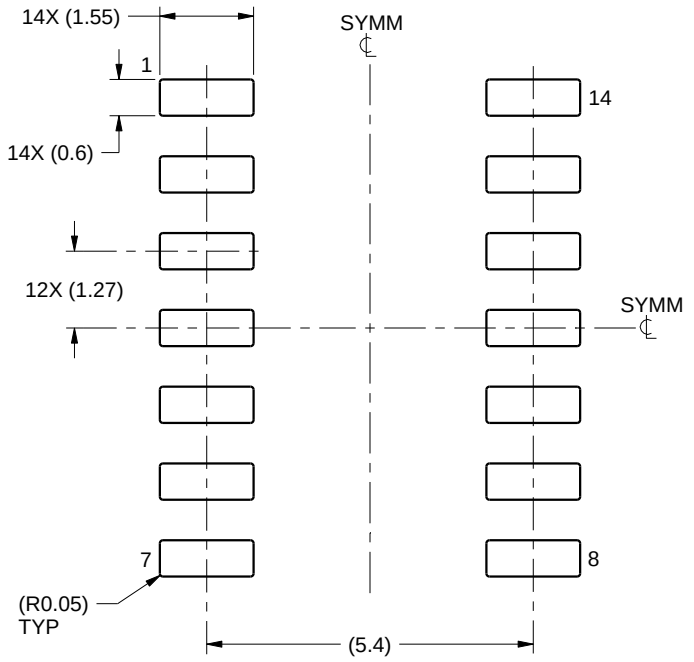
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

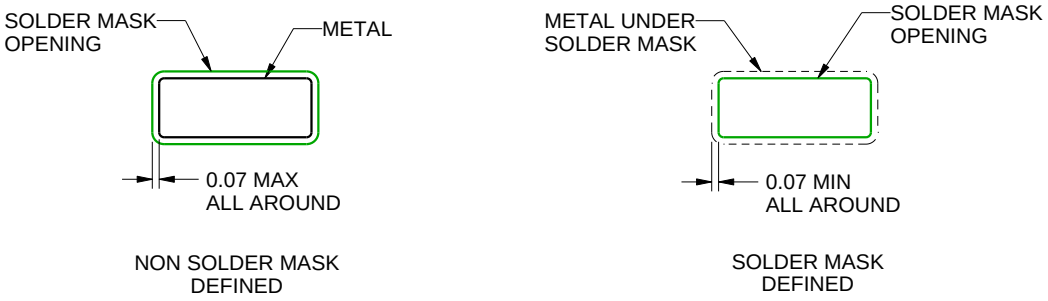


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

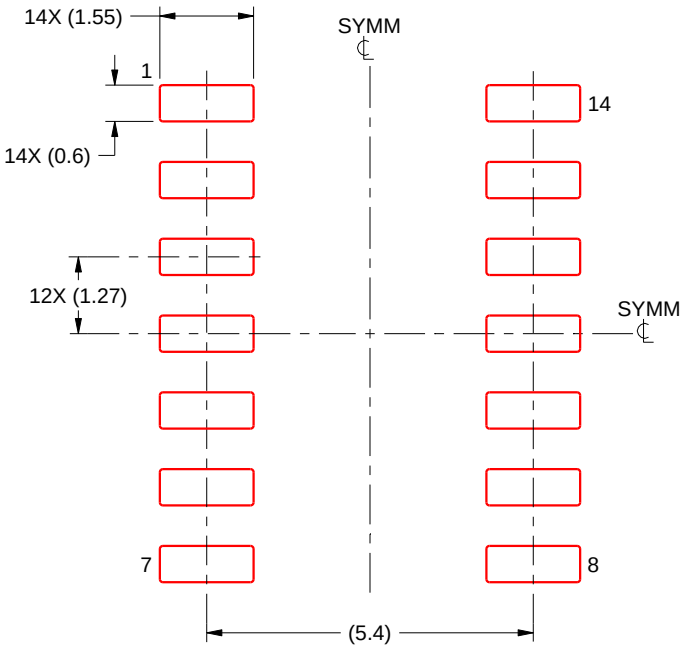
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

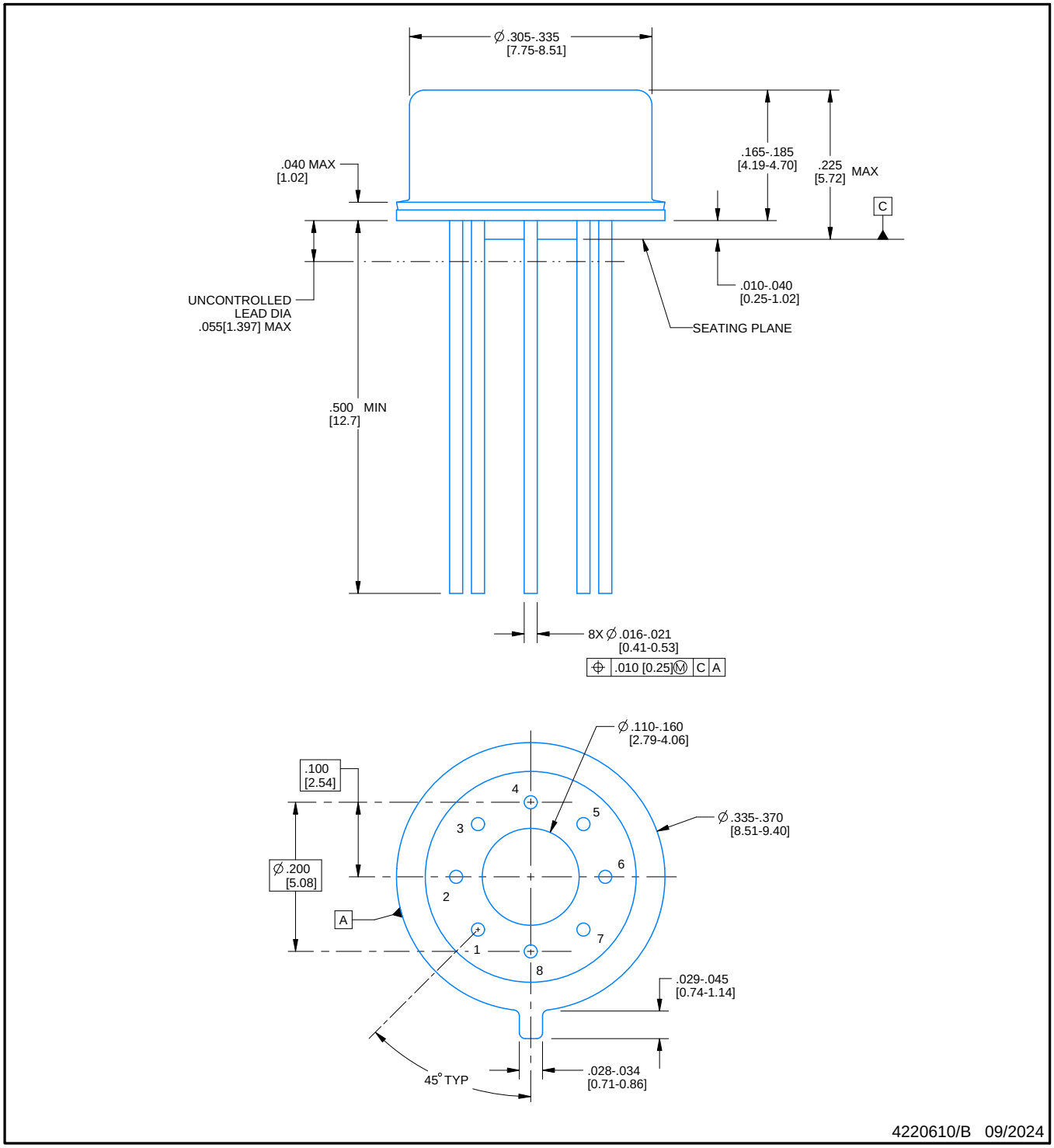
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

LMC0008A

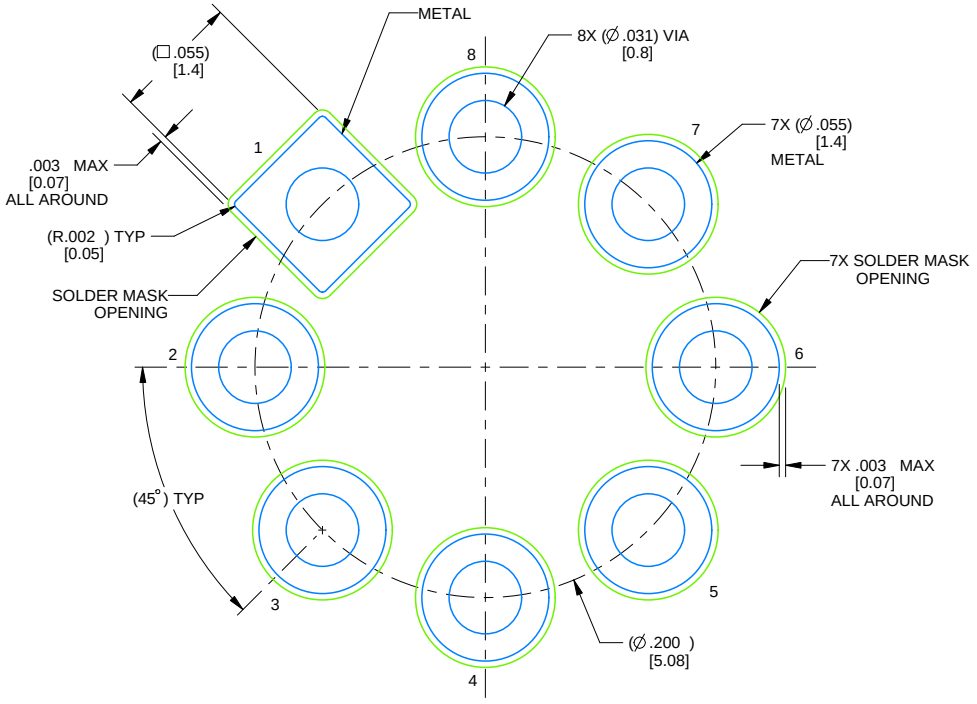
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



NOTES:

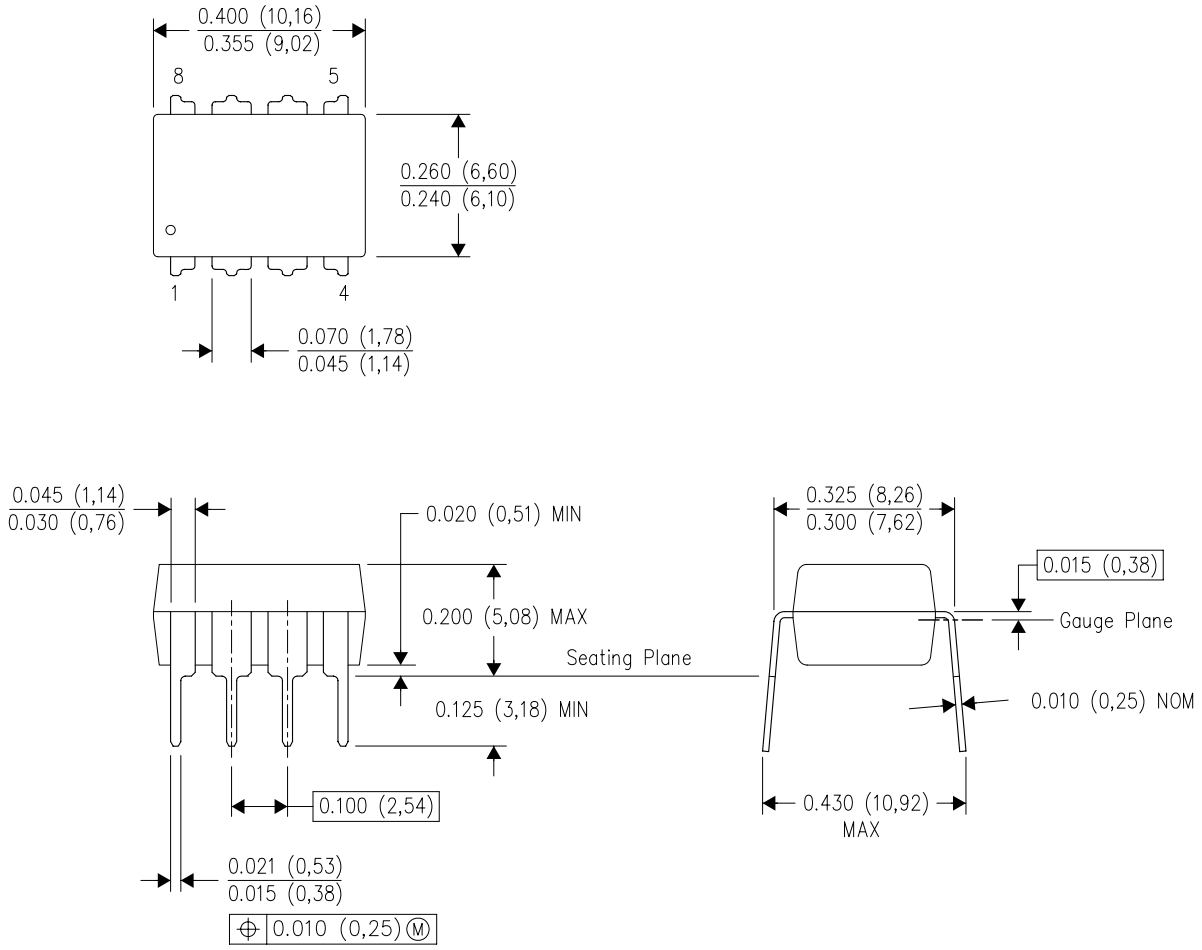
1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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