LM3674 2-MHz, 600-mA Step-Down DC-DC Converter in SOT-23

1 Features

- Input Voltage Range From 2.7 V to 5.5 V
- 600-mA Maximum Load Current
- Available in Fixed and Adjustable Output Voltages Ranging From 1 V to 3.3 V
- Operates From a Single Li-Ion Cell Battery
- Internal Synchronous Rectification for High Efficiency
- Internal Soft-Start
- 0.01-µA Typical Shutdown Current
- 2-MHz PWM Fixed Switching Frequency (typical)
- Current Overload Protection and Thermal Shutdown Protection

2 Applications

- Mobile Phones
- PDAs
- MP3 Players
- Portable Instruments
- W-LAN
- Digital Still Cameras
- Portable Hard Disk Drives

3 Description

The LM3674 step-down DC-DC converter is optimized for powering low-voltage circuits from a single Li-Ion cell battery and input voltage rails from 2.7 V to 5.5 V. It provides up to 600-mA load current over the entire input voltage range. There are several fixed output voltages and adjustable output voltage versions.

The device offers superior features and performance for mobile phones and similar portable systems. During the Pulse Width Modulation (PWM) mode, the device operates at a fixed-frequency of 2 MHz (typical). Internal synchronous rectification provides high efficiency during the PWM mode operation. In shutdown mode, the device turns off and reduces battery consumption to 0.01 µA (typical).

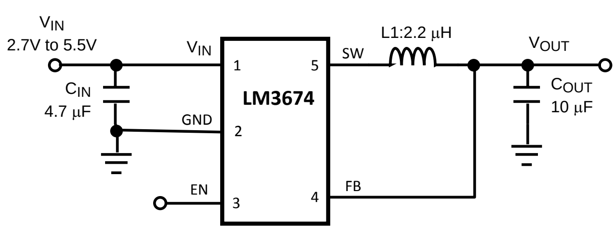
The LM3674 is available in a 5-pin SOT-23 package. A high switching frequency of 2 MHz (typical) allows use of only three tiny external surface-mount components, an inductor and two ceramic capacitors.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3674	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Typical Application Circuit for Adjustable Voltage Option

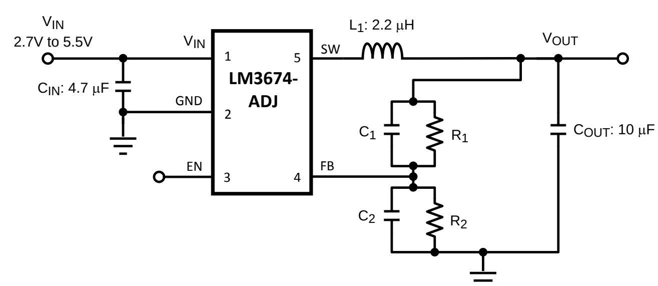


Table of Contents

4 Revision History

Changes from Revision F (May 2013) to Revision G — **Page**

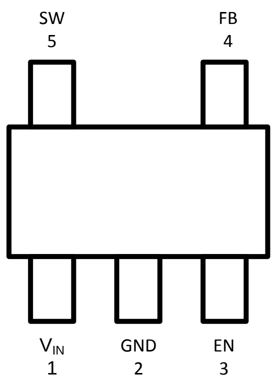
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Deleted "in leaded (Pb) and lead-free (no Pb) versions" 1

Changes from Revision E (April 2013) to Revision F — **Page**

- Changed layout of National Data Sheet to TI format 18

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Note: The actual physical placement of the package marking will vary from part to part.

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
EN	3	Digital	Enable input. The device is in shutdown mode when voltage to this pin is < 0.4 V and enable when > 1 V. Do not leave this pin floating.
FB	4	Analog	Feedback analog input. Connect to the output filter capacitor, C_{OUT}, for fixed voltage versions. For adjustable version, external resistor dividers are required (R_1 and R_2). The internal resistor dividers are disabled for the adjustable version.
GND	2	Ground	Ground pin
SW	5	Analog	Switching node connection to the internal PFET switch and NFET synchronous rectifier.
V_{IN}	1	Power	Power supply input. Connect to the input filter capacitor, C_{IN}.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{IN} pin: voltage to GND	−0.2	6	V
EN, FB, and SW pins	GND − 0.2	V_{IN} + 0.2	V
Continuous power dissipation(3)	Internally Limited		
Junction temperature (T_{J-MAX})		125	°C
Maximum lead temperature (soldering, 10 seconds)		260	°C
Storage temperature, T_{stg}	–65		°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military- or Aerospace-specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) In applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX}), the maximum power dissipation of the device in the application (P_{D-MAX}) and the junction-to-ambient thermal resistance of the package ($R_{θJA}$) in the application, as given by the following equation: $T_{A-MAX} = T_{J-MAX} – (R_{θJA} × P_{D-MAX})$. See *Dissipation Ratings* for P_{D-MAX} values at different ambient temperatures.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage(2)	2.7	5.5	V
Recommended load current	0	600	mA
Junction temperature, T_J	–30	125	°C
Ambient temperature,T_A	–30	85	°C

(1) All voltages are with respect to the potential at the GND pin.
(2) Input voltage range recommended for ideal applications performance for the specified output voltages are given below:
V_{IN} = 2.7 V to 5.5 V for 1 V ≤ V_{OUT} < 1.8 V
$V_{IN} = (V_{OUT} + V_{DROP\ OUT})$ to 5.5 V for 1.8 ≤ V_{OUT} ≤ 3.3 V, where $V_{DROP\ OUT} = I_{LOAD} × (R_{DSON\ (P)} + R_{INDUCTOR})$

6.4 Thermal Information

THERMAL METRIC(1)			LM3674 DBV (SOT-23) 5 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	4-layer board	130	°C/W
		2-layer board	250	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Dissipation Ratings

over operating free-air temperature range (unless otherwise noted)

$R_{θJA}$	T_A ≤ 25°C (POWER RATING)	T_A = 60°C (POWER RATING)	T_A = 85°C (POWER RATING)
250°C/W (2-layer board)	400 mW	260 mW	160 mW
130°C/W (4-layer board)	770 mW	500 mW	310 mW

6.6 Electrical Characteristics

Typical limits are T_A = 25°C; unless otherwise noted, specifications apply to the LM3674 with V_{IN} = EN = 3.6 V[(1)(2)(3)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback voltage[(4)(5)]	I_O = 10 mA, −30°C ≤ T_J ≤ 125°C	–4%		4%	
	Line regulation	2.7 V ≤ V_{IN} ≤ 5.5 V, I_O = 100 mA		0.083		%/V
	Load regulation	100 mA ≤ I_O ≤ 600 mA, V_{IN} = 3.6 V		0.0010		%/mA
V_{REF}	Internal reference voltage	See[(6)]		0.5		V
I_{SHDN}	Shutdown supply current	EN = 0 V		0.01		µA
		EN = 0 V, –30°C ≤ T_J ≤ 125°C			1	
I_Q	DC bias current into V_{IN}	No load, device is not switching (FB = 0 V)		300		µA
		No load, device is not switching (FB = 0 V) –30°C ≤ T_J ≤ 125°C			600	
$R_{DSON\ (P)}$	Pin-to-pin resistance for PFET	I_{SW} = 200 mA		380	500	mΩ
$R_{DSON\ (N)}$	Pin-to-pin resistance for NFET	I_{SW} = 200 mA		250	400	mΩ
I_{LIM}	Switch peak current limit	Open loop[(7)]		1020		mA
		Open loop[(7)], –30°C ≤ T_J ≤ 125°C	830		1200	
V_{IH}	Logic high input	–30°C ≤ T_J ≤ 125°C	1			V
V_{IL}	Logic low input	–30°C ≤ T_J ≤ 125°C			0.4	V
I_{EN}	Enable (EN) input current			0.01		µA
		–30°C ≤ T_J ≤ 125°C			1	
F_{OSC}	Internal oscillator frequency	PWM mode		2		MHz
		PWM mode, −30°C ≤ T_J ≤ 125°C	1.6		2.6	

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and maximum limits are specified by design, test, or statistical analysis. Typical numbers represent the most likely values.
(3) The parameters in the *Electrical Characteristics* are tested at V_{IN} = 3.6 V unless otherwise specified. For performance curves over the input voltage range, see *Typical Characteristics*.
(4) ADJ configured to 1.5-V output.
(5) For V_{OUT} < 2.5 V, V_{IN} = 3.6 V; for V_{OUT} ≥ 2.5 V, V_{IN} = V_{OUT} + 1.
(6) For the ADJ version the resistor dividers should be selected such that at the desired output voltage, the voltage at the FB pin is 0.5 V.
(7) See *Typical Characteristics* for closed loop data and its variation with regards to supply voltage and temperature. *Electrical Characteristics* reflect open loop data (FB = 0 V and current drawn from the SW pin ramped up until cycle-by-cycle current limit is activated). Closed-loop current limit is the peak inductor current measured in the application circuit by increasing output current until output voltage drops by 10%.

6.7 Typical Characteristics

(unless otherwise stated: V_{IN} = 3.6 V, V_{OUT} = 1.5 V, T_A = 25°C)

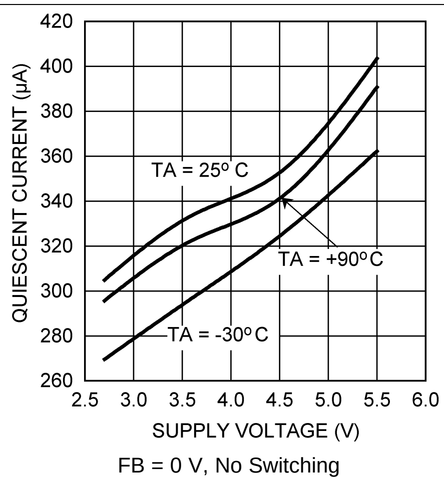


Figure 1. Quiescent Current vs Supply Voltage

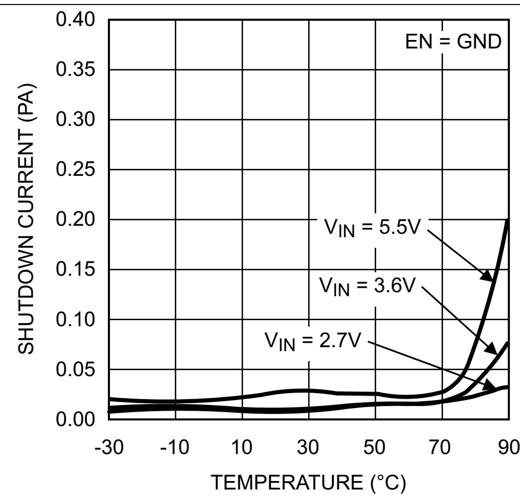


Figure 2. I_Q Shutdown vs Temperature

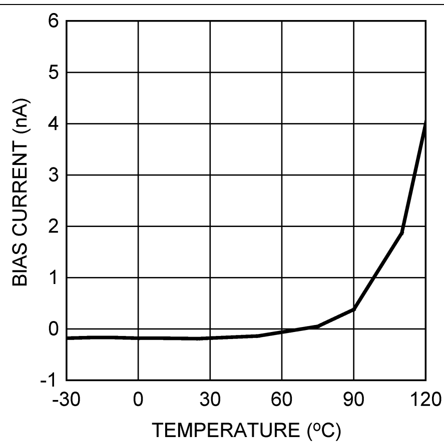


Figure 3. Feedback Bias Current vs Temperature

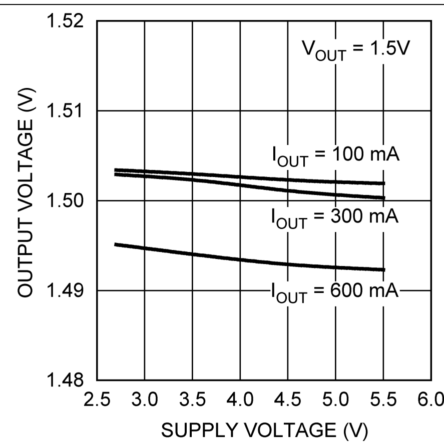


Figure 4. Output Voltage vs Supply Voltage

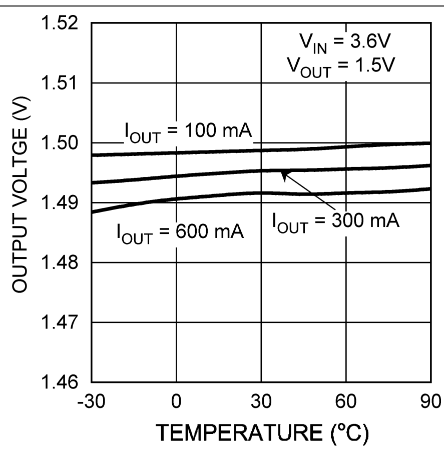


Figure 5. Output Voltage vs Temperature

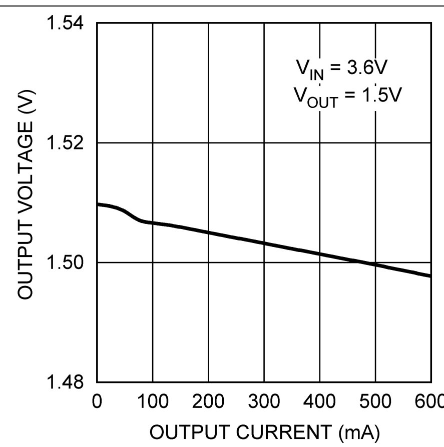


Figure 6. Output Voltage vs Output Current

Typical Characteristics (continued)

(unless otherwise stated: V_{IN} = 3.6 V, V_{OUT} = 1.5 V, T_A = 25°C)

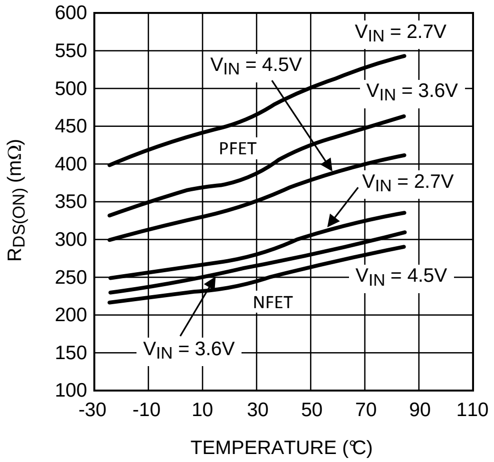


Figure 7. R_{DSON} vs Temperature

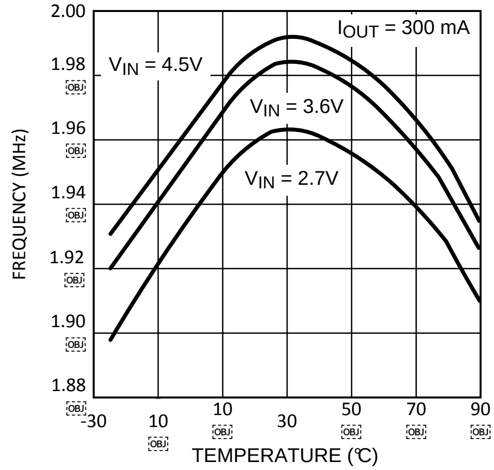
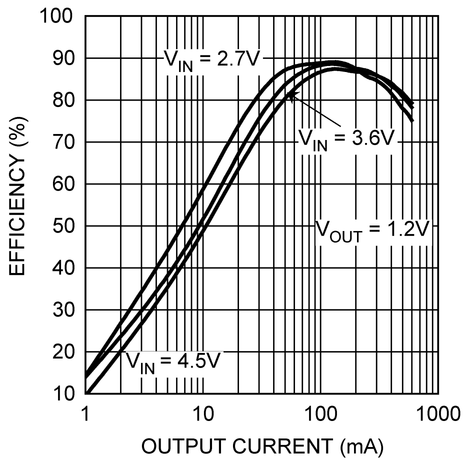
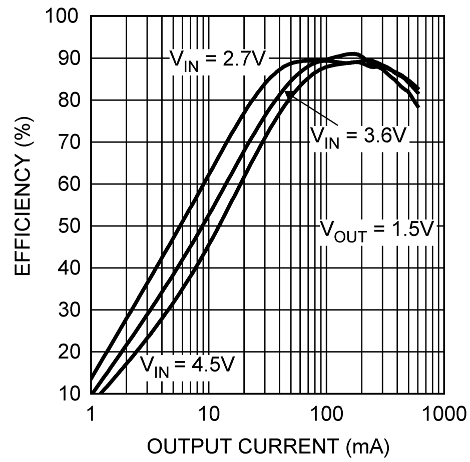


Figure 8. Switching Frequency vs Temperature



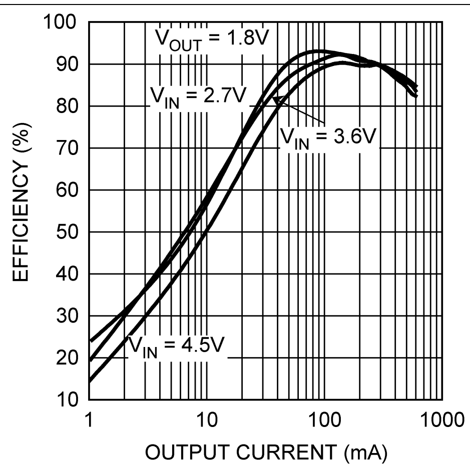
V_{OUT} = 1.2 V, L = 2.2 µH, DCR = 200 mΩ

Figure 9. Efficiency vs Output Current



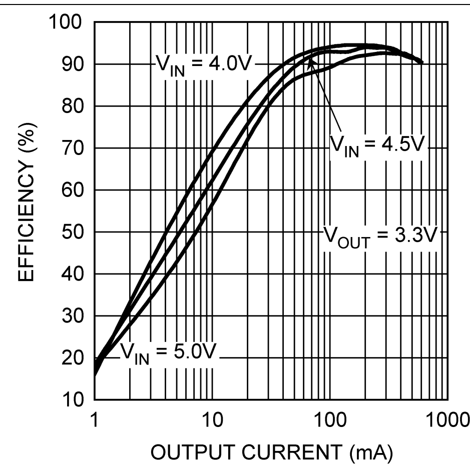
V_{OUT} = 1.5 V, L = 2.2 µH, DCR = 200 mΩ

Figure 10. Efficiency vs Output Current



V_{OUT} = 1.8 V, L = 2.2 µH, DCR = 200 mΩ

Figure 11. Efficiency vs Output Current



V_{OUT} = 3.3 V, L = 2.2 µH, DCR = 200 mΩ

Figure 12. Efficiency vs Output Current

Typical Characteristics (continued)

(unless otherwise stated: V_{IN} = 3.6 V, V_{OUT} = 1.5 V, T_A = 25°C)

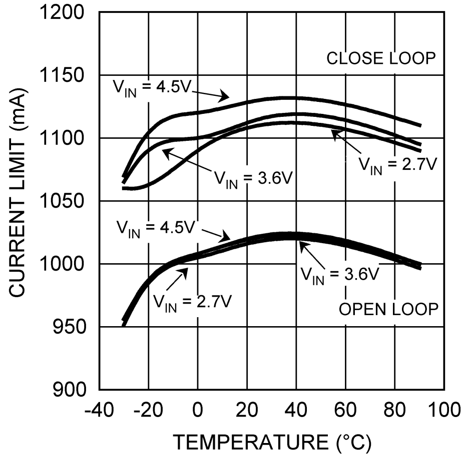


Figure 13. Open or Closed Loop Current Limit vs Temperature

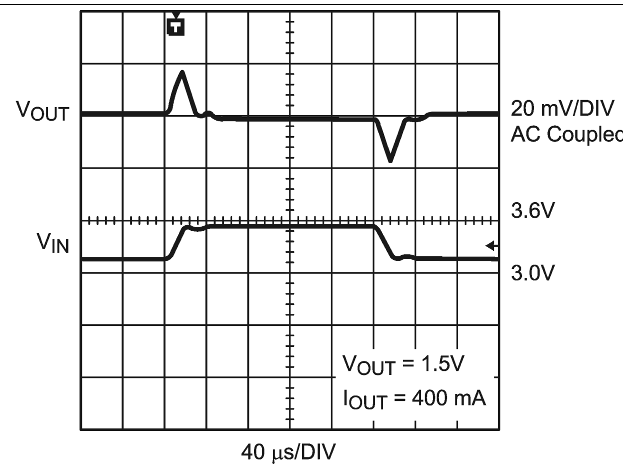


Figure 14. Line Transient Response

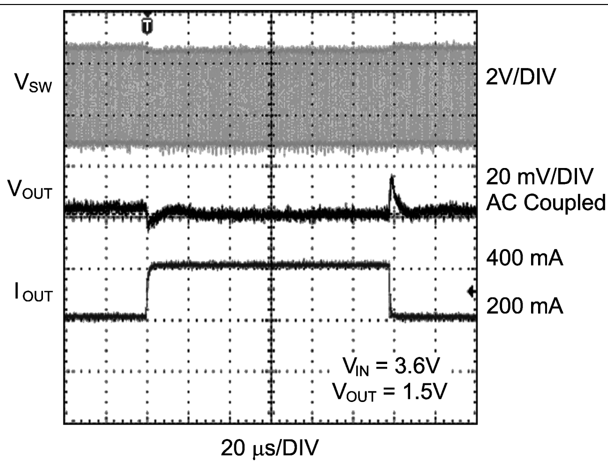
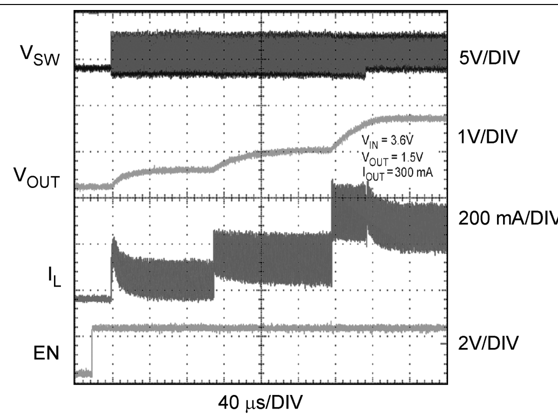
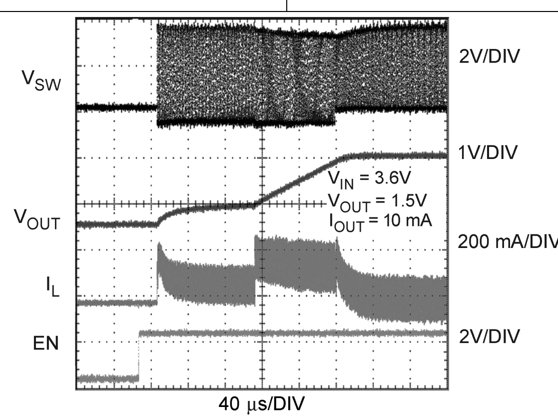


Figure 15. Load Transient



Output Current = 300 mA

Figure 16. Start-Up



Output Current = 10 mA

Figure 17. Start-Up

7 Detailed Description

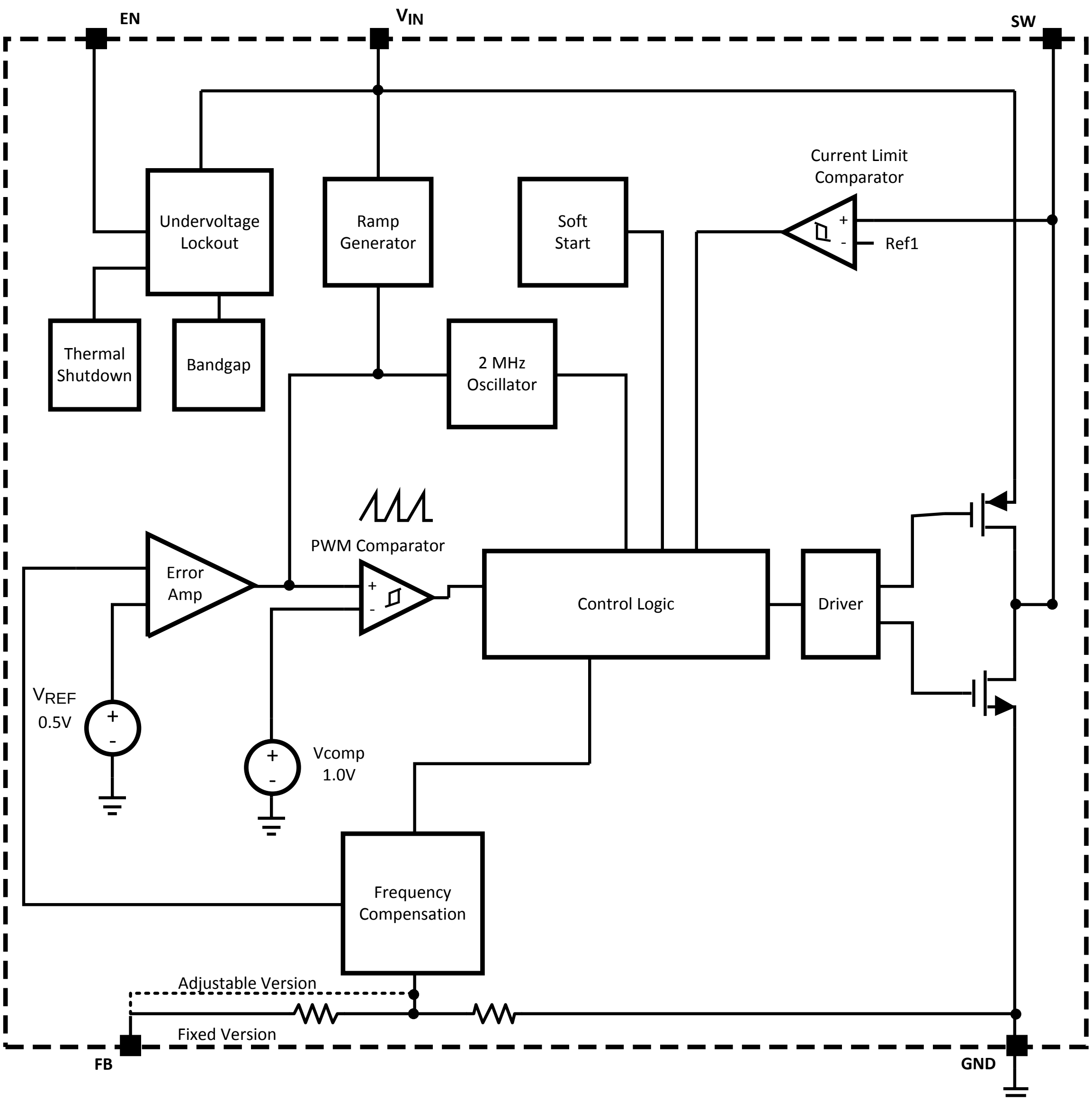
7.1 Overview

The LM3674, a high-efficiency, step-down, DC-DC switching buck converter, delivers a constant voltage from a single Li-Ion battery and input voltage rails from 2.7 V to 5.5 V to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, the LM3674 has the ability to deliver up to 600 mA depending on the input voltage, output voltage, ambient temperature, and the inductor chosen.

Additional features include soft-start, undervoltage protection, current overload protection, and thermal overload protection. As shown in *Typical Application Circuit*, only three external power components, C_{IN}, C_{OUT}, and L_1, are required for implementation.

The part uses an internal reference voltage of 0.5 V. It is recommended to keep the part in shutdown mode until the input voltage is 2.7 V or higher.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Circuit Operation

During the first portion of each switching cycle, the control block in the LM3674 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of:

$$\frac{V_{IN}-V_{OUT}}{L} \tag{1}$$

by storing energy in a magnetic field. During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of:

$$\frac{-V_{OUT}}{L} \tag{2}$$

The output filter stores charge when the inductor current is high, and releases it when the inductor current is low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch-on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

7.3.2 PWM Operation

During PWM operation, the converter operates as a voltage-mode controller with input voltage feed-forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed-forward inversely proportional to the input voltage is introduced.

While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle, the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch.

The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

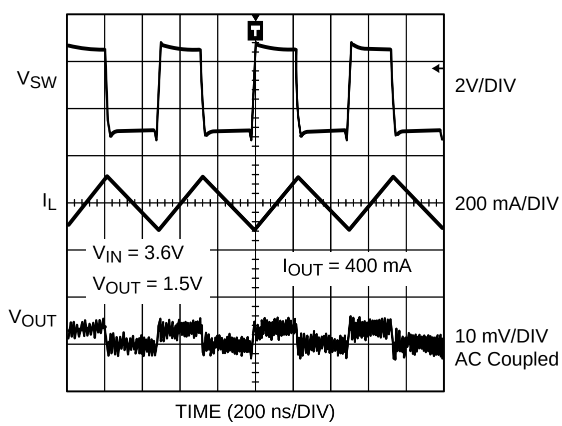


Figure 18. PWM Operation

Feature Description (continued)

7.3.2.1 Internal Synchronous Rectification

While in PWM mode, the LM3674 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

7.3.2.2 Current Limiting

A current limit feature allows the LM3674 to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1020 mA (typical). If the output is shorted to ground, then the device enters a timed current-limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, and thereby preventing runaway.

7.4 Device Functional Modes

There are two modes of operation depending on the current required: Pulse Width Modulation (PWM) and shutdown. The device operates in PWM mode throughout the I_{OUT} range. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 0.01 µA, typical). Additional features include soft-start, undervoltage protection, and current overload protection.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Soft-Start

The LM3674 has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft-start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.7 V. Soft-start is implemented by increasing switch current limit in steps of 70 mA, 140 mA, 280 mA, and 1020 mA (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with 10-µF output capacitor and a 300-mA load current is 350 µs and with a 10-mA load current is 240 µs.

8.1.2 Low-Dropout (LDO) Operation

The LM3674-ADJ can operate at 100% duty-cycle (no switching, PMOS switch completely on) for low-dropout support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty-cycle, the output voltage supply ripple is slightly higher, approximately 25 mV.

The minimum input voltage needed to support the output voltage is:

$$V_{IN,MIN} = I_{LOAD} \times (R_{DSON\ (P)} + R_{INDUCTOR}) + V_{OUT}$$

where:

- I_{LOAD} is load current
- $R_{DSON\ (P)}$ is drain-to-source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$ is inductor resistance (3)

8.2 Typical Applications

8.2.1 Typical Application for Fixed Voltage Configuration

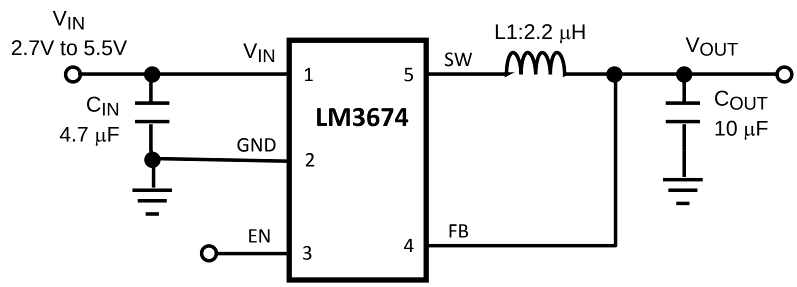


Figure 19. Fixed-Voltage Typical Application Circuit

8.2.1.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.6 V
Output voltage	1.5 V
Output current	300 mA

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

There are two main considerations when choosing an inductor:

- The inductor should not saturate.
- The inductor current ripple should be small enough to achieve the desired output voltage ripple.

Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of the application should be requested from the manufacturer. The minimum value of inductance to ensure good performance is 1.76 µH at I_{LIM} (typical) DC current over the ambient temperature range. Shielded inductors radiate less noise and should be preferred.

There are two methods to choose the inductor saturation current rating:

Method 1:

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as:

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE} \tag{4}$$

where $I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 \times L}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{f}\right)$

and

- I_{RIPPLE} is average-to-peak inductor current
- I_{OUTMAX} is maximum load current (600 mA)
- V_{IN} is maximum input voltage in application
- L is minimum inductor value including worst case tolerances (30% drop can be considered for method 1
- f is minimum switching frequency (1.6 MHz)
- V_{OUT} is output voltage (5)

Method 2:

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the maximum current limit of 1200 mA.

A 2.2-µH inductor with a saturation current rating of at least 1200 mA is recommended for most applications. The resistance of the inductor should be less than 0.3 Ω for good efficiency. Table 1 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor is suggested. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise toroidal inductor in the event that noise from low-cost bobbin models is unacceptable.

Table 1. Suggested Inductors and Their Suppliers

MODEL	VENDOR	DIMENSIONS L×W×H (mm)	D.C.R (maximum) (mΩ)
DO3314-222MX	Coilcraft	3.3 x 3.3 x 1.4	200
LPO3310-222MX	Coilcraft	3.3 x 3.3 x 1.0	150
ELL5GM2R2N	Panasonic	5.2 x 5.2 x 1.5	53
CDRH2D14NP-2R2NC	Sumida	3.2 x 3.2 x 1.55	94

8.2.1.2.2 Input Capacitor Selection

A ceramic input capacitor of 4.7 µF, 6.3 V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The minimum input capacitance to ensure good performance is 2.2 µF at 3-V DC bias; 1.5 µF at 5-V DC bias including tolerances and over ambient temperature range. The input filter capacitor supplies current to the PFET switch of the LM3674 in the first half of each cycle and reduces voltage ripple imposed on the input power source. The low equivalent series resistance (ESR) of a ceramic capacitor provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times f \times I_{OUTMAX} \times V_{IN}} \quad \text{The worst case is when } V_{IN} = 2 \times V_{OUT} \tag{6}$$

8.2.1.2.3 Output Capacitor Selection

A ceramic output capacitor of 10 µF, 6.3 V is sufficient for most applications. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC-bias characteristics vary from manufacturer to manufacturer and DC-bias curves should be requested from them as part of the capacitor selection process.

The minimum output capacitance to ensure good performance is 5.75 µF at 1.8 V DC bias including tolerances and over ambient temperature range. The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes, and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and by the R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed as:

$$V_{PP\text{-}C} = \frac{I_{ripple}}{f \times 4 \times C} \tag{7}$$

Voltage peak-to-peak ripple due to ESR:

$$V_{OUT} = V_{PP\text{-}ESR} = I_{PP} * R_{ESR} \tag{8}$$

Because these two components are out of phase, the root mean squared (rms) value can be used to get an approximate value of peak-to-peak ripple.

Voltage peak-to-peak ripple, rms:

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^2 + V_{PP\text{-}ESR}^2} \tag{9}$$

Note that the output ripple is dependent on the current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency-dependent (as well as temperature-dependent); make sure the value used for calculations is at the switching frequency of the part.

Table 2. Suggested Capacitors and Their Suppliers

MODEL	TYPE	VENDOR	VOLTAGE RATING (V)	CASE SIZE [Inch (mm)]
10 µF for C_{OUT}				
GRM21BR60J106K	Ceramic, X5R	Murata	6.3	0805 (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3	0805 (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3	0805 (2012)
4.7 µF for C_{IN}				
GRM21BR60J475K	Ceramic, X5R	Murata	6.3	0805 (2012)
JMK212BJ475K	Ceramic, X5R	Taiyo-Yuden	6.3	0805 (2012)
C2012X5R0J475K	Ceramic, X5R	TDK	6.3	0805 (2012)

8.2.1.3 Application Curves

Table 3. Related Plots

PLOT TITLE	FIGURE
Output Voltage vs Supply Voltage	Figure 4
Output Voltage vs Temperature	Figure 5
Output Voltage vs Output Current	Figure 6
Efficiency vs Output Current	Figure 9
Efficiency vs Output Current	Figure 10
Efficiency vs Output Current	Figure 11
Efficiency vs Output Current	Figure 12
Line Transient Response	Figure 14
Load Transient	Figure 15
Start-Up	Figure 16
Start-Up	Figure 17

8.2.2 Typical Application Circuit for Adjustable Voltage Option

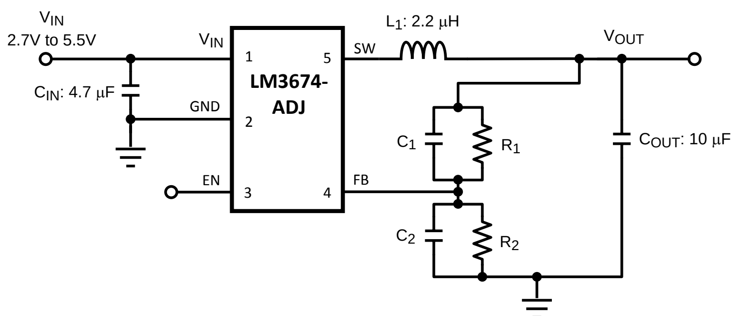


Figure 20. Typical Application Circuit for Adjustable Voltage Option Schematic

8.2.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	1.5 V

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Output Voltage Selection for Adjustable (LM3674-ADJ)

The output voltage of the adjustable parts can be programmed through the resistor network connected from V_{OUT} to FB then to GND. V_{OUT} will be adjusted to make FB equal to 0.5 V. The resistor from FB to GND (R2) should be 200 kΩ to keep the current drawn through this network small but large enough that it is not susceptible to noise. If R_2 is 200 kΩ, and given the V_{FB} is 0.5 V, then the current through the resistor feedback network will be 2.5 µA. The output voltage formula is:

$$V_{OUT} = V_{FB} * \left(\frac{R_1}{R_2} + 1\right)$$

where:
- V_{OUT} = Output voltage (V)
- V_{FB} = Feedback voltage (0.5 V typical)
- R_1 = Resistor from V_{OUT} to FB (Ω)
- R_2 = Resistor from FB to GND (Ω) (10)

For any output voltage greater than or equal to 1.0 V, a frequency zero must be added at 45 kHz for stability. The formula is:

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times 45\text{ kHz}} \quad (11)$$

For output voltages greater than or equal to 2.5 V, a pole must also be placed at 45 kHz as well. If the pole and zero are at the same frequency the formula for calculation of C2 is:

$$C_2 = \frac{1}{2 \times \pi \times R_2 \times 45\text{ kHz}} \quad (12)$$

The formula for location of zero and pole frequency created by adding C1,C2 are given below. It can be seen that by adding C1, a zero as well as a higher frequency pole is introduced.

$$Fz = \frac{1}{(2 * \pi * R1 * C1)} \quad Fp = \frac{1}{2 * \pi * (R1 \| R2) * (C1+C2)} \quad (13)$$

See Table 4.

Table 4. Adjustable LM3674 Configurations for Various V_{OUT}

VOUT (V)	R1 (kΩ)	R2 (kΩ)	C1 (pF)	C2 (pF)	L (µH)	C_{IN} (µF)	C_{OUT} (µF)
1.0	200	200	18	None	2.2	4.7	10
1.1	191	158	18	None	2.2	4.7	10
1.2	280	200	12	None	2.2	4.7	10
1.5	357	178	10	None	2.2	4.7	10
1.6	442	200	8.2	None	2.2	4.7	10
1.7	432	178	8.2	None	2.2	4.7	10
1.8	464	178	8.2	None	2.2	4.7	10
1.875	523	191	6.8	None	2.2	4.7	10
2.5	402	100	8.2	None	2.2	4.7	10
2.8	464	100	8.2	33	2.2	4.7	10
3.3	562	100	6.8	33	2.2	4.7	10

8.2.2.3 Application Curves

Table 5. Related Plots

PLOT TITLE	FIGURE
Output Voltage vs Supply Voltage	Figure 4
Output Voltage vs Temperature	Figure 5
Output Voltage vs Output Current	Figure 6
Efficiency vs Output Current	Figure 9
Efficiency vs Output Current	Figure 10
Efficiency vs Output Current	Figure 11
Efficiency vs Output Current	Figure 12
Line Transient Response	Figure 14
Load Transient	Figure 15
Start-Up	Figure 16
Start-Up	Figure 17

9 Power Supply Recommendations

The LM3674 requires a single supply input voltage. This voltage can range between 2.7 V to 5.5 V and be able to supply enough current for a given application.

10 Layout

10.1 Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter device, resulting in poor regulation or instability.

Good layout for the LM3674 can be implemented by following a few simple design rules, as illustrated in Figure 21.

1. Place the LM3674, inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must by given to place the input filter capacitor very close to the V_{IN} and GND pin.
2. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the LM3674 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3674 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. Connect the ground pins of the LM3674, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3674 by giving it a low-impedance ground connection.
4. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
5. Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components. The voltage feedback trace must remain close to the LM3674 circuit and should be direct but should be routed opposite to noisy components. This reduces the EMI radiated onto the voltage feedback trace of the DC-DC converter. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner for the adjustable part it is desired to have the feedback dividers on the bottom layer.
6. Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks

Layout Guidelines (continued)

and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (because this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise by using low-dropout linear regulators.

10.2 Layout Example

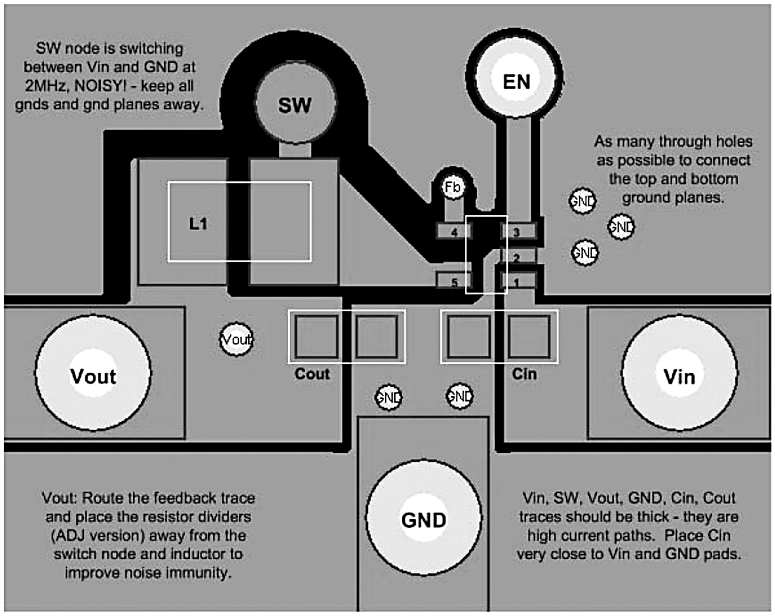


Figure 21. Board Layout Design Rules for the LM3674

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3674MF-1.2/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	SLRB	Samples
LM3674MF-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	SLSB	Samples
LM3674MF-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	SLHB	Samples
LM3674MF-1.875/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	SNNB	Samples
LM3674MF-2.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	SLZB	Samples
LM3674MF-ADJ	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-30 to 85	SLTB	
LM3674MF-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	SLTB	Samples
LM3674MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	SLRB	Samples
LM3674MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	SLHB	Samples
LM3674MFX-1.875/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	SNNB	Samples
LM3674MFX-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-30 to 85	SLTB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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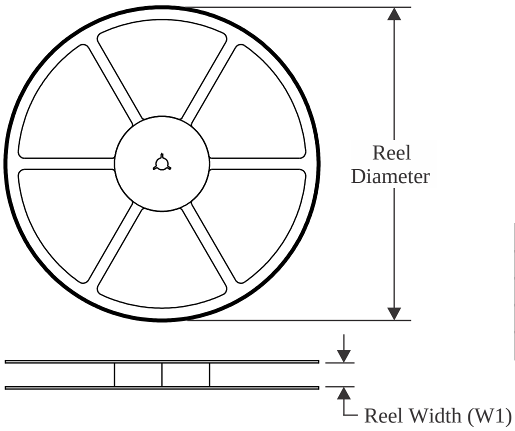
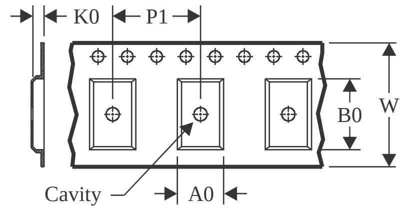
TAPE AND REEL INFORMATION

REEL DIMENSIONS

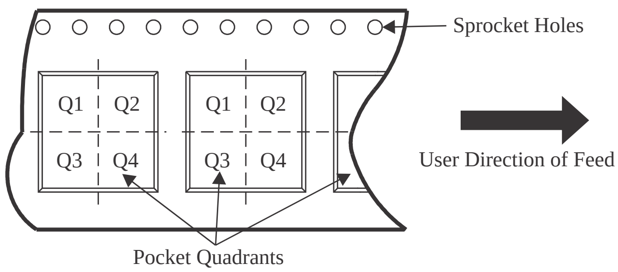


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

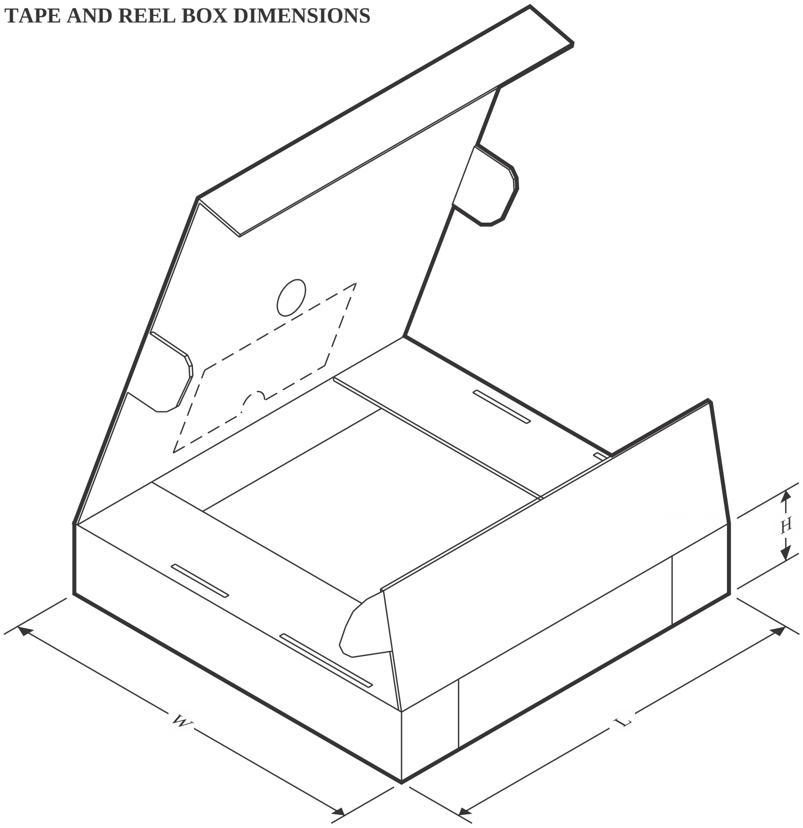
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

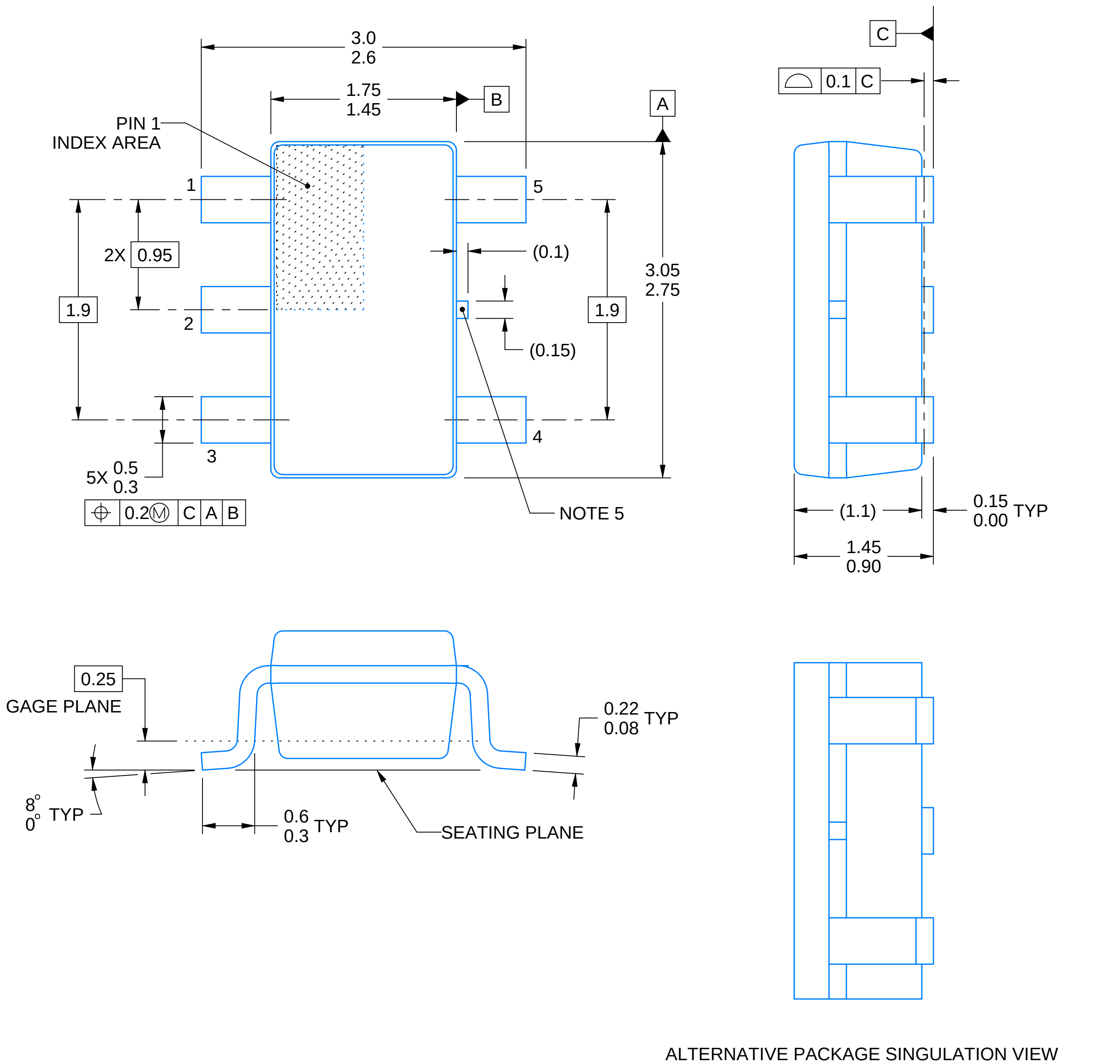
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3674MF-1.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3674MF-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3674MF-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3674MF-1.875/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3674MF-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3674MF-ADJ	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3674MF-ADJ/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3674MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3674MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3674MFX-1.875/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3674MFX-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3674MF-1.2/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3674MF-1.5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3674MF-1.8/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3674MF-1.875/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3674MF-2.8/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3674MF-ADJ	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3674MF-ADJ/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LM3674MFX-1.2/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM3674MFX-1.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM3674MFX-1.875/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LM3674MFX-ADJ/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0



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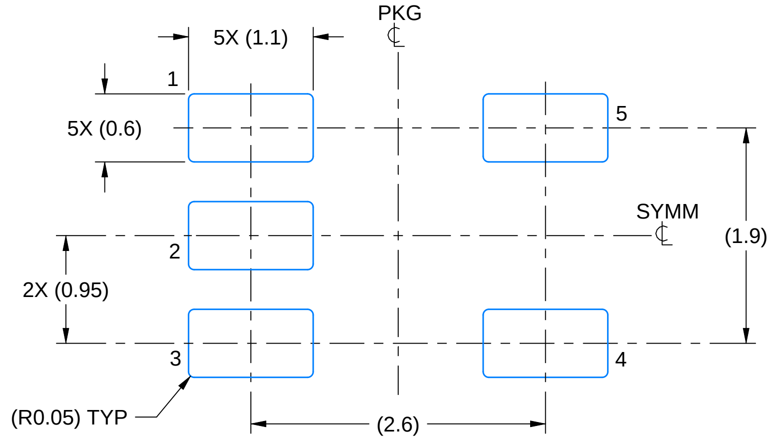
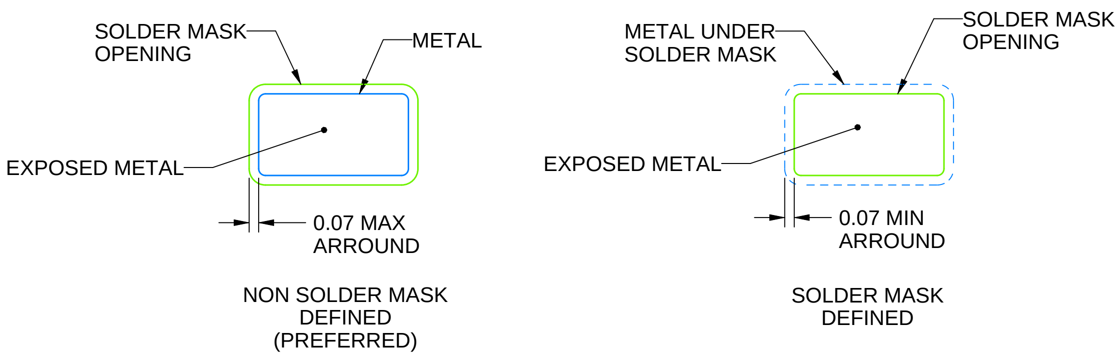
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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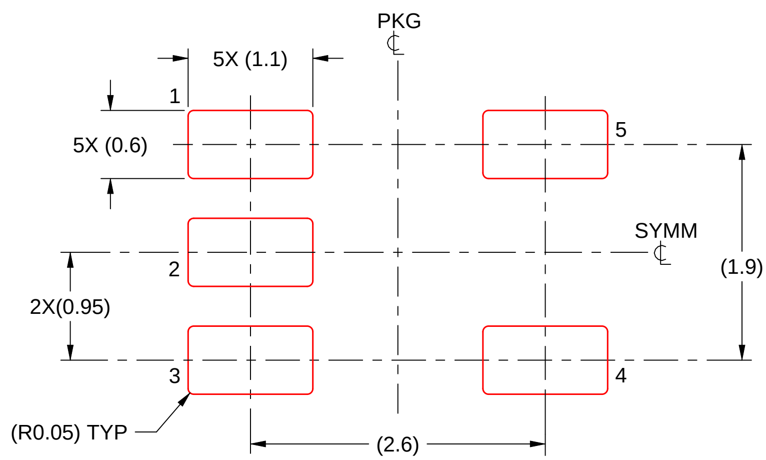
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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