TEXAS INSTRUMENTS
LM74721-Q1
SNOSDC2B – SEPTEMBER 2021 – REVISED JULY 2022

LM74721-Q1 *TVS Less* Low IQ Automotive Reverse Battery Protection Ideal Diode Controller with Active Rectification

1 Features

- AEC-Q100 qualified with the following results
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- 3-V to 65-V input range
- Reverse input protection down to –33 V
- Integrated VDS clamp for Input TVS less operation for ISO7637 pulse suppression
- Low quiescent current 35 µA (max) in operation
- Low 3.3-µA (max) shutdown current (EN = Low)
- Ideal diode operation with 17-mV A to C forward voltage drop regulation
- Drives external back-to-back N-Channel MOSFETs
- Integrated 30-mA boost regulator
- Fast response to reverse current blocking: 0.5 µs
- Active rectification up to 100 kHz
- Adjustable overvoltage protection
- Available in space saving 12-pin WSON package
- Pin-to-pin compatible with LM74720-Q1

2 Applications

- Automotive battery protection
  - ADAS domain controller
  - Camera, radar ECUs
  - Premium audio amplifier
  - Head-up display

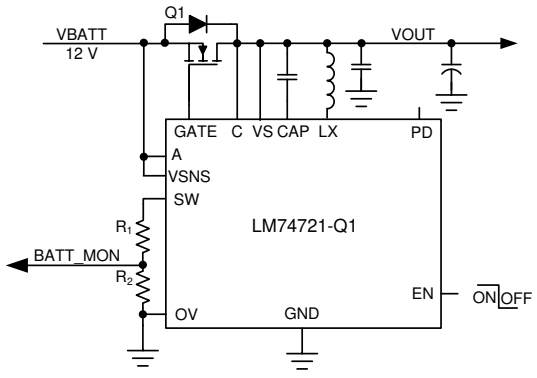
3 Description

The LM74721-Q1 ideal diode controller drives and controls external back to back N-Channel MOSFETs to emulate an ideal diode rectifier with power path ON and OFF control and overvoltage protection. The wide input supply of 3 V to 65 V allows protection and control of 12-V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to –33-V DC. An integrated ideal diode controller (GATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. Integrated VDS clamp feature enables input TVS less system designs for automotive ISO7637 pulse suppression. A strong boost regulator with fast turn ON and OFF comparators ensures robust and efficient MOSFET switching performance during automotive testing such as ISO16750 or LV124, where an ECU is subjected to input short interruptions and AC superimpose input signals up to 100-kHz frequency. Low Quiescent Current 35 µA (maximum) in operation enables always ON system designs. With a second MOSFET in the power path, the device allows load disconnect control using EN pin. Quiescent current reduces to 3.3 µA (maximum) with EN low. The device features an adjustable overvoltage cutoff protection feature for load dump protection.

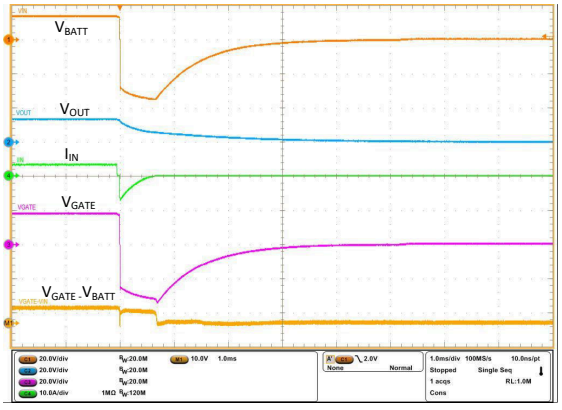
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM74721-Q1	WSON (12)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Low IQ TVS Less Ideal Diode for 12-V Battery Powered Automotive Applications



TVS Less ISO7637-2 Pulse 1 Performance

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2022) to Revision B (July 2022)	Page
• Changed status from "Advance Information" to Production Data"	1

Changes from Revision * (September 2021) to Revision A (February 2022)	Page
• Updated the data sheet title	1
• Updated the *Load Disconnect Switch Control (PD)* description	13

5 Pin Configuration and Functions

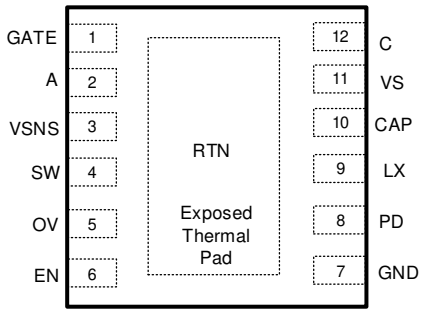


Figure 5-1. WSON 12-Pin DRR Transparent Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	LM74721-Q1 DRR-12 (WSON)		
GATE	1	O	Diode controller gate drive output. Connect to the GATE of the external MOSFET.
A	2	I	Anode of the ideal diode. Connect to the source of the external MOSFET.
VSNS	3	I	Voltage sensing input
SW	4	I	Voltage sensing disconnect switch terminal. VSNS and SW are internally connected through a switch. Use SW as the top connection of the battery sensing or OV resistor ladder network. When EN is pulled low, the switch is OFF, disconnecting the resistor ladder from the battery line, thereby cutting off the leakage current. If the internal disconnect switch between VSNS and SW is not used, then short them together and connect to C pin.
OV	5	I	Adjustable overvoltage threshold input. Connect a resistor ladder across SW to OV terminal. When the voltage at OV exceeds the overvoltage cutoff threshold, then the PD is pulled low turning OFF the HSFET. PD is driven high when the sense voltage goes below the OV falling threshold.
EN	6	I	EN Input. Connect to A or C pin for always ON operation. In this mode, the device consumes an IQ of 35 µA (maximum) that can be driven externally from a micro controller I/O. Pulling this pin low below 0.5 V enters the device in low Iq shutdown mode.
GND	7	G	Connect to the system ground plane.
PD	8	O	Pull down connection for the external HSFET. Connect to the GATE of the external FET. Leave PD pin floating if the load disconnect FET is not used.
LX	9	I	Switch node of the internal boost regulator. This node must be kept small on the PCB for good performance and low EMI. Connect the boost inductor between this pin and the DRAIN connection of the external FET.
CAP	10	O	Boost Regulator Output. This pin is used to provide a drive voltage to the gate driver of the ideal diode stage as well as drive supply for the HSFET. Connect a 1-µF capacitor between this pin and the VS pin.
VS	11	I	Supply voltage pin. Place 0.1-µF capacitor from VS pin to GND.
C	12	I	Cathode of the ideal diode. Connect to the DRAIN of the external MOSFET. The voltage sensed at this pin is used to control the external MOSFET GATE. This pin must be locally bypassed with at least 1 µF.
RTN	Thermal Pad	—	Leave exposed pad floating. Do not connect to GND plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	A to GND	– (V_{CLAMP} + 1)	70	V
Input Pins	VS, C to GND	–0.3	70	
Input Pins	VSNS, SW, EN, OV to GND, $V_{(A)}$ > 0 V	–0.3	70	
Input Pins	VSNS, SW, EN, OV to GND, $V_{(A)}$ ≤ 0 V	$V_{(A)}$	(70 + $V_{(A)}$)	
Input Pins	C to GND, $V_{(A)}$ ≤ 0 V	–1	(70 + $V_{(A)}$)	
Input Pins	RTN to GND	– (V_{CLAMP} + 1)	0.3	
Input Pins	I_{VSNS}, I_{SW}	–1	10	mA
Input Pins	I_{EN}, I_{OV}, $V_{(A)}$ > 0 V	–1		
Input Pins	I_{EN}, I_{OV}, $V_{(A)}$ ≤ 0 V	Internally limited		
Output Pins	CAP to C	–0.3	15.9	V
Output Pins	CAP to A	–0.3	V_{CLAMP} + 15.9	
Output Pins	GATE to A	–0.3	15	
Output Pins	LX, CAP, PD to GND	–0.3	85	
Output to Input Pins	C to A	–5	V_{CLAMP}	
Operating junction temperature, T_j (2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (GATE, EN, GND, C)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	A to GND	–60		65	V
	VS, C to GND			65	
	EN to GND	–60		65	
External capacitance	A	0.1			µF
	CAP to VS	1			
External Inductor	LX	100			µH
External MOSFET max V_{DS} rating		60			V
External MOSFET max V_{GS} rating	GATE to A	15			

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature range(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC(1)		LM74721-Q1 DRR (WSON) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32.7	°C/W
$R_{\theta JC}$	Junction-to-case (botton) thermal resistance	6.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 1 µF, $V_{(EN)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_A, $V_{(VS)}$ SUPPLY VOLTAGE						
V_{CLAMP}	$V_{(C–A)}$ clamp voltage		34.5		43	V
$V_{(A\ POR)}$	VA POR Rising threshold		3.1	3.4	3.85	V
	VA POR Falling threshold		2.2	2.6	2.9	
$V_{(VS)}$	Minimum Voltage at VS				3	V
	VS POR Rising		2.58	2.8	2.95	
	VS POR Falling		2.35	2.6	2.85	
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN)}$ = 0 V		2	3.3	µA
$I_{(Q)}$	Total System Quiescent Current	$V_{(EN)}$ = 2 V, Active Rectifier Controller In Regulation, –40°C ≤ T_J ≤ +85°C		27	32	
		$V_{(EN)}$ = 2 V, Active Rectifier Controller In Regulation, –40°C ≤ T_J ≤ +125°C		27	35	
ENABLE INPUT						
$V_{(EN\_IH)}$	Enable input high threshold				2	V
$V_{(EN\_IL)}$	Enable input low threshold		0.5	0.85	1.2	
$V_{(EN\_Hys)}$	Enable Hysteresis			485		mV
$I_{(EN)}$	Enable sink current	$V_{(EN)}$ = 12 V		55	155	nA
V_{ANODE} to $V_{CATHODE}$						
$V_{(AC\_REG)}$	Regulated Forward $V_{(AC)}$ Threshold		9	16.4	22.7	mV
$V_{(AC\_FWD)}$	$V_{(AC)}$ threshold from RCB to Forward conduction		75	105	140	
$V_{(AC\_REV)}$	$V_{(AC)}$ threshold for reverse current blocking		–12	–5.65	–1.3	
GATE DRIVE						

6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 1 µF, $V_{(EN)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(GATE)}$ - $V_{(A)}$		3V < $V_{(VS)}$ < 65V	9.5		13	V
$I_{(GATE\_Pull\ down)}$	Peak Pulldown current	$V_{(A)}$ – $V_{(C)}$ = –20 mV, $V_{(GATE)}$ – $V_{(A)}$ = 100 mV		2.5		A
$I_{(GATE)}$	Regulation max sink current	$V_{(A)}$ – $V_{(C)}$ = 0 V, $V_{(GATE)}$ – $V_{(A)}$ = 5 V	14	26	39	µA
R_{GATE}	GATE pulldown resistance	$V_{(A)}$ – $V_{(C)}$ = –20 mV, $V_{(GATE)}$ – $V_{(A)}$ = 100 mV		1.2		Ω
BOOST REGULATOR CHARGE PUMP						
$V_{(CAP)}$ – $V_{(c)}$	Boost output rising threshold			13	15.5	V
	Hysteresis			1.1		
$I_{(CAP)}$	Boost load capacity	$V_{(CAP)}$ – $V_{(VS)}$ = 7.5 V		29		mA
$I_{(LX)}$	Peak inductor current limit threshold	$V_{(VS)}$ = 12 V	110	140	170	mA
		$V_{(VS)}$ = 3 V			210	
$R_{(LX)}$	Low side switch On-Resistance		1.3	2.7	5.1	Ω
BATTERY SENSING (VSNS, SW) AND OVER VOLTAGE DETECTION (OVP, PD)						
$R_{(SW)}$	Battery sensing disconnect switch resistance		104	226	430	Ω
$V_{(OVR)}$	Overvoltage threshold input, rising		1.13	1.231	1.33	V
$V_{(OVF)}$	Overvoltage threshold input, falling		1.03	1.125	1.215	
$V_{(OV\_Hys)}$	OV Hysteresis			110		mV
$I_{(OV)}$	OV Input leakage current	0 V < $V_{(OV)}$ < 5 V		50	110	nA
$I_{(PD\_SRC)}$	Pullup current	3V < V_S < 65V	43	50	60	µA
$I_{(PD\_SINK)}$	Peak Pulldown current	$V_{(OV)}$ > $V_{(OVR)}$	55	88	117	mA
	DC Pulldown current		7	10	14	
CATHODE						
$I_{(C)}$	CATHODE sink current	$V_{(A)}$ = 12 V, $V_{(A)}$ – $V_{(C)}$ = –100 mV		9.4	15	µA
		$V_{(A)}$ = –14 V, $V_{(C)}$ = 14 V		10.6	18	

6.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(A)}$ = $V_{(VS)}$ = 12 V, $C_{(CAP)}$ = 1 µF, $V_{(EN)}$ = 2 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{A\_POR(DLY)}$	A (low to high) to GATE Turn-On delay	$V_{(A)}$ ↑ $V_{(A\_POR)}$ to $V_{(GATE-A)}$ > 5V, $C_{(GATE-A)}$ = 10 nF			200	µs
$t_{Reverse\ delay}$	Reverse voltage detection to Gate Turn-Off delay	$V_{(A)}$ – $V_{(C)}$ = +30 mV to –100 mV, $V_{(GATE-A)}$ <1V, $C_{(GATE-A)}$ = 10 nF		0.47	0.81	
$t_{Forward\ recovery}$	Forward voltage detection to Gate Turn-On delay	$V_{(A)}$ – $V_{(C)}$ = –100 mV to 700 mV, $V_{(GATE-A)}$ >5V, $C_{(GATE-A)}$ = 10 nF		1.9	2.9	
$t_{EN\_OFF(DLY)PD}$	EN to PD Delay	EN ↓ to PD ↓		6.5	12	
$t_{OV\_OFF(DLY)PD}$	OV to PD Deglitch	OV ↑ to PD ↓		0.9	1.5	
t_{PD_Pk}	Peak Pulldown duration	$I_{(PD\_SINK,Pk)}$ ↑ to $I_{(PD\_SINK,DC)}$ ↓	11	38	65	

6.7 Typical Characteristics

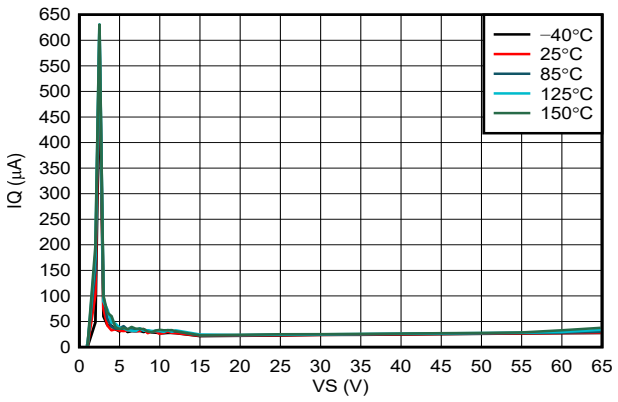


Figure 6-1. Operating Quiescent Current vs Supply Voltage

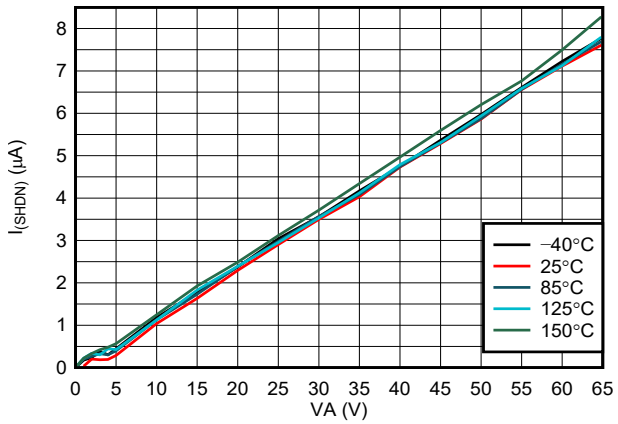


Figure 6-2. Shutdown Supply Current vs Supply Voltage

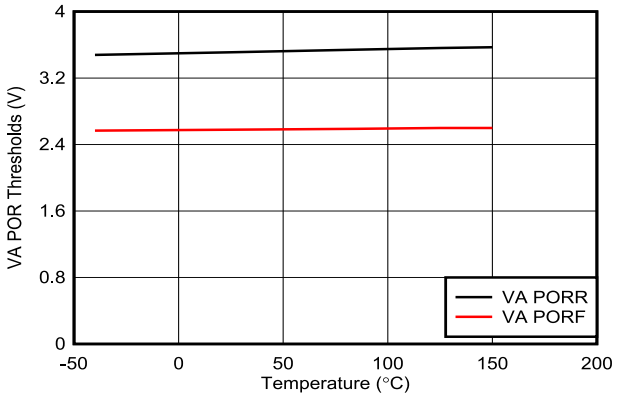


Figure 6-3. VA POR Threshold vs Temperature

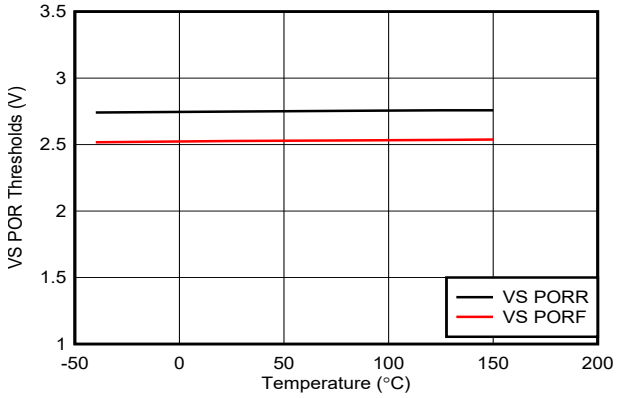


Figure 6-4. VS POR Threshold vs Temperature

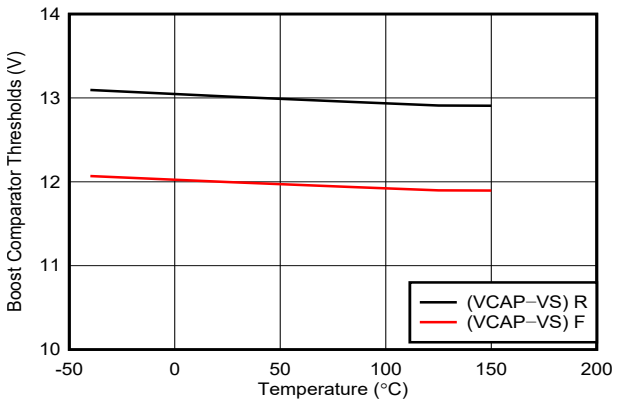


Figure 6-5. Boost Comparator Threshold vs Temperature

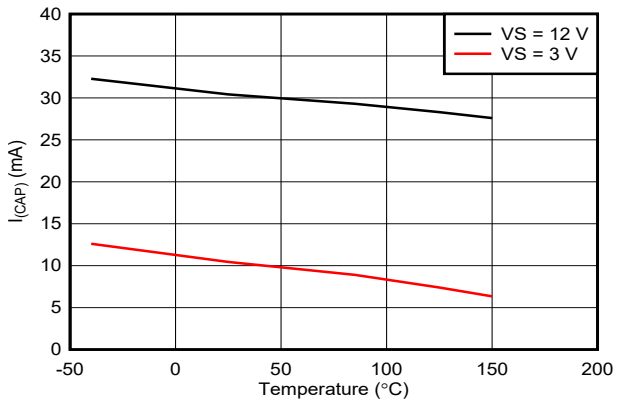


Figure 6-6. Boost Loading Capacity vs Temperature

6.7 Typical Characteristics (continued)

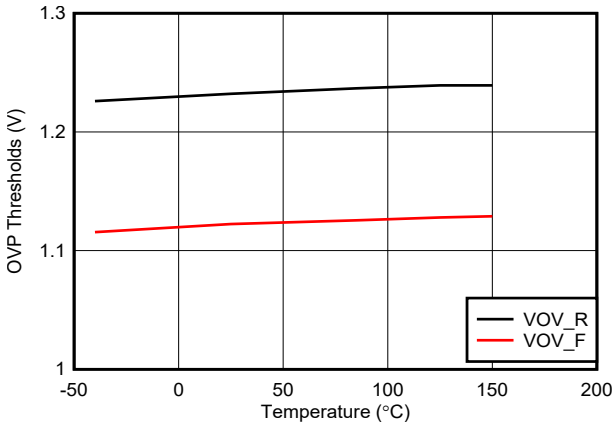


Figure 6-7. OV Threshold vs Temperature

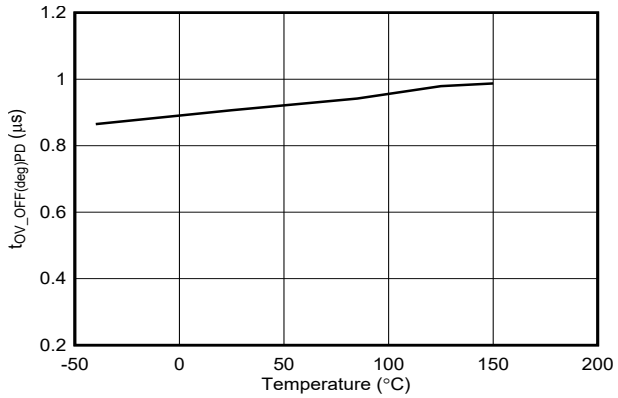


Figure 6-8. PD Turn-off Delay During OV

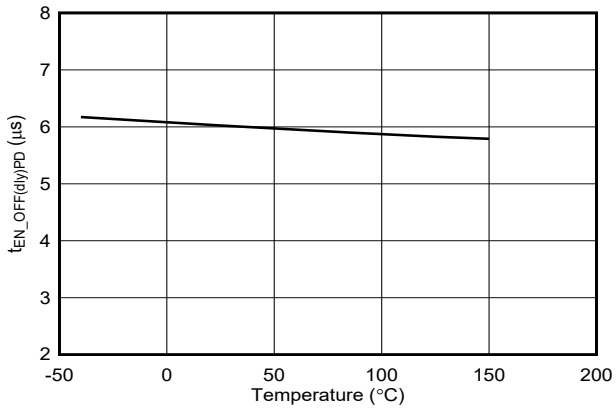


Figure 6-9. PD Turn-off Delay During EN

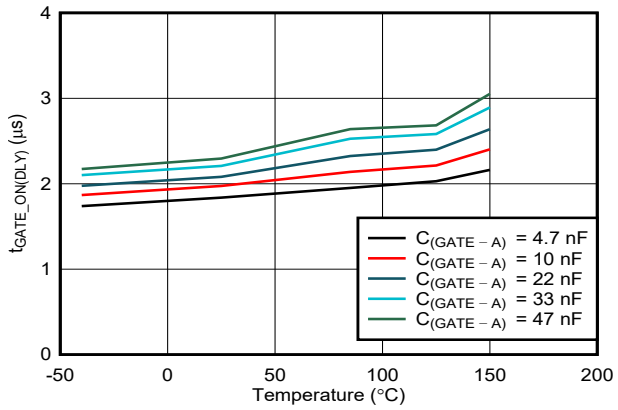


Figure 6-10. Forward Turn-on Delay vs Temperature

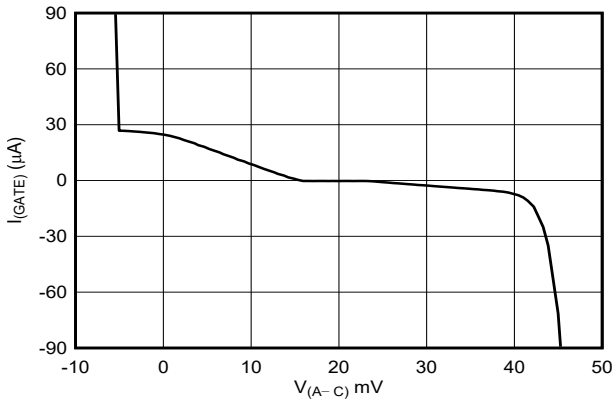


Figure 6-11. Gate Current vs Forward Voltage Drop

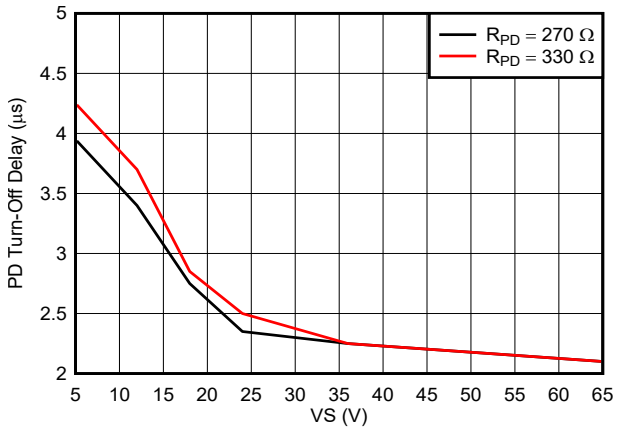


Figure 6-12. PD Turn-off Delay vs Supply Voltage

6.7 Typical Characteristics (continued)

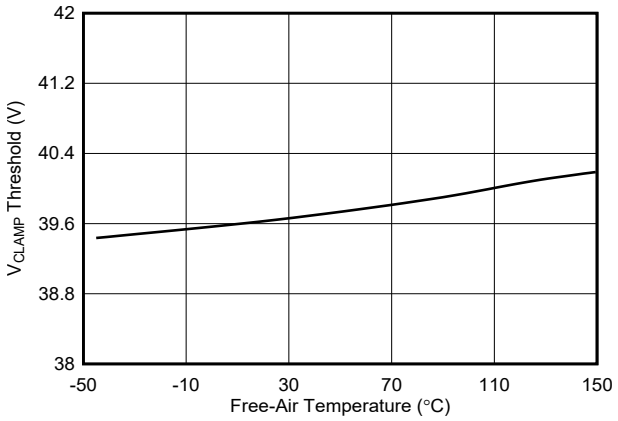


Figure 6-13. V_{CLAMP} vs Temperature

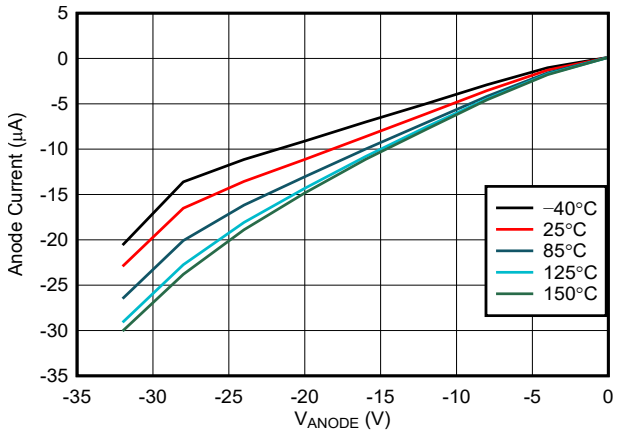


Figure 6-14. Anode Leakage Current vs Reverse Anode Voltage

7 Parameter Measurement Information

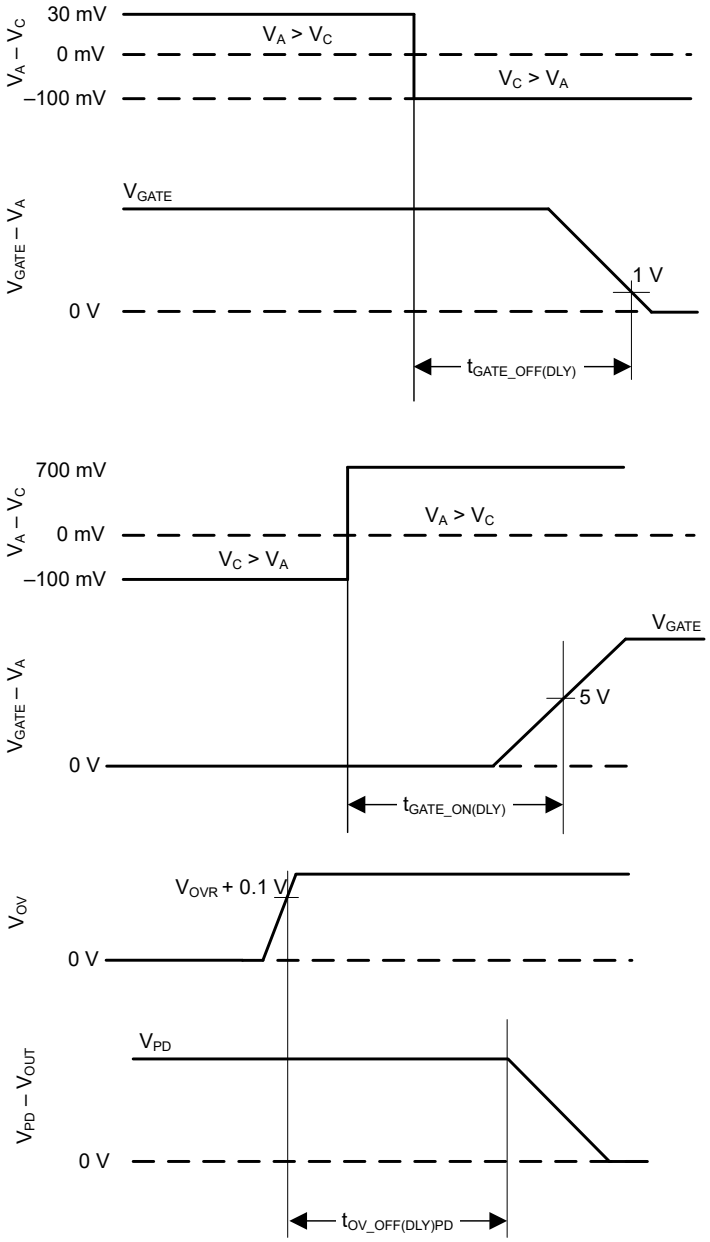


Figure 7-1. Timing Waveforms

8 Detailed Description

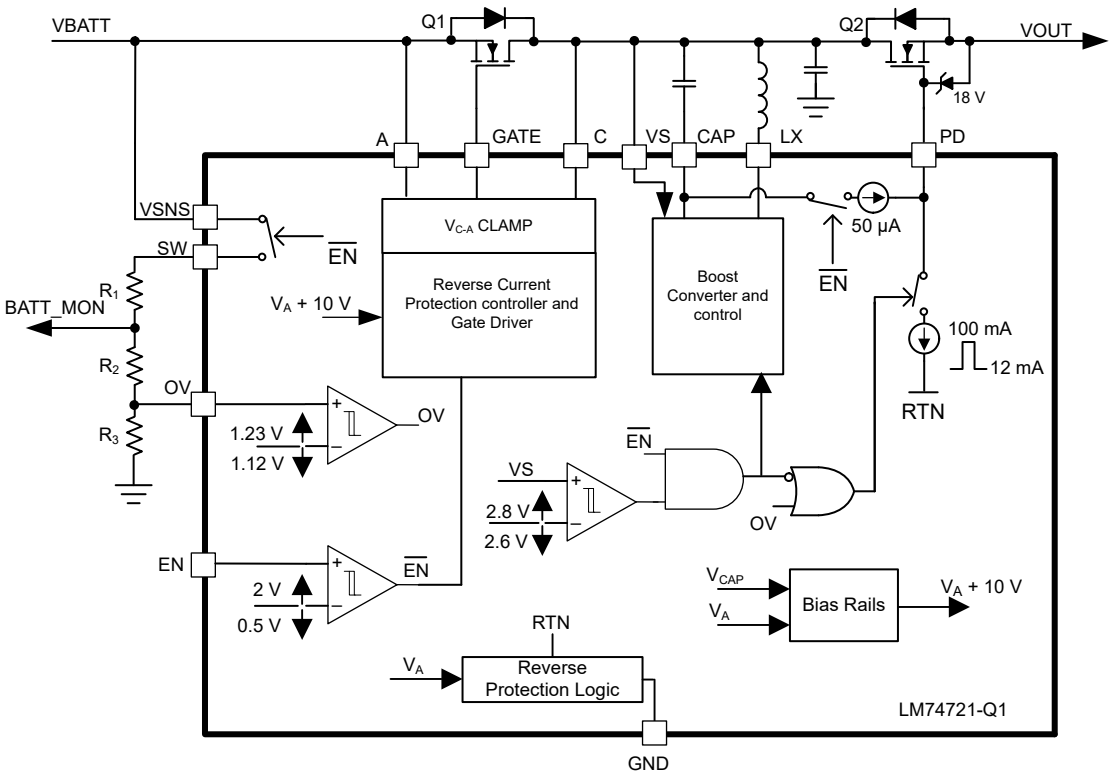
8.1 Overview

The LM74721-Q1 ideal diode controller drives and controls external N-Channel MOSFET to emulate an ideal diode rectifier. The wide input supply of 3 V to 65 V allows protection and control of 12-V automotive battery powered ECUs. IQ during operation (EN = High) is < 35 µA and < 3.3 µA during shutdown mode (EN = Low). The device can withstand and protect the loads from negative supply voltages down to –33-V DC. Integrated VDS clamp feature enables input TVS less system designs for automotive ISO7637 pulse suppression. An integrated ideal diode controller (GATE) drives the first MOSFET to replace a Schottky diode for reverse input protection and output voltage holdup. A strong 30-mA boost regulator and short turn ON and turn OFF delay times of comparator ensures fast transient response, ensuring robust and efficient MOSFET switching performance during automotive testing, such as ISO16750 or LV124, where an ECU is subjected to input short interruptions and AC superimpose input signals up to 100-kHz frequency.

The LM74721-Q1 controls the GATE of the MOSFET to regulate the forward voltage drop at 17 mV. The linear regulation scheme in these devices enables graceful control of the GATE voltage and turns off of the MOSFET during a reverse current event and ensures zero DC reverse current flow.

Low quiescent current (< 35 µA) in operation enables always ON system designs. With a second MOSFET in the power path, the device allows load disconnect control using EN pin. Quiescent current reduces to < 3.3 µA with EN low.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reverse Battery Protection (A, C, GATE)

A, C, GATE comprises of ideal diode stage. Connect the Source of the external MOSFET to A, Drain to C and Gate to GATE pin. The LM74721-Q1 has integrated reverse input protection down to –33 V.

In LM74721-Q1 the voltage drop across the MOSFET is continuously monitored between the A and C pins, and the GATE to A voltage is adjusted as needed to regulate the forward voltage drop at 17 mV (typical) for LM74721-Q1. This closed loop regulation scheme enables graceful turn-off of the MOSFET during a

reverse current event and ensures zero DC reverse current flow. This scheme ensures robust performance during slow input voltage ramp down tests. Along with the linear regulation amplifier scheme, the LM74721-Q1 also integrates a fast reverse voltage comparator. When the voltage drop across A and C reaches $V_{(AC\_REV)}$ threshold, then the GATE goes low within 0.5 µs (typical). This fast reverse voltage comparator scheme ensures robust performance during fast input voltage ramp down tests such as input micro-shorts. The external MOSFET is turned ON back when the voltage across A and C hits $V_{(AC\_FWD)}$ threshold within 1.9 µs (typical) for LM74721-Q1. For ideal diode only designs, connect LM74721-Q1 as shown in Figure 8-1

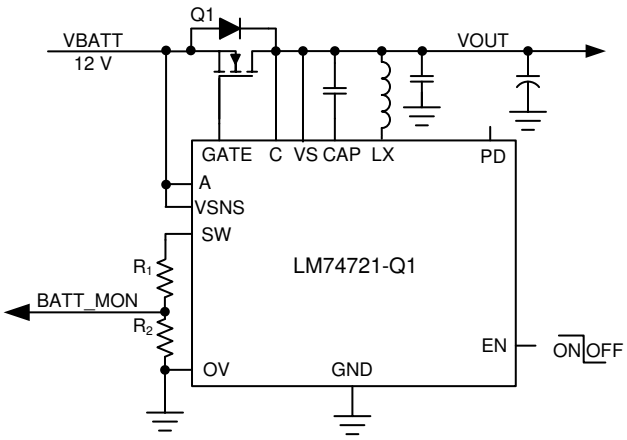


Figure 8-1. Configuring LM74721-Q1 for Ideal Diode Only

8.3.1.1 Input TVS Less Operation: VDS Clamp

The LM74721-Q1 features an integrated VDS clamp that operates the external MOSFET as an active clamp to dissipate the automotive ISO7637 pulse 1 transient.

When the ISO7637 pulse 1 is applied at the input:

- The GATE goes low and turns OFF the MOSFET after the voltage drop across A and C reaches $V_{(AC\_REV)}$ threshold.
- After the voltage across Drain and Source of the MOSFET reaches V_{CLAMP} level (34-V minimum), it is turned ON back in saturation, operating as an active clamp and dissipates the ISO7637 pulse 1 energy.

Figure 8-2 shows circuit operation during ISO7637 pulse 1.

Note that the reverse current flows from V_{OUT} back to input during the ISO7637 pulse 1 test dropping the V_{OUT}. The output filter must be designed to ensure that VOUT does not go negative during ISO7637 pulse 1 test. For all the other ISO7637 pulses that is pulse 2a, 2b, 3a, 3b, the input and output filter components suppress these pulses.

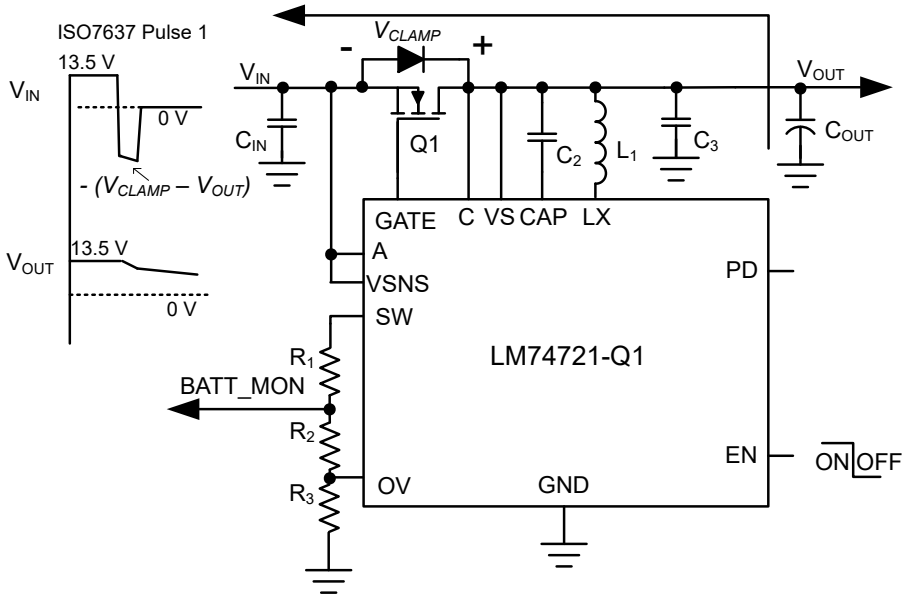


Figure 8-2. LM74721-Q1 Ideal Diode Circuit Operation During ISO7637 Pulse 1

8.3.2 Load Disconnect Switch Control (PD)

The PD pin provides a 50-µA drive and 88-mA peak pulldown strength for the load disconnect switch stage. Connect the Gate of the FET to PD pin. Place a 18-V Zener (Dz) across the FET gate and source.

For inrush current limiting, connect C_{dVdT} capacitor and R_1 as shown in Figure 8-3.

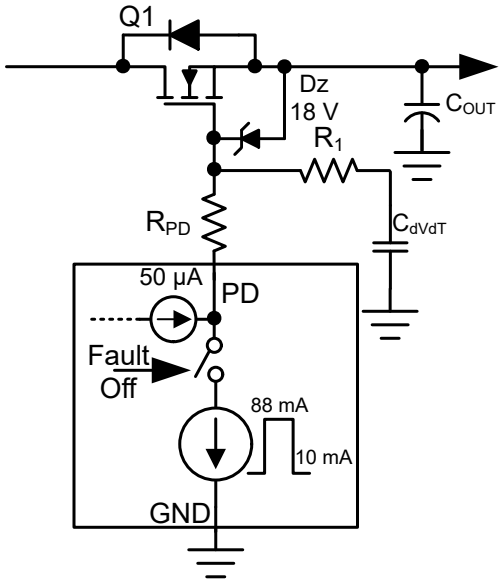


Figure 8-3. Inrush Current Limiting

The C_{dVdT} capacitor is required for slowing down the PD voltage ramp during power up for inrush current limiting. Use Equation 1 to calculate C_{dVdT} capacitance value.

$$C_{(dVdT)} = \frac{I_{PD\_DRV} \times C_{OUT}}{I_{INRUSH}} \quad (1)$$

where I_{PD_DRV} is 50 µA (typical), I_{INRUSH} is the inrush current, and C_{OUT} is the output load capacitance. An extra resistor, R_1, in series with the C_{dVdT} capacitor improves the turn-off time.

PD is pulled low during the following conditions:

- During an OV event with the OV pin voltage rising above the $V_{(OVR)}$ threshold
- When the EN pin is pulled low with $V_{(EN)}$ driven lower than $V_{(EN\_IL)}$ level
- When the voltage at VS pin drops below the $V_{(VS\ POR)}$ falling threshold

During these conditions, the FET Q1 turns OFF with its GATE connected to its SOURCE terminal through the external Zener (Dz).

Use Equation 2 to calculate the peak power dissipated in the LM74721-Q1 at the instance of PD pulldown.

$$P_{PD\_peak} = V_{OUT} \times I_{PD\_SINK} \quad (2)$$

where

- I_{PDSINK_peak} is the peak sink current of 88 mA (typical)

In the system designs with input voltage above 48 V, TI recommends to place a resistor, R_{PD}, in series with the PD pin as shown in Figure 8-3. The peak power dissipation during the pulldown events gets distributed in R_{PD} and the internal PD switch. A resistor value in the range of 270 Ω to 330 Ω can be selected to limit the device power dissipation within the safe limits.

8.3.3 Overvoltage Protection and Battery Voltage Sensing (VSNS, SW, OV)

A disconnect switch is integrated between VSNS and SW pins. This switch is turned OFF when EN pin is pulled low. This action helps to reduce the leakage current through the resistor divider network during system shutdown state (IGN_OFF state).

Connect a resistor ladder as shown in Figure 8-4 for battery voltage sensing and overvoltage threshold programming.

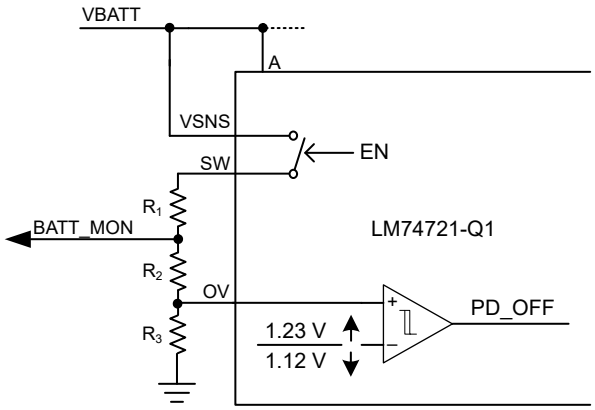


Figure 8-4. Programming Overvoltage Threshold and Battery Voltage Sensing

8.3.4 Boost Regulator

The LM74721-Q1 integrates a boost converter to provide voltage necessary to drive the external N-channel MOSFETs for the ideal diode and the load disconnect stages. The boost converter uses hysteretic mode control scheme for the output voltage (V_{CAP}-V_{VS}) regulation along with the constant peak inductor current limit (I_{LX}). When the CAP–VS voltage is below its nominal value of typically 11.9 V, the low side switch of the boost is turned on and the inductor current rises with the slope of VS/L approximately. After the current hits the limit of 140 mA (typical), then the low side switch is turned off and the inductor current discharges to the output till it reaches zero. The low side switch is turned on again and the switching cycle repeats until the CAP–VS voltage has risen above the boost rising threshold of 13 V (typical). After this threshold level is reached, the boost converter switching is turned OFF to reduce the quiescent current.

For the boost converter to be enabled, the EN pin voltage must be above the specified input high threshold, $V_{(ENR)}$. The boost converter has a maximum output load capacity of 30-mA typical. If EN pin is pulled low, then the boost converter remains disabled.

8.4 Shutdown Mode

The LM74721-Q1 enters shutdown mode when the EN pin voltage is below the specified input low threshold, $V_{(EN\_IL)}$. Both the gate drivers (GATE and PD) and the boost regulator are disabled in shutdown mode. During shutdown mode, the LM74721-Q1 enters low IQ operation with a total input quiescent consumption of 2 µA (typical).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

LM74721-Q1 controls two N-channel power MOSFETs with GATE used to control diode MOSFET to emulate an ideal diode and PD controlling second MOSFET for power path cutoff when disabled or during an overvoltage protection and provide inrush current limiting. IQ during operation (EN = High) is < 35 µA and < 3.3 µA during shutdown mode (EN = Low). LM74721-Q1 can be placed into low quiescent current mode using EN = low, where both GATE and PD are turned OFF.

9.2 Typical 12-V Reverse Battery Protection Application

Figure 9-1 shows a typical application circuit of LM74721-Q1 configured to provide TVS less reverse battery protection.

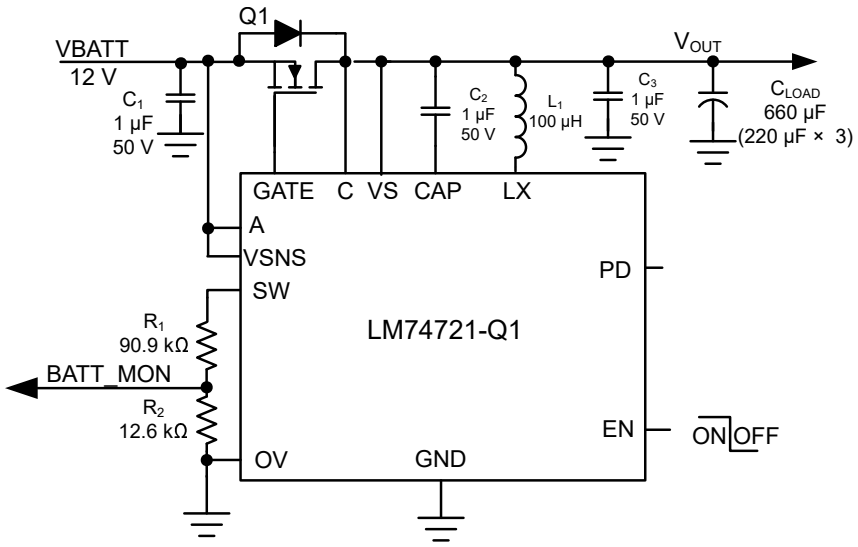


Figure 9-1. Typical Application Circuit for 12-V TVS-less Reverse Battery Protection

9.2.1 Design Requirements for 12-V Battery Protection

Table 9-1 lists the system design requirements.

Table 9-1. Design Parameters – 12-V Reverse Battery Protection and Overvoltage Protection

DESIGN PARAMETER	EXAMPLE VALUE
Operating input voltage range	12-V battery, 12-V nominal with 3.2-V cold crank and 35-V load dump
Output power	50 W
Output current range	4-A nominal, 5-A maximum
Input capacitance	0.1-µF minimum
Output capacitance	220 µF × 3
AC super imposed test	2-V peak-peak, 30 kHz (maximum)

Table 9-1. Design Parameters – 12-V Reverse Battery Protection and Overvoltage Protection (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Automotive transient immunity compliance	ISO 7637-2 with pulse 1 maximum level of –100-V peak level and 10-Ω generator impedance, ISO 16750-2 and LV124

9.2.2 Detailed Design Procedure

9.2.2.1 Boost Converter Components (C2, C3, L1)

Place a minimum of a 1-µF capacitor across drain of the FET to GND (C2) and across CAP pin of LM74721-Q1 to drain of the FET (C3). Use a 100-µH inductor (L1) with saturation current rating > 175 mA. Example: XPL2010-104ML from coil craft.

9.2.2.2 Input and Output Capacitance

TI recommends a minimum input capacitance C1 of 1 µF and output capacitance C_{OUT} of 0.1 µF.

9.2.2.3 Hold-Up Capacitance

Usually bulk capacitors are placed on the output due to various reasons, such as uninterrupted operation during power interruption or micro-short at the input, hold-up requirements for doing a memory dump before turning of the module and filtering requirements as well. This design considers minimum bulk capacitors requirements for meeting functional status "A" during LV124 E10 test case 2 100-µs input interruption. To achieve functional pass status A, acceptable voltage droop in the output of LM74721-Q1 is based on the UVLO settings of downstream DC/DC converters. For this design, 1-V drop in output voltage for 100 µs is considered and the minimum hold-up capacitance required is calculated by:

$$C_{(HOLD\_UP\_MIN)} = \frac{I_{LOAD\_MAX} \times 100\mu s}{dV_{OUT}} \quad (3)$$

Minimum hold-up capacitance required for 1-V drop in 100 µs is 500 µF. 3 × 220-µF electrolytic capacitors are selected.

Also during ISO7637-2 pulse 1 transient event, LM74721-Q1 operates external MOSFET in active clamp mode, allowing reverse current to flow from output to back to the input source. The output hold-up capacitor also ensures output voltage does not swing negative when device is operating VDS clamp mode.

9.2.2.4 MOSFET Selection: Q1

For selecting the blocking MOSFET Q1, important electrical parameters are the maximum continuous drain current ID, the maximum drain-to-source voltage $VDS_{(MAX)}$, the maximum drain-to-source voltage $VGS_{(MAX)}$, Safe Operating Area (SOA), the maximum source current through body diode and the drain-to-source ON resistance $R_{DS(ON)}$.

The maximum continuous drain current (I_D) rating must exceed the maximum continuous load current.

To reduce the MOSFET conduction losses, MOSFET with the lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ cannot be beneficial always. Higher $R_{DS(ON)}$ provides increased voltage information to LM74721-Q1 reverse current comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Choosing a MOSFET with forward voltage drop of less than 50 mV at maximum current is a good starting point.

The maximum drain-to-source voltage, $VDS_{(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. With LM74721-Q1, the maximum differential voltage across the MOSFET is V_{CLAMP} (maximum) of 43 V. TI recommends a minimum of 60-V VDS rated. This includes all the automotive transient events and any anticipated fault conditions.

During the ISO7637 pulse 1, the maximum VDS seen by the external MOSFET Q1 is $VDS_{CLAMP\ (max)}$ that is 43 V. Use Equation 4 to calculate the peak current during ISO7637-2 pulse 1.

$$I_{ISO\_PEAK} = (V_{ISO} + V_{OUT} - VDS_{CLAMP(max)}) / R_S \quad (4)$$

Where

- V_{ISO} is the negative peak of the ISO7637-2 pulse 1
- V_{OUT} is the initial level of the VBATT before ISO pulse is applied
- VDS_{CLAMP} is maximum VCLAMP threshold of LM74721-Q1
- R_S is the ISO7637 pulse generator input impedance (10 Ω)

For ISO7637-2 pulse 1 with amplitude of –100 V, V_{OUT} nominal voltage of 13.5 V the peak current seen by MOSFET Q1 comes around 7 A.

The current profile tapers down from 7 A to 0 A from the peak of 7 A as shown in Figure 9-5. The resulting average current (I_{ISO_AVG}) can be approximated as one third of the peak current that is around 2.4 A. The VDS clamp operation lasts for about 1 ms (maximum). Selecting a MOSFET with SOA characteristics covering the load line of 43 V which can support drain current greater than (I_{ISO_PEAK} / 2) for 1 ms is a good starting point. For this particular design example, MOSFET which can support greater than 3.5 A of drain current at 43-V V_{DS} on SoA curve is suitable.

Figure 9-2 shows typical SoA characteristics plot highlighting maximum drain current supported by the MOSFET for the duration of 1 ms. MOSFET data sheet SoA curves are typically plotted at ambient temperature, so consider sufficient margin over MOSFET parameters calculated values to ensure safe operation over desired operating temperature range.

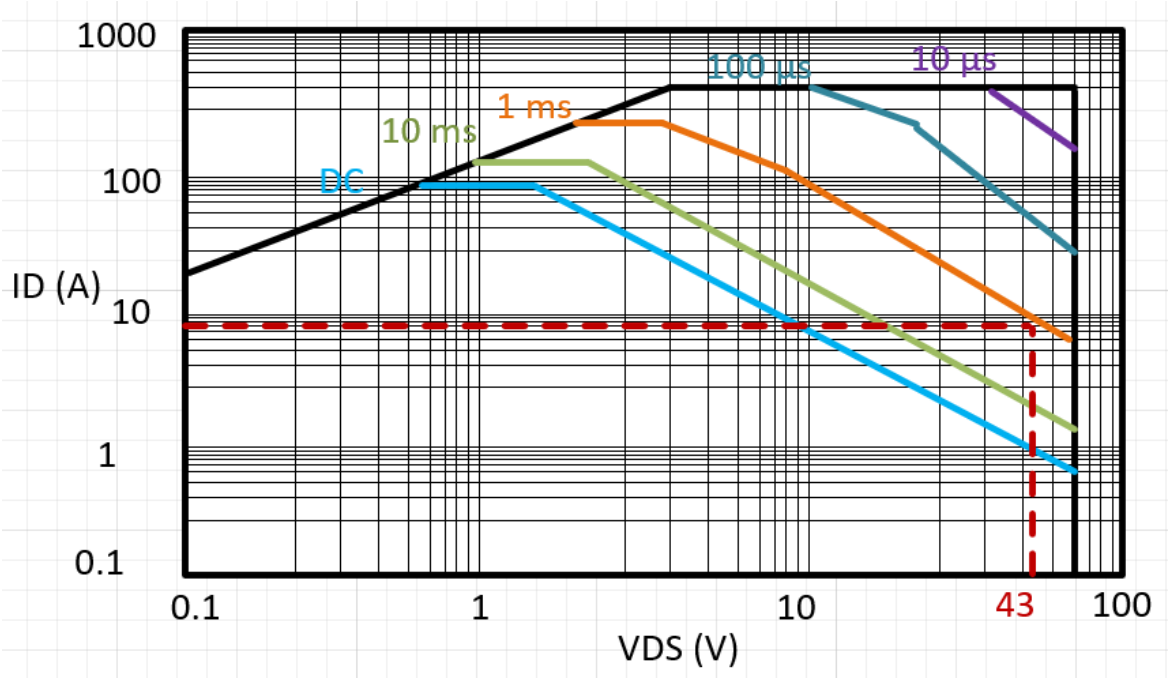


Figure 9-2. Typical MOSFET SoA Characteristics

As external MOSFET dissipates ISO7637-2 pulse 1 energy, a special attention must be given while calculating maximum power dissipation and effective temperature rise. Use Equation 5 to calculate an average power dissipation across the MOSFET.

$$P_{D\_AVG} = VDS_{CLAMP(max)} \times I_{ISO\_AVG} \quad (5)$$

For given design example, average power dissipation comes around.

$$P_{D\_AVG} = 43\ V \times 2.4\ A = 103.2\ W \quad (6)$$

Typical ISO7637-2 pulse 1 transient lasts for 2 ms with total time period of 200 ms between two consecutive pulses (duty cycle of 1%). The effective temperature rise due to power dissipation across MOSFET during

ISO7637-2 pulse 1 event can be calculated by looking at transient thermal impedance curve in a MOSFET data sheet. Figure 9-3 shows an example of how to estimate transient thermal impedance of a MOSFET for ISO7637-2 pulse 1 event.

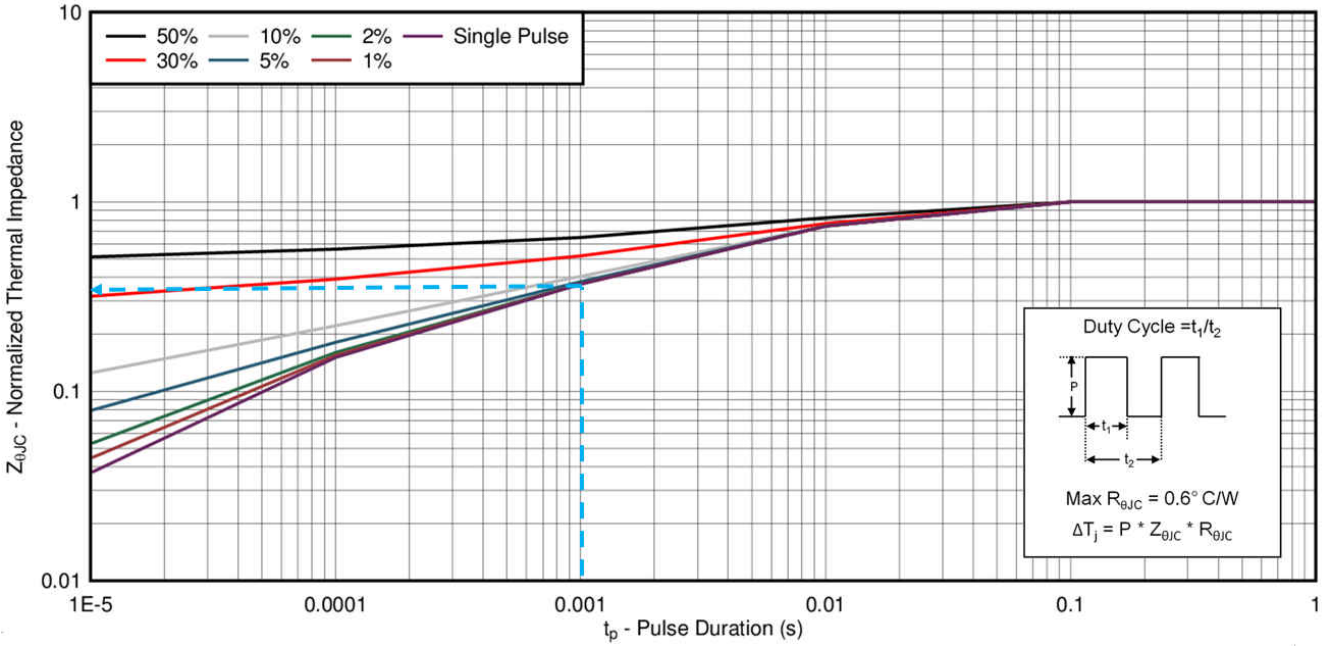


Figure 9-3. Typical MOSFET Transient Thermal Impedance

The maximum V_{GS} LM74721-Q1 can drive is 13.9 V, so a MOSFET with 15-V minimum V_{GS} rating must be selected.

Based on the design requirements and MOSFET selection criteria BUK7Y4R8-60E, SQJ460AEP, STL130N6F7 are some of the 60-V MOSFET options that can be selected.

9.2.3 Application Curves

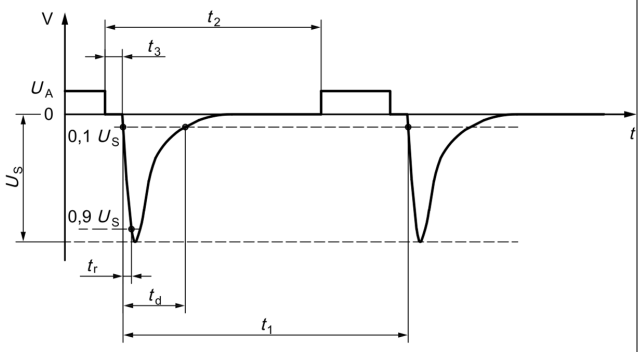
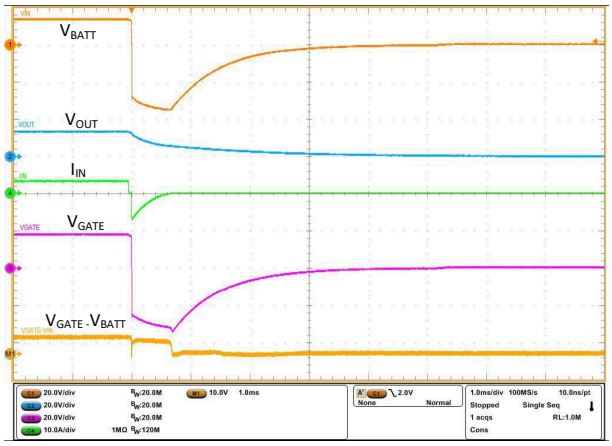
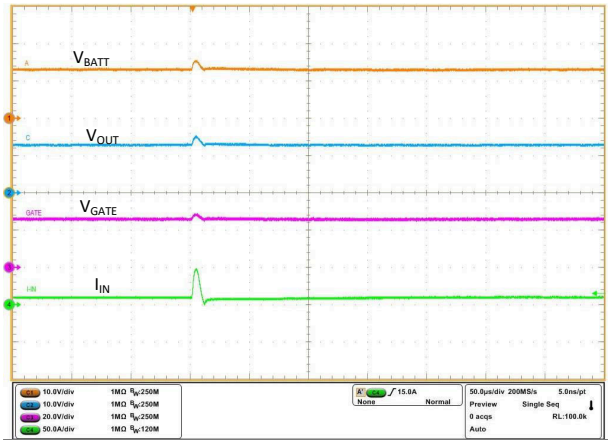


Figure 9-4. ISO 7637-2 Pulse 1



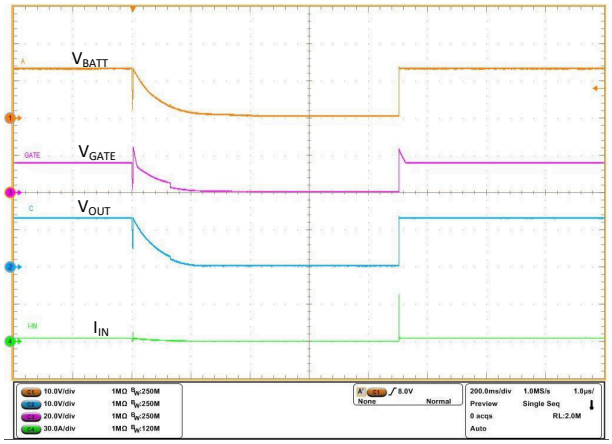
Time (4 ms/DIV)

Figure 9-5. Response to ISO 7637-2 Pulse 1



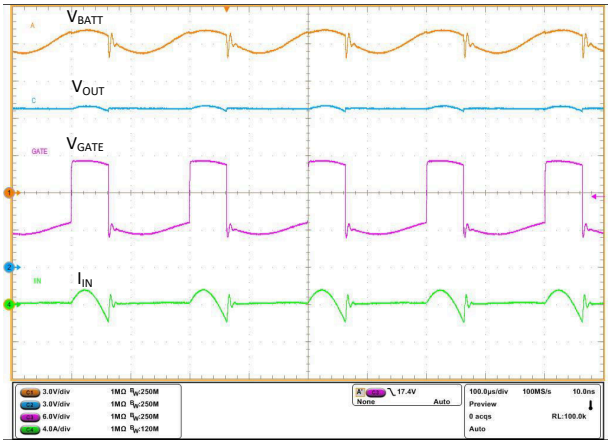
Time (100 µs/DIV)

Figure 9-6. Response to ISO 7637-2 Pulse 2A



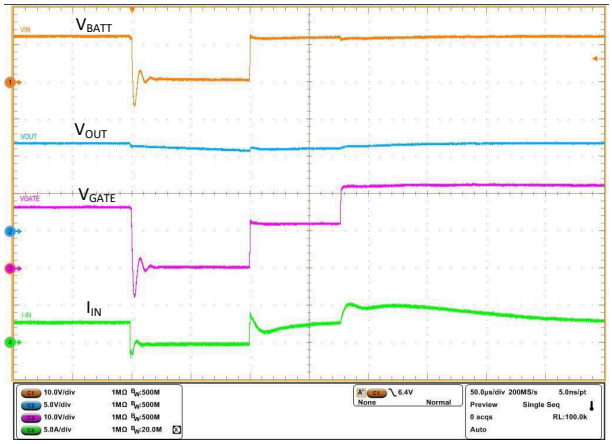
Time (200 ms/DIV)

Figure 9-7. Response to ISO 7637-2 Pulse 2B



Time (100 ms/DIV)

Figure 9-8. Response to LV124 E-06 (AC Superimpose Test)



Time (40 µs/DIV)

Figure 9-9. Response to LV124 E-10 (Input Micro Short, 100 us)

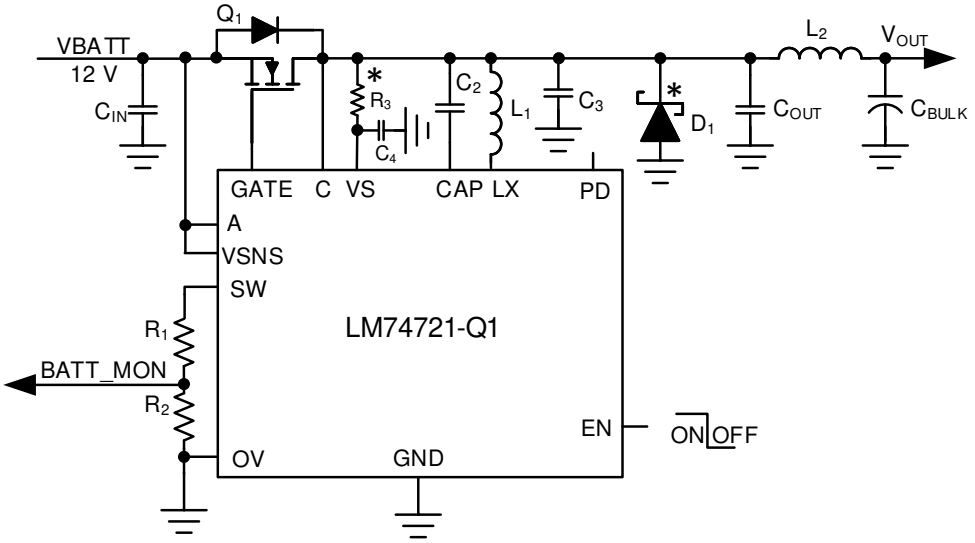
9.3 What to Do and What Not to Do

Leave the exposed pad (RTN) of the IC floating. Do not connect the exposed pad to the GND plane. Connecting RTN to GND disables the reverse polarity protection feature.

10 Power Supply Recommendations

10.1 Transient Protection

When the MOSFET is turned OFF during conditions such as reverse current blocking in the system designs where there is an output C-L-C filter (for EMI filtering) as shown in Figure 10-1, the voltage across C_{OUT} can swing negative based on the values of L_2 ,C_{OUT} and the initial reverse current in L_2 before the MOSFET turns OFF. Use a low VF Schottky diode D_1 across C_{OUT} to GND and place a R-C filter with 100 Ω and 0.1 µF at Vs pin, ensuring the device pins does not exceed the *Absolute Maximum Ratings*.



* Optional components needed for suppression of transients

Figure 10-1. Circuit Implementation with Optional Protection Components for LM74721-Q1

11 Layout

11.1 Layout Guidelines

- Connect A, GATE and C pins of LM74721-Q1 close to the MOSFET SOURCE, GATE and DRAIN pins for the ideal diode stage, c.
- Use thick and short traces for source and drain of the MOSFET to minimize resistive losses because the high current path of for this solution is through the MOSFET.
- Have the PowerPAD™ integrated circuit package (exposed pad) of the MOSFET soldered directly to the top plane for best thermal performance. Other planes, such as the bottom side of the circuit board, can be used to increase heat sinking. Thermal considerations: during the VDS clamp operation, the MOSFET acts as an active clamp with pulse power dissipation.
- Connect the GATE pin of the LM74721-Q1 to the MOSFET GATE with short trace.
- Minimize the loops formed by capacitor across CAP pin and DRAIN of the FET and C3 to GND by placing these capacitors as close as possible. Keep the GND side of the C3 capacitor close to GND pin of LM74721-Q1. Boost converter switching currents flow into LX, CAP, GND pins and C3 (across DRAIN of the FET to GND).
- Place transient suppression components like output Schottky close to C pin of LM74721-Q1.

11.2 Layout Example

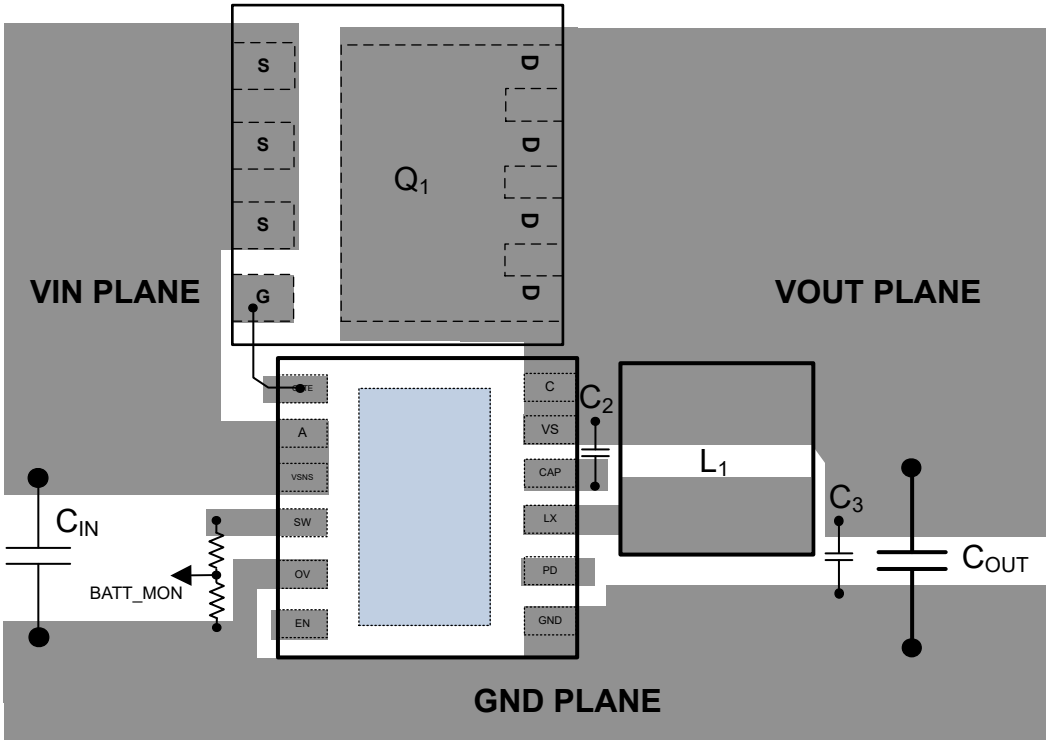


Figure 11-1. LM74721-Q1 Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74721QDRRRQ1	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	L74721	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

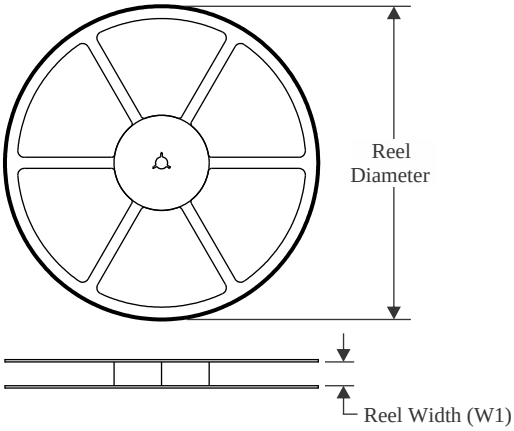
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

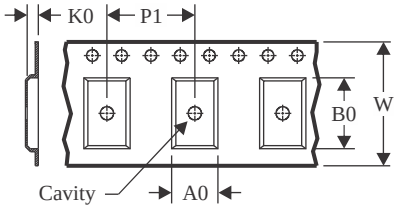
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

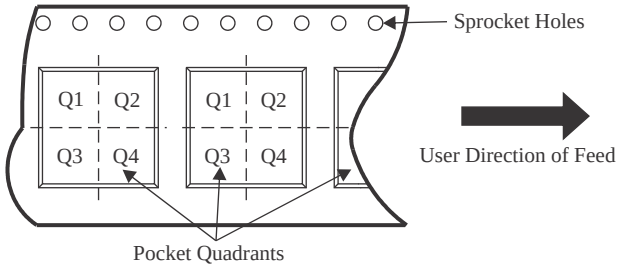


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

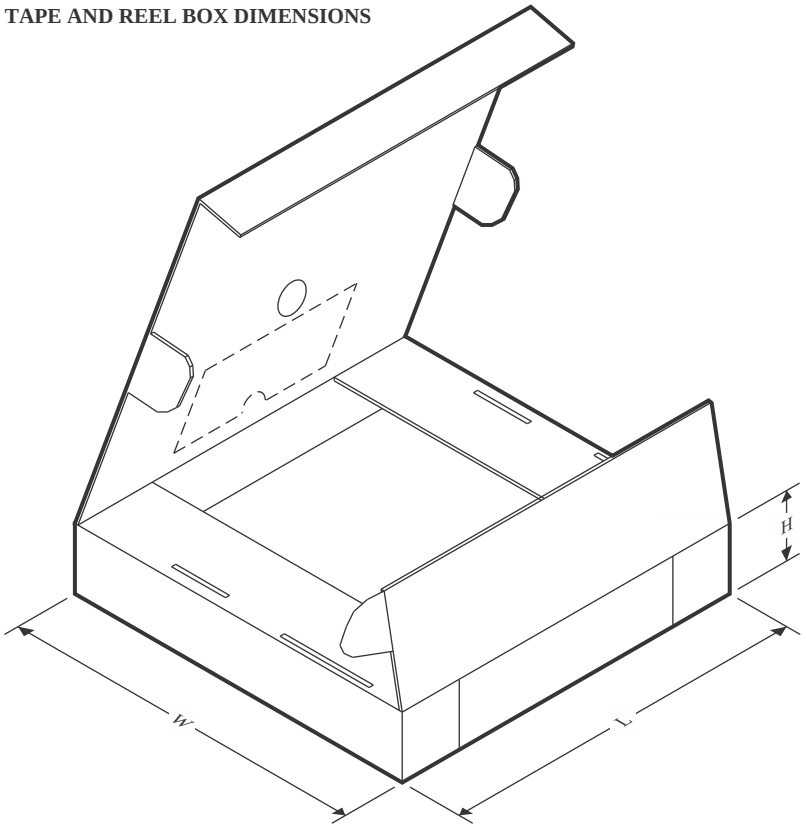
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74721QDRRRQ1	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74721QDRRRQ1	WSON	DRR	12	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

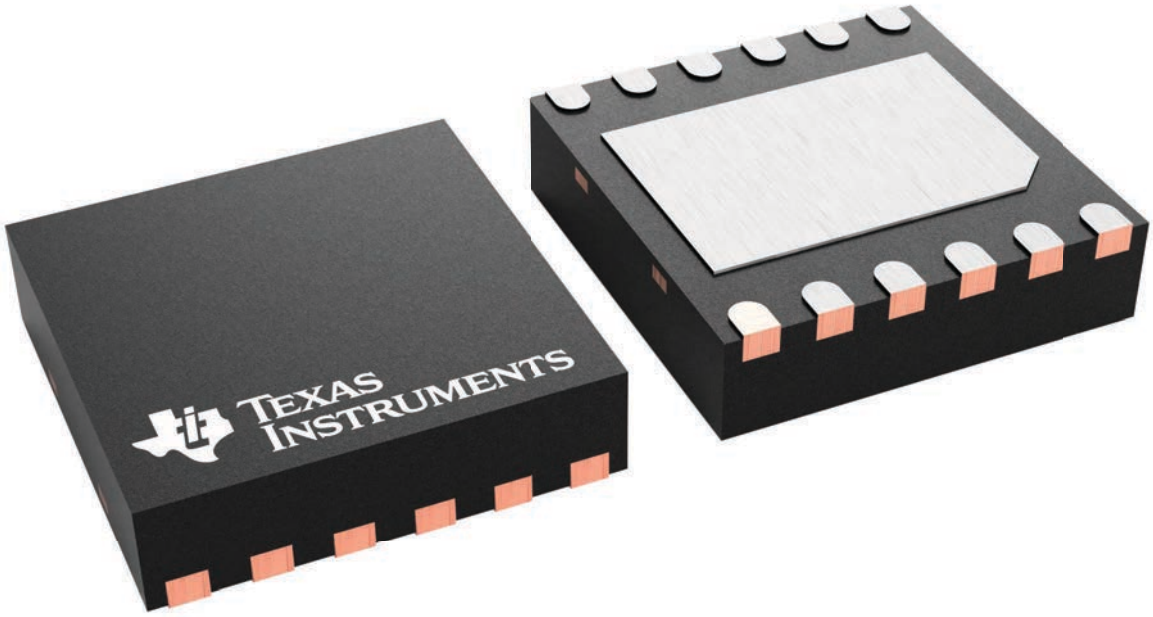
DRR 12

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



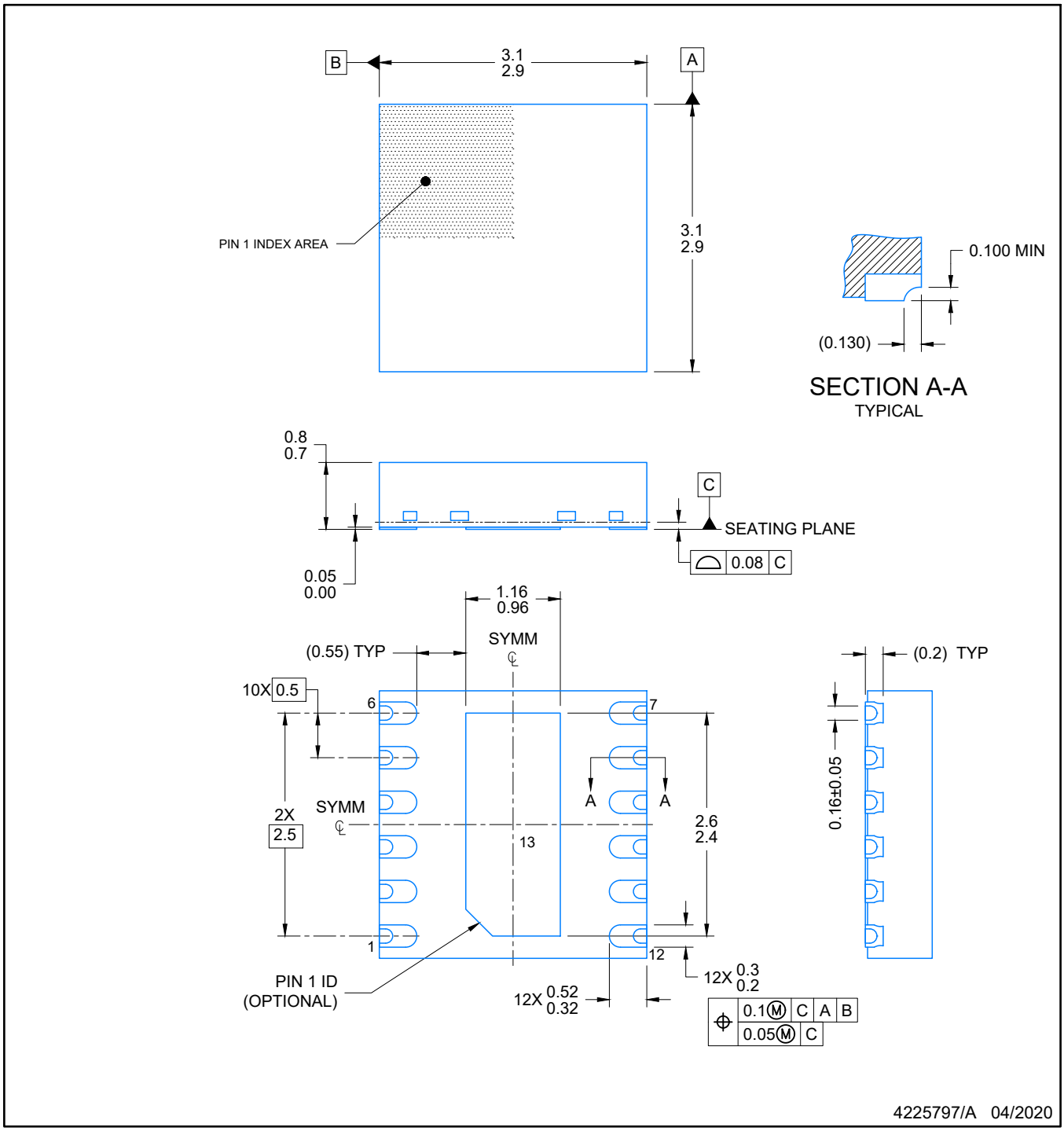
4223490/B

PACKAGE OUTLINE

DRR0012F

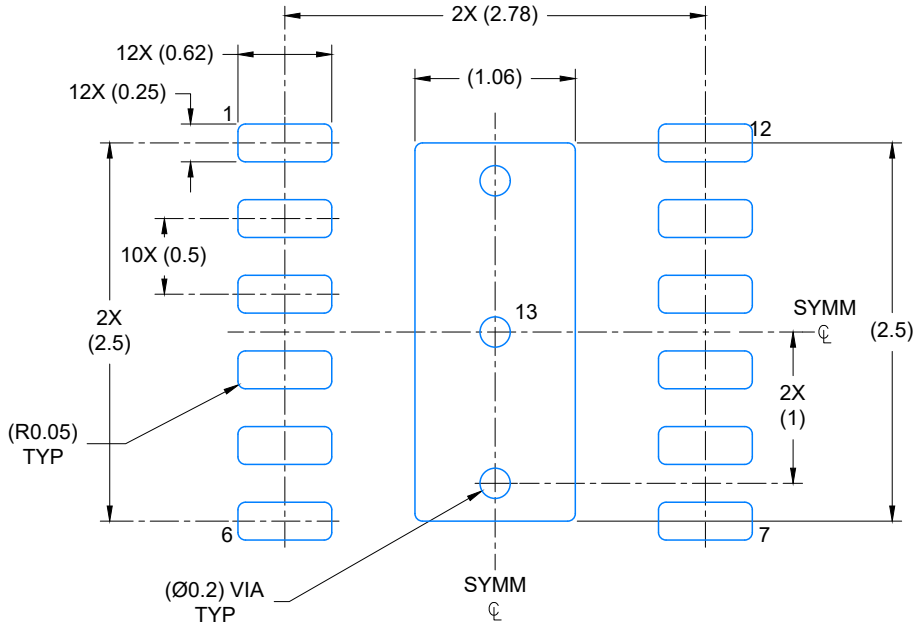
WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

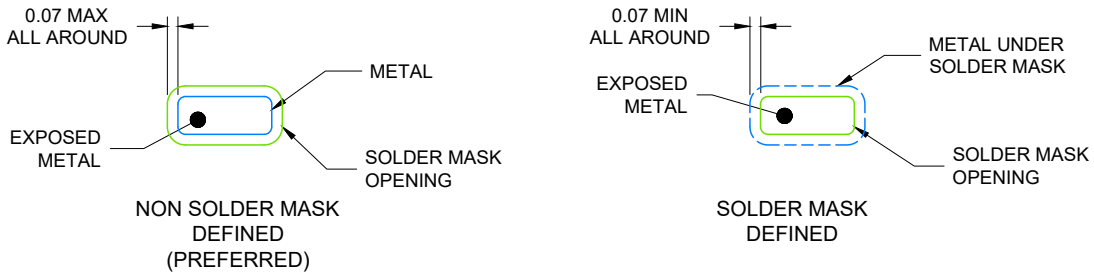


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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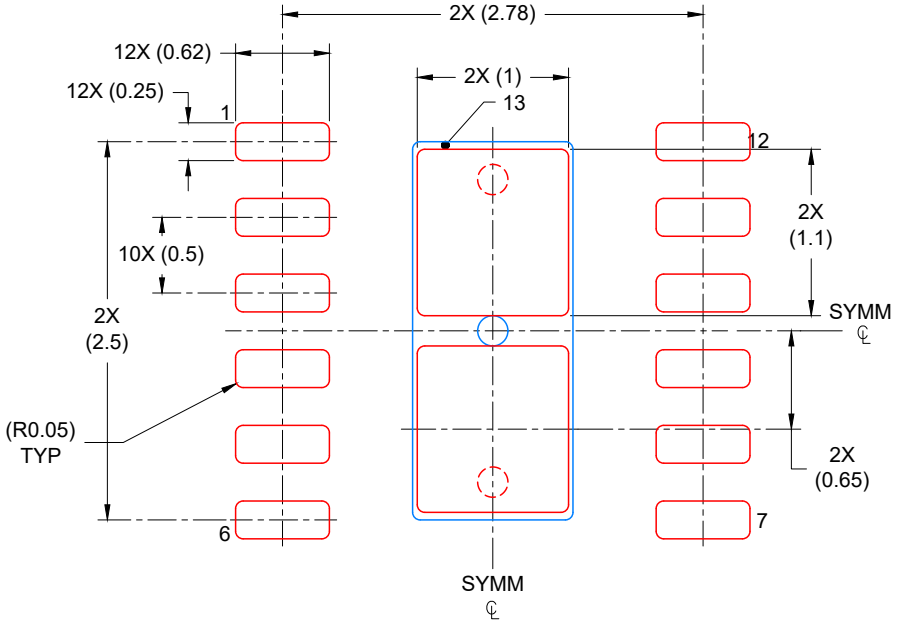
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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