LMH6559 High-Speed, Closed-Loop Buffer

Check for Samples: LMH6559

FEATURES

- **Closed-Loop Buffer**
- **1750MHz Small Signal Bandwidth**
- **4580V/µs Slew Rate**
- **0.06% / 0.02° Differential Gain/Phase**
- **−52dBc THD at 20MHz**
- **Single Supply Operation (3V Min.)**
- **75mA Output Current**

APPLICATIONS

- **Video Switching and Routing**
- **Test Point Drivers**
- **High Frequency Active Filters**
- **Wideband DC Clamping Buffers**
- **High-Speed Peak Detector Circuits**
- **Transmission Systems**
- **Telecommunications**
- **Test Equipment and Instrumentation**

DESCRIPTION

The LMH6559 is a high-speed, closed-loop buffer designed for applications requiring the processing of very high frequency signals. While offering a small signal bandwidth of 1750MHz, and an ultra high slew rate of 4580V/µs the LMH6559 consumes only 10mA of quiescent current. Total harmonic distortion into a load of 100Ω at 20MHz is −52dBc. The LMH6559 is configured internally for a loop gain of one. Input resistance is 200kΩ and output resistance is but 1.2Ω. These characteristics make the LMH6559 an ideal choice for the distribution of high frequency signals on printed circuit boards. Differential gain and phase specifications of 0.06% and 0.02° respectively at 3.58MHz make the LMH6559 well suited for the buffering of video signals.

The device is fabricated on Texas Instruments' high-speed VIP10 process using TI's proven high performance circuit architectures.

Typical Schematic

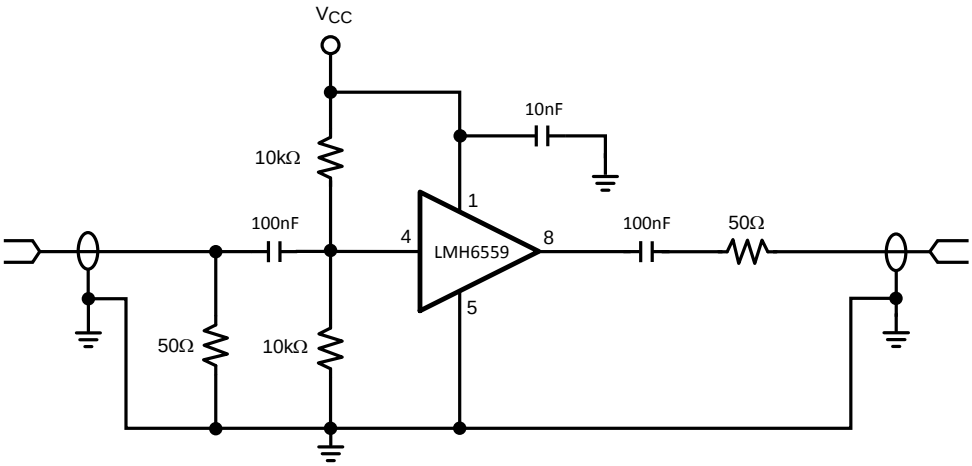


Figure 1.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Absolute Maximum Ratings[1][2]

ESD Tolerance[3]	Human Body Model	2000V
	Machine Model	200V
Output Short Circuit Duration		See[4], [5] and [6]
Supply Voltage ($V^+ - V^-$)		13V
Voltage at Input/Output Pins		V^+ +0.8V, V^- −0.8V
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C
Storage Temperature Range		−65°C to +150°C
Junction Temperature		+150°C

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) Short circuit test is a momentary test.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings[1]

Supply Voltage ($V^+ - V^-$)		3 - 10V
Temperature Range[2][3]		−40°C to +85°C
Package Thermal Resistance[2][3]	8-Pin SOIC	172°C/W
	5-Pin SOT-23	235°C/W

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.
(3) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. There is no specification of parametric performance as indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications section for information on temperature de-rating of this device.

±5V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = +5V, V^- = −5V, V_O = V_{CM} = 0V and R_L = 100Ω to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_O < 0.5V_{PP}		1750		MHz
GFN	Gain Flatness < 0.1dB	V_O < 0.5V_{PP}		200		MHz
FPBW	Full Power Bandwidth (−3dB)	V_O = 2V_{PP} (+10dBm)		1050		MHZ
DG	Differential Gain	R_L = 150Ω to 0V, f = 3.58 MHz		0.06		%
DP	Differential Phase	R_L = 150Ω to 0V, f = 3.58 MHz		0.02		deg
Time Domain Response						
t_r	Rise Time	3.3V Step (20-80%)		0.4		ns
t_f	Fall Time			0.5		ns
t_s	Settling Time to ±0.1%	3.3V Step		9		ns
OS	Overshoot	1V Step		4		%
SR	Slew Rate	See (3)		4580		V/µs
Distortion And Noise Performance						
HD2	2nd Harmonic Distortion	V_O = 2V_{PP}, f = 20MHz		−58		dBc
HD3	3rd Harmonic Distortion	V_O = 2V_{PP}, f = 20MHz		−53		dBc
THD	Total Harmonic Distortion	V_O = 2V_{PP}, f = 20MHz		−52		dBc
e_n	Input-Referred Voltage Noise	f = 1MHz		5.7		nV/√Hz
CP	1dB Compression point	f = 10MHz		+23		dBm
SNR	Signal to Noise Ratio	f > 100kHz, BW = 5MHz, V_O = 350mVrms		89		dB

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Slew rate is the average of the positive and negative slew rate.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = +5V, V^- = −5V, V_O = V_{CM} = 0V and R_L = 100Ω to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Static, DC Performance						
A_{CL}	Small Signal Voltage Gain	V_O = 100mV$_{PP}$ R_L = 100Ω to 0V	**.97**	.996		V/V
		V_O = 100mV$_{PP}$ R_L = 2kΩ to 0V	**.99**	.998		
V_{OS}	Input Offset Voltage			3	20 **25**	mV
TC V_{OS}	Temperature Coefficient Input Offset Voltage	See (4)		23		µV/°C
I_B	Input Bias Current	See (5)	−10 **−14**	−3		µA
TC I_B	Temperature Coefficient Input Bias Current	See (4)		−3.6		nA/°C
R_{OUT}	Output Resistance	R_L = 100Ω to 0V, f = 100kHz		1.2		Ω
		R_L = 100Ω to 0V, f = 10MHz		1.3		
PSRR	Power Supply Rejection Ratio	V_S = ±5V to V_S = ±5.25V	48 **44**	63		dB
I_S	Supply Current	No Load		10	14 **17**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance			200		kΩ
C_{IN}	Input Capacitance			1.7		pF
V_O	Output Swing Positive	R_L = 100Ω to 0V	3.20 **3.18**	3.45		V
		R_L = 2kΩ to 0V	3.55 **3.54**	3.65		
	Output Swing Negative	R_L = 100Ω to 0V		−3.45	−3.20 **−3.18**	V
		R_L = 2kΩ to 0V		−3.65	−3.55 **−3.54**	
I_{SC}	Output Short Circuit Current	Sourcing: V_{IN} = +V_S, V_O = 0V		−83		mA
		Sinking: V_{IN} = −V_S, V_O = 0V		83		
I_O	Linear Output Current	Sourcing: V_{IN} - V_O = 0.5V (5)	−50 **−43**	−74		mA
		Sinking: V_{IN} - V_O = −0.5V (5)	50 **43**	74		

(4) Average Temperature Coefficient is determined by dividing the change in a parameter at temperature extremes by the total temperature change.

(5) Positive current corresponds to current flowing into the device.

5V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, V_O = V_{CM} = $V^+/2$ and R_L = 100Ω to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_O < 0.5V_{PP}		745		MHz
GFN	Gain Flatness < 0.1dB	V_O < 0.5V_{PP}		90		MHz
FPBW	Full Power Bandwidth (−3dB)	V_O = 2V_{PP} (+10dBm)		485		MHZ
DG	Differential Gain	R_L = 150Ω to $V^+/2$, f = 3.58 MHz		0.29		%
DP	Differential Phase	R_L = 150Ω to $V^+/2$, f = 3.58 MHz		0.06		deg
Time Domain Response						
t_r	Rise Time	2.3V_{PP} Step (20-80%)		0.6		ns
t_f	Fall Time			0.9		ns
t_s	Settling Time to ±0.1%	2.3V Step		9.6		ns
OS	Overshoot	1V Step		3		%
SR	Slew Rate	See (3)		2070		V/µs
Distortion And Noise Performance						
HD2	2nd Harmonic Distortion	V_O = 2V_{PP}, f = 20MHz		−53		dBc
HD3	3rd Harmonic Distortion	V_O = 2V_{PP}, f = 20MHz		−56		dBc
THD	Total Harmonic Distortion	V_O = 2V_{PP}, f = 20MHz		−52		dBc
e_n	Input-Referred Voltage Noise	f = 1MHz		4.0		nV/√Hz
CP	1dB Compression point	f = 10MHz		+7		dBm
SNR	Signal to Noise Ratio	f > 100kHz, BW = 5MHz, V_O = 350mVrms		92		dB
Static, DC Performance						
A_{CL}	Small Signal Voltage Gain	V_O = 100mV_{PP} R_L = 100Ω to $V^+/2$	**.97**	.996		V/V
		V_O = 100mV_{PP} R_L = 2kΩ to $V^+/2$	**.99**	.998		
V_{OS}	Input Offset Voltage			1.52	12 **16**	mV
TC V_{OS}	Temperature Coefficient Input Offset Voltage	See (4)		23		µV/°C
I_B	Input Bias Current	See (5)	−5 **−8**	−2.7		µA
TC I_B	Temperature Coefficient Input Bias Current	See (4)		1.6		nA/°C
R_{OUT}	Output Resistance	R_L = 100Ω to $V^+/2$, f = 100kHz		1.4		Ω
		R_L = 100Ω to $V^+/2$, f = 10MHz		1.6		
PSRR	Power Supply Rejection Ratio	V_S = +5V to V_S = +5.5V, V_{IN} = $V_S/2$	48 **44**	68		dB
I_S	Supply Current	No Load		4.7	7 **8.5**	mA

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Slew rate is the average of the positive and negative slew rate.
(4) Average Temperature Coefficient is determined by dividing the change in a parameter at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_O = V_{CM} = V^+/2$ and R_L = 100Ω to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Miscellaneous Performance						
R_{IN}	Input Resistance			200		kΩ
C_{IN}	Input Capacitance			2.0		pF
V_O	Output Swing Positive	R_L = 100Ω to $V^+/2$	3.80 **3.75**	3.88		V
		R_L = 2kΩ to $V^+/2$	3.94 **3.92**	3.98		
	Output Swing Negative	R_L = 100Ω to $V^+/2$		1.12	1.20 **1.25**	V
		R_L = 2kΩ to $V^+/2$		1.03	1.06 **1.09**	
I_{SC}	Output short circuit Current	Sourcing: $V_{IN} = +V_S$, $V_O = V^+/2$		−57		mA
		Sinking: $V_{IN} = -V_S$, $V_O = V^+/2$		26		
I_O	Linear Output Current	Sourcing: $V_{IN} - V_O$ = 0.5V (6)	−50 **−43**	−64		mA
		Sinking: $V_{IN} - V_O$ = −0.5V (6)	30 **23**	42		

(6) Positive current corresponds to current flowing into the device.

3V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 3V, V^- = 0V, $V_O = V_{CM} = V^+/2$ and R_L = 100Ω to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	$V_O < 0.5V_{PP}$		315		MHz
GFN	Gain Flatness < 0.1dB	$V_O < 0.5V_{PP}$		44		MHz
FPBW	Full Power Bandwidth (−3dB)	$V_O = 1V_{PP}$ (+4.5dBm)		265		MHZ
Time Domain Response						
t_r	Rise Time	1.0V Step (20-80%)		0.8		ns
t_f	Fall Time			1.2		ns
t_s	Settling Time to ±0.1%	1V Step		10		ns
OS	Overshoot	0.5V Step		0		%
SR	Slew Rate	See (3)		770		V/µs
Distortion And Noise Performance						
HD2	2nd Harmonic Distortion	$V_O = 2V_{PP}$, f = 20MHz		−74		dBc
HD3	3rd Harmonic Distortion	$V_O = 2V_{PP}$, f = 20MHz		−57		dBc
THD	Total Harmonic Distortion	$V_O = 2V_{PP}$, f = 20MHz		−56		dBc
e_n	Input-Referred Voltage Noise	f = 1MHz		3.9		nV/√Hz
CP	1dB Compression point	f = 10MHz		+4		dBm
SNR	Signal to Noise Ratio	f > 100kHz, BW = 5MHz, V_O = 350mVrms		92		dB

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Slew rate is the average of the positive and negative slew rate.

3V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 3V, V^- = 0V, V_O = V_{CM} = $V^+/2$ and R_L = 100Ω to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
Static, DC Performance						
A_{CL}	Small Signal Voltage Gain	V_O = 100mV$_{PP}$ R_L = 100Ω to $V^+/2$	**.97**	.995		V/V
		V_O = 100mV$_{PP}$ R_L = 2kΩ to $V^+/2$	**.99**	.998		
V_{OS}	Input Offset Voltage			1	7 **9**	mV
TC V_{OS}	Temperature Coefficient Input Offset Voltage	See (4)		3.5		µV/°C
I_B	Input Bias Current	See (5)	−3 **−3.5**	−1.5		µA
TC I_B	Temperature Coefficient Input Bias Current	See (4)		0.46		nA/°C
R_{OUT}	Output Resistance	R_L = 100Ω to $V^+/2$, f = 100kHz		1.8		Ω
		R_L = 100Ω to $V^+/2$, f = 10MHz		2.3		
PSRR	Power Supply Rejection Ratio	V_S = +3V to V_S = +3.5V, V_{IN} = $V^+/2$	48 **46**	68		dB
I_S	Supply Current	No Load		2.4	3.5 **4.5**	mA
Miscellaneous Performance						
R_{IN}	Input Resistance			200		kΩ
C_{IN}	Input Capacitance			2.3		pF
V_O	Output Swing Positive	R_L = 100Ω to $V^+/2$	2.02 **1.95**	2.07		V
		R_L = 2kΩ to $V^+/2$	2.12 **2.02**	2.17		
	Output Swing Negative	R_L = 100Ω to $V^+/2$		.930	.970 **1.050**	V
		R_L = 2kΩ to $V^+/2$		.830	.880 **.980**	
I_{SC}	Output Short Circuit Current	Sourcing: V_{IN} = +V_S, V_O = $V^+/2$		−32		mA
		Sinking: V_{IN} = −V_S, V_O = $V^+/2$		15		
I_O	Linear Output Current	Sourcing: V_{IN} - V_O = 0.5V (5)	−20 **−13**	−28		mA
		Sinking: V_{IN} - V_O = −0.5V (5)	12 **8**	17		

(4) Average Temperature Coefficient is determined by dividing the change in a parameter at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

CONNECTION DIAGRAMS

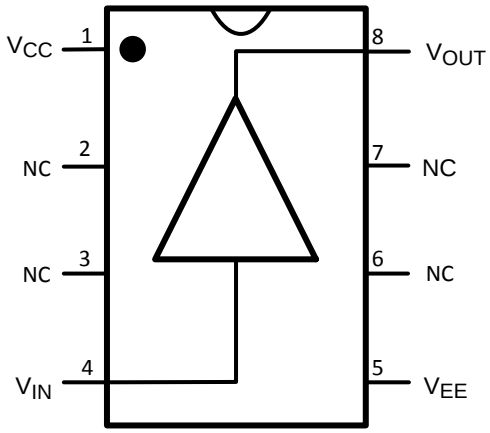


Figure 2. 8-Pin SOIC (Top View)
See Package Number D (R-PDSO-G8)

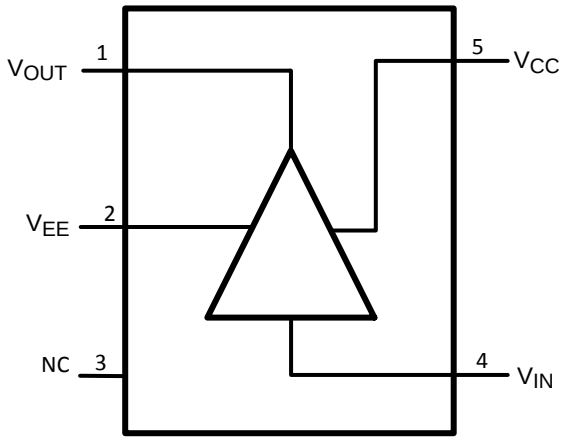


Figure 3. 5-Pin SOT-23 (Top View)
See Package Number DBV (R-PDSO_G5)

Typical Performance Charac teristics

At T_J = 25°C; V^+ = +5V; V^- = −5V; Unless otherwise specified.

Frequency Response

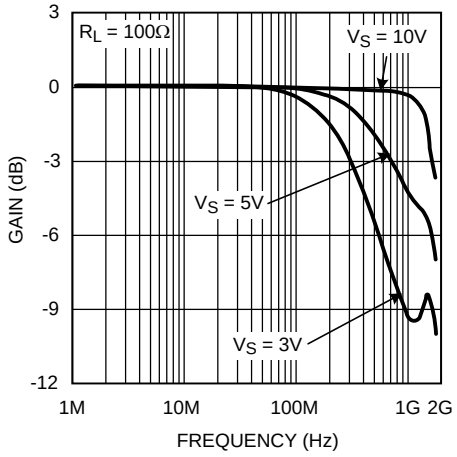


Figure 4.

Frequency Response Over Temperature

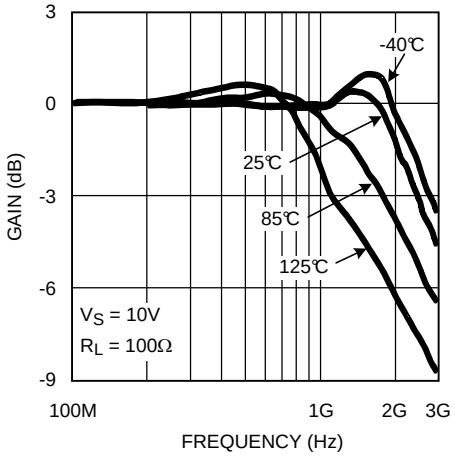


Figure 5.

Gain Flatness

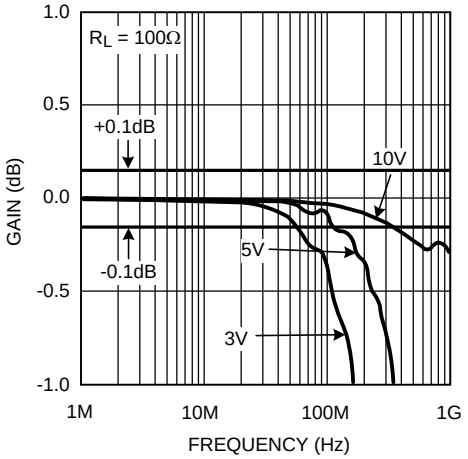


Figure 6.

Differential Gain and Phase

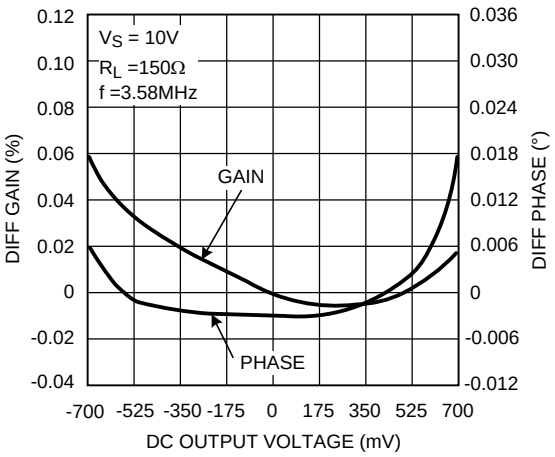


Figure 7.

Differential Gain and Phase

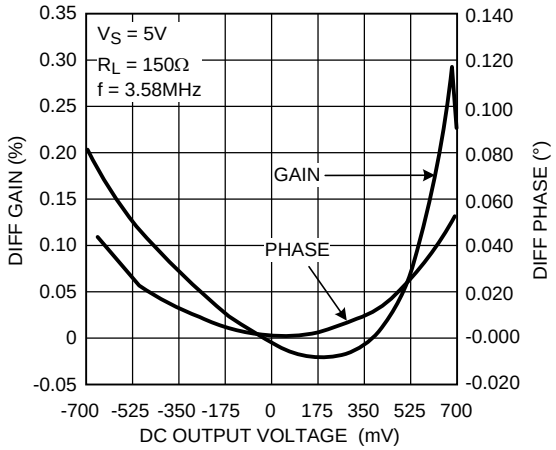


Figure 8.

Transient Response Positive

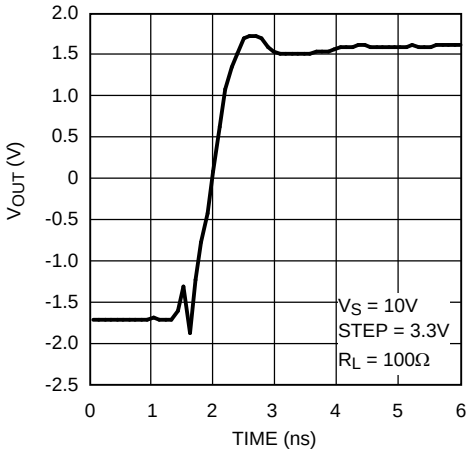


Figure 9.

Typical Performance Charac teristics (continued)

At T_J = 25°C; V^+ = +5V; V^- = −5V; Unless otherwise specified.

Transient Response Negative

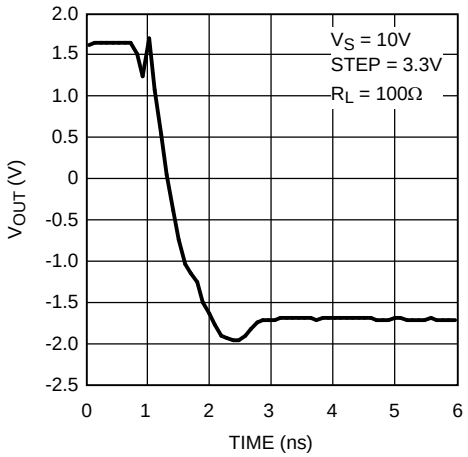


Figure 10.

Transient Response Positive for Various V_{SUPPLY}

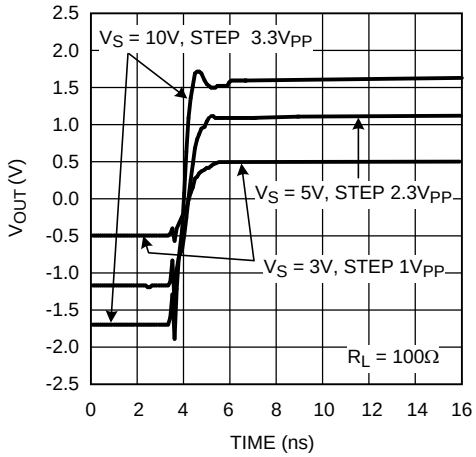


Figure 11.

Transient Response Negative for Various V_{SUPPLY}

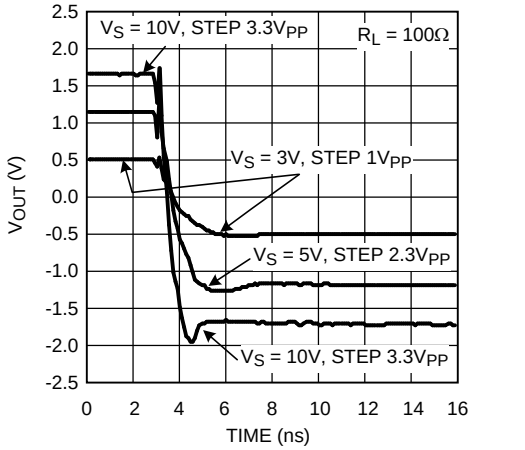


Figure 12.

Harmonic Distortion vs. V_{OUT} @ 5MHz

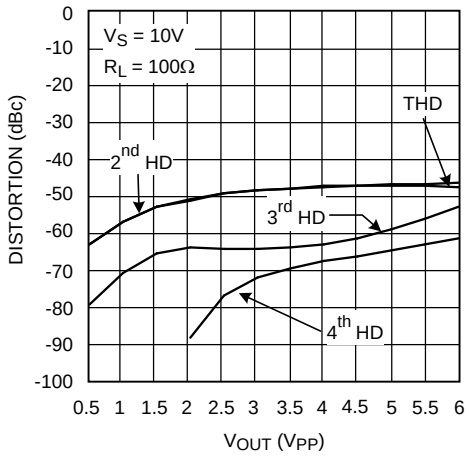


Figure 13.

Harmonic Distortion vs. V_{OUT} @ 10MHz

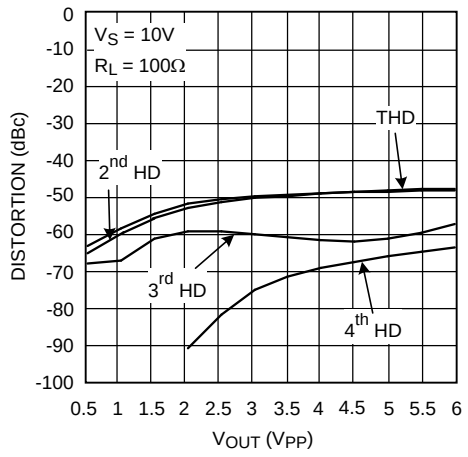


Figure 14.

Harmonic Distortion vs. V_{OUT} @ 20MHz

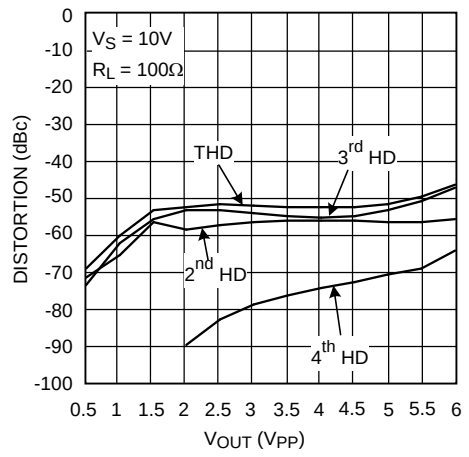


Figure 15.

Typical Performance Charac teristics (continued)

At T_J = 25°C; V^+ = +5V; V^- = −5V; Unless otherwise specified.

THD vs. V_{OUT} for Various Frequencies

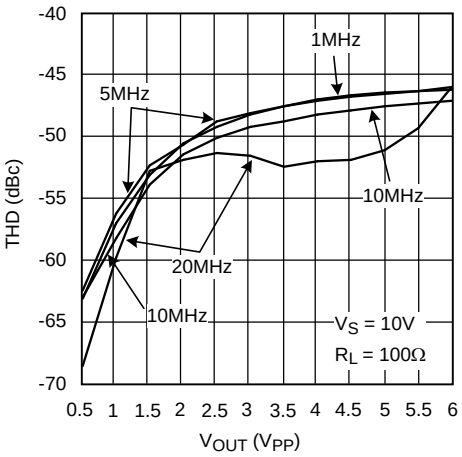


Figure 16.

Voltage Noise

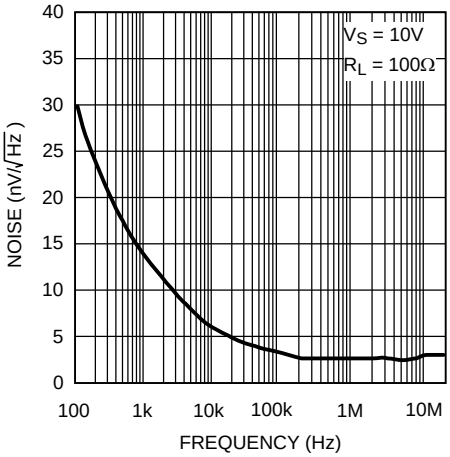


Figure 17.

Linearity V_{OUT} vs. V_{IN}

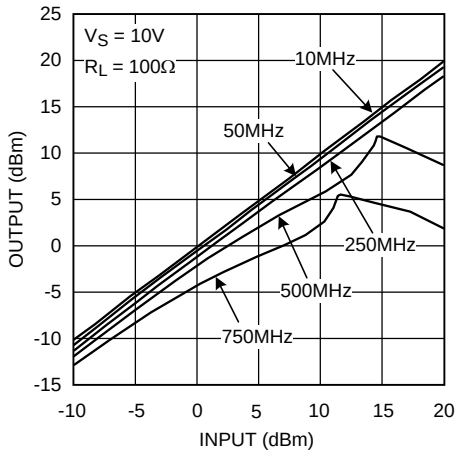


Figure 18.

V_{OS} vs. V_{SUPPLY} for 3 Units

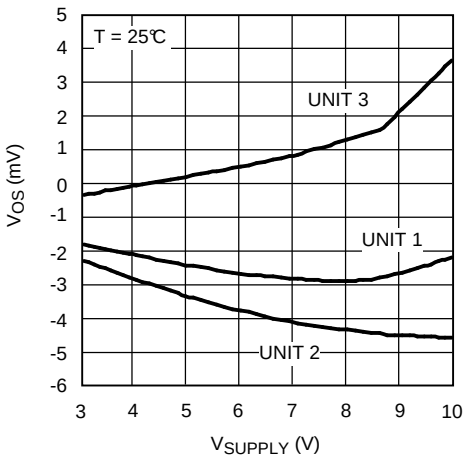


Figure 19.

V_{OS} vs. V_{SUPPLY} for Unit 1

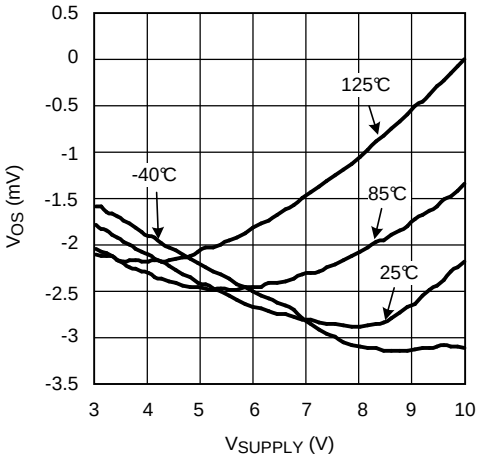


Figure 20.

V_{OS} vs. V_{SUPPLY} for Unit 2

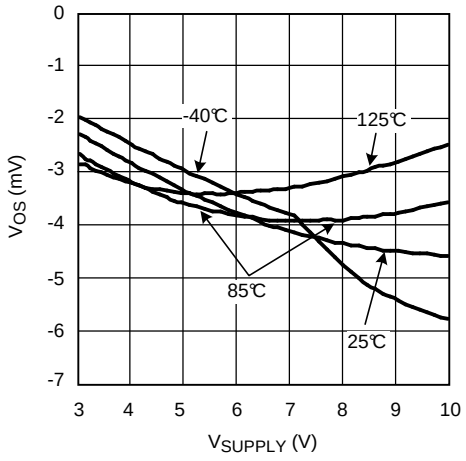


Figure 21.

Typical Performance Charac teristics (continued)

At T_J = 25°C; V^+ = +5V; V^- = −5V; Unless otherwise specified.

V_{OS} vs. V_{SUPPLY} for Unit 3

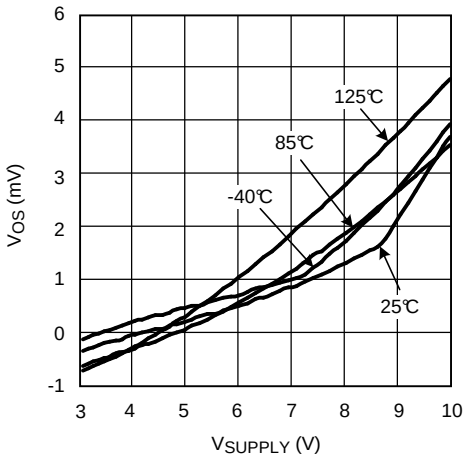


Figure 22.

I_B vs. V_{SUPPLY} (1)

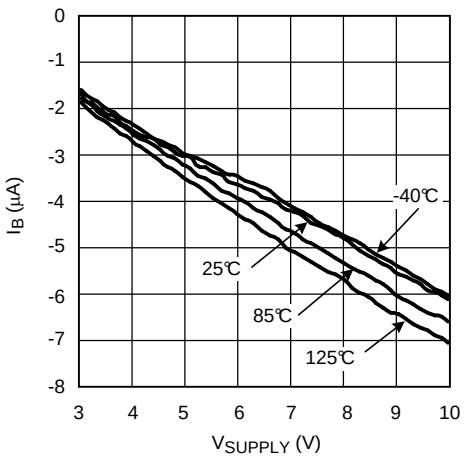


Figure 23.

R_{OUT} vs. Frequency

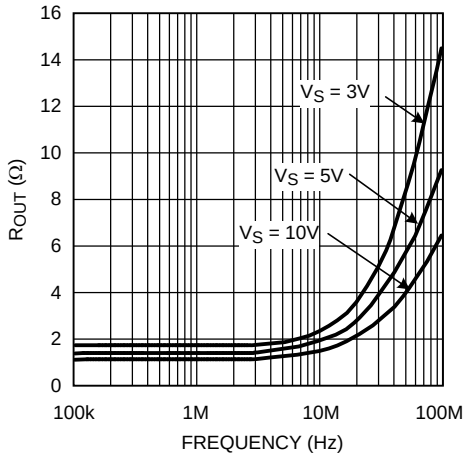


Figure 24.

PSRR vs. Frequency

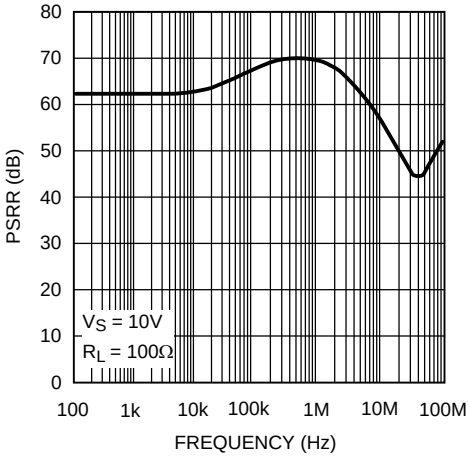


Figure 25.

I_{SUPPLY} vs. V_{SUPPLY}

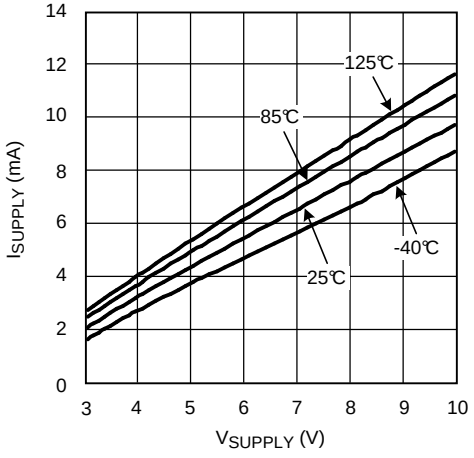


Figure 26.

I_{SUPPLY} vs. V_{IN}

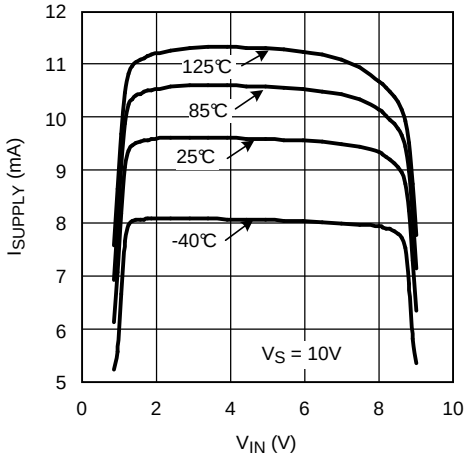


Figure 27.

(1) Positive current corresponds to current flowing into the device.

Typical Performance Charac teristics (continued)

At T_J = 25°C; V^+ = +5V; V^- = −5V; Unless otherwise specified.

V_{OUT} vs. I_{OUT} Sinking

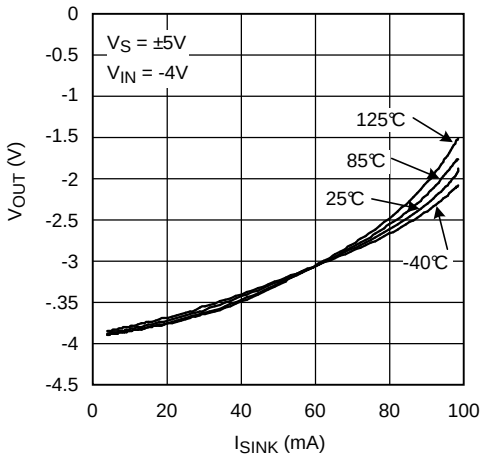


Figure 28.

V_{OUT} vs. I_{OUT} Sourcing

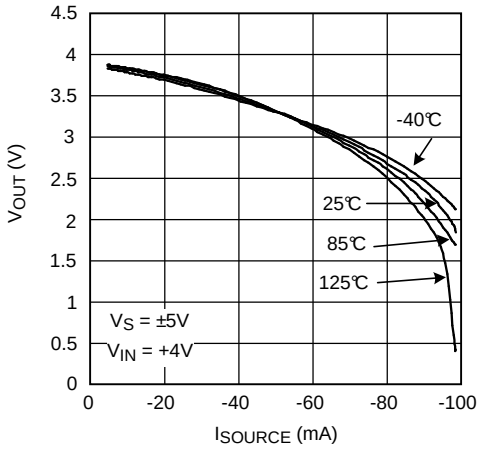


Figure 29.

I_O Sinking vs. V_{SUPPLY}

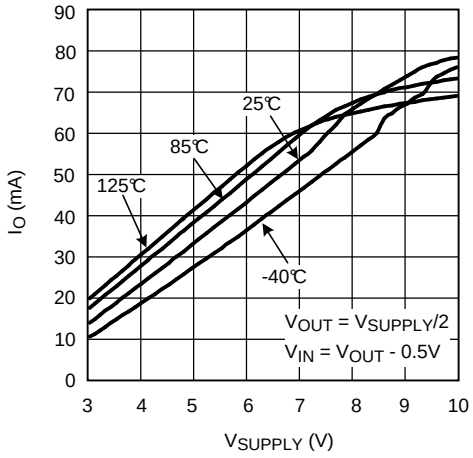


Figure 30.

I_O Sourcing vs. V_{SUPPLY}

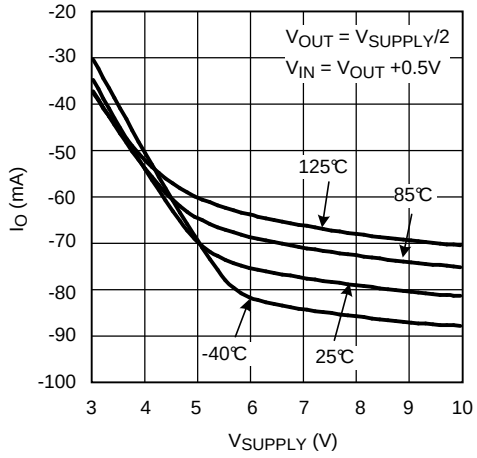


Figure 31.

Small Signal Pulse Response

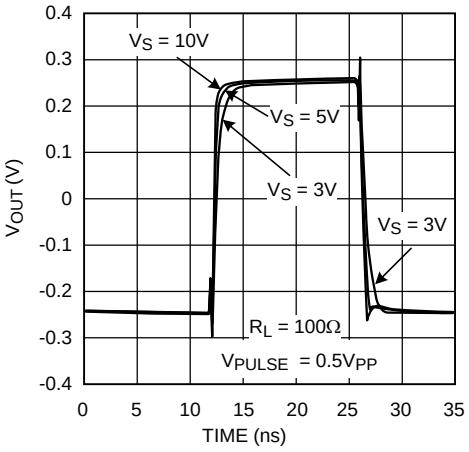


Figure 32.

Large Signal Pulse Response @ V_S = 3V

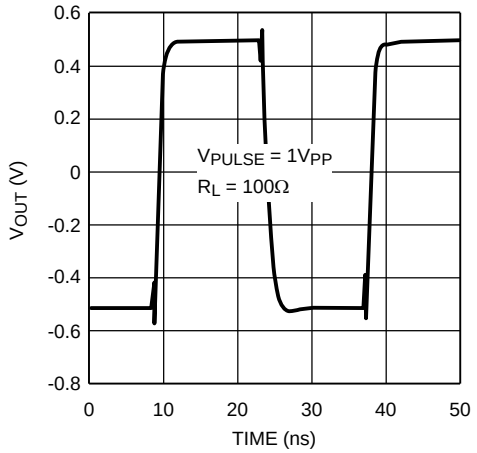


Figure 33.

Typical Performance Charac teristics (continued)

At T_J = 25°C; V^+ = +5V; V^- = −5V; Unless otherwise specified.

Large Signal Pulse Response @ V_S = 5V

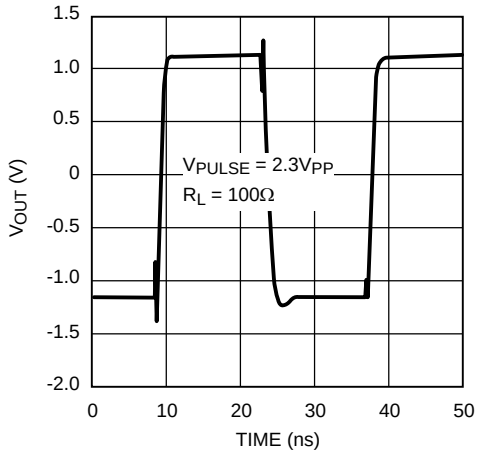


Figure 34.

Large Signal Pulse Response @ V_S = 10V

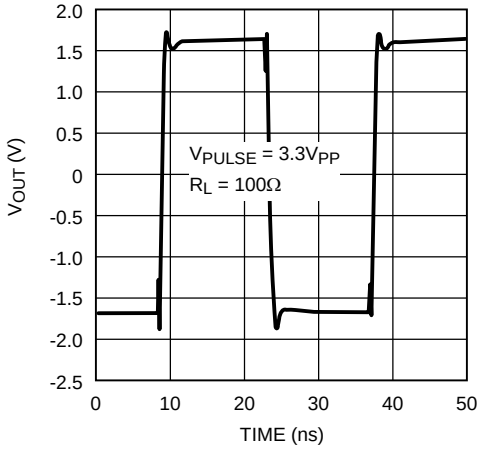


Figure 35.

APPLICATION NOTES

USING BUFFERS

A buffer is an electronic device delivering current gain but no voltage gain. It is used in cases where low impedances need to be driven and more drive current is required. Buffers need a flat frequency response and small propagation delay. Furthermore, the buffer needs to be stable under resistive, capacitive and inductive loads. High frequency buffer applications require that the buffer be able to drive transmission lines and cables directly.

IN WHAT SITUATION WILL WE USE A BUFFER?

In case of a signal source not having a low output impedance one can increase the output drive capability by using a buffer. For example, an oscillator might stop working or have frequency shift which is unacceptably high when loaded heavily. A buffer should be used in that situation. Also in the case of feeding a signal to an A/D converter it is recommended that the signal source be isolated from the A/D converter. Using a buffer assures a low output impedance, the delivery of a stable signal to the converter, and accommodation of the complex and varying capacitive loads that the A/D converter presents to the OpAmp. Optimum value is often found by experimentation for the particular application.

The use of buffers is strongly recommended for the handling of high frequency signals, for the distribution of signals through transmission lines or on pcb's, or for the driving of external equipment. There are several driving options:

- Use one buffer to drive one transmission line (see Figure 36)
- Use one buffer to drive to multiple points on one transmission line (see Figure 37)
- Use one buffer to drive several transmission lines each driving a different receiver. (see Figure 38)

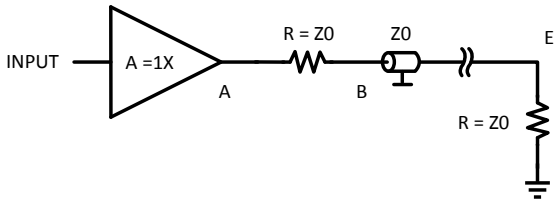


Figure 36.

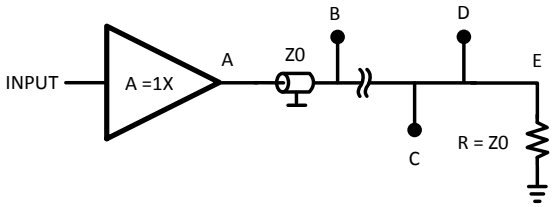


Figure 37.

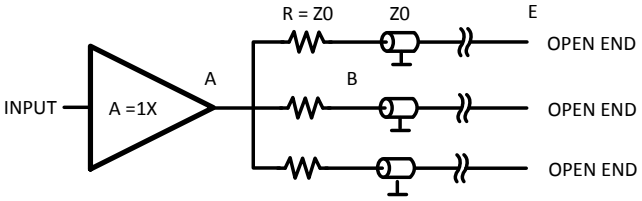


Figure 38.

In these three options it is seen that there is more than one preferred method to reach an (end) point on a transmission line. Until a certain point the designer can make his own choice but the designer should keep in mind never to break the rules about high frequency transport of signals. An explanation follows in the text below.

TRANSMISSION LINES

Introduction to transmission lines. The following is an overview of transmission line theory. Transmission lines can be used to send signals from DC to very high frequencies. At all points across the transmission line, Ohm's law must apply. For very high frequencies, parasitic behavior of the PCB or cables comes into play. The type of cable used must match the application. For example an audio cable looks like a coax cable but is unusable for radar frequencies at 10GHz. In this case one have to use special coax cables with lower attenuation and radiation characteristics.

Normally a pcb trace is used to connect components on a pcb board together. An important considerations is the amount of current carried by these pcb traces. Wider pcb traces are required for higher current densities and for applications where very low series resistance is needed. When routed over a ground plane, pcb traces have a defined Characteristic Impedance. In many design situations characteristic impedance is not utilized. In the case of high frequency transmission, however it is necessary to match the load impedance to the line characteristic impedance (more on this later). Each trace is associated with a certain amount of series resistance and series inductance plus each trace exhibits parallel capacitance to the ground plane. The combination of these parameters defines the line's characteristic impedance. The formula with which we calculate this impedance is as follows:

$Z_0 = \sqrt{(L/C)}$

In this formula L and C are the value/unit length, and R is assumed to be zero. C and L are unknown in many cases so we have to follow other steps to calculate the Z_0. The characteristic impedance is a function of the geometry of the cross section of the line. In (Figure 39) we see three cross sections of commonly used transmission lines.

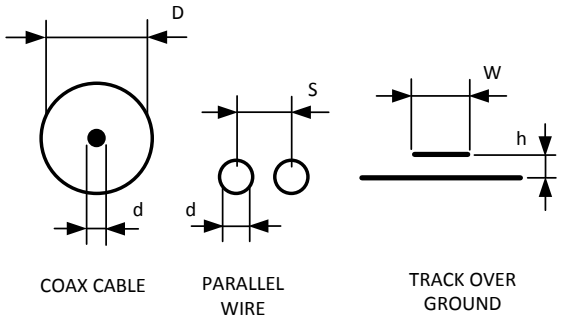


Figure 39.

Z_0 can be calculated by knowing some of the physical dimensions of the pcb line, such as pcb thickness, width of the trace and ε_r, relative dielectric constant. The formula given in transmission line theory for calculating Z_0 is as follows:

$$Z = \frac{87}{\sqrt{(\varepsilon r + 1.41)}} \times \ln \frac{(5.98 \times h)}{(th + 0.8W)} \quad (1)$$

where

- $\boldsymbol{\varepsilon_r}$= relative dielectric constant
- **h**= pcb height
- **W**= trace width
- **th**= thickness of the copper

If we ignore the thickness of the copper in comparison to the width of the trace then we have the following equation:

$$Z = \frac{87}{\sqrt{(\varepsilon r + 1.41)}} \times \ln \frac{(5.98 \times h)}{(0.8W)} \quad (2)$$

With this formula it is possible to calculate the line impedance vs. the trace width. Figure 40 shows the impedance associated with a given line width. Using the same formula it is also possible to calculate what happens when ε_r varies over a certain range of values. Varying the ε_r over a range of 1 to 10 gives a variation for the Characteristic Impedance of about 40Ω from 80Ω to 38Ω. Most transmission lines are designed to have 50Ω or 75Ω impedance. The reason for that is that in many cases the pcb trace has to connect to a cable whose impedance is either 50Ω or 75Ω. As shown ε_r and the line width influence this value.

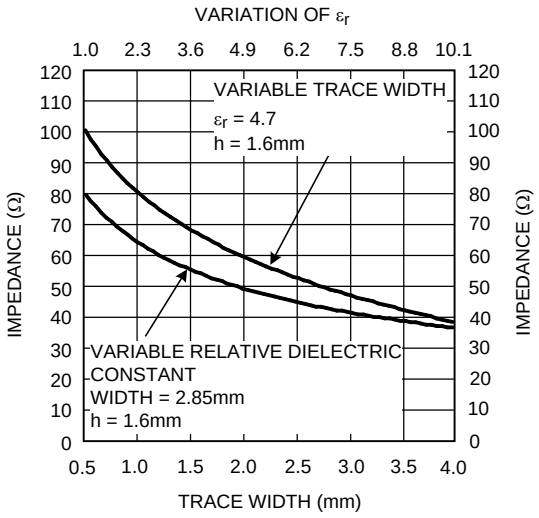


Figure 40.

Next, there will be a discussion of some issues associated with the interaction of the transmission line at the source and at the load.

Connecting A Load Using A Transmission Line

In most cases, it is unrealistic to think that we can place a driver or buffer so close to the load that we don't need a transmission line to transport the signal. The pcb trace length between a driver and the load may affect operation depending upon the operating frequency. Sometimes it is possible to do measurements by connecting the DUT directly to the analyzer. As frequencies become higher the short lines from the DUT to the analyzer become long lines. When this happens there is a need to use transmission lines. The next point to examine is what happens when the load is connected to the transmission line. When driving a load, it is important to match the line and load impedance, otherwise reflections will occur and this phenomena will distort the signal. If a transient is applied at T = 0 (Figure 41, trace A) the resultant waveform may be observed at the start point of the transmission line. At this point (begin) on the transmission line the voltage increases to (V) and the wave front travels along the transmission line and arrives at the load at T = 10. At any point across along the line $I = V/Z_0$, where Z_0 is the impedance of the transmission line. For an applied transient of 2V with $Z_0 = 50\Omega$ the current from the buffer output stage is 40mA. Many vintage opamps cannot deliver this level of current because of an output current limitation of about 20mA or even less. At T = 10 the wave front arrives at the load. Since the load is perfectly matched to the transmission line all of the current traveling across the line will be absorbed and there will be no reflections. In this case source and load voltages are exactly the same. When the load and the transmission line have unequal values of impedance a different situation results. Remember there is another basic which says that energy cannot be lost. The power in the transmission line is $P = V^2/R$. In our example the total power is $2^2/50 = 80mW$. Assume a load of 75Ω. In that case a power of 80mW arrives at the 75Ω load and causes a voltage of the proper amplitude to maintain the incoming power.

$$V = \sqrt{(P \times R)} = \sqrt{(80 \times 10^{-3} \times 75)} = 2.45V \quad (3)$$

The voltage wavefront of 2.45V will now set about traveling back over the transmission line towards the source, thereby resulting in a reflection caused by the mismatch. On the other hand if the load is less then 50Ω the backwards traveling wavefront is subtracted from the incoming voltage of 2V. Assume the load is 40Ω. Then the voltage across the load is:

$$\sqrt{(80 \times 10^{-3} \times 40)} = 1.79V \quad (4)$$

This voltage is now traveling backwards through the line toward the start point. In the case of a sinewave interferences develop between the incoming waveform and the backwards-going reflections, thus distorting the signal. If there is no load at all at the end point the complete transient of 2V is reflected and travels backwards to the beginning of the line. In this case the current at the endpoint is zero and the maximum voltage is reflected. In the case of a short at the end of the line the current is at maximum and the voltage is zero.

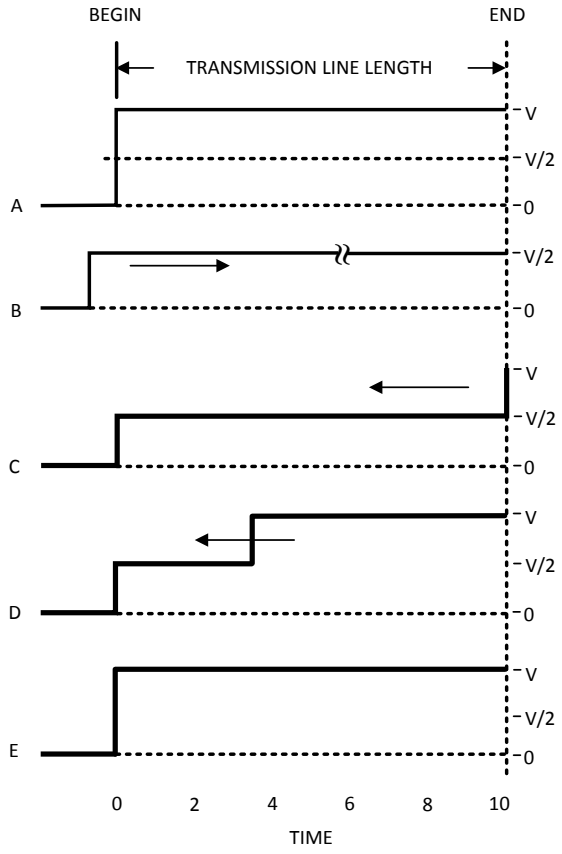


Figure 41.

Using Serial And Parallel Termination

Many applications, such as video, use a series resistance between the driver and the transmission line (see Figure 36). In this case the transmission line is terminated with the characteristic impedance at both ends of the line. See Figure 41 trace B. The voltage traveling through the transmission line is half the voltage seen at the output of the buffer, because the series resistor in combination with Z_0 forms a two-to-one voltage divider. The result is a loss of 6dB. For video applications, amplifier gain is set to 2 in order to realize an overall gain of 1. Many operational amplifiers have a relatively flat frequency response when set to a gain of two compared to unity gain. In trace B it is seen that, if the voltage reaches the end of the transmission line, the line is perfectly matched and no reflections will occur. The end point voltage stays at half the output voltage of the opamp or buffer.

Driving More Than One Input

Another transmission line possibility is to route the trace via several points along a transmission line (Figure 37) This is only possible if care is taken to observe certain restrictions. Failure to do so will result in impedance discontinuities that will cause distortion of the signal. In the configuration of Figure 37 there is a transmission line connected to the buffer output and the end of the line is terminated with Z_0. We have seen in the Connecting A Load Using A Transmission Line section that for the condition above, the signal throughout the entire transmission line has the same value, that the value is the nominal value initiated by the opamp output, and no reflections occur at the end point. Because of the lack of reflections no interferences will occur. Consequently the signal has every where on the line the same amplitude. This allows the possibility of feeding this signal to the input port of any device which has high ohmic impedance and low input capacitance. In doing so keep in mind that the transient arrives at different times at the connected points in the transmission line. The speed of light in vacuum, which is about $3 * 10^8$ m/sec, reduces through a transmission line or a cable down to a value of about $2 * 10^8$ m/sec. The distance the signal will travel in 1ns is calculated by solving the following formula:

$$S = V*t \quad (5)$$

where

- S = distance
- V = speed in the cable
- t = time

This calculation gives the following result: $s = 2*10^8 * 1*10^{-9} = 0.2m$

That is for each nanosecond the wave front shifts 20cm over the length of the transmission line. Keep in mind that in a distance of just 2cm the time displacement is already 100ps.

Using Serial Termination To More Than One Transmission Line

Another way to reach several points via a transmission line is to start several lines from one buffer output (see Figure 38). This is possible only if the output can deliver the needed current into the sum of all transmission lines. As can be seen in this figure there is a series termination used at the beginning of the transmission line and the end of the line has no termination. This means that only the signal at the endpoint is usable because at all other points the reflected signal will cause distortion over the line. Only at the endpoint will the measured signal be the same as at the startpoint. Referring to Figure 41 trace C, the signal at the beginning of the line has a value of V/2 and at T = 0 this voltage starts traveling towards the end of the transmission line. Once at the endpoint the line has no termination and 100% reflection will occur. At T = 10 the reflection causes the signal to jump to 2V and to start traveling back along the line to the buffer (see Figure 41 trace D). Once the wavefront reaches the series termination resistor, provided the termination value is Z_0, the wavefront undergoes total absorption by the termination. This is only true if the output impedance of the buffer/driver is low in comparison to the characteristic impedance Z_0. At this moment the voltage in the whole transmission line has the nominal value of 2V (see Figure 41 trace E). If the three transmission lines each have a different length the particular point in time at which the voltage at the series termination resistor jumps to 2V is different for each case. However, this transient is not transferred to the other lines because the output of the buffer is low and this transient is highly attenuated by the combination of the termination resistor and the output impedance of the buffer. A simple calculation illustrates the point. Assume that the output impedance is 5Ω. For the frequency of interest the attenuation is $V_B/V_A = 55/5 = 11$, where A and B are the points in Figure 38. In this case the voltage caused by the reflection is 2/11 = 0.18V. This voltage is transferred to the remaining transmission lines in sequence and following the same rules as before this voltage is seen at the end points of those lines. The lower the output resistance the higher the decoupling between the different lines. Furthermore one can see that at the endpoint of these transmission lines there is a normal transient equal to the original transient at the beginning point. However at all other points of the transmission line there is a step voltage at different distances from the startpoint depending at what point this is measured (see trace D).

Measuring The Length Of A Transmission Line

An open transmission line can be used to measure the length of a particular transmission line. As can be seen in Figure 42 the line of interest has a certain length. A transient is applied at T = 0 and at that point in time the wavefront starts traveling with an amplitude of V/2 towards the end of the line where it is reflected back to the startpoint.

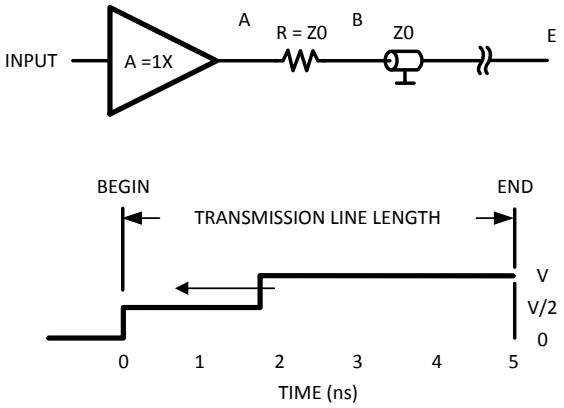


Figure 42.

To calculate the length of the line it is necessary to measure immediately after the series termination resistor. The voltage at that point remains at half nominal voltage, thus V/2, until the reflection returns and the voltage jumps to V. During an interval of 5ns the signal travels to the end of the line where the wave front is reflected and returns to the measurement point. During the time interval when the wavefront is traveling to the end of the transmission line and back the voltage has a value of V/2. This interval is 10ns. The length can be calculated with the following formula: S = (V*T)/2

$$S = \frac{(2 \times 10^{8}) \times (10 \times 10^{-9})}{2} = 1\text{mtr} \quad (6)$$

As calculated before in the Driving More Than One Input section the signal travels 20cm/ns so in 5ns this distance indicated distance is 1m. So this example is easily verified.

APPLYING A CAPACITIVE LOAD

The assumption of pure resistance for the purpose of connecting the output stage of a buffer or opamp to a load is appropriate as a first approximation. Unfortunately that is only a part of the truth. Associated with this resistor is a capacitor in parallel and an inductor in series. Any capacitance such as C_L-1 which is connected directly to the output stage is active in the loop gain as seen in Figure 43. Output capacitance, present also at the minus input in the case of a buffer, causes an increasing phase shift leading to instability or even oscillation in the circuit.

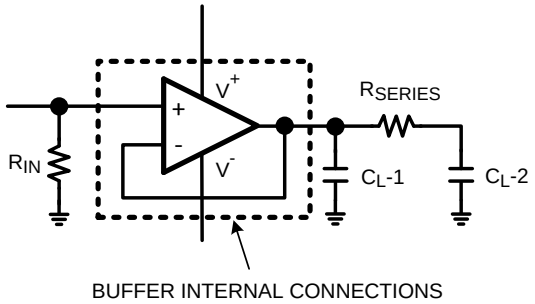


Figure 43.

Unfortunately the leads of the output capacitor also contain series inductors which become more and more important at high frequencies. At a certain frequency this series capacitor and inductor forms an LC combination which becomes series resonant. At the resonant frequency the reactive component vanishes leaving only the ohmic resistance (R-1 or R-2) of the series L/C combination. (see Figure 44).

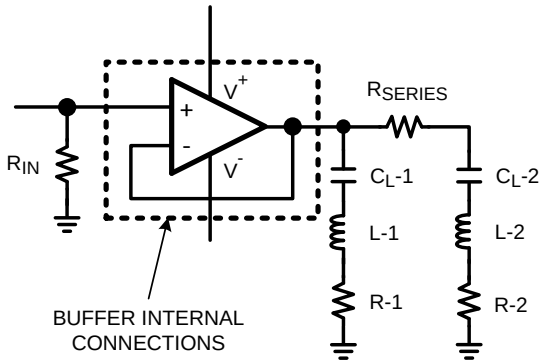


Figure 44.

Consider a frequency sweep over the entire spectrum for which the LMH6559 high frequency buffer is active. In the first instance peaking occurs due to the parasitic capacitance connected at the load whereas at higher frequencies the effects of the series combination of L and C become noticeable. This causes a distinctive dip in the output frequency sweep and this dip varies depending upon the particular capacitor as seen in Figure 45.

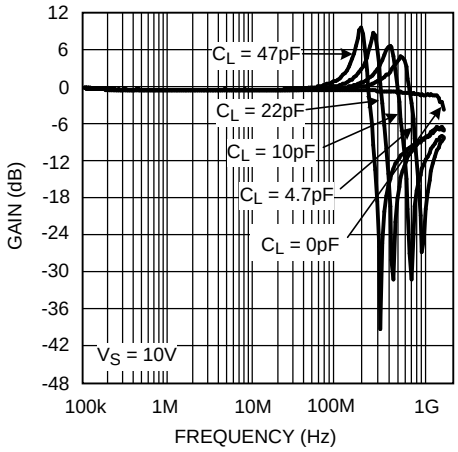


Figure 45.

To minimize peaking due to CL a series resistor for the purpose of isolation from the output stage should be used. A low valued resistor will minimize the influence of such a load capacitor. In a 50Ω system as is common in high frequency circuits a 50Ω series resistor is often used. Usage of the series resistor, as seen in Figure 46 eliminates the peaking but not the dip. The dip will vary with the particular capacitor. Using a resistor in series with a capacitor creates in a single pole situation a 6dB/oct rolloff. However, at high frequencies the internal inductance is appreciable and forms a series LC combination with the capacitor. Choice of a higher valued resistor, for example 500 to 1kΩ, and a capacitor of hundreds of pF's provides the expected response at lower frequencies.

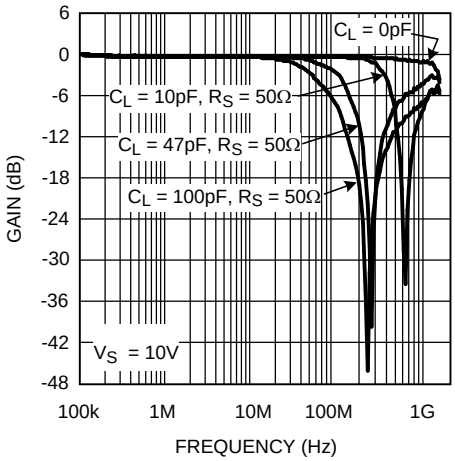


Figure 46.

USING GROUND PLANES

The use of ground planes is recommended both for providing a low impedance path to ground (or to one of the other supply voltages) and also for forming effective controlled impedance transmission lines for the high frequency signal flow on the board. Multilayer boards often make use of inner conductive layers for routing supply voltages. These supply voltage layers form a complete plane rather than using discrete traces to connect the different points together for the specified supply. Signal traces on the other hand are routed on outside layers both top and bottom. This allows for easy access for measurement purposes. Fortunately, only very high density boards have signal layers in the middle of the board. In an earlier section, the formula for Z_0 was derived as:

$$Z = \frac{87}{\sqrt{(\varepsilon r + 1.41)}} \times \ln \frac{(5.98 \times h)}{(0.8W)} \tag{7}$$

The width of a trace is determined by the thickness of the board. In the case of a multilayer board the thickness is the space between the trace and the first supply plane under this trace layer. By common practice, layers do not have to be evenly divided in the construction of a pcb. Refer to Figure 47. The design of a transmission line design over a pcb is based upon the thickness of the different internal layers and the ε_r of the board material. The pcb manufacturer can supply information about important specifications. For example, a nominal 1.6mm thick pcb produces a 50Ω trace for a calculated width of 2.9mm. If this layer has a thickness of 0.35mm and for the same ε_r, the trace width for 50Ω should be of 0.63mm, as calculated from Equation 8, a derivation from Equation 7.

$$w = \frac{5.98 \times h}{e^{A}}$$

$$\text{where } A = \frac{\left[Z_O \times \sqrt{(\varepsilon_r + 1.41)}\right]}{87} \tag{8}$$

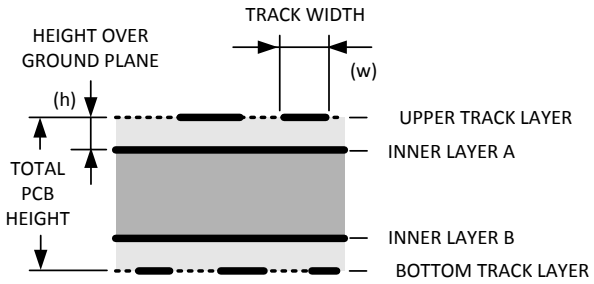


Figure 47.

Using a trace over a ground plane has big advantages over the use of a standard single or double sided board. The main advantage is that the electric field generated by the signal transported over this trace is fixed between the trace and the ground plane e.g. there is almost no possibility of radiation (see Figure 48).

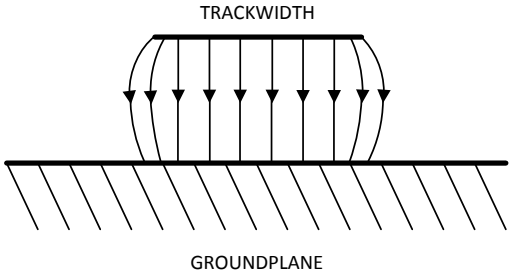


Figure 48.

This effect works to both sides because the circuit will not generate radiation but the circuit is also not sensible if exposed to a certain radiation level. The same is also noticeable when placing components flat on the printed circuit board. Standard through hole components when placed upright can act as an antenna causing an electric field which could be picked up by a nearby upright component. If placed directly at the surface of the pcb this influence is much lower.

The Effect Of Variation For ε_r

When using pcb material the ε_r has a certain shift over the used frequency spectrum, so if necessary to work with very accurate trace impedances one must taken into account for which frequency region the design has to be functional. Figure 49 (Courtesy of Islola Corporation) gives an example what the drift in ε_r will be when using the pcb material produced by Isola. If working at frequencies of 100MHz then a 50Ω trace has a width of 3.04mm for standard 1.6mm FR4 pcb material, and the same trace needs a width of 3.14mm. for frequencies around 10GHz.

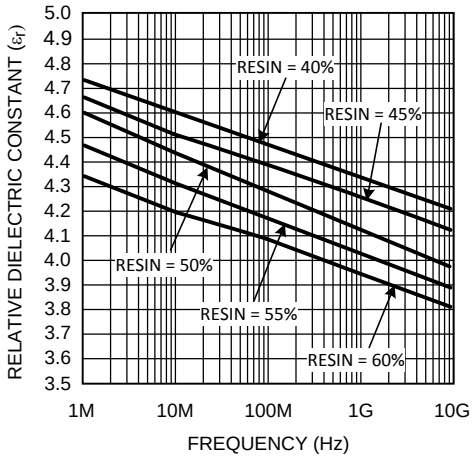


Figure 49.

Routing Power Traces

Power line traces routed over a pcb should be kept together for best practice. If not a ground loop will occur which may cause more sensitivity to radiation. Also additional ground trace length may lead to more ringing on digital signals. Careful attention to power line distribution leads to improved overall circuit performance. This is especially valid for analog circuits which are more sensitive to spurious noise and other unwanted signals.

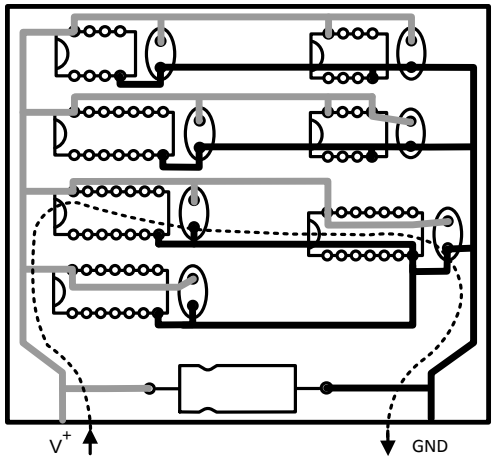


Figure 50.

As demonstrated in Figure 50 the power lines are routed from both sides on the pcb. In this case a current loop is created as indicated by the dotted line. This loop can act as an antenna for high frequency signals which makes the circuit sensitive to R_F radiation. A better way to route the power traces can be seen in the following setup. (see Figure 51)

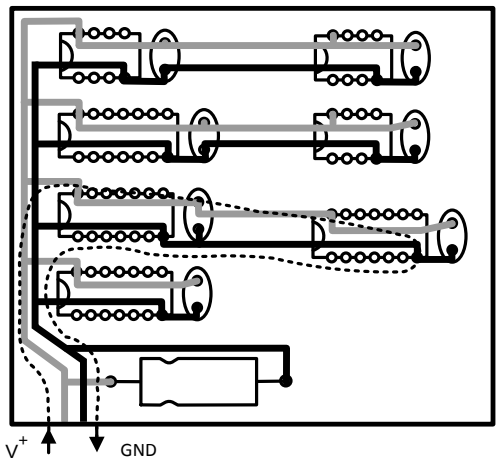


Figure 51.

In this arrangement the power lines have been routed in order to avoid ground loops and to minimize sensitivity to noise etc. The same technique is valid when routing a high frequent signal over a board which has no ground plane. In that case is it good practice to route the high frequency signal alongside a ground trace. A still better way to create a pcb carrying high frequency signals is to use a pcb with a ground plane or planes.

Discontinuities In A Ground Plane

A ground plane with traces routed over this plane results in the build up of an electric field between the trace and the ground plane as seen in Figure 48. This field is build up over the entire routing of the trace. For the highest performance the ground plane should not be interrupted because to do so will cause the field lines to follow a roundabout path. In Figure 52 it was necessary to interrupt the ground plane with a crossing trace. This interruption causes the return current to follow a longer route than the signal path follows to overcome the discontinuity.

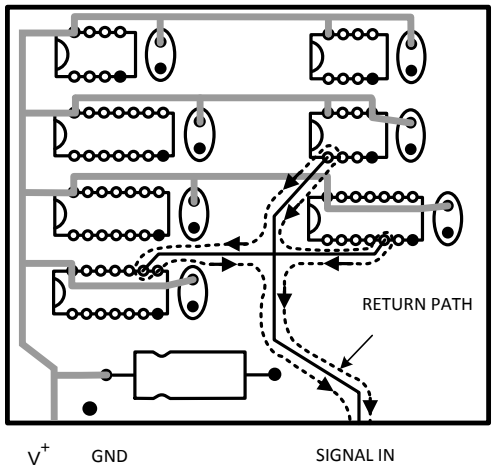


Figure 52.

If needed it is possible to bypass the interruption with traces that are parallel to the signal trace in order to reduce the negative effects of the discontinuity in the ground plane. In doing so, the current in the ground plane closely follows the signal trace on the return path as can be seen in Figure 53. Care must be taken not to place too many traces in the ground plane or the ground plane effectively vanishes such that even bypasses are unsuccessful in reducing negative effects.

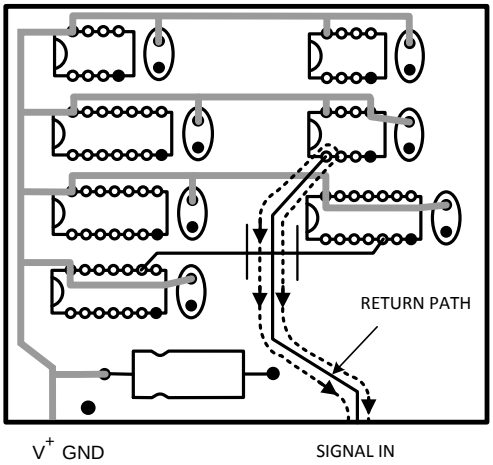


Figure 53.

If the overall density becomes too high it is better to make a design which contains additional metal layers such that the ground planes actually function as ground planes. The costs for such a pcb are increased but the payoff is in overall effectiveness and ease of design.

Ground Planes At Top And Bottom Layer Of A PCB

In addition to the bottom layer ground plane another useful practice is to leave as much copper as possible at the top layer. This is done to reduce the amount of copper to be removed from the top layer in the chemical process. This causes less pollution of the chemical baths allowing the manufacturer to make more pcb's with a certain amount of chemicals. Connecting this upper copper to ground provides additional shielding and signal performance is enhanced. For lower frequencies this is specifically true. However, at higher frequencies other effects become more and more important such that unwanted coupling may result in a reduction in the bandwidth of a circuit. In the design of a test circuit for the LMH6559 this effect was clearly noticeable and the useful bandwidth was reduced from 1500MHz to around 850MHz.

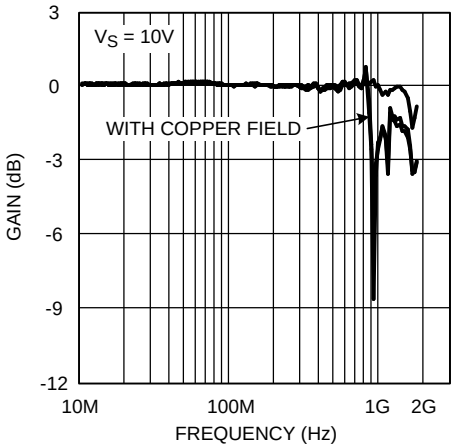


Figure 54.

As can be seen in Figure 54 the presence of a copper field close to the transmission line to and from the buffer causes unwanted coupling effects which can be seen in the dip at about 850MHz. This dip has a depth of about 5dB for the case when all of the unused space is filled with copper. In case of only one area being filled with copper this dip is about 9dB.

PCB Board Layout And Component Selection

Sound practice in the area of high frequency design requires that both active and passive components be used for the purposes for which they were designed. It is possible to amplify signals at frequencies of several hundreds of MHz using standard through hole resistors. Surface mount devices, however, are better suited for this purpose. Surface mount resistors and capacitors are smaller and therefore parasitics are of lower value and therefore have less influence on the properties of the amplifier. Another important issue is the pcb itself, which is no longer a simple carrier for all the parts and a medium to interconnect them. The pcb board becomes a real component itself and consequently contributes its own high frequency properties to the overall performance of the circuit. Sound practice dictates that a design have at least one ground plane on a pcb which provides a low impedance path for all decoupling capacitors and other ground connections. Care should be taken especially that on- board transmission lines have the same impedance as the cables to which they are connected - 50Ω for most applications and 75Ω in case of video and cable TV applications. Such transmission lines usually require much wider traces on a standard double sided PCB board than needed for a 'normal' trace. Another important issue is that inputs and outputs must not 'see' each other. This occurs if inputs and outputs are routed together over the pcb with only a small amount of physical separation, particularly when there is a high differential in signal level between them. Furthermore components should be placed as flat and low as possible on the surface of the PCB. For higher frequencies a long lead can act as a coil, a capacitor or an antenna. A pair of leads can even form a transformer. Careful design of the pcb avoids oscillations or other unwanted behaviors. For ultra high frequency designs only surface mount components will give acceptable results. (for more information see OA-15 (Literature Number SNOA367).

TI suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization.

Device	Package	Evaluation Board Part Number
LMH6559MA	SOIC	CLC730245
LMH6559MAX	SOIC	CLC730245
LMH6559MF	SOT-23	CLC730136
LMH6559MFX	SOT-23	CLC730136

These free evaluation boards are shipped when a device sample request is placed with Texas Instruments.

POWER SEQUENCING OF THE LMH6559

Caution should be exercised in applying power to the LMH6559. When the negative power supply pin is left floating it is recommended that other pins, such as positive supply and signal input should also be left unconnected. If the ground is floating while other pins are connected the input circuitry is effectively biased to ground, with a mostly low ohmic resistor, while the positive power supply is capable of delivering significant current through the circuit. This causes a high input bias current to flow which degrades the input junction. The result is an input bias current which is out of specification. When using inductive relays in an application care should be taken to connect first both power connections before connecting the bias resistor to the input.

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	27

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6559MA	LIFEBUY	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LMH65 59MA	
LMH6559MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 59MA	Samples
LMH6559MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH65 59MA	Samples
LMH6559MF	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	B05A	
LMH6559MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	B05A	Samples
LMH6559MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	B05A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

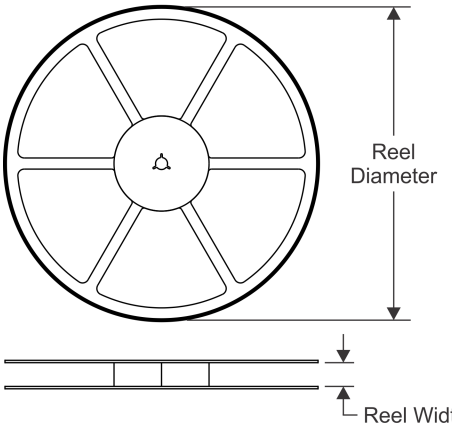
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

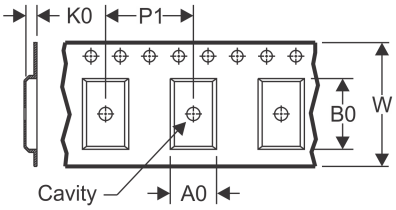
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

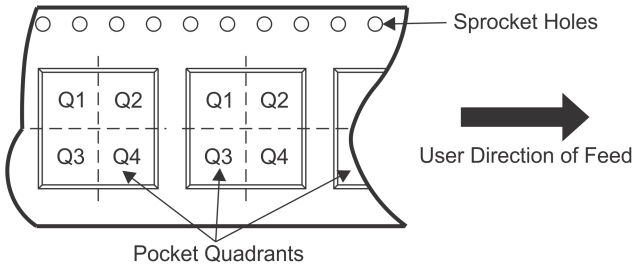


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

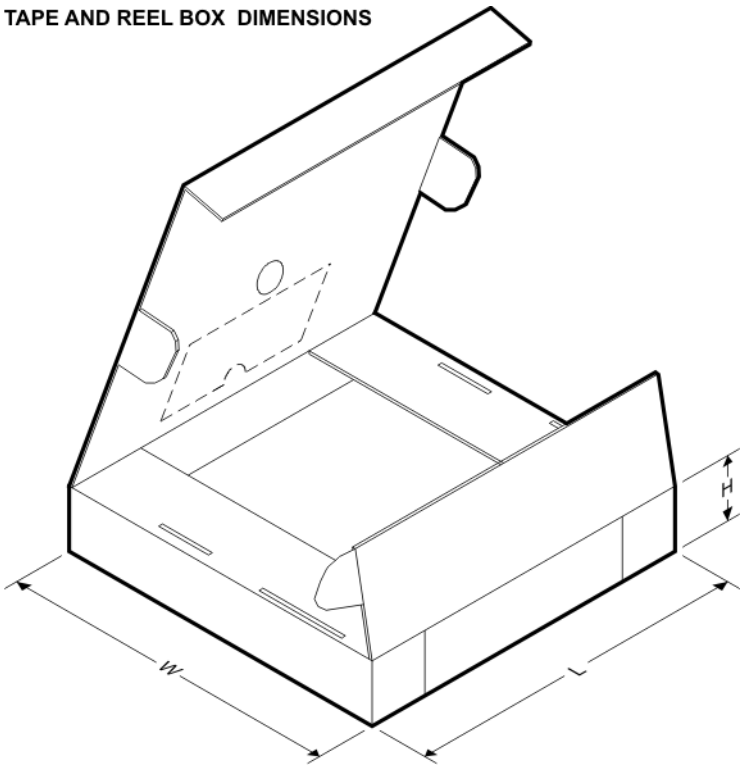
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6559MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6559MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6559MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6559MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

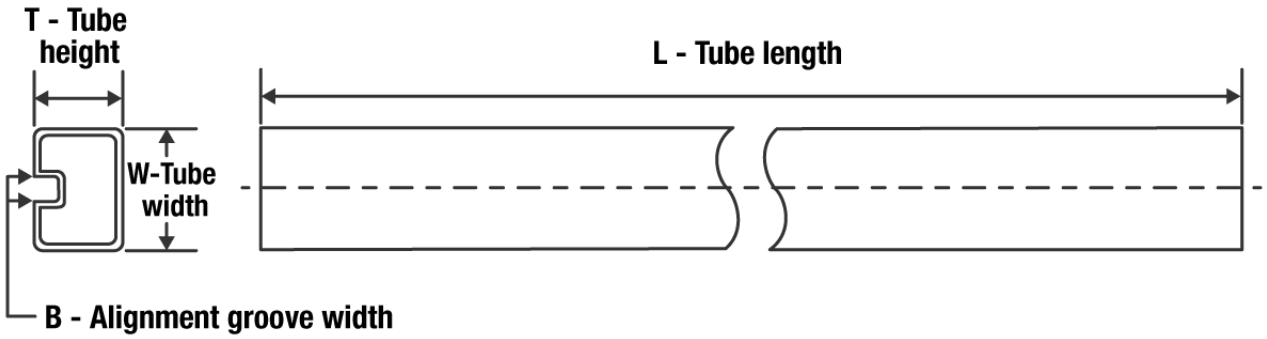
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

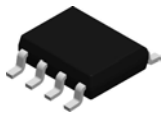
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6559MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6559MF	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMH6559MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMH6559MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6559MA	D	SOIC	8	95	495	8	4064	3.05
LMH6559MA	D	SOIC	8	95	495	8	4064	3.05
LMH6559MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

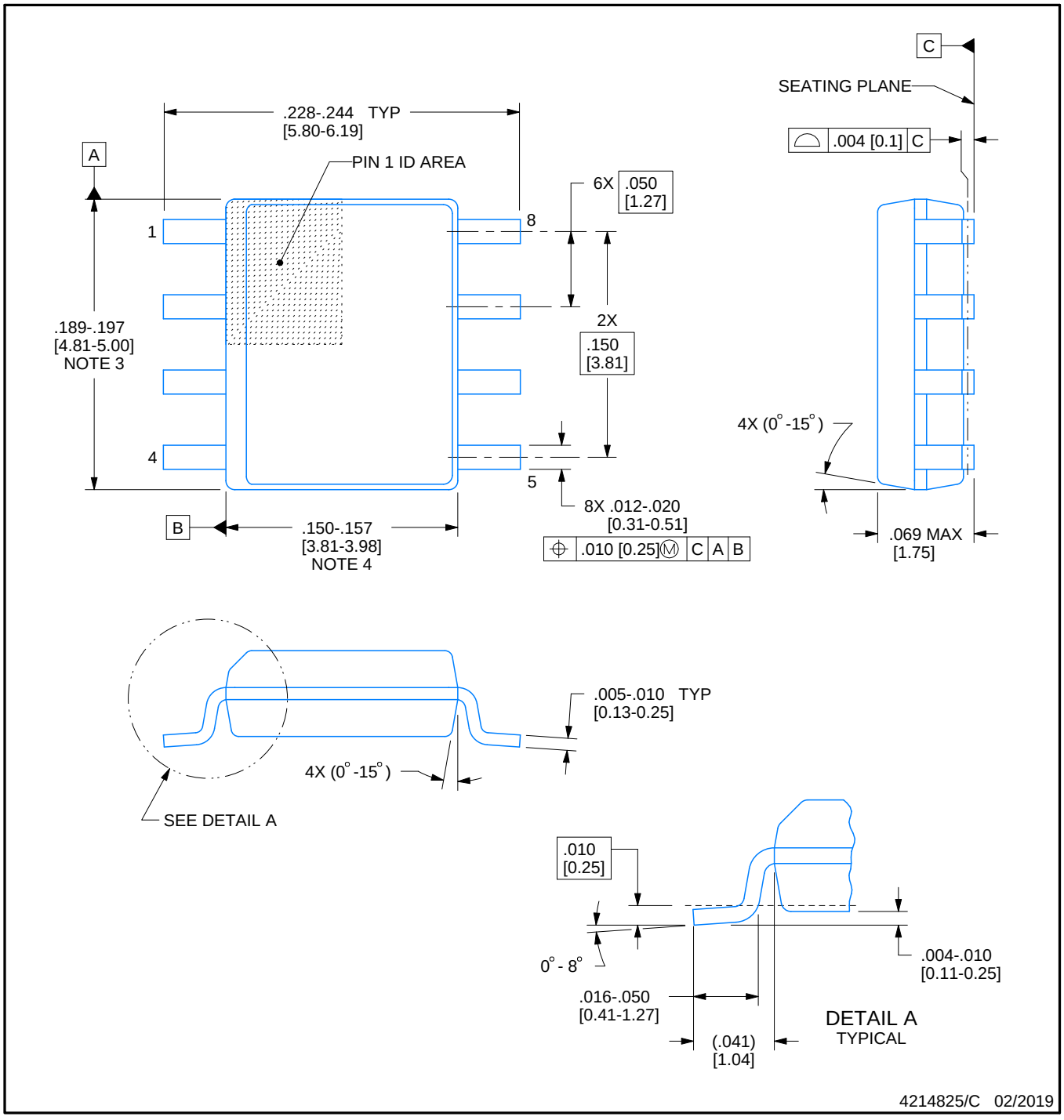


PACKAGE OUTLINE

D0008A

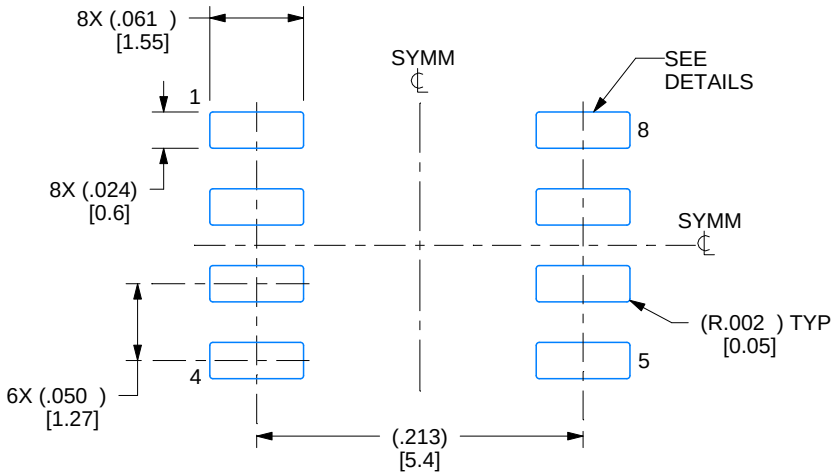
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

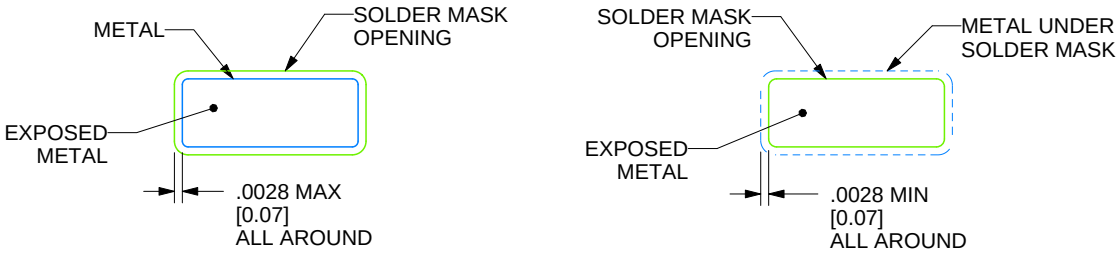


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

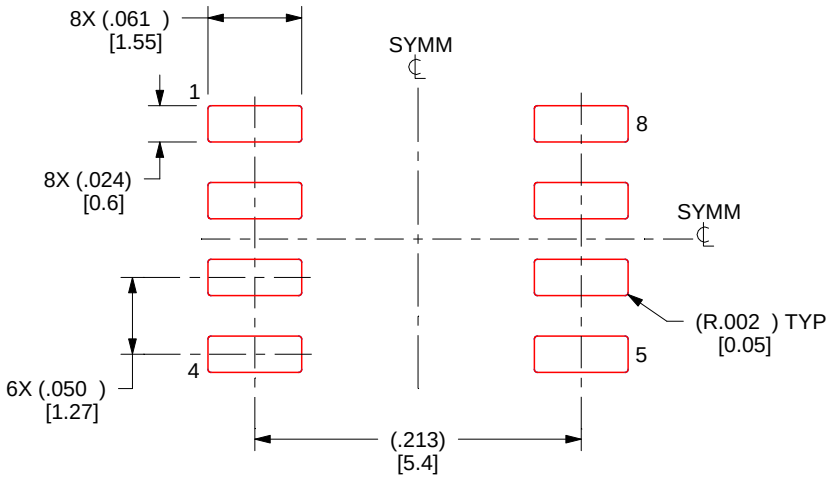
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

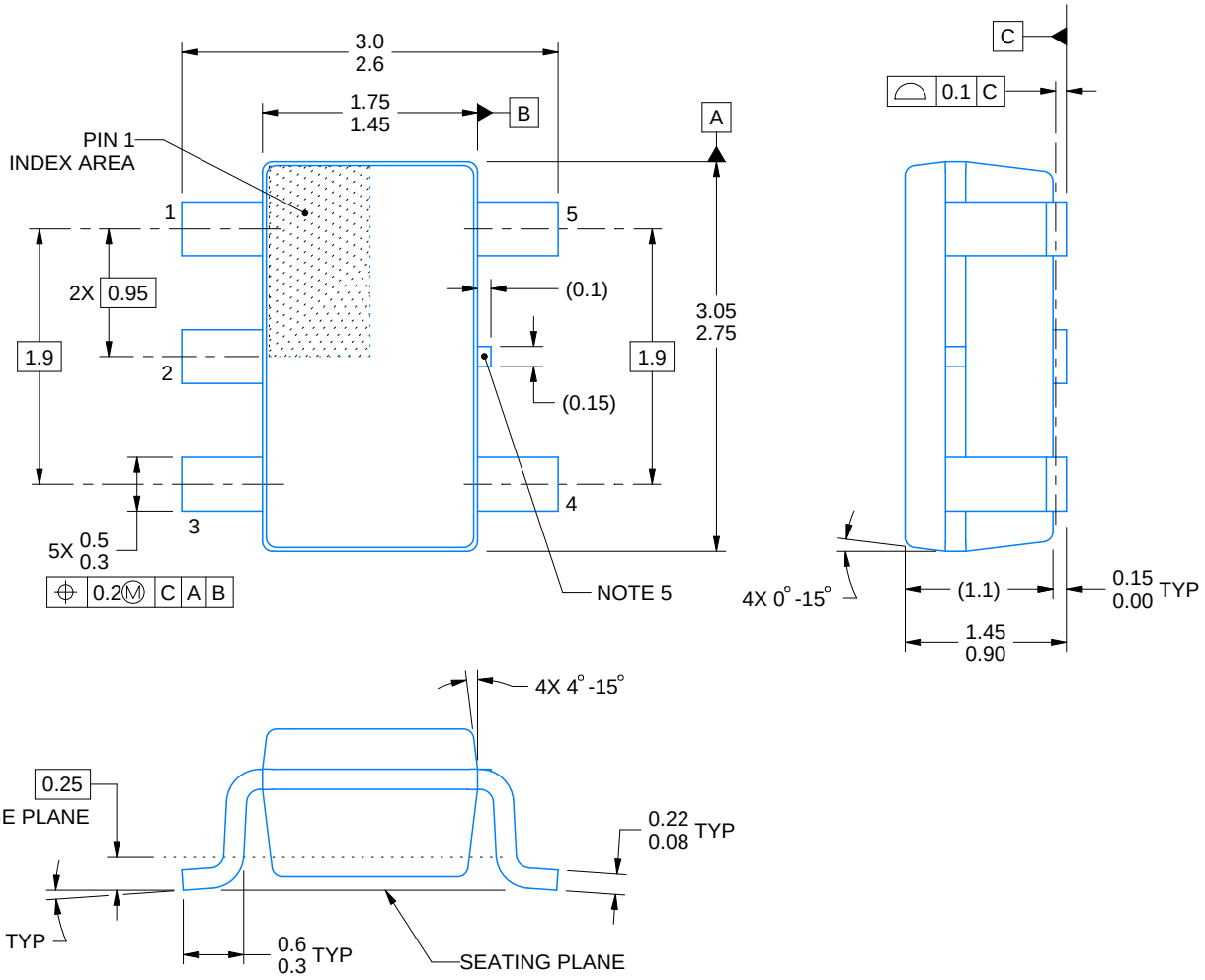
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

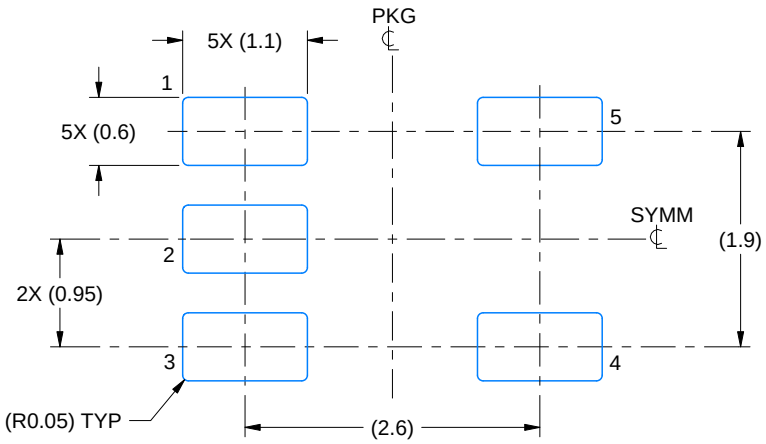
SMALL OUTLINE TRANSISTOR



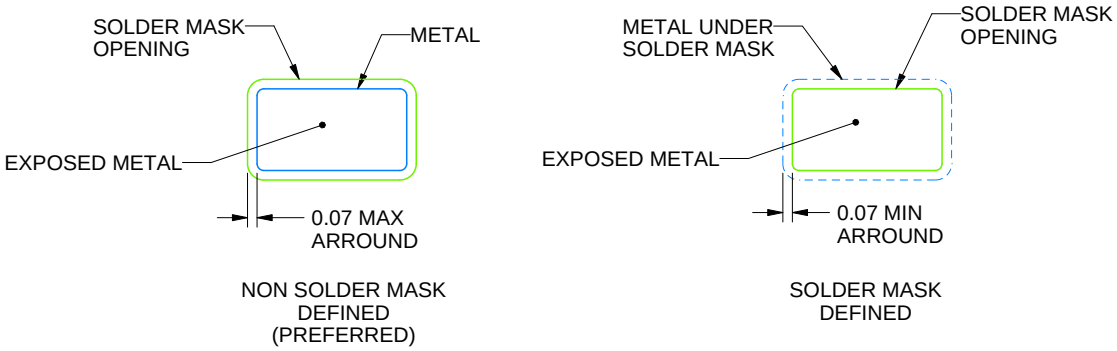
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

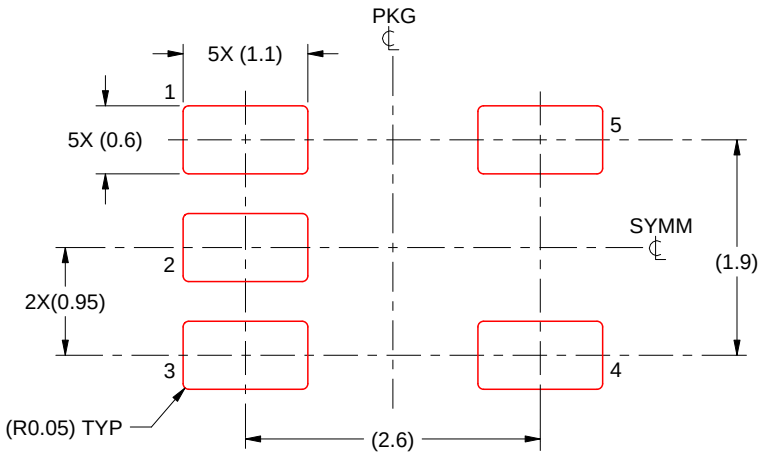


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265