LMH6732 High Speed Op Amp with Adjustable Bandwidth

Check for Samples: LMH6732

FEATURES

- **Exceptional Performance at Any Supply Current:** **V_S = ±5V, T_A = 25°C, A_V = +2V/V, V_{OUT} = $2V_{PP}$, Typical unless Noted:**

I_{CC} (mA)	-3dB BW (MHz)	DG/DP (%/deg.) PAL	Slew Rate (V/µs)	THD 1MHz (dBc)	Output Current (mA)
1.0	55	0.20 / 0.036	400	-70.0	9
3.4	180	0.022 / 0.017	2100	-78.5	45
9.0	540	0.025 / 0.010	2700	-79.6	115

- **Ultra High Speed (−3dB BW) 1.5GHz (I_{CC} = 10mA, $0.25V_{PP}$)**
- **Single Resistor Adjustability of Supply Current**
- **Fast Enable/ Disable Capability 20ns (I_{CC} = 9mA)**
- **"Popless" Output on "Enable" 15mV (I_{CC} = 1mA)**
- **Ultra Low Disable Current <1µA**
- **Unity Gain Stable**
- **Improved Replacement for CLC505 & CLC449**

APPLICATIONS

- **Battery Powered Systems**
- **Video Switching and Distribution**
- **Remote Site Instrumentation**
- **Mobile Communications Gear**

DESCRIPTION

The LMH6732 is a high speed op amp with a unique combination of high performance, low power consumption, and flexibility of application. The supply current is adjustable, over a continuous range of more than 10 to 1, with a single resistor, R_P. This feature allows the device to be used in a wide variety of high performance applications including device turn on/ turn off (Enable/ Disable) for power saving or multiplexing. Typical performance at any supply current is exceptional. The LMH6732's design has been optimized so that the output is well behaved, eliminating spurious outputs on "Enable".

The LMH6732's combination of high performance, low power consumption, and large signal performance makes it ideal for a wide variety of remote site equipment applications such as battery powered test instrumentation and communications gear. Other applications include video switching matrices, ATE and phased array radar systems.

The LMH6732 is available in the SOIC and SOT-23 packages. To reduce design times and assist in board layout, the LMH6732 is supported by an evaluation board.

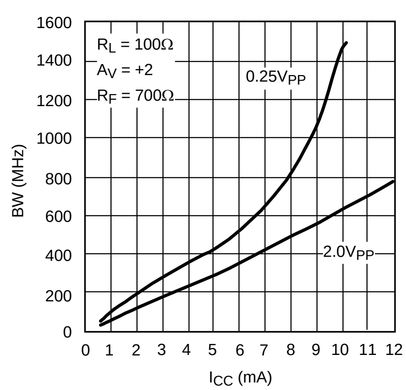

Figure 1. −3dB BW vs. I_{CC}

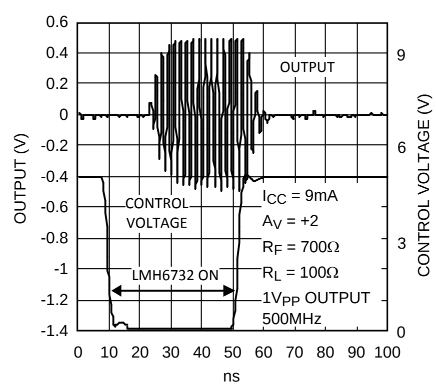

Figure 2. Turn-On/Off Characteristics

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

V_S		±6.75V
I_{OUT}		See (3)
I_{CC}		14mA
Common Mode Input Voltage		V^- to V^+
Maximum Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering (10 sec)	260°C
ESD Tolerance (4)	Human Body Model	2000V
	Machine Model	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications..
(3) The maximum output current (I_O) is determined by device power dissipation limitations.
(4) Human body model: 1.5kΩ in series with 100pF. Machine model: 0Ω in series with 200pF.

Operating Ratings (1)

Thermal Resistance		
Package	θ_{JC} (°C/W)	θ_{JA} (°C/W)
8-Pin SOIC	65°C/W	166°C/W
6-Pin SOT-23	120°C/W	198°C/W
Operating Temperature		−40°C to +85°C
Nominal Supply Voltage		±4.5V to ±6V
Operating Supply Current		0.5mA < I_{CC} < 12mA

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.

Electrical Characteristics I_{CC} = 9mA [1]

A_V = +2, R_F = 700Ω, V_S = ±5V, R_L = 100Ω, R_P = 39kΩ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min [2]	Typ [2]	Max [2]	Units
Frequency Domain Response						
SSBW	-3dB Bandwidth	V_{OUT} = 2V_{PP}		540		MHz
LSBW	-3dB Bandwidth	V_{OUT} = 4.0V_{PP}		315		MHz
$GF_{0.1dB}$	0.1dB Gain Flatness	V_{OUT} = 2V_{PP}		180		MHz
GFP	Frequency Response Peaking	DC to 200MHz, V_{OUT} = 2V_{PP}		0.01		dB
GFR	Frequency Response Rolloff	DC to 200MHz, V_{OUT} = 2V_{PP}		0.15		dB
LPD	Linear Phase Deviation	DC to 200MHz, V_{OUT} = 2V_{PP}		0.6		deg
		DC to 140MHz, V_{OUT} = 2V_{PP}		0.1		
DG	Differential Gain	R_L = 150Ω, 4.43MHz		0.025		%
DP	Differential Phase	R_L = 150Ω, 4.43MHz		0.010		deg
Time Domain Response						
TRS	Rise Time	2V Step		0.8		ns
TRL	Fall Time	2V Step		0.9		
T_S	Settling Time to 0.04%	A_V = −1, 2V Step		18		ns
OS	Overshoot	2V Step		1		%
SR	Slew Rate	5V Step, 40% to 60% [3]		2700		V/µs
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	2V_{PP}, 20MHz		−60		dBc
HD3	3rd Harmonic Distortion	2V_{PP}, 20MHz		−64		dBc
THD	Total Harmonic Distortion	2V_{PP}, 1MHz		−79.6		dBc
V_N	Input Referred Voltage Noise	>1MHz		2.5		nV/√Hz
I_N	Input Referred Inverting Noise Current	>1MHz		9.7		pA/√Hz
I_{NN}	Input Referred Non-Inverting Noise Current	>1MHz		1.8		pA/√Hz
SNF	Noise Floor	>1MHz		−154		dBm_{1Hz}
INV	Total Integrated Input Noise	1MHz to 200MHz		60		µV

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Min/Max ratings are based on production testing unless otherwise specified.
(2) Typical numbers are the most likely parametric norm. Bold numbers refer to over temperature limits.
(3) Slew Rate is the average of the rising and falling edges.

Electrical Characteristics I_{CC} = 9mA(1) (continued)

A_V = +2, R_F = 700Ω, V_S = ±5V, R_L = 100Ω, R_P = 39kΩ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min(2)	Typ(2)	Max(2)	Units
Static, DC Performance						
V_{IO}	Input Offset Voltage			±3.0	±8.0 **9.9**	mV
DV_{IO}	Input Offset Voltage Average Drift	See(4)		16		μV/°C
I_{BN}	Input Bias Current	Non Inverting(5)		−2	±11 **±12**	μA
DI_{BN}	Input Bias Current Average Drift	Non-Inverting(4)		5		nA/°C
I_{BI}	Input Bias Current	Inverting(5)		−9	±20 **± 30**	μA
DI_{BI}	Input Bias Current Average Drift	Inverting(4)		−14		nA/°C
+PSRR	Positive Power Supply Rejection Ratio	DC	52 **50**	62		dB
−PSRR	Negative Power Supply Rejection Ratio	DC	51 **48**	56		dB
CMRR	Common Mode Rejection Ratio	DC	49 **46**	52		dB
I_{CC}	Supply Current	R_L = ∞, R_P = 39kΩ	7.5 **6.6**	9.0	10.5 **11.7**	mA
$I_{CC}I$	Supply Current During Shutdown			<1		μA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting		4.7		MΩ
C_{IN}	Input Capacitance	Non-Inverting		1.8		pF
R_{OUT}	Output Resistance	Closed Loop		32		mΩ
V_O	Output Voltage Range	R_L = ∞	±3.60 **±3.55**	±3.75		V
V_{OL}		R_L = 100Ω	±2.90 **±2.85**	±3.10		V
CMIR	Common Mode Input Range	Common Mode		±2.2		V
I_O	Output Current	Closed Loop −40mV ≤ V_O ≤ 40mV	±75	±115		mA
TON	Turn-on Time	0.5V_{PP} Sine Wave, 90% of Full Value		20		ns
TOFF	Turn-off Time	0.5V_{PP} Sine Wave, <5% of Full Value		9		ns
$V_{O\ glitch}$	Turn-on Glitch			50		mV
FDTH	Feed-Through	f = 10MHz, A_V = +2, Off State		−61		dB

(4) Drift determined by dividing the change in parameter distribution average at temperature extremes by the total temperature change
(5) Negative input current implies current flowing out of the device.

Electrical Characteristics I_{CC} = 3.4mA (1)

A_V = +2, R_F = 1kΩ, V_S = ±5V, R_L = 100Ω, R_P = 137kΩ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (2)	Typ (2)	Max (2)	Units
Frequency Domain Response						
SSBW	-3dB Bandwidth	V_{OUT} = 2V_{PP}		180		MHz
LSBW	-3dB Bandwidth	V_{OUT} = 4.0V_{PP}		100		MHz
$GF_{0.1dB}$	0.1dB Gain Flatness	V_{OUT} = 2V_{PP}		50		MHz
GFP	Frequency Response Peaking	DC to 75MHz, V_{OUT} = 2V_{PP}		0.15		dB
GFR	Frequency Response Rolloff	DC to 75MHz, V_{OUT} = 2V_{PP}		0.05		dB
LPD	Linear Phase Deviation	DC to 55MHz, V_{OUT} = 2V_{PP}		0.5		deg
		DC to 25MHz, V_{OUT} = 2V_{PP}		0.1		
DG	Differential Gain	R_L = 150Ω, 4.43MHz		0.022		%
DP	Differential Phase	R_L = 150Ω, 4.43MHz		0.017		deg
Time Domain Response						
TRS	Rise Time	2V Step		1.7		ns
TRL	Fall Time	2V Step		2.1		
T_S	Settling Time to 0.04%	A_V = −1, 2V Step		18		ns
OS	Overshoot	2V Step		2		%
SR	Slew Rate	5V Step, 40% to 60% (3)		2100		V/µs
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	2V_{PP}, 10MHz		−51		dBc
HD3	3rd Harmonic Distortion	2V_{PP}, 10MHz		−65		dBc
THD	Total Harmonic Distortion	2V_{PP}, 1MHz		−78.5		dBc
V_N	Input Referred Voltage Noise	>1MHz		4.1		$nV/\sqrt{Hz}$
I_N	Input Referred Inverting Noise Current	>1MHz		8.8		$pA/\sqrt{Hz}$
I_{NN}	Input Referred Non-Inverting Noise Current	>1MHz		1.1		$pA/\sqrt{Hz}$
SNF	Noise Floor	>1MHz		−151		dBm_{1Hz}
INV	Total Integrated Input Noise	1MHz to 100MHz		60		µV

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Min/Max ratings are based on production testing unless otherwise specified.
(2) Typical numbers are the most likely parametric norm. Bold numbers refer to over temperature limits.
(3) Slew Rate is the average of the rising and falling edges.

Electrical Characteristics I_{CC} = 3.4mA[1] (continued)

A_V = +2, R_F = 1kΩ, V_S = ±5V, R_L = 100Ω, R_P = 137kΩ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min [2]	Typ [2]	Max [2]	Units
Static, DC Performance						
V_{IO}	Input Offset Voltage			±2.5	±7.0 **±8.5**	mV
DV_{IO}	Input Offset Voltage Average Drift	See[4]		10		μV/°C
I_{BN}	Input Bias Current	Non Inverting[5]		−0.4	±4 **±6**	μA
DI_{BN}	Input Bias Current Average Drift	Non-Inverting[4]		8		nA/°C
I_{BI}	Input Bias Current	Inverting[5]		−1	±12 **±16**	μA
DI_{BI}	Input Bias Current Average Drift	Inverting[4]		−3		nA/°C
+PSRR	Positive Power Supply Rejection Ratio	DC	52 **50**	64		dB
−PSRR	Negative Power Supply Rejection Ratio	DC	51 **50**	57		dB
CMRR	Common Mode Rejection Ratio	DC	49 **48**	55		dB
I_{CC}	Supply Current	R_L = ∞, R_P = 137kΩ	2.8 **2.6**	3.4	3.9 **4.1**	mA
$I_{CC}I$	Supply Current During Shutdown			<1		μA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting		15		MΩ
C_{IN}	Input Capacitance	Non-Inverting		1.7		pF
R_{OUT}	Output Resistance	Closed Loop		50		mΩ
V_O	Output Voltage Range	R_L = ∞	±3.60 **±3.55**	±3.78		V
V_{OL}		R_L = 100Ω	±2.90 **±2.85**	±3.10		
CMIR	Common Mode Input Range	Common Mode		±2.2		V
I_O	Output Current	Closed Loop −20mV ≤ V_O ≤ 20mV	±30	±45		mA
TON	Turn-on Time	0.5V_{PP} Sine Wave, 90% of Full Value		42		ns
TOFF	Turn-off Time	0.5V_{PP} Sine Wave, <5% of Full Value		10		
$V_{O\ glitch}$	Turn-on Glitch			25		mV
FDTH	Feed-Through	f = 10MHz, A_V = +2, Off State		−61		dB

(4) Drift determined by dividing the change in parameter distribution average at temperature extremes by the total temperature change
(5) Negative input current implies current flowing out of the device.

Electrical Characteristics I_{CC} = 1.0mA[(1)]

A_V = +2, R_F = 1kΩ, V_S = ±5V, R_L = 500Ω, R_P = 412kΩ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (2)	Typ (2)	Max (2)	Units
Frequency Domain Response						
SSBW	-3dB Bandwidth	V_{OUT} = $2V_{PP}$		55		MHz
LSBW	-3dB Bandwidth	V_{OUT} = $4.0V_{PP}$		30		MHz
$GF_{0.1dB}$	0.1dB Gain Flatness	V_{OUT} = $2V_{PP}$		20		MHz
GFP	Frequency Response Peaking	DC to 25MHz, V_{OUT} = $2V_{PP}$		0.11		dB
GFR	Frequency Response Rolloff	DC to 25MHz, V_{OUT} = $2V_{PP}$		0.05		dB
LPD	Linear Phase Deviation	DC to 20MHz, V_{OUT} = $2V_{PP}$		1		deg
		DC to 14MHz, V_{OUT} = $2V_{PP}$		0.3		
DG	Differential Gain	R_L = 500Ω, 4.43MHz		0.020		%
DP	Differential Phase	R_L = 500Ω, 4.43MHz		0.036		deg
Time Domain Response						
TRS	Rise Time	2V Step		3.7		ns
TRL	Fall Time	2V Step		5.1		
T_S	Settling Time to 0.04%	A_V = −1, 2V Step		18		ns
OS	Overshoot	2V Step		2		%
SR	Slew Rate	5V Step, 40% to 60%[(3)]		400		V/µs
Distortion And Noise Response						
HD2	2nd Harmonic Distortion	$2V_{PP}$, 5MHz		−43		dBc
HD3	3rd Harmonic Distortion	$2V_{PP}$, 5MHz		−65		dBc
THD	Total Harmonic Distortion	$2V_{PP}$, 1MHz		−70.0		dBc
V_N	Input Referred Voltage Noise	>1MHz		8.4		$nV/\sqrt{Hz}$
I_N	Input Referred Inverting Noise Current	>1MHz		9.0		$pA/\sqrt{Hz}$
I_{NN}	Input Referred Non-Inverting Noise Current	>1MHz		0.8		$pA/\sqrt{Hz}$
SNF	Noise Floor	>1MHz		−147		dBm_{1Hz}
INV	Total Integrated Input Noise	1MHz to 100MHz		29		µV

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Min/Max ratings are based on production testing unless otherwise specified.
(2) Typical numbers are the most likely parametric norm. Bold numbers refer to over temperature limits.
(3) Slew Rate is the average of the rising and falling edges.

Electrical Characteristics I_{CC} = 1.0mA[1] (continued)

A_V = +2, R_F = 1kΩ, V_S = ±5V, R_L = 500Ω, R_P = 412kΩ; Unless otherwise specified.

Symbol	Parameter	Conditions	Min (2)	Typ (2)	Max (2)	Units
Static, DC Performance						
V_{IO}	Input Offset Voltage			±1.6	±6.0 **±7.3**	mV
DV_{IO}	Input Offset Voltage Average Drift	See[4]		4		μV/°C
I_{BN}	Input Bias Current	Non Inverting[5]		0.04	±2.0 **±2.5**	μA
DI_{BN}	Input Bias Current Average Drift	Non-Inverting[4]		−1		nA/°C
I_{BI}	Input Bias Current	Inverting[5]		−0.1	±6 **±8**	μA
DI_{BI}	Input Bias Current Average Drift	Inverting[4]		−3		nA/°C
+PSRR	Positive Power Supply Rejection Ratio	DC	52 **51**	64		dB
−PSRR	Negative Power Supply Rejection Ratio	DC	51 **49**	59		dB
CMRR	Common Mode Rejection Ratio	DC	49 **47**	55		dB
I_{CC}	Supply Current	R_L = ∞, R_P = 412kΩ	0.70 **0.66**	1.0	1.3 **1.4**	mA
$I_{CC}I$	Supply Current During Shutdown			<1		μA
Miscellaneous Performance						
R_{IN}	Input Resistance	Non-Inverting		46		MΩ
C_{IN}	Input Capacitance	Non-Inverting		1.7		pF
R_{OUT}	Output Resistance	Closed Loop		100		m Ω
V_O	Output Voltage Range	R_L = ∞	±3.60 **±3.55**	±3.78		V
V_{OL}		R_L = 500Ω	±2.90 **±2.85**	±3.10		
CMIR	Common Mode Input Range	Common Mode		±2.2		V
I_O	Output Current	Closed Loop −15mV ≤ V_O ≤ 15mV	±6	±9		mA
TON	Turn-on Time	0.5V_{PP} Sine Wave, 90% of Full Value		95		ns
TOFF	Turn-off Time	0.5V_{PP} Sine Wave, <5% of Full Value		40		
$V_{O\ glitch}$	Turn-on Glitch			15		mV
FDTH	Feed-Through	f = 10MHz, A_V = +2, Off State		−61		dB

(4) Drift determined by dividing the change in parameter distribution average at temperature extremes by the total temperature change
(5) Negative input current implies current flowing out of the device.

CONNECTION DIAGRAMS

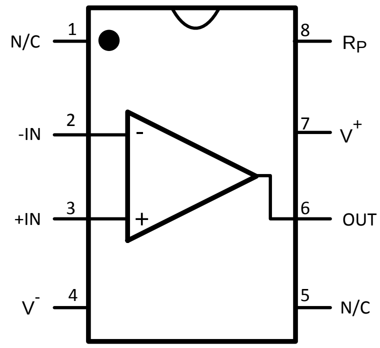

Figure 3. 8-Pin SOIC (Top View)
See Package Number D (R-PDSO-G8)

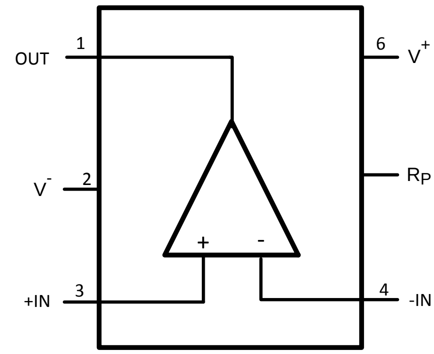

Figure 4. 6-Pin SOT-23 (Top View)
See Package Number DBV (R-PDSO-G6)

TYPICAL PERFORMANCE CHARACTERISTICS

Frequency Response I_{CC} = 9mA

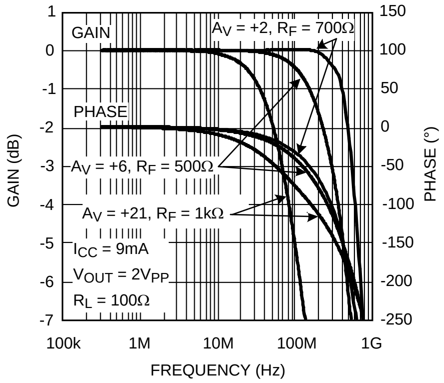

Figure 5.

Frequency Response I_{CC} = 3.4mA

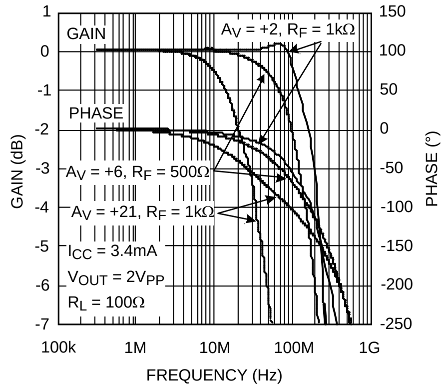

Figure 6.

Frequency Response I_{CC} = 1mA

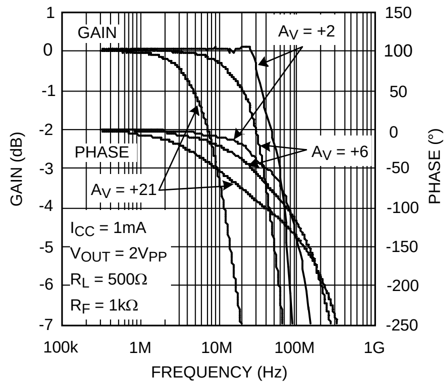

Figure 7.

Frequency Response I_{CC} = 9mA

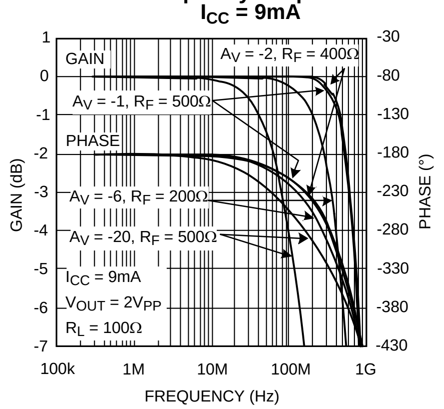

Figure 8.

Frequency Response I_{CC} = 3.4mA

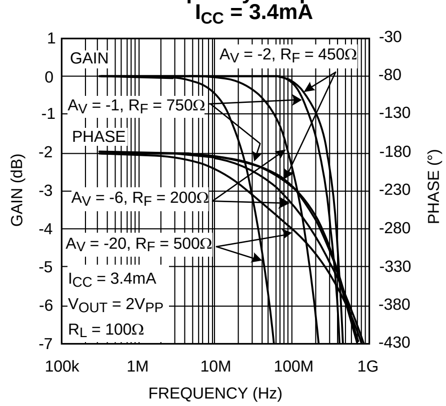

Figure 9.

Frequency Response I_{CC} = 1mA

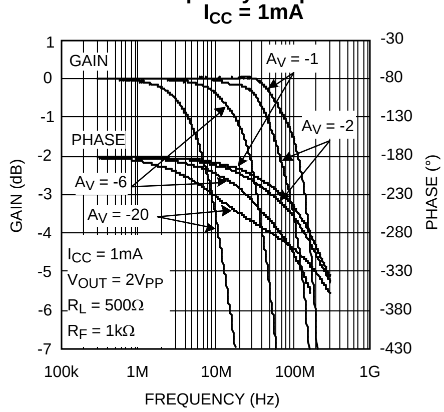

Figure 10.

Frequency Response I_{CC} = 9mA

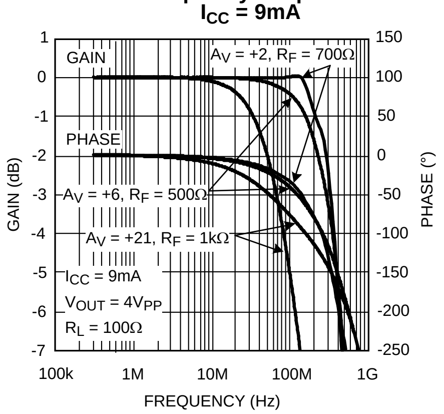

Figure 11.

Frequency Response I_{CC} = 3.4mA

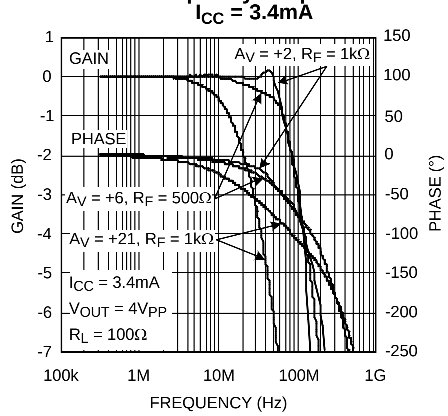

Figure 12.

Frequency Response I_{CC} = 1mA

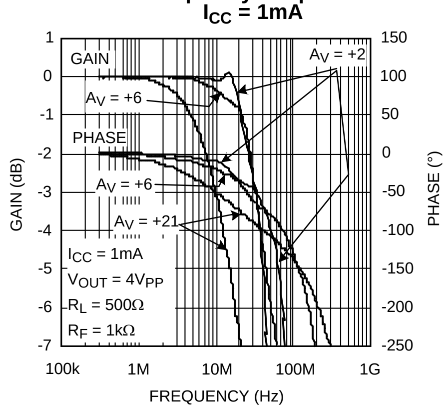

Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Frequency Response
I_{CC} = 9mA

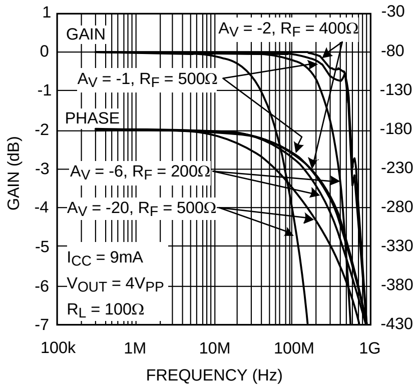

Figure 14.

Frequency Response
I_{CC} = 3.4mA

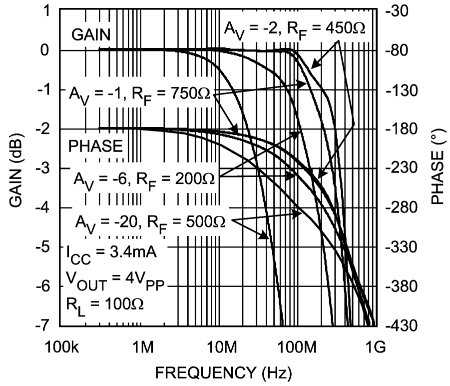

Figure 15.

Frequency Response
I_{CC} = 1mA

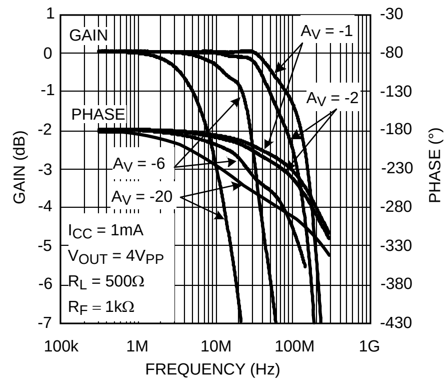

Figure 16.

Noise
I_{CC} = 9mA

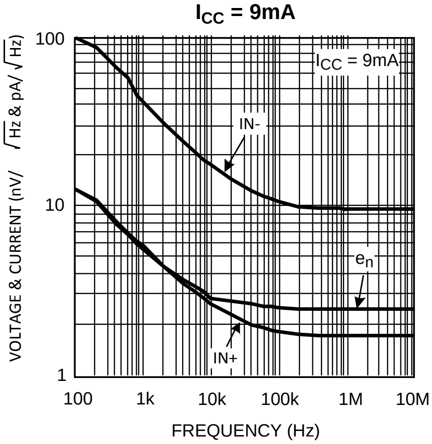

Figure 17.

Noise
I_{CC} = 3.4mA

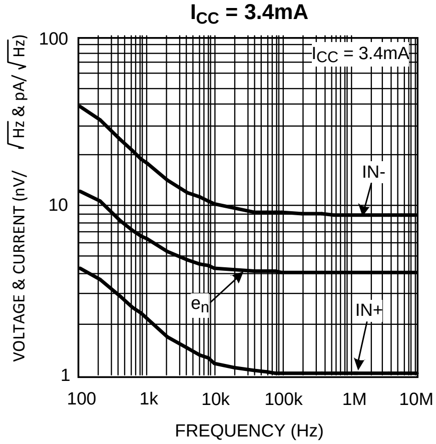

Figure 18.

Noise
I_{CC} = 1mA

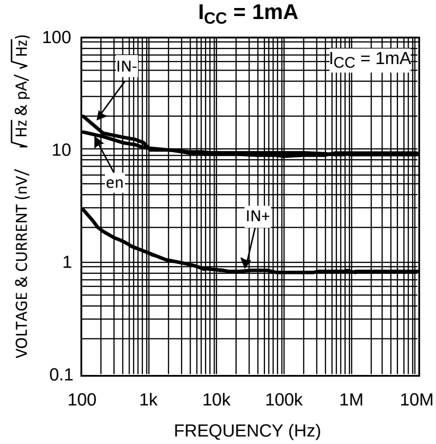

Figure 19.

CMRR and PSRR
I_{CC} = 9mA

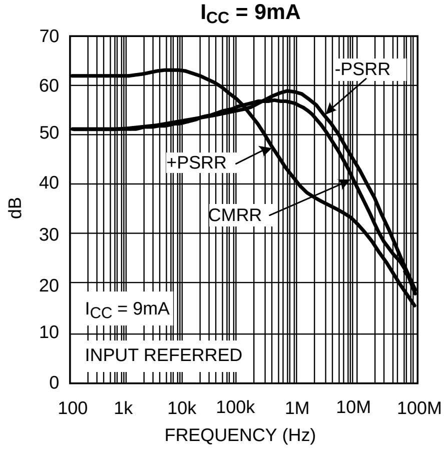

Figure 20.

CMRR and PSRR
I_{CC} = 3.4mA

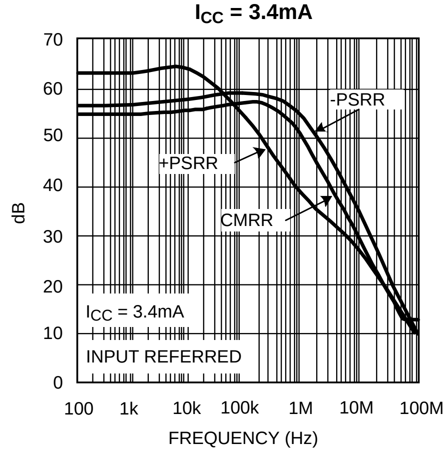

Figure 21.

CMRR and PSRR
I_{CC} = 1mA

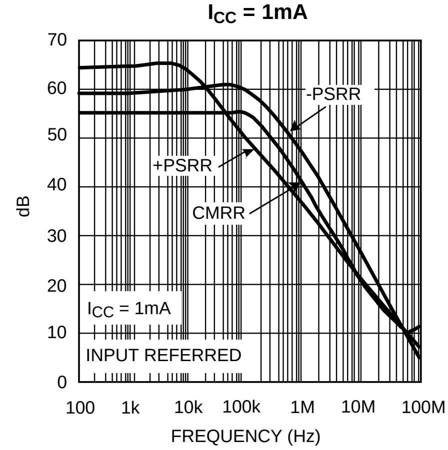

Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

2nd Distortion vs. Output Amplitude
I_{CC} = 9mA

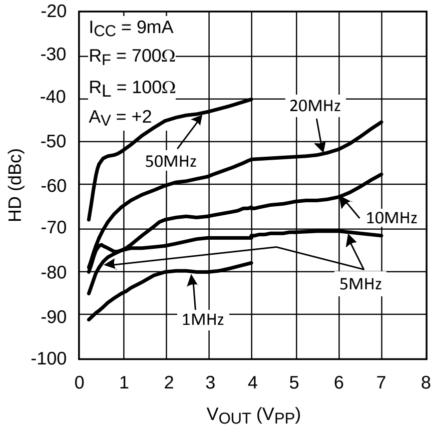

Figure 23.

2nd Distortion vs. Output Amplitude
I_{CC} = 3.4mA

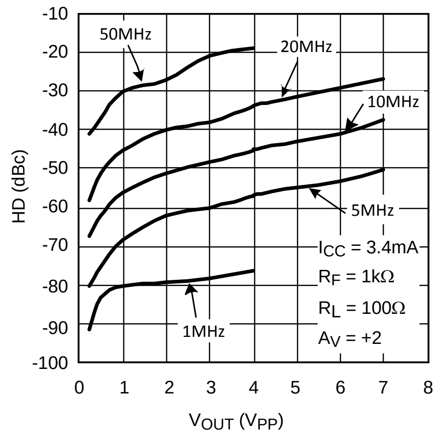

Figure 24.

2nd Distortion vs. Output Amplitude
I_{CC} = 1mA

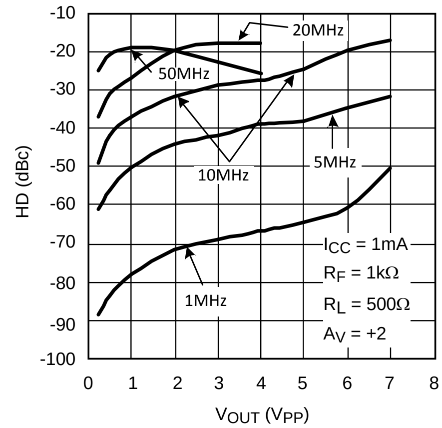

Figure 25.

3rd Distortion vs. Output Amplitude
I_{CC} = 9mA

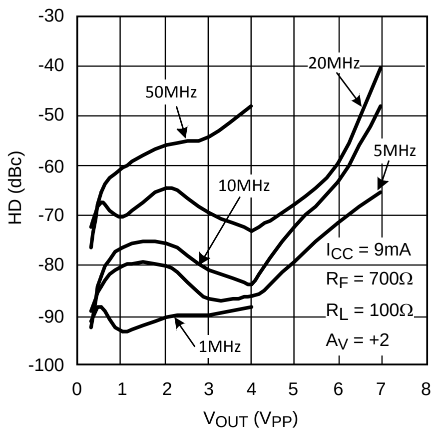

Figure 26.

3rd Distortion vs. Output Amplitude
I_{CC} = 3.4mA

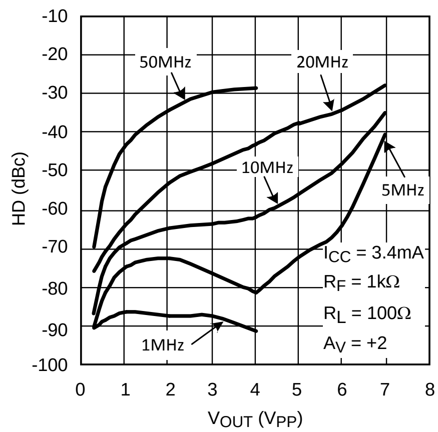

Figure 27.

3rd Distortion vs. Output Amplitude
I_{CC} = 1mA

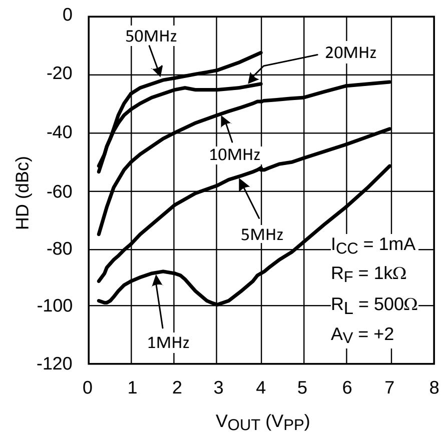

Figure 28.

Frequency Response for Various C_L
I_{CC} = 9mA

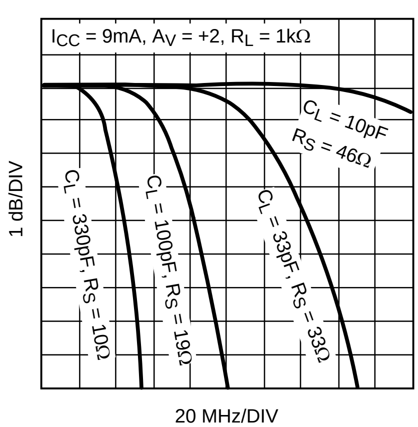

Figure 29.

Frequency Response for Various C_L
I_{CC} = 3.4mA

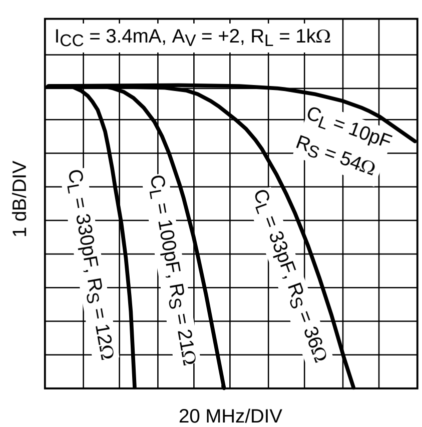

Figure 30.

Frequency Response for Various C_L
I_{CC} = 1mA

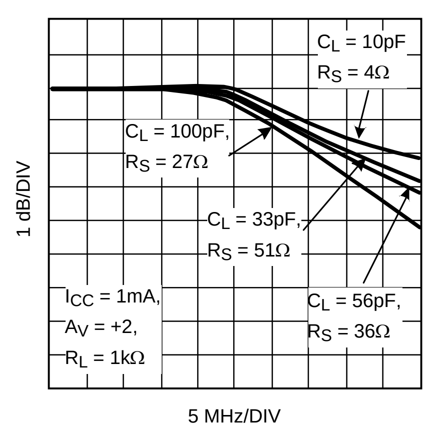

Figure 31.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Small Signal Step Response
I_{CC} = 9mA

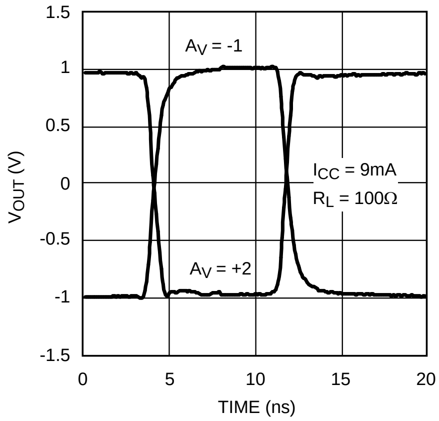

Figure 32.

Small Signal Step Response
I_{CC} = 3.4mA

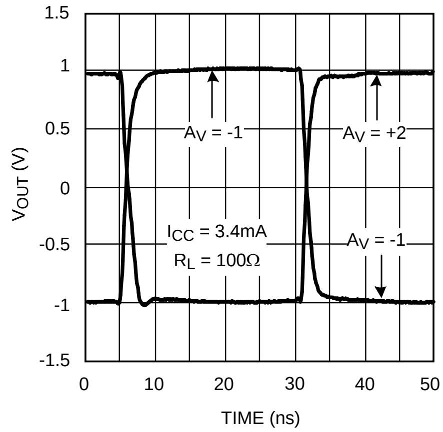

Figure 33.

Small Signal Step Response
I_{CC} = 1mA

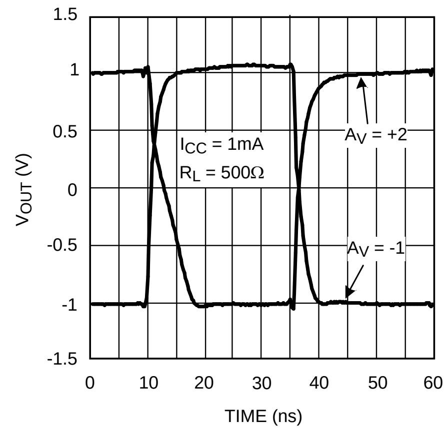

Figure 34.

Large Signal Step Response
I_{CC} = 9mA

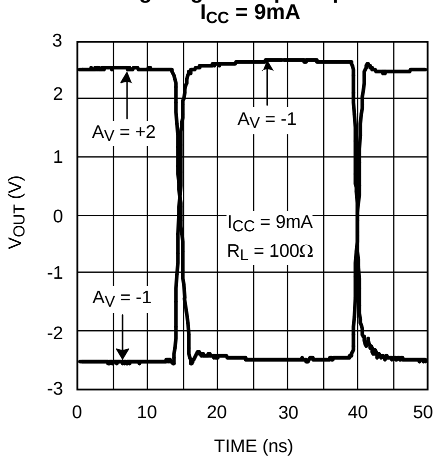

Figure 35.

Large Signal Step Response
I_{CC} = 3.4mA

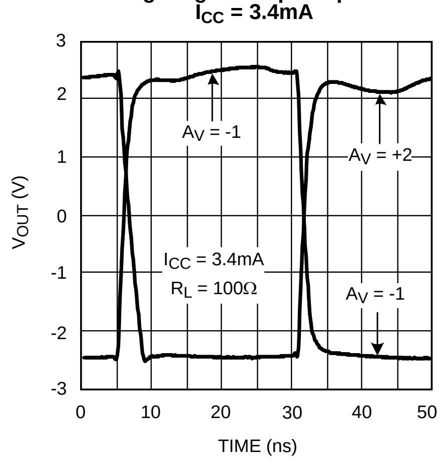

Figure 36.

Large Signal Step Response
I_{CC} = 1mA

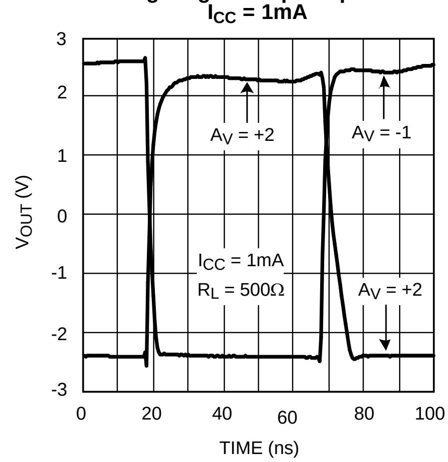

Figure 37.

Output Glitch
I_{CC} = 9mA

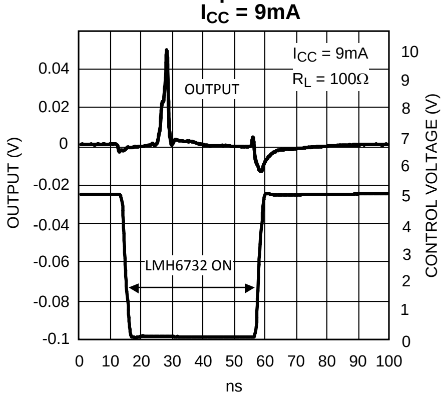

Figure 38.

Output Glitch
I_{CC} = 3.4mA

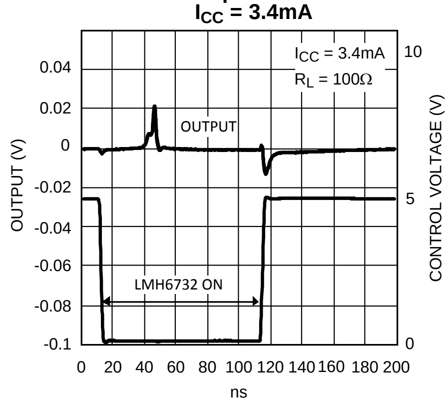

Figure 39.

Output Glitch
I_{CC} = 1mA

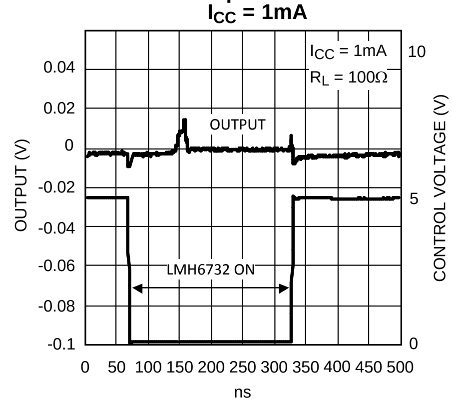

Figure 40.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Turn-On/Off Characteristics I_{CC} = 9mA

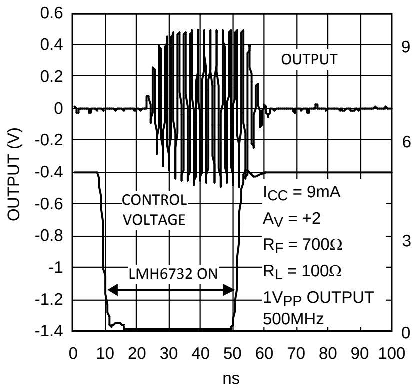

Figure 41.

Turn-On/Off Characteristics I_{CC} = 3.4mA

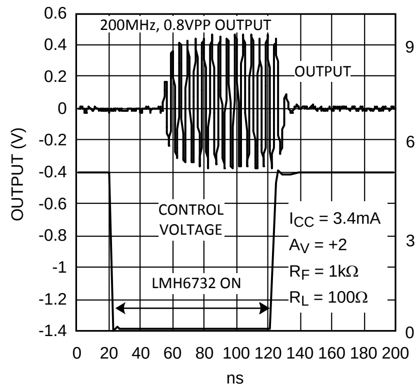

Figure 42.

Turn-On/Off Characteristics I_{CC} = 1mA

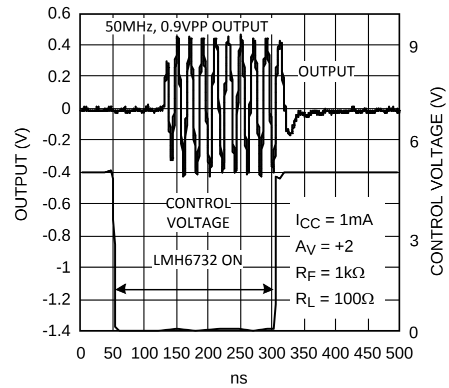

Figure 43.

I_{CC} vs. R_P

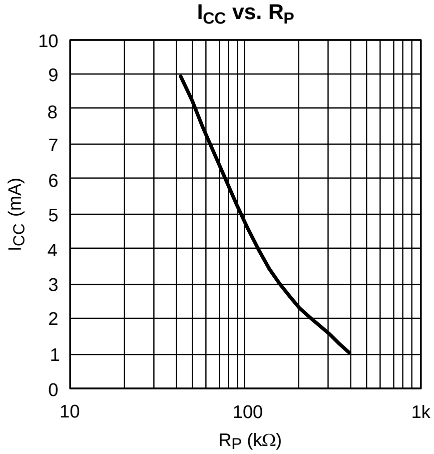

Figure 44.

I_P vs. I_{CC}

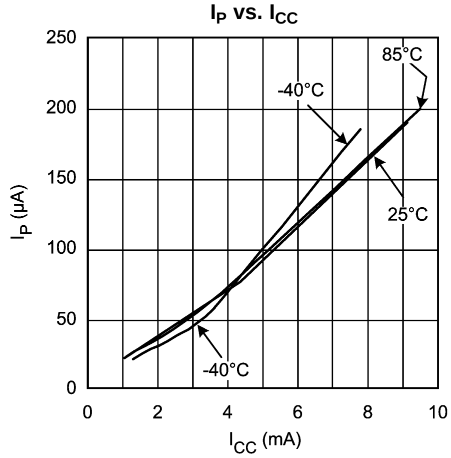

Figure 45.

Max Output Current vs. I_{CC}

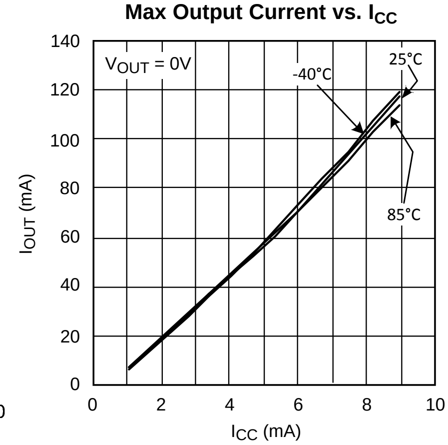

Figure 46.

Slew Rate vs. I_{CC}

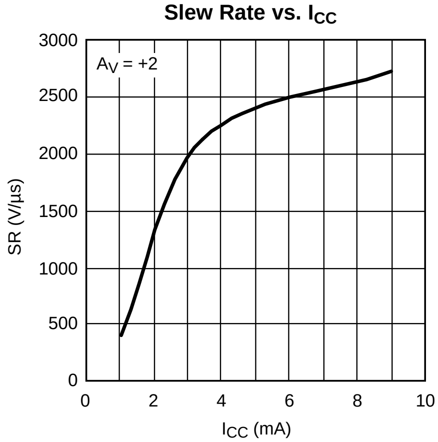

Figure 47.

BW vs. I_{CC}

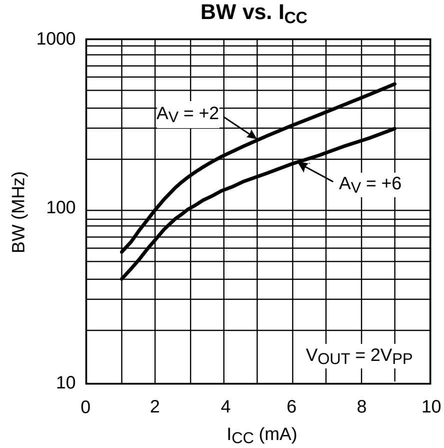

Figure 48.

BW vs. I_{CC} for Various Temperature

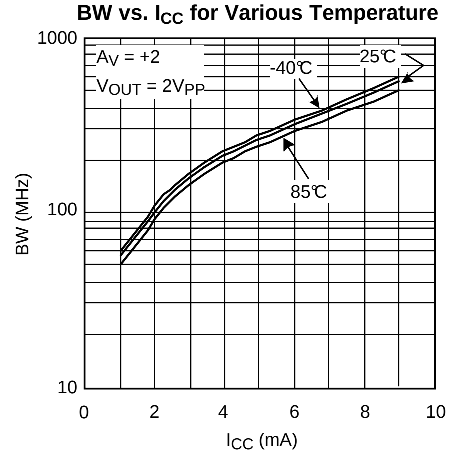

Figure 49.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

−3dB BW vs. I_{CC}

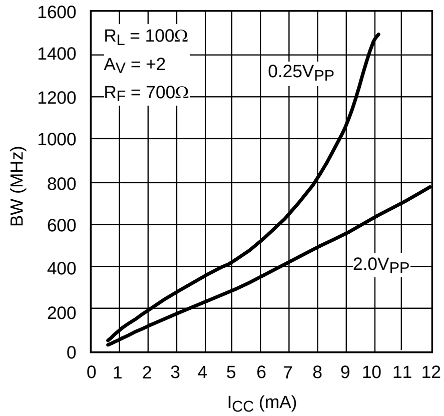

Figure 50.

V_{OS}, I_{BI} & I_{BN} VS. I_{CC}

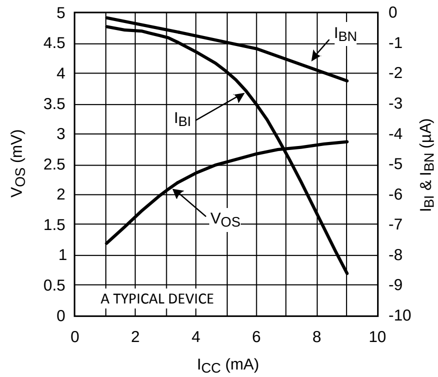

Figure 51.

Output Impedance vs. Frequency

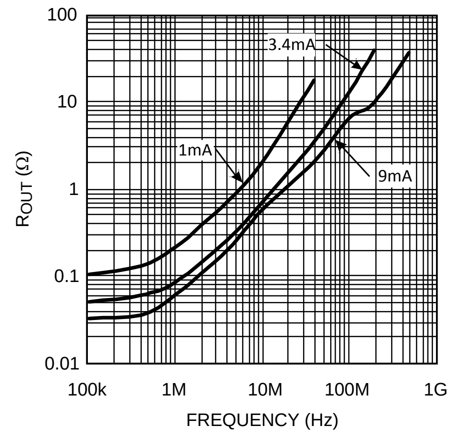

Figure 52.

Transimpedance

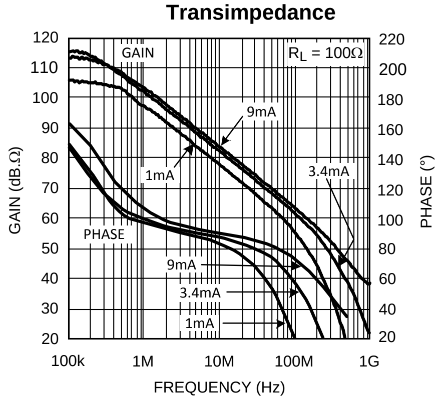

Figure 53.

Recommended R_S vs. C_L

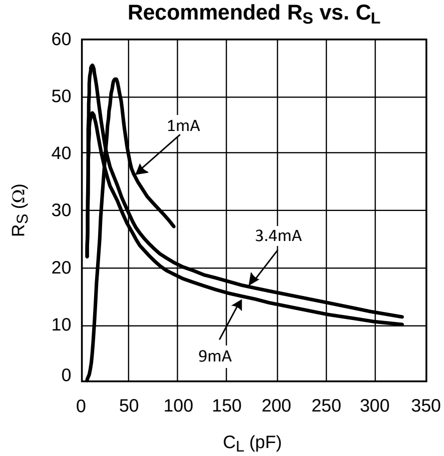

Figure 54.

Settling Time

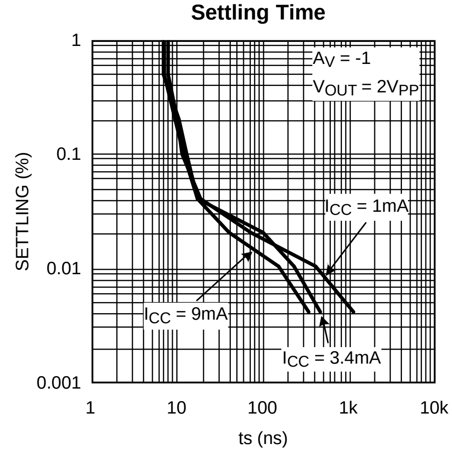

Figure 55.

DG/DP
I_{CC} = 9mA

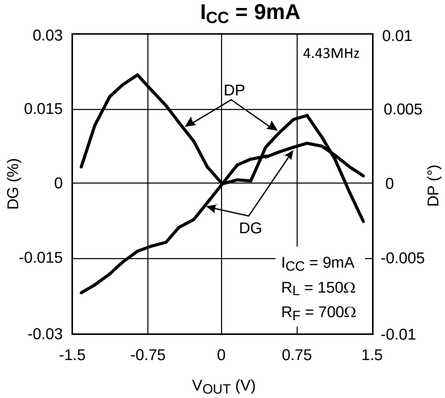

Figure 56.

DG/DP for Various R_L
I_{CC} = 9mA

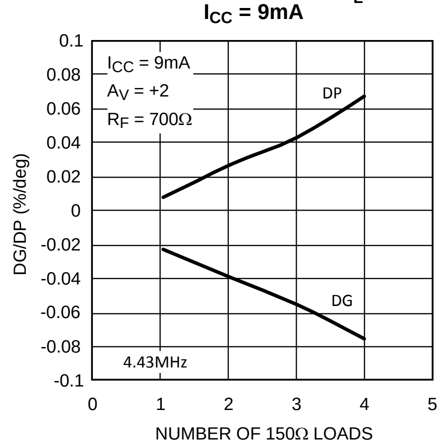

Figure 57.

DG/DP for Various R_L
I_{CC} = 3.4mA

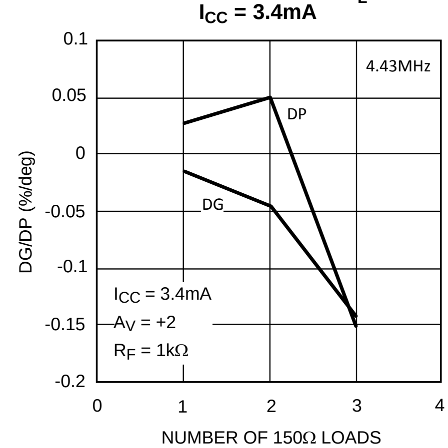

Figure 58.

APPLICATION INFORMATION

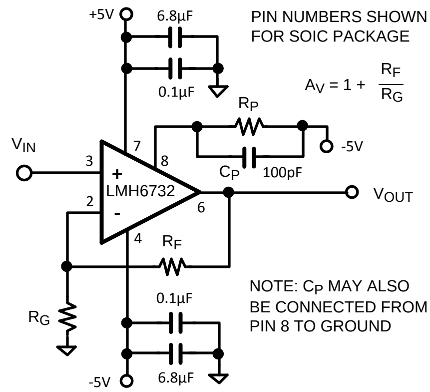

Figure 59. Recommended Non-Inverting Gain Circuit

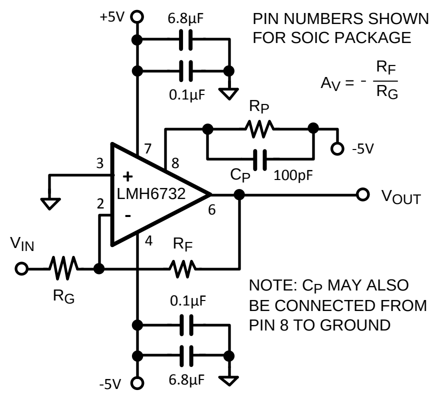

Figure 60. Recommended Inverting Gain Circuit

DESCRIPTION

The LMH6732 is an adjustable supply current, current-feedback operational amplifier. Supply current and consequently dynamic performance can be easily adjusted by selecting the value of a single external resistor (R_P).

NOTE

The following discussion uses the SOIC package pin numbers. For the corresponding SOT-23 package pin numbers, please refer to the Connection Diagrams section.

SELECTING AN OPERATING POINT

The operating point is determined by the supply current which in turn is determined by current (I_P) flowing out of pin 8. As the supply current is increased, the following effects will be observed:

Table 1. Device Parameters Related to Supply Current

Specification	Effect as I_{CC} Increases
Bandwidth	Increases
Rise Time	Decreases
Enable/ Disable Speed	Increases
Output Drive	Increases
Input Bias Current	Increases
Input Impedance	Decreases (see Source impedance Discussion)

Both the Electrical Characteristics pages and the TYPICAL PERFORMANCE CHARACTERISTICS section illustrate these effects to help make the supply current vs. performance trade-off. The supply current is adjustable over a continuous range of more than 10 to 1 with a single resistor, R_P, allowing for easy trade-off between power consumption and speed. Performance is specified and tested at I_{CC} = 1mA, 3.4mA, and 9mA. (Note: Some test conditions and especially the load resistances are different for the three supply current settlings.) The performance plots show typical performance for all three supply currents levels.

When making the supply current vs. performance trade-off, it is first a good idea to see if one of the standard operating points (I_{CC} = 1mA, 3.4mA, or 9mA) fits the application. If it does, performance ensured on the specification pages will apply directly to your application. In addition, the value of R_P may be obtained directly from the Electrical Characteristics pages.

BEYOND 1GHz BANDWIDTH

As stated above, the LMH6732 speed can be increased by increasing the supply current. The −3dB Bandwidth can even reach the unprecedented value of 1.5GHz (A_V = +2, V_{OUT} = 0.25V_{PP}). Of course, this comes at the expense of power consumption (i.e. supply current). The relationship between −3dB BW and supply current is shown in Figure 48 to Figure 50. The supply current would nominally have to be set to around 10mA to achieve this speed. The absolute maximum supply current setting for the LMH6732 is 14mA. Beyond this value, the operation may become unpredictable.

The following discussion will assist in selecting I_{CC} for applications that cannot operate at one of the specified supply current settlings.

Use the typical performance plots for critical specifications to select the best I_{CC}. For parameters containing Min/Max ratings in the data sheet tables, interpolate between the values of I_{CC} in the plots & specification tables to estimate the max/min values in the application.

The simplified schematic for the supply current setting path (I_P) is shown below in Figure 61.

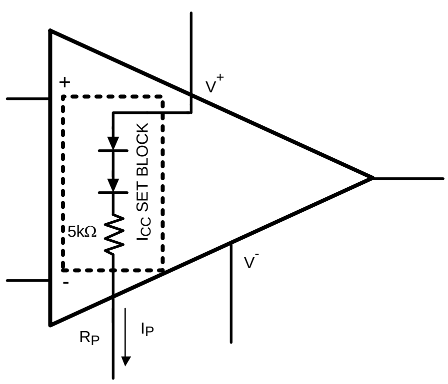

Figure 61. Supply Current Control's Simplified Schematic

The terminal marked "R_P" is tied to a potential through a resistor R_P. The current flowing through R_P (I_P) sets the LMH6732's supply current. Throughout the data sheet, the voltages applied to R_P and V^- are both considered to be −5V. However, the two potentials do not necessarily have to be the same. This is beneficial in applications where non-standard supply voltages are used or when there is a need to power down the op amp via digital logic control.

The relationship between I_{CC} and I_P is given by:

$I_P = I_{CC}/57$ (approximate ratio at I_{CC} = 3.4mA; consult Figure 45 for relationship at any I_{CC}).

Knowing I_P leads to a direct calculation of R_P.

$R_P + 5k\Omega = [(V^+ -1.6)-V^-]/ I_P$

$R_P + 5k\Omega = 8.4 / I_P$ (for V^+ = 5V and V^- = −5V).

First, an operating point needs to be determined from the plots & specifications as discussed above. From this, I_P is obtained. Knowing I_P and the potential R_P is tied to, R_P can be calculated.

EXAMPLE

An application requires that V_S = ±3V and performance in the 1mA operating point range. The required I_P can therefore be determined as follows:

I_P=21µA

R_P is connected from pin 8 to V^-. Calculate R_P under these conditions:

$R_P + 5k\Omega = [(V^+ -1.6)-V^-] / I_P$

$R_P + 5k\Omega = [(3V-1.6V) - (-3V)] / 21\mu A$

$R_P = 205k\Omega$

The LMH6732 will have performance similar to R_P = 412kΩ shown on the datasheet, but with 40% less power dissipation due to the reduced supply voltages. The op amp will also have a more restricted common-mode range and output swing.

DYNAMIC SHUTDOWN CAPABILITY

The LMH6732 may be powered on and off very quickly by controlling the voltage applied to R_P. If R_P is connected between pin 8 and the output of a CMOS gate powered from ±5V supplies, the gate can be used to turn the amplifier on and off. This is shown in Figure 62 below:

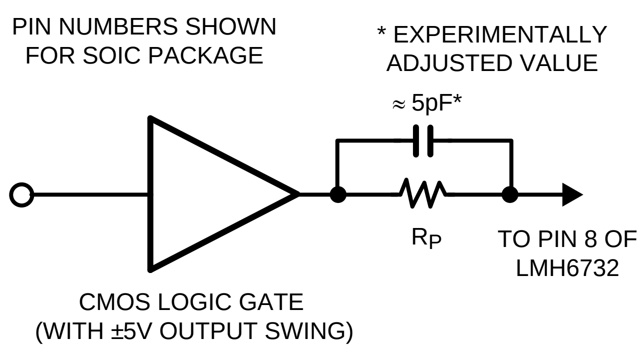

Figure 62. Dynamic Control of Power Consumption Using CMOS Logic

When the gate output is switched from high to low, the LMH6732 will turn on. In the off state, the supply current typically reduces to 1µA or less. The LMH6732's "off state" supply current is reduced significantly compared to the CLC505. This extremely low supply current in the "off state" is quite advantageous since it allows for significant power saving and minimizes feed-through. To improve switching time, a speed up capacitor from the gate output to pin 8 is recommended. The value of this capacitor will depend on the R_P value used and is best established experimentally. Turn-on and turn-off times of <20ns (I_{CC} = 9mA) are achievable with ordinary CMOS gates.

EXAMPLE

An open collector logic device is used to dynamically control the power dissipation of the circuit. Here, the desired connection for R_P is from pin 8 to the open collector logic device.

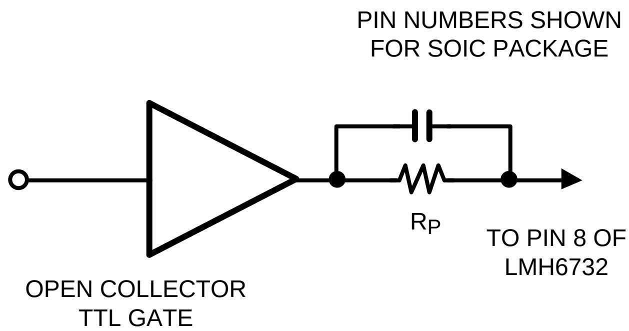

Figure 63. Controlling Power On State with TTL Logic (Open Collector Output)

When the logic gate goes low, the LMH6732 is turned on. The LMH6732 V^+ connection would be to +5V supply.

Performance desired is that given for I_{CC} = 3.4mA under standard conditions. From the I_{CC} vs. I_P plot, I_P = 61μA. Then calculating R_P:

R_P + 5kΩ = [(5V-1.6V)- 0] / 61μA

R_P = 51kΩ

"POPLESS OUTPUT" & OFF CONDITION OUTPUT STATE

The LMH6732 has been especially designed to have minimum glitches during turn-on and turn-off. This is advantageous in situations where the LMH6732 output is fed to another stage which could experience false auto-ranging, or even worse reset operation, due to these transient glitches. Example of this application would be an AGC circuit or an ADC with multiple ranges set to accommodate the largest input amplitude. For the LMH6732, these sorts of transients are typically less than 50mV in amplitude (see Electrical Characteristics Tables for Typical values). Applications designed to utilize the CLC505's low output glitch would benefit from using the LMH6732 instead since the LMH6732's output glitch is improved to be even lower than the CLC505's. In the "Off State", the output stage is turned off and is in effect put into a high-Z state. In this sate, output can be forced by other active devices. No significant current will flow through the device output pin in this mode of operation.

MUX APPLICATION

Since The LMH6732's output is essentially open in the “off” state, it is a good candidate for a fast 2:1 MUX. Figure 64 shows one such application along with the output waveform in Figure 65 displaying the switching between a continuous triangle wave and a single cycle sine wave (signals trigger locked to each other for stable scope photo). Switching speed of the MUX will be less than 50 ns and is governed by the “Ton" and “Toff” times for U1 and U2 at the supply current set by R_{P1} and R_{P2}. Note that the “Control” input is a 5V CMOS logic level.

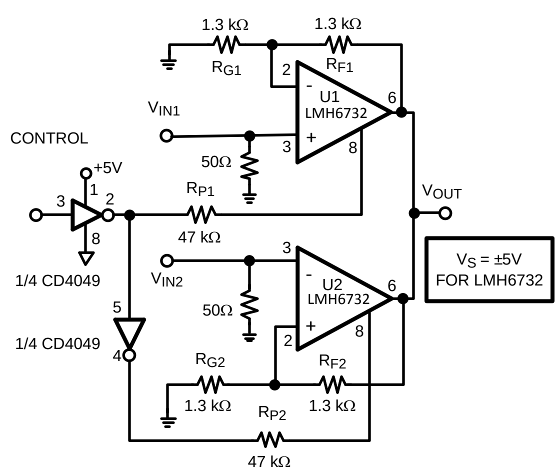

Figure 64. 50 ns 2:1 MUX Schematic

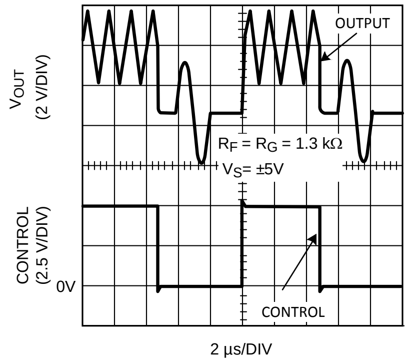

Figure 65. MUX "V_{OUT}" and "Control" Waveform

DIFFERENTIAL GAIN AND PHASE

Differential gain and phase are measurements useful primarily in composite video channels. They are measured by monitoring the gain and phase changes of a high frequency carrier (3.58MHz for NTSC and 4.43MHz for PAL systems) as the output of the amplifier is swept over a range of DC voltages. Specifications for the LMH6732 include differential gain and phase. Test signals used are based on a $1V_{PP}$ video level. Test conditions used are the following:

DC sweep range: 0 to 100 IRE units (black to white)

Carrier: 4.43MHz at 40 IRE units peak to peak

$A_V = +2$, $R_L = 75\Omega + 75\Omega$

SOURCE IMPEDANCE

For best results, source impedance in the non-inverting circuit configuration (see Figure 59) should be kept below 5kΩ.

Above 5kΩ it is possible for oscillation to occur, depending on other circuit board parasitics. For high signal source impedances, a resistor with a value of less than 5kΩ may be used to terminate the non-inverting input to ground.

FEEDBACK RESISTOR

In current-feedback op amps, the value of the feedback resistor plays a major role in determining amplifier dynamics. It is important to select the correct value. The LMH6732 provides optimum performance with feedback resistors as shown in Table 2 below. Selection of an incorrect value can lead to severe roll-off in frequency response, (if the resistor value is too large) or , peaking or oscillation (if the value is too low).

Table 2. Feedback Resistor Selection for Various Gain Settings and I_{CC}'s

Gain (V/V)	I_{CC} (mA)			Unit
	9	3.4	1	
$A_V = +1$	700	1k	1k	Ω
$A_V = +2$	700	1k	1k	Ω
$A_V = -1$	500	750	1k	Ω
$A_V = -2$	400	450	1k	Ω
$A_V = +6$	500	500	1k	Ω
$A_V = -6$	200	200	1k	Ω
$A_V = +21$	1k	1k	1k	Ω
$A_V = -20$	500	500	1k	Ω

For I_{CC} > 9mA at any closed loop gain setting, a good starting point for R_F would be the 9mA value stated in Table 2 above. This value could then be readjusted, if necessary, to achieve the desired response.

PRINTED CIRCUIT LAYOUT & EVALUATION BOARDS

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 (SNOA367) for more information).

Use the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board Part Number
LMH6732MF	SOT-23	LMH730216
LMH6732MA	SOIC	LMH730227

The supply current adjustment resistor, R_P, in both evaluation boards should be tied to the appropriate potential to get the desired supply current. To do so, leave R2 (LMH730216) [R5 (LMH730227)] uninstalled. Jumper "Dis" connector to V−. Install R1 (LMH730216) [R4 (LMH730227)] to set the supply current.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6732MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMH67 32MA	Samples
LMH6732MF/NOPB	ACTIVE	SOT-23	DBV	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A97A	Samples
LMH6732MFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A97A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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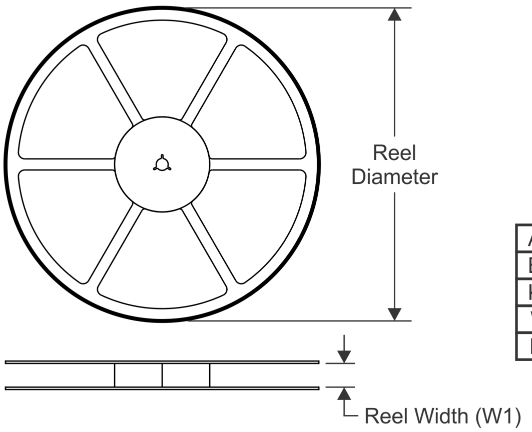
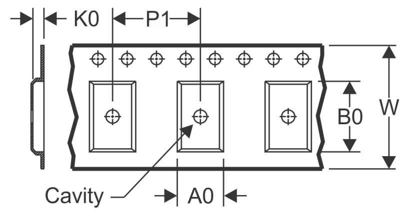
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

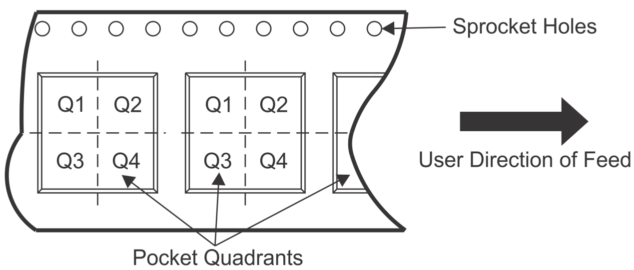
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

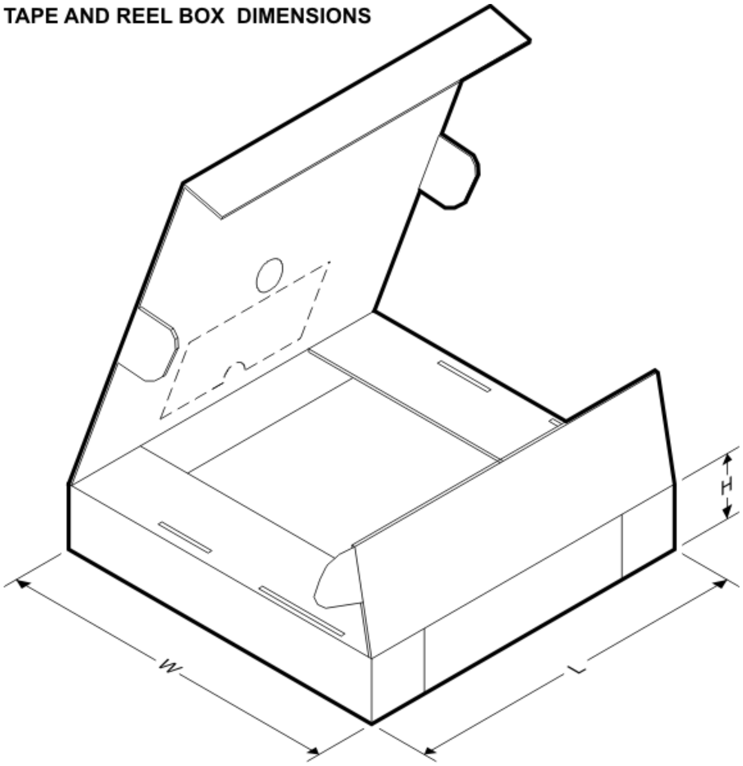
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6732MF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6732MFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

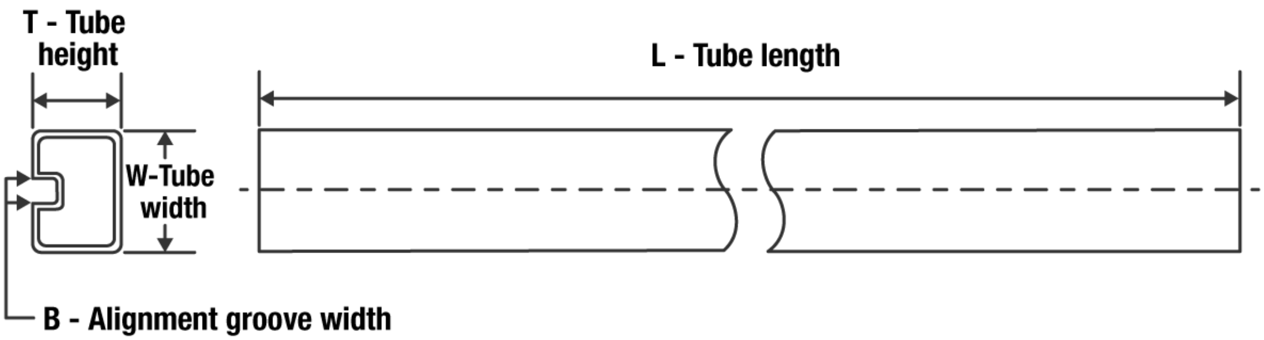
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

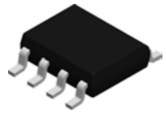
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6732MF/NOPB	SOT-23	DBV	6	1000	208.0	191.0	35.0
LMH6732MFX/NOPB	SOT-23	DBV	6	3000	208.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMH6732MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

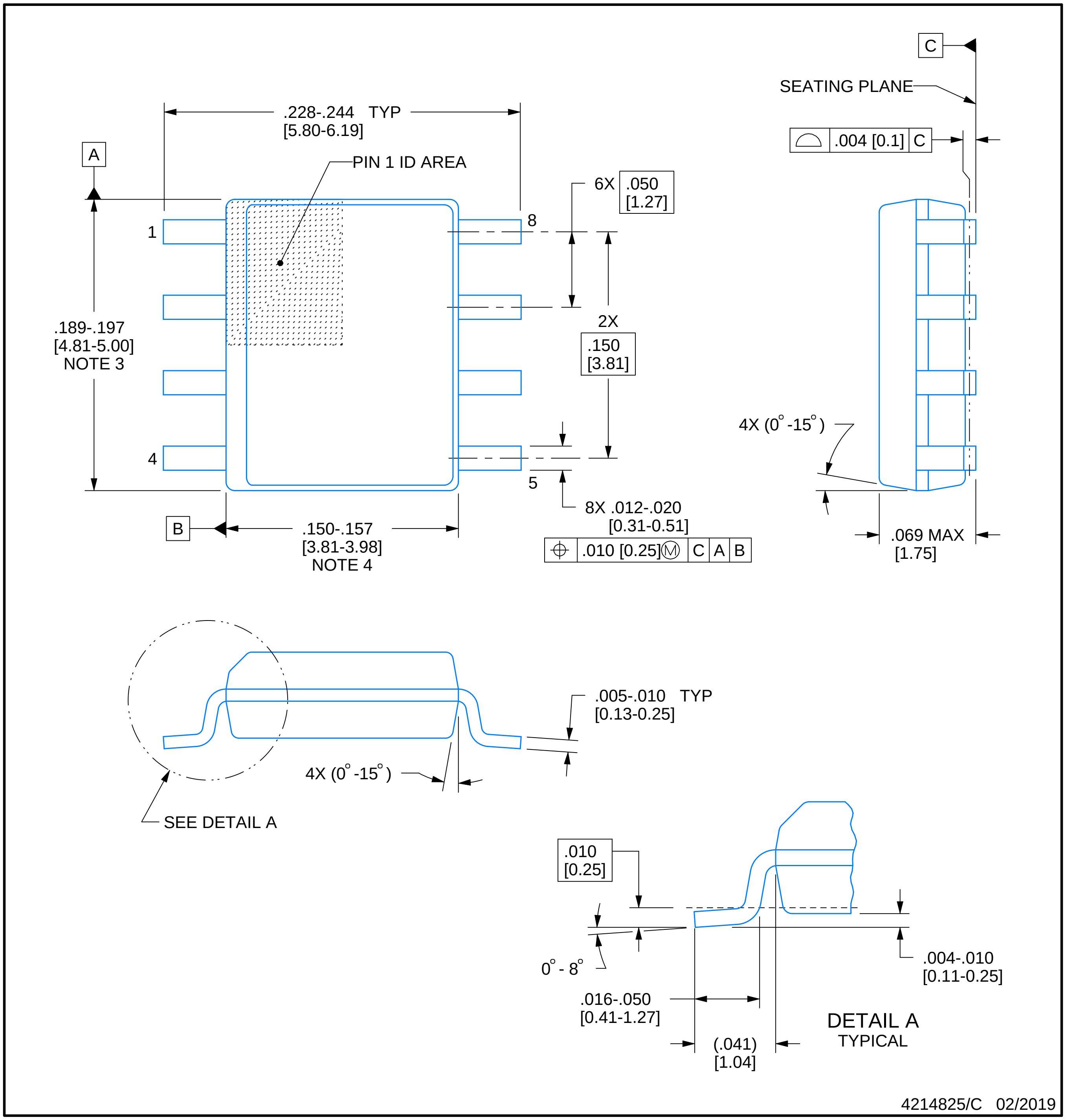


PACKAGE OUTLINE

D0008A

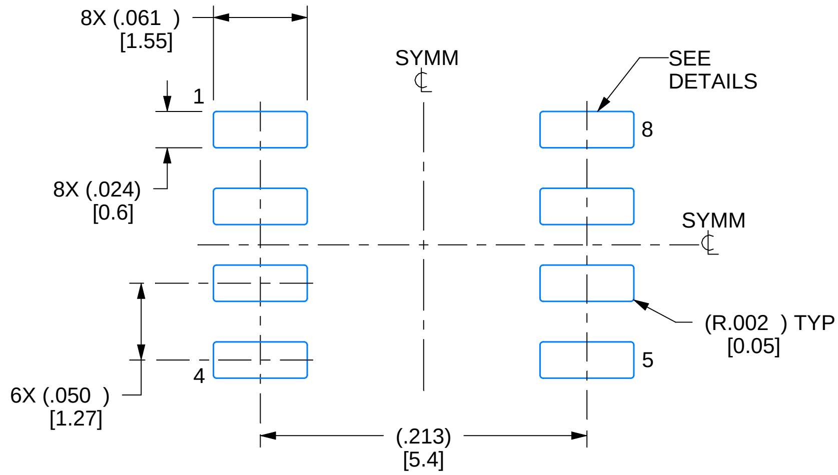
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

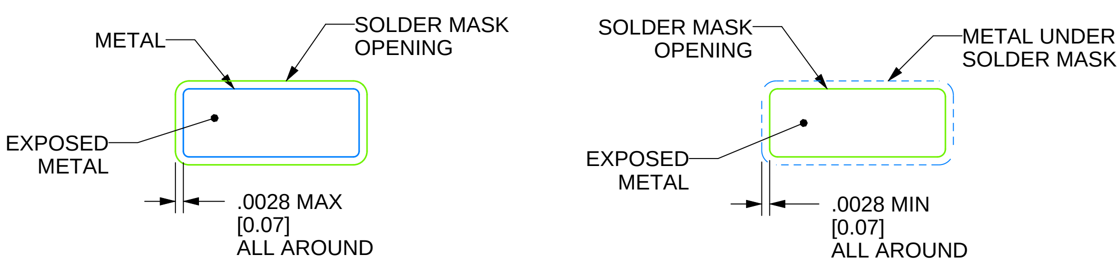


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

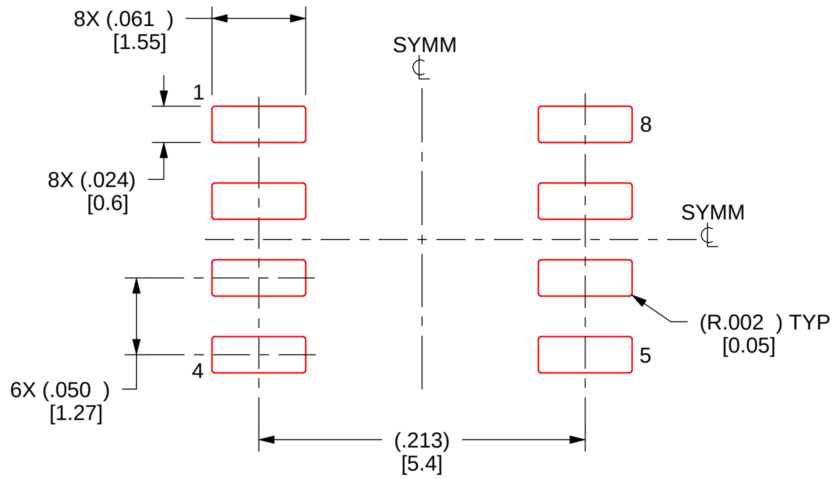
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

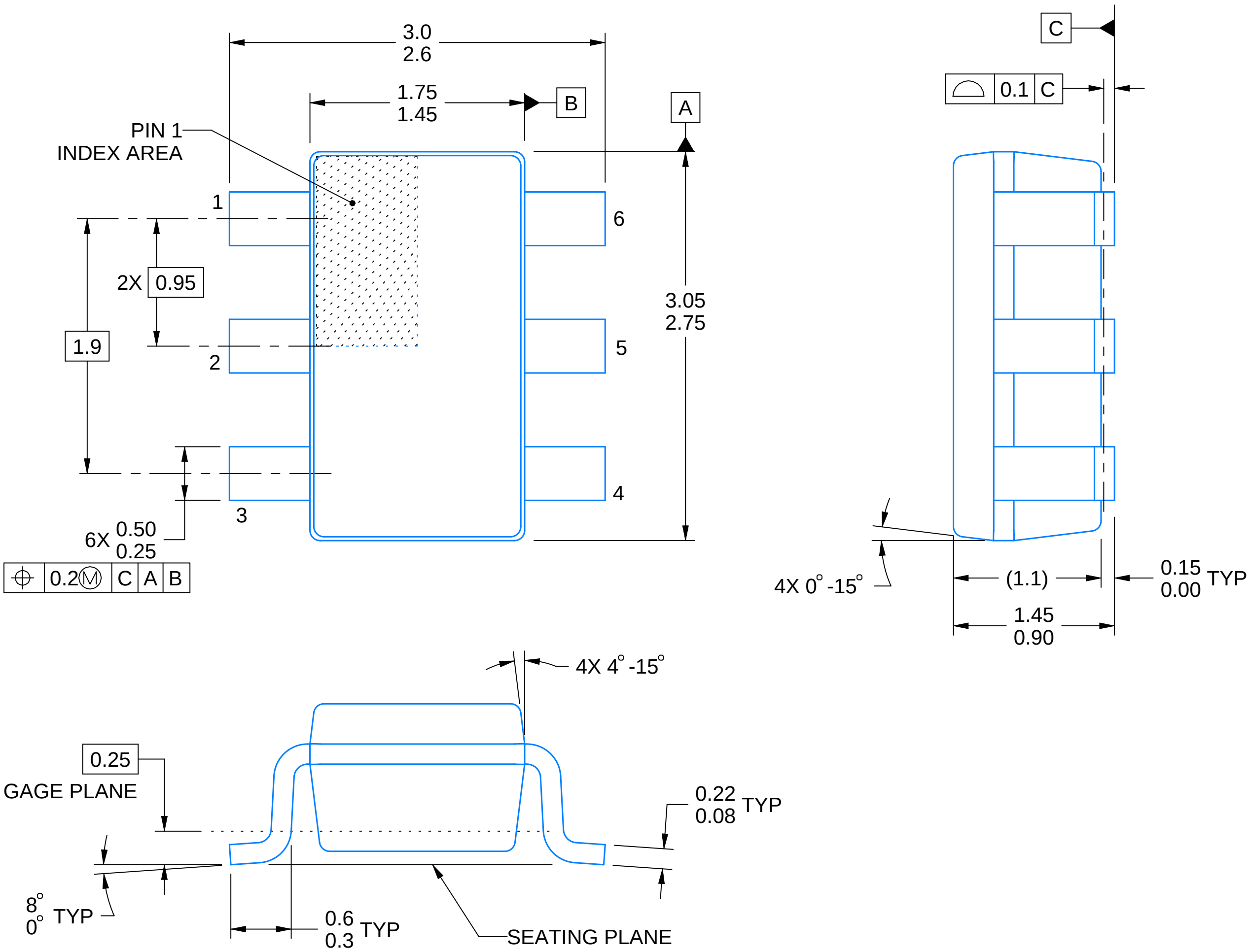


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

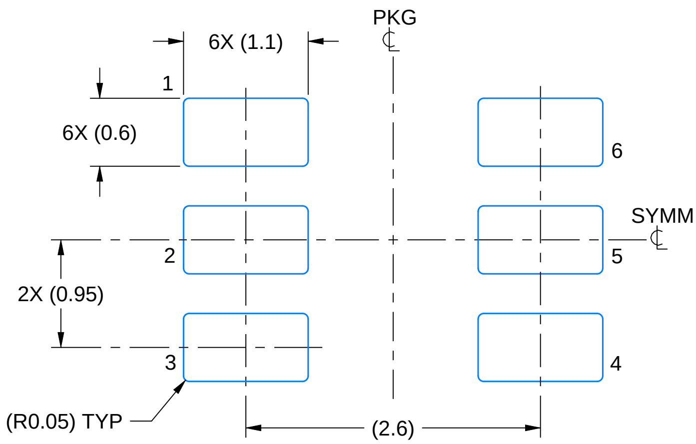
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



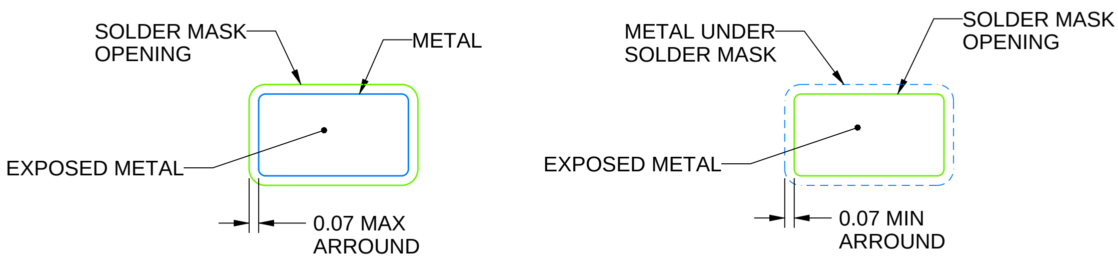
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

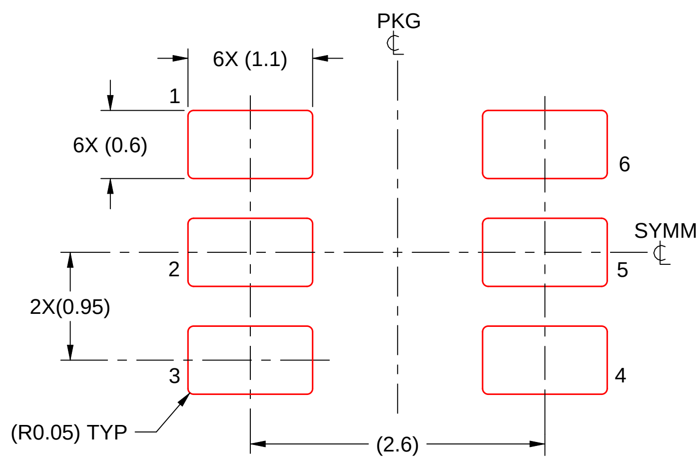
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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