LMK01801 Dual Clock Divider Buffer

1 Features

- Pin control mode or MICROWIRE (SPI)
- Input and output frequency range: 1 kHz to 3.1 GHz
- Separate input for clock output banks A and B
- 14 differential clock outputs in two banks (A and B)
  - Output Bank A
    - 8 differential, programmable outputs (up to 8 as LVCMOS)
    - Divider values of 1 to 8, even and odd.
  - Output Bank B
    - 6 differential outputs (or up to 12 as LVCMOS)
    - Divides values of 1 to 1045 or 1 to 8, even and odd
    - Analog and digital delays
- 50% duty cycle on all outputs for all divides
- Separate synchronization of bank A and B.
- RMS additive jitter 50 fs at 800 MHz
  - 50-fs RMS additive jitter (12 kHz to 20 MHz)
- Industrial temperature range: –40°C to 85°C
- 3.15-V to 3.45-V Operation

2 Applications

- High Performance Clock Distribution and Division
- Wireless Infrastructure
- Datacom and Telecom Clock Distribution
- Medical Imaging
- Test and Measurement
- Military / Aerospace

3 Description

The LMK01801 is a very low noise solution for clocking systems that require distribution and frequency division of precision clocks.

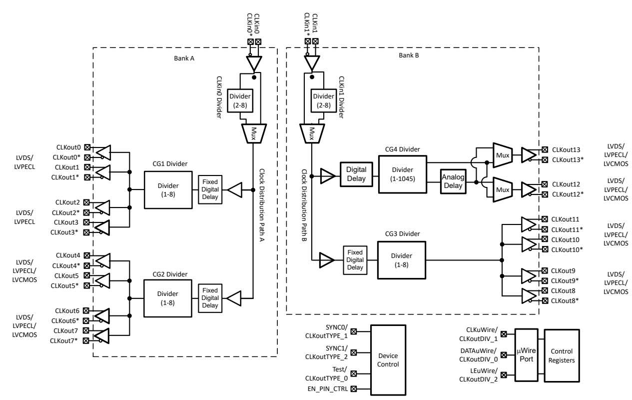
The LMK01801 features extremely low residual noise, frequency division, digital and analog delay adjustments, and fourteen (14) programmable differential outputs: LVPECL, LVDS and LVCMOS (2 outputs per differential output).

The LMK01801 features two independent inputs that can be driven differentially (LVDS, LVPECL) or in single-ended mode (LVCMOS, RF Sinewave). The first input drives output Bank A consisting of eight (8) outputs. The second input drives output Bank B consisting of six (6) outputs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
LMK01801	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2019) to Revision D (September 2021) **Page**

- Updated Delay column for *Clock Output Configurations* table 4
- Added Fixed Digital Delay note for *Clock Output Configurations* table 4
- Changed *Absolute Maximum Ratings* note 1 7
- Added Fixed Digital Delay block for CLKout0 to CLKout11 in *Functional Block Diagram* 14
- Changed content and renamed *Large Divider (1 to 1045)* section to *CLKout0 to CLKout11 Digital Delay* 15
- Added CLKoutX_Y_OFFSET_PD description to the *Fixed Digital Delay* section 17
- Added CLKoutX_Y_OFFSET_PD description to *SYNC Timing* section 19
- Added CLKoutX_Y_OFFSET_PD to Figure 9-1 19
- Added CLKoutX_Y_OFFSET_PD to Figure 9-2 19
- Added CLKoutX_Y_OFFSET_PD to the *Register Map* table 27
- Added CLKoutX_Y_OFFSET_PD fields to the *Default Device Register Settings* table 28
- Added *CLKoutX_Y_OFFSET_PD* section 35

Changes from Revision B (January 2019) to Revision C (October 2019) **Page**

- Changed Test/CLKoutTYPE_0 type from: I to: I/O 5
- Added propagation delay parameter in the *Electrical Characteristics* table 8
- Added note to *Clock Output Synchronization (SYNC)* section 19
- Changed *Clock Output Synchronization Using the SYNC1 Pin* graphic 19
- Changed the *Relative Dynamic Digital Delay Programming Example, 2nd Adjust* graphic 24
- Changed divide value for 1 (0x01) in the *CLKinX_DIV* table from: 2 to: 1 30
- Changed *CLKoutX_Y_Div, 2 Bits* table title to: *CLKoutX_Y_Div, 3 Bits* 37
- Added *Unused GPIO (CLKoutTYPE_X)* section 47

Changes from Revision A (April 2013) to Revision B (January 2019) **Page**

- Added *Device Information* table 1
- Changed Pin Control Mode Table for EN_PIN_CTRL = Low 4
- Added SPI note for Pin Control Mode Tables 4
- Changed polarity for pins 4,5 and 9,10 to be correct 5

Copyright © 2021 Texas Instruments Incorporated

Changes from Revision * (April 2013) to Revision A (April 2013)	Page

5 Device Comparison

5.1 Functional Configurations

Table 5-1. Clock Output Configurations

Bank	Input	Clock Group	Output CLKoutX/CLKoutX*	Output Type	Outputs in Divider Group	Divider Ratios	Delay
A	CLKin0/ CLKin0*	CG1	0 to 3	LVDS/LVPECL	0 to 3	1 to 8	Fixed Digital(2)
		CG2	4 to 7	LVDS/LVPECL/ LVCMOS	4 to 7	1 to 8	Fixed Digital(2)
B	CLKin1/ CLKin1*	CG3	8 to 11	LVDS/LVPECL/ LVCMOS	8 to 11	1 to 8	Fixed Digital(2)
		CG4	12 and 13	LVDS/LVPECL/ LVCMOS	12 and 13	1 to 1045(1)	Digital and Analog(3)

(1) Digital Delay will not work if CLKout12_13_DIV = 1.
(2) Fixed Digital Delay occurs when CLKoutX_Y_OFFSET_PD = 0. See Section 9.4.5.
(3) See Section 7.4

Table 5-2. Pin Control Mode for EN_PIN_CTRL = Low(1)

Pin	Output Groups	Pin=Low	Pin=Middle	Pin=High
CLKoutTYPE_0	CLKout0 to CLKout3	LVDS	Powerdown	LVPECL
	CLKout4 to CLKout7		LVCMOS (Norm/Inv)	
CLKoutTYPE_1	CLKout8 to CLKout11	LVDS	LVCMOS (Norm/Inv)	LVPECL
CLKoutTYPE_2	CLKout12 to CLKout13	LVDS	LVCMOS (Norm/Inv)	LVPECL
CLKoutDIV_0	CLKout0 to CLKout3 Divider	÷ 1	÷ 4	÷ 2
CLKoutDIV_1	CLKout4 to CLKout7 Divider	÷ 1	÷ 4	÷ 2
CLKoutDIV_2	CLKout8 to CLKout11 Divider	÷ 1	÷ 4	÷ 2
	CLKout12 to CLKout13 Divider	÷ 8	÷ 512	÷ 16

(1) Floating is SPI. See Section 9.4.2.

Table 5-3. Pin Control Mode for EN_PIN_CTRL = High(1) (2)

Pin	Output Groups	Pin=Low	Pin=Middle	Pin=High
CLKoutTYPE_0	CLKout0 to CLKout3	LVDS	LVPECL	LVPECL
	CLKout4 to CLKout7		LVCMOS (Norm/Inv)	
CLKoutTYPE_1	CLKout8 to CLKout11	LVDS	LVCMOS (Norm/Inv)	LVPECL
CLKoutTYPE_2	CLKout12 to CLKout13	LVDS	LVCMOS (Norm/Inv)	LVPECL
CLKoutDIV_0	CLKout0 to CLKout7 Dividers	÷ 1	÷ 4	÷ 2
CLKoutDIV_1	CLKout8 to CLKout11 Divider	÷ 1	÷ 4	÷ 2
CLKoutDIV_2	CLKout12 to CLKout13 Divider	÷ 4	÷ 512	÷ 16

(1) Digital Delay will not work if CLKout12_13_DIV = 1.
(2) See Section 7.4

Copyright © 2021 Texas Instruments Incorporated

6 Pin Configuration and Functions

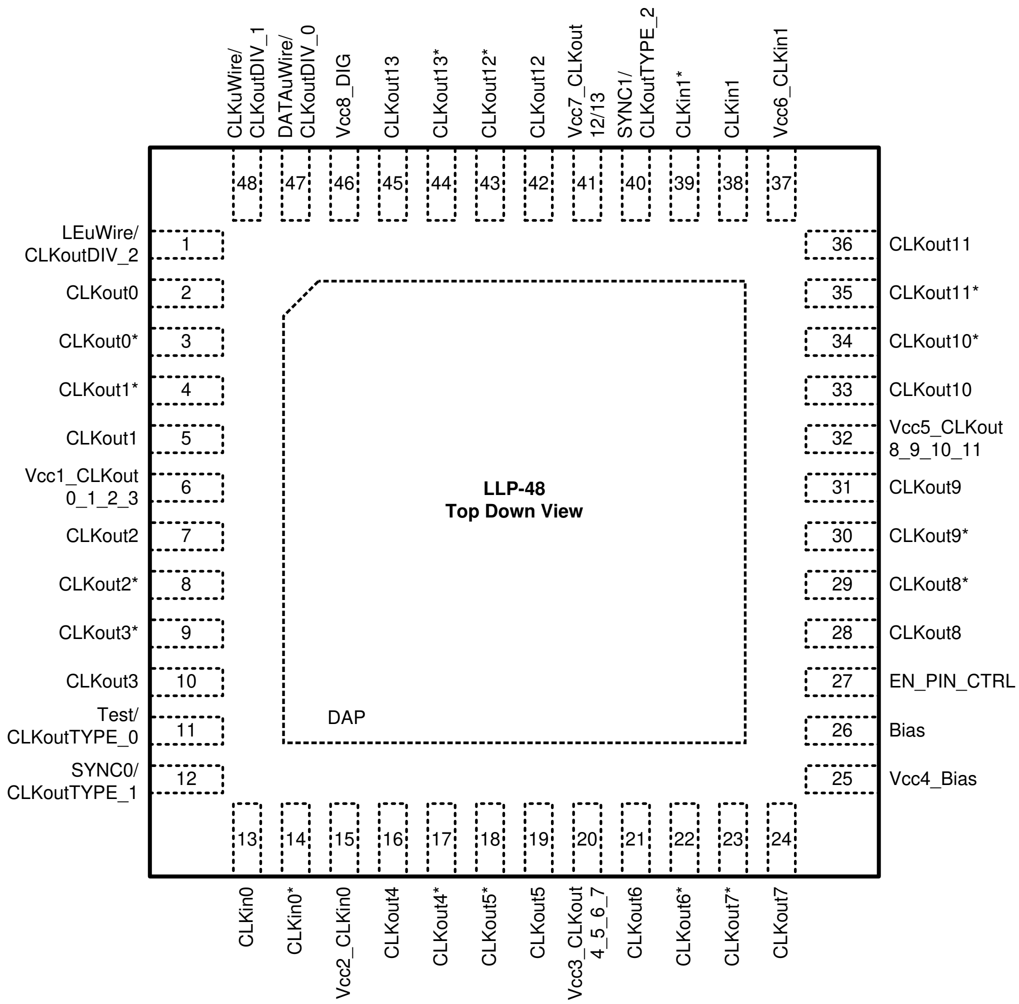


Figure 6-1. 48-Pin Package

Table 6-1. Pin Functions(1)

Pin Number	Name(s)	I/O	Type	Description
1	LEuWire/ CLKoutDIV_2	I	CMOS / 3-State	MICROWIRE Latch Enable Input / Pin control mode: clock divider 2
2, 3	CLKout0, CLKout0*	O	Programmable	Clock output 0: LVDS or LVPECL
4, 5	CLKout1*, CLKout1	O	Programmable	Clock output 1: LVDS or LVPECL
6	Vcc1_CLKout 0_1_2_3	I	PWR	Power supply for clock outputs 0, 1, 2, and 3
7, 8	CLKout2, CLKout2*	O	Programmable	Clock output 2: LVDS or LVPECL
9, 10	CLKout3*, CLKout3	O	Programmable	Clock output 3: LVDS or LVPECL
11	Test/ CLKoutTYPE_0	I/O	CMOS / 3-State	Reserved Test Pin / Pin control mode: clock output type select 0
12	SYNC0/ CLKoutTYPE_1	I	CMOS / 3-State	SYNC0 / Pin control mode: clock output type select 1
13, 14	CLKin0, CLKin0*	I	ANLG	Clock input 0. Supports clocking types including but not limited to LVDS, LVPECL, and LVCMOS

Copyright © 2021 Texas Instruments Incorporated

Table 6-1. Pin Functions(1) (continued)

Pin Number	Name(s)	I/O	Type	Description
15	Vcc2_CLKin0	I	PWR	Power supply for clock input 0
16, 17	CLKout4, CLKout4*	O	Programmable	Clock output 4: LVDS, LVPECL, or LVCMOS
18, 19	CLKout5*, CLKout5	O	Programmable	Clock output 5: LVDS, LVPECL, or LVCMOS
20	Vcc3_CLKout 4_5_6_7	I	PWR	Power supply for clock outputs 4, 5, 6, and 7
21, 22	CLKout6, CLKout6*	O	Programmable	Clock output 6: LVDS, LVPECL, or LVCMOS
23, 24	CLKout7*, CLKout7	O	Programmable	Clock output 7: LVDS, LVPECL, or LVCMOS
25	Vcc4_Bias	I	PWR	Power supply for Bias
26	Bias		ANLG	Bias bypass pin
27	EN_PIN_CTRL	I	3-State	Select MICROWIRE or pin control mode
28, 29	CLKout8, CLKout8*	O	Programmable	Clock output 8: LVDS, LVPECL, or LVCMOS
30, 31	CLKout9*, CLKout9	O	Programmable	Clock output 9: LVDS, LVPECL, or LVCMOS
32	Vcc5_CLKout 8_9_10_11	I	PWR	Power supply for clock outputs 8, 9, 10, and 11
33, 34	CLKout10, CLKout10*	O	Programmable	Clock output 10: LVDS, LVPECL, or LVCMOS
35, 36	CLKout11*, CLKout11	O	Programmable	Clock output 11: LVDS, LVPECL, or LVCMOS
37	Vcc6_CLKin1	I	PWR	Power supply for clock input 1
38, 39	CLKin1, CLKin1*	I	ANLG	Clock input 1. Supports clocking types including but not limited to LVDS, LVPECL, and LVCMOS
40	SYNC1/ CLKoutTYPE_2	I	CMOS / 3-State	SYNC pin for CLKin1 and bank B. Pin control mode: Clock output type select 2
41	Vcc7_CLKout 12_13	I	PWR	Power supply for clock outputs 12, and 13
42, 43	CLKout12, CLKout12*	O	Programmable	Clock output 12: LVDS, LVPECL, or LVCMOS
44, 45	CLKout13*, CLKout13	O	Programmable	Clock output 13: LVDS, LVPECL, or LVCMOS
46	Vcc8_DIG	I	PWR	Power supply for digital
47	DATAuWire/ CLKoutDIV_0	I	CMOS / 3-State	MICROWIRE DATA Pin / Pin control mode: Clock divider 0
48	CLKuWire/ CLKoutDIV_1	I	CMOS / 3-State	MICROWIRE CLK Pin / Pin control mode: Clock divider 1
DAP	DAP		GND	DIE ATTACH PAD, connect to GND

(1) See Section 12.1.1 for recommended connections.

Copyright © 2021 Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

see (1) (2) (3) (5)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage (4)	–0.3	3.6	V
V_{IN}	Input Voltage	–0.3	(V_{CC} + 0.3)	V
T_L	Lead Temperature (solder 4 seconds)		260	°C
I_{IN}	Differential Input Current (CLKinX/X*)		±5	mA
MSL	Moisture Sensitivity Level		3	
T_{stg}	Storage Temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) This device is a high performance RF integrated circuit with an ESD rating up to 2.5 kV Human Body Model, up to 250 V Machine Model and up to 1,250 V Charged Device Model and is ESD sensitive. Handling and assembly of this device should only be done at ESD-free workstations.
(3) Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is only implied at these or any other conditions in excess of those given in the operation sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.
(4) Never to exceed 3.6 V.
(5) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

7.2 Recommended Operating Conditions

PARAMETER			MIN	NOM	MAX	UNIT
T_A	Ambient Temperature	V_{CC} = 3.3 V	-40	25	85	°C
V_{CC}	Supply Voltage		3.15	3.3	3.45	V
T_J	Junction Temperature				125	°C

7.3 Thermal Information

48-Lead WQFN

		VALUE	UNIT
θ_{JA}	Thermal resistance from junction to ambient on 4-layer JEDEC board (1)	26	°C/W
θ_{JC}	Thermal resistance from junction to case	3	°C/W

(1) Specification assumes 9 thermal vias connect the die attach pad to the embedded copper plane on the 4-layer JEDEC board. These vias play a key role in improving the thermal performance of the WQFN. It is recommended that the maximum number of vias be used in the board layout.

7.4 Electrical Characteristics

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ 85°C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25°C, at the Recommended Operating Conditions at the time of product characterization and are not ensured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
I_{CC_PD}	Power Down Supply Current			1		mA
I_{CC_CLKS}	Supply Current with all clocks enabled (2)	All clock delays disabled, CLKoutX_Y_DIV = 1, CLKoutX_TYPE = 1 (LVDS),		313	390	mA
CLKin0/0* AND CLKin1/1* INPUT CLOCK SPECIFICATIONS						
f_{CLKinX}	Clock 0 or 1 Input Frequency	CLKinX_MUX = Bypassed CLKoutX_Y_DIV = 1	0.001		3100	MHz
		CLKinX_MUX = Bypassed CLKoutX_Y_DIV = 2 to 8	0.001		1600	MHz
		CLKin_MUX = Divide CLKinX_DIV = 2 to 8	0.001		3100	MHz
$SLEW_{CLKin}$	Slew Rate on CLKin (3)	20% to 80%	0.15	0.5		V/ns
$DUTY_{CLKin}$	Clock input duty cycle			50%		
V_{CLKin}	Clock Input, Single-ended Input Voltage	AC coupled to CLKinX; CLKinX* AC coupled to Ground (CLKinX_BUF_TYPE = Bipolar	0.25		2.4	Vpp
		AC coupled to CLKinX; CLKinX* AC coupled to Ground (CLKinX_BUF_TYPE = MOS	0.25		2.4	Vpp
$V_{ID}CLK_{in}$	Clock Input Differential Input Voltage (1) (9)	AC coupled (CLKinX_BUF_TYPE = Bipolar	0.25		1.55	|V|
$V_{SS}CLK_{in}$			0.5		3.1	Vpp
$V_{ID}CLK_{in}$		AC coupled (CLKinX_BUF_TYPE = MOS	0.25		1.55	|V|
$V_{SS}CLK_{in}$			0.5		3.1	Vpp
$V_{CLKinX\text{-}offset}$	DC offset voltage between CLKinX/ CLKinX* CLKinX* - CLKinX	Each pin AC coupled CLKinX_BUF_TYPE = Bipolar		0		mV
				0		mV
$V_{CLKin\text{-}}V_{IH}$	Maximum input voltage	DC coupled to CLKinX; CLKinX* AC coupled to Ground CLKinX_BUF_TYPE = MOS	2.0		V_{CC}	V
$V_{CLKin\text{-}}V_{IL}$	Minimum input voltage		0.0		0.4	V
$V_{CLKinX\text{-}offset}$	DC offset voltage between CLKinX/ CLKinX* CLKinX* - CLKinX	Each pin AC coupled CLKinX_BUF_TYPE = MOS		55		mV
DIGITAL INPUTS (CLKuWire, DATAuWire, LEuWire) for EN_PIN_CTRL = MIDDLE						
V_{IH}	High-Level Input Voltage		1.2		V_{CC}	V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IH}	High-Level Input Current	V_{IH} = V_{CC}	-5		5	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0	-5		5	µA
DIGITAL INPUTS (SYNC0, SYNC1) FOR EN_PIN_CTRL = MIDDLE						
V_{IH}	High-Level Input Voltage		1.2		V_{CC}	V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IH}	High-Level Input Current V_{IH} = V_{CC}	V_{IH} = V_{CC}	-5		5	µA
I_{IL}	Low-Level Input Current V_{IL} = 0 V	V_{IL} = 0	-40		-5	µA
DIGITAL INPUTS (CLKuWire, DATAuWire, LEuWire, SYNC0, SYNC1) FOR EN_PIN_CTRL= LOW OR HIGH						
V_{IH}	High-Level Input Voltage		2.6		V_{CC}	V
V_{IM}	Mid-Level Input Voltage		1.3		1.85	V

Copyright © 2021 Texas Instruments Incorporated

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ 85°C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25°C, at the Recommended Operating Conditions at the time of product characterization and are not ensured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-Level Input Voltage				0.7	V
I_{IH}	High-Level Input Current	V_{IH} = V_{CC}			100	µA
I_{IM}	Mid-Level Input Current		-10		10	µA
I_{IL}	Low-Level Input Current	V_{IL}= 0	-100			µA
CLOCK SKEW AND DELAY						
T_{PD}	CLKinX to CLKoutY	Single-ended CLKinX* input, LVDS output		2.25		ns
T_{SKEW}	CLKoutX to CLKoutY (4) (5)	LVDS-to-LVDS, T = 25°C, F_{CLK} = 800 MHz, R_L= 100 Ω AC coupled, Within same Divider		3		ps
		LVPECL-to-LVPECL, T = 25°C F_{CLK} = 800 MHz, R_L= 100 Ω emitter resistors = 240 Ω to GND AC coupled, Within same Divider		3		
	Skew between any two LVCMOS outputs, same CLKout or different CLKout (4) (5)	R_L = 50 Ω, C_L = 10 pF, T = 25 °C, F_{CLK} = 100 MHz, Within same Divider		50		
MixedT_{SKEW} CLKoutX - CLKoutY	LVPECL to LVDS skew	Same device, T = 25°C, 250 MHz, Within same Divider		32		ps
	LVDS to LVCMOS skew			830		
	LVCMOS to LVPECL skew			800		
F_{ADLY}	Maximum Analog Delay Frequency		1536			MHz
LVDS CLOCK OUTPUTS (CLKoutX)						
f_{CLKout}	Maximum Clock Frequency (5) (6)	R_L = 100 Ω	1600			MHz
V_{OD}	Differential Output Voltage (1) (9)	T = 25°C, DC measurement AC coupled to receiver input R = 100 Ω differential termination	225	400	575	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for complementary output states		-50		50	mV
V_{OS}	Output Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} for complementary output states				35	|mV|
T_R	Output Rise Time	20% to 80%, R_L = 100 Ω		200		ps
T_F	Output Fall Time	80% to 20%, R_L = 100 Ω		300		ps
I_{SA} I_{SB}	Output short circuit current - single ended	Single-ended output shorted to GND, T = 25°C	-24		24	mA
I_{SAB}	Output short circuit current - differential	Complimentary outputs tied together	-12		12	mA

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ 85°C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25°C, at the Recommended Operating Conditions at the time of product characterization and are not ensured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVPECL CLOCK OUTPUTS (CLKoutX)						
T_R	Output Rise Time	20% to 80%, R_L = 100 Ω, emitter resistors = 240 Ω to GND		200		ps
T_F	Output Fall Time	80% to 20%, R_L = 100 Ω, emitter resistors = 240 Ω to GND		200		ps
LOW COMMON-MODE VOLTAGE PECL (LCPECL)[(7), (8)]						
f_{CLKout}	Maximum Clock Frequency (5) (6)	R_L = 100 Ω, emitter resistors = 240 Ω to GND	3100			MHz
V_{OH}	Output High Voltage	T = 25°C, DC Measurement Termination = 50 Ω to V_{CC} - 0.6 V		1.6		V
V_{OL}	Output Low Voltage			0.75		V
V_{OD}	Output Voltage		535	840	1145	mV
1600-mV LVPECL (LVPECL) CLOCK OUTPUTS (CLKoutX)						
f_{CLKout}	Maximum Clock Frequency (5) (6)	R_L = 100 Ω, emitter resistors = 240 Ω to GND	3100			MHz
V_{OH}	Output High Voltage	T = 25°C, DC Measurement Termination = 50 Ω to V_{CC} - 2.0 V		V_{CC} - 0.94		V
V_{OL}	Output Low Voltage			V_{CC} - 1.9		V
V_{OD}	Output Voltage		585	925	1240	mV
2000-mV LVPECL (2VPECL) CLOCK OUTPUTS (CLKoutX)						
f_{CLKout}	Maximum Clock Frequency (5) (6)	R_L = 100 Ω, emitter resistors = 240 Ω to GND	3100			MHz
V_{OH}	Output High Voltage	T = 25°C, DC Measurement Termination = 50 Ω to V_{CC} - 2.3 V		V_{CC} - 0.97		V
V_{OL}	Output Low Voltage			V_{CC} - 1.95		V
V_{OD}	Output Voltage		705	1150	1585	mV
LVCMOS CLOCK OUTPUTS (CLKoutX)						
f_{CLKout}	Maximum Clock Frequency (5) (6)	5-pF Load	250			MHz
V_{OH}	Output High Voltage	1-mA Load	V_{CC} - 0.1			V
V_{OL}	Output Low Voltage	1-mA Load			0.1	V
I_{OH}	Output High Current (Source)	V_{CC} = 3.3 V, V_O = 1.65 V		28		mA
I_{OL}	Output Low Current (Sink)	V_{CC} = 3.3 V, V_O = 1.65 V		28		mA
$DUTY_{CLK}$	Output Duty Cycle (5)	V_{CC}/2 to V_{CC}/2, F_{CLK} = 100 MHz, T = 25 °C	45%	50%	55%	
T_R	Output Rise Time	20% to 80%, R_L = 50 Ω, C_L = 5 pF		400		ps
T_F	Output Fall Time	80% to 20%, R_L = 50 Ω, C_L = 5 pF		400		ps

Copyright © 2021 Texas Instruments Incorporated

3.15 V ≤ V_{CC} ≤ 3.45 V, –40°C ≤ T_A ≤ 85°C. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25°C, at the Recommended Operating Conditions at the time of product characterization and are not ensured.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICROWIRE INTERFACE TIMING						
T_{ECS}	LE to Clock Set Up Time	See MICROWIRE Input Timing	25			ns
T_{DCS}	Data to Clock Set Up Time	See MICROWIRE Input Timing	25			ns
T_{CDH}	Clock to Data Hold Time	See MICROWIRE Input Timing	8			ns
T_{CWH}	Clock Pulse Width High	See MICROWIRE Input Timing	25			ns
T_{CWL}	Clock Pulse Width Low	See MICROWIRE Input Timing	25			ns
T_{CES}	Clock to LE Set Up Time	See MICROWIRE Input Timing	25			ns
T_{EWH}	LE Pulse Width	See MICROWIRE Input Timing	25			ns

(1) See applications section Section 8.1 for definition of V_{ID} and V_{OD} voltages.
(2) For Icc for specific part configuration, see applications section Section 11.1 for calculating Icc.
(3) The minimum recommended slew rate for all input clocks is 0.5 V/ns. This is especially true for single-ended clocks. Phase noise performance will begin to degrade as the clock input slew rate is reduced. However, the device will function at slew rates down to the minimum listed. When compared to single-ended clocks, differential clocks (LVDS, LVPECL) will be less susceptible to degradation in phase noise performance at lower slew rates due to their common mode noise rejection. However, it is also recommended to use the highest possible slew rate for differential clocks to achieve optimal phase noise performance at the device outputs.
(4) Equal loading and identical clock output configuration on each clock output is required for specification to be valid. Specification not valid for delay mode.
(5) Ensured by characterization.
(6) Refer to typical performance charts for output operation performance at higher frequencies than the minimum maximum output frequency.
(7) For LCPECL, the common mode voltage is regulated (VOH=1.6V, VOL=VOH-Vsw, Vcm=(VOH+VOL)/2) and is more stable against with PVT (process, supply, temperature) variations than conventional LVPECL implementations..
(8) With proper selection of external emitter resistors, LCPECL can also be used for DC-coupling with devices with low common voltage such as 0.5V or 0.8V etc.
(9) Refer to application note *AN-912 Common Data Transmission Parameters and their Definitions* (SNLA036) for more information.

7.5 Serial MICROWIRE Timing Diagram

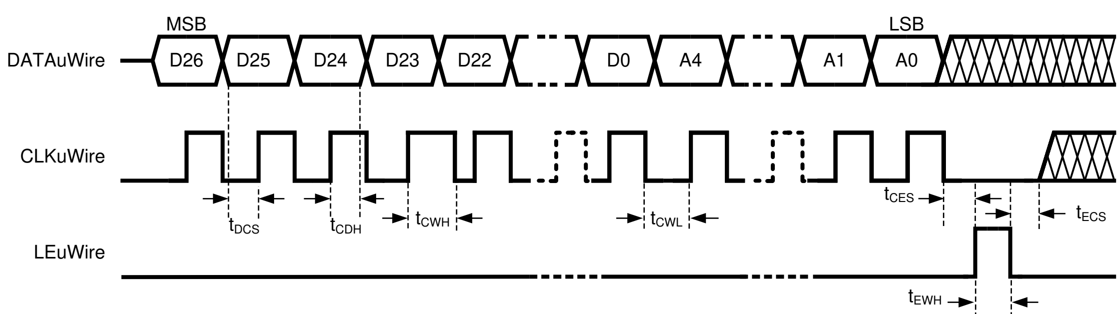
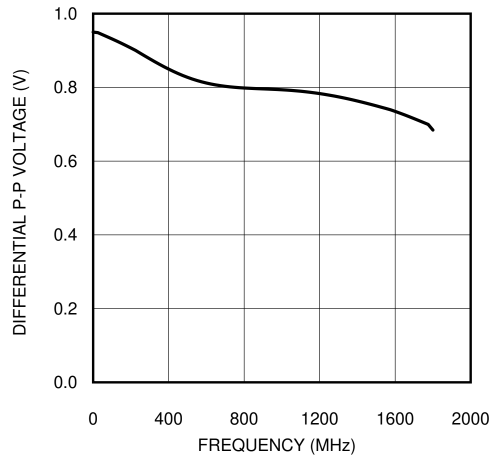


Figure 7-1. MICROWIRE Timing Diagram

Register programming information on the DATAuWire pin is clocked into a shift register on each rising edge of the CLKuWire signal. On the rising edge of the LEuWire signal, the register is sent from the shift register to the register addressed. A slew rate of at least 30 V/μs is recommended for these signals. After programming is complete the CLKuWire, DATAuWire, and LEuWire signals should be returned to a low state.

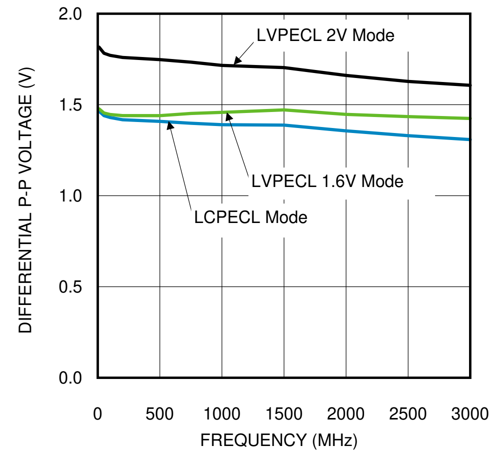
7.6 Typical Characteristics

Unless otherwise specified: V_{dd}=3.3V, T_A=25 °C



See Section 8.1 for a description of V_{SS}.

Figure 7-2. LVDS V_{SS} vs. Frequency



See Section 8.1 for a description of V_{SS}.

Figure 7-3. LVPECL V_{SS} vs. Frequency

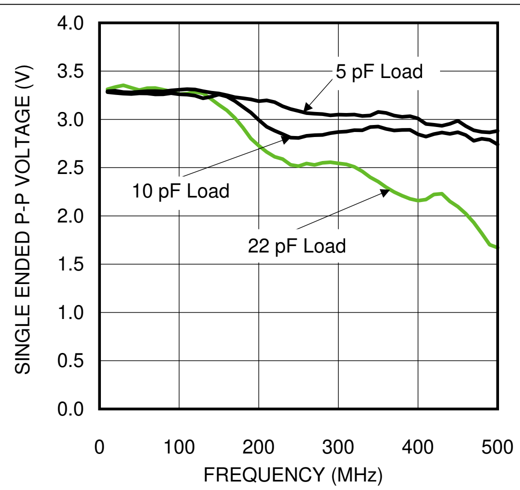


Figure 7-4. LVCMOS Vpp vs. Frequency

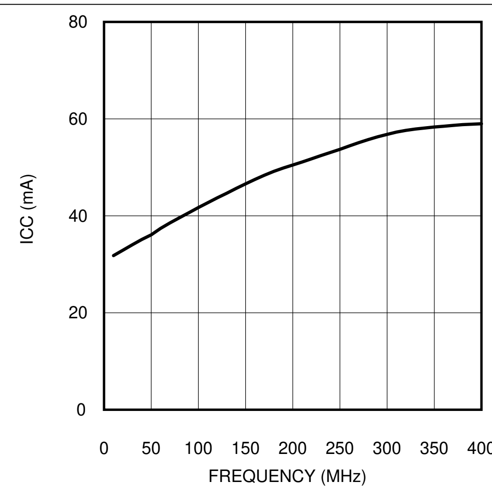


Figure 7-5. Typical Dynamic I_{CC}, C_L = 5 pF

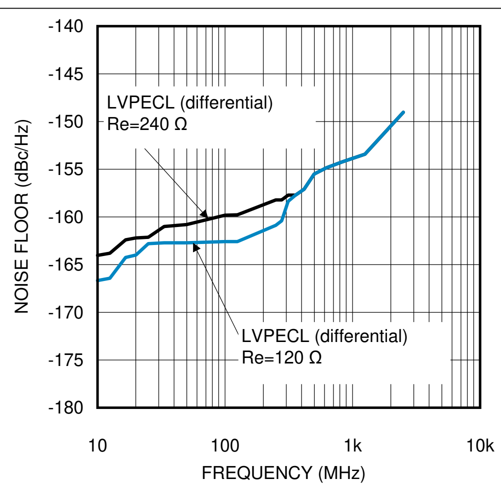
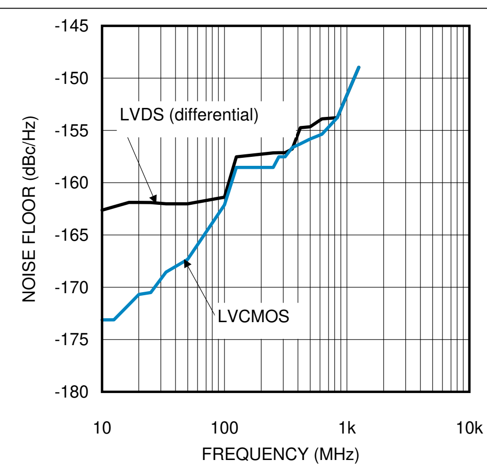


Figure 7-6. LVPECL Noise Floor vs. Frequency



See Section 8.1 for a description of V_{SS}.

Figure 7-7. LVDS & LVCMOS Noise Floor vs. Frequency

Copyright © 2021 Texas Instruments Incorporated

8 Parameter Measurement Information

8.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading data sheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and discern between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and non-inverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the non-inverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first section

Figure 8-1 illustrates the two different definitions side-by-side for inputs and Figure 8-2 illustrates the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the noninverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined in volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

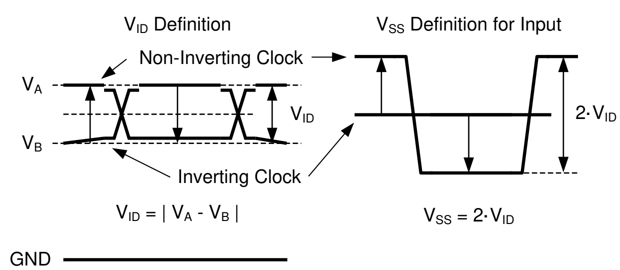


Figure 8-1. Two Different Definitions for Differential Input Signals

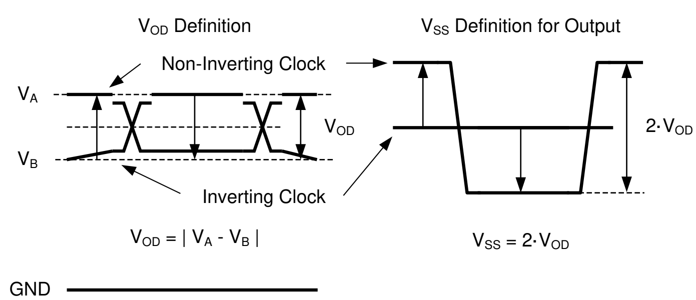


Figure 8-2. Two Different Definitions for Differential Output Signals

Copyright © 2021 Texas Instruments Incorporated

9 Detailed Description

9.1 Overview

The LMK01801 is a dual clock buffer which allows separate clock domains on the same IC with options to divide and delay signals.

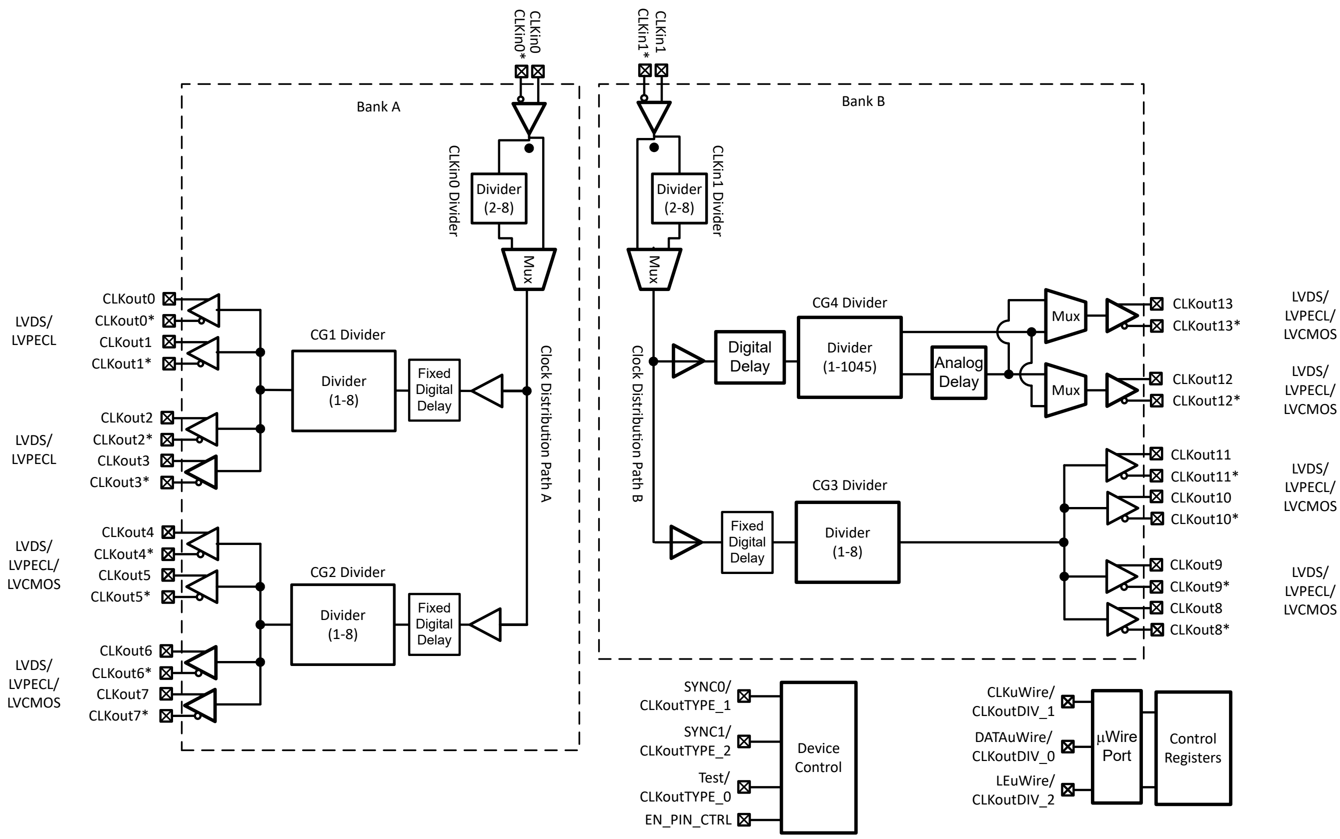
The LMK01801 consists of two separate buffer banks, each with its own input divider, output dividers and programmable control of clock output channels.

- Bank A has two clock output groups, see the Section 5.1 for more details.
- Bank B has two clock output groups, one of which has analog and digital delay. See the Section 5.1 for more details.

Each bank has it own common input divider and is then divided into output groups which share an output divider.

The LMK01801 comes in a 48-pin WQFN package.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 High-Speed Clock Inputs (CLKin0/CLKin0* and CLKin1/CLKin1*)

The LMK01801 has two clock inputs, CLKin0 and CLKin1 which can be driven differentially or single-ended. See Section 10.1.1.1 for more information. Each input has a 2 to 8 divider that may be enabled or bypassed.

9.3.2 Clock Distribution

The LMK01801 features a total of 14 differential outputs. CLKout0 through CLKout7 are driven from CLKin0 and CLKout8 through CLKout13 are driven from CLKin1.

Copyright © 2021 Texas Instruments Incorporated

9.3.3 Small Divider (1 to 8)

There are three small dividers which drive CLKout0 to CLKout3, CLKout4 to CLKout7, and CLKout8 to CLKout11. These dividers support a divide range of 1 to 8 (even and odd).

9.3.4 Large Divider (1 to 1045)

The divider for CLKout12 and CLKout13 supports a divide range of 1 to 1045 (even and odd). When divides of 26 or greater are used, the divider/delay block uses extended mode.

9.3.5 CLKout Analog Delay

Clock outputs 12 and 13 include a fine (analog) delay for phase adjustment of the clock outputs.

The fine (analog) delay allows a nominal 25 ps step size and range from 0 to 475 ps of total delay. Enabling the analog delay adds a nominal 500 ps of delay in addition to the programmed value.

When adjusting analog delay, glitches may occur on the clock outputs being adjusted.

9.3.6 CLKout0 to CLKout11 Digital Delay

CLKout0 to CLKout11 include a fixed digital delay for phase adjustment of the clock outputs.

The fixed delay allows a group of outputs to be delayed by 5 clock distribution path cycles. The 5-cycle offset takes effect on the clock outputs after a SYNC event. The delay is enabled through the CLKoutX_Y_OFFSET_PD register bit.

See Section 9.4.5 for more information.

Copyright © 2021 Texas Instruments Incorporated

9.3.7 CLKout12 and CLKout13 Digital Delay

CLKout12 and CLKout13 includes a coarse (digital) delay for phase adjustment of the clock outputs.

The coarse (digital) delay allows a group of outputs to be delayed by 4.5 to 12 clock distribution path cycles in normal mode, or from 12.5 to 522 clock cycles in extended mode. The delay step can be as small as half the period of the clock distribution path by using the CLKout12_13_HS bit. For example, a 2-GHz clock frequency without using CLKin1 input clock divider results in 250-ps coarse tuning steps.

The coarse (digital) delay value takes effect on the clock outputs after a SYNC event.

There are 2 different ways to use the digital (coarse) delay.

1. Fixed Digital Delay
2. Relative Dynamic Digital Delay

See *Device Functional Modes* for more information.

9.3.8 Programmable Outputs

The outputs of the LMK01801 are programmable in a combination of output types based on Table 5-1. Programming the outputs is by MICROWIRE or by pin control mode based on the state of EN_PIN_CTRL pin.

Any LVPECL output type can be programmed to LCPECL, 1600, or 2000 mVpp amplitude levels. The 2000 mVpp LVPECL output type is a Texas Instruments proprietary configuration that produces a 2000 mVpp differential swing for compatibility with many data converters and is also known as 2VPECL.

9.3.9 Clock Output Synchronization

Using the SYNC input causes all active clock outputs to share a rising edge. See Section 9.4.6 for more information.

The SYNC event also causes the digital delay value to take effect.

9.3.10 Default Clock Outputs

The power on reset sets the device to operate with all outputs active in bypass mode (no divide) with LVDS output type. In this way the device can be used without programming for fan-out purposes.

Copyright © 2021 Texas Instruments Incorporated

9.4 Device Functional Modes

9.4.1 Programmable Mode

When the EN_PIN_CTRL pin is floating (default by internal pull-up/pull-down) then programming is via MICROWIRE.

See Table 5-1 for a description of available programming options for the LMK01801 in programmable mode.

9.4.2 Pin Control Mode

The LMK01801 provides for an alternate function of the MICROWIRE (uWire) pins. This pin control mode is set by the logic of the EN_PIN_CTRL pin to provide limited control of the outputs and dividers.

When the EN_PIN_CTRL pin is set high or low (not open) then the output states can be programmed by pins, eliminating the need for an external FPGA or CPU.

If EN_PIN_CTRL is LOW then Table 5-2 in Section 5.1 defines how the outputs and dividers are configured.

If EN_PIN_CTRL is HIGH then Table 5-3 in Section 5.1 defines how the outputs and dividers are configured.

9.4.3 Inputs / Outputs

9.4.3.1 CLKin0 and CLKin1

There are two clock inputs CLKin0 and CLKin1. CLKin0 provides the input for output Bank A and CLKin1 provides the input for the output Bank B. Each input has it's own divider (2 to 8) that may be bypassed.

9.4.4 Input and Output Dividers

This section discusses the recommended usage of input and output dividers.

Clock inputs 0 and 1 each have an associated divider (2 to 8) that may be enabled or bypassed.

Clock groups 1, 2 and 3 have small output dividers (1 to 8). Clock group 4 (CLKout12 and CLKout13) has a large output divider (1 to 1045).

While the input and output clock dividers may be used in any combination the recommended operating frequency ranges are shown in the table below to minimize the phase noise floor:

Table 9-1. Input and Output Divider Input Frequency Ranges

Input Divider	Output Divider	Max Frequency
Bypassed	Divide = 1	3.1 GHz
Bypassed	Divide > 1	1.6 GHz
Divide = 2 to 8	Divide = 1 to 8	3.1 GHz

9.4.5 Fixed Digital Delay

This section discusses Fixed Digital Delay and associated registers.

Clock outputs 0 to 11 may be delayed after synchronization by a fixed offset of 5 clock distribution path cycles. The CLKoutX_Y_OFFSET_PD register bit inserts the delay for each respective clock group. By default, the fixed offset is enabled for CLKout8_11 and disabled for CLKout0_3 and CLKout4_7. CLKoutX_Y_OFFSET_PD aligns the specified clock group with CLKout12_13 after a SYNC event upon meeting the following conditions:

1. The input clock frequency of the specified clock group(s) is the same as CLKout12_13 (CLKin1).
2. CLKout12_13 does not have any digital or analog delays enabled.

See SYNC Timing for further synchronization details on CLKoutX_Y_OFFSET_PD.

Clock outputs 12 and 13 may be delayed relative to CLKout8 to CLKout11 by up to 517.5 clock distribution path periods if divide is 1 and 518.5 clock distribution path periods if divide is greater than 1. By programming a digital delay value from 4.5 to 522 clock distribution path periods, a relative clock output delay from 0 to 517.5 periods is achieved. The CLKout12_13_DDLY register sets the digital delay as shown in the table Table 9-2.

Copyright © 2021 Texas Instruments Incorporated

Table 9-2. Possible Digital Delay Values

CLKout12_13_DDLY	CLKout12_13_HS	DIGITAL DELAY
5	1	4.5
5	0	5
6	1	5.5
6	0	6
7	1	6.5
7	0	7
...	...	...
520	0	520
521	1	520.5
521	0	521
522	1	521.5
522	0	522

The CLKout12_13_DDLY value only takes effect during a SYNC event and if the NO_SYNC_CLKout12_13 bit is cleared for this clock group. See Section 9.4.6 for more information.

The resolution of digital delay is related to the frequency at the input to the Clock Group 4 (CG4) clock distribution path.

Digital Delay Resolution = 1 / (2 * Clock Frequency)

The digital delay between clock outputs can be dynamically adjusted with minimum or no disruption of the output clocks. See Section 9.4.6.1 for more information.

9.4.5.1 Fixed Digital Delay - Example

Given a CLKin1 clock frequency of 983.04 MHz as input to CG4, by using digital delay the outputs can be adjusted in 1 / (2 * 983.04 MHz) = ~509 ps steps (Assumes CLKin1_MUX = bypass).

To achieve a quadrature (90 degree) phase shift on 122.88 MHz outputs between CLKout12 and CLKout11 from a clock frequency of 983.04 MHz program:

- Clock output divider to 8. CLKout8_11 = 8 and CLKout12_13_DIV = 8
- Set clock digital delay value. CLKout12_13_DDLY = 5, CLKout12_13_HS = 0.

The frequency of 122.88 MHz has a period of ~8.14 ns. To delay 90 degrees of a 122.88 MHz clock period requires a ~2.03 ns delay. Given a digital delay step of ~509 ps, this requires a digital delay value of 4 steps (2.03 ns / 509 ps = 4). Since the 4 steps are half period steps, CLKout12_13_DDLY is programmed 2 full periods beyond 5 for a total of 7.

Table 9-3 shows some of the possible phase delays in degrees achievable in the above example.

Table 9-3. Relative Phase Shift From CLKout12 and CLKout13 to CLKout8 to CLKout11

CLKout12_13_DDLY	CLKout12_13_HS	Relative Digital Delay	Degrees of 122.88 MHz
5	1	-0.5	-23°
5	0	0.0	0°
6	1	0.5	23°
6	0	1.0	45°
7	1	1.5	68°
7	0	2.0	90°
8	1	2.5	113°
8	0	3.0	135°
9	1	3.5	158°

Copyright © 2021 Texas Instruments Incorporated

Table 9-3. Relative Phase Shift From CLKout12 and CLKout13 to CLKout8 to CLKout11 (continued)

CLKout12_13_DDLY	CLKout12_13_HS	Relative Digital Delay	Degrees of 122.88 MHz
9	0	4.0	180°
10	1	4.5	203°
10	0	5.0	225°
11	1	5.5	248°
11	0	6.0	270°
12	1	6.5	293°
12	0	7.0	315°
13	1	7.5	338°
13	0	8.0	360°
...	...	...	...

Figure 9-2 illustrates clock outputs programmed with different digital delay values during a SYNC event.

Refer to Section 9.4.6.1 for more information on dynamically adjusting digital delay.

9.4.6 Clock Output Synchronization (SYNC)

The purpose of the SYNC function is to synchronize the clock outputs with a fixed and known phase relationship between each clock output selected for SYNC. SYNC can also be used to hold the outputs in a low or 0 state. The NO_SYNC_CLKoutX_Y bits can be set to disable synchronization for a clock group.

The digital delay value set by CLKout12_13_DDLY takes effect only upon a SYNC event. The digital delay due to CLKout12_13_HS takes effect immediately upon programming. See Section 9.4.6.1 for more information on dynamically changing digital delay.

It is necessary to ensure that the CLKin1 signal is stable before a sync event occurs when CLKout12_13_DIV is greater than 1.

Copyright © 2021 Texas Instruments Incorporated

Effect of SYNC

When SYNC is asserted, the outputs to be synchronized are held in a logic low state. When SYNC is unasserted, the clock outputs to be synchronized are activated and will transition to a high state simultaneously with one another except where digital delay values have been programmed.

Refer to Section 9.4.6.1 for SYNC functionality when SYNC_QUAL = 1.

Table 9-4. Steady-State Clock Output Condition Given Specified Inputs

SYNC_POL_INV	SYNC PIN	CLOCK STEADY STATE
0	0	Active
0	1	Low
1	0	Low
1	1	Active

Methods of Generating SYNC

There are three methods to generate a SYNC event:

- Manual:
  - Asserting the SYNC pin according to the polarity set by SYNC_POL_INV.
  - Toggling the SYNC_POL_INV bit though MICROWIRE will cause a SYNC to be asserted.
- Automatic:
  - Programming Register R4 when SYNC_EN_AUTO = 1 will generate a SYNC event for Bank B.
  - Programming Register R5 when SYNC_EN_AUTO = 1 will generate a SYNC event for both Bank A and Bank B.

Due to the high speed of the clock distribution path (as fast as ~322 ps period) and the slow slew rate of the SYNC, the exact clock cycle at which the SYNC is asserted or unasserted by the SYNC is undefined. The timing diagrams show a sharp transition of the SYNC to clarify functionality.

Avoiding clock output interruption due to SYNC

Note

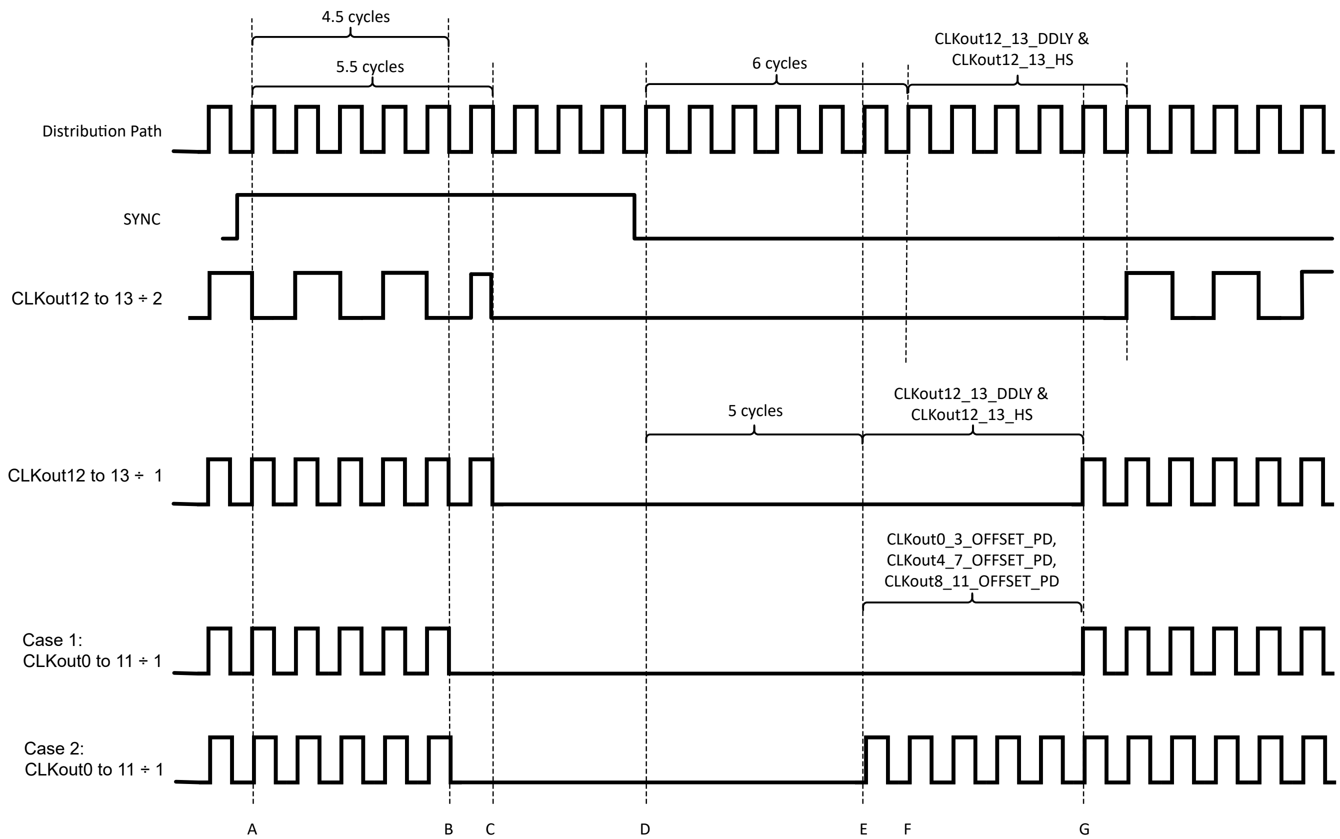
When Automatic SYNC is enabled, after a write to registers 4 of 5, there is an 170-ns delay after LE falling edge before the SYNC event is registered.

If a clock output has the NO_SYNC_CLKoutX_Y bits set they will be unaffected by the SYNC event. It is possible to perform a SYNC operation with the NO_SYNC_CLKoutX_Y bit cleared, set the NO_SYNC_CLKoutX_Y bits so that the selected clocks will not be affected by a future SYNC. Future SYNC events will not effect these clocks but will still cause the newly synchronized clocks to be resynchronized using the currently programmed digital delay values. When this happens, the phase relationship between the first group of synchronized clocks and the second group of synchronized clocks will be undefined. Except for CLKout12 and CLKout13 when synced using qualification mode. See Section 9.4.6.1.

SYNC Timing

When discussing the timing of the SYNC function, one cycle refers to one period of the clock distribution path.

Copyright © 2021 Texas Instruments Incorporated



CLKout12_13_DDLY = 5, CLKout12_13_HS = 0

SYNC1_QUAL = 0 (No qualification), CLKout12_ADLY_SEL & CLKout13_ADLY_SEL = 0

Case 1: CLKout0_3_OFFSET_PD, CLKout4_7_OFFSET_PD, & CLKout8_11_OFFSET_PD = 0

Case 2: CLKout0_3_OFFSET_PD, CLKout4_7_OFFSET_PD, & CLKout8_11_OFFSET_PD = 1

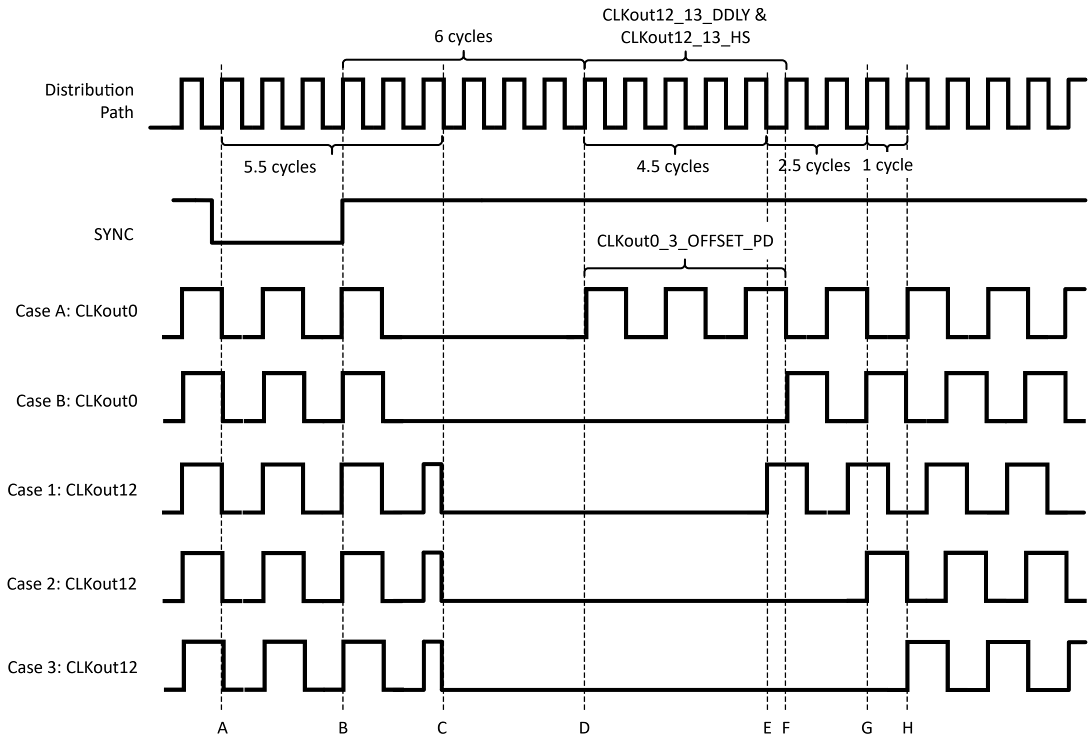
Figure 9-1. Clock Output Synchronization Using the SYNC1 Pin (SYNC1 is Active High, SYNC1_POL_INV = 0)

Refer to Figure 9-1 during this discussion on the timing of SYNC. SYNC must be asserted for greater than one clock cycle of the clock distribution path to register the SYNC event. After SYNC is asserted the SYNC event will begin on the following rising edge of the distribution path clock, at time A. After this event has been registered, the outputs will not reflect the low state for 4.5 cycles for CLKout0 to CLKout11 at time B or 5.5 cycles for CLKout12 and CLKout13 if divide = 1 or 6.5 cycles for CLKout12 and CLKout13 if divide > 1, at time C. Due to the asynchronous nature of SYNC with respect to the output clocks, it is possible that a runt pulse could be created when the clock output goes low from the SYNC event. This is shown by CLKout12 and CLKout13. See Section 9.4.6.1.2 for more information on synchronizing relative to an output clock to eliminate or minimize this runt pulse for CLKout12 or CLKout13.

After SYNC becomes unasserted the event will be registered on the following rising edge of the distribution path clock, time D. CLKout0 to CLKout11 will rise at time E, if Case 2, coincident with a rising distribution clock edge that occurs after 5 cycles for CLKout0 to CLKout11 and for CLKout12 to CLKout13, if CLKout12_13_DIV = 1. If CLKoutX_Y_OFFSET_PD = 0, CLKout0 to CLKout11 will rise at time G after an additional 5 cycles. If CLKout12_13_DIV > 1 then the rising edge of CLKout12 and CLKout13 will occur after 6 cycles of the distribution path at time F plus as many more cycles as programmed by the digital delay for that clock output path. CLKout12 and CLKout13 will rise at time G, which is the Digital Delay value plus 5 cycles when CLKout12_13_DIV = 1 or 6 cycles when CLKout12_13_DIV > 1.

See Figure 9-2 for further SYNC timing detail using different digital delays.

Copyright © 2021 Texas Instruments Incorporated



Case A: CLKout0_3_DIV = 2, CLKout0_3_OFFSET_PD = 1
Case B: CLKout0_3_DIV = 2, CLKout0_3_OFFSET_PD = 0
Case 1: CLKout12_13_DIV = 2, CLKout12_13_DDLY = 5, CLKout12_13_HS = 1
Case 2: CLKout12_13_DIV = 2, CLKout12_13_DDLY = 7, CLKout12_13_HS = 0
Case 3: CLKout12_13_DIV = 2, CLKout12_13_DDLY = 8, CLKout12_13_HS = 0
SYNC1_QUAL = 0 (No qualification), CLKout12_ADLY_SEL & CLKout13_ADLY_SEL = 0

Figure 9-2. Clock Output Synchronization Using the SYNC Pin (SYNC is Active Low, SYNC_POL_INV = 1)

Figure 9-2 illustrates the timing with various digital delays programmed.

- Time A) SYNC assertion event is registered.
- Time B) SYNC unassertion registered.
- Time C) CLKout12 outputs toggle and remain low. A runt pulse can occur at this time as shown.
- Time D) After 5 cycles, in Case A, CLKout0 rises.
- Time E) After 6 + 4.5 = 10.5 cycles, in Case 1, CLKout12 rises.
- Time F) After 5 + 5 = 10 cycles, in Case B, CLKout0 rises.
- Time G) After 6 + 7 = 13 cycles, in Case 2, CLKout12 rises.
- Time H) After 6 + 8 = 14 cycles, in Case 3, CLKout12 rises.
- Note: CLKout 12 and CLKout 13 are driven by the same divider and delay circuit, therefore, their timing is always the same except when analog delay is used.

9.4.6.1 Dynamically Programming Digital Delay

To use dynamic digital delay **synchronization qualification** set SYNC1_QUAL = 3. This causes the SYNC pulse to be qualified by a clock output so that the SYNC event occurs after a specified time from a clock output transition. This allows the relative adjustment of clock output phase in real-time with no or minimum interruption of clock outputs. Hence the term dynamic digital delay.

Note that changing the phase of a clock output requires momentarily altering in the rate of change of the clock output phase and therefore by definition results in a frequency distortion of the signal.

Without qualifying the SYNC with an output clock, the newly synchronized clocks would have a random and unknown digital delay (or phase) with respect to clock outputs not currently being synchronized. Only CLKout12 can be used as a qualifying clock.

Copyright © 2021 Texas Instruments Incorporated

Relative Dynamic Digital Delay

When the qualifying clock digital delay is being adjusted, because the qualifying clock and the adjusted clock are the same, then a **relative dynamic digital delay** adjust is performed. Clocks with NO_SYNC_CLKoutX_Y = 1 are defined as clocks not being adjusted. These clocks operate without interruption.

SYNC and Minimum Step Size

The minimum step size adjustment for digital delay is half a clock distribution path cycle. This is achieved by using the CLKout12_13_HS bit. The CLKout12_13_HS bit change effect is immediate without the need for SYNC. To shift digital delay using CLKout12_13_DDLY, a SYNC signal must be generated for the change to take effect.

Programming Overview

To dynamically adjust the digital delay with respect to an existing clock output the device should be programmed as follows:

- Set SYNC1_QUAL = 3 for clock output qualification.
- Set NO_SYNC_CLKout12_13 = 0 to enable synchronization on CLKout12 and CLKout13.
- Set CLKout12_ADLY_SEL = 0.
- Set NO_SYNC_CLKoutX_Y = 1 for the output clocks, except CLKout12 and CLKout13, that will continue to operate during the SYNC event. There is no interruption of output on these clocks.
- The SYNC_EN_AUTO bit may be set to cause a SYNC event to begin when register R4 is programmed. The auto SYNC feature is a convenience since it does not require the application to manually assert SYNC by toggling the SYNC_POL_INV bit or the SYNC pin when changing digital delay.

Internal Dynamic Digital Delay Timing

Once SYNC is qualified by an output clock, 1.5 cycles later an internal one shot pulse will occur. The width of the one shot pulse is 3 cycles. This internal one shot pulse will cause the outputs to turn off and then back on with a fixed delay with respect to the falling edge of the qualification clock. This allows for dynamic adjustments of digital delay with respect to an output clock.

The qualified SYNC timing is shown in Figure 9-3 for relative dynamic digital delay.

Dynamic Digital Delay Conditions

To perform a dynamic digital delay adjustment, the analog delay must be bypassed by setting CLKout12_ADLY_SEL to 0. If the analog delay is not bypassed the output synchronization may be inaccurate due to unknown analog delay settings.

When adjusting digital delay dynamically, the falling edge of the qualifying clock must coincide with the falling edge of the clock distribution path. For this requirement to be met, program the CLKout12_13_HS value of the qualifying clock group according to Table 9-5.

Table 9-5. Half-Step Programming Requirement of Qualifying Clock During SYNC Event

CLKout12_13_DIV VALUE	CLKout12_13_HS
Odd	Must = 1 during SYNC event.
Even	Must = 0 during SYNC event.

9.4.6.1.1 Relative Dynamic Digital Delay

Relative dynamic digital delay can be used to program a clock output to a specific phase offset from another clock output.

Pros:

- Direct phase adjustment with respect to same clock output.
- Possible glitch pulses from clock output will always be the same during digital delay adjustment transient.

Cons:

- For some clock divide values there may be a glitch pulse due to SYNC assertion.
- Adjustments of digital delay requiring the half step bit (CLKout12_13_HS) for finer digital delay adjust is complicated due to the half step requirement in Table 9-5 above.

9.4.6.1.2 Relative Dynamic Digital Delay - Example

To illustrate the relative dynamic digital delay adjust procedure, consider the following example.

System Requirements:

- CLKin1 Frequency = 983.04 MHz
- CLKout8 = 983.04 MHz (CLKout8_11_DIV = 1)
- CLKout12 = 491.52 MHz (CLKout12_13_DIV = 2)
- During initial programming:
  - CLKout12_13_DDLY = 5
  - CLKout12_13_HS = 0
  - NO_SYNC_CLKoutX_Y = 0

The application requires the 491.52 MHz clock to be stepped in 90 degree steps (~508.6 ps), which is the minimum step resolution allowable by the clock distribution path. That is 1 / 983.04 MHz / 2 = ~169.5 ps. During the stepping of the 491.52 MHz clocks the 983.04 MHz clock must not be interrupted.

Step 1: The device is programmed from register R0 to R5 with values that result in the device operating as desired, see the system requirements above. The phase of all the output clocks are aligned because all the digital delay and half step values were the same when the SYNC was generated by programming register R5. The timing of this is as shown in Figure 9-1.

Step 2: Now the registers will be programmed to prepare for changing digital delay (or phase) dynamically.

REGISTER	PURPOSE
SYNC1_QUAL = 3	Use clock output for qualifying the SYNC pulse for dynamically adjusting digital delay.
NO_SYNC_CLKout7_11 = 1	Clock output 8 (983.04 MHz) won't be affected by SYNC. It will operate without interruption.
SYNC1_AUTO = 0 (default)	Automatically generation of SYNC is not allowed because of the half step requirement. SYNC must be generated manually by toggling the SYNC_POL_INV bit or the SYNC pin.

After the above registers have been programmed, the application may now dynamically adjust the digital delay of the 491.52 MHz clocks.

Step 3: Adjust digital delay of CLKout12 by one step.

Refer to Table 9-6 for the programming sequence to step one half clock distribution period forward or backwards.

Table 9-6. Programming Sequence for One-Step Adjust

STEP DIRECTION AND CURRENT HS STATE	PROGRAMMING SEQUENCE
Adjust clock output one step forward. CLKout12_13_HS = 0.	1. CLKout12_13_HS = 1.

Copyright © 2021 Texas Instruments Incorporated

Table 9-6. Programming Sequence for One-Step Adjust (continued)

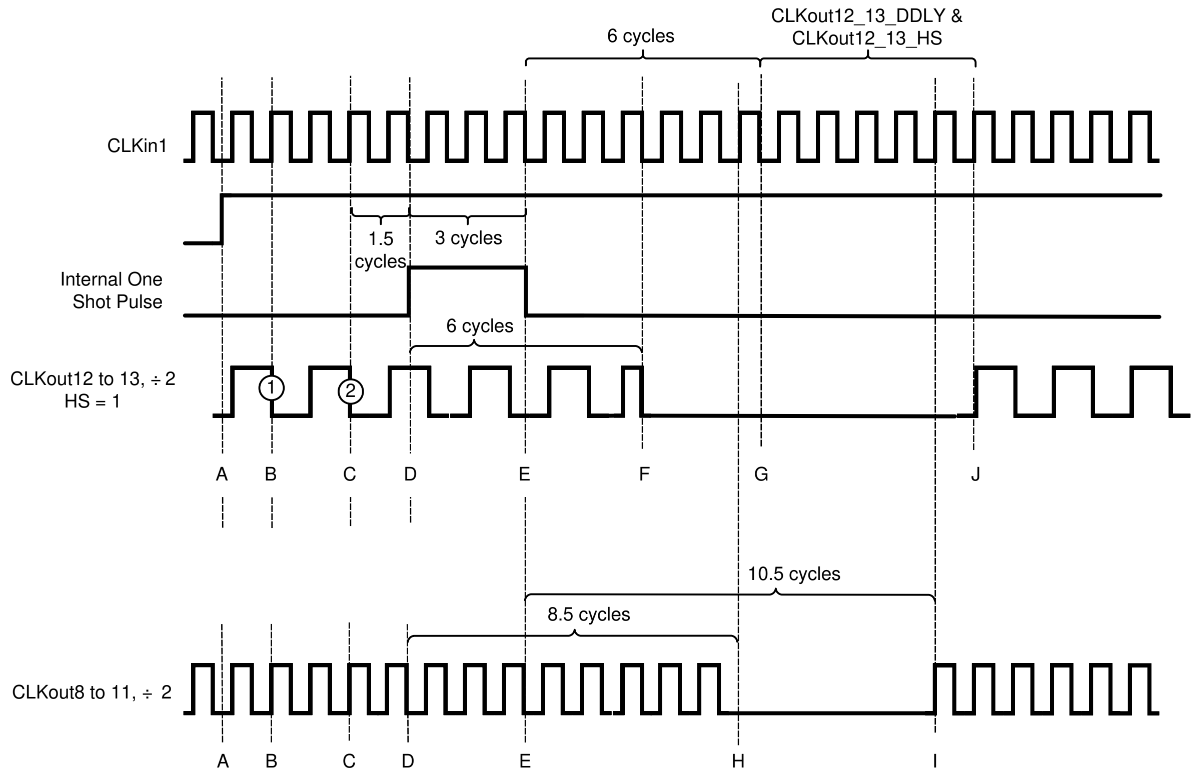
STEP DIRECTION AND CURRENT HS STATE	PROGRAMMING SEQUENCE
Adjust clock output one step forward. CLKout12_13_HS = 1.	1. CLKout12_13_DDLY = 9. 2. Perform SYNC event. 3. CLKout12_13_HS = 0.
Adjust clock output one step backward. CLKout12_13_HS = 0.	1. CLKout12_13_HS = 1. 2. CLKout12_13_DDLY = 5. 3. Perform SYNC event.
Adjust clock output one step backward. CLKout12_13_HS = 1.	1. CLKout12_13_HS = 0.

To fulfill the qualifying clock output half step requirement in Table 9-5 when dynamically adjusting digital delay, the CLKout12_13_HS bit must be set if CLKout12 or CLKout13 has an odd divide. So before any dynamic digital delay adjustment, CLKout12_13_HS must be set because the clock divide value is odd. To achieve the final required digital delay adjustment, the CLKout12_13_HS bit may cleared after SYNC.

If a SYNC is to be generated this can be done by toggling the SYNC pin or by toggling the SYNC_POL_INV bit. Because of the internal one shot pulse, no strict timing of the SYNC pin or SYNC_POL_INV bit is required. After the SYNC event, the clock output will be at the specified phase. See Figure 9-3 for a detailed view of the timing diagram. The timing diagram critical points are:

- Time A) SYNC assertion event is registered.
- Time B) First qualifying falling clock output edge.
- Time C) Second qualifying falling clock output edge.
- Time D) Internal one shot pulse begins. 5.5 cycles later CLKout12 outputs will be forced low while 8.5 cycles later CLKout8 outputs will be forced low.
- Time E) Internal one shot pulse ends. 6 cycles + digital delay cycles later CLKout12 or CLKout13 outputs rise. 10 cycles later CLKout8 to CLKout11 outputs rise.
- Time F) CLKout12 to CLKout13 outputs are forced low.
- Time G) Beginning of digital delay cycles.
- Time H) CLKout8 to CLKout11 outputs are forced low.
- Time I) CLKout8 to CLKout11 outputs rise now.
- Time j) For CLKout12_13_DDLY = 5; the CLKout12 and CLKout13 outputs rise now.

Copyright © 2021 Texas Instruments Incorporated



(SYNC1_QUAL = 1, Qualify with clock output) Starting condition is after half step is removed (CLKout12_13_HS = 0).

Figure 9-3. Relative Dynamic Digital Delay Programming Example, 2nd Adjust

9.5 Programming

LMK01801 devices are programmed using 32-bit registers. Each register consists of a 4-bit address field and 23-bit data field. The address field is formed by bits 0 through 3 (LSBs) and the data field is formed by bits 4 through 31 (MSBs). The contents of each register is clocked in MSB first (bit 31), and the LSB (bit 0) last. During programming, the LE signal should be held LOW. The serial data is clocked in on the rising edge of the CLK signal. After the LSB (bit 0) is clocked in the LE signal should be toggled LOW-to-HIGH-to-LOW to latch the contents into the register selected in the address field. It is recommended to program registers in numeric order, for example R0 to R5 and R15 to achieve proper device operation. Figure 7-1 illustrates the serial data timing sequence.

9.5.1 Recommended Programming Sequence

Registers are programmed in numeric order with R0 being the first and R15 being the last register programmed. The recommended programming sequence involves programming R0 with the reset bit (b4) set to 1 to ensure the device is in a default state. Then R0 is programmed again, the reset bit is be cleared to 0 during the re-programming of R0.

9.5.1.1 Overview

- R0 (Init):
  - Program R0 with RESET = 1. This ensures that the device is configured with default settings. When RESET =1, all other R0 bits are ignored.
- R0: Powerdown Controls and CLKin Dividers
  - Program R0 with RESET = 0
- R1 and R2: Clock output types
- R3: SYNC Features and Analog Delay for CLKout12 and CLKout13
- R4: Dynamic Digital Delay for CLKout12 and CLKout13
- R5: CLKout Dividers and Analog Delay Select
- R15: uWireLock

Copyright © 2021 Texas Instruments Incorporated

9.6 Register Map

Table 9-7 provides the register map for device programming:

Table 9-7. Register Map

REGISTER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data [31:4]																												Address [3:0]			
R0	0	1	0	0	1	0	0	0	CLKin1_MUX		CLKin1_DIV			CLKin0_MUX		CLKin0_DIV			1	1	CLKin1_BUF_TYPE	CLKin0_BUF_TYPE	CLKout12_13_PD	CLKout8_11_PD	CLKout4_7_PD	CLKout0_3_PD	POWERDOWN	RESET	0	0	0	0
R1	CLKout7_TYPE				CLKout6_TYPE				CLKout5_TYPE				CLKout4_TYPE				CLKout3_TYPE			CLKout2_TYPE			CLKout1_TYPE			CLKout0_TYPE			0	0	0	1
R2	0	0	0	0	CLKout13_TYPE				CLKout12_TYPE				CLKout11_TYPE				CLKout10_TYPE				CLKout9_TYPE				CLKout8_TYPE				0	0	1	0
R3	0	0	0	1	0	SYNC1_AUTO	SYNC0_AUTO	SYNC1_FAST	SYNC0_FAST	CLKout8_11_OFFSET_PD	CLKout4_7_OFFSET_PD	CLKout0_3_OFFSET_PD	NO_SYNC_CLKout12_13	NO_SYNC_CLKout8_11	NO_SYNC_CLKout4_7	NO_SYNC_CLKout0_3	SYNC1_POL_INV	SYNC0_POL_INV	0	SYNC1_QUAL		CLKout12_13_HS	CLKout12_13_ADLY						0	0	1	1
R4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout12_13_DDLY										0	1	0	0
R5	0	0	0	0	CLKout12_13_DIV											0	0	CLKout13_ADLY_SEL	CLKout12_ADLY_SEL	CLKout8_11_DIV			CLKout4_7_DIV			CLKout0_3_DIV			0	1	0	1
R15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	uWireLock	1	1	1	1

Copyright © 2021 Texas Instruments Incorporated

9.6.1 Default Device Register Settings After Power On/Reset

The Default Device Register Settings after Power On/Reset Table below illustrates the default register settings programmed in silicon for the LMK018xx after power on or asserting the reset bit. Capital X and Y represent numeric values.

Table 9-8. Default Device Register Settings After Power On/Reset

FIELD NAME	DEFAULT VALUE (DECIMAL)	DEFAULT STATE	FIELD DESCRIPTION	REGISTER	BIT LOCATION (MSB:LSB)
RESET	0	Not in reset	Performs power on reset for device	R0	4
POWERDOWN	0	Disabled (device is active)	Device power down control	R0	5
CLKout0_3_PD	0	Disabled	Power down the divider and clock outputs 0 through 3	R0	6
CLKout4_7_PD	0	Disabled	Power down the divider and clock outputs 4 through 7	R0	7
CLKout8_11_PD	0	Disabled	Power down the divider and clock outputs 8 through 11	R0	8
CLKout12_13_PD	0	Disabled	Power down the divider and clock outputs 12 through 13	R0	9
CLKin0_BUF_TYPE	0	Bipolar	Clock in buffer type	R0	10
CLKin1_BUF_TYPE	0	Bipolar	Clock in buffer type	R0	11
CLKin0_DIV	2	Divide by 2	Divider value for CLKin0	R0	14:16 [3]
CLKin0_MUX	0	Bypass	Enables or bypasses the CLKin0 divider	R0	17:18 [2]
CLKin1_DIV	2	Divide by 2	Divider value for CLKin1	R0	19:21 [3]
CLKin1_MUX	0	Bypass	Enables or bypasses the CLKin1 divider	R0	22:23 [2]
CLKout0_TYPE	1	LVDS	Individual clock output format. Select from LVDS/LVPECL.	R1	4:6 [3]
CLKout1_TYPE	1	LVDS		R1	7:9 [3]
CLKout2_TYPE	1	LVDS		R1	10:12 [3]
CLKout3_TYPE	1	LVDS		R1	13:15 [3]
CLKout4_TYPE	1	LVDS	Individual clock output format. Select from LVDS/LVPECL/LVCMOS.	R1	16:19 [4]
CLKout5_TYPE	1	LVDS		R1	20:23 [4]
CLKout6_TYPE	1	LVDS		R1	24:27 [4]
CLKout7_TYPE	1	LVDS		R1	28:31 [4]
CLKout8_TYPE	1	LVDS		R2	4:7 [4]
CLKout9_TYPE	1	LVDS		R2	8:11 [4]
CLKout10_TYPE	1	LVDS		R2	12:15 [4]
CLKout11_TYPE	1	LVDS		R2	16:19 [4]
CLKout12_TYPE	1	LVDS		R2	20:23 [4]
CLKout13_TYPE	1	LVDS		R2	24:27 [4]
CLKout12_13_ADLY	0	No delay	Analog delay setting for CLKout12 & CLKout13.	R3	4:9 [6]
CLKout12_13_HS	0	No Shift	Half shift for digital delay.	R3	10
SYNC1_QUAL	0	Not Qualified	Allows SYNC operations to be qualified by a clock output	R3	11:12 [2]
SYNC0_POL_INV	1	Logic Low	Sets the polarity of the SYNC pin when input	R3	14
SYNC1_POL_INV	1	Logic Low		R3	15
NO_SYNC_CLKout0_3	0	Will sync	Disable individual clock groups from being synchronized.	R3	16
NO_SYNC_CLKout4_7	0	Will sync		R3	17
NO_SYNC_CLKout8_11	0	Will sync		R3	18
NO_SYNC_CLKout12_13	0	Will sync		R3	19

Copyright © 2021 Texas Instruments Incorporated

Table 9-8. Default Device Register Settings After Power On/Reset (continued)

FIELD NAME	DEFAULT VALUE (DECIMAL)	DEFAULT STATE	FIELD DESCRIPTION	REGISTER	BIT LOCATION (MSB:LSB)
CLKout0_3_OFFSET_PD	1	Disabled	Enables a fixed 5-cycle digital delay offset.	R3	20
CLKout4_7_OFFSET_PD	1	Disabled		R3	21
CLKout8_11_OFFSET_PD	0	5 clock cycles		R3	22
SYNC0_FAST	0	Disabled	Enables synchronization circuitry.	R3	23
SYNC1_FAST	0	Disabled		R3	24
SYNC0_AUTO	1	Automatic	SYNC is started by programming a Register R5	R3	25
SYNC1_AUTO	1	Automatic	SYNC is started by programming a Register R4 or R5	R3	26
CLKout12_13_DDLY	5	5 clock cycles	Digital Delay setting for CLKout12 & CLKout13.	R4	4:13 [10]
CLKout0_3_DIV	1	Divide-by-1	Divider for clock outputs.	R5	4:6 [3]
CLKout4_7_DIV	1	Divide-by-1		R5	7:9 [3]
CLKout8_11_DIV	1	Divide-by-1		R5	10:12 [3]
CLKout12_ADLY_SEL	0	No Delay	Enable Digital Delay for CLKout12	R5	13
CLKout13_ADLY_SEL	0	No Delay	Enable Digital Delay for CLKout13	R5	14
CLKout12_13_DIV	1	Divide-by-1	Divider for clock output.	R5	17:27 [11]
uWireLock	0	Writeable	The values of registers R0 to R5 are lockable	R15	4

9.6.2 Register R0

The R0 register controls reset, global power down, the power down functions for the channel dividers and their corresponding outputs, CLKinX divider value and CLKinX divide select. The X, Y in CLKoutX_Y_PD denote the actually clock output which may be from 0 to 13 where X is the first CLKout and Y is the last CLKout.

9.6.2.1 RESET

Setting this bit will cause the silicon default values to be set upon loading of R0 by a high LEuWire pin. When programming register R0 with the RESET bit set, all other programmed values are ignored.

The RESET bit is automatically cleared upon writing any other register. For instance, when R0 is written to again with default values.

If the user reprograms the R0, after the initial programming then set RESET = 0.

Table 9-9. RESET

R0[4]	STATE
0	Normal operation
1	Reset (automatically cleared)

9.6.2.2 POWERDOWN

Setting this bit causes the device to enter powerdown mode. Normal operation is resumed by clearing this bit with MICROWIRE. All other MICROWIRE settings are preserved during POWERDOWN.

Table 9-10. POWERDOWN

R1[5]	State
0	Normal operation
1	Powerdown

Copyright © 2021 Texas Instruments Incorporated

9.6.2.3 CLKoutX_Y_PD

This bit powers down the clock outputs as specified by CLKoutX to CLKoutY. This includes the divider and output buffers.

Table 9-11. CLKoutX_Y_PD Programming Addresses

CLKoutX_Y_PD	Programming Address
CLKout0_3_PD	R0[6]
CLKout4_7_PD	R0[7]
CLKout8_11_PD	R0[8]
CLKout12_13_PD	R0[9]

Table 9-12. CLKoutX_Y_PD

R0[6,7,8,9]	State
0	Power up clock group
1	Power down clock group

9.6.2.3.1 CLKinX_BUF_TYPE

There are two input buffer types for CLKin0 and CLKin1: bipolar or CMOS. Bipolar is recommended for differential inputs such as LVDS and LVPECL. CMOS is recommended for DC coupled single ended inputs.

When using bipolar, CLKinX and CLKinX* input pins must be AC coupled when using differential or single ended input.

When using CMOS, CLKinX and CLKinX* input pins may be AC or DC coupled with a differential input.

When using CMOS in a single ended mode, the used clock input pin (CLKinX or CLKinX*) may be AC or DC coupled to the signal source. The unused CLKin shouLd be AC coupled to ground.

The programming address table shows at what register the specified CLKinX_BUF_TYPE is located.

The CLKinX_BUF_TYPE table shows the programming definition for these registers.

Table 9-13. CLKinX_BUF_TYPE Programming Addresses

CLKinX_BUF_TYPE	Programming Address
CLKin0_BUF_TYPE	R0[10]
CLKin1_BUF_TYPE	R0[11]

Table 9-14. CLKinX_BUF_TYPE

R0[10]	CLKinX Buffer Type
0	Bipolar
1	CMOS

9.6.2.3.2 CLKinX_DIV

These set the CLKin divide value, from 2-8.

Table 9-15. CLKinX_DIV Programming Address

CLKinX_DIV	Programming Address
CLKin0_DIV	R0[16:14]
CLKin1_DIV	R0[21:19]

Table 9-16. CLKinX_DIV

R0[21:19, 16:14]	Divide Value
0 (0x00)	8
1 (0x01)	1
2 (0x02)	2

Copyright © 2021 Texas Instruments Incorporated

Table 9-16. CLKinX_DIV (continued)

R0[21:19, 16:14]	Divide Value
3 (0x03)	3
4 (0x04)	4
5 (0x05)	5
6 (0x06)	6
7 (0x07)	7

9.6.2.3.3 CLKinX_MUX

These bits select whether or not the CLKin divider is bypassed or enabled.

Table 9-17. CLKinX_MUX Programming Address

CLKinX_MUX	Programming Address
CLKin0_MUX	R0[18:17]
CLKin1_MUX	R0[23:22]

Table 9-18. CLKinX_MUX

R0[23:22, 18:17]	State
0 (0x00)	Bypass
1(0x01)	Divide

9.6.3 Register R1 and R2

Registers R1 and R2 set the clock output types.

9.6.3.1 CLKoutX_TYPE

The clock output types of the LMK01801 are individually programmable. The CLKoutX_TYPE registers set the output type of an individual clock output to LVDS, LVPECL, LVCMOS, or powers down the output buffer. Note that LVPECL supports three different amplitude levels and LVCMOS supports single LVCMOS outputs, inverted, and normal polarity of each output pin for maximum flexibility.

The programming addresses table shows at what register and address the specified clock output CLKoutX_TYPE register is located.

The CLKoutX_TYPE table shows the programming definition for these registers.

Copyright © 2021 Texas Instruments Incorporated

Table 9-19. CLKoutX_TYPE Programming Addresses

CLKoutX	Programming Address
CLKout0	R1[4:6]
CLKout1	R1[7:9]
CLKout2	R1[10:12]
CLKout3	R1[13:15]
CLKout4	R1[16:19]
CLKout5	R1[20:23]
CLKout6	R1[24:27]
CLKout7	R1[28:31]
CLKout8	R2[4:7]
CLKout9	R2[8:11]
CLKout10	R2[12:15]
CLKout11	R2[16:19]
CLKout12	R2[20:23]
CLKout13	R2[24:27]

Table 9-20. CLKoutX_TYPE, 4 Bits

R1[31:28,27:24,23:20,19:16], R2[27:24,23:20,19:16,15:12,11:8,7:4]	Definition
0 (0x00)	Powerdown
1 (0x01)	LVDS
2 (0x02)	LCPECL
3 (0x03)	Reserved
4 (0x04)	LVPECL (1600 mVpp)
5 (0x05)	LVPECL (2000 mVpp)
6 (0x06)	LVCMOS (Norm/Inv)
7 (0x07)	LVCMOS (Inv/Norm)
8 (0x08)	LVCMOS (Norm/Norm)
9 (0x09)	LVCMOS (Inv/Inv)
10 (0x0A)	LVCMOS (Off/Norm)
11 (0x0A)	LVCMOS (Off/Inv)
12 (0x0C)	LVCMOS (Norm/Off)
13 (0x0D)	LVCMOS (Inv/Off)
14 (0x0E)	LVCMOS (Off/Off)

Copyright © 2021 Texas Instruments Incorporated

9.6.4 Register R3

Register R3 sets the analog delay, digital delay half-shift and SYNC controls.

9.6.4.1 CLKout12_13_ADLY

This registers controls the analog delay of the clock outputs 12 and 13. Adding analog delay to the output will increase the noise floor of the output. For this analog delay to be active for a clock output, it must be selected with ADLY12_SEL or ADLY13_SEL. If neither clock output selects the analog delay, then the analog delay block is powered down.

In addition to the programmed delay, a fixed 500 ps of delay will be added by engaging the delay block.

The CLKout12_13_ADLY table shows the programming definition for these registers.

Table 9-21. CLKout12_13_ADLY, 6 Bits

R3[4:9]	Definition
0 (0x00)	500 ps + No delay
1 (0x01)	500 ps + 25 ps
2 (0x02)	500 ps + 50 ps
3 (0x03)	500 ps + 75 ps
4 (0x04)	500 ps + 100 ps
5 (0x05)	500 ps + 125 ps
6 (0x06)	500 ps + 150 ps
7 (0x07)	500 ps + 175 ps
8 (0x08)	500 ps + 200 ps
9 (0x09)	500 ps + 225 ps
10 (0x0A)	500 ps + 250 ps
11 (0x0B)	500 ps + 275 ps
12 (0x0C)	500 ps + 300 ps
13 (0x0D)	500 ps + 325 ps
14 (0x0E)	500 ps + 350 ps
15 (0x0F)	500 ps + 375 ps
16 (0x10)	500 ps + 400 ps
17 (0x11)	500 ps + 425 ps
18 (0x12)	500 ps + 450 ps
19 (0x13)	500 ps + 475 ps
20 (0x14)	500 ps + 500 ps
21 (0x15)	500 ps + 525 ps
22 (0x16)	500 ps + 550 ps
23 (0x17)	500 ps + 575 ps

9.6.4.2 CLKout12_13_HS, Digital Delay Half Shift

This bit subtracts a half clock cycle of the clock distribution path period to the digital delay of CLKout12 and CLKout13. CLKout12_13_HS is used together with CLKout12_13_DDLY to set the digital delay value.

The state of this bit does not affect the power mode of the clock output group.

When changing CLKout12_13_HS, the digital delay immediately takes effect without a SYNC event.

Table 9-22. CLKout12_13_HS

R3[10]	State
0	Normal

Copyright © 2021 Texas Instruments Incorporated

Table 9-22. CLKout12_13_HS (continued)

R3[10]	State
1	Subtract half of a clock distribution path period from the total digital delay

9.6.4.3 SYNC1_QUAL

When SYNC1_QUAL is set clock outputs on Bank B will be synchronized.

CLKout12 will be used as the SYNC qualification clock.

Only CLKout12 and CLKout13 support dynamic digital delay. However, this permits the relative phase relationship between CLKout12 and CLKout13 to be dynamically adjusted with respect to all other clock outputs. When NO_SYNC_CLKoutX_Y = 1, the corresponding clock outputs will not be interrupted during the SYNC event.

Qualifying the SYNC means that the pulse which turns the clock outputs off and on will have a fixed time relationship with the phase of the other clock outputs.

See Section 9.3.9 for more information.

Table 9-23. SYNC1_QUAL

R3[11]	Mode
0 (0x00)	No Qualification
1 (0x01)	Reserved
2 (0x10)	Reserved
3 (0x11)	Qualification Enabled

9.6.4.4 SYNCX_POL_INV

Sets the polarity of a SYNCX input pin. When SYNC is asserted the clock outputs will transition to a low state.

A pull-up on the SYNCX pin results in normal operation when the SYNCX_POL_INV = 1 and the SYNCX input is a no connect.

See Section 9.4.6 for more information on SYNC. A SYNC event can be generated by toggling this bit through the MICROWIRE interface.

Table 9-24. SYNCX_POL_INV

R3[14, 15]	Polarity
0	SYNC is active high
1	SYNC is active low

9.6.4.5 NO_SYNC_CLKoutX_Y

The NO_SYNC_CLKoutX_Y bits prevent individual clock groups from becoming synchronized during a SYNC event. A reason to prevent individual clock groups from becoming synchronized is that during synchronization, the clock output is in a fixed low state or can have a glitch pulse.

By disabling SYNC on a clock group, it will continue to operate normally during a SYNC event.

Digital delay requires a SYNC operation to take effect. If NO_SYNC_CLKout12_13 is set before a SYNC event, the digital delay value will be unused.

Setting the NO_SYNC_CLKoutX_Y bit has no effect on clocks already synchronized together.

Table 9-25. NO_SYNC_CLKoutX_Y Programming Addresses

NO_SYNC_CLKoutX_Y	Programming Address
CLKout0 to CLKout3	R3[16]
CLKout4 to CLKout7	R3[17]

Copyright © 2021 Texas Instruments Incorporated

Table 9-25. NO_SYNC_CLKoutX_Y Programming Addresses (continued)

NO_SYNC_CLKoutX_Y	Programming Address
CLKout8 to CLKout11	R3[18]
CLKout12 to CLKout13	R3[19]

Table 9-26. NO_SYNC_CLKoutX_Y

R3[19, 18, 17, 16]	Definition
0	CLKoutX_Y will synchronize
1	CLKoutX_Y will not synchronize

9.6.4.6 CLKoutX_Y_OFFSET_PD

CLKoutX_Y_OFFSET_PD sets a fixed digital delay of 5 clock distribution path cycles for clock groups 0 to 11.

Setting the bit powers down the offset for the respective clock group, starting the outputs 5 cycles earlier. Clearing the bit enables the offset, inserting the 5-cycle delay. For example, CLKout4_7_OFFSET_PD = 0 adds a 5-cycle delay to outputs 4 to 7 after synchronization.

CLKoutX_Y_OFFSET_PD takes effect upon a SYNC event.

Table 9-27. CLKoutX_Y_OFFSET_PD Programming Addresses

CLKoutX_Y_OFFSET_PD	PROGRAMMING ADDRESS
CLKout0 to CLKout3	R3[20]
CLKout4 to CLKout7	R3[21]
CLKout8 to CLKout11	R3[22]

Table 9-28. CLKoutX_Y_OFFSET_PD

R3[20, 21, 22]	DEFINITION
0	5 cycle delay enabled in CLKoutX_Y
1	5 cycle delay disabled in CLKoutX_Y

9.6.4.7 SYNCX_FAST

SYNC1_FAST must be set to 1 when using SYNC1_QUAL

9.6.4.8 SYNCX_AUTO

When set, causes a SYNC event to occur when programming R4 to adjust digital delay values (this will cause a SYNC event for Bank B only) or R5 when adjusting divide values (this will cause a SYNC event for both Bank A and B).

The SYNC event will coincide with the LE uWire pin falling edge.

Table 9-29. SYNCX_AUTO

R3[26, 25]	Mode
0	Manual SYNC
1	SYNC internally generated

9.6.5 Register R4

9.6.5.1 CLKout12_13_DDLY, Clock Channel Digital Delay

CLKout12_13_DDLY and CLKout12_13_HS sets the digital delay used for CLKout12 and CLKout13. CLKout12_13_DDLY only takes effect during a SYNC event and if the NO_SYNC_CLKout12_13 bit is cleared for this clock group.

Programming CLKout12_13_DDLY can require special attention. See section Section 9.4.6.1 for more details.

Using a CLKout12_13_DDLY value of 13 or greater will cause the clock outputs to operate in extended mode regardless of the clock group's divide value or the half step value.

One clock cycle is equal to the period of the clock distribution path. The period of the clock distribution path is equal to clock divider value divided by the CLKin1 frequency.

$t_{clock\ distribution\ path}$ = CLKout divide value / f_{CLKin}

Copyright © 2021 Texas Instruments Incorporated

Table 9-30. CLKout12_13_DDLY, 10 Bits

R4[13:4]	Delay (Divide = 1)	Delay (Divide >1)	Power Mode
0 (0x00)	5 clock cycles	6 clock cycles	Normal Mode
1 (0x01)	5 clock cycles	6 clock cycles	
2 (0x02)	5 clock cycles	6 clock cycles	
3 (0x03)	5 clock cycles	6 clock cycles	
4 (0x04)	5 clock cycles	6 clock cycles	
5 (0x05)	5 clock cycles	6 clock cycles	
6 (0x06)	6 clock cycles	7 clock cycles	
7 (0x07)	7 clock cycles	8 clock cycles	
...	...	...	
12 (0x0C)	12 clock cycles	13 clock cycles	
13 (0x0D)	13 clock cycles	14 clock cycles	Extended Mode
...	...	...	
520 (0x208)	520 clock cycles	521 clock cycles	
521 (0x209)	521 clock cycles	522 clock cycles	
522 (0x20A)	522 clock cycles	523 clock cycles	

9.6.6 Register R5

Register 5 sets the clock output dividers and analog delay.

9.6.6.1 CLKout12_ADLY_SEL[13], CLKout13_ADLY_SEL[14], Select Analog Delay

These bits individually select the analog delay block for use with CLKout12 or CLKout13. It is not required for both outputs of a clock output group to use analog delay, but if both outputs do select the analog delay block, then the analog delay will be the same for each output. When neither clock output uses analog delay, the analog delay block is powered down.

Table 9-31. CLKout12_ADLY_SEL[13], CLKout13_ADLY_SEL[14]

R5[13]	R5[14]	STATE
0	0	Analog delay powered down
0	1	Analog delay on CLKout13
1	0	Analog delay on CLKout12
1	1	Analog delay on both CLKouts

9.6.6.2 CLKoutX_Y_DIV Clock Output Divide

CLKoutX_Y_DIV sets the divide value for the clock outputs X through Y. The divide may be even or odd. Both even and odd divides output a 50% duty cycle clock.

Programming CLKoutX_Y_DIV is as follows:

Table 9-32. CLKoutX_Y_DIV Programming Addresses

CLKoutX_Y_DIV	Programming Address
CLKout0_3_DIV	R5[6:4]
CLKout4_7_DIV	R5[9:7]
CLKout8_11_DIV	R5[12:10]
CLKout12_13_DIV	R5[27:17]

Table 9-33. CLKoutX_Y_Div, 3 Bits

R5[12:10, 9:7, 6:4]	Divide Value
0 (0x00)	8

Table 9-33. CLKoutX_Y_Div, 3 Bits (continued)

R5[12:10, 9:7, 6:4]	Divide Value
1 (0x01)	1
2 (0x02)	2
3 (0x03)	3
4 (0x04)	4
5 (0x05)	5
6 (0x06)	6
7 (0x07)	7

Table 9-34. CLKout12_13_DIV, 11 Bits

R5[27:17]	Divide Value	Power Mode
0 (0x00)	Invalid	Normal Mode
1 (0x01)	1	
2 (0x02)	2 (1)	
3 (0x03)	3	
4 (0x04)	4 (1)	
5 (0x05)	5 (1)	
6 (0x06)	6	
...	...	
24 (0x18)	24	
25 (0x19)	25	
26 (0x1A)	26	Extended Mode
27 (0x1B)	27	
...	...	
1044 (0x414)	1044	
1045 (0x415)	1045	

(1) After programming CLKout12_13_DIV a SYNC event must occur on the channels using this divide value (CLKout12 and CLKout13), A SYNC event may be generated by changing the SYNC1_POL_INV bit or through the SYNC1 pin. Ensure that CLKin1 is stable before this SYNC event occurs.

Using a divide value of 26 or greater will cause the clock group to operate in extended mode regardless of the clock group's digital delay value.

9.6.7 Register 15

9.6.7.1 uWireLock

Setting uWireLock will prevent any changes to uWire registers R0 to R5. Only by clearing uWireLock bit in R15 can the MICROWIRE registers be unlocked and written to once more.

Table 9-35. uWireLock

R15 [4]	State
0	Registers Unlocked
1	Registers locked, Write-protected

Copyright © 2021 Texas Instruments Incorporated

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Typical Application

10.1.1 Detailed Design Procedure

10.1.1.1 Driving CLKin Inputs

10.1.1.1.1 Driving CLKin Pins With a Differential Source

Both CLKin ports can be driven by differential signals. It is recommended that the input mode be set to bipolar (CLKinX_BUF_TYPE = 0) when using differential reference clocks. The LMK01801 family internally biases the input pins so the differential interface should be AC coupled. The recommended circuits for driving the CLKin pins with either LVDS or LVPECL are shown in Figure 10-1 and Figure 10-2.

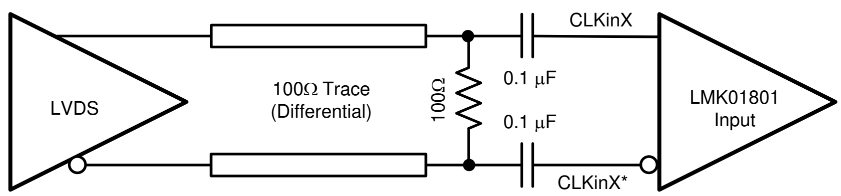


Figure 10-1. CLKinX/X* Termination for an LVDS Reference Clock Source

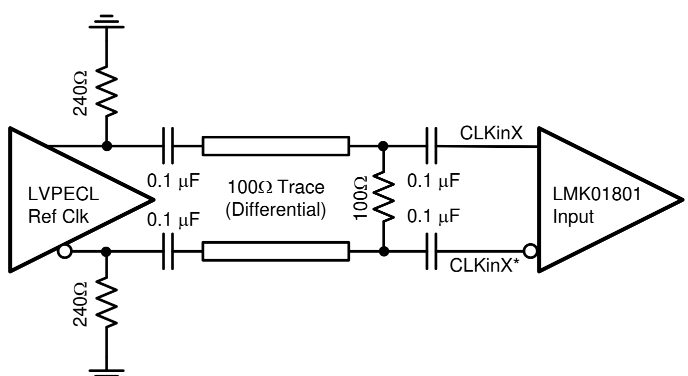


Figure 10-2. CLKinX/X* Termination for an LVPECL Reference Clock Source

Finally, a reference clock source that produces a differential sine wave output can drive the CLKin pins using the circuit shown in Figure 10-3. Note: the signal level must conform to the requirements for the CLKin pins listed in the Section 7.4.

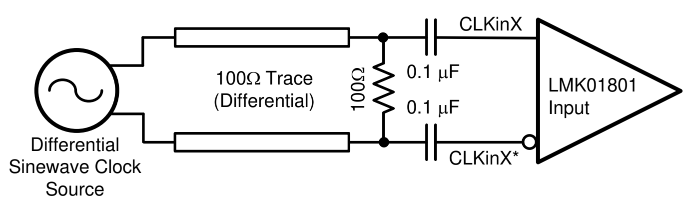


Figure 10-3. CLKinX/X* Single-Ended Termination

10.1.1.1.2 Driving CLKin Pins With a Single-Ended Source

The CLKin pins of the LMK01801 family can be driven using a single-ended reference clock source, for example, either a sine wave source or an LVCMOS/LVTTL source. Either AC coupling or DC coupling may be used. In the case of the sine wave source that is expecting a 50 Ω load, it is recommended that AC coupling be used as shown in Figure 10-4 the circuit below with a 50 Ω termination.

Note

The signal level must conform to the requirements for the CLKin pins listed in the Section 7.4. CLKinX_BUF_TYPE is recommended to be set to bipolar mode (CLKinX_BUF_TYPE = 0).

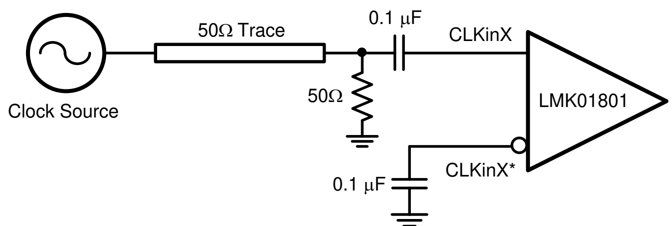


Figure 10-4. DC-Coupled LVCMOS/LVTTL Reference Clock

If the CLKin pins are being driven with a single-ended LVCMOS/ LVTTL source, either DC coupling or AC coupling may be used. If DC coupling is used, see Figure 10-5, the CLKinX_BUF_TYPE should be set to MOS buffer mode (CLKinX_BUF_TYPE = 1) and the voltage swing of the source must meet the specifications for DC coupled, MOS-mode clock inputs given in the table of Electrical Characteristics. If AC coupling is used, the CLKinX_BUF_TYPE should be set to the bipolar buffer mode (CLKinX_BUF_TYPE = 0). The voltage swing at the input pins must meet the specifications for AC coupled, bipolar mode clock inputs given in the table of Electrical Characteristics. In this case, some attenuation of the clock input level may be required. A simple resistive divider circuit before the AC coupling capacitor is sufficient.

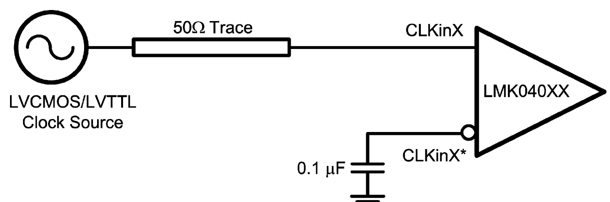


Figure 10-5. DC-Coupled LVCMOS/LVTTL Reference Clock

Copyright © 2021 Texas Instruments Incorporated

10.1.1.2 Termination and Use of Clock Output (Drivers)

When terminating clock drivers keep in mind these guidelines for optimum phase noise and jitter performance:

- Transmission line theory should be followed for good impedance matching to prevent reflections.
- Clock drivers should be presented with the proper loads. For example:
  – LVDS drivers are current drivers and require a closed current loop.
  – LVPECL drivers are open emitters and require a DC path to ground.
- Receivers should be presented with a signal biased to their specified DC bias level (common mode voltage) for proper operation. Some receivers have self-biasing inputs that automatically bias to the proper voltage level. In this case, the signal should normally be AC coupled.

It is possible to drive a non-LVPECL or non-LVDS receiver with an LVDS or LVPECL driver as long as the above guidelines are followed. Check the datasheet of the receiver or input being driven to determine the best termination and coupling method to be sure that the receiver is biased at its optimum DC voltage (common mode voltage).

For example, when driving the OSCin/OSCin* input of the LMK04800 family, OSCin/OSCin* should be AC coupled because OSCin/ OSCin* biases the signal to the proper DC level. This is only slightly different from the AC coupled cases described in Section 10.1.1.1.2 because the DC blocking capacitors are placed between the termination and the OSCin/OSCin* pins, but the concept remains the same. The receiver (OSCin/OSCin*) sets the input to the optimum DC bias voltage (common mode voltage), not the driver.

10.1.1.2.1 Termination for DC-Coupled Differential Operation

For DC coupled operation of an LVDS driver, terminate with 100 Ω as close as possible to the LVDS receiver as shown in Figure 10-6.

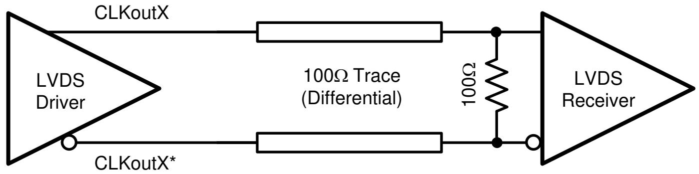


Figure 10-6. Differential LVDS Operation, DC Coupling, No Biasing of the Receiver

For DC coupled operation of an LVPECL driver, terminate with 50 Ω to VCC - 2 V as shown in Figure 10-7. Alternatively terminate with a Thevenin equivalent circuit (120 Ω resistor connected to VCC and an 82 Ω resistor connected to ground with the driver connected to the junction of the 120 Ω and 82 Ω resistors) as shown in Figure 10-8 for VCC = 3.3 V.

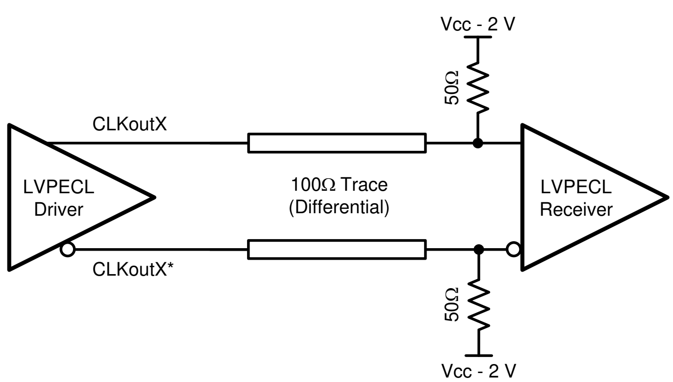


Figure 10-7. Differential LVPECL Operation, DC Coupling

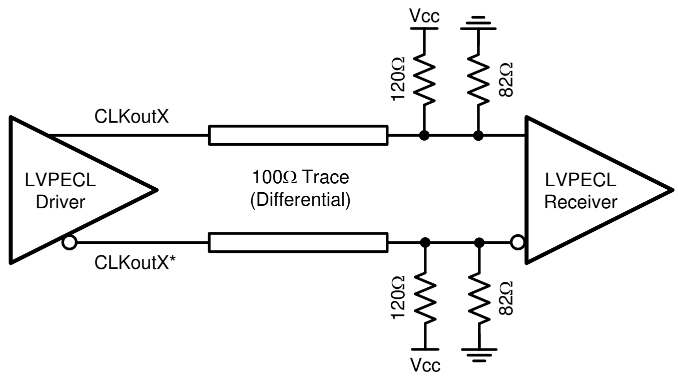


Figure 10-8. Differential LVPECL Operation, DC Coupling, Thevenin Equivalent

10.1.1.2.2 Termination for AC-Coupled Differential Operation

AC coupling allows for shifting the DC bias level (common-mode voltage) when driving different receiver standards. AC coupling prevents the driver from providing a DC bias voltage at the receiver, therefore it is important to ensure the receiver is biased to its ideal DC level.

When driving non-biased LVDS receivers with an LVDS driver, the signal may be AC coupled by adding DC blocking capacitors, however the proper DC bias point needs to be established at the receiver. One way to do this is with the termination circuitry in Figure 10-9.

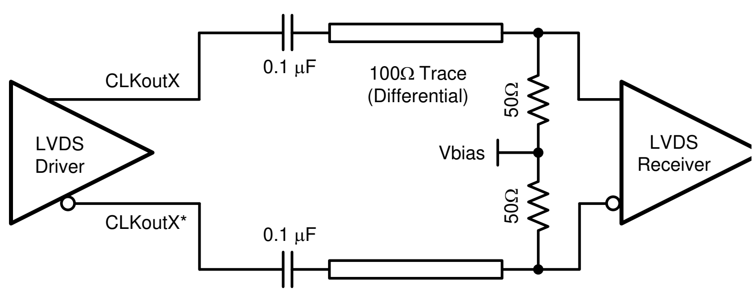


Figure 10-9. Differential LVDS Operation, AC Coupling, External Biasing at the Receiver

Some LVDS receivers may have internal biasing on the inputs. In this case, the circuit shown in is modified by replacing the 50-Ω terminations to Vbias with a single 100-Ω resistor across the input pins of the receiver, as shown in Figure 10-10. When using AC coupling with LVDS outputs, there may be a start-up delay observed in the clock output due to capacitor charging. The previous figures employ a 0.1-µF capacitor. This value may need to be adjusted to meet the start-up requirements for a particular application.

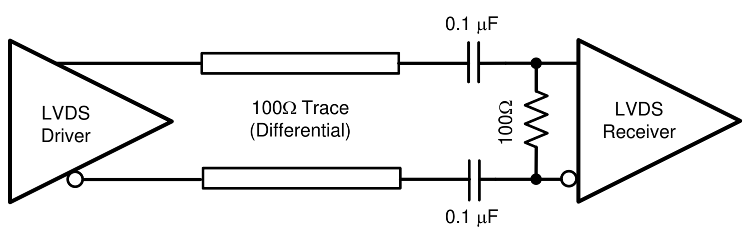


Figure 10-10. LVDS Termination for a Self-Biased Receiver

LVPECL drivers require a DC path to ground. When AC coupling an LVPECL signal use 120-Ω to 240-Ω emitter resistors close to the LVPECL driver to provide a DC path to ground as shown in Figure 10-11. For proper receiver operation, the signal should be biased to the DC bias level (common-mode voltage) specified by the receiver. The typical DC bias voltage for LVPECL receivers is 2 V.

A typical application is shown in Figure 10-11, where R_{em} = 120 Ω to 240 Ω. Refer to the receiver input recommendations to determine if the proper value of C_A's, if needed.

Copyright © 2021 Texas Instruments Incorporated

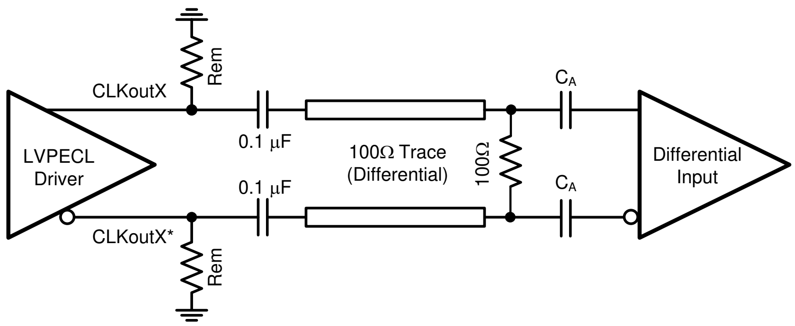


Figure 10-11. Differential LVPECL Operation, AC Coupling, External Biasing at the Receiver, R_{em} = 120 Ω to 240 Ω

10.1.1.2.3 Termination for Single-Ended Operation

A balun can be used with either LVDS or LVPECL drivers to convert the balanced, differential signal into an unbalanced, single-ended signal.

It is possible to use an LVPECL driver as one or two separate 800 mVpp signals. When using only one LVPECL driver of a CLKoutX/CLKoutX* pair, be sure to properly terminated the unused driver. When DC coupling one of the LMK04800 family clock LVPECL drivers, the termination should be 50 Ω to VCC - 2 V as shown in Figure 10-12. The Thevenin equivalent circuit is also a valid termination as shown in Figure 10-13 for Vcc = 3.3 V.

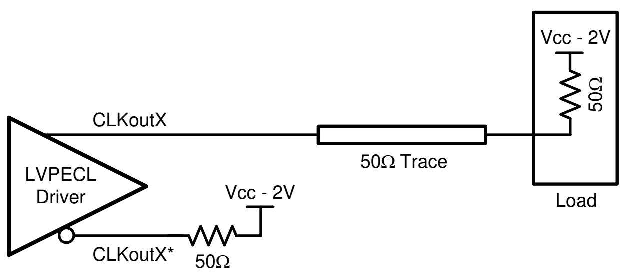


Figure 10-12. Single-Ended LVPECL Operation, DC Coupling

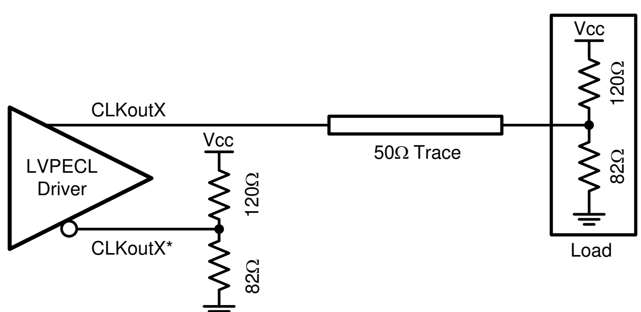


Figure 10-13. Single-Ended LVPECL Operation, DC Coupling, Thevenin Equivalent

When AC coupling an LVPECL driver use a 120 Ω to 240 Ω emitter resistor to provide a DC path to ground and ensure a 50 Ω termination with the proper DC bias level for the receiver. The typical DC bias voltage for LVPECL receivers is 2 V (See Section 10.1.1.2.2). If the companion driver is not used it should be terminated with either a proper AC or DC termination. This latter example of AC coupling a single-ended LVPECL signal can be used to measure single-ended LVPECL performance using a spectrum analyzer or phase noise analyzer. When using most RF test equipment no DC bias point (0 VDC) is required for safe and proper operation. The internal 50 Ω termination of the test equipment correctly terminates the LVPECL driver being measured as shown in Figure 10-14.

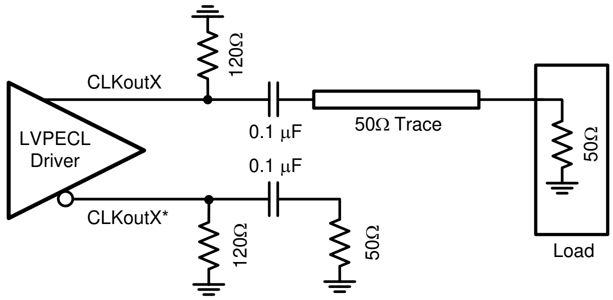


Figure 10-14. Single-Ended LVPECL Operation, AC Coupling R_{em}=120 Ω to 240 Ω

Copyright © 2021 Texas Instruments Incorporated

11 Power Supply Recommendations

11.1 Current Consumption

Note

Assuming θ_{JA} = 25.8°C/W, the total power dissipated on chip must be less than (125°C - 85°C) / 25.8°C/W = 1.5 W to ensure a junction temperature less than 145°C.

Worst case power dissipation can be estimated by multiplying typical power dissipation with a factor of 1.20.

From Table 11-1 the current consumption can be calculated for any configuration.

For example, the current for the entire device with 1 LVDS (CLKout0) and 1 LVPECL 1600 mVpp /w 240 Ω emitter resistors (CLKout1) output active with a clock output divide = 1, and no other features enabled can be calculated by adding the following blocks:

- Core Current
- Clock Buffer
- One LVDS Output Buffer Current
- Bank A
- Output Divider Buffer Current
- LVPECL 1600 mVpp buffer /w 240 Ω emitter resistors

Since there will be one LVPECL output drawing emitter current, this means some of the power from the current draw of the device is dissipated in the external emitter resistors which doesn't add to the power dissipation budget for the device but is important for LDO I_{CC} calculations.

For total current consumption of the device add up the significant functional blocks. In this example 92 mA =

- 1 mA (core current)
- 22 mA (Bank A current)
- 15 mA (Output Buffer current)
- 21 mA (Output Divider current)
- 9 mA (LVDS output current)
- 24 mA (LVPECL 1600 mVpp buffer /w 240 Ω emitter resistors)

Once the total current consumption has been calculated, power dissipated by the device can be calculated. The power dissipation of the device is equal to the total current entering the device multiplied by the voltage at the device minus the power dissipated in any emitter resistors connected to any of the LVPECL outputs. If no emitter resistors are connected to the LVPECL outputs, this power will be 0 watts. Continuing the output with 240 Ω emitter resistors. Total IC power = 275.1 mW = 3.3 V * 95 mA -28.5 mW.

Copyright © 2021 Texas Instruments Incorporated

Table 11-1. Typical Current Consumption for Selected Functional Blocks (T_A = 25°C, V_{CC} = 3.3 V)

Block	Condition		Typical I_{CC} (mA)	Power dissipated in device (mW)	Power dissipated externally (mW) (1)
Core					
Core	All outputs and dividers off		1	3.3	-
Bank	Bank A	At least on output enabled	22	72.6	-
	Bank B	At least on output enabled	25	82.5	-
Buffers	CLKout0 to CLKout3	On when any on output in the group is enabled	15	49.5	-
	CLKout4 to CLKout7				-
	CLKout8 to CLKout11				-
	CLKout12 to CLKout13				-
Output Divider	CLKout0 to CLKout11	Divide = 1	21	69.3	-
		Divide = 2 to 8	24.2	79.8	-
	CLKout12 and CLKout13	Divide = 1 to 25 and DDLY = 1 to 12	15	49.5	-
		Divide = 26 to 1045 or DDLY > 13	19.1	63.0	-
Input Divider	Bank A	Divide = 2 to 8	9	29.7	-
	Bank B	Divide = 2 to 8			-
Analog Delay	Analog Delay Value	CLKout12_13_ADLY = 0 to 3	3.4	11.2	-
		CLKout12_13_ADLY = 4 to 7	3.8	12.5	-
		CLKout12_13_ADLY = 8 to 11	4.2	13.9	-
		CLKout12_13_ADLY = 12 to 15	4.7	15.5	-
		CLKout12_13_ADLY = 16 to 23	5.2	17.2	-
	When only one, CLKout12 or CLKout13, have Analog Delay Selected.		2.8	9.2	-
Clock Output Buffers					
LVDS	CLkout0 to CLKout11; 100 Ω differential termination		9	29.7	-
	CLkout12 to CLKout13; 100 Ω differential termination		14	46.2	-
LVPECL	CLKout0 to CLKout11; LVPECL 1600 mVpp, AC coupled using 240 Ω emitter resistors		24	79.2	28.5
	CLkout12 to CLKout13; LVPECL 1600 mVpp, AC coupled using 240 Ω emitter resistors		29.5	97.3	28.5
LVCMOS	LVCMOS Pair, CLKout4 to CLKout11, (CLKoutX_TYPE = 6 - 10), C_L = 5 pF	10 MHz	18.6	61.4	-
		50 MHz	23.1	76.2	-
		150 MHz	31.7	104.6	-
	LVCMOS Pair, CLKout12 and CLKout13, (CLKoutX_TYPE = 6 - 10), C_L = 5 pF	10 MHz	24.7	81.51	-
		50 MHz	30.3	100	-
		150 MHz	42.0	138.6	-
	LVCMOS Single, CLKout4 to CLKout11, (CLKoutX_TYPE=11 - 13), C_L = 5 pF	10 MHz	9.7	32	-
		50 MHz	10.8	35.6	-
		150 MHz	13.5	44.5	-
	LVCMOS Single, CLKout12 and CLKout13, (CLKoutX_TYPE= 11 - 13), C_L = 5 pF	10 MHz	15	49.5	-
		50 MHz	17.5	57.7	-
		150 MHz	22.8	75.2	-

(1) Power is dissipated externally in LVPECL emitter resistors. The externally dissipated power is calculated as twice the DC voltage level of one LVPECL clock output pin squared over the emitter resistance. That is to say power dissipated in emitter resistors = 2 * $V_{em}{}^2/R_{em}$

Copyright © 2021 Texas Instruments Incorporated

12 Layout

12.1 Layout Guidelines

12.1.1 Pin Connection Recommendations

12.1.1.1 Vcc Pins and Decoupling

All Vcc pins must always be connected.

Integrated capacitance on the IC makes high frequency decoupling capacitors unnecessary. Ferrite beads should be used on CLKout Vcc pins to minimize crosstalk through power supply. When several clocks share the same frequency, a single ferrite bead can be shared with the common frequency CLKout V_{CC}'s for power supply isolation.

12.1.1.2 Unused clock outputs

Leave unused clock outputs floating and powered down.

12.1.1.3 Unused clock inputs

Unused clock inputs can be left floating.

12.1.1.4 Unused GPIO (CLKoutTYPE_X)

Unused GPIO pins can be left floating. Alternatively, unused GPIO pins can individually be pulled to GND.

12.1.1.5 Bias

Proper bypassing of the Bias pin with a 1-µF capacitor connected to Vcc4_Bias (Pin 25) is important for low noise performance.

12.1.1.6 In MICROWIRE Mode

SYNC0 and SYNC1 have an internal pullup and may be left as a no-connect if external SYNC is not required. MIRCROWIRE SYNC may still be used in this condition.

12.2 Thermal Management

Power consumption of the LMK01801 can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times θ_{JA} should not exceed 125°C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to a printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

A recommended footprint including recommended solder mask and solder paste layers can be found at: http://www.ti.com/packaging for the RHS0048A package.

13 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

13.1 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the DSP, related peripherals, and other technical collateral is listed below.

Application Reports

AN-912 Common Data Transmission Parameters and their Definitions (SNLA036)

User's Guides

LMK01801 User's Guide (SNAU118)

Selection and Solution Guides

Clock and Timing Solutions (SLYB210)

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2021 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK01801BISQ/NOPB	ACTIVE	WQFN	RHS	48	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	K01801BI	Samples
LMK01801BISQE/NOPB	ACTIVE	WQFN	RHS	48	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	K01801BI	Samples
LMK01801BISQX/NOPB	ACTIVE	WQFN	RHS	48	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	K01801BI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

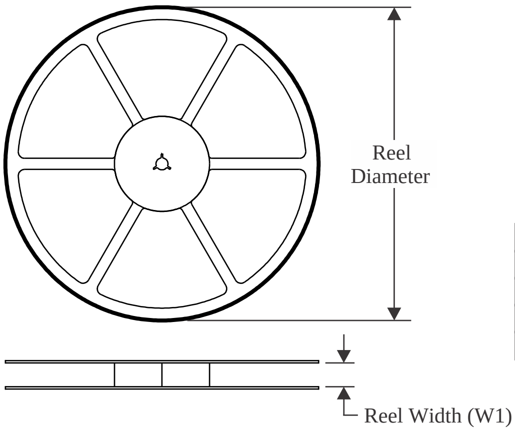
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

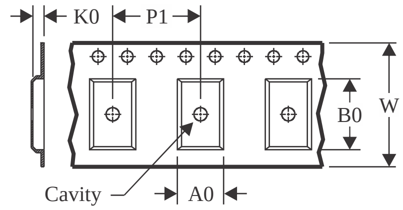
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

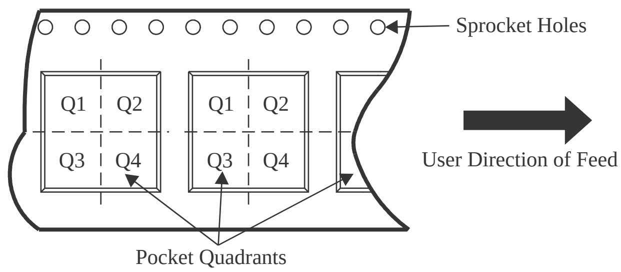


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

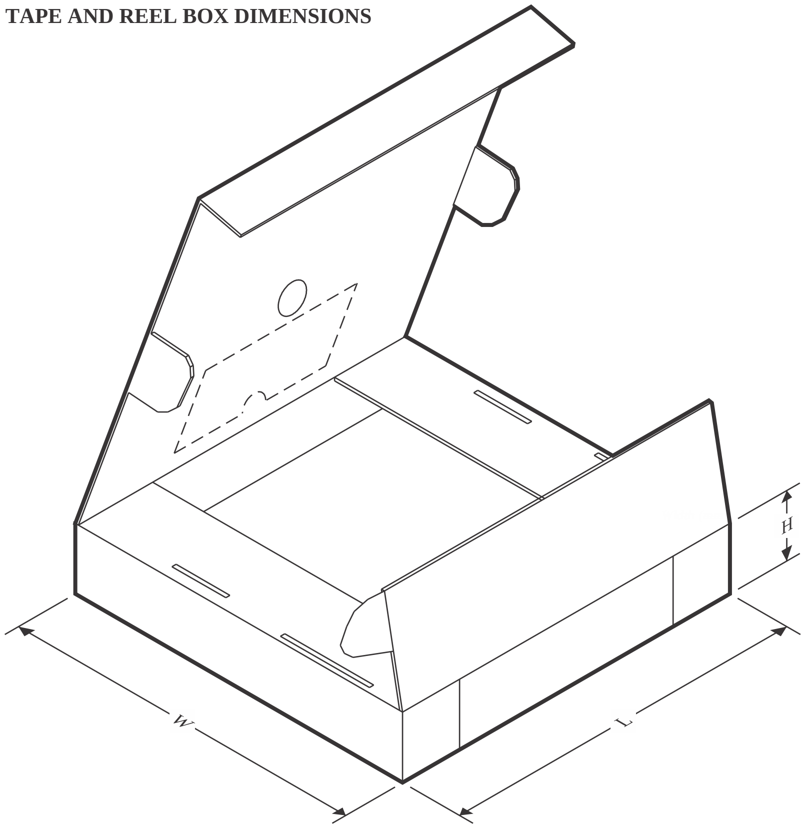
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

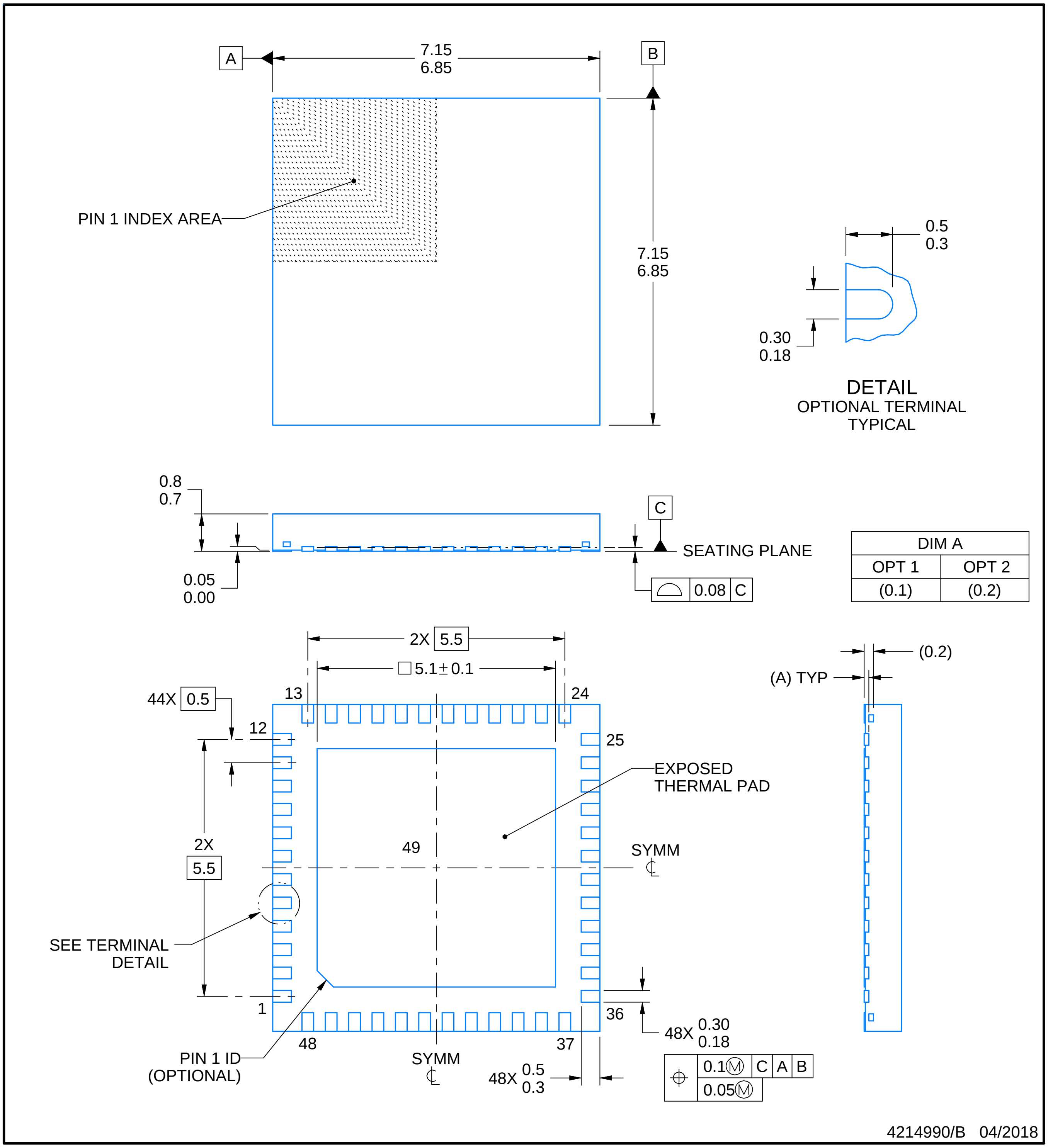
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK01801BISQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
LMK01801BISQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
LMK01801BISQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



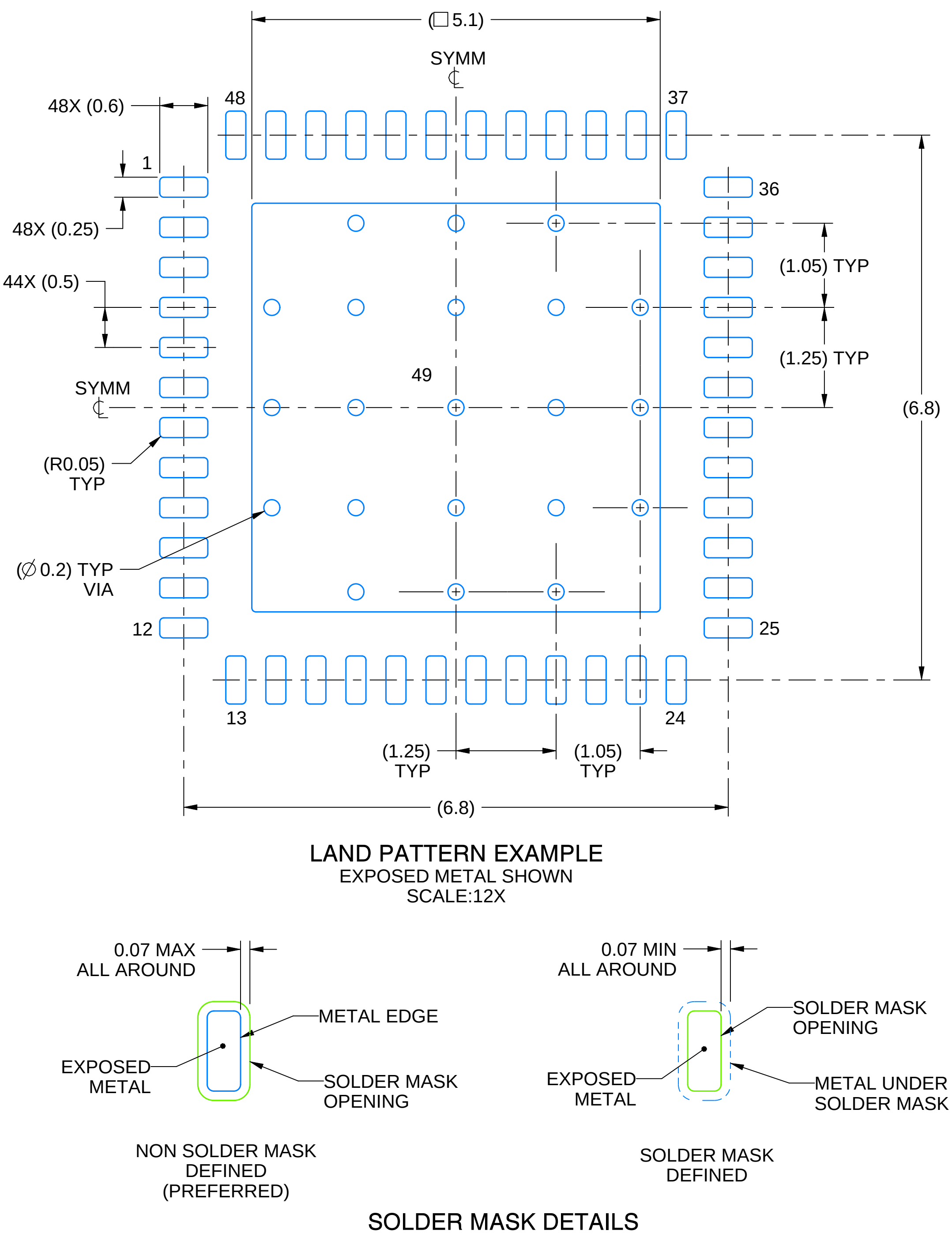
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK01801BISQ/NOPB	WQFN	RHS	48	1000	356.0	356.0	36.0
LMK01801BISQE/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
LMK01801BISQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	36.0



NOTES:

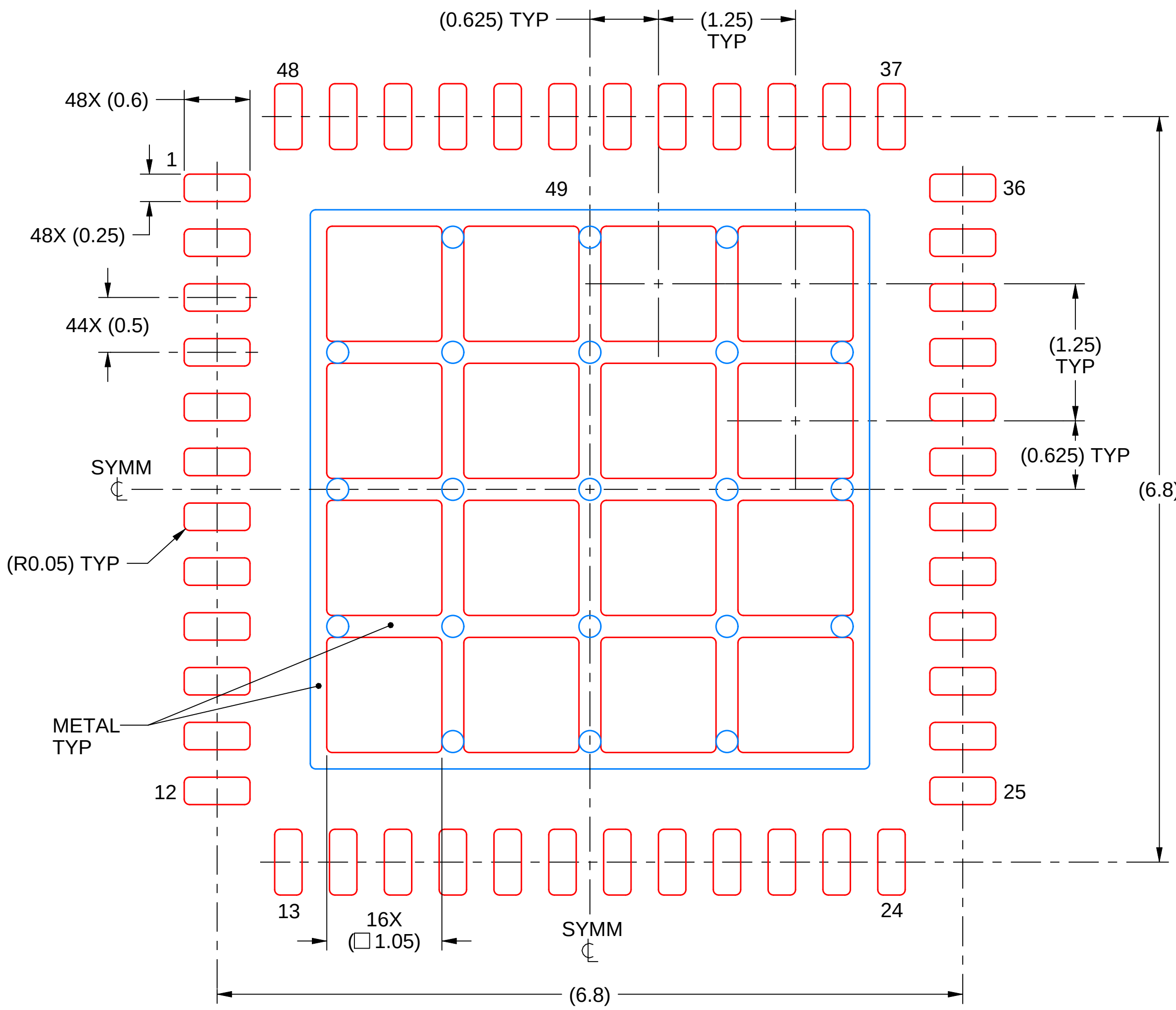
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



4214990/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4214990/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated