LMK04828-EP Ultra-Low-Noise, JESD204B-Compliant Clock Jitter Cleaner

1 Features

- EP Features
  - Gold Bondwires
  - Temperature Range: –55 to +105 °C
  - Lead Finish SnPb
- Maximum Distribution Frequency: 3.2 GHz
- JESD204B Support
- Ultra-Low RMS Jitter
  - 88-fs RMS Jitter (12 kHz to 20 MHz)
  - 91-fs RMS Jitter (100 Hz to 20 MHz)
  - –162.5 dBc/Hz Noise Floor at 245.76 MHz
- Up to 14 Differential Device Clocks From PLL2
  - Up to 7 SYSREF Clocks
  - Maximum Clock Output Frequency 3.2 GHz
  - LVPECL, LVDS, HSDS, LCPECL Programmable Outputs From PLL2
- Up to 1 Buffered VCXO/Crystal Output From PLL1
  - LVPECL, LVDS, 2xLVCMOS Programmable
- Multi-Mode: Dual PLL, Single PLL, and Clock Distribution
- Dual Loop PLLatinum™ PLL Architecture
- PLL1
  - Up to 3 Redundant Input Clocks
    - Automatic and Manual Switchover Modes
    - Hitless Switching and LOS
  - Integrated Low-Noise Crystal Oscillator Circuit
  - Holdover Mode When Input Clocks are Lost
- PLL2
  - Normalized [1 Hz] PLL Noise Floor of –227 dBc/Hz
  - Phase Detector Rate up to 155 MHz
  - OSCin Frequency-Doubler
  - Two Integrated Low-Noise VCOs
- 50% Duty Cycle Output Divides, 1 to 32 (Even and Odd)
- Precision Digital Delay, Dynamically Adjustable
- 25-ps Step Analog Delay
- 3.15-V to 3.45-V Operation
- Package: 64-Pin WQFN (9.0 mm × 9.0 mm × 0.8 mm)

2 Applications

- Wireless Infrastructure
- Data Converter Clocking
- Networking, SONET/SDH, DSLAM
- Medical / Video / Military / Aerospace
- Test and Measurement

3 Description

The LMK04828-EP device is the industry's highest performance clock conditioner with JESD204B support.

The 14 clock outputs from PLL2 can be configured to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. SYSREF can be provided using both DC and AC coupling. Not limited to JESD204B applications, each of the 14 outputs can be individually configured as high-performance outputs for traditional clocking systems.

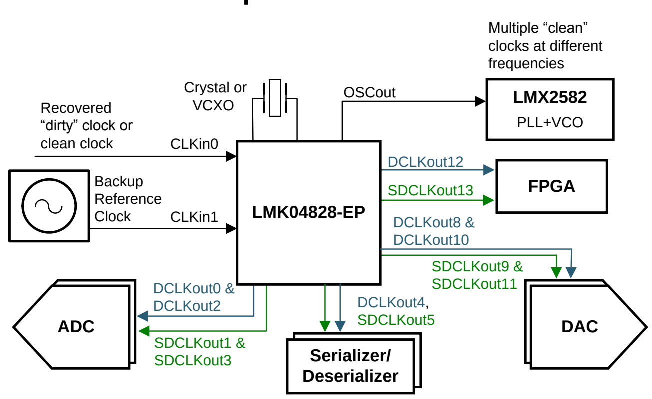
The high performance combined with features like the ability to trade off between power or performance, dual VCOs, dynamic digital delay, holdover, and glitchless analog delay make the LMK04828-EP ideal for providing flexible high-performance clocking trees.

Device Information(1)

PART NUMBER	VCO0 FREQUENCY	VCO1 FREQUENCY
LMK04828-EP	2450 to 2755 MHz	2875 to 3080 MHz

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

DATE	REVISION	NOTES
April 2017	*	Initial release

5 Device Comparison Table

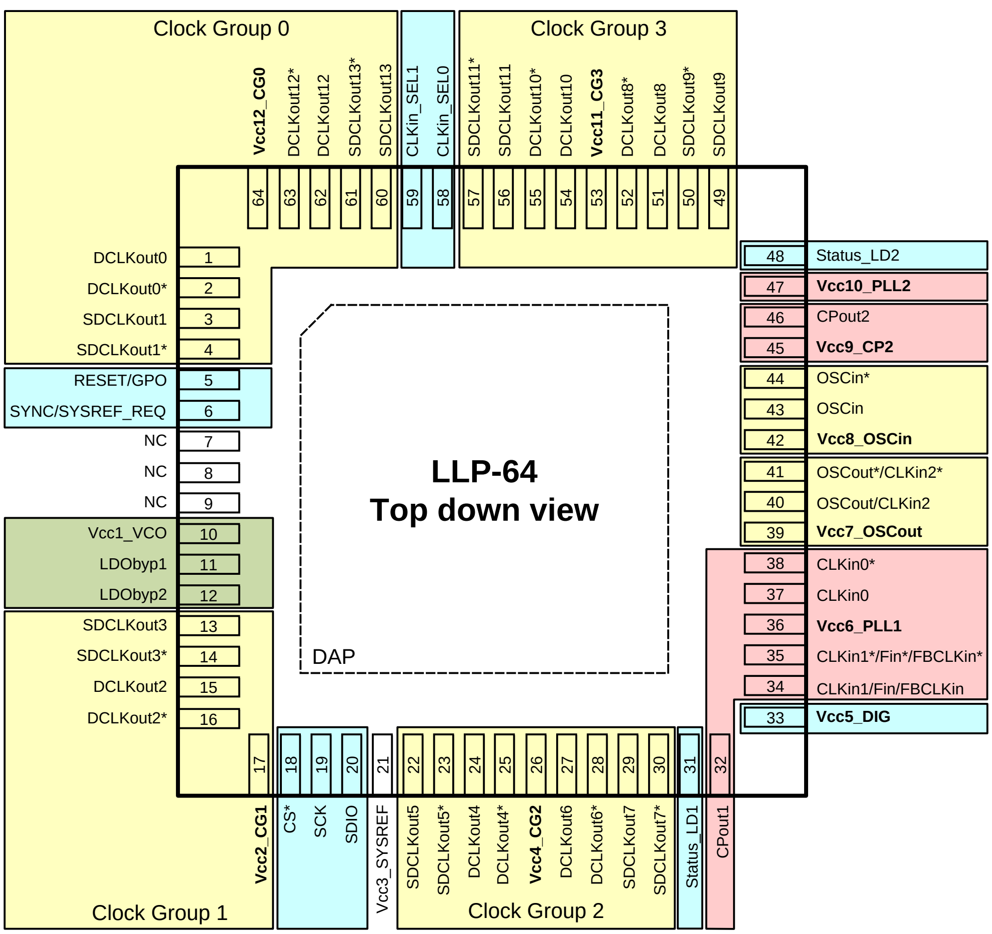
Table 1. Device Configuration Information

PART NUMBER	REFERENCE INPUTS(1)	OSCout (BUFFERED OSCin Clock) LVDS/ LVPECL/ LVCMOS (1)	PLL2 PROGRAMMABLE LVDS/LVPECL/HSDS OUTPUTS	VCO0 FREQUENCY	VCO1 FREQUENCY
LMK04828-EP	Up to 3	Up to 1	14	2450 to 2755 MHz	2875 to 3080 MHz

(1) OSCout may also be third clock input, CLKin2.

6 Pin Configuration and Functions

NKD Package
64-Pin WQFN
Top View



Pin Functions

PIN NO.	PIN NAME	I/O	TYPE	DESCRIPTION(1)
1 2	DCLKout0, DCLKout0*	O	Programmable	Device clock output 0
3 4	SDCLKout1, SDCLKout1*	O	Programmable	SYSREF or device clock output 1
5	RESET/GPO	I	CMOS	Device reset input or GPO

(1) See *Pin Connection Recommendations* for recommended connections.

Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION(1)
NO.	NAME			
6	SYNC/SYSREF_REQ	I	CMOS	Synchronization input or SYSREF_REQ for requesting continuous SYSREF
7, 8, 9	NC			Do not connect. These pins must be left floating.
10	Vcc1_VCO		PWR	Power supply for VCO LDO
11	LDObyp1		ANLG	LDO bypass, bypassed to ground with 10-µF capacitor.
12	LDObyp2		ANLG	LDO bypass, bypassed to ground with a 0.1-µF capacitor.
13 14	SDCLKout3, SDCLKout3*	O	Programmable	SYSREF or device clock output 3
15 16	DCLKout2, DCLKout2*	O	Programmable	Device clock output 2
17	Vcc2_CG1		PWR	Power supply for clock outputs 2 and 3
18	CS*	I	CMOS	Chip select
19	SCK	I	CMOS	SPI clock
20	SDIO	I/O	CMOS	SPI data
21	Vcc3_SYSREF		PWR	Power supply for SYSREF divider and SYNC
22 23	SDCLKout5, SDCKLout5*	O	Programmable	SYSREF or device clock output 5
24 25	DCLKout4, DCLKout4*	O	Programmable	Device clock output 4
26	Vcc4_CG2		PWR	Power supply for clock outputs 4, 5, 6 and 7
27 28	DCLKout6, DCLKout6*	O	Programmable	Device clock output 6
29 30	SDCLKout7, SDCLKout7*	O	Programmable	SYSREF or device clock output 7
31	Status_LD1	I/O	Programmable	Programmable status pin
32	CPout1	O	ANLG	Charge pump 1 output
33	Vcc5_DIG		PWR	Power supply for the digital circuitry
34 35	CLKin1, CLKin1*	I	ANLG	Reference clock Input Port 1 for PLL1
	FBCLKin, FBCLKin*	I	ANLG	Feedback input for external clock feedback input (0–delay mode)
	Fin, Fin*	I	ANLG	External VCO input (external VCO mode)
36	Vcc6_PLL1		PWR	Power supply for PLL1, charge pump 1, holdover DAC
37 38	CLKin0, CLKin0*	I	ANLG	Reference clock input port 0 for PLL1
39	Vcc7_OSCout		PWR	Power supply for OSCout port
40 41	OSCout, OSCout*	I/O	Programmable	Buffered output of OSCin port
	CLKin2, CLKin2*			Reference clock Input Port 2 for PLL1
42	Vcc8_OSCin		PWR	Power supply for OSCin
43 44	OSCin, OSCin*	I	ANLG	Feedback to PLL1, reference input to PLL2 — AC-coupled
45	Vcc9_CP2		PWR	Power supply for PLL2 charge pump
46	CPout2	O	ANLG	Charge pump 2 output
47	Vcc10_PLL2		PWR	Power supply for PLL2
48	Status_LD2	I/O	Programmable	Programmable status pin
49 50	SDCLKout9, SDCLKout9*	O	Programmable	SYSREF or device clock 9
51 52	DCLKout8, DCLKout8*	O	Programmable	Device clock output 8
53	Vcc11_CG3		PWR	Power supply for clock outputs 8, 9, 10, and 11
54 55	DCLKout10, DCLKout10*	O	Programmable	Device clock output 10
56 57	SDCLKout11, SDCLKout11*	O	Programmable	SYSREF or device clock output 11
58	CLKin_SEL0	I/O	Programmable	Programmable status pin
59	CLKin_SEL1	I/O	Programmable	Programmable status pin
60 61	SDCLKout13, SDCLKout13*	O	Programmable	SYSREF or device clock output 13
62 63	DCLKout12, DCLKout12*	O	Programmable	Device clock output 12
64	Vcc12_CG0		PWR	Power supply for clock outputs 0, 1, 12, and 13
DAP	DAP		GND	DIE ATTACH PAD, connect to GND

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage (2)	–0.3	3.6	V
V_{IN}	Input voltage	–0.3	(V_{CC} + 0.3)	V
T_L	Lead temperature (solder 4 seconds)		260	°C
T_J	Junction temperature		150	°C
I_{IN}	Differential input current (CLKinX/X*, OSCin/OSCin*, FBCLKin/FBCLKin*, Fin/Fin*)		±5	mA
MSL	Moisture sensitivity level		3	
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Never to exceed 3.6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	
		Machine Model (MM)	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±200 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±250 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Junction temperature			125	°C
T_A	Ambient temperature	–55	25	105	°C
V_{CC}	Supply voltage	3.15	3.3	3.45	V

7.4 Thermal Information

THERMAL METRIC[(1)]		LMK04828-EP NKD (WQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[(2)]	24.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[(3)]	6.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance[(4)]	3.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter[(5)]	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter[(6)]	3.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance[(7)]	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, Ψ_{JB} estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

(3.15 V < V_{CC} < 3.45 V, –55 °C < T_A < +105°C. Typical values at V_{CC} = 3.3 V, T_A = 25 °C, at the recommended operating conditions and are *not* assured.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
I_{CC_PD}	Power-down supply current			1	3	mA
I_{CC_CLKS}	Supply current[(1)]	14 HSDS 8 mA clocks enabled PLL1 and PLL2 locked.		565	670	mA
CLKin0/0*, CLKin1/1*, and CLKin2/2* INPUT CLOCK SPECIFICATIONS						
f_{CLKin}	Clock input frequency		0.001		750	MHz
$SLEW_{CLKin}$	Clock input slew rate [(2)]	20% to 80%	0.15	0.5		V/ns
V_{ID}CLKin	Differential clock input voltage[(3)] See Figure 4	AC-coupled	0.125		1.55	|V|
V_{SS}CLKin			0.25		3.1	Vpp
V_{CLKin}	Clock input Single-ended input voltage	AC-coupled to CLKinX; CLKinX* AC-coupled to Ground CLKinX_TYPE = 0 (Bipolar)	0.25		2.4	Vpp
		AC-coupled to CLKinX; CLKinX* AC-coupled to Ground CLKinX_TYPE = 1 (MOS)	0.35		2.4	Vpp
$\|V_{CLKinX\text{-}offset}\|$	DC offset voltage between CLKinX/CLKinX* (CLKinX* - CLKinX)	Each pin is AC-coupled, CLKin0/1/2 CLKinX_TYPE = 0 (Bipolar)		0		|mV|
		Each pin is AC-coupled, CLKin0/1 CLKinX_TYPE = 1 (MOS)		55		|mV|
	DC offset voltage between CLKin2/CLKin2* (CLKin2* - CLKin2)	Each pin is AC-coupled CLKinX_TYPE = 1 (MOS)		20		|mV|
$V_{CLKin\text{-}}$ V_{IH}	High input voltage	DC-coupled to CLKinX; CLKinX* AC-coupled to Ground CLKinX_TYPE = 1 (MOS)	2		V_{CC}	V
$V_{CLKin–}$ V_{IL}	Low input voltage		0		0.4	V

(1) See the applications section of *Power Supply Recommendations* for I_{CC} for specific part configuration and how to calculate I_{CC} for a specific design.
(2) To meet the jitter performance listed in the subsequent sections of this data sheet, the minimum recommended slew rate for all input clocks is 0.5 V/ns. This is especially true for single-ended clocks. Phase noise performance will begin to degrade as the clock input slew rate is reduced. However, the device functions at slew rates down to the minimum listed. When compared to single-ended clocks, differential clocks (LVDS, LVPECL) will be less susceptible to degradation in phase noise performance at lower slew rates due to their common mode noise rejection. However, it is also recommended to use the highest possible slew rate for differential clocks to achieve optimal phase noise performance at the device outputs.
(3) See *Differential Voltage Measurement Terminology* for definition of V_{ID} and V_{OD} voltages.

Electrical Characteristics (continued)

(3.15 V < V_{CC} < 3.45 V, –55 °C < T_A < +105°C. Typical values at V_{CC} = 3.3 V, T_A = 25 °C, at the recommended operating conditions and are *not* assured.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FBCLKin/FBCLKin* and Fin/Fin* INPUT SPECIFICATIONS						
$f_{FBCLKin}$	Clock input frequency for 0-delay with external feedback.	AC-coupled CLKinX_TYPE = 0 (Bipolar)	0.001		750	MHz
f_{Fin}	Clock input frequency for external VCO mode	AC-coupled (4) CLKinX_TYPE = 0 (Bipolar)	0.001		3100	MHz
	Clock input frequency for distribution mode	AC-coupled CLKinX_TYPE = 0 (Bipolar)	0.001		3200	
$V_{FBCLKin/Fin}$	Single-ended clock input voltage	AC-coupled CLKinX_TYPE = 0 (Bipolar)	0.25		2	Vpp
$SLEW_{FBCLKin/Fin}$	Slew rate on CLKin (2)	AC-coupled; 20% to 80%; (CLKinX_TYPE = 0)	0.15	0.5		V/ns
PLL1 SPECIFICATIONS						
f_{PD1}	PLL1 phase detector frequency				40	MHz
I_{CPout1}SOURCE	PLL1 charge pump source current (5)	V_{CPout1} = V_{CC}/2, PLL1_CP_GAIN = 0		50		µA
		V_{CPout1} = V_{CC}/2, PLL1_CP_GAIN = 1		150		
		V_{CPout1} = V_{CC}/2, PLL1_CP_GAIN = 2		250		
		…		…		
		V_{CPout1} = V_{CC}/2, PLL1_CP_GAIN = 14		1450		
		V_{CPout1} = V_{CC}/2, PLL1_CP_GAIN = 15		1550		
I_{CPout1}SINK	PLL1 Charge pump sink current (5)	V_{CPout1}=V_{CC}/2, PLL1_CP_GAIN = 0		–50		µA
		V_{CPout1}=V_{CC}/2, PLL1_CP_GAIN = 1		–150		
		V_{CPout1}=V_{CC}/2, PLL1_CP_GAIN = 2		–250		
		…		…		
		V_{CPout1}=V_{CC}/2, PLL1_CP_GAIN = 14		–1450		
		V_{CPout1}=V_{CC}/2, PLL1_CP_GAIN = 15		–1550		
I_{CPout1}%MIS	Charge pump sink / source mismatch	V_{CPout1} = V_{CC}/2, T = 25 °C		1%	10%	
$I_{CPout1}V_{TUNE}$	Magnitude of charge pump current variation vs. charge pump voltage	0.5 V < V_{CPout1} < V_{CC} - 0.5 V T_A = 25 °C		4%		
I_{CPout1}%TEMP	Charge pump current vs. temperature variation			4%		
I_{CPout1}TRI	Charge pump TRI-STATE leakage current	0.5 V < V_{CPout} < V_{CC} - 0.5 V			10	nA
PN10kHz	PLL 1/f Noise at 10-kHz offset. Normalized to 1-GHz Output Frequency	PLL1_CP_GAIN = 350 µA		–117		dBc/Hz
		PLL1_CP_GAIN = 1550 µA		–118		
PN1Hz	Normalized phase noise contribution	PLL1_CP_GAIN = 350 µA		–221.5		dBc/Hz
		PLL1_CP_GAIN = 1550 µA		–223		
PLL2 REFERENCE INPUT (OSCin) SPECIFICATIONS						
f_{OSCin}	PLL2 reference input (6)				500	MHz
$SLEW_{OSCin}$	PLL2 reference clock minimum slew rate on OSCin (2)	20% to 80%	0.15	0.5		V/ns
V_{OSCin}	Input voltage for OSCin or OSCin*	AC-coupled; Single-ended (Unused pin AC-coupled to GND)	0.2		2.4	Vpp
V_{ID}OSCin	Differential voltage swing See Figure 4	AC-coupled	0.2		1.55	|V|
V_{SS}OSCin			0.4		3.1	Vpp
$\|V_{OSCin-offset}\|$	DC offset voltage between OSCin/OSCin* (OSCinX* - OSCinX)	Each pin is AC-coupled		20		|mV|
$f_{doubler\_max}$	Doubler input frequency (7)	EN_PLL2_REF_2X = 1 (8); OSCin Duty Cycle 40% to 60%			155	MHz

(4) Assured by characterization.
(5) This parameter is programmable.
(6) F_{OSCin} maximum frequency assured by characterization. Production tested at 122.88 MHz.
(7) Assured by characterization. ATE tested at 122.88 MHz.
(8) The EN_PLL2_REF_2X bit enables/disables a frequency doubler mode for the PLL2 OSCin path.

Electrical Characteristics (continued)

(3.15 V < V_{CC} < 3.45 V, –55 °C < T_A < +105°C. Typical values at V_{CC} = 3.3 V, T_A = 25 °C, at the recommended operating conditions and are *not* assured.)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CRYSTAL OSCILLATOR MODE SPECIFICATIONS							
F_{XTAL}	Crystal frequency range	Fundamental mode crystal ESR = 200 Ω (10 to 30 MHz) ESR = 125 Ω (30 to 40 MHz)		10		40	MHz
C_{IN}	Input capacitance of OSCin port	–40 to 85 °C			1		pF
PLL2 PHASE DETECTOR and CHARGE PUMP SPECIFICATIONS							
f_{PD2}	Phase detector frequency (7)					155	MHz
I_{CPout}SOURCE	PLL2 charge pump source current (5)	V_{CPout2} = V_{CC}/2, PLL2_CP_GAIN = 0			100		µA
		V_{CPout2} = V_{CC}/2, PLL2_CP_GAIN = 1			400		
		V_{CPout2} = V_{CC}/2, PLL2_CP_GAIN = 2			1600		
		V_{CPout2} = V_{CC}/2, PLL2_CP_GAIN = 3			3200		
I_{CPout}SINK	PLL2 charge pump sink current (5)	V_{CPout2} = V_{CC}/2, PLL2_CP_GAIN = 0			–100		µA
		V_{CPout2} = V_{CC}/2, PLL2_CP_GAIN = 1			–400		
		V_{CPout2} = V_{CC}/2, PLL2_CP_GAIN = 2			–1600		
		V_{CPout2} = V_{CC}/2, PLL2_CP_GAIN = 3			–3200		
I_{CPout2}%MIS	Charge pump sink/source mismatch	V_{CPout2} = V_{CC}/2, T_A = 25°C			1%	10%	
$I_{CPout2}V_{TUNE}$	Magnitude of charge pump current vs. charge pump voltage variation	0.5 V < V_{CPout2} < V_{CC} – 0.5 V			4%		
I_{CPout2}%TEMP	Charge pump current vs. temperature variation				4%		
I_{CPout2}TRI	Charge pump leakage	0.5 V < V_{CPout2} < V_{CC} – 0.5 V				20	nA
PN10kHz	PLL 1/f noise at 10-kHz offset (9). Normalized to 1-GHz output frequency	PLL2_CP_GAIN = 400 µA			–118		dBc/Hz
		PLL2_CP_GAIN = 3200 µA			–121		
PN1Hz	Normalized phase noise contribution (10)	PLL2_CP_GAIN = 400 µA			–222.5		dBc/Hz
		PLL2_CP_GAIN = 3200 µA			–227		
INTERNAL VCO SPECIFICATIONS							
f_{VCO}	LMK04828-EP VCO tuning range	VCO0		2450		2755	MHz
		VCO1		2875		3080	
K_{VCO}	LMK04828-EP fine tuning sensitivity	VCO0	Lower end		17		MHz/V
			Higher end		27		
		VCO1	Lower end		17		
			Higher end		23		
$\|\Delta T_{CL}\|$	Allowable temperature drift for continuous lock (11)	After programming for lock, no changes to output configuration are permitted to assure continuous lock.				160	°C

(9) A specification in modeling PLL in-band phase noise is the 1/f flicker noise, $L_{PLL\_flicker}(f)$, which is dominant close to the carrier. Flicker noise has a 10 dB/decade slope. PN10kHz is normalized to a 10-kHz offset and a 1-GHz carrier frequency. PN10kHz = $L_{PLL\_flicker}$(10 kHz) – 20log(F_{out} / 1 GHz), where $L_{PLL\_flicker}(f)$ is the single side band phase noise of only the flicker noise's contribution to total noise, L(f). To measure $L_{PLL\_flicker}(f)$ it is important to be on the 10 dB/decade slope close to the carrier. A high compare frequency and a clean crystal are important to isolating this noise source from the total phase noise, L(f). $L_{PLL\_flicker}(f)$ can be masked by the reference oscillator performance if a low power or noisy source is used. The total PLL in-band phase noise performance is the sum of $L_{PLL\_flicker}(f)$ and $L_{PLL\_flat}(f)$.

(10) A specification modeling PLL in-band phase noise. The normalized phase noise contribution of the PLL, $L_{PLL\_flat}(f)$, is defined as: PN1HZ=$L_{PLL\_flat}(f)$ - 20log(N) – 10log(f_{PDX}). $L_{PLL\_flat}(f)$ is the single side band phase noise measured at an offset frequency, f, in a 1-Hz bandwidth and f_{PDX} is the phase detector frequency of the synthesizer. $L_{PLL\_flat}(f)$ contributes to the total noise, L(f).

(11) Maximum Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction from the value it was at the time that the 0x168 register was last programmed with PLL2_FCAL_DIS = 0, and still have the part stay in lock. The action of programming the 0x168 register, even to the same value, activates a frequency calibration routine. This implies the part will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reload the appropriate register to ensure it stays in lock. Regardless of what temperature the part was initially programmed at, the temperature can never drift outside the frequency range of –55°C to 105°C without violating specifications.

Electrical Characteristics (continued)

(3.15 V < V_{CC} < 3.45 V, –55 °C < T_A < +105°C. Typical values at V_{CC} = 3.3 V, T_A = 25 °C, at the recommended operating conditions and are *not* assured.)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE FLOOR							
$L(f)_{CLKout}$	LMK04828-EP, VCO0, noise floor 20-MHz offset (12)	245.76 MHz	LVDS		–156.3		dBc/Hz
			HSDS 6 mA		–158.4		
			HSDS 8 mA		–159.3		
			HSDS 10 mA		–158.9		
			LVPECL16 with 240 Ω		–161.6		
			LVPECL20 with 240 Ω		–162.5		
			LCPECL		–162.1		
$L(f)_{CLKout}$	LMK04828-EP, VCO1, noise floor 20-MHz offset (12)	245.76 MHz	LVDS		–155.7		dBc/Hz
			HSDS 6 mA		–157.5		
			HSDS 8 mA		–158.1		
			HSDS 10 mA		–157.7		
			LVPECL16 with 240 Ω		–160.3		
			LVPECL20 with 240 Ω		–161.1		
			LCPECL		–160.8		
CLKout CLOSED LOOP PHASE NOISE SPECIFICATIONS A COMMERCIAL QUALITY VCXO (13)							
$L(f)_{CLKout}$	LMK04828-EP VCO0 SSB phase noise (12) 245.76 MHz	Offset = 1 kHz			–124.3		dBc/Hz
		Offset = 10 kHz			–134.7		
		Offset = 100 kHz			–136.5		
		Offset = 1 MHz			–148.4		
		Offset = 10 MHz	LVDS		–156.4		
			HSDS 8 mA		–159.1		
			LVPECL16 with 240 Ω		–160.8		
$L(f)_{CLKout}$	LMK04828-EP VCO1 SSB phase noise (12) 245.76 MHz	Offset = 1 kHz			–124.2		dBc/Hz
		Offset = 10 kHz			–134.4		
		Offset = 100 kHz			–135.2		
		Offset = 1 MHz			–151.5		
		Offset = 10 MHz	LVDS		–159.9		
			HSDS 8 mA		–155.8		
			LVPECL16 with 240 Ω		–158.1		

(12) Data collected using ADT2-1T+ balun. Loop filter is C1 = 47 pF, C2 = 3.9 nF, R2 = 620 Ω, C3 = 10 pF, R3 = 200 Ω, C4 = 10 pF, R4 = 200 Ω, PLL1_CP = 450 µA, PLL2_CP = 3.2 mA.. VCO0 loop filter bandwidth = 344 kHz, phase margin = 73 degrees. VCO1 Loop filter loop bandwidth = 233 kHz, phase margin = 70 degrees. CLKoutX_Y_IDL = 1, CLKoutX_Y_ODL = 0.
(13) VCXO used is a 122.88-MHz Crystek CVHD-950-122.880.

Electrical Characteristics (continued)

(3.15 V < V_{CC} < 3.45 V, –55 °C < T_A < +105°C. Typical values at V_{CC} = 3.3 V, T_A = 25 °C, at the recommended operating conditions and are *not* assured.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLKout CLOSED LOOP JITTER SPECIFICATIONS A COMMERCIAL QUALITY VCXO (13)						
J_{CLKout}	LMK04828-EP, VCO0 f_{CLKout} = 245.76 MHz Integrated RMS jitter (12)	LVDS, BW = 100 Hz to 20 MHz		112		fs rms
		LVDS, BW = 12 kHz to 20 MHz		109		
		HSDS 8 mA, BW = 100 Hz to 20 MHz		102		
		HSDS 8 mA, BW = 12 kHz to 20 MHz		99		
		LVPECL16 with 240 Ω, BW = 100 Hz to 20 MHz		98		
		LVPECL20 with 240 Ω, BW = 12 kHz to 20 MHz		95		
		LCPECL with 240 Ω, BW = 100 Hz to 20 MHz		96		
		LCPECL with 240 Ω, BW = 12 kHz to 20 MHz		93		
	LMK04828-EP, VCO1 f_{CLKout} = 245.76 MHz Integrated RMS jitter (12)	LVDS, BW = 100 Hz to 20 MHz		108		fs rms
		LVDS, BW = 12 kHz to 20 MHz		105		
		HSDS 8 mA, BW = 100 Hz to 20 MHz		98		
		HSDS 8 mA, BW = 12 kHz to 20 MHz		94		
		LVPECL16 with 240 Ω, BW = 100 Hz to 20 MHz		93		
		LVPECL20 with 240 Ω, BW = 12 kHz to 20 MHz		90		
		LCPECL with 240 Ω, BW = 100 Hz to 20 MHz		91		
		LCPECL with 240 Ω, BW = 12 kHz to 20 MHz		88		
DEFAULT POWER ON RESET CLOCK OUTPUT FREQUENCY						
$f_{CLKout\text{-}start\text{-}up}$	Default output clock frequency at device power on (14)	LMK04828-EP		315		MHz
f_{OSCout}	OSCout frequency	See (7)			500	MHz
CLOCK SKEW AND DELAY						
$\lvert T_{SKEW} \rvert$	DCLKoutX to SDCLKoutY F_{CLK} = 245.76 MHz, R_L= 100 Ω AC-coupled (15)	Same pair, same format (16) SDCLKoutY_MUX = 0 (device clock)			25	|ps|
	Maximum DCLKoutX or SDCLKoutY to DCLKoutX or SDCLKoutY F_{CLK} = 245.76 MHz, R_L= 100 Ω AC-coupled	Any pair, same format (16) SDCLKoutY_MUX = 0 (device clock)		50		
$ts_{JESD204B}$	SYSREF to device clock setup time base reference. See *SYSREF to Device Clock Alignment* to adjust SYSREF to device clock setup time as required.	SDCLKoutY_MUX = 1 (SYSREF) SYSREF_DIV = 30 SYSREF_DDLY = 8 (global) SDCLKoutY_DDLY = 1 (2 cycles, local) DCLKoutX_MUX = 1 (Div + DCC + HS) DCLKoutX_DIV = 30 DCLKoutX_DDLY_CNTH = 7 DCLKoutX_DDLY_CNTL = 6 DCLKoutX_HS = 0 SDCLKoutY_HS = 0		–80		ps
t_{PD}CLKin0_ SDCLKout1	Propagation delay from CLKin0 to SDCLKout1	CLKin0_OUT_MUX = 0 (SYSREF Mux) SYSREF_CLKin0_MUX = 1 (CLKin0) SDCLKout1_PD = 0 SDCLKout1_DDLY = 0 (Bypass) SDCLKout1_MUX = 1 (SR) EN_SYNC = 1 LVPECL16 with 240 Ω		0.65		ns
f_{ADLY}max	Maximum analog delay frequency	DCLKoutX_MUX = 4		1536		MHz

(14) OSCout will oscillate at start-up at the frequency of the VCXO attached to OSCin port.
(15) Equal loading and identical clock output configuration on each clock output is required for specification to be valid. Specification not valid for delay mode.
(16) LVPECL uses a 120-Ω emitter resistor, LVDS and HSDS use a 560-Ω shunt.

Electrical Characteristics (continued)

(3.15 V < V_{CC} < 3.45 V, –55 °C < T_A < +105°C. Typical values at V_{CC} = 3.3 V, T_A = 25 °C, at the recommended operating conditions and are *not* assured.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS CLOCK OUTPUTS (DCLKoutX, SDCLKoutY, AND OSCout)						
V_{OD}	Differential output voltage	T = 25°C, DC measurement AC-coupled to receiver input R_L = 100-Ω differential termination		395		|mV|
ΔV_{OD}	Change in magnitude of V_{OD} for complementary output states		–60		60	mV
V_{OS}	Output offset voltage		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} for complementary output states				35	|mV|
T_R / T_F	Output rise time	20% to 80%, R_L = 100 Ω, 245.76 MHz		180		ps
	Output fall time	80% to 20%, R_L = 100 Ω				
I_{SA} I_{SB}	Output short-circuit current - single-ended	Single-ended output shorted to GND T = 25 °C	–24		24	mA
I_{SAB}	Output short-circuit current - differential	Complimentary outputs tied together	–12		12	mA
6-mA HSDS CLOCK OUTPUTS (DCLKoutX AND SDCLKoutY)						
V_{OH}		T = 25 °C, DC measurement Termination = 50 Ω to V_{CC} – 1.42 V		V_{CC} – 1.05		
V_{OL}				V_{CC} – 1.64		
V_{OD}	Differential output voltage			590		|mV|
ΔV_{OD}	Change in V_{OD} for complementary output states		–80		80	mVpp
8-mA HSDS CLOCK OUTPUTS (DCLKoutX AND SDCLKoutY)						
T_R / T_F	Output rise time	245.76 MHz, 20% to 80%, R_L = 100 Ω		170		ps
	Output fall time	245.76 MHz, 80% to 20%, R_L = 100 Ω				
V_{OH}		DC measurement Termination = 50 Ω to V_{CC} – 1.64 V		V_{CC} – 1.26		
V_{OL}				V_{CC} – 2.06		
V_{OD}	Differential output voltage			800		|mV|
ΔV_{OD}	Change in V_{OD} for complementary output states		–115		115	mVpp
10-mA HSDS CLOCK OUTPUTS (DCLKoutX AND SDCLKoutY)						
V_{OH}		T = 25 °C, DC measurement Termination = 50 Ω to V_{CC} – 1.43 V		V_{CC} – 0.99		
V_{OL}				V_{CC} – 1.97		
V_{OD}				980		mVpp
ΔV_{OD}	Change in V_{OD} for complementary output states		–115		115	mVpp
LVPECL CLOCK OUTPUTS (DCLKoutX AND SDCLKoutY)						
T_R / T_F	20% to 80% output rise	R_L = 100 Ω, emitter resistors = 240 Ω to GND DCLKoutX_TYPE = 4 or 5 (1600 or 2000 mVpp)		150		ps
	80% to 20% output fall time					
1600-mVpp LVPECL CLOCK OUTPUTS (DCLKoutX AND SDCLKoutY)						
V_{OH}	Output high voltage	DC Measurement Termination = 50 Ω to V_{CC} – 2 V		V_{CC} – 1.04		V
V_{OL}	Output low voltage			V_{CC} – 1.80		V
V_{OD}	Output voltage See Figure 5			760		|mV|
2000-mVpp LVPECL CLOCK OUTPUTS (DCLKoutX AND SDCLKoutY)						
V_{OH}	Output high voltage	DC Measurement Termination = 50 Ω to V_{CC} – 2.3 V		V_{CC} – 1.09		V
V_{OL}	Output low voltage			V_{CC} – 2.05		V
V_{OD}	Output voltage See Figure 5			960		|mV|
LCPECL CLOCK OUTPUTS (DCLKoutX AND SDCLKoutY)						
V_{OH}	Output high voltage	DC Measurement Termination = 50 Ω to 0.5 V		1.57		V
V_{OL}	Output low voltage			0.62		V
V_{OD}	Output voltage See Figure 5			950		|mV|

Electrical Characteristics (continued)

(3.15 V < V_{CC} < 3.45 V, –55 °C < T_A < +105°C. Typical values at V_{CC} = 3.3 V, T_A = 25 °C, at the recommended operating conditions and are *not* assured.)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVCMOS CLOCK OUTPUTS (OSCout)						
f_{CLKout}	Maximum frequency See [17]	5-pF Load	250			MHz
V_{OH}	Output high voltage	1-mA Load	V_{CC} – 0.1			V
V_{OL}	Output low voltage	1-mA Load			0.1	V
I_{OH}	Output high current (source)	V_{CC} = 3.3 V, V_O = 1.65 V		28		mA
I_{OL}	Output low current (sink)	V_{CC} = 3.3 V, V_O = 1.65 V		28		mA
$DUTY_{CLK}$	Output duty cycle[18]	V_{CC}/2 to V_{CC}/2, F_{CLK} = 100 MHz, T = 25°C		50%		
T_R	Output rise time	20% to 80%, R_L = 50 Ω, C_L = 5 pF		400		ps
T_F	Output fall time	80% to 20%, R_L = 50 Ω, C_L = 5 pF		400		ps
DIGITAL OUTPUTS (CLKin_SELX, Status_LDX, AND RESET/GPO)						
V_{OH}	High-level output voltage	I_{OH} = –500 µA CLKin_SELX_TYPE = 3 or 4 Status_LDX_TYPE = 3 or 4 RESET_TYPE = 3 or 4	V_{CC} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 500 µA CLKin_SELX_TYPE = 3, 4, or 6 Status_LDX_TYPE = 3, 4, or 6 RESET_TYPE = 3, 4, or 6			0.4	V
DIGITAL OUTPUT (SDIO)						
V_{OH}	High-level output voltage	I_{OH} = –500 µA ; during SPI read. SDIO_RDBK_TYPE = 0	V_{CC} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 500 µA ; during SPI read. SDIO_RDBK_TYPE = 0 or 1			0.4	V
DIGITAL INPUTS (CLKinX_SEL, RESET/GPO, SYNC, SCK, SDIO, OR CS*)						
V_{IH}	High-level input voltage		1.2		V_{CC}	V
V_{IL}	Low-level input voltage				0.4	V
DIGITAL INPUTS (CLKinX_SEL)						
I_{IH}	High-level input current V_{IH} = V_{CC}	CLKin_SELX_TYPE = 0, (high impedance)	–5		5	µA
		CLKin_SELX_TYPE = 1 (pullup)	–5		5	
		CLKin_SELX_TYPE = 2 (pulldown)	10		80	
I_{IL}	Low-level input current V_{IL} = 0 V	CLKin_SELX_TYPE = 0, (high impedance)	–5		5	µA
		CLKin_SELX_TYPE = 1 (pullup)	–40		–5	
		CLKin_SELX_TYPE = 2 (pulldown)	–5		5	
DIGITAL INPUT (RESET/GPO)						
I_{IH}	High-level input current V_{IH} = V_{CC}	RESET_TYPE = 2 (pulldown)	10		80	µA
I_{IL}	Low-level input current V_{IL} = 0 V	RESET_TYPE = 0 (high impedance)	–5		5	µA
		RESET_TYPE = 1 (pullup)	–40		–5	
		RESET_TYPE = 2 (pulldown)	–5		5	
DIGITAL INPUTS (SYNC)						
I_{IH}	High-level input current	V_{IH} = V_{CC}			25	µA
I_{IL}	Low-level input current	V_{IL} = 0 V	–5		5	
DIGITAL INPUTS (SCK, SDIO, CS*)						
I_{IH}	High-level input current	V_{IH} = V_{CC}	–5		5	µA
I_{IL}	Low-level input current	V_{IL} = 0	–5		5	µA
DIGITAL INPUT TIMING						
t_{HIGH}		RESET pin held high for device reset	25			ns

(17) Assured by characterization. ATE tested to 10 MHz.
(18) Assumes OSCin has 50% input duty cycle.

7.6 SPI Interface Timing

			MIN	NOM	MAX	UNIT
td_S	Setup time for SDI edge to SCLK rising edge	See Figure 1	10			ns
td_H	Hold time for SDI edge from SCLK rising edge	See Figure 1	10			ns
t_{SCLK}	Period of SCLK	See Figure 1	50 (1)			ns
t_{HIGH}	High width of SCLK	See Figure 1	25			ns
t_{LOW}	Low width of SCLK	See Figure 1	25			ns
tc_S	Setup time for CS* falling edge to SCLK rising edge	See Figure 1	10			ns
tc_H	Hold time for CS* rising edge from SCLK rising edge	See Figure 1	30			ns
td_V	SCLK falling edge to valid read back data	See Figure 1			20	ns

(1) 20 MHz

7.7 Timing Diagram

Register programming information on the SDIO pin is clocked into a shift register on each rising edge of the SCK signal. On the rising edge of the CS* signal, the register is sent from the shift register to the register addressed. A slew rate of at least 30 V/µs is recommended for these signals. After programming is complete the CS* signal should be returned to a high state. If the SCK or SDIO lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during this programming.

4-wire mode read back has the same timing as the SDIO pin.

R/W bit = 0 is for SPI write. R/W bit = 1 is for SPI read.

W1 and W0 is written as 0.

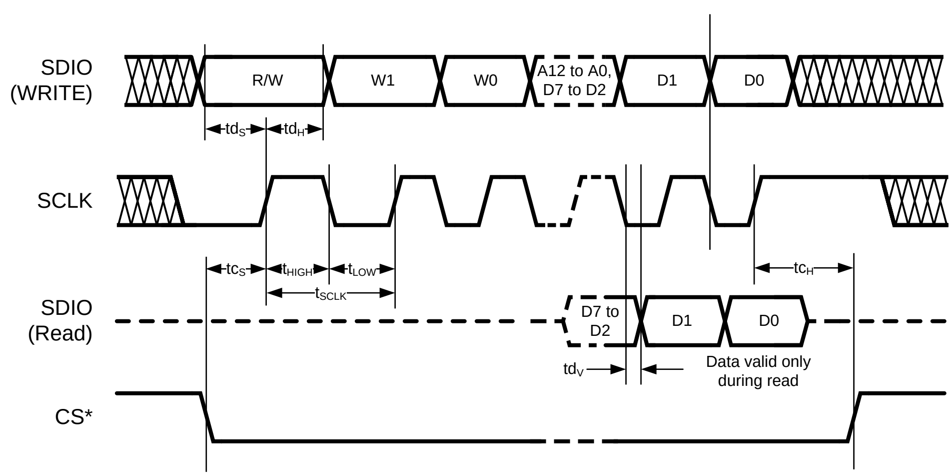
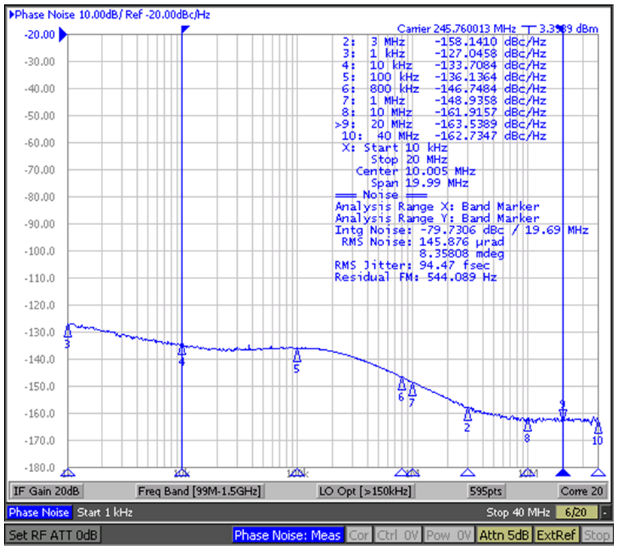


Figure 1. SPI Timing Diagram

7.8 Typical Characteristics – Clock Output AC Characteristics

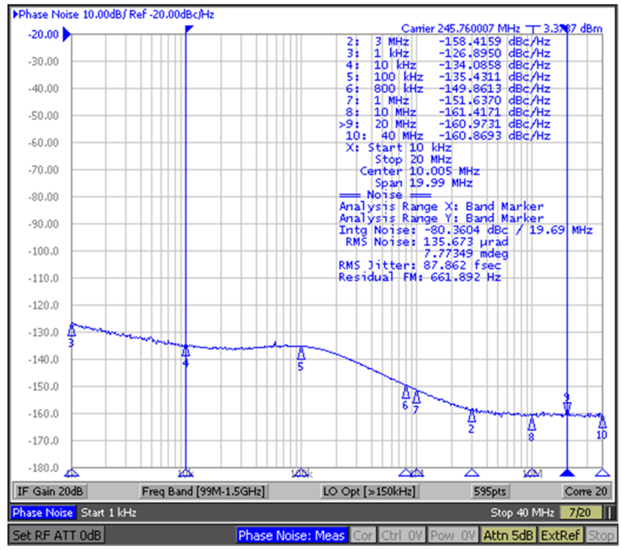
NOTE: These plots show performance at frequencies beyond the point at which the part is ensured to operate in order to give an idea of the capabilities of the part. They do not imply any sort of ensured specification.

For Figure 2 and Figure 3, CLKout2_3_IDL=1; CLKout2_3_ODL=0; LVPECL20 with 240-Ω emitter resistors; DCLKout2 Frequency = 245.76 MHz; DCLKout2_MUX = 0 (Divider). Balun is ADT2-1T+.



VCO_MUX = 0 (VCO0)
VCO0 = 2457.6 MHz
DCLKout2_DIV = 10
PLL2 Loop Filter Bandwidth = 344 kHz
PLL2 Phase Margin = 73°

Figure 2. LMK04828-EP DCLKout2 Phase Noise

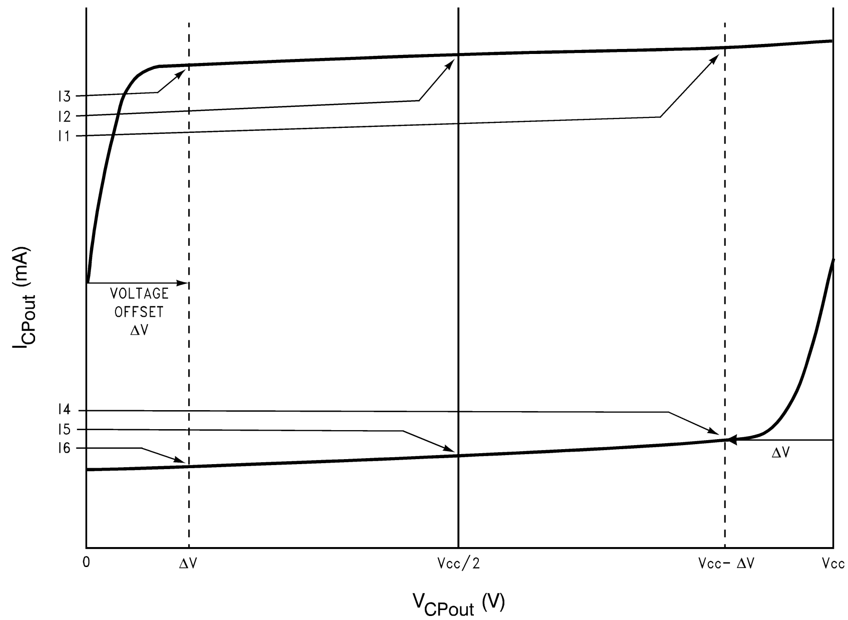


VCO_MUX = 1 (VCO1)
VCO = 2949.12 MHz
DCLKout2_DIV = 12
PLL2 Loop Filter Bandwidth = 233 kHz
PLL2 Phase Margin = 70°

Figure 3. LMK04828-EP DCLKout2 Phase Noise

8 Parameter Measurement Information

8.1 Charge Pump Current Specification Definitions



I1 = Charge Pump Sink Current at $V_{CPout} = V_{CC} - \Delta V$

I2 = Charge Pump Sink Current at $V_{CPout} = V_{CC}/2$

I3 = Charge Pump Sink Current at $V_{CPout} = \Delta V$

I4 = Charge Pump Source Current at $V_{CPout} = V_{CC} - \Delta V$

I5 = Charge Pump Source Current at $V_{CPout} = V_{CC}/2$

I6 = Charge Pump Source Current at $V_{CPout} = \Delta V$

ΔV = Voltage offset from the positive and negative supply rails. Defined to be 0.5 V for this device.

8.1.1 Charge Pump Output Current Magnitude Variation vs Charge Pump Output Voltage

$$I_{CPout} \text{ Vs } V_{CPout} = \frac{|I1| - |I3|}{|I1| + |I3|} \times 100\%$$

$$= \frac{|I4| - |I6|}{|I4| + |I6|} \times 100\%$$

8.1.2 Charge Pump Sink Current vs Charge Pump Output Source Current Mismatch

$$I_{CPout} \text{ Sink Vs } I_{CPout} \text{ Source} = \frac{|I2| - |I5|}{|I2| + |I5|} \times 100\%$$

8.1.3 Charge Pump Output Current Magnitude Variation vs Ambient Temperature

$$I_{CPout} \text{ Vs } T_A = \frac{|I_2|\big|_{T_A} - |I_2|\big|_{T_A = 25°C}}{|I_2|\big|_{T_A = 25°C}} \times 100\%$$

$$= \frac{|I_5|\big|_{T_A} - |I_5|\big|_{T_A = 25°C}}{|I_5|\big|_{T_A = 25°C}} \times 100\%$$

8.2 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions, causing confusion when reading data sheets or communicating with other engineers. This section addresses the measurement and description of a differential signal so the reader can understand and distinguish between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD}, depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. This signal only exists in reference to its differential pair and does not exist in the IC with respect to ground. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 4 illustrates the two different definitions side-by-side for inputs and Figure 5 illustrates the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the non-inverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the non-inverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus, the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

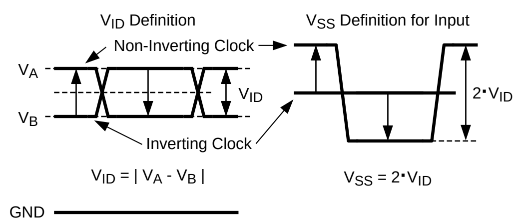


Figure 4. Two Different Definitions for Differential Input Signals

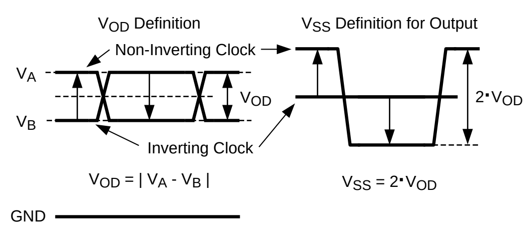


Figure 5. Two Different Definitions for Differential Output Signals

Refer to application note *AN-912 Common Data Transmission Parameters and their Definitions* for more information.

9 Detailed Description

9.1 Overview

The LMK04828-EP device is very flexible in meeting many application requirements. The typical use case for the LMK04828-EP is as a cascaded dual loop jitter cleaner for JESD204B systems. However, traditional (non-JESD204B) systems are possible with use of the large SYSREF divider to produce a low frequency. Note that while the Device Clock outputs (DCLKoutX) do not provide LVCMOS outputs, the OSCout may be used to provide LVCMOS outputs at DCLKout6 or DCLKout8 frequency using the feedback mux.

In addition to dual loop operation, by powering down various blocks the LMK04828-EP may be configured for single loop or clock distribution modes also.

9.1.1 Jitter Cleaning

The dual loop PLL architecture of the LMK04828-EP provides the lowest jitter performance over a wide range of output frequencies and phase noise integration bandwidths for clock inputs with unknown signal quality or low frequency. The first stage PLL (PLL1) is driven by an external reference clock and uses an external VCXO or tunable crystal to provide a frequency accurate, low phase noise reference clock for the second stage frequency multiplication PLL (PLL2).

PLL1 uses a narrow loop bandwidth (typically 10 Hz to 300 Hz) to retain the frequency accuracy of the reference clock input signal while at the same time suppressing the higher offset frequency phase noise that the reference clock may have accumulated along its path or from other circuits. This “cleaned” reference clock provides the reference input to PLL2.

The low phase noise reference provided to PLL2 allows PLL2 to operate with a wide loop bandwidth (typically 50 kHz to 200 kHz). The loop bandwidth for PLL2 is chosen to "minimize noise contribution from both PLL and VCO.

Ultra-low jitter is achieved by allowing the phase noise of the external VCXO or crystal to dominate the final output phase noise at low offset frequencies, and thephase noise of the internal VCO to dominate the final output phase noise at high offset frequencies. This results in best overall phase noise and jitter performance.

9.1.2 JEDEC JESD204B Support

The LMK04828-EP provides support for JEDEC JESD204B. The LMK04828-EP will clock up to seven JESD204B targets using seven device clocks (DCLKoutX) and seven SYSREF clocks (SDCLKoutY). Each device clock is grouped with a SYSREF clock.

It is also possible to reprogram SYSREF clocks to behave as extra device clocks for applications which have non-JESD204B clock requirements.

9.1.3 Three PLL1 Redundant Reference Inputs (CLKin0/CLKin0*, CLKin1/CLKin1*, and CLKin2/CLKin2*)

The LMK04828-EP has up to three reference clock inputs for PLL1: they are CLKin0, CLKin1, and CLKin2. The active clock is chosen based on CLKin_SEL_MODE. Automatic or manual switching can occur between the inputs.

CLKin0, CLKin1, and CLKin2 each have their own PLL1 R dividers.

CLKin1 is shared for use as an external 0-delay feedback (FBCLKin), or for use with an external VCO (Fin).

CLKin2 is shared for use as OSCout. To use power-down OSCout, see *VCO_MUX, OSCout_MUX, OSCout_FMT*.

Fast manual switching between reference clocks is possible with a external pins CLKin_SEL0 and CLKin_SEL1.

9.1.4 VCXO or Crystal Buffered Output

The LMK04828-EP provides OSCout, which by default is a buffered copy of the PLL1 feedback and PLL2 reference input. This reference input is typically a low noise VCXO or Crystal. When using a VCXO, this output can be used to clock external devices such as microcontrollers, FPGAs, CPLDs, and so forth, before the LMK04828-EP is programmed.

The OSCout buffer output type is programmable to LVDS, LVPECL, or LVCMOS.

Overview (continued)

The VCXO or Crystal buffered output can be synchronized to the VCO clock distribution outputs by using Cascaded 0-Delay Mode. The buffered output of VCXO/Crystal has deterministic phase relationship with CLKin.

9.1.5 Frequency Holdover

The LMK04828-EP supports holdover operation to keep the clock outputs on frequency with minimum drift when the reference is lost until a valid reference clock signal is re-established.

9.1.6 PLL2 Integrated Loop Filter Poles

The LMK04828-EP features programmable 3rd and 4th order loop filter poles for PLL2. These internal resistors and capacitor values may be selected from a fixed range of values to achieve either a 3rd or 4th order loop filter response. The integrated programmable resistors and capacitors compliment external components mounted near the chip.

These integrated components can be effectively disabled by programming the integrated resistors and capacitors to their minimum values.

9.1.7 Internal VCOs

The LMK04828-EP has two internal VCOs, selected by VCO_MUX. The output of the selected VCO is routed to the *Clock Distribution Path*. This same selection is also fed back to the PLL2 phase detector through a prescaler and N-divider.

9.1.8 External VCO Mode

The Fin/Fin* input allows an external VCO to be used with PLL2 of the LMK04828-EP.

Using an external VCO reduces the number of available clock inputs by one.

9.1.9 Clock Distribution

The LMK04828-EP features a total of 14 PLL2 clock outputs driven from the internal or external VCO.

All PLL2 clock outputs have programmable output types. They can be programmed to LVPECL, LVDS, or HSDS, or LCPECL.

If OSCout is included in the total number of clock outputs the LMK04828-EP is able to distribute, then up to 15 differential clocks. OSCout may be a buffered version of OSCin, DCLKout6, DCLKout8, or SYSREF.

The following sections discuss specific features of the clock distribution channels that allow the user to control various aspects of the output clocks.

9.1.9.1 Device Clock Divider

Each device clock, DCLKoutX, has a single clock output divider. The divider supports a divide range of 1 to 32 (even and odd) with 50% output duty cycle using duty cycle correction mode. The output of this divider may also be directed to SDCLKoutY, where Y = X + 1.

9.1.9.2 SYSREF Clock Divider

The SYSREF clocks, SDCLKoutY, all share a common divider. The divider supports a divide range of 8 to 8191 (even and odd).

9.1.9.3 Device Clock Delay

The device clocks include both a analog and digital delay for phase adjustment of the clock outputs.

The analog delay allows a nominal 25 ps step size and range from 0 to 575 ps of total delay. Enabling the analog delay adds a nominal 500 ps of delay in addition to the programmed value.

The digital delay allows a group of outputs to be delayed from 4 to 32 VCO cycles. The delay step can be as small as half the period of the clock distribution path. For example, 2-GHz VCO frequency results in 250-ps coarse tuning steps. The coarse (digital) delay value takes effect on the clock outputs after a SYNC event.

Overview (continued)

There are two different ways to use the digital delay.

1. Fixed Digital Delay - Allows all the outputs to have a known phase relationship upon a SYNC event. Typically performed at start-up.
2. Dynamic Digital Delay - Allows the phase relationships of clocks to change while clocks continue to operate.

9.1.9.4 SYSREF Delay

The global SYSREF divider includes a digital delay block which allows a global phase shift with respect to the other clocks.

Each local SYSREF clock output includes both an analog and additional local digital delay for unique phase adjustment of each SYSREF clock.

The local analog delay allows for 150-ps steps.

The local digital delay and SYSREF_HS bit allows the each individual SYSREF output to be delayed from, 1.5 to 11 VCO cycles. The delay step can be as small as half the period of the clock distribution path by using the DCLKoutX_HS bit. For example, 2-GHz VCO frequency results in 250-ps coarse tuning steps.

9.1.9.5 Glitchless Half Step and Glitchless Analog Delay

The device clocks include a features to ensure glitchless operation of the half step and analog delay operations when enabled.

9.1.9.6 Programmable Output Formats

For increased flexibility, all LMK04828-EP device and SYSREF clock outputs (DCLKoutX and SDCLKoutY) can be programmed to an LVDS, HSDS, LVPECL, or LCPECL output type. The OSCout can be programmed to an LVDS, LVPECL, or LVCMOS output type.

Any LVPECL output type can be programmed to 1600-mVpp or 2000-mVpp amplitude levels. The 2000-mVpp LVPECL output type is a Texas Instruments proprietary configuration that produces a 2000-mVpp differential swing for compatibility with many data converters and is also known as 2VPECL.

LCPECL allows for DC-coupling SYSREF to low voltage converters.

9.1.9.7 Clock Output Synchronization

Using the SYNC input causes all active clock outputs to share a rising edge as programmed by fixed digital delay.

The SYNC event must occur for digital delay values to take effect.

9.1.10 0-Delay

The LMK04828-EP supports two types of 0-delay.

1. Cascaded 0-delay
2. Nested 0-delay

Cascaded 0-delay mode establishes a fixed deterministic phase relationship of the phase of the PLL2 input clock (OSCin) to the phase of a clock selected by the feedback mux. The 0-delay feedback may performed with an internal feedback from CLKout6, CLKout8, SYSREF, or with an external feedback loop into the FBCLKin port as selected by the FB_MUX. Because OSCin has a fixed deterministic phase relationship to the feedback clock, OSCout will also have a fixed deterministic phase relationship to the feedback clock. In this mode PLL1 input clock (CLKinX) also has a fixed deterministic phase relationship to PLL2 input clock (OSCin), this results in a fixed deterministic phase relationship between all clocks from CLKinX to the clock outputs.

Nested 0-delay mode establishes a fixed deterministic phase relationship of the phase of the PLL1 input clock (CLKinX) to the phase of a clock selected by the feedback mux. The 0-delay feedback may performed with an internal feedback from CLKout6, CLKout8, SYSREF, or with an external feedback loop into the FBCLKin port as selected by the FB_MUX.

Overview (continued)

Without using 0-delay mode there will be n possible fixed phase relationships from clock input to clock output depending on the clock output divide value.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

9.1.11 Status Pins

The LMK04828-EP provides status pins which can be monitored for feedback or in some cases used for input depending upon device programming. For example:

- The CLKin_SEL0 pin may indicate the LOS (loss-of-signal) for CLKin0.
- The CLKin_SEL1 pin may be an input for selecting the active clock input.
- The Status_LD1 pin may indicate if the device is locked.
- The Status_LD2 pin may indicate if PLL2 is locked.

The status pins can be programmed to a variety of other outputs including PLL divider outputs, combined PLL lock detect signals, PLL1 Vtune railing, readback, and so forth. Refer to the programming section of this data sheet for more information.

9.2 Functional Block Diagram

Figure 6 illustrate the complete LMK04828-EP block diagram.

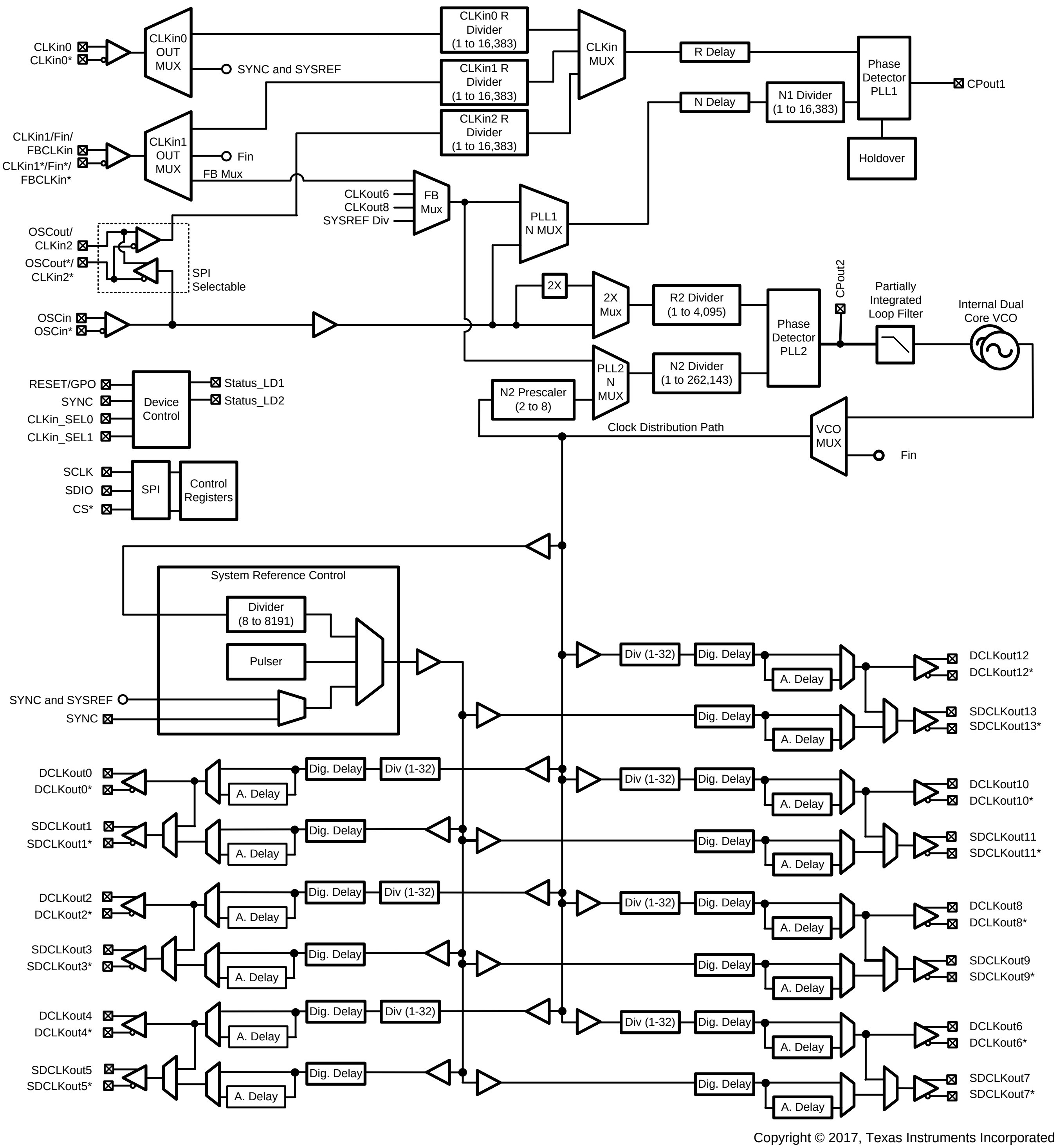


Figure 6. Detailed LMK04828-EP Block Diagram

Functional Block Diagram (continued)

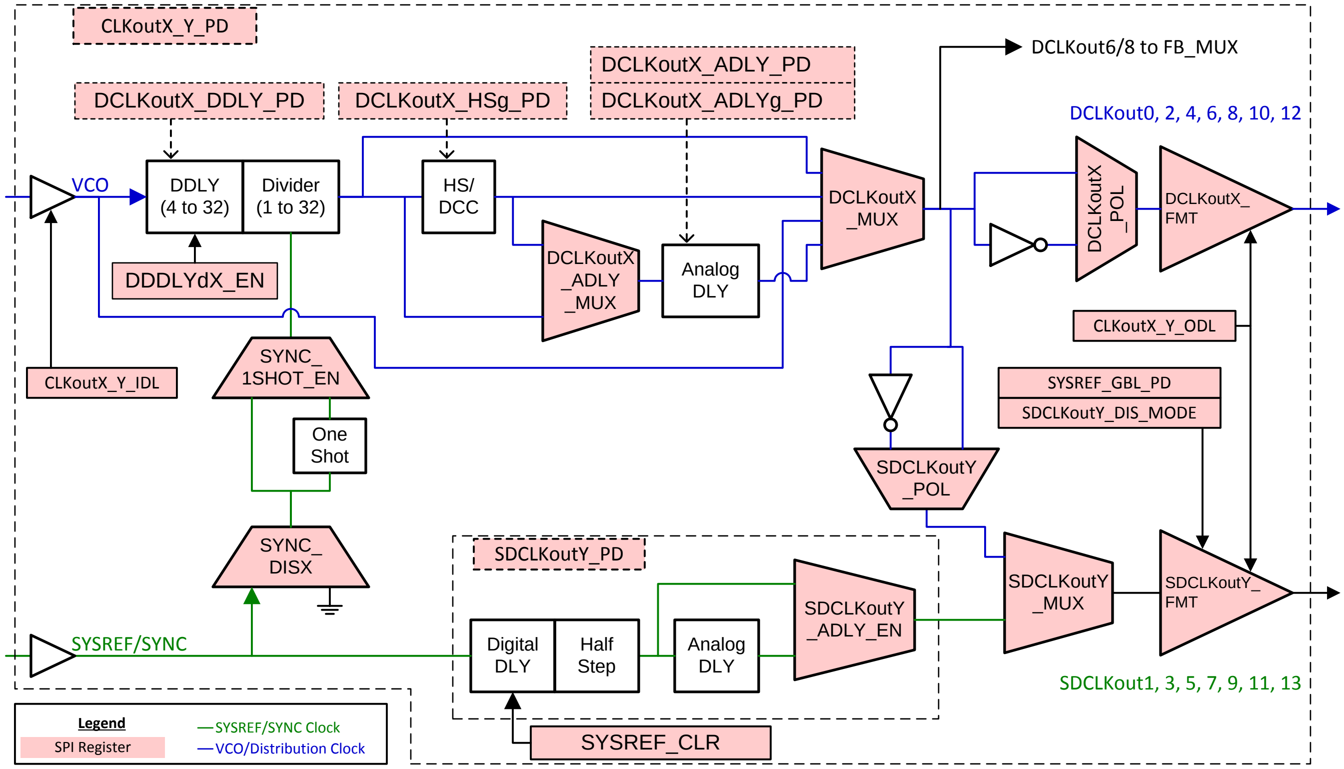


Figure 7. Device and SYSREF Clock Output Block

Functional Block Diagram (continued)

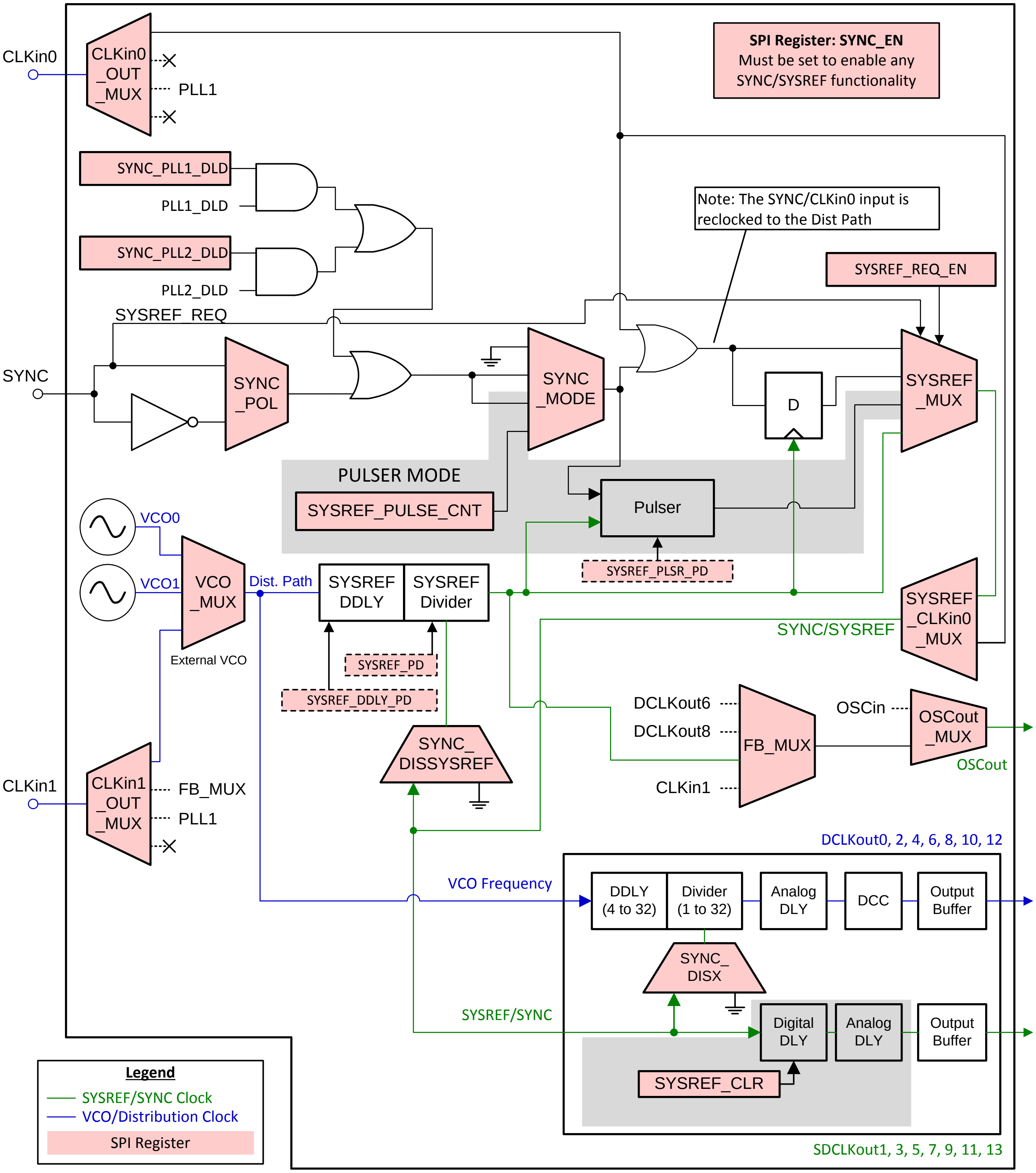


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Figure 8. SYNC/SYSREF Clocking Paths

9.3 Feature Description

9.3.1 SYNC/SYSREF

The SYNC and SYSREF signals share the same clocking path. To properly use SYNC or SYSREF for JESD204B, it is important to understand the SYNC and SYSREF system. Figure 7 illustrates the detailed diagram of a clock output block with SYNC circuitry included. Figure 8 illustrates the interconnects and highlights some important registers used in controlling the device for SYNC and SYSREF purposes.

To reset or synchronize a divider, the following conditions must be met:

1. SYNC_EN must be set. This ensures proper operation of the SYNC circuitry.
2. SYSREF_MUX and SYNC_MODE must be set to a proper combination to provide a valid SYNC or SYSREF signal.
   - If SYSREF block is being used, the SYSREF_PD bit must be clear.
   - If the SYSREF Pulser is being used, the SYSREF_PLSR_PD bit must be clear.
   - For each SDCLKoutY being used for SYSREF, respective SDCLKoutY_PD bits must be cleared.
3. SYSREF_DDLY_PD and DCLKoutX_DDLY_PD bits must be clear to power up the digital delay circuitry during SYNC as use requires.
4. The SYNC_DISX bit must be clear to allow SYNC/SYSREF signal to divider circuit. The SYSREF_MUX register selects the SYNC source which resets the SYSREF and CLKoutX dividers provided the corresponding SYNC_DISX bit is clear.
5. Other bits which impact the operation of SYNC signal, such as SYNC_1SHOT_EN, may be set as desired.

Table 2 illustrates the some possible combinations of SYSREF_MUX and SYNC_MODE.

Table 2. Some Possible SYNC Configurations

NAME	SYNC_MODE	SYSREF_MUX	OTHER	DESCRIPTION
SYNC Disabled	0	0	CLKin0_OUT_MUX ≠ 0	No SYNC will occur.
Pin or SPI SYNC	1	0	CLKin0_OUT_MUX ≠ 0	Basic SYNC functionality, SYNC pin polarity is selected by SYNC_POL. To achieve SYNC through SPI, toggle the SYNC_POL bit.
Differential input SYNC	0 or 1	0 or 1	CLKin0_OUT_MUX = 0	Differential CLKin0 now operates as SYNC input.
JESD204B Pulser on pin transition	2	2	SYSREF_PULSE_CNT sets pulse count	Produce SYSREF_PULSE_CNT programmed number of pulses on pin transition. SYNC_POL can be used to cause SYNC via SPI.
JESD204B Pulser on SPI programming	3	2	SYSREF_PULSE_CNT sets pulse count	Programming SYSREF_PULSE_CNT register starts sending the number of pulses.
Re-clocked SYNC	1	1	SYSREF operational, SYSREF Divider as required for training frame size.	Allows precise SYNC for n-bit frame training patterns for non-JESD converters such as LM97600.
External SYSREF request	0	2	SYSREF_REQ_EN = 1 Pulser powered up	When SYNC pin is asserted, continuous SYSERF pulses occur. Turning on and off of the pulses is synchronized to prevent runt pulses from occurring on SYSREF.
Continuous SYSREF	X	3	SYSREF_PD = 0 SYSREF_DDLY_PD = 0 SYSREF_PLSR_PD = 1 (1)	Continuous SYSREF signal.

(1) SDCLKoutY_PD = 0 as required per SYSREF output. This applies to any SYNC or SYSREF output on SDCLKoutY when SDCLKoutY_MUX = 1 (SYSREF output)

Feature Description (continued)

Table 2. Some Possible SYNC Configurations (continued)

NAME	SYNC_MODE	SYSREF_MUX	OTHER	DESCRIPTION
Direct SYSREF distribution	0	0	CLKin0_OUT_MUX = 0 SDCLKoutY_DDLY = 0 (Local sysref DDLY bypassed) SYSREF_DDLY_PD = 1 SYSREF_PLSR_PD = 1 SYSREF_PD = 1.	A direct fan-out of SYSREF with no re-clocking to clock distribution path.

9.3.2 JEDEC JESD204B

9.3.2.1 How To Enable SYSREF

Table 3 summarizes the bits needed to make SYSREF functionality operational.

Table 3. SYSREF Bits

REGISTER	FIELD	VALUE	DESCRIPTION
0x140	SYSREF_PD	0	Must be clear, power-up SYSREF circuitry.
0x140	SYSREF_DDLY_PD	0	Must be clear to power-up digital delay circuitry during initial SYNC to ensure deterministic timing.
0x143	SYNC_EN	1	Must be set, enable SYNC.
0x143	SYSREF_CLR	1 → 0	Do not hold local SYSREF DDLY block in reset except at start. Anytime SYSREF_PD = 1 because of user programming or device RESET, it is necessary to set SYSREF_CLR for 15 VCO clock cycles to clear the local SYSREF digital delay. Once cleared, SYSREF_CLR must be cleared to allow SYSREF to operate.

Enabling JESD204B operation involves synchronizing all the clock dividers with the SYSREF divder, then configuring the actual SYSREF functionality.

9.3.2.1.1 Setup of SYSREF Example

The following procedure is a programming example for a system which is to operate with a 3000 MHz VCO frequency. Use DCLKout0 and DCLKout2 to drive converters at 1500 MHz. Use DCLKout4 to drive an FPGA at 150 MHz. Synchronize the converters and FPGA using a two SYSREF pulses at 10 MHz.

1. **Program registers 0x000 to 0x1fff as desired, but follow the *Recommended Programming Sequence* section for out-of-order registers. Key to prepare for SYSREF operations:**
   (a) Prepare for manual SYNC: SYNC_POL = 0, SYNC_MODE = 1, SYSREF_MUX = 0
   (b) Set up output dividers as per example: DCLKout0_DIV and DCLKout2_DIV = 2 for frequency of 1500 MHz. DCLKout4_DIV = 20 for frequency of 150 MHz.
   (c) Set up output dividers as per example: SYSREF_DIV = 300 for 10 MHz SYSREF
   (d) Set up SYSREF: SYSREF_PD = 0, SYSREF_DDLY_PD = 0, DCLKout0_DDLY_PD = 0, DCLKout2_DDLY_PD = 0, DCLKout4_DDLY_PD = 0, SYNC_EN = 1, SYSREF_PLSR_PD = 0, SYSREF_PULSE_CNT = 1 (2 pulses). SDCLKout1_PD = 0, SDCLKout3_PD = 0
   (e) Clear Local SYSREF DDLY: SYSREF_CLR = 1.
2. **Establish deterministic phase relationships between SYSREF and Device Clock for JESD204B:**
   (a) Set device clock and SYSREF divider digital delays: DCLKout0_DDLY_CNTH, DCLKout0_DDLY_CNTL, DCLKout2_DDLY_CNTH, DCLKout2_DDLY_CNTL, DCLKout4_DDLY_CNTH, DCLKout4_DDLY_CNTL, SYSREF_DDLY.
   (b) Set device clock digital delay half steps: DCLKout0_HS, DCLKout2_HS, DCLKout4_HS.
   (c) Set SYSREF clock digital delay as required to achieve known phase relationships: SDCLKout1_DDLY, SDCLKout3_DDLY, SDCLKout5_DDLY.
   (d) To allow SYNC to affect dividers: SYNC_DIS0 = 0, SYNC_DIS2 = 0, SYNC_DIS4 = 0, SYNC_DISSYSREF = 0
   (e) **Perform SYNC by toggling SYNC_POL = 1 then SYNC_POL = 0.**

3. **Disable SYNC from resetting these dividers** when the dividers are synchronized. It is not desired for SYSREF to reset the divider of the SYSREF or the dividers of the output clocks.
   (a) Prevent SYNC (SYSREF) from affecting dividers: SYNC_DIS0 = 1, SYNC_DIS2 = 1, SYNC_DIS4 = 1, SYNC_DISSYSREF = 1.
4. **Release reset of local SYSREF digital delay.**
   (a) SYSREF_CLR = 0. Note this bit needs to be set for only 15 VCO clocks after SYSREF_PD = 0.
5. **Set SYSREF operation**.
   (a) Allow pin SYNC event to start pulser: SYNC_MODE = 2.
   (b) Select pulser as SYSREF signal: SYSREF_MUX = 2.
6. **Complete!** Now asserting the SYNC pin, or toggling SYNC_POL will result in a series of two SYSREF pulses.

9.3.2.1.2 SYSREF_CLR

The local digital delay of the SDCLKout is implemented as a shift buffer. To ensure no unwanted pulses occur at this SYSREF output at start-up, when using SYSREF, users must clear the buffers by setting SYSREF_CLR = 1 for 15 VCO clock cycles. The SYSREF_CLR bit is set after a POR or software reset, so it must be cleared before the SYSREF output is used.

9.3.2.2 SYSREF Modes

9.3.2.2.1 SYSREF Pulser

This mode allows for the output of 1, 2, 4, or 8 SYSREF pulses for every SYNC pin event or SPI programming. This implements the gapped periodic functionality of the JEDEC JESD204B specification.

When in SYSREF Pulser mode, programming the field SYSREF_PULSE_CNT in register 0x13E results in the pulser sending the programmed number of pulses.

9.3.2.2.2 Continuous SYSREF

This mode allows for continuous output of the SYSREF clock.

Continuous operation of SYSREF is not recommended due to crosstalk from the SYSREF clock to device clock. JESD204B is designed to operate with a single burst of pulses to initialize the system at start-up after which it is theoretically not required to send another SYSREF because the system continues to operate with deterministic phases.

If continuous operation of SYSREF is required, consider using a SYSREF output from a non-adjacent output or SYSREF from the OSCout pin to minimize crosstalk.

9.3.2.2.3 SYSREF Request

This mode allows an external source to synchronously turn on or off a continuous stream of SYSREF pulses using pin 6, the SYNC/SYSREF_REQ pin.

Setup the mode by programming SYSREF_REQ_EN = 1 and SYSREF_MUX = 2 (Pulser). The pulser does not need to be powered for this mode of operation.

When the SYSREF_REQ pin is asserted, the SYSREF_MUX will synchronously be set to continuous mode providing continuous pulses at the SYSREF frequency until the SYSREF_REQ pin is un-asserted and the final SYSREF pulse will complete sending synchronously.

9.3.3 Digital Delay

Digital (coarse) delay allows a group of outputs to be delayed by 4 to 32 VCO cycles. The delay step can be as small as half the period of the VCO cycle by using the DCLKoutX_HS bit. There are two different ways to use the digital delay:

1. Fixed digital delay
2. Dynamic digital delay

In both delay modes, the regular clock divider is substituted with an alternative divide value. The substitute divide value consists of two values, DCLKoutX_DDLY_CNTH and DCLKoutX_DDLY_CNTL. The minimum _CNTH or _CNTL value is 2 and the maximum _CNTH or _CNTL value is 16. This results in a minimum alternative divide value of 4 and a maximum of 32.

9.3.3.1 Fixed Digital Delay

Fixed digital delay value takes effect on the clock outputs after a SYNC event. As such, the outputs are LOW for a while during the SYNC event. Applications that cannot accept clock breakup when adjusting digital delay should use dynamic digital delay.

9.3.3.1.1 Fixed Digital Delay Example

Assume the device already has the following initial configurations, and the application should delay DCLKout2 by one VCO cycle compared to DCLKout0.

- VCO frequency = 2949.12 MHz
- DCLKout0 = 368.64 MHz (DCLKout0_DIV = 8)
- DCLKout2 = 368.64 MHz (DCLKout2_DIV = 8)

The following steps should be followed

1. Set DCLKout0_DDLY_CNTH = 4 and DCLKout2_DDLY_CNTH = 4. First part of delay for each clock.
2. Set DCLKout0_DDLY_CNTL = 4 and DCLKout2_DDLY_CNTL = 5. Second part of delay for each clock.
3. Set DCLKout0_DDLY_PD = 0 and DCLKout2_DDLY_PD = 0. Power up the digital delay circuit.
4. Set SYNC_DIS0 = 0 and SYNC_DIS2 = 0. Allow the output to be synchronized.
5. Perform SYNC by asserting, then unasserting SYNC. Either by using SYNC_POL bit or the SYNC pin.
6. Now that the SYNC is complete, to save power it is allowable to power down DCLKout0_DDLY_PD = 1 and/or DCLKout2_DDLY_PD = 1.
7. Set SYNC_DIS0 = 1 and SYNC_DIS2 = 1. To prevent the output from being synchronized, very important for steady state operation when using JESD204B.

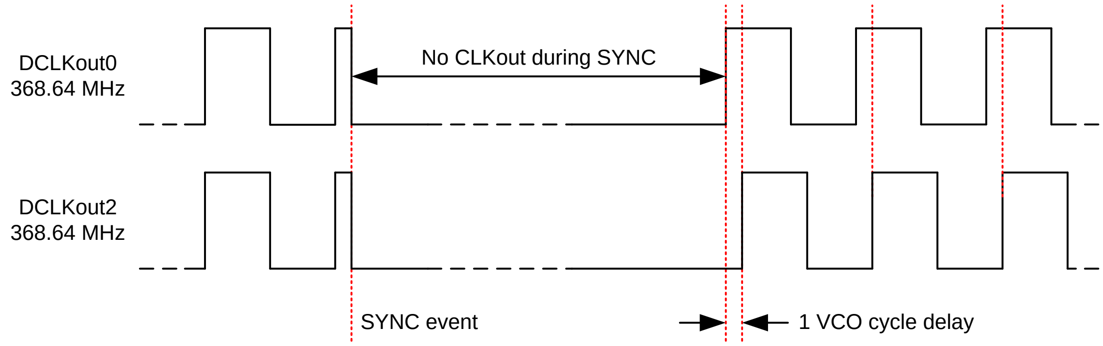


Figure 9. Fixed Digital Delay Example

9.3.3.2 Dynamic Digital Delay

Dynamic digital delay allows the phase of clocks to be changed with respect to each other with little impact to the clock signal. This is accomplished by substituting the regular clock divider with an alternate divide value for one cycle. This substitution occurs a number of times equal to the value programmed into the DDLYd_STEP_CNT field for all outputs with DDLYdX_EN = 1 or DDLYd_SYSREF_EN = 1 (see *DDLYd_SYSREF_EN, DDLYdX_EN*) and DCLKoutX_DDLY_PD = 0 or SYSREF_DDLY_PD = 0.

- By programming a larger alternate divider (delay) value, the phase of the adjusted outputs are delayed with respect to the other clocks.
- By programming a smaller alternate divider (delay) value, the phase of the adjusted output advances with respect to the other clocks.

NOTE

When programming DDLYd_STEP_CNT to execute more than one step adjustment, the output frequency of the lowest frequency divider having dynamic digital delay enabled must be greater than or equal to 50 MHz to ensure every programmed step is taken. If not, DDLYd_STEP_CNT must be programmed with single step adjustments. When programming back-to-back single DDLYd_STEP_CNT adjustments, wait 70 ns + period of slowest clock for which dynamic digital delay is enabled between DDLYd_STEP_CNT register programmings. This note typically only applies to dynamic digital delay adjustments on the SYSREF divider.

Table 4 shows the recommended DCLKoutX_DDLY_CNTH and DCLKoutX_DDLY_CNTL alternate divide setting for delay by one VCO cycle. The clock outputs high during the DCLKoutX_DDLY_CNTH time to permit a continuous output clock. The clock output is low during the DCLKoutX_DDLY_CNTL time.

When using dynamic digital delay, before the divider SYNC occurs, it is required to setup DCLKoutX_DDLY_CNTH/CNTL and DCLKoutX_DDLYd_CNTH/CNTL values to be the same. After a divider SYNC it is not permitted to change either of these values. If a different phase alignment is required that what is programmed, use the DDLYdX_EN/DDLYd_SYSREF_EN bits to toggle which dividers respond to a dynamic digital delay and execute dynamic digital delay adjustments so outputs have the required phase.

Table 4. Recommended DCLKoutX_DDLY_CNTH/_CNTL and DCLKoutX_DDLYd_CNTH/_CNTL Values for Delay by One VCO Cycle

CLOCK DIVIDER	_CNTH	_CNTL		CLOCK DIVIDER	_CNTH	_CNTL
2	2	3		17	9	9
3	3	4		18	9	10
4	2	3		19	10	10
5	3	3		20	10	11
6	3	4		21	11	11
7	4	4		22	11	12
8	4	5		23	12	12
9	5	5		24	12	13
10	5	6		25	13	13
11	6	6		26	13	14
12	6	7		27	14	14
13	7	7		28	14	15
14	7	8		29	15	15
15	8	8		30	15	16 (1)
16	8	9		31	16 (1)	16 (1)

(1) To achieve _CNTH/_CNTL value of 16, 0 must be programmed into the _CNTH/_CNTL field.

9.3.3.3 Single and Multiple Dynamic Digital Delay Example

In this example, two separate adjustments are made to the device clocks. In the first adjustment, a single delay of one VCO cycle occurs between DCLKout2 and DCLKout0. In the second adjustment, two delays of one VCO cycle occurs between DCLKout2 and DCLKout0. At this point in the example, DCLKout2 is delayed three VCO cycles behind DCLKout0.

Assuming the device already has the following initial configurations and has had the dividers synchronized:

- VCO frequency: 2949.12 MHz
- DCLKout0 = 368.64 MHz, DCLKout0_DIV = 8
- DCLKout2 = 368.64 MHz, DCLKout2_DIV = 8

The following steps illustrate the example above:

1. DCLKout2_DDLY_CNTH = 4 and DCLKout2_DDLYd_CNTH = 4. The delays of DCLKout2 and DCLKout0 are set before divider SYNC. Same settings were used for DLCKout0.

2. DCLKout2_DDLY_CNTL = 5 and DCLKout2_DDLYd_CNTL = 5. The delays of DCLKout2 and DCLKout0 are set before divider SYNC. Same settings were used for DLCKout0. Together with the high count, this gives a substituted divide of 9.

3. Set DCLKout2_DDLY_PD = 0 if not already powered up. This enable the digital delay for DCLKout2. Note it is required for the DDLY_PD = 0 during SYNC to ensure deterministic phase from the SYNC.

4. Set DDLYd2_EN = 1. Enable dynamic digital delay for DCLKout2.

5. Set DDLYd_STEP_CNT = 1. This begins the **first adjustment.**

Before step 5, DCLKout2 clock edge is aligned with DCLKout0.

After step 5, DCLKout2 counts four VCO cycles high and then five VCO cycles low as programmed by DCLKout2_DDLYd_CNTH and DCLKout2_DDLYd_CNTL fields, effectively delaying DCLKout2 by one VCO cycle with respect to DCLKout0. ***This is the first adjustment.***

6. Set DDLYd_STEP_CNT = 2. This begins the **second adjustment.**

Before step 6, DCLKout2 clock edge was delayed 1 VCO cycle from DCLKout0.

After step 6, DCLKout2 counts four VCO cycles high and then five VCO cycles low as programmed by DCLKout2_DDLYd_CNTH and DCLKout2_DDLYd_CNTL fields twice, but not necessarily back to back. In total this delays DCLKout2 by two VCO cycles with respect to DCLKout0. ***This is the second adjustment illustrating multi-step.***

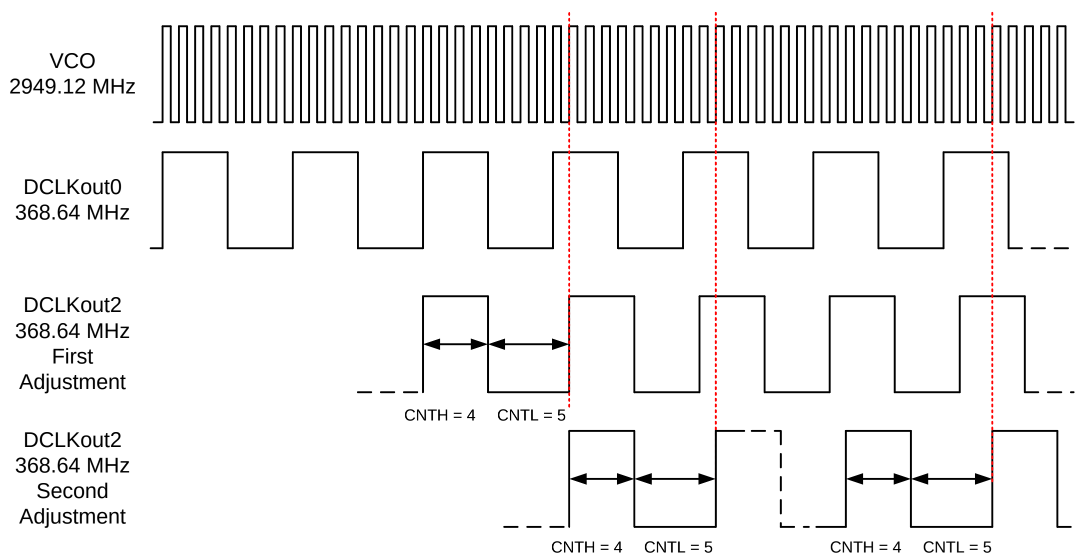


Figure 10. Single and Multiple Adjustment Dynamic Digital Delay Example

9.3.4 SYSREF to Device Clock Alignment

To ensure proper JESD204B operation, the timing relationship between the SYSREF and the Device clock must be adjusted for optimum setup and hold time. The $ts_{JESD204B}$ defines the time between SYSREF and Device Clock for a specific condition of SYSREF divider and Device Clock digital delay. From this point, the SYSREF_DDLY. SDCLKoutY_DDLY, DCLKoutX_DDLY_CNTH, DCLKoutDDLY_CNTL, and DCLKoutX_MUX, SDCKLoutX_ADLY, and so forth. can be adjusted to provide the required setup and hold time between SYSREF and Device Clock.

It is possible to digitally adjust the SYSREF up to 20 VCO cycles before the SYSREF. So for example with a 2949.12 MHz VCO frequency, $ts_{JESD204B}$ + 20 × (1/VCO Frequency) = –80 ps + 20 × (1/2949.12 MHz) = 6.7 ns.

9.3.5 Input Clock Switching

Manual, pin select, and automatic are three different kinds clock input switching modes can be set with the CLKin_SEL_MODE register.

Below is information about how the active input clock is selected and what causes a switching event in the various clock input selection modes.

9.3.5.1 Input Clock Switching - Manual Mode

When CLKin_SEL_MODE is 0, 1, or 2 then CLKin0, CLKin1, or CLKin2 respectively is always selected as the active input clock. Manual mode also overrides the EN_CLKinX bits such that the CLKinX buffer operates even if CLKinX is disabled with EN_CLKinX = 0.

If holdover is entered in this mode, then the device relocks to the selected CLKin upon holdover exit.

9.3.5.2 Input Clock Switching - Pin Select Mode

When CLKin_SEL_MODE is 3, the pins CLKin_SEL0 and CLKin_SEL1 select which clock input is active.

Configuring Pin Select Mode

The CLKin_SEL0_TYPE must be programmed to an input value for the CLKin_SEL0 pin to function as an input for pin select mode.

The CLKin_SEL1_TYPE must be programmed to an input value for the CLKin_SEL1 pin to function as an input for pin select mode.

If the CLKin_SELX_TYPE is set as output, the pin input value is considered LOW.

The polarity of CLKin_SEL0 and CLKin_SEL1 input pins can be inverted with the CLKin_SEL_INV bit.

Table 5 defines which input clock is active depending on CLKin_SEL0 and CLKin_SEL1 state.

Table 5. Active Clock Input - Pin Select Mode, CLKin_SEL_INV = 0

PIN CLKin_SEL1	PIN CLKin_SEL0	ACTIVE CLOCK
Low	Low	CLKin0
Low	High	CLKin1
High	Low	CLKin2
High	High	Holdover

The pin select mode overrides the EN_CLKinX bits such that the CLKinX buffer operates even if CLKinX is disabled with EN_CLKinX = 0. To switch as fast as possible, the clock input buffers (EN_CLKinX = 1) that could be switched to must remain enabled..

9.3.5.3 Input Clock Switching - Automatic Mode

When CLKin_SEL_MODE is 4, the active clock is selected in round-robin order of enabled clock inputs starting upon an input clock switch event. The switching order of the clocks is CLKin0 → CLKin1 → CLKin2 → CLKin0, and so forth.

For a clock input to be eligible to be switched through, it must be enabled using EN_CLKinX.

Starting Active Clock

Upon programming this mode, the currently active clock remains active if PLL1 lock detect is high. To ensure a particular clock input is the active clock when starting this mode, program CLKin_SEL_MODE to the manual mode which selects the desired clock input (CLKin0, 1, or 2). Wait for PLL1 to lock PLL1_DLD = 1, then select this mode with CLKin_SEL_MODE = 4.

9.3.6 Digital Lock Detect

Both PLL1 and PLL2 support digital lock detect. Digital lock detect compares the phase between the reference path (R) and the feedback path (N) of the PLL. When the time error, which is phase error, between the two signals is less than a specified window size (ε) a lock detect count increments. When the lock detect count reaches a user specified value, PLL1_DLD_CNT or PLL2_DLD_CNT, lock detect is asserted true. Once digital lock detect is true, a single phase comparison outside the specified window causes digital lock detect to be asserted false. This is illustrated in Figure 11.

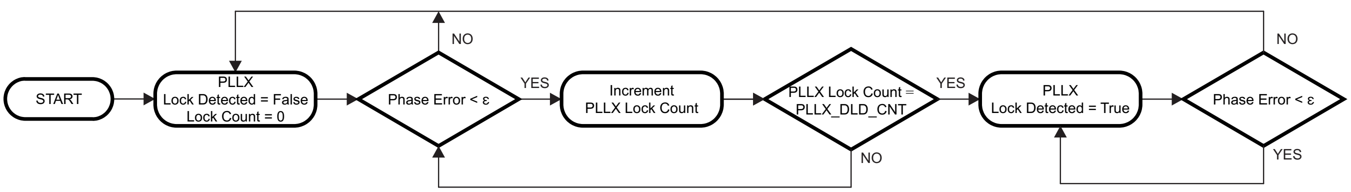


Figure 11. Digital Lock Detect Flowchart

This incremental lock detect count feature functions as a digital filter to ensure that lock detect isn't asserted for only a brief time when the phases of R and N are within the specified tolerance for only a brief time during initial phase lock.

See *Digital Lock Detect Frequency Accuracy* for more detailed information on programming the registers to achieve a specified frequency accuracy in ppm with lock detect.

The digital lock detect signal can be monitored on the Status_LD1 or Status_LD2 pin. The pin may be programmed to output the status of lock detect for PLL1, PLL2, or both PLL1 and PLL2.

9.3.6.1 Calculating Digital Lock Detect Frequency Accuracy

See *Digital Lock Detect Frequency Accuracy* for more detailed information on programming the registers to achieve a specified frequency accuracy in ppm with lock detect.

The digital lock detect feature can also be used with holdover to automatically exit holdover mode. See *Exiting Holdover* for more info.

9.3.7 Holdover

Holdover mode causes PLL2 to stay locked on frequency with minimal frequency drift when an input clock reference to PLL1 becomes invalid. While in holdover mode, the PLL1 charge pump is TRI-STATED and a fixed tuning voltage is set on CPout1 to operate PLL1 in open loop.

9.3.7.1 Enable Holdover

Program HOLDOVER_EN = 1 to enable holdover mode.

Holdover mode can be configured to set the CPout1 voltage upon holdover entry to a fixed user defined voltage or a tracked voltage.

9.3.7.1.1 Fixed (Manual) CPout1 Holdover Mode

By programming MAN_DAC_EN = 1, then the MAN_DAC value is set on the CPout1 pin during holdover.

The user can optionally enable CPout1 voltage tracking (TRACK_EN = 1), read back the tracked DAC value, then re-program MAN_DAC value to a user desired value based on information from previous DAC read backs. This allows the most user control over the holdover CPout1 voltage, but also requires more user intervention.

9.3.7.1.2 Tracked CPout1 Holdover Mode

By programming MAN_DAC_EN = 0 and TRACK_EN = 1, the tracked voltage of CPout1 is set on the CPout1 pin during holdover. When the DAC has acquired the current CPout1 voltage, the *DAC_Locked* signal is set which may be observed on Status_LD1 or Status_LD2 pins by programming PLL1_LD_MUX or PLL2_LD_MUX respectively.

Updates to the DAC value for the Tracked CPout1 sub-mode occurs at the rate of the PLL1 phase detector frequency divided by (DAC_CLK_MULT × DAC_CLK_CNTR).

The DAC update rate should be programmed for ≤ 100 kHz to ensure DAC holdover accuracy.

The ability to program slow DAC update rates, for example one DAC update per 4.08 seconds when using 1024 kHz PLL1 phase detector frequency with DAC_CLK_MULT = 16,384 and DAC_CLK_CNTR = 255, allows the device to *look-back* and set CPout1 at previous *good* CPout1 tuning voltage values before the event which caused holdover to occur.

The current voltage of DAC value can be read back using RB_DAC_VALUE, see *RB_DAC_VALUE* .

9.3.7.2 During Holdover

PLL1 is run in open loop mode.

- PLL1 charge pump is set to TRI-STATE.
- PLL1 DLD is un-asserted.
- The HOLDOVER status is asserted
- During holdover If PLL2 was locked prior to entry of holdover mode, PLL2 DLD continues to be asserted.
- CPout1 voltage is set to:
  – a voltage set in the MAN_DAC register (MAN_DAC_EN = 1).
  – a voltage determined to be the last valid CPout1 voltage (MAN_DAC_EN = 0).
- PLL1 attempts to lock with the active clock input.

The HOLDOVER status signal can be monitored on the Status_LD1 or Status_LD2 pin by programming the PLL1_DLD_MUX or PLL2_DLD_MUX register to *Holdover Status*.

9.3.7.3 Exiting Holdover

Holdover mode can be exited in one of two ways.

- Manually, by programming the device from the host.
- Automatically, By a clock operating within a specified ppm of the current PLL1 frequency on the active clock input.

9.3.7.4 Holdover Frequency Accuracy and DAC Performance

When in holdover mode, PLL1 runs in open-loop and the DAC sets the CPout1 voltage. If Fixed CPout1 mode is used, then the output of the DAC is a voltage dependant upon the MAN_DAC register. If Tracked CPout1 mode is used, then the output of the DAC is the voltage at the CPout1 pin before holdover mode was entered. When using Tracked mode and MAN_DAC_EN = 1, during holdover the DAC value is loaded with the programmed value in MAN_DAC, not the tracked value.

When in Tracked CPout1 mode, the DAC has a worst case tracking error of ±2 LSBs once PLL1 tuning voltage is acquired. The step size is approximately 3.2 mV, therefore the VCXO frequency error during holdover mode caused by the DAC tracking accuracy is ±6.4 mV × Kv, where Kv is the tuning sensitivity of the VCXO in use. Therefore, the accuracy of the system when in holdover mode in ppm is:

$$\text{Holdover accuracy (ppm)} = \frac{\pm 6.4\text{ mV} \times \text{Kv} \times 1\text{e}6}{\text{VCXO Frequency}} \quad (1)$$

Example: consider a system with a 19.2-MHz clock input, a 153.6-MHz VCXO with a Kv of 17 kHz/V. The accuracy of the system in holdover in ppm is:

$$\pm 0.71\text{ ppm} = \pm 6.4\text{ mV} \times 17\text{ kHz/V} \times 1\text{e}6 / 153.6\text{ MHz} \quad (2)$$

It is important to account for this frequency error when determining the allowable frequency error window to cause holdover mode to exit.

9.3.7.5 Holdover Mode - Automatic Exit of Holdover

The LMK048xx device can be programmed to automatically exit holdover mode when the accuracy of the frequency on the active clock input achieves a specified accuracy. The programmable variables include PLL1_WND_SIZE and HOLDOVER_DLD_CNT.

See *Digital Lock Detect Frequency Accuracy* to calculate the register values to cause holdover to automatically exit upon reference signal recovery to within a user specified ppm error of the holdover frequency.

It is possible for the time to exit holdover to vary because the condition for automatic holdover exit is for the reference and feedback signals to have a time/phase error less than a programmable value. Because it is possible for two clock signals to be very close in frequency but not close in phase, it may take a long time for the phases of the clocks to align themselves within the allowable time/phase error before holdover exits.

9.4 Device Functional Modes

The following section describes the settings to enable various modes of operation for the LMK04828-EP. See Figure 7 and Figure 8 for visual diagrams of each mode.

The LMK04828-EP is a flexible device that can be configured for many different use cases. The following simplified block diagrams help show the user the different use cases of the device.

9.4.1 DUAL PLL

Figure 12 illustrates the typical use case of the LMK04828-EP in dual loop mode. In dual loop mode the reference to PLL1 from CLKin0, CLKin1, or CLKin2. An external VCXO or tunable crystal is used to provide feedback for the first PLL and a reference to the second PLL. This first PLL cleans the jitter with the VCXO or low cost tunable crystal by using a narrow loop bandwidth. The VCXO or tunable crystal output may be buffered through the OSCout port. The VCXO or tunable crystal is used as the reference to PLL2 and may be doubled using the frequency doubler. The internal VCO drives up to seven divide/delay blocks which drive up to 14 clock outputs.

Hitless switching and holdover functionality are optionally available when the input reference clock is lost. Holdover works by fixing the tuning voltage of PLL1 to the VCXO or tunable crystal.

It is also possible to use an external VCO in place of the internal VCO of the PLL2. In this case one less CLKin is available as a reference.

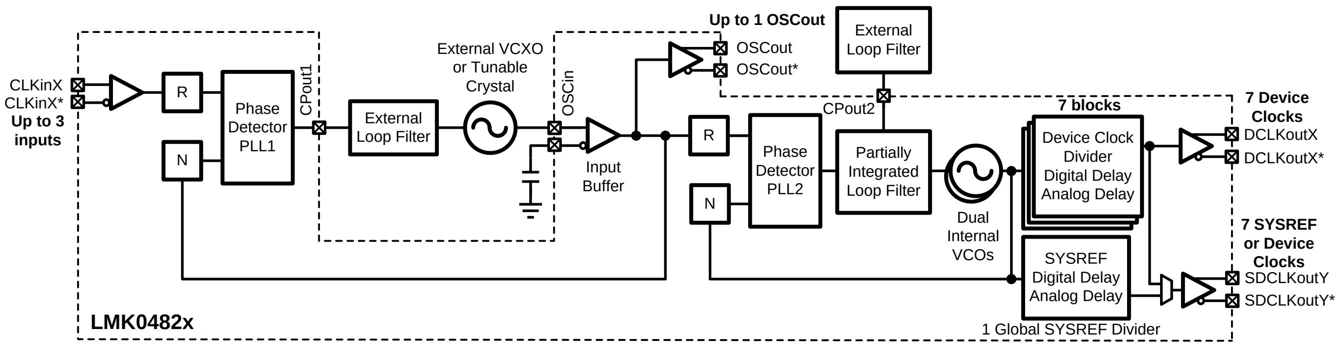


Figure 12. Simplified Functional Block Diagram for Dual Loop Mode

Table 6. Dual Loop Mode Register Configuration

FIELD	REGISTER ADDRESS	FUNCTION	VALUE	SELECTED VALUE
PLL1_NCLK_MUX	0x13F	Selects the input to the PLL1 N divider	0	OSCin
PLL2_NCLK_MUX	0x13F	Selects the input to the PLL2 N divider	0	PLL2_P
FB_MUX_EN	0x13F	Enables the Feedback Mux	0	Disabled
FB_MUX	0x13F	Selects the output of the Feedback Mux	X	Don't care because FB_MUX is disabled
OSCin_PD	0x140	Powers down the OSCin port	0	Powered up
CLKin0_OUT_MUX	0x147	Selects where the output of CLKin0 is directed.	2	PLL1
CLKin1_OUT_MUX	0x147	Selects where the output of CLKin1 is directed.	2	PLL1
VCO_MUX	0x138	Selects the VCO 0, 1, or an external VCO	0 or 1	VCO 0 or VCO 1

9.4.2 0-DELAY Dual PLL

Figure 13 illustrates the use case of cascaded 0-delay dual loop mode. This configuration differs from dual loop mode Figure 12 in that the feedback for PLL2 is driven by a clock output instead of the VCO output. Figure 14 illustrates the use case of nested 0-delay dual loop mode. This configuration is similar to the dual PLL in *DUAL PLL* except that the feedback to the first PLL is driven by a clock output. This causes the clock outputs to have deterministic phase relationship with the clock input. Since all the clock outputs can be synchronized together, all the clock outputs can share the same deterministic phase relationship with the clock input signal. The feedback to PLL1 can be connected internally as shown using CLKout6, CLKout8, SYSREF, or externally using FBCLKin (CLKin1).

It is also possible to use an external VCO in place of the internal VCO of PLL2, but one less CLKin is available as a reference and external 0-delay feedback is not available.

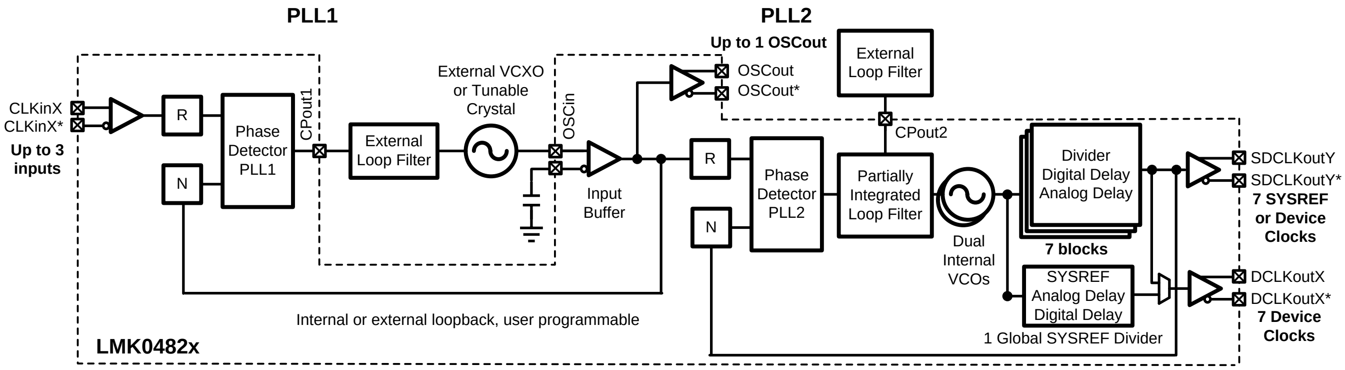


Figure 13. Simplified Functional Block Diagram for Cascaded 0-delay Dual Loop Mode

Table 7. Cascaded 0-delay Dual Loop Mode Register Configuration

FIELD	REGISTER ADDRESS	FUNCTION	VALUE	SELECTED VALUE
PLL1_NCLK_MUX	0x13F	Selects the input to the PLL1 N divider.	0	OSCin
PLL2_NCLK_MUX	0x13F	Selects the input to the PLL2 N divider	1	Feedback Mux
FB_MUX_EN	0x13F	Enables the Feedback Mux.	1	Feedback Mux Enabled
FB_MUX	0x13F	Selects the output of the Feedback Mux.	0, 1, or 2	Select between DCLKout6, DCLKout8, SYSREF
OSCin_PD	0x140	Powers down the OSCin port.	0	Powered up
CLKin0_OUT_MUX	0x147	Selects where the output of CLKin0 is directed.	0	PLL1
CLKin1_OUT_MUX	0x147	Selects where the output of CLKin1 is directed.	0 or 2	Fin or PLL1
VCO_MUX	0x138	Selects the VCO 0, 1, or an external VCO	0 or 1	VCO 0 or VCO 1

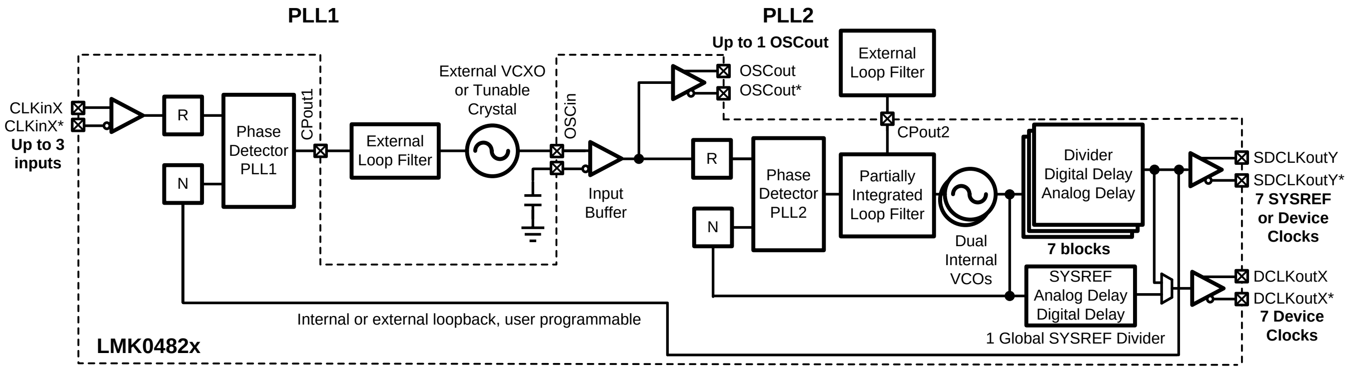


Figure 14. Simplified Functional Block Diagram for Nested 0-delay Dual Loop Mode

Table 8 illustrates nested 0-delay mode. This mode is the same as cascaded except the clock out feedback is to PLL1. The CLKin and CLKout have the same deterministic phase relationship but the VCXO's phase is not deterministic to the CLKin or CLKouts.

Table 8. Nested 0-delay Dual Loop Mode Register Configuration

FIELD	REGISTER ADDRESS	FUNCTION	VALUE	SELECTED VALUE
PLL1_NCLK_MUX	0x13F	Selects the input to the PLL1 N divider.	1	Feedback Mux
PLL2_NCLK_MUX	0x13F	Selects the input to the PLL2 N divider	0	PLL2 P
FB_MUX_EN	0x13F	Enables the Feedback Mux.	1	Enabled
FB_MUX	0x13F	Selects the output of the Feedback Mux.	0, 1, or 2	Select between DCLKout6, DCLKout8, SYSREF
OSCin_PD	0x140	Powers down the OSCin port.	0	Powered up
CLKin0_OUT_MUX	0x147	Selects where the output of CLKin0 is directed.	2	PLL1
CLKin1_OUT_MUX	0x147	Selects where the output of CLKin1 is directed.	0 or 2	Fin or PLL1
VCO_MUX	0x138	Selects the VCO 0, 1, or an external VCO	0 or 1	VCO 0 or VCO 1

9.5 Programming

LMK04828-EP devices are programmed using 24-bit registers. Each register consists of a 1-bit command field (R/W), a 2-bit multibyte field (W1, W0), a 13-bit address field (A12 to A0), and an 8-bit data field (D7 to D0). The contents of each register is clocked in MSB first (R/W), and the LSB (D0) last. During programming, the CS* signal is held low. The serial data is clocked in on the rising edge of the SCK signal. After the LSB is clocked in, the CS* signal goes *high* to latch the contents into the shift register. In general it is recommended to program registers in numeric order, for example 0x000 to 0x1FFF with exceptions as called out in *Recommended Programming Sequence*, to achieve proper device operation. This does not preclude the users ability to change single registers during operation.. Each register consists of one or more fields which control the device functionality. See electrical characteristics and Figure 1 for timing details.

R/W bit = 0 is for SPI write. R/W bit = 1 is for SPI read.

W1 and W0 shall be written as 0.

9.5.1 Recommended Programming Sequence

Registers are programmed in numeric order with 0x000 being the first and 0x1FFF being the last register programmed. The recommended programming sequence from POR involves:

1. Program register 0x000 with RESET = 1.
2. Program registers in numeric order from 0x000 to 0x165. Ensure the following register is programmed as follows:
   – 0x145 = 127 (0x7F)
3. Program register 0x171 to 0xAA and 0x172 to 0x02 as required by *OPT_REG_1* and *OPT_REG_2*.
4. Program registers 0x17C and 0x17D as required by *OPT_REG_1* and *OPT_REG_2*.
5. Program registers 0x166 to 0x1FFF.

Program register 0x171, 0x172, 0x17C (OPT_REG_1) and 0x17D (OPT_REG_2) before programming PLL2 in registers: 0x166, 0x167, and 0x168 to optimize PLL2_N and VCO1 phase noise performance over temperature.

9.5.1.1 SPI LOCK

When writing to SPI_LOCK, registers 0x1FFD, 0x1FFE, and 0x1FFF should all always be written sequentially.

9.5.1.2 SYSREF_CLR

When using SYSREF output, SYSREF local digital delay block should be cleared using SYSREF_CLR bit. See *SYSREF_CLR* for more infoormation.

9.6 Register Maps

9.6.1 Register Map for Device Programming

Table 9 provides the register map for device programming. Any register can be read from the same data address it is written to.

Table 9. LMK04828-EP Register Map

ADDRESS	DATA							
[11:0]	7	6	5	4	3	2	1	0
0x000	RESET	0	0	SPI_3WIRE_DIS	0	0	0	0
0x002	0	0	0	0	0	0	0	POWER DOWN
0x003	ID_DEVICE_TYPE							
0x004	ID_PROD[15:8]							
0x005	ID_PROD[7:0]							
0x006	ID_MASKREV							
0x00C	ID_VNDR[15:8]							
0x00D	ID_VNDR[7:0]							
0x100	0	CLKout0_1_ODL	CLKout0_1_IDL	DCLKout0_DIV				
0x101	DCLKout0_DDLY_CNTH				DCLKout0_DDLY_CNTL			
0x102	DCLKout0_DDLYd_CNTH				DCLKout0_DDLYd_CNTL			
0x103	DCLKout0_ADLY					DCLKout0_ADLY_MUX	DCLKout0_MUX	
0x104	0	DCLKout0_HS	SDCLKout1_MUX	SDCLKout1_DDLY				SDCLKout1_HS
0x105	0	0	0	SDCLKout1_ADLY_EN	SDCLKout1_ADLY			
0x106	DCLKout0_DDLY_PD	DCLKout0_HSg_PD	DCLKout0_ADLYg_PD	DCLKout0_ADLY_PD	CLKout0_1_PD	SDCLKout1_DIS_MODE		SDCLKout1_PD
0x107	SDCLKout1_POL	CLKout1_FMT			DCLKout0_POL	CLKout0_FMT		
0x108	0	CLKout2_3_ODL	CLKout2_3_IDL	DCLKout2_DIV				
0x109	DCLKout2_DDLY_CNTH				DCLKout2_DDLY_CNTL			
0x10A	DCLKout2_DDLYd_CNTH				DCLKout2_DDLYd_CNTL			
0x10B	DCLKout2_ADLY					DCLKout2_ADLY_MUX	DCLKout2_MUX	
0x10C	0	DCLKout2_HS	SDCLKout3_MUX	SDCLKout3_DDLY				SDCLKout3_HS
0x10D	0	0	0	SDCLKout3_ADLY_EN	SDCLKout3_ADLY			
0x10E	DCLKout2_DDLY_PD	DCLKout2_HSg_PD	DCLKout2_ADLYg_PD	DCLKout2_ADLY_PD	CLKout2_3_PD	SDCLKout3_DIS_MODE		SDCLKout3_PD
0x10F	SDCLKout3_POL	CLKout3_FMT			DCLKout2_POL	CLKout2_FMT		
0x110	0	CLKout4_5_ODL	CLKout4_5_IDL	DCLKout4_DIV				
0x111	DCLKout4_DDLY_CNTH				DCLKout4_DDLY_CNTL			
0x112	DCLKout4_DDLYd_CNTH				DCLKout4_DDLYd_CNTL			
0x113	DCLKout4_ADLY					DCLKout4_ADLY_MUX	DCLKout4_MUX	
0x114	0	DCLKout4_HS	SDCLKout5_MUX	SDCLKout5_DDLY				SDCLKout5_HS
0x115	0	0	0	SDCLKout5_ADLY_EN	SDCLKout5_ADLY			
0x116	DCLKout4_DDLY_PD	DCLKout4_HSg_PD	DCLKout4_ADLYg_PD	DCLKout4_ADLY_PD	CLKout4_5_PD	SDCLKout5_DIS_MODE		SDCLKout5_PD

Register Maps (continued)

Table 9. LMK04828-EP Register Map (continued)

ADDRESS [11:0]	DATA 7	6	5	4	3	2	1	0
0x117	SDCLKout5 _POL	CLKout5_FMT			DCLKout4 _POL	CLKout4_FMT		
0x118	0	CLKout6_7 _ODL	CLKout6_8 _IDL	DCLKout6_DIV				
0x119	DCLKout6_DDLY_CNTH				DCLKout6_DDLY_CNTL			
0x11A	DCLKout6_DDLYd_CNTH				DCLKout6_DDLYd_CNTL			
0x11B	DCLKout6_ADLY					DCLKout6_ ADLY_MUX	DCLKout6_MUX	
0x11C	0	DCLKout6 _HS	SDCLKout7 _MUX	SDCLKout7_DDLY				SDCLKout7 _HS
0x11D	0	0	0	SDCLKout7 _ ADLY_EN	SDCLKout7_ADLY			
0x11E	DCLKout6 _ DDLY_PD	DCLKout6 _ HSg_PD	DCLKout6 _ ADLYg_PD	DCLKout6 _ADLY _PD	CLKout6_7 _PD	SDCLKout7_DIS_MODE		SDCLKout7 _PD
0x11F	SDCLKout7 _POL	CLKout7 _FMT			DCLKout6 _POL	CLKout6_FMT		
0x120	0	CLKout8_9 _ODL	CLKout8_9 _IDL	DCLKout8_DIV				
0x121	DCLKout8_DDLY_CNTH				DCLKout8_DDLY_CNTL			
0x122	DCLKout8_DDLYd_CNTH				DCLKout8_DDLYd_CNTL			
0x123	DCLKout8_ADLY					DCLKout8 _ ADLY_MUX	DCLKout8_MUX	
0x124	0	DCLKout8 _HS	SDCLKout9 _MUX	SDCLKout9_DDLY				SDCLKout9 _HS
0x125	0	0	0	SDCLKout9 _ ADLY_EN	SDCLKout9_ADLY			
0x126	DCLKout8 _ DDLY_PD	DCLKout8 _ HSg_PD	DCLKout8 _ ADLYg_PD	DCLKout8 _ADLY _PD	CLKout8_9 _PD	SDCLKout9_DIS_MODE		SDCLKout9 _PD
0x127	SDCLKout9 _POL	CLKout9_FMT			DCLKout8 _POL	CLKout8_FMT		
0x128	0	CLKout10 _11 _ODL	CLKout10 _11_IDL	DCLKout10_DIV				
0x129	DCLKout10_DDLY_CNTH				DCLKout10_DDLY_CNTL			
0x12A	DCLKout10_DDLYd_CNTH				DCLKout10_DDLYd_CNTL			
0x12B	DCLKout10_ADLY					DCLKout10 _ ADLY_MUX	DCLKout10_MUX	
0x12C	0	DCLKout10 _HS	SDCLKout11 _MUX	SDCLKout11_DDLY				SDCLKout11 _HS
0x12D	0	0	0	SDCKLout11 _ ADLY_EN	SDCLKout11_ADLY			
0x12E	DCLKout10 _ DDLY_PD	DCLKout10 _ HSg_PD	DLCLKout10 _ ADLYg_PD	DCLKout10 _ ADLY_PD	CLKout10 _11_PD	SDCLKout11_DIS_MODE		SDCLKout11 _PD
0x12F	SDCLKout11 _POL	CLKout11_FMT			DCLKout10 _POL	CLKout10_FMT		
0x130	0	CLKout12 _13 _ODL	CLKout12 _13_IDL	DCLKout12_DIV				
0x131	DCLKout12_DDLY_CNTH				DCLKout12_DDLY_CNTL			
0x132	DCLKout12_DDLYd_CNTH				DCLKout12_DDLYd_CNTL			
0x133	DCLKout12_ADLY					DCLKout12_ ADLY_MUX	DCLKout12_MUX	
0x134	0	DCLKout12 _HS	SDCLKout13 _MUX	SDCLKout13_DDLY				SDCLKout13 _HS
0x135	0	0	0	SDCLKout13 _ ADLY_EN	SDCLKout13_ADLY			
0x136	DCLKout12 _ DDLY_PD	DCLKout12 _ HSg_PD	DCLKout12 _ ADLYg_PD	DCLKout12 _ ADLY_PD	CLKout12 _13_PD	SDCLKout13_DIS_MODE		SDCLKout13 _PD

Register Maps (continued)

Table 9. LMK04828-EP Register Map (continued)

ADDRESS	DATA							
[11:0]	7	6	5	4	3	2	1	0
0x137	SDCLKout13_POL	CLKout13_FMT			DCLKout12_POL	CLKout12_FMT		
0x138	0	VCO_MUX		OSCout_MUX	OSCout_FMT			
0x139	0	0	0	0	0	SYSREF_CLKin0_MUX	SYSREF_MUX	
0x13A	0	0	0	SYSREF_DIV[12:8]				
0x13B	SYSREF_DIV[7:0]							
0x13C	0	0	0	SYSREF_DDLY[12:8]				
0x13D	SYSREF_DDLY[7:0]							
0x13E	0	0	0	0	0	0	SYSREF_PULSE_CNT	
0x13F	0	0	0	PLL2_NCLK_MUX	PLL1_NCLK_MUX	FB_MUX		FB_MUX_EN
0x140	PLL1_PD	VCO_LDO_PD	VCO_PD	OSCin_PD	SYSREF_GBL_PD	SYSREF_PD	SYSREF_DDLY_PD	SYSREF_PLSR_PD
0x141	DDLYd_SYSREF_EN	DDLYd12_EN	DDLYd10_EN	DDLYd7_EN	DDLYd6_EN	DDLYd4_EN	DDLYd2_EN	DDLYd0_EN
0x142	0	0	0	DDLYd_STEP_CNT				
0x143	SYSREF_DDLY_CLR	SYNC_1SHOT_EN	SYNC_POL	SYNC_EN	SYNC_PLL2_DLD	SYNC_PLL1_DLD	SYNC_MODE	
0x144	SYNC_DISSYSREF	SYNC_DIS12	SYNC_DIS10	SYNC_DIS8	SYNC_DIS6	SYNC_DIS4	SYNC_DIS2	SYNC_DIS0
0x145	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**
0x146	0	0	CLKin2_EN	CLKin1_EN	CLKin0_EN	CLKin2_TYPE	CLKin1_TYPE	CLKin0_TYPE
0x147	CLKin_SEL_POL	CLKin_SEL_MODE			CLKin1_OUT_MUX		CLKin0_OUT_MUX	
0x148	0	0	CLKin_SEL0_MUX			CLKin_SEL0_TYPE		
0x149	0	SDIO_RDBK_TYPE	CLKin_SEL1_MUX			CLKin_SEL1_TYPE		
0x14A	0	0	RESET_MUX			RESET_TYPE		
0x14B	LOS_TIMEOUT		LOS_EN	TRACK_EN	HOLDOVER_FORCE	MAN_DAC_EN	MAN_DAC[9:8]	
0x14C	MAN_DAC[7:0]							
0x14D	0	0	DAC_TRIP_LOW					
0x14E	DAC_CLK_MULT		DAC_TRIP_HIGH					
0x14F	DAC_CLK_CNTR							
0x150	0	CLKin_OVERRIDE	0	HOLDOVER_PLL1_DET	HOLDOVER_LOS_DET	HOLDOVER_VTUNE_DET	HOLDOVER_HITLESS_SWITCH	HOLDOVER_EN
0x151	0	0	HOLDOVER_DLD_CNT[13:8]					
0x152	HOLDOVER_DLD_CNT[7:0]							
0x153	0	0	CLKin0_R[13:8]					
0x154	CLKin0_R[7:0]							
0x155	0	0	CLKin1_R[13:8]					
0x156	CLKin1_R[7:0]							
0x157	0	0	CLKin2_R[13:8]					
0x158	CLKin2_R[7:0]							
0x159	0	0	PLL1_N[13:8]					
0x15A	PLL1_N[7:0]							
0x15B	PLL1_WND_SIZE		PLL1_CP_TRI	PLL1_CP_POL	PLL1_CP_GAIN			
0x15C	0	0	PLL1_DLD_CNT[13:8]					
0x15D	PLL1_DLD_CNT[7:0]							

Register Maps (continued)

Table 9. LMK04828-EP Register Map (continued)

ADDRESS	DATA							
[11:0]	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x15E	0	0	PLL1_R_DLY			PLL1_N_DLY		
0x15F	PLL1_LD_MUX					PLL1_LD_TYPE		
0x160	0	0	0	0	PLL2_R[11:8]			
0x161	PLL2_R[7:0]							
0x162	PLL2_P			OSCin_FREQ			PLL2 _XTAL_EN	PLL2 _REF_2X_EN
0x163	0	0	0	0	0	0	PLL2_N_CAL[17:16]	
0x164	PLL2_N_CAL[15:8]							
0x165	PLL2_N_CAL[7:0]							
0x166	0	0	0	0	0	PLL2_FCAL _DIS	PLL2_N[17:16]	
0x167	PLL2_N[15:8]							
0x168	PLL2_N[7:0]							
0x169	0	PLL2_WND_SIZE		PLL2_CP_GAIN		PLL2 _CP_POL	PLL 2_CP_TRI	**1**
0x16A	0	SYSREF_REQ_ EN	PLL2_DLD_CNT[15:8]					
0x16B	PLL2_DLD_CNT[7:0]							
0x16C	0	0	PLL2_LF_R4			PLL2_LF_R3		
0x16D	PLL2_LF_C4				PLL2_LF_C3			
0x16E	PLL2_LD_MUX					PLL2_LD_TYPE		
0x171	**1**	0	**1**	0	**1**	0	**1**	0
0x172	0	0	0	0	0	0	**1**	0
0x173	0	PLL2_PRE_PD	PLL2_PD	0	0	0	0	0
0x174	0	0	0	VCO1_DIV				
0x17C	OPT_REG_1							
0x17D	OPT_REG_2							
0x182	0	0	0	0	0	RB_PLL1_ LD_LOST	RB_PLL1_LD	CLR_PLL1_ LD_LOST
0x183	0	0	0	0	0	RB_PLL2_ LD_LOST	RB_PLL2_LD	CLR_PLL2_ LD_LOST
0x184	RB_DAC_VALUE[9:8]		RB_CLKin2_ SEL	RB_CLKin1_ SEL	RB_CLKin0_ SEL	X	RB_CLKin1_ LOS	RB_CLKin0_ LOS
0x185	RB_DAC_VALUE[7:0]							
0x188	0	0	0	RB_ HOLDOVER	X	X	X	X
0x1FFD	SPI_LOCK[23:16]							
0x1FFE	SPI_LOCK[15:8]							
0x1FFF	SPI_LOCK[7:0]							

9.7 Device Register Descriptions

The following section details the fields of each register, the Power On Reset Defaults, and specific descriptions of each bit.

In some cases similar fields are located in multiple registers. In this case specific outputs may be designated as X or Y. In these cases, the X represents even numbers from 0 to 12 and the Y represents odd numbers from 1 to 13. In the case where X and Y are both used in a bit name, then Y = X + 1.

9.7.1 System Functions

9.7.1.1 RESET, SPI_3WIRE_DIS

This register contains the RESET function.

Table 10. Register 0x000

BIT	NAME	POR DEFAULT	DESCRIPTION
7	RESET	0	0: Normal Operation 1: Reset (automatically cleared)
6:5	NA	0	Reserved
4	SPI_3WIRE_DIS	0	Disable 3 wire SPI mode. 4 Wire SPI mode is enabled by selecting SPI Read back in one of the output MUX settings. For example CLKin0_SEL_MUX. 0: 3 Wire Mode enabled 1: 3 Wire Mode disabled
3:0	NA	NA	Reserved

9.7.1.2 POWERDOWN

This register contains the POWERDOWN function.

Table 11. Register 0x002

BIT	NAME	POR DEFAULT	DESCRIPTION
7:1	NA	0	Reserved
0	POWERDOWN	0	0: Normal Operation 1: Powerdown

9.7.1.3 ID_DEVICE_TYPE

This register contains the product device type. This is read only register.

Table 12. Register 0x003

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	ID_DEVICE_TYPE	6	PLL product device type.

9.7.1.4 ID_PROD[15:8], ID_PROD

These registers contain the product identifier. This is a read only register.

Table 13. ID_PROD Register Configuration, ID_PROD[15:0]

MSB	LSB
0x004[7:0]	0x005[7:0]

BIT	REGISTERS	FIELD NAME	POR DEFAULT	DESCRIPTION
7:0	0x004	ID_PROD[15:8]	208	MSB of the product identifier.
7:0	0x005	ID_PROD	91	LSB of the product identifier.

9.7.1.5 ID_MASKREV

This register contains the IC version identifier. This is a read only register.

Table 14. Register 0x006

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	ID_MASKREV	32	IC version identifier for LMK04828-EP

9.7.1.6 ID_VNDR[15:8], ID_VNDR

These registers contain the vendor identifier. This is a read only register.

Table 15. ID_VNDR Register Configuration, ID_VNDR[15:0]

MSB	LSB
0x00C[7:0]	0x00D[7:0]

Table 16. Registers 0x00C, 0x00D

BIT	REGISTERS	NAME	POR DEFAULT	DESCRIPTION
7:0	0x00C	ID_VNDR[15:8]	81	MSB of the vendor identifier.
7:0	0x00D	ID_VNDR	4	LSB of the vendor identifier.

9.7.2 (0x100 - 0x138) Device Clock and SYSREF Clock Output Controls

9.7.2.1 CLKoutX_Y_ODL, CLKoutX_Y_IDL, DCLKoutX_DIV

These registers control the input and output drive level as well as the device clock out divider values.

Table 17. Registers 0x100, 0x108, 0x110, 0x118, 0x120, 0x128, and 0x130

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	NA	0	Reserved	
6	CLKoutX_Y_ODL	0	Output drive level.	
5	CLKoutX_Y_IDL	0	Input drive level.	
4:0	DCLKoutX_DIV	X = 0 → 2 X = 2 → 4 X = 4 → 8 X = 6 → 8 X = 8 → 8 X = 10 → 8 X = 12 → 2	DCLKoutX_DIV sets the divide value for the clock output, the divide may be even or odd. Both even or odd divides output a 50% duty cycle clock if duty cycle correction (DCC) is selected. Divider is unused if DCLKoutX_MUX = 2 (bypass), equivalent divide of 1.	
			Field Value	**Divider Value**
			0 (0x00)	32
			1 (0x01)	1 (1)
			2 (0x02)	2
			...	...
			30 (0x1E)	30
			31 (0x1F)	31

(1) Not valid if DCLKoutX_MUX = 0, Divider only. Not valid if DCLKoutX_MUX = 3 (Analog Delay + Divider) and DCLKoutX_ADLY_MUX = 0 (without duty cycle correction/halfstep).

9.7.2.2 DCLKoutX_DDLY_CNTH, DCLKoutX_DDLY_CNTL

This register controls the digital delay high and low count values for the device clock outputs.

Table 18. Registers 0x101, 0x109, 0x111, 0x119, 0x121, 0x129, 0x131

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:4	DCLKoutX _DDLY_CNTH	5	Number of clock cycles the output will be high when digital delay is engaged.	
			Field Value	**Delay Values**
			0 (0x00)	16
			1 (0x01)	Reserved
			2 (0x02)	2
			...	...
			15 (0x0F)	15
3:0	DCLKoutX _DDLY_CNTL	5	Number of clock cycles the output will be low when digital delay is engaged.	
			Field Value	**Delay Values**
			0 (0x00)	16
			1 (0x01)	Reserved
			2 (0x02)	2
			...	...
			15 (0x0F)	15

9.7.2.3 DCLKoutX_DDLYd_CNTH, DCLKoutX_DDLYd_CNTL

This register controls the digital delay high and low count values for the device clock outputs during dynamic digital delay. The corresponding DCLKoutX_DDLY_CNTH/CNTL registers must be programmed to the same value.

Table 19. Registers 0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:4	DCLKoutX _DDLYd_CNTH	5	Number of clock cycles the output will be high when dynamic digital delay is engaged.	
			Field Value	**Delay Values**
			0 (0x00)	16
			1 (0x01)	Reserved
			2 (0x02)	2
			...	...
			15 (0x0F)	15
3:0	DCLKoutX _DDLYd_CNTL	5	Number of clock cycles the output will be low when dynamic digital delay is engaged.	
			Field Value	**Delay Values**
			0 (0x00)	16
			1 (0x01)	Reserved
			2 (0x02)	2
			...	...
			15 (0x0F)	15

9.7.2.4 DCLKoutX_ADLY, DCLKoutX_ADLY_MUX, DCLKout_MUX

These registers control the analog delay properties for the device clocks.

Table 20. Registers 0x103, 0x10B, 0x113, 0x11B, 0x123, 0x12B, 0x133

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:3	DCLKoutX_ADLY	0	Device clock analog delay value. Setting this value results in a 500 ps timing delay in additional to the delay of each 25 ps step. Effective range is 500 ps to 1075 ps.	
			Field Value	**Delay Value**
			0 (0x00)	0 ps
			1 (0x01)	25 ps
			2 (0x02)	50 ps
			...	...
			23 (0x17)	575 ps
2	DCLKoutX_ADLY _MUX	0	This register selects the input to the analog delay for the device clock. Used when DCLKoutX_MUX = 3. 0: Divided without duty cycle correction or half step. (1) 1: Divided with duty cycle correction and half step.	
1:0	DCLKoutX_MUX	0	This selects the input to the device clock buffer.	
			Field Value	**Mux Output**
			0 (0x0)	Divider only (1)
			1 (0x1)	Divider with Duty Cycle Correction and Half Step
			2 (0x2)	Bypass
			3 (0x3)	Analog Delay + Divider

(1) DCLKoutX_DIV = 1 is not valid.

9.7.2.5 DCLKoutX_HS, SDCLKoutY_MUX, SDCLKoutY_DDLY, SDCLKoutY_HS

These registers set the half step for the device clock, the SYSREF output MUX, the SYSREF clock digital delay, and half step.

Table 21. Registers 0x104, 0x10C, 0x114, 0x11C, 0x124, 0x12C, 0x134

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td>6</td><td>DCLKoutX_HS</td><td>0</td><td colspan="2">Sets the device clock half step value. Half step must be zero (0) for a divide of 1.
0: 0 cycles
1: -0.5 cycles</td></tr>
<tr><td>5</td><td>SDCLKoutY_MUX</td><td>0</td><td colspan="2">Sets the input the the SDCLKoutY outputs.
0: Device clock output
1: SYSREF output</td></tr>
<tr><td rowspan="8">4:1</td><td rowspan="8">SDCLKoutY_DDLY</td><td rowspan="8">0</td><td colspan="2">Sets the number of VCO cycles to delay the SDCLKoutY by when SYSREF output is selected by SDCLKoutY_MUX.</td></tr>
<tr><td>Field Value</td><td>Delay Cycles</td></tr>
<tr><td>0 (0x00)</td><td>Bypass</td></tr>
<tr><td>1 (0x01)</td><td>2</td></tr>
<tr><td>2 (0x02)</td><td>3</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>10 (0x0A)</td><td>11</td></tr>
<tr><td>11 to 15 (0x0B to 0x0F)</td><td>Reserved</td></tr>
<tr><td>0</td><td>SDCLKoutY_HS</td><td>0</td><td colspan="2">Sets the SYSREF clock half step value.
0: 0 cycles
1: -0.5 cycles</td></tr>
</table>

9.7.2.6 SDCLKoutY_ADLY_EN, SDCLKoutY_ADLY

These registers set the analog delay parameters for the SYSREF outputs.

Table 22. Registers 0x105, 0x10D, 0x115, 0x11D, 0x125, 0x12D, 0x135

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:5	NA	0	Reserved	
4	SDCLKoutY _ADLY_EN	0	Enables analog delay for the SYSREF output. 0: Disabled 1: Enabled	
3:0	SDCLKoutY _ADLY	0	Sets the analog delay value for the SYSREF output. Selecting analog delay adds an additional 700 ps in propagation delay. Effective range is 700 ps to 2950 ps.	
			Field Value	**Delay Value**
			0 (0x0)	0 ps
			1 (0x1)	600 ps
			2 (0x2)	750 ps (+150 ps from 0x1)
			3 (0x3)	900 ps (+150 ps from 0x2)
			...	...
			14 (0xE)	2100 ps (+150 ps from 0xD)
			15 (0xF)	2250 ps (+150 ps from 0xE)

9.7.2.7 DCLKoutX_DDLY_PD, DCLKoutX_HSg_PD, DCLKout_ADLYg_PD, DCLKout_ADLY_PD, DCLKoutX_Y_PD, SDCLKoutY_DIS_MODE, SDCLKoutY_PD

This register controls the power down functions for the digital delay, glitchless half step, glitchless analog delay, analog delay, outputs, and SYSREF disable modes.

Table 23. Registers 0x106, 0x10E, 0x116, 0x11E, 0x126, 0x12E, 0x136

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>DCLKoutX
_DDLY_PD</td><td>0</td><td colspan="2">Powerdown the device clock digital delay circuitry.
0: Enabled
1: Powerdown</td></tr>
<tr><td>6</td><td>DCLKoutX
_HSg_PD</td><td>1</td><td colspan="2">Powerdown the device clock glitchless half step feature.
0: Enabled
1: Powerdown</td></tr>
<tr><td>5</td><td>DCLKoutX
_ADLYg_PD</td><td>1</td><td colspan="2">Powerdown the device clock glitchless analog delay feature.
0: Enabled, analog delay step size of one code is glitchless between values 1 to 23.
1: Powerdown</td></tr>
<tr><td>4</td><td>DCLKoutX
_ADLY_PD</td><td>1</td><td colspan="2">Powerdown the device clock analog delay feature.
0: Enabled
1: Powerdown</td></tr>
<tr><td>3</td><td>CLKoutX_Y_PD</td><td>X_Y = 0_1 → 1
X_Y = 2_3 → 1
X_Y = 4_5 → 0
X_Y = 6_7 → 0
X_Y = 8_9 → 0
X_Y = 10_11 → 0
X_Y = 12_13 → 1</td><td colspan="2">Powerdown the clock group defined by X and Y.
0: Enabled
1: Powerdown</td></tr>
<tr><td rowspan="6">2:1</td><td rowspan="6">SDCLKoutY
_DIS_MODE</td><td rowspan="6">0</td><td colspan="2">Configures the output state of the SYSREF</td></tr>
<tr><td>Field Value</td><td>Disable Mode</td></tr>
<tr><td>0 (0x00)</td><td>Active in normal operation</td></tr>
<tr><td>1 (0x01)</td><td>If SYSREF_GBL_PD = 1, the output is a logic low, otherwise it is active.</td></tr>
<tr><td>2 (0x02)</td><td>If SYSREF_GBL_PD = 1, the output is a nominal Vcm voltage[(1)], otherwise it is active.</td></tr>
<tr><td>3 (0x03)</td><td>Output is a nominal Vcm voltage[(1)]</td></tr>
<tr><td>0</td><td>SDCLKoutY_PD</td><td>1</td><td colspan="2">Powerdown SDCLKoutY and set to the state defined by SDCLKoutY_DIS_MODE</td></tr>
</table>

(1) If LVPECL mode is used with emitter resistors to ground, the output Vcm will be ~0 V, each pin will be ~0 V.

9.7.2.8 SDCLKoutY_POL, SDCLKoutY_FMT, DCLKoutX_POL, DCLKoutX_FMT

These registers configure the output polarity, and format.

Table 24. Registers 0x107, 0x10F, 0x117, 0x11F, 0x127, 0x12F, 0x137

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>SDCLKoutY_POL</td><td>0</td><td colspan="2">Sets the polarity of clock on SDCLKoutY when device clock output is selected with SDCLKoutY_MUX.
0: Normal
1: Inverted</td></tr>
<tr><td rowspan="10">6:4</td><td rowspan="10">SDCLKoutY_FMT</td><td rowspan="10">0</td><td colspan="2">Sets the output format of the SYSREF clocks</td></tr>
<tr><td>Field Value</td><td>Output Format</td></tr>
<tr><td>0 (0x00)</td><td>Powerdown</td></tr>
<tr><td>1 (0x01)</td><td>LVDS</td></tr>
<tr><td>2 (0x02)</td><td>HSDS 6 mA</td></tr>
<tr><td>3 (0x03)</td><td>HSDS 8 mA</td></tr>
<tr><td>4 (0x04)</td><td>HSDS 10 mA</td></tr>
<tr><td>5 (0x05)</td><td>LVPECL 1600 mV</td></tr>
<tr><td>6 (0x06)</td><td>LVPECL 2000 mV</td></tr>
<tr><td>7 (0x07)</td><td>LCPECL</td></tr>
<tr><td>3</td><td>DCLKoutX_POL</td><td>0</td><td colspan="2">Sets the polarity of the device clocks from the DCLKoutX outputs
0: Normal
1: Inverted</td></tr>
<tr><td rowspan="10">2:0</td><td rowspan="10">DCLKoutX_FMT</td><td rowspan="10">LMK04828-EP:
X = 0 → 0
X = 2 → 0
X = 4 → 1
X = 6 → 1
X = 8 → 1
X = 10 → 1
X = 12 → 0</td><td colspan="2">Sets the output format of the device clocks.</td></tr>
<tr><td>Field Value</td><td>Output Format</td></tr>
<tr><td>0 (0x00)</td><td>Powerdown</td></tr>
<tr><td>1 (0x01)</td><td>LVDS</td></tr>
<tr><td>2 (0x02)</td><td>HSDS 6 mA</td></tr>
<tr><td>3 (0x03)</td><td>HSDS 8 mA</td></tr>
<tr><td>4 (0x04)</td><td>HSDS 10 mA</td></tr>
<tr><td>5 (0x05)</td><td>LVPECL 1600 mV</td></tr>
<tr><td>6 (0x06)</td><td>LVPECL 2000 mV</td></tr>
<tr><td>7 (0x07)</td><td>LCPECL</td></tr>
</table>

9.7.3 SYSREF, SYNC, and Device Config

9.7.3.1 VCO_MUX, OSCout_MUX, OSCout_FMT

This register selects the clock distribution source, and OSCout parameters.

Table 25. Register 0x138

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	NA	0	Reserved	
6:5	VCO_MUX	0	Selects clock distribution path source from VCO0, VCO1, or CLKin (external VCO)	
			Field Value	**VCO Selected**
			0 (0x00)	VCO 0
			1 (0x01)	VCO 1
			2 (0x02)	CLKin1 (external VCO)
			3 (0x03)	Reserved
4	OSCout_MUX	0	Select the source for OSCout: 0: Buffered OSCin 1: Feedback Mux	
3:0	OSCout_FMT	4	Selects the output format of OSCout. When powered down, these pins may be used as CLKin2.	
			Field Value	**OSCout Format**
			0 (0x00)	Powerdown (CLKin2)
			1 (0x01)	LVDS
			2 (0x02)	Reserved
			3 (0x03)	Reserved
			4 (0x04)	LVPECL 1600 mVpp
			5 (0x05)	LVPECL 2000 mVpp
			6 (0x06)	LVCMOS (Norm / Inv)
			7 (0x07)	LVCMOS (Inv / Norm)
			8 (0x08)	LVCMOS (Norm / Norm)
			9 (0x09)	LVCMOS (Inv / Inv)
			10 (0x0A)	LVCMOS (Off / Norm)
			11 (0x0B)	LVCMOS (Off / Inv)
			12 (0x0C)	LVCMOS (Norm / Off)
			13 (0x0D)	LVCMOS (Inv / Off)
			14 (0x0E)	LVCMOS (Off / Off)

9.7.3.2 SYSREF_CLKin0_MUX, SYSREF_MUX

This register sets the source for the SYSREF outputs. Refer to Figure 8 and SYNC/SYSREF.

Table 26. Register 0x139

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:3</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">2</td><td rowspan="4">SYSREF_
CLKin0_MUX</td><td rowspan="4">0</td><td colspan="2">Selects the SYSREF output from SYSREF_MUX or CLKin0 direct</td></tr>
<tr><td>Field Value</td><td>SYSREF Source</td></tr>
<tr><td>0</td><td>SYSREF Mux</td></tr>
<tr><td>1</td><td>CLKin0 Direct (from CLKin0_OUT_MUX)</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">SYSREF_MUX</td><td rowspan="6">0</td><td colspan="2">Selects the SYSREF source.</td></tr>
<tr><td>Field Value</td><td>SYSREF Source</td></tr>
<tr><td>0 (0x00)</td><td>Normal SYNC</td></tr>
<tr><td>1 (0x01)</td><td>Re-clocked</td></tr>
<tr><td>2 (0x02)</td><td>SYSREF Pulser</td></tr>
<tr><td>3 (0x03)</td><td>SYSREF Continuous</td></tr>
</table>

9.7.3.3 SYSREF_DIV[12:8], SYSREF_DIV[7:0]

These registers set the value of the SYSREF output divider.

Table 27. Registers 0x13A, 0x13B

MSB	LSB
0x13A[4:0]	0x13B[7:0]

BIT	REGISTERS	NAME	POR DEFAULT	DESCRIPTION	
7:5	0x13A	NA	0	Reserved	
4:0	0x13A	SYSREF_DIV[12:8]	12	Divide value for the SYSREF outputs.	
				Field Value	**Divide Value**
				0x00 to 0x07	Reserved
				8 (0x08)	8
7:0	0x13B	SYSREF_DIV[7:0]	0	9 (0x09)	9
				...	...
				8190 (0x1FFE)	8190
				8191 (0X1FFF)	8191

9.7.3.4 SYSREF_DDLY[12:8], SYSREF_DDLY[7:0]

These registers set the delay of the SYSREF digital delay value.

Table 28. SYSREF Digital Delay Register Configuration, SYSREF_DDLY[12:0]

MSB	LSB
0x13C[4:0]	0x13D[7:0]

BIT	REGISTERS	NAME	POR DEFAULT	DESCRIPTION	
7:5	0x13C	NA	0	Reserved	
4:0	0x13C	SYSREF_DDLY[12:8]	0	Sets the value of the SYSREF digital delay.	
				Field Value	**Delay Value**
				0x00 to 0x07	Reserved
				8 (0x08)	8
7:0	0x13D	SYSREF_DDLY[7:0]	8	9 (0x09)	9
				...	...
				8190 (0x1FFE)	8190
				8191 (0X1FFF)	8191

9.7.3.5 SYSREF_PULSE_CNT

This register sets the number of SYSREF pulses if SYSREF is not in continuous mode. See *SYSREF_CLKin0_MUX, SYSREF_MUX* for further description of SYSREF's outputs.

Programming the register causes the specified number of pulses to be output if "SYSREF Pulses" is selected by SYSREF_MUX and SYSREF functionality is powered up.

Table 29. Register 0x13E

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:2	NA	0	Reserved	
1:0	SYSREF_PULSE_CNT	3	Sets the number of SYSREF pulses generated when not in continuous mode. See *SYSREF_CLKin0_MUX, SYSREF_MUX* for more information on SYSREF modes.	
			Field Value	**Number of Pulses**
			0 (0x00)	1 pulse
			1 (0x01)	2 pulses
			2 (0x02)	4 pulses
			3 (0x03)	8 pulses

9.7.3.6 PLL2_NCLK_MUX, PLL1_NCLK_MUX, FB_MUX, FB_MUX_EN

This register controls the feedback feature.

Table 30. Register 0x13F

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:5	NA	0	Reserved	
4	PLL2_NCLK_MUX	0	Selects the input to the PLL2 N Divider 0: PLL Prescaler 1: Feedback Mux	
3	PLL1_NCLK_MUX	0	Selects the input to the PLL1 N Delay. 0: OSCin 1: Feedback Mux	
2:1	FB_MUX	0	When in 0-delay mode, the feedback mux selects the clock output to be fed back into the PLL1 N Divider.	
			Field Value	**Source**
			0 (0x00)	DCLKout6
			1 (0x01)	DCLKout8
			2 (0x02)	SYSREF Divider
			3 (0x03)	External
0	FB_MUX_EN	0	When using 0-delay, FB_MUX_EN must be set to 1 power up the feedback mux. 0: Feedback mux powered down 1: Feedback mux enabled	

9.7.3.7 PLL1_PD, VCO_LDO_PD, VCO_PD, OSCin_PD, SYSREF_GBL_PD, SYSREF_PD, SYSREF_DDLY_PD, SYSREF_PLSR_PD

This register contains powerdown controls for OSCin and SYSREF functions.

Table 31. Register 0x140

BIT	NAME	POR DEFAULT	DESCRIPTION
7	PLL1_PD	0	Powerdown PLL1 0: Normal operation 1: Powerdown
6	VCO_LDO_PD	0	Powerdown VCO_LDO 0: Normal operation 1: Powerdown
5	VCO_PD	0	Powerdown VCO 0: Normal operation 1: Powerdown
4	OSCin_PD	0	Powerdown the OSCin port. 0: Normal operation 1: Powerdown
3	SYSREF_GBL_PD	0	Powerdown individual SYSREF outputs depending on the setting of SDCLKoutY_DIS_MODE for each SYSREF output. SYSREF_GBL_PD allows many SYSREF outputs to be controlled through a single bit. 0: Normal operation 1: Activate Powerdown Mode
2	SYSREF_PD	1	Powerdown the SYSREF circuitry and divider. If powered down, SYSREF output mode cannot be used. SYNC cannot be provided either. 0: SYSREF can be used as programmed by individual SYSREF output registers. 1: Powerdown
1	SYSREF_DDLY_PD	1	Powerdown the SYSREF digital delay circuitry. 0: Normal operation, SYSREF digital delay may be used. Must be powered up during SYNC for deterministic phase relationship with other clocks. 1: Powerdown
0	SYSREF_PLSR_PD	1	Powerdown the SYSREF pulse generator. 0: Normal operation 1: Powerdown

9.7.3.8 DDLYd_SYSREF_EN, DDLYdX_EN

This register enables dynamic digital delay for enabled device clocks and SYSREF when DDLYd_STEP_CNT is programmed.

Table 32. Register 0x141

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	DDLYd_SYSREF_EN	0	Enables dynamic digital delay on SYSREF outputs	0: Disabled 1: Enabled
6	DDLYd12_EN	0	Enables dynamic digital delay on DCLKout12	
5	DDLYd10_EN	0	Enables dynamic digital delay on DCLKout10	
4	DDLYd8_EN	0	Enables dynamic digital delay on DCLKout8	
3	DDLYd6_EN	0	Enables dynamic digital delay on DCLKout6	
2	DDLYd4_EN	0	Enables dynamic digital delay on DCLKout4	
1	DDLYd2_EN	0	Enables dynamic digital delay on DCLKout2	
0	DDLYd0_EN	0	Enables dynamic digital delay on DCLKout0	

9.7.3.9 DDLYd_STEP_CNT

This register sets the number of dynamic digital delay adjustments occur. Upon programming, the dynamic digital delay adjustment begins for each clock output with dynamic digital delay enabled. Dynamic digital delay can only be started by SPI.

Other registers must be set: SYNC_MODE = 3

Table 33. Register 0x142

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:4	NA	0	Reserved	
3:0	DDLYd_STEP_CNT	0	Sets the number of dynamic digital delay adjustments that will occur.	
			Field Value	**SYNC Generation**
			0 (0x00)	No Adjust
			1 (0x01)	1 step
			2 (0x02)	2 steps
			3 (0x03)	3 steps
			...	...
			14 (0x0E)	14 steps
			15 (0x0F)	15 steps

9.7.3.10 SYSREF_CLR, SYNC_1SHOT_EN, SYNC_POL, SYNC_EN, SYNC_PLL2_DLD, SYNC_PLL1_DLD, SYNC_MODE

This register sets general SYNC parameters such as polarization, and mode. Refer to Figure 8 for block diagram. Refer to Table 2 for using SYNC_MODE for specific SYNC use cases.

Table 34. Register 0x143

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>SYSREF_CLR</td><td>1</td><td colspan="2">Except during SYSREF Setup Procedure (see SYNC/SYSREF), this bit should always be programmed to 0. While this bit is set, extra current is used. Refer to Table 85.</td></tr>
<tr><td>6</td><td>SYNC_1SHOT_EN</td><td>0</td><td colspan="2">SYNC one shot enables edge sensitive SYNC.
0: SYNC is level sensitive and outputs will be held in SYNC as long as SYNC is asserted.
1: SYNC is edge sensitive, outputs will be SYNCed on rising edge of SYNC. This results in the clock being held in SYNC for a minimum amount of time.</td></tr>
<tr><td>5</td><td>SYNC_POL</td><td>0</td><td colspan="2">Sets the polarity of the SYNC pin.
0: Normal
1: Inverted</td></tr>
<tr><td>4</td><td>SYNC_EN</td><td>1</td><td colspan="2">Enables the SYNC functionality.
0: Disabled
1: Enabled</td></tr>
<tr><td>3</td><td>SYNC_PLL2_DLD</td><td>0</td><td colspan="2">0: Off
1: Assert SYNC until PLL2 DLD = 1</td></tr>
<tr><td>2</td><td>SYNC_PLL1_DLD</td><td>0</td><td colspan="2">0: Off
1: Assert SYNC until PLL1 DLD = 1</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">SYNC_MODE</td><td rowspan="6">1</td><td colspan="2">Sets the method of generating a SYNC event.</td></tr>
<tr><th>Field Value</th><th>SYNC Generation</th></tr>
<tr><td>0 (0x00)</td><td>Prevent SYNC Pin, SYNC_PLL1_DLD flag, or SYNC_PLL2_DLD flag from generating a SYNC event.</td></tr>
<tr><td>1 (0x01)</td><td>SYNC event generated from SYNC pin or if enabled the SYNC_PLL1_DLD flag or SYNC_PLL2_DLD flag.</td></tr>
<tr><td>2 (0x02)</td><td>For use with pulser - SYNC/SYSREF pulses are generated by pulser block via SYNC Pin or if enabled SYNC_PLL1_DLD flag or SYNC_PLL2_DLD flag.</td></tr>
<tr><td>3 (0x03)</td><td>For use with pulser - SYNC/SYSREF pulses are generated by pulser block when programming register 0x13E (SYSREF_PULSE_CNT) is written to (see).</td></tr>
</table>

9.7.3.11 SYNC_DISSYSREF, SYNC_DISX

SYNC_DISX will prevent a clock output from being synchronized or interrupted by a SYNC event or when outputting SYSREF.

Table 35. Register 0x144

BIT	NAME	POR DEFAULT	DESCRIPTION
7	SYNC_DISSYSREF	0	Prevent the SYSREF clocks from becoming synchronized during a SYNC event. If SYNC_DISSYSREF is enabled it will continue to operate normally during a SYNC event.
6	SYNC_DIS12	0	Prevent the device clock output from becoming synchronized during a SYNC event or SYSREF clock. If SYNC_DIS bit for a particular output is enabled then it will continue to operate normally during a SYNC event or SYSREF clock.
5	SYNC_DIS10	0	
4	SYNC_DIS8	0	
3	SYNC_DIS6	0	
2	SYNC_DIS4	0	
1	SYNC_DIS2	0	
0	SYNC_DIS0	0	

9.7.3.12 Fixed Register

Always program this register to value 127.

Table 36. Register 0x145

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	Fixed Register	0	Always program to 127

9.7.4 (0x146 - 0x149) CLKin Control

9.7.4.1 CLKin2_EN, CLKin1_EN, CLKin0_EN, CLKin2_TYPE, CLKin1_TYPE, CLKin0_TYPE

This register has CLKin enable and type controls.

Table 37. Register 0x146

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:6</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td>5</td><td>CLKin2_EN</td><td>0</td><td colspan="2">Enable CLKin2 to be used during auto-switching of CLKin_SEL_MODE.
0: Not enabled for auto mode
1: Enabled for auto mode</td></tr>
<tr><td>4</td><td>CLKin1_EN</td><td>1</td><td colspan="2">Enable CLKin1 to be used during auto-switching of CLKin_SEL_MODE.
0: Not enabled for auto mode
1: Enabled for auto mode</td></tr>
<tr><td>3</td><td>CLKin0_EN</td><td>1</td><td colspan="2">Enable CLKin0 to be used during auto-switching of CLKin_SEL_MODE.
0: Not enabled for auto mode
1: Enabled for auto mode</td></tr>
<tr><td>2</td><td>CLKin2_TYPE</td><td>0</td><td rowspan="3">0: Bipolar
1: MOS</td><td rowspan="3">There are two buffer types for CLKin0, 1, and 2: bipolar and CMOS.
Bipolar is recommended for differential inputs like LVDS or LVPECL.
CMOS is recommended for DC-coupled, single-ended inputs.
When using bipolar, CLKinX and CLKinX* must be AC-coupled.
When using CMOS, CLKinX and CLKinX* may be AC- or DC-coupled if the input signal is differential. If the input signal is single-ended the used input may be either AC- or DC-coupled and the unused input must AC grounded.</td></tr>
<tr><td>1</td><td>CLKin1_TYPE</td><td>0</td></tr>
<tr><td>0</td><td>CLKin0_TYPE</td><td>0</td></tr>
</table>

9.7.4.2 CLKin_SEL_POL, CLKin_SEL_MODE, CLKin1_OUT_MUX, CLKin0_OUT_MUX

Table 38. Register 0x147

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>CLKin_SEL_POL</td><td>0</td><td colspan="2">Inverts the CLKin polarity for use in pin select mode.
0: Active High
1: Active Low</td></tr>
<tr><td rowspan="10">6:4</td><td rowspan="10">CLKin_SEL_MODE</td><td rowspan="10">3</td><td colspan="2">Sets the mode used in determining the reference for PLL1.</td></tr>
<tr><td>Field Value</td><td>CLKin Mode</td></tr>
<tr><td>0 (0x00)</td><td>CLKin0 Manual</td></tr>
<tr><td>1 (0x01)</td><td>CLKin1 Manual</td></tr>
<tr><td>2 (0x02)</td><td>CLKin2 Manual</td></tr>
<tr><td>3 (0x03)</td><td>Pin Select Mode</td></tr>
<tr><td>4 (0x04)</td><td>Auto Mode</td></tr>
<tr><td>5 (0x05)</td><td>Reserved</td></tr>
<tr><td>6 (0x06)</td><td>Reserved</td></tr>
<tr><td>7 (0x07)</td><td>Reserved</td></tr>
<tr><td rowspan="6">3:2</td><td rowspan="6">CLKin1_OUT_MUX</td><td rowspan="6">2</td><td colspan="2">Selects where the output of the CLKin1 buffer is directed.</td></tr>
<tr><td>Field Value</td><td>CLKin1 Destination</td></tr>
<tr><td>0 (0x00)</td><td>Fin</td></tr>
<tr><td>1 (0x01)</td><td>Feedback Mux (0-delay mode)</td></tr>
<tr><td>2 (0x02)</td><td>PLL1</td></tr>
<tr><td>3 (0x03)</td><td>Off</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">CLKin0_OUT_MUX</td><td rowspan="6">2</td><td colspan="2">Selects where the output of the CLKin0 buffer is directed.</td></tr>
<tr><td>Field Value</td><td>CLKin0 Destination</td></tr>
<tr><td>0 (0x00)</td><td>SYSREF Mux</td></tr>
<tr><td>1 (0x01)</td><td>Reserved</td></tr>
<tr><td>2 (0x02)</td><td>PLL1</td></tr>
<tr><td>3 (0x03)</td><td>Off</td></tr>
</table>

9.7.4.3 CLKin_SEL0_MUX, CLKin_SEL0_TYPE

This register has CLKin_SEL0 controls.

Table 39. Register 0x148

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>7:6</td><td>NA</td><td>0</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="10">5:3</td><td rowspan="10">CLKin_SEL0_MUX</td><td rowspan="10">0</td><td colspan="3">This set the output value of the CLKin_SEL0 pin. This register only applies if CLKin_SEL0_TYPE is set to an output mode</td></tr>
<tr><td>Field Value</td><td colspan="2">Output Format</td></tr>
<tr><td>0 (0x00)</td><td colspan="2">Logic Low</td></tr>
<tr><td>1 (0x01)</td><td colspan="2">CLKin0 LOS</td></tr>
<tr><td>2 (0x02)</td><td colspan="2">CLKin0 Selected</td></tr>
<tr><td>3 (0x03)</td><td colspan="2">DAC Locked</td></tr>
<tr><td>4 (0x04)</td><td colspan="2">DAC Low</td></tr>
<tr><td>5 (0x05)</td><td colspan="2">DAC High</td></tr>
<tr><td>6 (0x06)</td><td colspan="2">SPI Readback</td></tr>
<tr><td>7 (0x07)</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="9">2:0</td><td rowspan="9">CLKin_SEL0_TYPE</td><td rowspan="9">2</td><td colspan="3">This sets the IO type of the CLKin_SEL0 pin.</td></tr>
<tr><td>Field Value</td><td>Configuration</td><td>Function</td></tr>
<tr><td>0 (0x00)</td><td>Input</td><td rowspan="3">Input mode, see Input Clock Switching - Pin Select Mode for description of input mode.</td></tr>
<tr><td>1 (0x01)</td><td>Input /w pull-up resistor</td></tr>
<tr><td>2 (0x02)</td><td>Input /w pull-down resistor</td></tr>
<tr><td>3 (0x03)</td><td>Output (push-pull)</td><td rowspan="4">Output modes; the CLKin_SEL0_MUX register for description of outputs.</td></tr>
<tr><td>4 (0x04)</td><td>Output inverted (push-pull)</td></tr>
<tr><td>5 (0x05)</td><td>Reserved</td></tr>
<tr><td>6 (0x06)</td><td>Output (open drain)</td></tr>
</table>

9.7.4.4 SDIO_RDBK_TYPE, CLKin_SEL1_MUX, CLKin_SEL1_TYPE

This register has CLKin_SEL1 controls and register readback SDIO pin type.

Table 40. Register 0x149

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>7</td><td>NA</td><td>0</td><td colspan="3">Reserved</td></tr>
<tr><td>6</td><td>SDIO_RDBK_TYPE</td><td>1</td><td colspan="3">Sets the SDIO pin to open drain when during SPI readback in 3 wire mode.
0: Output, push-pull
1: Output, open drain.</td></tr>
<tr><td rowspan="10">5:3</td><td rowspan="10">CLKin_SEL1_MUX</td><td rowspan="10">0</td><td colspan="3">This set the output value of the CLKin_SEL1 pin. This register only applies if CLKin_SEL1_TYPE is set to an output mode.</td></tr>
<tr><td>Field Value</td><td colspan="2">Output Format</td></tr>
<tr><td>0 (0x00)</td><td colspan="2">Logic Low</td></tr>
<tr><td>1 (0x01)</td><td colspan="2">CLKin1 LOS</td></tr>
<tr><td>2 (0x02)</td><td colspan="2">CLKin1 Selected</td></tr>
<tr><td>3 (0x03)</td><td colspan="2">DAC Locked</td></tr>
<tr><td>4 (0x04)</td><td colspan="2">DAC Low</td></tr>
<tr><td>5 (0x05)</td><td colspan="2">DAC High</td></tr>
<tr><td>6 (0x06)</td><td colspan="2">SPI Readback</td></tr>
<tr><td>7 (0x07)</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="9">2:0</td><td rowspan="9">CLKin_SEL1_TYPE</td><td rowspan="9">2</td><td colspan="2">This sets the IO type of the CLKin_SEL1 pin.</td><td></td></tr>
<tr><td>Field Value</td><td>Configuration</td><td>Function</td></tr>
<tr><td>0 (0x00)</td><td>Input</td><td rowspan="3">Input mode, see Input Clock Switching - Pin Select Mode for description of input mode.</td></tr>
<tr><td>1 (0x01)</td><td>Input /w pull-up resistor</td></tr>
<tr><td>2 (0x02)</td><td>Input /w pull-down resistor</td></tr>
<tr><td>3 (0x03)</td><td>Output (push-pull)</td><td rowspan="4">Output modes; see the CLKin_SEL1_MUX register for description of outputs.</td></tr>
<tr><td>4 (0x04)</td><td>Output inverted (push-pull)</td></tr>
<tr><td>5 (0x05)</td><td>Reserved</td></tr>
<tr><td>6 (0x06)</td><td>Output (open drain)</td></tr>
</table>

9.7.5 RESET_MUX, RESET_TYPE

This register contains control of the RESET pin.

Table 41. Register 0x14A

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>7:6</td><td>NA</td><td>0</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="9">5:3</td><td rowspan="9">RESET_MUX</td><td rowspan="9">0</td><td colspan="3">This sets the output value of the RESET pin. This register only applies if RESET_TYPE is set to an output mode.</td></tr>
<tr><td>Field Value</td><td colspan="2">Output Format</td></tr>
<tr><td>0 (0x00)</td><td colspan="2">Logic Low</td></tr>
<tr><td>1 (0x01)</td><td colspan="2">Reserved</td></tr>
<tr><td>2 (0x02)</td><td colspan="2">CLKin2 Selected</td></tr>
<tr><td>3 (0x03)</td><td colspan="2">DAC Locked</td></tr>
<tr><td>4 (0x04)</td><td colspan="2">DAC Low</td></tr>
<tr><td>5 (0x05)</td><td colspan="2">DAC High</td></tr>
<tr><td>6 (0x06)</td><td colspan="2">SPI Readback</td></tr>
<tr><td rowspan="9">2:0</td><td rowspan="9">RESET_TYPE</td><td rowspan="9">2</td><td colspan="3">This sets the IO type of the RESET pin.</td></tr>
<tr><td>Field Value</td><td>Configuration</td><td>Function</td></tr>
<tr><td>0 (0x00)</td><td>Input</td><td rowspan="3">Reset Mode
Reset pin high = Reset</td></tr>
<tr><td>1 (0x01)</td><td>Input /w pull-up resistor</td></tr>
<tr><td>2 (0x02)</td><td>Input /w pull-down resistor</td></tr>
<tr><td>3 (0x03)</td><td>Output (push-pull)</td><td rowspan="4">Output modes; see the RESET_MUX register for description of outputs.</td></tr>
<tr><td>4 (0x04)</td><td>Output inverted (push-pull)</td></tr>
<tr><td>5 (0x05)</td><td>Reserved</td></tr>
<tr><td>6 (0x06)</td><td>Output (open drain)</td></tr>
</table>

9.7.6 (0x14B - 0x152) Holdover

9.7.6.1 LOS_TIMEOUT, LOS_EN, TRACK_EN, HOLDOVER_FORCE, MAN_DAC_EN, MAN_DAC[9:8]

This register contains the holdover functions.

Table 42. Register 0x14B

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">LOS_TIMEOUT</td><td rowspan="6">0</td><td colspan="2">This controls the amount of time in which no activity on a CLKin forces a clock switch event.</td></tr>
<tr><td>Field Value</td><td>Timeout</td></tr>
<tr><td>0 (0x00)</td><td>370 kHz</td></tr>
<tr><td>1 (0x01)</td><td>2.1 MHz</td></tr>
<tr><td>2 (0x02)</td><td>8.8 MHz</td></tr>
<tr><td>3 (0x03)</td><td>22 MHz</td></tr>
<tr><td>5</td><td>LOS_EN</td><td>0</td><td colspan="2">Enables the LOS (Loss-of-Signal) timeout control. Valid for MOS clock inputs.
0: Disabled
1: Enabled</td></tr>
<tr><td>4</td><td>TRACK_EN</td><td>1</td><td colspan="2">Enable the DAC to track the PLL1 tuning voltage, optionally for use in holdover mode. After device reset, tracking starts at DAC code = 512.
Tracking can be used to monitor PLL1 voltage in any mode.
0: Disabled
1: Enabled, will only track when PLL1 is locked.</td></tr>
<tr><td>3</td><td>HOLDOVER _FORCE</td><td>0</td><td colspan="2">This bit forces holdover mode. When holdover mode is forced, if MAN_DAC_EN = 1, then the DAC will set the programmed MAN_DAC value. Otherwise the tracked DAC value will set the DAC voltage.
0: Disabled
1: Enabled.</td></tr>
<tr><td>2</td><td>MAN_DAC_EN</td><td>1</td><td colspan="2">This bit enables the manual DAC mode.
0: Automatic
1: Manual</td></tr>
<tr><td>1:0</td><td>MAN_DAC[9:8]</td><td>2</td><td colspan="2">See MAN_DAC[9:8], MAN_DAC[7:0] for more information on the MAN_DAC settings.</td></tr>
</table>

9.7.6.2 MAN_DAC[9:8], MAN_DAC[7:0]

These registers set the value of the DAC in holdover mode when used manually.

Table 43. MAN_DAC[9:0]

MSB	LSB
0x14B[1:0]	0x14C[7:0]

<table>
<tr><th>BIT</th><th>REGISTERS</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:2</td><td>0x14B</td><td></td><td></td><td colspan="2">See LOS_TIMEOUT, LOS_EN, TRACK_EN, HOLDOVER_FORCE, MAN_DAC_EN, MAN_DAC[9:8] for information on these bits.</td></tr>
<tr><td rowspan="4">1:0</td><td rowspan="4">0x14B</td><td rowspan="4">MAN_DAC[9:8]</td><td rowspan="4">2</td><td colspan="2">Sets the value of the manual DAC when in manual DAC mode.</td></tr>
<tr><td>Field Value</td><td>DAC Value</td></tr>
<tr><td>0 (0x00)</td><td>0</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td rowspan="4">7:0</td><td rowspan="4">0x14C</td><td rowspan="4">MAN_DAC[7:0]</td><td rowspan="4">0</td><td>2 (0x02)</td><td>2</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>1022 (0x3FE)</td><td>1022</td></tr>
<tr><td>1023 (0x3FF)</td><td>1023</td></tr>
</table>

9.7.6.3 DAC_TRIP_LOW

This register contains the high value at which holdover mode is entered.

Table 44. Register 0x14D

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:6</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="10">5:0</td><td rowspan="10">DAC_TRIP_LOW</td><td rowspan="10">0</td><td colspan="2">Voltage from GND at which holdover is entered if HOLDOVER_VTUNE_DET is enabled.</td></tr>
<tr><td>Field Value</td><td>DAC Trip Value</td></tr>
<tr><td>0 (0x00)</td><td>1 x Vcc / 64</td></tr>
<tr><td>1 (0x01)</td><td>2 x Vcc / 64</td></tr>
<tr><td>2 (0x02)</td><td>3 x Vcc / 64</td></tr>
<tr><td>3 (0x03)</td><td>4 x Vcc / 64</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>61 (0x17)</td><td>62 x Vcc / 64</td></tr>
<tr><td>62 (0x18)</td><td>63 x Vcc / 64</td></tr>
<tr><td>63 (0x19)</td><td>64 x Vcc / 64</td></tr>
</table>

9.7.6.4 DAC_CLK_MULT, DAC_TRIP_HIGH

This register contains the multiplier for the DAC clock counter and the low value at which holdover mode is entered.

Table 45. Register 0x14E

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">DAC_CLK_MULT</td><td rowspan="6">0</td><td colspan="2">This is the multiplier for the DAC_CLK_CNTR which sets the rate at which the DAC value is tracked.</td></tr>
<tr><td>Field Value</td><td>DAC Multiplier Value</td></tr>
<tr><td>0 (0x00)</td><td>4</td></tr>
<tr><td>1 (0x01)</td><td>64</td></tr>
<tr><td>2 (0x02)</td><td>1024</td></tr>
<tr><td>3 (0x03)</td><td>16384</td></tr>
<tr><td rowspan="10">5:0</td><td rowspan="10">DAC_TRIP_HIGH</td><td rowspan="10">0</td><td colspan="2">Voltage from Vcc at which holdover is entered if HOLDOVER_VTUNE_DET is enabled.</td></tr>
<tr><td>Field Value</td><td>DAC Trip Value</td></tr>
<tr><td>0 (0x00)</td><td>1 x Vcc / 64</td></tr>
<tr><td>1 (0x01)</td><td>2 x Vcc / 64</td></tr>
<tr><td>2 (0x02)</td><td>3 x Vcc / 64</td></tr>
<tr><td>3 (0x03)</td><td>4 x Vcc / 64</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>61 (0x17)</td><td>62 x Vcc / 64</td></tr>
<tr><td>62 (0x18)</td><td>63 x Vcc / 64</td></tr>
<tr><td>63 (0x19)</td><td>64 x Vcc / 64</td></tr>
</table>

9.7.6.5 DAC_CLK_CNTR

This register contains the value of the DAC when in tracked mode.

Table 46. Register 0x14F

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="10">7:0</td><td rowspan="10">DAC_CLK_CNTR</td><td rowspan="10">127</td><td colspan="2">This with DAC_CLK_MULT set the rate at which the DAC is updated. The update rate is = DAC_CLK_MULT * DAC_CLK_CNTR / PLL1 PDF</td></tr>
<tr><td>Field Value</td><td>DAC Value</td></tr>
<tr><td>0 (0x00)</td><td>0</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td>2 (0x02)</td><td>2</td></tr>
<tr><td>3 (0x03)</td><td>3</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>253 (0xFD)</td><td>253</td></tr>
<tr><td>254 (0xFE)</td><td>254</td></tr>
<tr><td>255 (0xFF)</td><td>255</td></tr>
</table>

9.7.6.6 CLKin_OVERRIDE, HOLDOVER_PLL1_DET, HOLDOVER_LOS_DET, HOLDOVER_VTUNE_DET, HOLDOVER_HITLESS_SWITCH, HOLDOVER_EN

This register has controls for enabling clock in switch events.

Table 47. Register 0x150

BIT	NAME	POR DEFAULT	DESCRIPTION
7	NA	0	Reserved
6	CLKin _OVERRIDE	0	When CLKin_SEL_MODE = 0/1/2 to select a manual clock input, CLKin_OVERRIDE = 1 will force that clock input. Used with clock distribution mode for best performance. 0: Normal, no override. 1: Force select of only CLKin0/1/2 as specified by CLKin_SEL_MODE in manual mode.
5	NA	0	Reserved
4	HOLDOVER _PLL1_DET	0	This enables the HOLDOVER when PLL1 lock detect signal transitions from high to low. 0: PLL1 DLD does not cause a clock switch event 1: PLL1 DLD causes a clock switch event
3	HOLDOVER _LOS_DET	0	This enables HOLDOVER when PLL1 LOS signal is detected. 0: Disabled 1: Enabled
2	HOLDOVER _VTUNE_DET	0	Enables the DAC Vtune rail detections. When the DAC achieves a specified Vtune, if this bit is enabled, the current clock input is considered invalid and an input clock switch event is generated. 0: Disabled 1: Enabled
1	HOLDOVER _HITLESS _SWITCH	1	Determines whether a clock switch event will enter holdover use hitless switching. 0: Hard Switch 1: Hitless switching (has an undefined switch time)
0	HOLDOVER_EN	1	Sets whether holdover mode is active or not. 0: Disabled 1: Enabled

9.7.6.7 HOLDOVER_DLD_CNT[13:8], HOLDOVER_DLD_CNT[7:0]

Table 48. HOLDOVER_DLD_CNT[13:0]

MSB	LSB
0x151[5:0]	0x152[7:0]

This register has the number of valid clocks of PLL1 PDF before holdover is exited.

Table 49. Registers 0x151 and 0x152

<table>
<tr><th>BIT</th><th>REGISTERS</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:6</td><td>0x151</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">5:0</td><td rowspan="4">0x151</td><td rowspan="4">HOLDOVER _DLD_CNT[13:8]</td><td rowspan="4">2</td><td colspan="2">The number of valid clocks of PLL1 PDF before holdover mode is exited.</td></tr>
<tr><td>Field Value</td><td>Count Value</td></tr>
<tr><td>0 (0x00)</td><td>0</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td rowspan="4">7:0</td><td rowspan="4">0x152</td><td rowspan="4">HOLDOVER _DLD_CNT[7:0]</td><td rowspan="4">0</td><td>2 (0x02)</td><td>2</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>16382 (0x3FFE)</td><td>16382</td></tr>
<tr><td>16383 (0x3FFF)</td><td>16383</td></tr>
</table>

9.7.7 (0x153 - 0x15F) PLL1 Configuration

9.7.7.1 CLKin0_R[13:8], CLKin0_R[7:0]

Table 50. CLKin0_R[13:0]

MSB	LSB
0x153[5:0]	0x154[7:0]

These registers contain the value of the CLKin0 divider.

BIT	REGISTERS	NAME	POR DEFAULT	DESCRIPTION	
7:6	0x153	NA	0	Reserved	
5:0	0x153	CLKin0_R[13:8]	0	The value of PLL1 N counter when CLKin0 is selected.	
				Field Value	**Divide Value**
				0 (0x00)	Reserved
				1 (0x01)	1
7:0	0x154	CLKin0_R[7:0]	120	2 (0x02)	2
				...	...
				16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383

9.7.7.2 CLKin1_R[13:8], CLKin1_R[7:0]

Table 51. CLKin1_R[13:0]

MSB	LSB
0x155[5:0]	0x156[7:0]

These registers contain the value of the CLKin1 R divider.

Table 52. Registers 0x155 and 0x156

BIT	REGISTERS	NAME	POR DEFAULT	DESCRIPTION	
7:6	0x155	NA	0	Reserved	
5:0	0x155	CLKin1_R[13:8]	0	The value of PLL1 N counter when CLKin1 is selected.	
				Field Value	**Divide Value**
				0 (0x00)	Reserved
				1 (0x01)	1
7:0	0x156	CLKin1_R[7:0]	150	2 (0x02)	2
				...	...
				16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383

9.7.7.3 CLKin2_R[13:8], CLKin2_R[7:0]

MSB	LSB
0x157[5:0]	0x158[7:0]

Table 53. Registers 0x157 and 0x158

BIT	REGISTERS	NAME	POR DEFAULT	DESCRIPTION	
7:6	0x157	NA	0	Reserved	
5:0	0x157	CLKin2_R[13:8]	0	The value of PLL1 N counter when CLKin2 is selected.	
				Field Value	**Divide Value**
				0 (0x00)	Reserved
				1 (0x01)	1
7:0	0x158	CLKin2_R[7:0]	150	2 (0x02)	2
				...	...
				16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383

9.7.7.4 PLL1_N

Table 54. PLL1_N[13:8], PLL1_N[7:0]

PLL1_N[13:0]	
MSB	**LSB**
0x159[5:0]	0x15A[7:0]

These registers contain the N divider value for PLL1.

Table 55. Registers 0x159 and 0x15A

BIT	REGISTERS	NAME	POR DEFAULT	DESCRIPTION	
7:6	0x159	NA	0	Reserved	
5:0	0x159	PLL1_N[13:8]	0	The value of PLL1 N counter.	
				Field Value	**Divide Value**
				0 (0x00)	Not Valid
				1 (0x01)	1
7:0	0x15A	PLL1_N[7:0]	120	2 (0x02)	2
				...	...
				4,095 (0xFFF)	4,095

9.7.7.5 PLL1_WND_SIZE, PLL1_CP_TRI, PLL1_CP_POL, PLL1_CP_GAIN

This register controls the PLL1 phase detector.

Table 56. Register 0x15B

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">PLL1_WND_SIZE</td><td rowspan="6">3</td><td colspan="2">PLL1_WND_SIZE sets the window size used for digital lock detect for PLL1. If the phase error between the reference and feedback of PLL1 is less than specified time, then the PLL1 lock counter increments.</td></tr>
<tr><td>Field Value</td><td>Definition</td></tr>
<tr><td>0 (0x00)</td><td>4 ns</td></tr>
<tr><td>1 (0x01)</td><td>9 ns</td></tr>
<tr><td>2 (0x02)</td><td>19 ns</td></tr>
<tr><td>3 (0x03)</td><td>43 ns</td></tr>
<tr><td>5</td><td>PLL1_CP_TRI</td><td>0</td><td colspan="2">This bit allows for the PLL1 charge pump output pin, CPout1, to be placed into TRI-STATE.
0: PLL1 CPout1 is active
1: PLL1 CPout1 is at TRI-STATE</td></tr>
<tr><td>4</td><td>PLL1_CP_POL</td><td>1</td><td colspan="2">PLL1_CP_POL sets the charge pump polarity for PLL1. Many VCXOs use positive slope. A positive slope VCXO increases output frequency with increasing voltage. A negative slope VCXO decreases output frequency with increasing voltage.
0: Negative Slope VCO/VCXO
1: Positive Slope VCO/VCXO</td></tr>
<tr><td rowspan="10">3:0</td><td rowspan="10">PLL1_CP_GAIN</td><td rowspan="10">4</td><td colspan="2">This bit programs the PLL1 charge pump output current level.</td></tr>
<tr><td>Field Value</td><td>Gain</td></tr>
<tr><td>0 (0x00)</td><td>50 µA</td></tr>
<tr><td>1 (0x01)</td><td>150 µA</td></tr>
<tr><td>2 (0x02)</td><td>250 µA</td></tr>
<tr><td>3 (0x03)</td><td>350 µA</td></tr>
<tr><td>4 (0x04)</td><td>450 µA</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>14 (0x0E)</td><td>1450 µA</td></tr>
<tr><td>15 (0x0F)</td><td>1550 µA</td></tr>
</table>

9.7.7.6 PLL1_DLD_CNT[13:8], PLL1_DLD_CNT[7:0]

Table 57. PLL1_DLD_CNT[13:0]

MSB	LSB
0x15C[5:0]	0x15D[7:0]

This register contains the value of the PLL1 DLD counter.

Table 58. Registers 0x15C and 0x15D

<table>
<tr><th>BIT</th><th>REGISTERS</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:6</td><td>0x15C</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">5:0</td><td rowspan="4">0x15C</td><td rowspan="4">PLL1_DLD
_CNT[13:8]</td><td rowspan="4">32</td><td colspan="2">The reference and feedback of PLL1 must be within the window of phase error as specified by PLL1_WND_SIZE for this many phase detector cycles before PLL1 digital lock detect is asserted.</td></tr>
<tr><td>Field Value</td><td>Delay Value</td></tr>
<tr><td>0 (0x00)</td><td>Reserved</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td rowspan="5">7:0</td><td rowspan="5">0x15D</td><td rowspan="5">PLL1_DLD
_CNT[7:0]</td><td rowspan="5">0</td><td>2 (0x02)</td><td>2</td></tr>
<tr><td>3 (0x03)</td><td>3</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>16,382 (0x3FFE)</td><td>16,382</td></tr>
<tr><td>16,383 (0x3FFF)</td><td>16,383</td></tr>
</table>

9.7.7.7 PLL1_R_DLY, PLL1_N_DLY

This register contains the delay value for PLL1 N and R delays.

Table 59. Register 0x15E

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:6</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="10">5:3</td><td rowspan="10">PLL1_R_DLY</td><td rowspan="10">0</td><td colspan="2">Increasing delay of PLL1_R_DLY will cause the outputs to lag from CLKinX. For use in 0-delay mode.</td></tr>
<tr><td>Field Value</td><td>Gain</td></tr>
<tr><td>0 (0x00)</td><td>0 ps</td></tr>
<tr><td>1 (0x01)</td><td>205 ps</td></tr>
<tr><td>2 (0x02)</td><td>410 ps</td></tr>
<tr><td>3 (0x03)</td><td>615 ps</td></tr>
<tr><td>4 (0x04)</td><td>820 ps</td></tr>
<tr><td>5 (0x05)</td><td>1025 ps</td></tr>
<tr><td>6 (0x06)</td><td>1230 ps</td></tr>
<tr><td>7 (0x07)</td><td>1435 ps</td></tr>
<tr><td rowspan="10">2:0</td><td rowspan="10">PLL1_N_DLY</td><td rowspan="10">0</td><td colspan="2">Increasing delay of PLL1_N_DLY will cause the outputs to lead from CLKinX. For use in 0-delay mode.</td></tr>
<tr><td>Field Value</td><td>Gain</td></tr>
<tr><td>0 (0x00)</td><td>0 ps</td></tr>
<tr><td>1 (0x01)</td><td>205 ps</td></tr>
<tr><td>2 (0x02)</td><td>410 ps</td></tr>
<tr><td>3 (0x03)</td><td>615 ps</td></tr>
<tr><td>4 (0x04)</td><td>820 ps</td></tr>
<tr><td>5 (0x05)</td><td>1025 ps</td></tr>
<tr><td>6 (0x06)</td><td>1230 ps</td></tr>
<tr><td>7 (0x07)</td><td>1435 ps</td></tr>
</table>

9.7.7.8 PLL1_LD_MUX, PLL1_LD_TYPE

This register configures the PLL1 LD pin.

Table 60. Register 0x15F

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:3	PLL1_LD_MUX	1	This sets the output value of the Status_LD1 pin.	
			Field Value	**MUX Value**
			0 (0x00)	Logic Low
			1 (0x01)	PLL1 DLD
			2 (0x02)	PLL2 DLD
			3 (0x03)	PLL1 & PLL2 DLD
			4 (0x04)	Holdover Status
			5 (0x05)	DAC Locked
			6 (0x06)	Reserved
			7 (0x07)	SPI Readback
			8 (0x08)	DAC Rail
			9 (0x09)	DAC Low
			10 (0x0A)	DAC High
			11 (0x0B)	PLL1_N
			12 (0x0C)	PLL1_N/2
			13 (0x0D)	PLL2_N
			14 (0x0E)	PLL2_N/2
			15 (0x0F)	PLL1_R
			16 (0x10)	PLL1_R/2
			17 (0x11)	PLL2_R (1)
			18 (0x12)	PLL2_R/2 (1)
2:0	PLL1_LD_TYPE	6	Sets the IO type of the Status_LD1 pin.	
			Field Value	**TYPE**
			0 (0x00)	Reserved
			1 (0x01)	Reserved
			2 (0x02)	Reserved
			3 (0x03)	Output (push-pull)
			4 (0x04)	Output inverted (push-pull)
			5 (0x05)	Reserved
			6 (0x06)	Output (open drain)

(1) Only valid when PLL2_LD_MUX is not set to 2 (PLL2_DLD) or 3 (PLL1 & PLL2 DLD).

9.7.8 (0x160 - 0x16E) PLL2 Configuration

9.7.8.1 PLL2_R[11:8], PLL2_R[7:0]

Table 61. PLL2_R[11:0]

MSB	LSB
0x160[3:0]	0x161[7:0]

This register contains the value of the PLL2 R divider.

Table 62. Registers 0x160 and 0x161

<table>
<tr><th>BIT</th><th>REGISTERS</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:4</td><td>0x160</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">3:0</td><td rowspan="4">0x160</td><td rowspan="4">PLL2_R[11:8]</td><td rowspan="4">0</td><td colspan="2">Valid values for the PLL2 R divider.</td></tr>
<tr><td>Field Value</td><td>Divide Value</td></tr>
<tr><td>0 (0x00)</td><td>Not Valid</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td rowspan="5">7:0</td><td rowspan="5">0x161</td><td rowspan="5">PLL2_R[7:0]</td><td rowspan="5">2</td><td>2 (0x02)</td><td>2</td></tr>
<tr><td>3 (0x03)</td><td>3</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>4,094 (0xFFE)</td><td>4,094</td></tr>
<tr><td>4,095 (0xFFF)</td><td>4,095</td></tr>
</table>

9.7.8.2 PLL2_P, OSCin_FREQ, PLL2_XTAL_EN, PLL2_REF_2X_EN

This register sets other PLL2 functions.

Table 63. Register 0x162

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="10">7:5</td><td rowspan="10">PLL2_P</td><td rowspan="10">2</td><td colspan="2">The PLL2 N Prescaler divides the output of the VCO as selected by Mode_MUX1 and is connected to the PLL2 N divider.</td></tr>
<tr><td>Field Value</td><td>Value</td></tr>
<tr><td>0 (0x00)</td><td>8</td></tr>
<tr><td>1 (0x01)</td><td>2</td></tr>
<tr><td>2 (0x02)</td><td>2</td></tr>
<tr><td>3 (0x03)</td><td>3</td></tr>
<tr><td>4 (0x04)</td><td>4</td></tr>
<tr><td>5 (0x05)</td><td>5</td></tr>
<tr><td>6 (0x06)</td><td>6</td></tr>
<tr><td>7 (0x07)</td><td>7</td></tr>
<tr><td rowspan="8">4:2</td><td rowspan="8">OSCin_FREQ</td><td rowspan="8">7</td><td colspan="2">The frequency of the PLL2 reference input to the PLL2 Phase Detector (OSCin/OSCin* port) must be programmed in order to support proper operation of the frequency calibration routine which locks the internal VCO to the target frequency.</td></tr>
<tr><td>Field Value</td><td>OSCin Frequency</td></tr>
<tr><td>0 (0x00)</td><td>0 to 63 MHz</td></tr>
<tr><td>1 (0x01)</td><td>>63 MHz to 127 MHz</td></tr>
<tr><td>2 (0x02)</td><td>>127 MHz to 255 MHz</td></tr>
<tr><td>3 (0x03)</td><td>Reserved</td></tr>
<tr><td>4 (0x04)</td><td>>255 MHz to 500 MHz</td></tr>
<tr><td>5 (0x05) to 7(0x07)</td><td>Reserved</td></tr>
<tr><td>1</td><td>PLL2_XTAL_EN</td><td>0</td><td colspan="2">If an external crystal is being used to implement a discrete VCXO, the internal feedback amplifier must be enabled with this bit in order to complete the oscillator circuit.
0: Oscillator Amplifier Disabled
1: Oscillator Amplifier Enabled</td></tr>
<tr><td>0</td><td>PLL2_REF_2X_EN</td><td>1</td><td colspan="2">Enabling the PLL2 reference frequency doubler allows for higher phase detector frequencies on PLL2 than would normally be allowed with the given VCXO or Crystal frequency.
Higher phase detector frequencies reduces the PLL N values which makes the design of wider loop bandwidth filters possible.
0: Doubler Disabled
1: Doubler Enabled</td></tr>
</table>

9.7.8.3 PLL2_N_CAL

PLL2_N_CAL[17:0]

PLL2 never uses 0-delay during frequency calibration. These registers contain the value of the PLL2 N divider used with PLL2 pre-scaler during calibration for cascaded 0-delay mode. Once calibration is complete, PLL2 will use PLL2_N value. Cascaded 0-delay mode occurs when PLL2_NCLK_MUX = 1.

Table 64. Register 0x162

MSB	—	LSB
0x163[1:0]	0x164[7:0]	0x165[7:0]

Table 65. Registers 0x163, 0x164, and 0x165

BIT	REGISTERS	NAME	POR DEFAULT	DESCRIPTION	
7:2	0x163	NA	0	Reserved	
1:0	0x163	PLL2_N _CAL[17:16]	0	**Field Value**	**Divide Value**
				0 (0x00)	Not Valid
7:0	0x164	PLL2_N_CAL[15:8]	0	1 (0x01)	1
				2 (0x02)	2
7:0	0x165	PLL2_N_CAL[7:0]	12	...	...
				262,143 (0x3FFFF)	262,143

9.7.8.4 PLL2_FCAL_DIS, PLL2_N

This register disables frequency calibration and sets the PLL2 N divider value. Programming register 0x168 starts a VCO calibration routine if PLL2_FCAL_DIS = 0.

Table 66. PLL2_N[17:0]

MSB	—	LSB
0x166[1:0]	0x167[7:0]	0x168[7:0]

Table 67. Registers 0x166, 0x167, and 0x168

BIT	REGISTERS	NAME	POR DEFAULT	DESCRIPTION	
7:3	0x166	NA	0	Reserved	
2	0x166	PLL2_FCAL_DIS	0	This disables the PLL2 frequency calibration on programming register 0x168. 0: Frequency calibration enabled 1: Frequency calibration disabled	
1:0	0x166	PLL2_N[17:16]	0	**Field Value**	**Divide Value**
				0 (0x00)	Not Valid
7:0	0x167	PLL2_N[15:8]	0	1 (0x01)	1
				2 (0x02)	2
7:0	0x168	PLL2_N[7:0]	12	...	...
				262,143 (0x3FFFF)	262,143

9.7.8.5 PLL2_WND_SIZE, PLL2_CP_GAIN, PLL2_CP_POL, PLL2_CP_TRI

This register controls the PLL2 phase detector.

Table 68. Register 0x169

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="6">6:5</td><td rowspan="6">PLL2_WND_SIZE</td><td rowspan="6">2</td><td colspan="2">PLL2_WND_SIZE sets the window size used for digital lock detect for PLL2. If the phase error between the reference and feedback of PLL2 is less than specified time, then the PLL2 lock counter increments. This value must be programmed to 2 (3.7 ns).</td></tr>
<tr><td>Field Value</td><td>Definition</td></tr>
<tr><td>0 (0x00)</td><td>Reserved</td></tr>
<tr><td>1 (0x01)</td><td>Reserved</td></tr>
<tr><td>2 (0x02)</td><td>3.7 ns</td></tr>
<tr><td>3 (0x03)</td><td>Reserved</td></tr>
<tr><td rowspan="6">4:3</td><td rowspan="6">PLL2_CP_GAIN</td><td rowspan="6">3</td><td colspan="2">This bit programs the PLL2 charge pump output current level. The table below also illustrates the impact of the PLL2 TRISTATE bit in conjunction with PLL2_CP_GAIN.</td></tr>
<tr><td>Field Value</td><td>Definition</td></tr>
<tr><td>0 (0x00)</td><td>100 µA</td></tr>
<tr><td>1 (0x01)</td><td>400 µA</td></tr>
<tr><td>2 (0x02)</td><td>1600 µA</td></tr>
<tr><td>3 (0x03)</td><td>3200 µA</td></tr>
<tr><td rowspan="4">2</td><td rowspan="4">PLL2_CP_POL</td><td rowspan="4">0</td><td colspan="2">PLL2_CP_POL sets the charge pump polarity for PLL2. The internal VCO requires the negative charge pump polarity to be selected. Many VCOs use positive slope.
A positive slope VCO increases output frequency with increasing voltage. A negative slope VCO decreases output frequency with increasing voltage.</td></tr>
<tr><td>Field Value</td><td>Description</td></tr>
<tr><td>0</td><td>Negative Slope VCO/VCXO</td></tr>
<tr><td>1</td><td>Positive Slope VCO/VCXO</td></tr>
<tr><td>1</td><td>PLL2_CP_TRI</td><td>0</td><td colspan="2">PLL2_CP_TRI TRI-STATEs the output of the PLL2 charge pump.
0: Disabled
1: TRI-STATE</td></tr>
<tr><td>0</td><td>Fixed Value</td><td>1</td><td colspan="2">When programming register 0x169, this field must be set to 1.</td></tr>
</table>

9.7.8.6 SYSREF_REQ_EN, PLL2_DLD_CNT

Table 69. PLL2_DLD_CNT[15:0]

MSB	LSB
0x16A[5:0]	0x16B[7:0]

This register has the value of the PLL2 DLD counter.

Table 70. Registers 0x16A and 0x16B

<table>
<tr><th>BIT</th><th>REGISTERS</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>0x16A</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td>6</td><td>0x16A</td><td>SYSREF_REQ_EN</td><td>0</td><td colspan="2">Enables the SYNC/SYSREF_REQ pin to force the SYSREF_MUX = 3 for continuous pulses. When using this feature enable pulser and set SYSREF_MUX = 2 (Pulser).</td></tr>
<tr><td rowspan="4">5:0</td><td rowspan="4">0x16A</td><td rowspan="4">PLL2_DLD _CNT[13:8]</td><td rowspan="4">32</td><td colspan="2">The reference and feedback of PLL2 must be within the window of phase error as specified by PLL2_WND_SIZE for PLL2_DLD_CNT cycles before PLL2 digital lock detect is asserted.</td></tr>
<tr><th>Field Value</th><th>Divide Value</th></tr>
<tr><td>0 (0x00)</td><td>Not Valid</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td rowspan="5">7:0</td><td rowspan="5">0x16B</td><td rowspan="5">PLL2_DLD_CNT</td><td rowspan="5">0</td><td>2 (0x02)</td><td>2</td></tr>
<tr><td>3 (0x03)</td><td>3</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>16,382 (0x3FFE)</td><td>16,382</td></tr>
<tr><td>16,383 (0x3FFF)</td><td>16,383</td></tr>
</table>

9.7.8.7 PLL2_LF_R4, PLL2_LF_R3

This register controls the integrated loop filter resistors.

Table 71. Register 0x16C

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	NA	0	Reserved	
5:3	PLL2_LF_R4	0	Internal loop filter components are available for PLL2, enabling either 3rd or 4th order loop filters without requiring external components. Internal loop filter resistor R4 can be set according to the following table.	
			Field Value	**Resistance**
			0 (0x00)	200 Ω
			1 (0x01)	1 kΩ
			2 (0x02)	2 kΩ
			3 (0x03)	4 kΩ
			4 (0x04)	16 kΩ
			5 (0x05)	Reserved
			6 (0x06)	Reserved
			7 (0x07)	Reserved
2:0	PLL2_LF_R3	0	Internal loop filter components are available for PLL2, enabling either 3rd or 4th order loop filters without requiring external components. Internal loop filter resistor R3 can be set according to the following table.	
			Field Value	**Resistance**
			0 (0x00)	200 Ω
			1 (0x01)	1 kΩ
			2 (0x02)	2 kΩ
			3 (0x03)	4 kΩ
			4 (0x04)	16 kΩ
			5 (0x05)	Reserved
			6 (0x06)	Reserved
			7 (0x07)	Reserved

9.7.8.8 PLL2_LF_C4, PLL2_LF_C3

This register controls the integrated loop filter capacitors.

Table 72. Register 0x16D

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:4	PLL2_LF_C4	0	Internal loop filter components are available for PLL2, enabling either 3rd or 4th order loop filters without requiring external components. Internal loop filter capacitor C4 can be set according to the following table.	
			Field Value	**Capacitance**
			0 (0x00)	10 pF
			1 (0x01)	15 pF
			2 (0x02)	29 pF
			3 (0x03)	34 pF
			4 (0x04)	47 pF
			5 (0x05)	52 pF
			6 (0x06)	66 pF
			7 (0x07)	71 pF
			8 (0x08)	103 pF
			9 (0x09)	108 pF
			10 (0x0A)	122 pF
			11 (0x0B)	126 pF
			12 (0x0C)	141 pF
			13 (0x0D)	146 pF
			14 (0x0E)	Reserved
			15 (0x0F)	Reserved
3:0	PLL2_LF_C3	0	Internal loop filter components are available for PLL2, enabling either 3rd or 4th order loop filters without requiring external components. Internal loop filter capacitor C3 can be set according to the following table.	
			Field Value	**Capacitance**
			0 (0x00)	10 pF
			1 (0x01)	11 pF
			2 (0x02)	15 pF
			3 (0x03)	16 pF
			4 (0x04)	19 pF
			5 (0x05)	20 pF
			6 (0x06)	24 pF
			7 (0x07)	25 pF
			8 (0x08)	29 pF
			9 (0x09)	30 pF
			10 (0x0A)	33 pF
			11 (0x0B)	34 pF
			12 (0x0C)	38 pF
			13 (0x0D)	39 pF
			14 (0x0E)	Reserved
			15 (0x0F)	Reserved

9.7.8.9 PLL2_LD_MUX, PLL2_LD_TYPE

This register sets the output value of the Status_LD2 pin.

Table 73. Register 0x16E

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:3	PLL2_LD_MUX	2	This sets the output value of the Status_LD2 pin.	
			Field Value	**MUX Value**
			0 (0x00)	Logic Low
			1 (0x01)	PLL1 DLD
			2 (0x02)	PLL2 DLD
			3 (0x03)	PLL1 & PLL2 DLD
			4 (0x04)	Holdover Status
			5 (0x05)	DAC Locked
			6 (0x06)	Reserved
			7 (0x07)	SPI Readback
			8 (0x08)	DAC Rail
			9 (0x09)	DAC Low
			10 (0x0A)	DAC High
			11 (0x0B)	PLL1_N
			12 (0x0C)	PLL1_N/2
			13 (0x0D)	PLL2_N
			14 (0x0E)	PLL2_N/2
			15 (0x0F)	PLL1_R
			16 (0x10)	PLL1_R/2
			17 (0x11)	PLL2_R (1)
			18 (0x12)	PLL2_R/2 (1)
2:0	PLL2_LD_TYPE	6	Sets the IO type of the Status_LD2 pin.	
			Field Value	**TYPE**
			0 (0x00)	Reserved
			1 (0x01)	Reserved
			2 (0x02)	Reserved
			3 (0x03)	Output (push-pull)
			4 (0x04)	Output inverted (push-pull)
			5 (0x05)	Reserved
			6 (0x06)	Output (open drain)

(1) Only valid when PLL1_LD_MUX is not set to 2 (PLL2_DLD) or 3 (PLL1 & PLL2 DLD).

9.7.9 (0x16F - 0x1FFF) Misc Registers

9.7.9.1 Fixed Register 0x171

Always program this register to value 170.

Table 74. Register 0x171

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	Fixed Register	10 (0x0A)	Always program to 170 (0xAA)

9.7.9.2 Fixed Register 0x172

Always program this register to value 2.

Table 75. Register 0x172

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	Fixed Register	0	Always program to 2 (0x02)

9.7.9.3 PLL2_PRE_PD, PLL2_PD

Table 76. Register 0x173

BIT	NAME	DESCRIPTION
7	N/A	Reserved
6	PLL2_PRE_PD	Powerdown PLL2 prescaler 0: Normal Operation 1: Powerdown
5	PLL2_PD	Powerdown PLL2 0: Normal Operation 1: Powerdown
4:0	N/A	Reserved

9.7.9.4 OPT_REG_1

This register must be written to optimize VCO1 phase noise performance over temperature. This register must be written before writing register 0x168 for PLL2 calibration when using VCO1.

Table 77. Register 0x17C

BIT	NAME	DESCRIPTION
7:0	OPT_REG_1	Program to 21 (0x15)

9.7.9.5 OPT_REG_2

This register must be written to optimize VCO1 phase noise performance over temperature. This register must be written before writing register 0x168 for PLL2 calibration when using VCO1.

Table 78. Register 0x17D

BIT	NAME	DESCRIPTION
7:0	OPT_REG_2	Program to 51 (0x33)

9.7.9.6 RB_PLL1_LD_LOST, RB_PLL1_LD, CLR_PLL1_LD_LOST

Table 79. Register 0x182

BIT	NAME	DESCRIPTION
7:3	N/A	Reserved
2	RB_PLL1_LD_LOST	This is set when PLL1 DLD edge falls. Does not set if cleared while PLL1 DLD is low.
1	RB_PLL1_LD	Read back 0: PLL1 DLD is low. Read back 1: PLL1 DLD is high.
0	CLR_PLL1_LD_LOST	To reset RB_PLL1_LD_LOST, write CLR_PLL1_LD_LOST with 1 and then 0. 0: RB_PLL1_LD_LOST will be set on next falling PLL1 DLD edge. 1: RB_PLL1_LD_LOST is held clear (0). User must clear this bit to allow RB_PLL1_LD_LOST to become set again.

9.7.9.7 RB_PLL2_LD_LOST, RB_PLL2_LD, CLR_PLL2_LD_LOST

Table 80. Register 0x0x183

BIT	NAME	DESCRIPTION
7:3	N/A	Reserved
2	RB_PLL2_LD_LOST	This is set when PLL2 DLD edge falls. Does not set if cleared while PLL2 DLD is low.
1	RB_PLL2_LD	PLL1_LD_MUX or PLL2_LD_MUX must select setting 2 (PLL2 DLD) for valid reading of this bit. Read back 0: PLL2 DLD is low. Read back 1: PLL2 DLD is high.
0	CLR_PLL2_LD_LOST	To reset RB_PLL2_LD_LOST, write CLR_PLL2_LD_LOST with 1 and then 0. 0: RB_PLL2_LD_LOST will be set on next falling PLL2 DLD edge. 1: RB_PLL2_LD_LOST is held clear (0). User must clear this bit to allow RB_PLL2_LD_LOST to become set again.

9.7.9.8 RB_DAC_VALUE(MSB), RB_CLKinX_SEL, RB_CLKinX_LOS

This register provides read back access to CLKinX selection indicator and CLKinX LOS indicator. The 2 MSBs are shared with the RB_DAC_VALUE. See RB_DAC_VALUE section.

Table 81. Register 0x184

BIT	NAME	DESCRIPTION
7:6	RB_DAC_VALUE[9:8]	See RB_DAC_VALUE section.
5	RB_CLKin2_SEL	Read back 0: CLKin2 is not selected for input to PLL1. Read back 1: CLKin2 is selected for input to PLL1.
4	RB_CLKin1_SEL	Read back 0: CLKin1 is not selected for input to PLL1. Read back 1: CLKin1 is selected for input to PLL1.
3	RB_CLKin0_SEL	Read back 0: CLKin0 is not selected for input to PLL1. Read back 1: CLKin0 is selected for input to PLL1.
2	N/A	
1	RB_CLKin1_LOS	Read back 1: CLKin1 LOS is active. Read back 0: CLKin1 LOS is not active.
0	RB_CLKin0_LOS	Read back 1: CLKin0 LOS is active. Read back 0: CLKin0 LOS is not active.

9.7.9.9 RB_DAC_VALUE

Contains the value of the DAC for user readback.

FIELD NAME	MSB	LSB
RB_DAC_VALUE	0x184 [7:6]	0x185 [7:0]

Table 82. Registers 0x184 and 0x185

BIT	REGISTERS	NAME	POR DEFAULT	DESCRIPTION
7:6	0x184	RB_DAC_ VALUE[9:8]	2	DAC value is 512 on power on reset, if PLL1 locks upon power-up the DAC value will change.
7:0	0x185	RB_DAC_ VALUE[7:0]	0	

9.7.9.10 RB_HOLDOVER

Table 83. Register 0x188

BIT	NAME	DESCRIPTION
7:5	N/A	Reserved
4	RB_HOLDOVER	Read back 0: Not in HOLDOVER. Read back 1: In HOLDOVER.
3:0	N/A	Reserved

9.7.9.11 SPI_LOCK

Prevents SPI registers from being written to, except for 0x1FFD, 0x1FFE, 0x1FFF. These registers must be written to sequentially and in order: 0x1FFD, 0x1FFE, 0x1FFF.

These registers cannot be read back.

MSB	—	LSB
0x1FFD [7:0]	0x1FFE [7:0]	0x1FFF [7:0]

Table 84. Registers 0x1FFD, 0x1FFE, and 0x1FFF

BIT	REGISTERS	NAME	POR DEFAULT	DESCRIPTION
7:0	0x1FFD	SPI_LOCK[23:16]	0	0: Registers unlocked. 1 to 255: Registers locked
7:0	0x1FFE	SPI_LOCK[15:8]	0	0: Registers unlocked. 1 to 255: Registers locked
7:0	0x1FFF	SPI_LOCK[7:0]	83	0 to 82: Registers locked 83: Registers unlocked 84 to 256: Registers locked

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

To assist customers in frequency planning and design of loop filters Texas Instrument's provides the Clock Design Tool (www.ti.com/tool/clockdesigntool) and Clock Architect (www.ti.com/clockarchitect).

10.1.1 Digital Lock Detect Frequency Accuracy

The digital lock detect circuit is used to determine PLL1 locked, PLL2 locked, and holdover exit events. A window size and lock count register are programmed to set a ppm frequency accuracy of reference to feedback signals of the PLL for each event to occur. When a PLL digital lock event occurs the PLL's digital lock detect is asserted true. When the holdover exit event occurs, the device exits holdover mode.

EVENT	PLL	WINDOW SIZE	LOCK COUNT
PLL1 Locked	PLL1	PLL1_WND_SIZE	PLL1_DLD_CNT
PLL2 Locked	PLL2	PLL2_WND_SIZE	PLL2_DLD_CNT
Holdover exit	PLL1	PLL1_WND_SIZE	HOLDOVER_DLD_CNT

For a digital lock detect event to occur there must be a *lock count* number of phase detector cycles of PLLX during which the time/phase error of the PLLX_R reference and PLLX_N feedback signal edges are within the user programmable *window size*. Because there must be at least *lock count* phase detector events before a lock event occurs, a minimum digital lock event time can be calculated as *lock count* / f_{PDX} where X = 1 for PLL1 or 2 for PLL2.

By using Equation 3, values for a *lock count* and *window size* can be chosen to set the frequency accuracy required by the system in ppm before the digital lock detect event occurs:

$$ppm = \frac{1e6 \times PLLX\_WND\_SIZE \times f_{PDX}}{PLLX\_DLD\_CNT} \quad (3)$$

The effect of the *lock count* value is that it shortens the effective lock window size by dividing the *window size* by *lock count*.

If at any time the PLLX_R reference and PLLX_N feedback signals are outside the time window set by *window size*, then the *lock count* value is reset to 0.

10.1.1.1 Minimum Lock Time Calculation Example

To calculate the minimum PLL2 digital lock time given a PLL2 phase detector frequency of 40 MHz and PLL2_DLD_CNT = 10,000. Then the minimum lock time of PLL2 is 10,000 / 40 MHz = 250 µs.

10.1.2 Driving CLKin and OSCin Inputs

10.1.2.1 Driving CLKin Pins With a Differential Source

Both CLKin ports and OSCin can be driven by differential signals. TI recommends setting the input mode to bipolar (CLKinX_BUF_TYPE = 0) when using differential reference clocks. The LMK04828-EP internally biases the input pins so the differential interface should be AC-coupled. The recommended circuits for driving the CLKin pins with either LVDS or LVPECL are shown in Figure 15 and Figure 16.

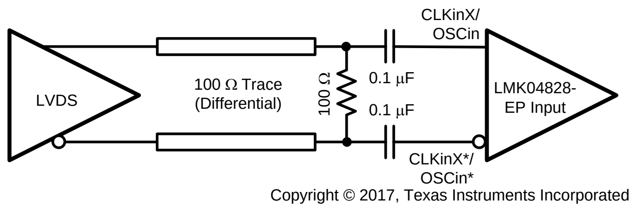


Figure 15. CLKinX/X* or OSCin Termination for an LVDS Reference Clock Source

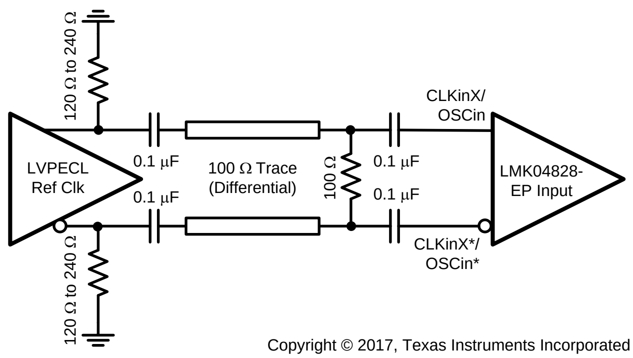


Figure 16. CLKinX/X* or OSCin Termination for an LVPECL Reference Clock Source

Finally, a reference clock source that produces a differential sine wave output can drive the CLKin or OSCin pins using Figure 17.

NOTE

The signal level must conform to the requirements for the CLKin pins or OSCin pins listed in *Electrical Characteristics*.

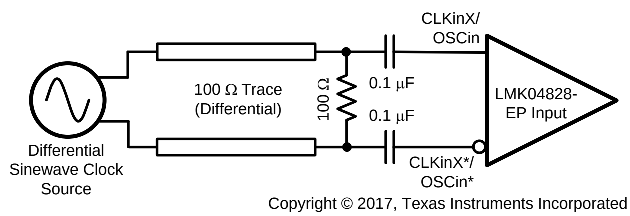


Figure 17. CLKinX/X* or OSCin Termination for a Differential Sinewave Reference Clock Source

10.1.2.2 Driving CLKin or OSCin Pins With a Single-Ended Source

The CLKin or OSCin pins of the LMK04828-EP can be driven using a single-ended reference clock source, for example, either a sine wave source or an LVCMOS/LVTTL source. Either AC coupling or DC coupling may be used for CLKin. OSCin requires AC coupling. In the case of the sine wave source that is expecting a 50 Ω load, TI recommends using AC coupling as shown in the circuit below with a 50-Ω termination. It may be required to add a series resistor to create a voltage divider to keep the input voltage within specification.

NOTE

The signal level must conform to the requirements for the CLKin pins listed in *Electrical Characteristics*. CLKinX_BUF_TYPE is recommended to be set to bipolar mode (CLKinX_BUF_TYPE = 0).

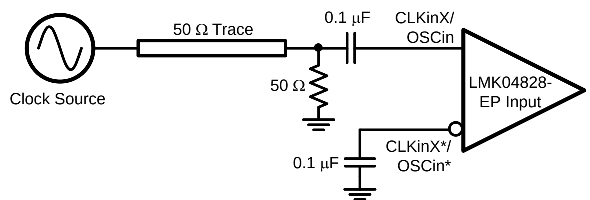


Figure 18. CLKinX/X* or OSCin Single-Ended Termination

If the CLKin pins are being driven with a single-ended LVCMOS/LVTTL source, either DC coupling or AC coupling may be used. If DC coupling is used, the CLKinX_BUF_TYPE should be set to MOS buffer mode (CLKinX_BUF_TYPE = 1) and the voltage swing of the source must meet the specifications for DC-coupled, MOS-mode clock inputs given in *Electrical Characteristics*. If AC coupling is used, the CLKinX_BUF_TYPE should be set to the bipolar buffer mode (CLKinX_BUF_TYPE = 0). The voltage swing at the input pins must meet the specifications for AC-coupled, bipolar mode clock inputs given in *Electrical Characteristics* . In this case, some attenuation of the clock input level may be required. A simple resistive divider circuit before the AC-coupling capacitor is sufficient.

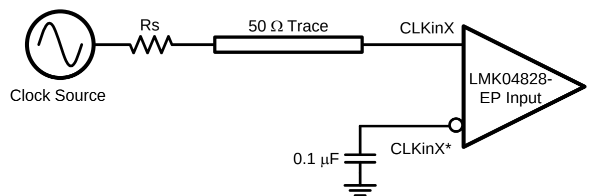


Figure 19. DC-Coupled LVCMOS/LVTTL Reference Clock

10.1.3 Using AC-Coupled Clock Outputs

When using LVDS or HSDS output modes and AC coupling, place shunt a 560 Ω across the outputs close to the IC to provide a DC path to the driver.

10.2 Typical Application

This design example below highlights using the available tools to design loop filters and create programming map for LMK04828-EP.

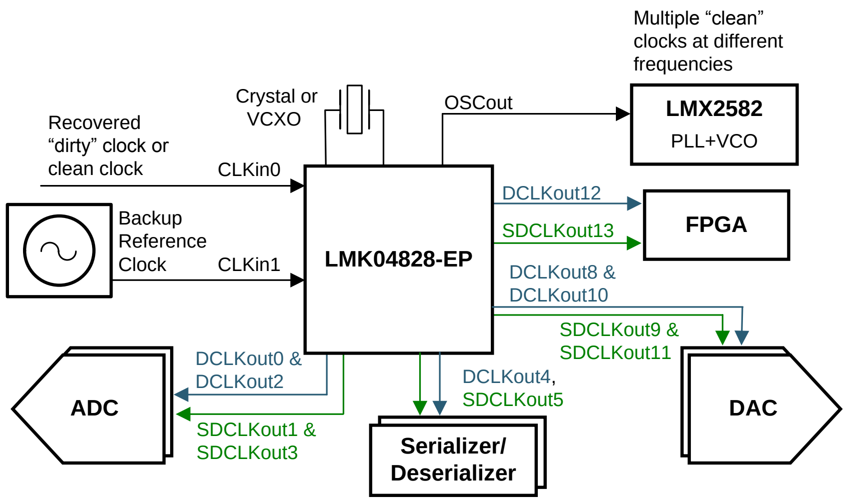


Figure 20. Typical Application

10.2.1 Design Requirements

Clocks outputs:

- 1x 245.76-MHz clock for JESD204B ADC, LVPECL.
  - This clock requires the best performance in this example.
- 2x 983.04-MHz clock for JESD204B DAC, LVPECL.
- 1x 122.88-MHz clock for JESD204B FPGA block, LVDS
- 3x 10.24-MHz SYSREF for ADC (LVPECL), DAC (LVPECL), FPGA (LVDS).
- 2x 122.88-MHz clock for FPGA, LVDS

For best performance, the highest possible phase detector frequency is used at PLL2. As such, a 122.88-MHz VCXO is used.

10.2.2 Detailed Design Procedure

Note this information is current as of the date of the release of this data sheet. Design tools receive continuous improvements to add features and improve model accuracy. Refer to software instructions or training for latest features.

10.2.2.1 Device Selection

Enter the required frequencies into the tools. In this design, the LMK04828-EP VCO1 meets the design requirements. Note that VCO0 offers lower noise floor while VCO1 offers improved VCO phase noise which reduces RMS jitter. Depending on application requirements only one or both VCOs may be an option. In this case, the only option is to choose the LMK04828-EP_VCO1 that has improved RMS jitter in the 12-kHz to 20-MHz integration range. Larger integration ranges may benefit from the lower noise floor of VCO0.

10.2.2.1.1 Clock Architect

Only one device of a part family is returned as a possible solution. For the above example, if there is a valid solution using both VCO0 and VCO1 of LMK04828-EP, only the solution for LMK04828-EP_VCO1 displays.

Under advanced tab, filtering of specific parts can be done using regular expressions in the Part Filter box. [LMK04828-EP] filters for only LMK04828-EP devices (without the brackets); this includes a VCO0 and VCO1 simulation profile. More detailed filters can be given such as the entire part name LMK04828-EP_VCO0 to force an LMK04828-EP using VCO0 solution if one is available.

Typical Application (continued)

10.2.2.1.2 Clock Design Tool

In wizard-mode, select Dual Loop PLL to find LMK04828-EP devices. If a high frequency and clean reference is available, it is not required to use dual loop; PLL1 can be powered down and input is then provided through the OSCin port. When simulating single loop solutions, set PLL1 loop filter block to [0 Hz LBW] and use VCXO as the reference block.

In the Clock Design Tool, use LMK04828B to simulate LMK04828-EP.

10.2.2.2 Device Configuration and Simulation

The tools automatically configure the simulation to meet the input and output frequency requirements given and make assumptions about other parameters to give some default simulations. However the user may chose to make adjustments for more accurate simulations to their application. For example:

- Entering the VCO Gain of the external VCXO or possible external VCO used device.
- Adjust the charge pump current to help with loop filter component selection. Lower charge pump currents result in smaller components but may increase impacts of leakage and at the lowest values reduce PLL phase nosie performance.
- Clock Design Tool allows loading a custom phase noise plot for any block. Typically, a custom phase noise plot is entered for CLKin to match the reference phase noise to device; a phase noise plot for the VCXO can additionally be provided to match the performance of VCXO used. For improved accuracy in simulation and optimum loop filter design, be sure to load these custom noise profiles for use in application.
- The design tools return with high reference or phase detector frequencies by default. In the Clock Design Tool the user may increase the reference divider to reduce the frequency if desired. Due to the narrow loop bandwidth used on PLL1, it is common to reduce the phase detector frequency on PLL1.

10.2.2.3 Device Programming

Using the clock design tools configuration the TICS Pro software is manually updated with this information to meet the required application. Note for the JESD204B outputs place device clocks on the DCLKoutX output, then turn on the paired SDCLKoutY output for SYSREF output. For Non-JESD204B outputs both DCLKoutX and paired SDCLKoutY may be driven by the device clock divider to maximize number of available outputs.

Frequency planning for assignment of outputs:

- To minimize crosstalk perform frequency planning or CLKout assignments to keep common frequencies on outputs close together.
- It is best to place common device clock output frequencies on outputs sharing the same V_{CC} group. For example, these outputs share Vcc4_CG2. Refer to *Pin Configuration and Functions* to see the V_{CC} groupings the clock outputs.

In this example, the 245.76-MHz ADC output needs the best performance. DCLKout2 on the LMK04828-EP provides the best noise floor or performance. The 245.76 MHz is placed on DCLKout2 with 10.24-MHz SYSREF on SDCLKout3.

- For best performance the input and output drive level bits may be set. Best noise floor performance is achieved with DCLKout2_IDL = 1 and DCLKout2_ODL = 1.

In this example, the 983.04-MHz DAC output is placed on DCLKout4 and DCLKout6 with 10.24-MHz SYSREF on paired SDCLKout5 and SDCLKout7 outputs.

- These outputs share Vcc4_CG2.

In this example, the 122.88-MHz FPGA JESD204B output is placed on DCLKout10 with 10.24-MHz SYSREF on paired SDCLKout11 output.

Additionally, the 122.88-MHz FPGA non-JESD204B outputs are placed on DCLKout8 and SDCLKout9.

- When frequency planning, consider PLL2 as a clock output at the phase detector frequency. As such, these 122.88-MHz outputs have been placed on the outputs close to the PLL2 and Charge Pump power supplies.

Once the device programming is completed as desired in the TICS Pro software, it is possible to export the register settings from the *Register* tab for use in application.

Typical Application (continued)

10.2.3 Application Curves

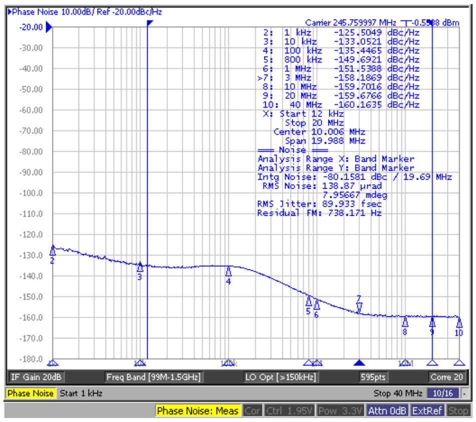


Figure 21. DCLKout0, 245.76 MHz, LVPECL20 With 240-Ω Emitter Resistors DCLKout0_1_IDL = 1, DCLKout0_1_ODL = 1

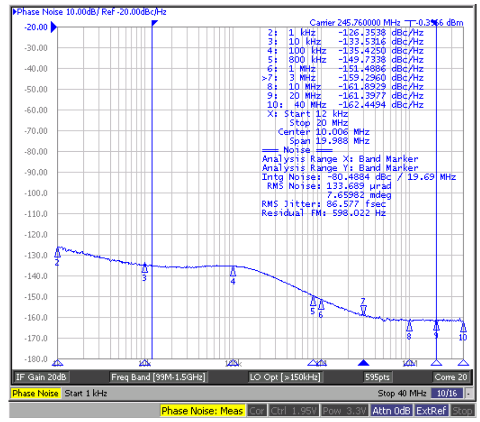


Figure 22. DCLKout2, 245.76 MHz, LVPECL20 With 240-Ω Emitter Resistors DCLKout2_3_IDL = 1, DCLKout2_3_ODL = 1

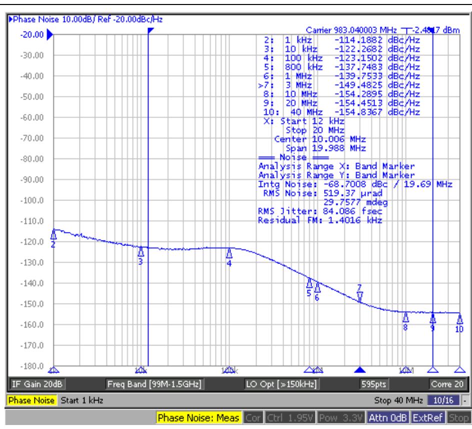


Figure 23. DCLKout4, 983.04 MHz, LVPECL16 With 240-Ω Emitter Resistors DCLKout0_1_IDL = 1, DCLKout0_1_ODL = 0

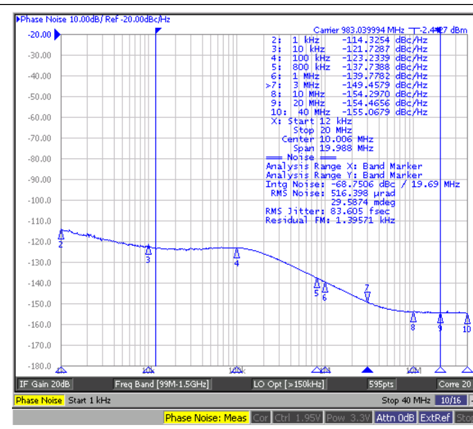


Figure 24. DCLKout6, 983.04 MHz, LVPECL16 With 240-Ω Emitter Resistors DCLKout0_1_IDL = 1, DCLKout0_1_ODL = 0

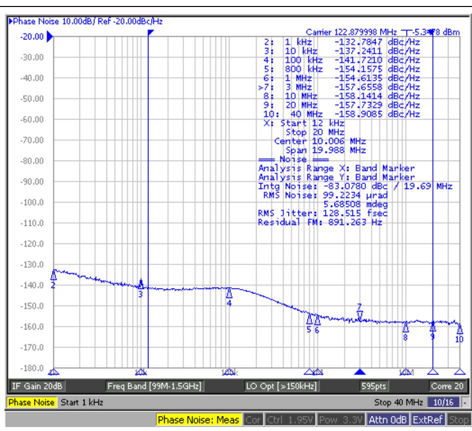


Figure 25. DCLKout10, 122.88 MHz, LVDS DCLKout0_1_IDL = 1, DCLKout0_1_ODL = 0

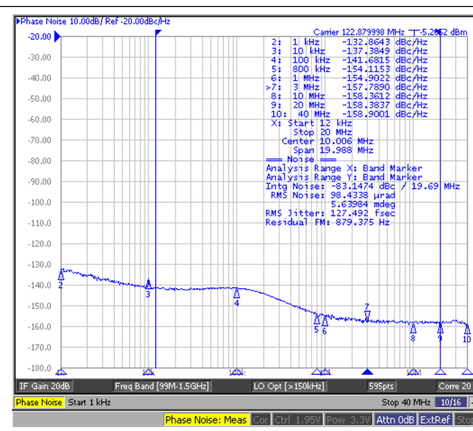


Figure 26. SDCLKout11, 122.88 MHz, LVDS DCLKout0_1_IDL = 1, DCLKout0_1_ODL = 0

Typical Application (continued)

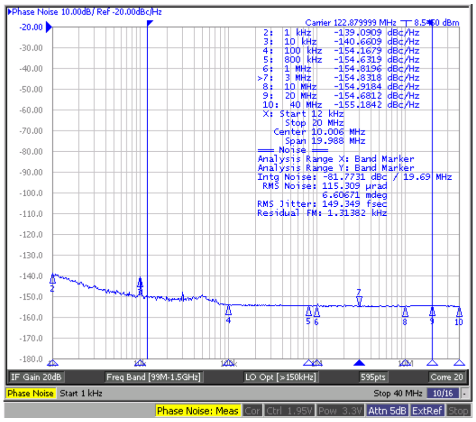


Figure 27. OSCout, 122.88 MHz, LVCMOS (Norm/Inv) Normal Output Measured, Inverse 50-Ω Termination

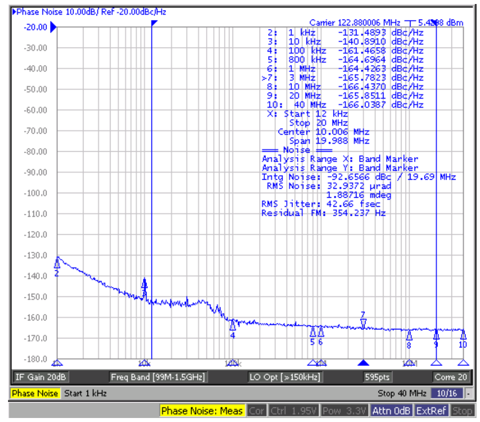


Figure 28. Direct VCXO Measurement Open-Loop, Holdover Mode Set

10.3 Do's and Don'ts

Do use the software RESET bit at the beginning of system programming as suggested in recommended programming sequence.

10.3.1 Pin Connection Recommendations

- **V_{CC} Pins and Decoupling**: all V_{CC} pins must always be connected.
- **Unused Clock Outputs:** leave unused clock outputs floating and powered down.
- **Unused Clock Inputs:** unused clock inputs can be left floating.
- Unused OSCin or OSCout can be left floating and powered down.
- If the RESET pin is unused, program the RESET pin as an output using RESET_MUX to prevent chance for device reset via RESET pin. If RESET pin is used, consider placing a capacitor at pin to prevent a possible glitch from system resetting the device.

11 Power Supply Recommendations

11.1 Current Consumption / Power Dissipation Calculations

From Table 85 the current consumption can be calculated for any configuration. Data below is typical and not assured.

Table 85. Typical Current Consumption for Selected Functional Blocks (T_A = 25°C, V_{CC} = 3.3 V)

BLOCK	TEST CONDITIONS		TYPICAL I_{CC} (mA)	POWER DISSIPATED in DEVICE (mW)	POWER DISSIPATED EXTERNALLY (mW)
CORE AND FUNCTIONAL BLOCKS					
Core	Dual Loop, Internal VCO0	PLL1 and PLL2 locked	131.5	433.95	—
VCO	VCO1 is selected	LMK04828-EP	13.5	44.55	—
OSCin Doubler	Doubler is enabled	EN_PLL2_REF_2X = 1	3	9.9	—
CLKin	Any one of the CLKinX is enabled		4.9	16.17	—
Holdover	Holdover is enabled	HOLDOVER_EN = 1	1.3	4.29	—
	Hitless switch is enabled	HOLDOVER_HITLESS_ SWITCH = 1	0.9	2.97	—
	Track mode	TRACK_EN = 1	2.5	8.25	—
SYNC_EN = 1	Required for SYNC and SYSREF functionality		7.6	25.08	—
SYSREF	Enabled	SYSREF_PD = 0	27.2	89.76	—
	Dynamic Digital Delay enabled	SYSREF_DDLY_PD = 0	5	16.5	—
	Pulser is enabled	SYSREF_PLSR_PD = 0	4.1	13.53	
	SYSREF Pulses mode	SYSREF_MUX = 2	3	9.9	
	SYSREF Continuous mode	SYSREF_MUX = 3	3	9.9	
CLOCK GROUP					
Enabled	Any one of the CLKoutX_Y_PD = 0		20.1	66.33	
IDL	Any one of the CLKoutX_Y_IDL = 1		2.2	7.26	
ODL	Andy one of the CLKoutX_Y_ODL = 1		3.2	10.56	
Clock Divider	Divider Only	DCLKoutX_MUX = 0	13.6	44.88	
	Divider + DCC + HS	DCLKoutX_MUX = 1	17.7	58.41	
	Analog Delay + Divider	DCLKoutX_MUX = 3	13.6	44.88	
CLOCK OUTPUT BUFFERS					
LVDS	100 Ω differential termination		6	19.8	—
HSDS	HSDS 6 mA, 100 Ω differential termination		8.8	29.04	—
	HSDS 8 mA, 100 Ω differential termination		11.6	38.28	—
	HSDS 10 mA, 100-Ω differential termination		19.4	64.02	—
OSCout BUFFERS					
LVDS	100-Ω differential termination		18.5	61.05	—
LVCMOS	LVCMOS Pair	150 MHz	42.6	140.58	—
	LVCMOS Single	150 MHz	27	89.1	—

12 Layout

12.1 Layout Guidelines

12.1.1 Thermal Management

Power consumption of the LMK04828-EP can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature must be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times $R_{\theta JA}$ must not exceed 125°C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to a printed-circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package.

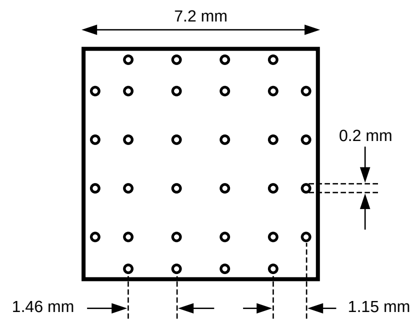
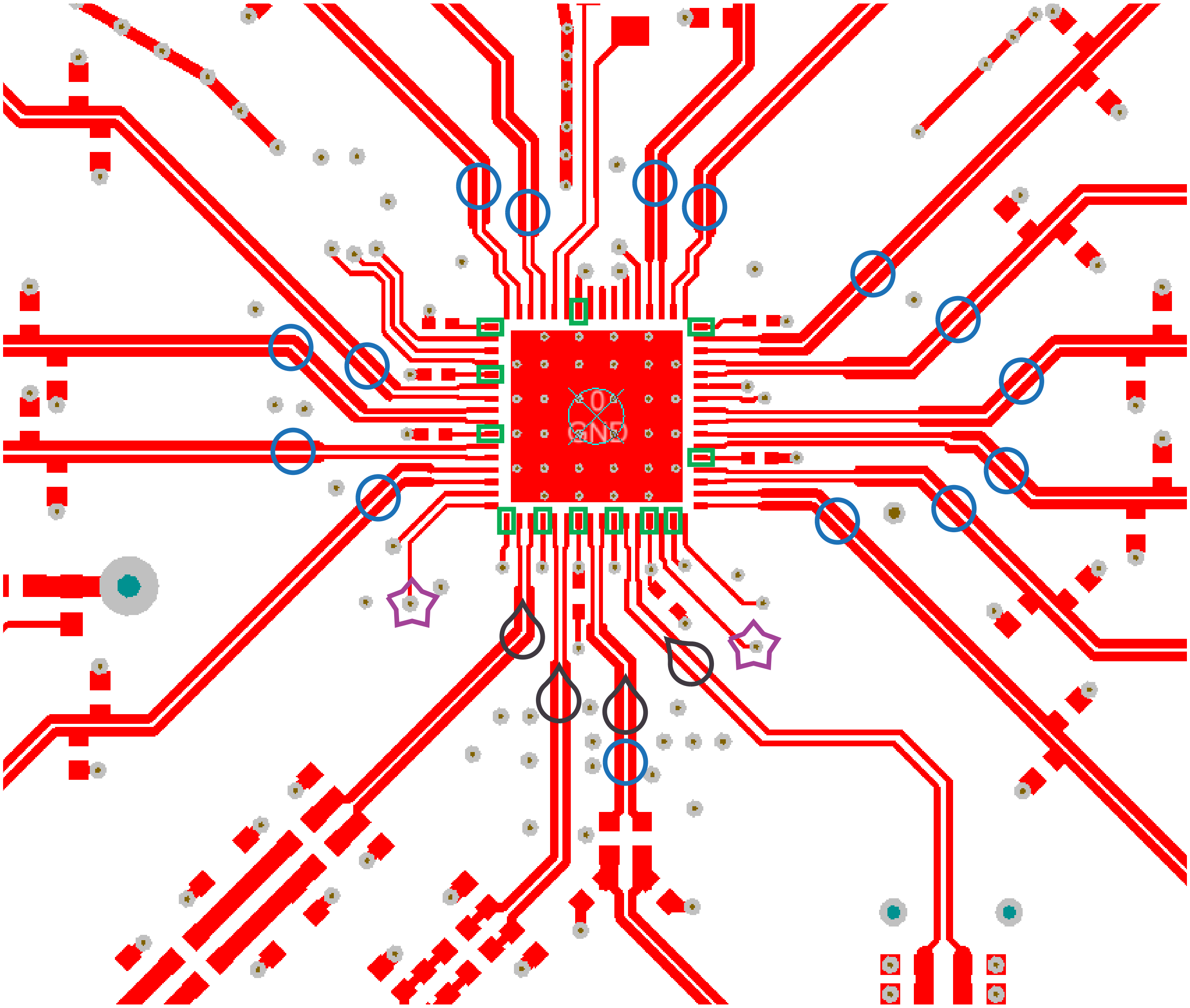


Figure 29. Recommended Land and Via Pattern

12.2 Layout Example



CLKin and OSCin path – if differential input (preferred) route traces tightly coupled. If single ended, have at least 3 trace width (of CLKin/OSCin trace) separation from other RF traces.
When using CLKin1 for high frequency input for external VCO or distribution, a 3 dB pi pad is suggested for termination.
Place terminations close to IC.
CLKin2 and OSCout share pins and is programmable for input or output.

For CLKout Vccs in JESD204B application, place ferrite beads then 1 µF capacitor. The 1 µF capacitor supports low frequency SYSREF switching/turn on. For CLKout Vccs in traditional application place ferrite bead on top layer close to pins to choke high frequency noise from via.

Charge pump output – shorter traces are better. Place all resistors and caps closer to IC except for a single capacitor and associated resistor, if any, next to VCXO. In a 2nd order filter place C1 close to VCXO Vtune pin. In a 3rd and 4th order filter place R3/C3 or R4/C4 respectively close to VCXO.

CLKouts/OSCouts – Normally differential signals, should be routed tightly coupled to minimize PCB crosstalk. Trace impedance and terminations should be designed according to output type being used (i.e. LVDS, LVPECL, LVCMOS). For LVPECL/LCPECL place emitter resistors close to IC. OSCout shares pins with CLKin2 and is programmable for input or output

Figure 30. LMK04828-EP Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support

13.1.1.1 Clock Architect

Part selection, loop filter design, simulation.

For the Clock Architect, go to www.ti.com/clockarchitect.

13.1.1.2 Clock Design Tool

Limited part selection, advanced loop filter design and simulation capabilities. For the Clock Design Tool, go to www.ti.com/tool/clockdesigntool. Note training videos on this tool page.

13.1.1.3 TICS Pro

EVM programming software. Can also be used to generate register map for programming for a specific application.

For TICS Pro, go to www.ti.com/tool/ticspro-sw

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

PLLatinum, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK04828SNKDREP	ACTIVE	WQFN	NKD	64	2000	Non-RoHS & Non-Green	Call TI	Call TI	-55 to 105	4828SNKDEP	Samples
LMK04828SNKDTEP	ACTIVE	WQFN	NKD	64	250	Non-RoHS & Non-Green	Call TI	Call TI		4828SNKDEP	Samples
V62/18602-01XB	ACTIVE	WQFN	NKD	64	2000	Non-RoHS & Non-Green	Call TI	Call TI		4828SNKDEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

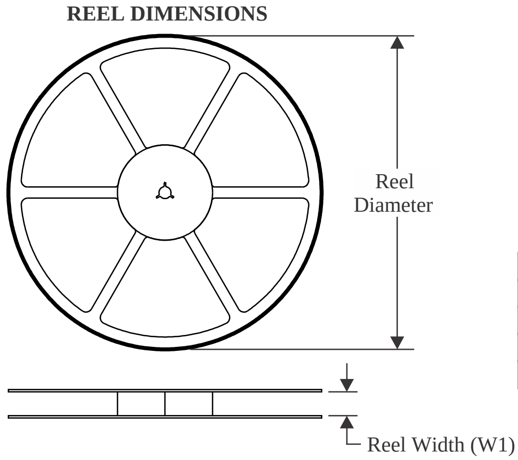
OTHER QUALIFIED VERSIONS OF LMK04828-EP :

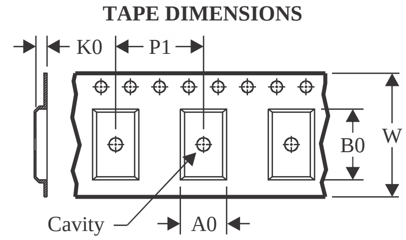
- Catalog : LMK04828

NOTE: Qualified Version Definitions:

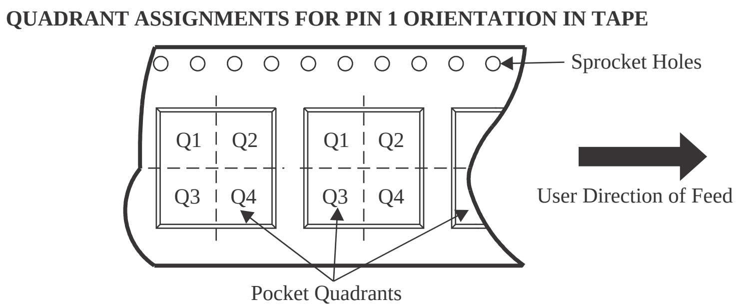
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





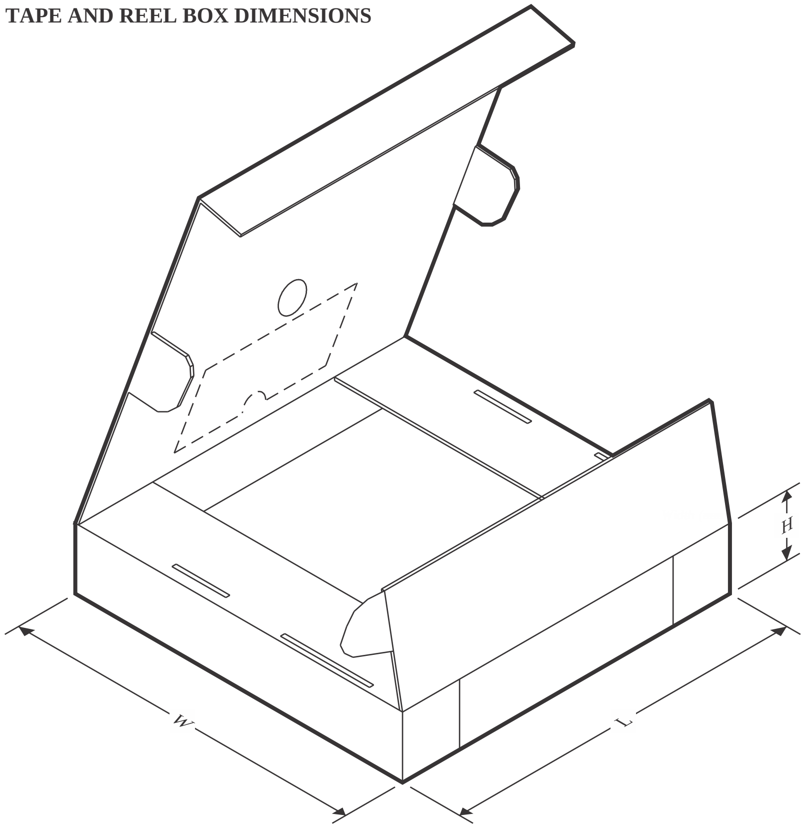
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK04828SNKDREP	WQFN	NKD	64	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
LMK04828SNKDTEP	WQFN	NKD	64	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK04828SNKDREP	WQFN	NKD	64	2000	356.0	356.0	36.0
LMK04828SNKDTEP	WQFN	NKD	64	250	208.0	191.0	35.0

GENERIC PACKAGE VIEW

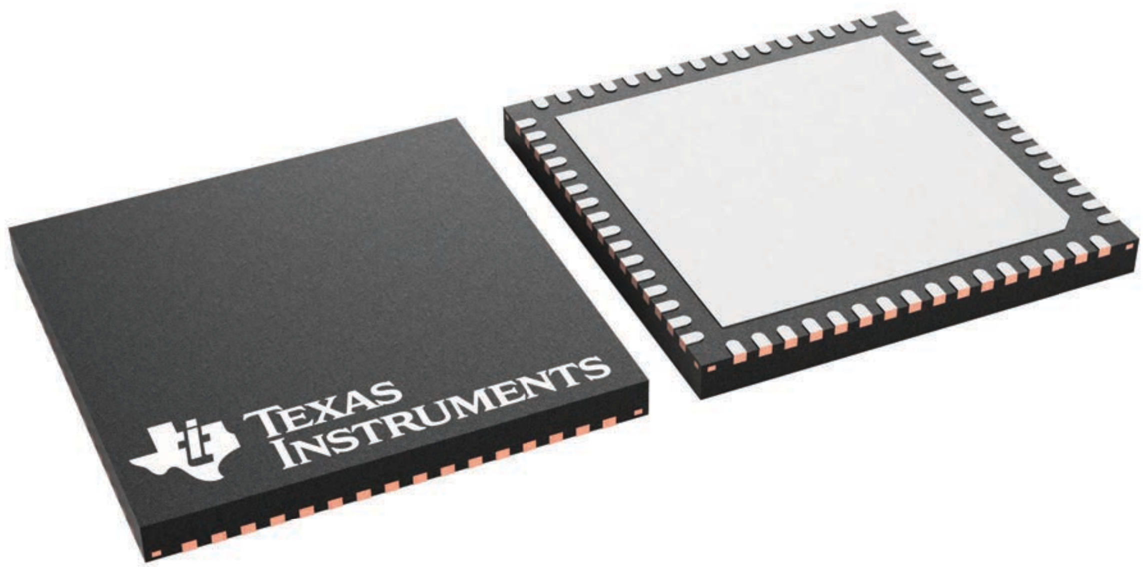
NKD 64

WQFN - 0.8 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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