

LMP93601 Low-Noise, High Gain, 3-Channel AFE for Thermopile Sensors

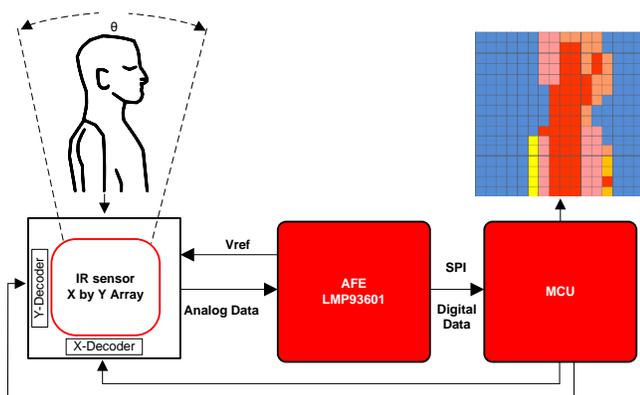
1 Features

- High Gain, Programmable up to 4096
- Low Gain Error Drift, <10 ppm/°C
- Low Offset Voltage and Drift; 1 μ V, 50 nV/°C
- Low Input Bias Current, 1.3 nA
- Low Input Offset Current, 120 pA
- VCM Output Signal for Level Shifting, AVDD/3
- Three Differential EMI Hardened Inputs
- 16-bit $\Delta\Sigma$ Analog-to-Digital Converter
- Low Noise Performance, ENOB 15.3 bits
- Four Output Data Rates, up to 1.3 kSPS
- Internal Voltage Reference for ADC
- SPI Interface Transfer Rate, 20 MHz
- Brown-Out Detect
- PGA Over-Range Detect
- Separate Analog and Digital Supplies, 2.7 to 5.5 V
- Low Current Consumption, 1.1 mA
- Low Power Shutdown Mode, < 0.1 μ A
- Operating Temp. –25 to 85 °C

2 Applications

- Thermopile Array Measurement
- Thermopile Flow Measurements
- Bridge Sensor Interface
- Gesture Recognition

4 Simplified Thermopile Array System Diagram



3 Description

The LMP93601 is an optimized Analog-Front-End (AFE) for occupancy detecting thermopile arrays up to 16 x 16 and thermopile mass flow sensors. The AFE combines excellent noise performance, low offset voltage, high gain, and low-power consumption at sampling rates ideal for monitoring thermopile sensors.

The LMP93601 is a precision, 16-bit, analog-to-digital converter (ADC) offered in a leadless WQFN-24 package. The device features three differential EMI hardened inputs, a low-noise, high-gain programmable gain amplifier (PGA), a level shifting voltage source, an internal reference, and a programmable sampling rate. The many integrated features and the simple control of the LMP93601 through an SPI-compatible interface ease precision measurements of thermopile sensor signals.

Device Information

| PART NUMBER | PACKAGE | BODY SIZE |
|-------------|-----------|-------------------|
| LMP93601 | WQFN (24) | 5.00 mm x 4.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Analog Supply Vs. Offset Voltage Plot

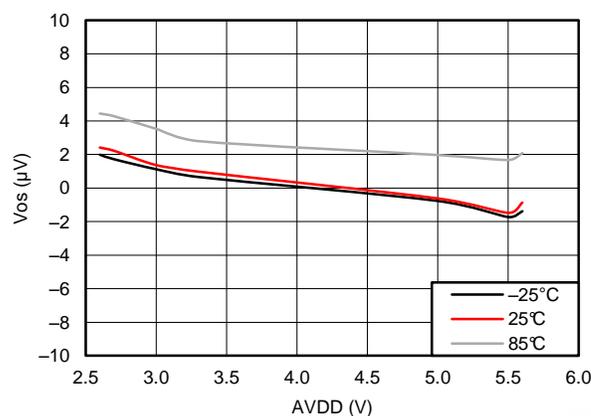


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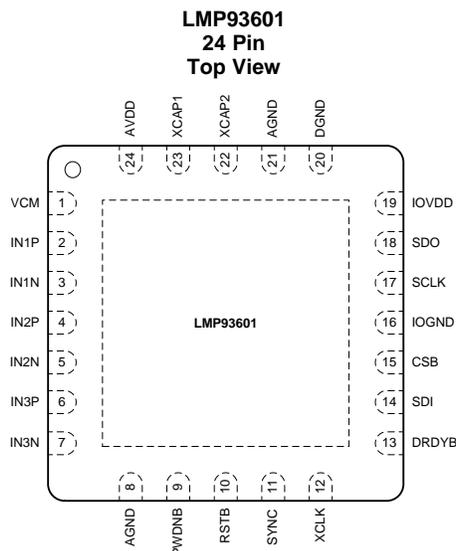
5 Revision History

Changes from Original (March 2014) to Revision A

Page

| | |
|---|---|
| • Added application curves | 3 |
| • Changed Handling Ratings format | 3 |

6 Pin Configuration and Functions



Pin Functions

| PIN ⁽¹⁾ | | TYPE(I/O) ⁽²⁾ | DESCRIPTION |
|--------------------|--------|--------------------------|--|
| NAME | NUMBER | | |
| VCM | 1 | Analog in/output | Sensor common mode bias voltage |
| INP1 | 2 | Analog input | Input signal positive pin |
| INN1 | 3 | Analog input | Input signal negative pin |
| INP2 | 4 | Analog input | Input signal positive pin |
| INN2 | 5 | Analog input | Input signal negative pin |
| INP3 | 6 | Analog input | Input signal positive pin |
| INN3 | 7 | Analog input | Input signal negative pin |
| AGND | 8 | Analog ground | |
| PWDNB | 9 | Digital input | Enable, active low |
| RSTB | 10 | Digital input | Master reset, active low |
| SYNC | 11 | Digital input | Sync, active high |
| XCLK | 12 | Digital input | External clock source |
| DRDYB | 13 | Digital output | Data ready signal, active low, push-pull |
| SDI | 14 | Digital input | Serial data input |
| CSB | 15 | Digital input | Chip select, active low |
| IOGND | 16 | Digital IO ground | |
| SCLK | 17 | Digital input | Serial interface clock |
| SDO | 18 | Digital output | Serial data output; push-pull |
| IOVDD | 19 | Digital IO supply rail | |
| DGND | 20 | Digital ground | |
| AGND | 21 | Analog ground | |
| XCAP2 | 22 | Digital LDO | External Cap2 |
| XCAP1 | 23 | Analog | External Cap1 |
| AVDD | 24 | Analog | Analog supply rail |

(1) For best performance, it is recommended that the DAP is connected to AGND (refer to *Mechanical, Packaging and Orderable Information*). All three "GND" connections (AGND, DGND and IOGND) must be connected to system ground and cannot be left floating.

(2) There is no pull-up/-down for any digital I/O

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | MIN | MAX | UNIT |
|---|------|------|------|
| Analog Supply Voltage, AVDD | -0.3 | 6.0 | V |
| Digital Supply Range, IOVDD; (IOVDD must always be lower than or equal to AVDD supply) | -0.3 | 6.0 | V |
| Voltage between any two analog pins | | 6.0 | V |
| Voltage between any two digital pins | | 6.0 | V |
| Voltage between XCAP2 and any GND (A, D or IO) | | 2.2 | V |
| Input current at any pin | -5.0 | +5.0 | mA |
| Junction Temperature | | 125 | °C |

(1) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

| | MIN | MAX | UNIT |
|--------------------|---------------------------|--|-------------|
| T _{stg} | Storage temperature range | | 150 °C |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 2000 K V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 500 |

(1) JEDEC document JEP155 states that 2000 -V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

| | MIN | MAX | UNIT |
|-------------------------------|---------------------|------|------|
| Analog Supply Voltage, AVDD | 2.7 | 5.5 | V |
| F _{clk} | 3.6 | 4.4 | MHz |
| Digital Supply Voltage, IOVDD | 2.7 | AVDD | V |
| Supply Ground | AGND = DGND = IOGND | | |
| Temperature range | -25 | 85 | °C |

7.4 Thermal Information

| SYMBOL | THERMAL METRIC | WQFN 24 PINS | UNIT |
|-----------------|---|-----------------|------|
| Θ _{JA} | Thermal resistance, junction to ambient | 37.9 | °C/W |
| Θ _{JC} | Thermal resistance, junction to case | 4.8 | °C/W |
| Ψ _{JB} | Thermal resistance, junction to board | 19.4 | °C/W |

7.5 Electrical Characteristics

Typical conditions: $T_A=+25^{\circ}\text{C}$, $AV_{DD}=IOV_{DD}=3.3\text{ V}$, INP1/INN1 enabled with $V_{ICM}=AV_{DD}/3$. PGA gain=64, PGA over-range masked, digital gain=1. SPS select=1057 SPS. $f_{CLK}=4.00\text{ MHz}$. Conversion power mode. XCAP1=1 μF . XCAP2=0.1 μF .

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|-------------------|---|---|-----|-----------------------|-----------|--------------------------------|
| INPUTS | | | | | | |
| XTLK | Crosstalk across input channels | Channel1 enabled with a 100 k Ω resistor as input, channel 2 disabled with 1 V peak-peak , 100 Hz signal as input. | | 80 | | dB |
| Z _{in} | Differential input impedance | | | 10//7 | | M Ω //pF ⁽¹⁾ |
| | Common mode input impedance | | | 100//4.5 | | M Ω //pF ⁽¹⁾ |
| I _B | Input bias current | | | -1.3 | | nA |
| I _{os} | Input offset current on differential channels | Maximum of INP1-INN1, ..., INP3-INN3 | | -200 | | pA |
| TCI _{os} | Input offset current drift on differential channels | Maximum of INP1-INN1, ..., INP3-INN3 | | -0.5 | | pA/ $^{\circ}\text{C}$ |
| V _{os} | Input referred offset voltage | Input short on chip, PGA 64 DG =1, CH1 | -15 | 1 | +15 | μV ⁽²⁾ |
| TCV _{os} | Input referred offset drift with temperature | Input short on chip | | 50 | | nV/ $^{\circ}\text{C}$ |
| V _{diff} | Input differential range for AVDD \geq 3V | Programmable gain settings =16; $\pm 3\%$ | -64 | | +64 | mV |
| | | Programmable gain settings =32; $\pm 3\%$ | -32 | | +32 | |
| | | Programmable gain settings =64; $\pm 3\%$ | -16 | | +16 | |
| | | Programmable gain settings = 128; $\pm 3\%$ | | ± 8 | | |
| | | PGA bypass | | | ± 1 | |
| V _{ICM} | Input common mode range. | PGA = 64 V/V; CMRR \geq 80 dB | 0.3 | | AVDD-1.4 | V ⁽³⁾ |
| | | PGA = 64 V/V ; CMRR \geq 72 dB -25 C to 85 C | 0.4 | | AVDD-1.45 | |
| BW | Channel bandwidth | | | See Figure 16 | | Hz |
| ODR | Output data rate | | | 265 | | SPS |
| | | | | 530 | | |
| | | | | 1057 | | |
| | | | | 1326 | | |
| PGA | Programmable gain settings | | | 16, 32 , 64 and 128 | | V/V |
| | Bypass mode | | | 1 | | V/V |
| Digital Gain | Programmable gain settings | | | 1, 2, 4, 8, 16 and 32 | | V/V |
| Total AFE Gain | Programmable gain settings (analog and digital) | | | 16 - 4096 | | V/V |
| | Gain steps | | | 2 x | | |
| GE | Gain error | | | 0.3 % | | |
| | | PGA bypassed | | -0.3 % | | |
| | GE drift with temperature | | | -9 | | ppm/ $^{\circ}\text{C}$ |

(1) Value from simulation

(2) The input referred offset is measure by an on-chip short.

(3) Temperature limits are ensured by statistical analysis or design

Electrical Characteristics (continued)

Typical conditions: $T_A = +25^\circ\text{C}$, $AV_{DD} = IOV_{DD} = 3.3\text{ V}$, INP1/INN1 enabled with $V_{ICM} = AV_{DD}/3$. PGA gain=64, PGA over-range masked, digital gain=1. SPS select=1057 SPS. $f_{XCLK} = 4.00\text{ MHz}$. Conversion power mode. XCAP1=1 uF. XCAP2=0.1 uF.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---------------------------------------|--|--------------------|---------------------|-----------------|-------------------|
| ENOB ⁽⁴⁾ | Effective number of bits | | | 15.3 | | Bits |
| THD | Total harmonic distortion (Linearity) | 100 Hz, 50 mVpp differential input, PGA 16 V/V | | 91 | | dB |
| Noise | RMS noise in a 1 kHz BW | PGA = 64 V/V | | 0.67 ⁽⁵⁾ | | uVrms |
| | 1/f noise corner | | | 1 | | Hz |
| CMRR | Common mode rejection ratio (at DC) | $V_{ICM} = 0.3\text{ to }AV_{DD}-1.4\text{ V}$ | 80 | 127 | | dB ⁽³⁾ |
| | | $V_{ICM} = 0.4\text{ to }AV_{DD}-1.45\text{ V}$, over operating temperature range -25 C to 85 C | 72 | 127 | | |
| PSRR | Power supply rejection ratio (at DC) | Supply ; 2.7 to 5.5 V | 80 | 120 | | dB ⁽³⁾ |
| | | Supply ; 2.7 to 5.5 V, over operating temperature range -25 C to 85 C | 72 | 120 | | |
| EMIRR | EMI rejection ratio | VRF = 100 mVPP | | | | dB |
| | | f=400 MHz | | 86 | | |
| | | f=900 MHz | | 87 | | |
| | | f=1800 MHz | | 85 | | |
| | | f=2400 MHz | | 84 | | |
| VCM | | | | | | |
| V_{VCM} | Output voltage | | | $AV_{DD}/3$ | | V |
| T_{strp_VCM} | Startup time | To within 90% of final value | | 10 | | ms |
| Acc_{VCM} | Accuracy | | | 0.2 | | % |
| TC_{VCM} | Drift over temperature | | | 0.5 | | ppm/°C |
| I_{VCM} | Output current | | | 0.5 | | mA |
| | Load regulation | 0 to 200uA | | 4 | 15 | mV |
| $Zload_{VCM}$ | Load range | | | 2.2//100 | | MΩ/nF |
| SLAVE SPI INTERFACE | | | | | | |
| | Clock frequency | | | 1 | 20 | MHz |
| DIGITAL INPUT/OUTPUT CHARACTERISTICS | | | | | | |
| V_{IH} | Logical "1" Input Voltage | | 0.7x | | | V |
| V_{IL} | Logical "0" Input Voltage | | | 0.3x | | V |
| V_{OH} | | $I_{source} = 300\mu\text{A}$ | $IOV_{DD} - 0.150$ | | | |
| V_{OL} | | $I_{sink} = 300\mu\text{A}$ | | | $IOGND + 0.150$ | |
| POWER SUPPLY | | | | | | |
| AV_{DD} | Analog supply voltage range | | 2.7 | | 5.5 | V |
| IOV_{DD} | Digital supply voltage range | $AV_{DD} \geq IOV_{DD}$ | | | AV_{DD} | V ⁽⁶⁾ |

(4) ENOB is a DC ENOB spec, not the dynamic ENOB that is measured using FFT and SINAD:

$$ENOB = \log_2 \left[\frac{2 \times V_{ref} / Gain}{RMSNoise} \right]$$

(5) See Table 1 for detailed noise performance

(6) IOV_{DD} always $\leq AV_{DD}$ and IOV_{DD} minimum is 2.7 V

Electrical Characteristics (continued)

Typical conditions: $T_A=+25^{\circ}\text{C}$, $AV_{DD}=IOV_{DD}=3.3\text{ V}$, INP1/INN1 enabled with $V_{ICM}=AV_{DD}/3$. PGA gain=64, PGA over-range masked, digital gain=1. SPS select=1057 SPS. $f_{XCLK}=4.00\text{ MHz}$. Conversion power mode. XCAP1=1 uF. XCAP2=0.1 uF.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--------------------------|----------------|---|-----|-----|-----|--------------------|
| SUPPLY CURRENT | | | | | | |
| I_{IOVDD} | Digital on AFE | Shutdown Mode, XCLK off | | 0.1 | 1 | μA |
| | | Standby Mode | | 1.9 | 25 | μA |
| | | Conversion Power Mode | | 2.7 | 25 | μA |
| | | Conversion Power Mode, PGA bypassed | | 3 | | μA |
| I_{AVDD} | Analog on AFE | Shutdown Mode, XCLK off | | 0.1 | 1 | μA |
| | | Standby Mode | | 175 | 250 | μA |
| | | Conversion Power Mode | | 1.1 | 1.6 | mA |
| | | Conversion Power Mode, 230 μA PGA bypassed | | 230 | | μA |
| TEMPERATURE RANGE | | | | | | |
| | Operating | | -25 | | 85 | $^{\circ}\text{C}$ |

7.6 Timing Requirements

Under typical conditions with maximum total load capacitance 10 pF.

| | | MIN | TYP | MAX | UNIT |
|-----------|----------------------|-----|-----|------|------|
| t_{PH} | High Period, SCLK | 25 | | | ns |
| t_{PL} | Low Period, SCLK | 25 | | | ns |
| t_{SU} | SDI input setup time | 10 | | | ns |
| t_H | SDI input hold time | 10 | | | ns |
| t_{OD} | SDO output hold time | | | 13.5 | ns |
| t_{CSS} | CSB setup time | 25 | | | ns |
| t_{CSH} | CSB hold time | 25 | | | ns |
| t_{IAG} | CSB high time | 50 | | | ns |

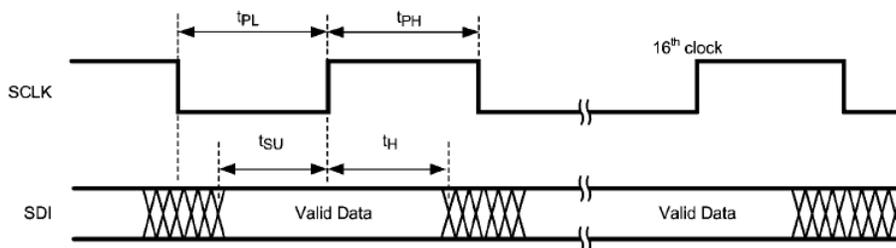


Figure 1. SPI Write Timing Diagram

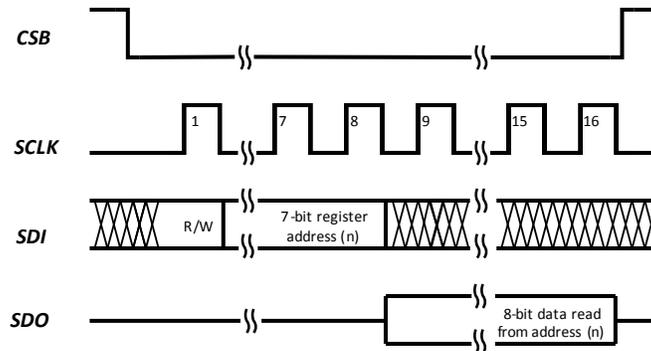


Figure 2. SPI Read Timing Diagram

7.7 Noise Performance

Table 1. Noise In μV_{RMS} at $AVDD = 3.3 V$, $AGND = 0 V$, and Internal Reference = $2.4 V_{RMS}$

| ODR (SPS) | PGA Gain (V/V) | D-Gain (V/V) | Vn (μV_{RMS}) |
|-----------|----------------|--------------|---|
| 265 | 16 | 1 | Below the resolution of the 16 bit SDM. |
| | | 2 | Below the resolution of the 16 bit SDM. |
| | | 4 | 0.661 |
| | | 8 | 0.597 |
| | | 16 | 0.578 |
| | | 32 | 0.574 |
| | 32 | 1 | Below the resolution of the 16 bit SDM. |
| | | 2 | 0.516 |
| | | 4 | 0.396 |
| | | 8 | 0.368 |
| | | 16 | 0.361 |
| | | 32 | 0.362 |
| | 64 | 1 | 0.556 |
| | | 2 | 0.321 |
| | | 4 | 0.287 |
| | | 8 | 0.281 |
| | | 16 | 0.275 |
| | | 32 | 0.277 |
| | 128 | 1 | 0.298 |
| | | 2 | 0.254 |
| 4 | | 0.247 | |
| 8 | | 0.242 | |
| 16 | | 0.242 | |
| 32 | | 0.240 | |

Noise Performance (continued)
Table 1. Noise In μV_{RMS} at AVDD= 3.3 V, AGND = 0 V, and Internal Reference = 2.4 V_{RMS} (continued)

| ODR (SPS) | PGA Gain (V/V) | D-Gain (V/V) | Vn (μV_{rms}) |
|-----------|----------------|--------------|---|
| 530 | 16 | 1 | Below the resolution of the 16 bit SDM. |
| | | 2 | 0.944 |
| | | 4 | 0.888 |
| | | 8 | 0.831 |
| | | 16 | 0.810 |
| | | 32 | 0.816 |
| | 32 | 1 | 0.509 |
| | | 2 | 0.609 |
| | | 4 | 0.543 |
| | | 8 | 0.517 |
| | | 16 | 0.521 |
| | | 32 | 0.511 |
| | 64 | 1 | 0.569 |
| | | 2 | 0.421 |
| | | 4 | 0.397 |
| | | 8 | 0.396 |
| | | 16 | 0.397 |
| | | 32 | 0.395 |
| | 128 | 1 | 0.377 |
| | | 2 | 0.348 |
| | | 4 | 0.340 |
| | | 8 | 0.341 |
| | | 16 | 0.340 |
| | | 32 | 0.339 |

Noise Performance (continued)
Table 1. Noise In μV_{RMS} at AVDD= 3.3 V, AGND = 0 V, and Internal Reference = 2.4 V_{RMS} (continued)

| ODR (SPS) | PGA Gain (V/V) | D-Gain (V/V) | Vn (μV_{RMS}) |
|-----------|----------------|--------------|-----------------------------------|
| 1057 | 16 | 1 | 1.565 |
| | | 2 | 1.517 |
| | | 4 | 1.410 |
| | | 8 | 1.409 |
| | | 16 | 1.398 |
| | | 32 | 1.401 |
| | 32 | 1 | 0.932 |
| | | 2 | 0.903 |
| | | 4 | 0.834 |
| | | 8 | 0.839 |
| | | 16 | 0.829 |
| | | 32 | 0.824 |
| | 64 | 1 | 0.667 |
| | | 2 | 0.596 |
| | | 4 | 0.580 |
| | | 8 | 0.580 |
| | | 16 | 0.579 |
| | | 32 | 0.574 |
| | 128 | 1 | 0.501 |
| | | 2 | 0.481 |
| | | 4 | 0.476 |
| | | 8 | 0.476 |
| | | 16 | 0.473 |
| | | 32 | 0.470 |

Noise Performance (continued)
Table 1. Noise In μV_{RMS} at AVDD= 3.3 V, AGND = 0 V, and Internal Reference = 2.4 V_{RMS} (continued)

| ODR (SPS) | PGA Gain (V/V) | D-Gain (V/V) | Vn (μV_{RMS}) |
|-----------|----------------|--------------|-----------------------------------|
| 1326 | 16 | 1 | 2.331 |
| | | 2 | 1.743 |
| | | 4 | 1.743 |
| | | 8 | 1.665 |
| | | 16 | 1.648 |
| | | 32 | 1.681 |
| | 32 | 1 | 1.189 |
| | | 2 | 0.975 |
| | | 4 | 0.981 |
| | | 8 | 0.954 |
| | | 16 | 0.941 |
| | | 32 | 0.937 |
| | 64 | 1 | 0.733 |
| | | 2 | 0.677 |
| | | 4 | 0.670 |
| | | 8 | 0.667 |
| | | 16 | 0.660 |
| | | 32 | 0.663 |
| | 128 | 1 | 0.575 |
| | | 2 | 0.546 |
| | | 4 | 0.541 |
| | | 8 | 0.537 |
| | | 16 | 0.540 |
| | | 32 | 0.538 |

7.8 Typical Characteristics

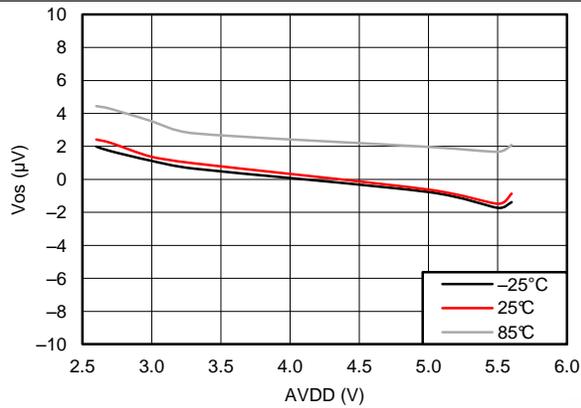


Figure 3. Vos vs AVDD (V)

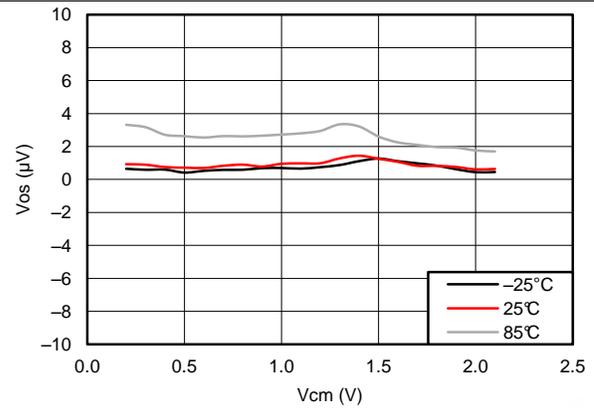


Figure 4. Vos vs Vcm (V)

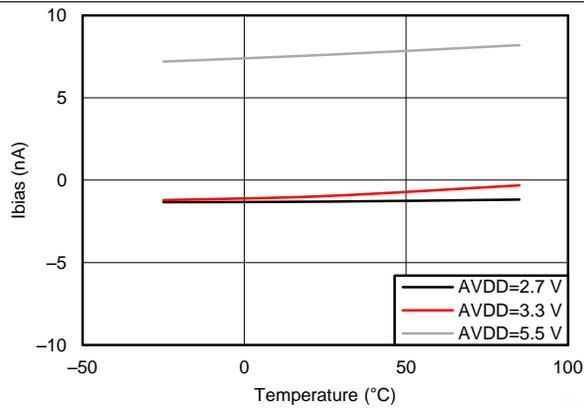


Figure 5. Ibias vs Temperature

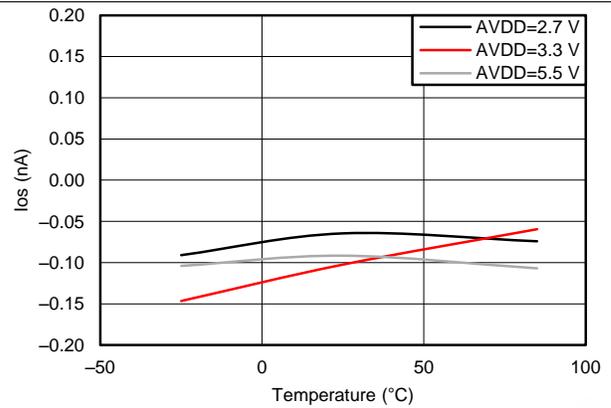


Figure 6. Ios vs Temperature

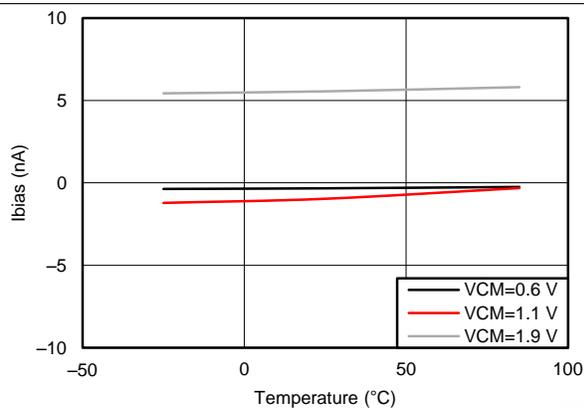


Figure 7. Ibias vs Temperature

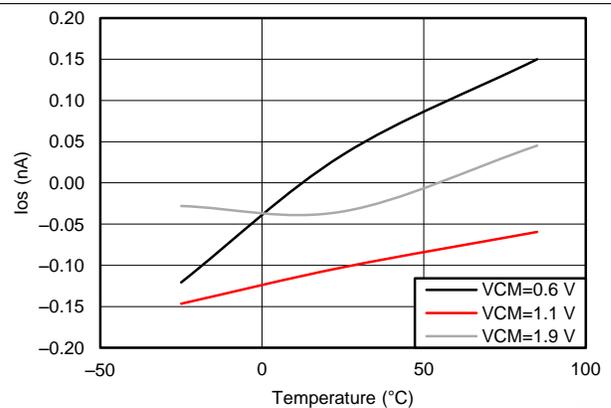


Figure 8. Ios vs Temperature

Typical Characteristics (continued)

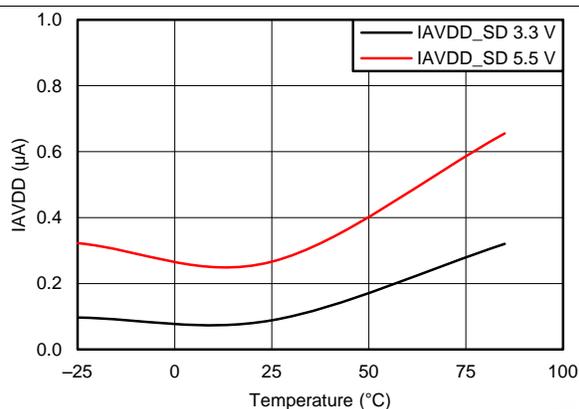


Figure 9. IAVDD vs Temperature

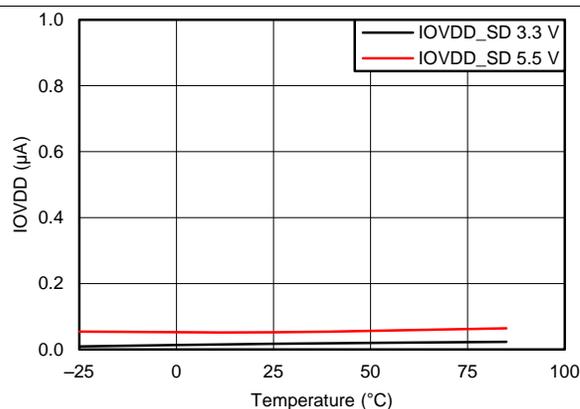


Figure 10. IOVDD vs Temperature

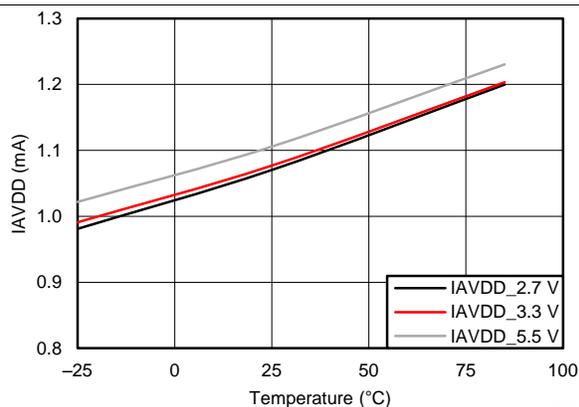


Figure 11. IAVDD vs Temperature

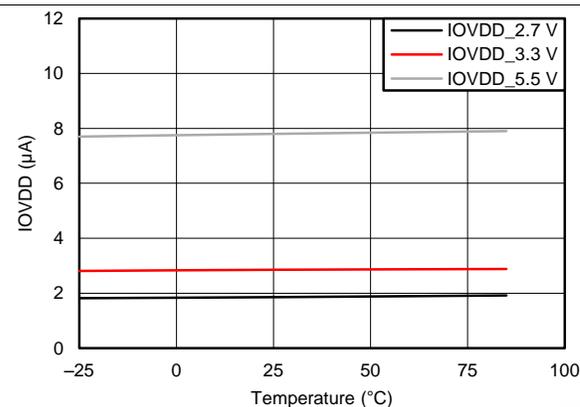


Figure 12. IOVDD vs Temperature

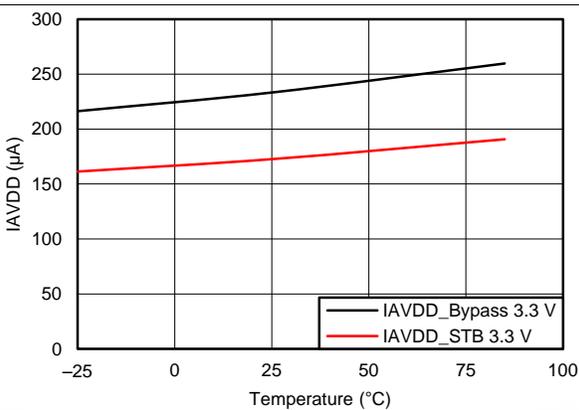


Figure 13. IAVDD vs Temperature

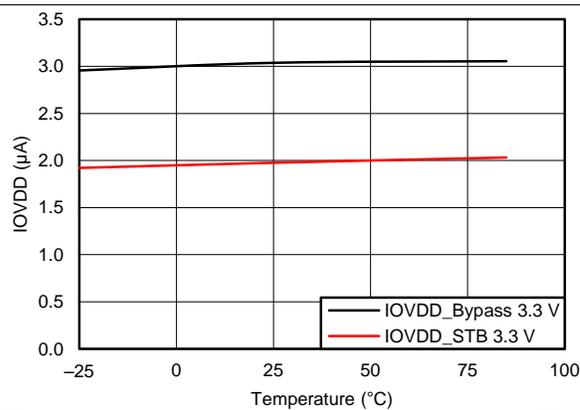


Figure 14. IOVDD vs Temperature

Typical Characteristics (continued)

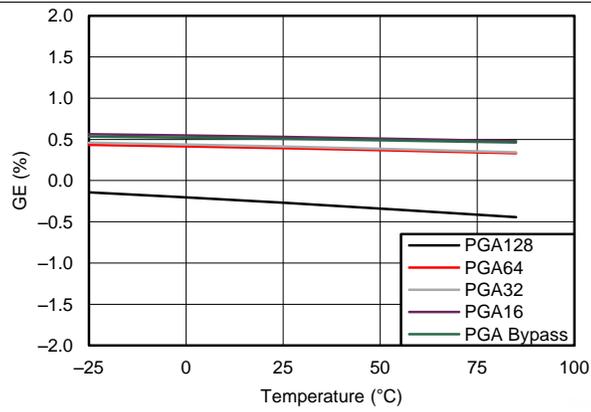


Figure 15. GE (%) vs Temperature

8 Detailed Description

8.1 Overview

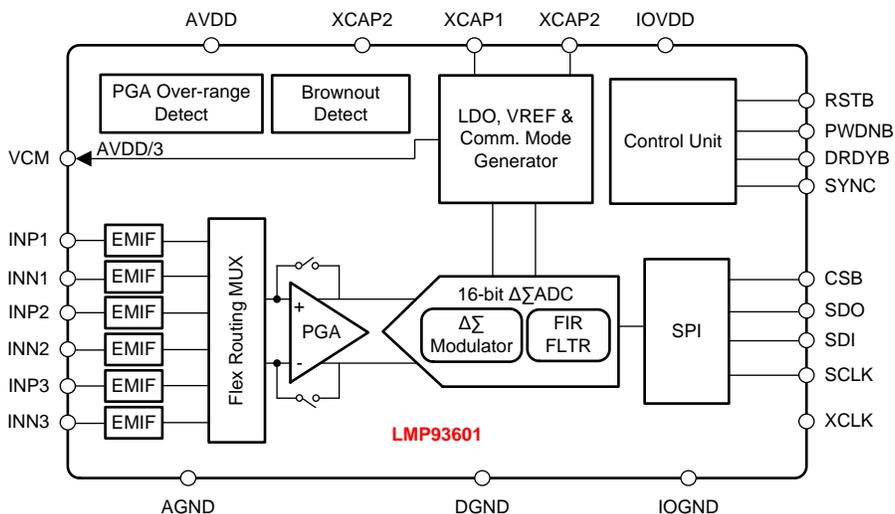
The LMP93601 Analog-Front-End is a unique device designed from ground up specifically for interfacing to 16 x 16 MEMS (Micro-electro-mechanical systems) thermopile arrays, and thermopile mass flow sensors with very low output signals in the range of 1 μV to 600 μV . For signal conditioning of thermopile sensors, the AFE is required to have very low noise performance, very low offset voltage, very high gain, and low-power consumption at sampling rates to process several frames per second.

The signal chain includes a PGA featuring low offset voltage (0.7 μVrms), low input bias current (-1.3 nA), and programmable gain of 1x, 16x, 32x, 64x and 128x. The total gain of the signal path combined with the programmable digital gain of the 16-bit Delta-Sigma data converter is up to 4096x.

The signal chain features excellent total noise performance of below 0.5 μVrms at programmable sampling rates of up to 1.3 kSPS, while providing optimal power consumption during full operation (1.1 mA). The device features ultra-low shutdown current (0.1 μA), and standby mode current of 250 μA .

Other features include Low EMI sensitivity due to EMI hardened input stage, Internal reference voltage for the ADC, output reference voltage for thermopile sensors (VCM), a brown-out detector for low-battery condition, synchronous serial communication (SPI) communication up to 20 MHz, flex routing multiplexer for interfacing to multiple flow sensors, and PGA over range detection.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Data Format

The LMP93601 provides 16 bits of data in binary two's complement format. The positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale (FS). [Table 2](#) summarizes the ideal output codes for different input signals.

8.3.2 Transfer Function

The ADC output code in decimal is given by the relation:

$$\text{code}_{\text{dec}} = \frac{\text{Vdiff} \times \text{PGA} \times \text{DG} \times 2^{16}}{2 \times \text{Vref}} \quad (1)$$

Table 2. Example of ADC Output Code

| CODE (HEX) | CODE (DEC) | PGA (V/V) | DG (V/V) | VDIF (V) |
|------------|------------|-----------|----------|------------|
| 1946 | 6470 | 64 | 1 | 7.404E-3 |
| 3000 | 12288 | 16 | 4 | 14.063E-3 |
| D0FC | -12036 | 16 | 1 | -55.096E-3 |
| FFFC | -4 | 64 | 1 | -4.578E-6 |

8.3.3 Input Routing Mux

The LMP93601 offers 5 differential input channel configurations for its 3 differential input pairs:

- For 1-ch system: One of the 3 channels, Ch1, Ch2, or Ch3 is enabled
- For 2-ch system: Ch1 & Ch2 are enabled
- For 3-ch system: Ch1, Ch2, Ch3 are enabled

8.3.4 Programmable Gain Amplifier

The PGA provides a high input impedance to interface with signal sources that may have relatively high output impedance, such as thermopiles. The Programmable Gain amplifier gain can be programmed to 16, 32 64, and 128 V/V.

The maximum differential input voltage (Vdiff) of the PGA is ± 64 mV when the programmed analog gain is 16 V/V. With analog gain programmed to 64V/V the maximum differential input voltage of the PGA is ± 16 mV.

The input common mode voltage range of the PGA is $\text{AGND} + 0.3 + \text{Vdiff} \times \text{Gain} / 2$ to $\text{AVDD} - 1.40 - \text{Vdiff} \times \text{Gain} / 2$.

The PGA also has an EMIRR filter incorporated. The EMIRR filter is a single pole roll off providing enhanced noise immunity for unwanted RF signals.

8.3.5 PGA Bypass Mode

The PGA can be bypassed to access the 16 bit Delta-Sigma modulator directly. This mode results in a typical gain of 1 V/V at a supply current of typically 230 μA . The input common mode range in the PGA-bypass mode is rail to rail and the maximum differential input voltage that can be applied to the Delta-Sigma modulator is ± 1.2 Vpp differential. The typical noise at 1057 SPS is 20 μVrms . Typical input impedance in the PGA bypass mode is 1.3 M Ω //7 pF. In the PGA-bypass mode, the PGA and overrange detectors are disabled. To access the PGA-bypass mode the following SPI write sequence must be followed in this exact order:

Table 3. PGA Bypass Mode SPI Write Sequence

| ADDRESS | WRITE | DESCRIPTION |
|---------|-----------------------------------|--|
| 0x1 | Program as normal | |
| 0x02 | Program as normal | |
| 0x03 | See Table 4 below | |
| 0x05 | 8'h01 | Mask PGA OR detectors (else the conversion will read 7FFF) |
| 0x60 | 8'h93 | First write to address 0x60 |

Table 3. PGA Bypass Mode SPI Write Sequence (continued)

| ADDRESS | WRITE | DESCRIPTION |
|---------|-------|--------------------------------------|
| 0x60 | 8'h60 | Second write to address 0x60 |
| 0x63 | 8'h10 | Override |
| 0x61 | 8'h28 | PGA bypass and OR detectors shutdown |
| 0x04 | 8'h01 | Conversion mode |
| 0x00 | 8'h01 | lock |

Table 4. PGA Bypass Register 0x03 Setting Description

| ADDR [6:0] | NAME | # OF BITS | TYPE | DEFAULT | DESCRIPTION |
|------------|---------|-----------|------|---------|---|
| 0x03 | Config3 | 5 | R/W | 8'h52 | PGA settings for differential channels [6:4] Digital 3'b000: 1 3'b001: 2 3'b010: 4 3'b011: 8 3'b100: 16 3'b101: 32(default) 3'b110-111: Reserved [1:0] Analog 2'b00: 16 2'b01: 32 2'b10: 64 (default) 2'b11: 128 [7] always 0 [2] Bypass PGA, bit [1:0] would be ignored |

To exit the PGA-bypass mode, a reset is required, either via the RSTB or SPI. Failure to follow this exact sequence may result in the device becoming unresponsive, thereby requiring a reset, either via the RSTB or SPI.

8.3.6 Over-Range Detection

The PGA has over-range detection and when signals are outside the minimum or maximum allowed signal, an out of range condition will be reported as “0x7FFF” for the corresponding channel. A status register provides further details of the out of range condition. The overrange detectors are at the output of the PGA and check for five conditions:

- PGA positive output low
- PGA negative output low
- PGA positive output high
- PGA negative output high
- PGA differential output high

The “output high” overrange detectors typically trip at AVDD-1.28 V. Both “output low” overrange detectors typically trip at 0.11 V and the differential overrange detector is typically at +1.22 and -1.22 V differential.

For example, if the input common mode is below 0.11 V and a zero differential voltage (shorted input) is applied, both the PGA positive and PGA negative “output low” detectors would trip. Likewise, if the input common mode is over AVDD-1.28 and a zero differential voltage (shorted input) is applied, both the PGA positive and PGA negative “output high” detectors would trip.

For the differential output high detector to trip, the output of the PGA has to be greater than 1.22 V or less than -1.22 V. At a gain of 64, this would translate to an input referred differential voltage of $V_{diff} = 1.22/64 = 19 \text{ mV}$

8.3.7 Analog-To-Digital Converter (ADC)

The 16 bit Sigma Delta Modulator (SDM) takes the output signal of the PGA and converts this signal into a high resolution bit stream that is further processed by the digital filters. The 2.4 V reference for the SDM is internally generated and requires a high-performance, low ESR (<0.1 Ω), and Low ESL(<1nH) 1uF (±10%) external bypass capacitor for optimal performance on the XCAP1 pin. This reference should not be used to drive external circuitry.

The SDM clock uses a divided-down external clock (XCLK).

8.3.8 Programmable Digital Filters

A programmable digital filter behind the SDM reconstructs the signal from the SDM output bit stream. The filter consists of programmable filter stages. Each of the stages further filters and decimates the bit stream so that the data rate and bandwidth of the signal is reduced and at the same time the resolution is enhanced.

An example of the filter response when programmed for 265, 530, 1057 or 1326 SPS is shown in Figure 16.

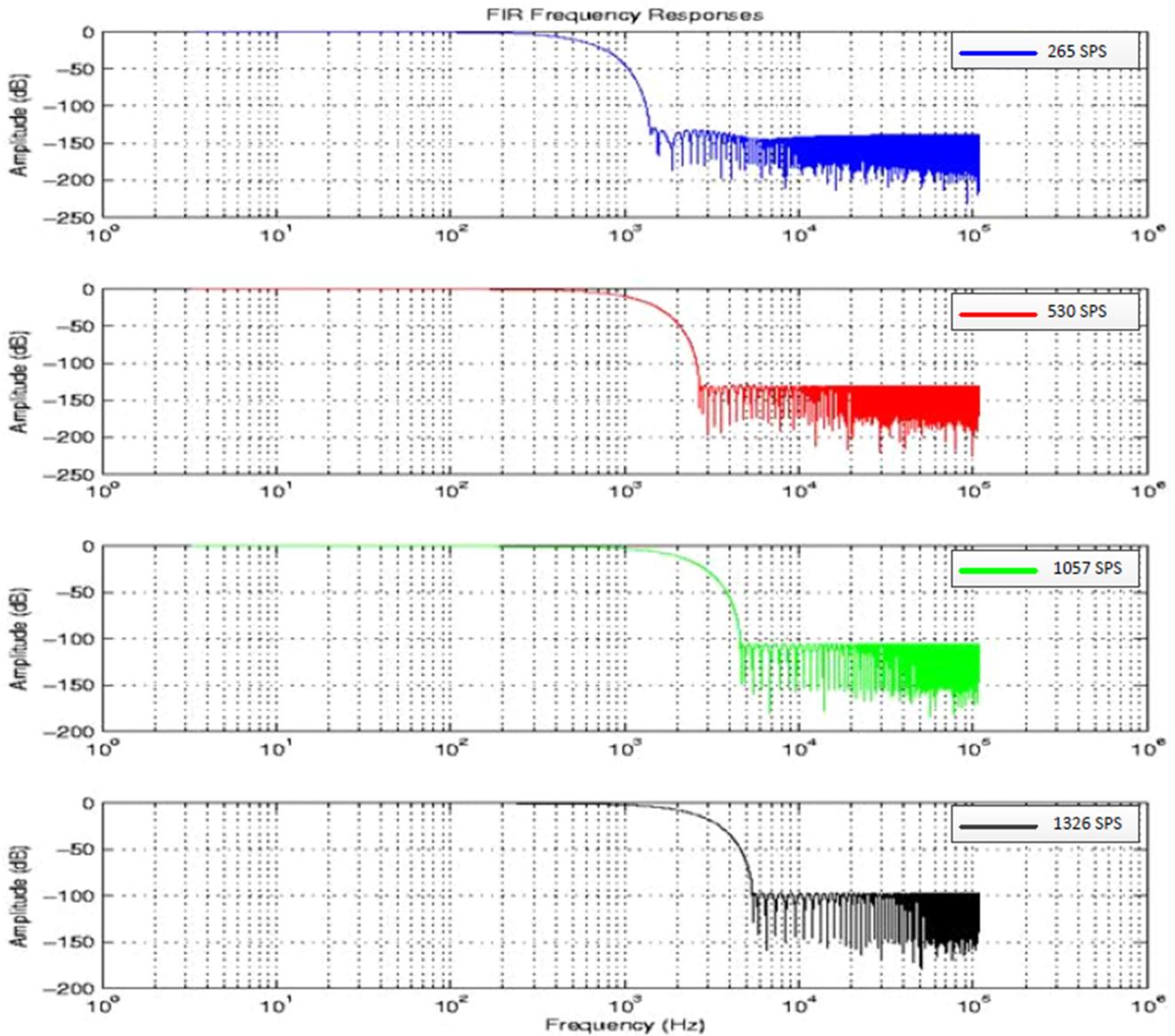


Figure 16. Bandwidth and Module Noise Performance

8.3.9 Common Mode Voltage Generator

The common mode reference generator (VCM) provides an AVDD/3 reference. It can drive a 100nF ($\pm 10\%$) external capacitance with typical ESR/ESL of 0.1 Ω and 1 nH. It can also be used to drive guard traces placed around the input PCB traces to reduce PCB leakage currents to the inputs. The VCM can be disabled with the Reference Enable register. In case the VCM is disabled, an external common mode voltage that tracks the common mode of the input channel(s) needs to be connected to the VCM pin to function as a reference for the over-range detection circuitry. In case the VCM is disabled, it is recommended to add an external 10 k Ω series resistor.

8.3.10 Low Drop-Out Regulator (LDO)

The on chip LDO generates 1.2V for the digital core. A 100nF ($\pm 10\%$) external capacitance with low ESR/ESL (typical 0.1 ohm and 1 nH) is required on the XCAP2 pin to provide adequate supply bypass for the internal digital core. The LDO should not be used to drive external circuitry.

8.3.11 External Clock

The LMP93601 does not have an internal oscillator and needs an external clock, XCLK. The XCLK needs to be running all the time when the LMP93601 is operating. The SYNC, DRDYB, and RSTB are synchronous to XCLK. The LMP93601 operating range for XCLK is 3.6 to 4.4 MHz.

8.3.12 Operating Modes

The LMP93601 can be programmed to convert data in continuous-time or single shot modes.

8.3.13 Data Ready Function (DRDYB)

DRDYB is an active low output signal. It is asserted when new data is ready to be read and should be used by the MCU for data capturing.

When DRDYB is asserted, the MCU can capture the data any time before the next DRDYB is asserted. The time is defined as 1/ODR. Please note that if data is not read within the time period, it will be over-written internally in the LMP93601 by the new data.

For DRDYB de-assertion, it is normally cleared by a data read. In the following example: it is de-asserted on the 14th SCLK rising edge.

If data has not been read when the new data is about to be ready, DRDYB will be de-asserted for 15 XCLK periods (defined as t_{DRDYB}) so that LMP93601 can re-assert the DRDYB. Once this happens, the μC should wait for the next DRDYB assertion before issuing an SPI read protocol.

DRDYB assertion and de-assertion is synchronous to XCLK and SCLK respectively in normal operation.

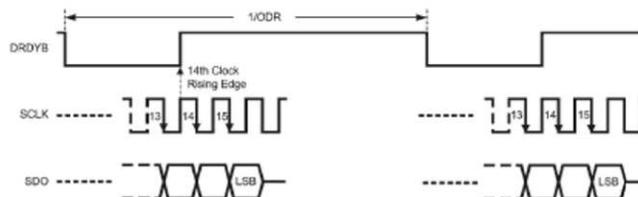
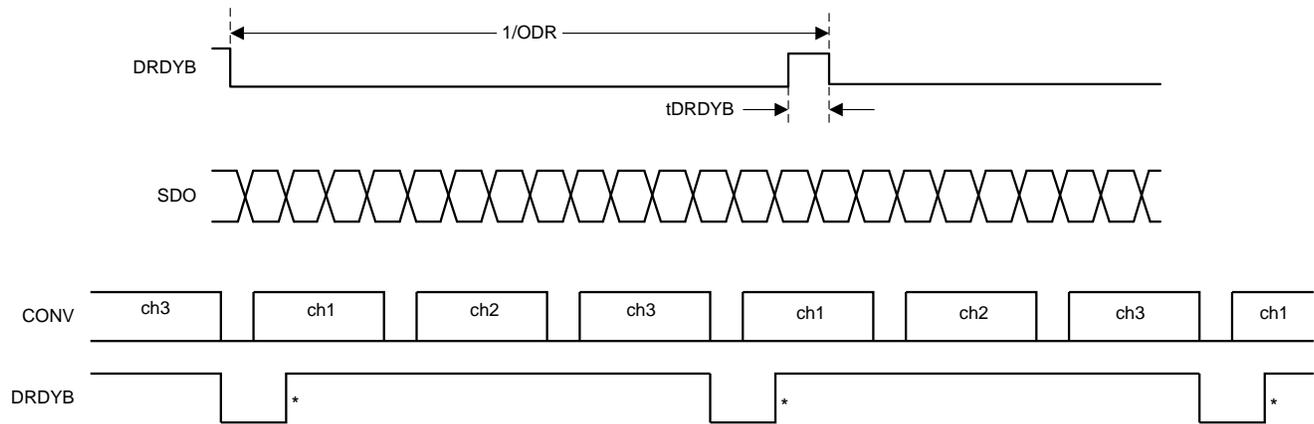
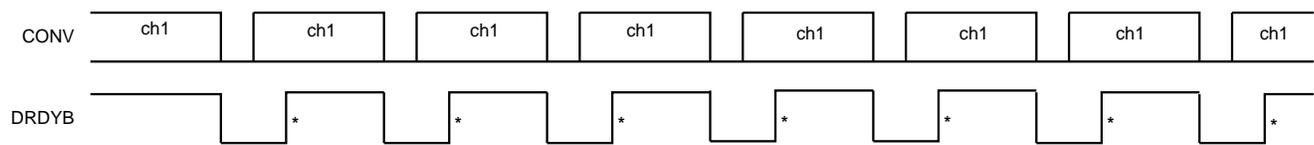


Figure 17. DRDYB Behavior for A Complete Read Operation



The above example is to show how DRDYB functions if more than 1 channel is enabled. DRDYB is only issued every round-robin. DRDYB is de-asserted when the LMP93601 starts to output data.



The above example is to show how DRDYB functions if only 1 channel is enabled. DRDYB is de-asserted when the LMP93601 starts to output data.

Figure 18. DRDYB Behavior for an Incomplete Read Operation

8.3.14 Synchronous Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) interface allows access to the control registers of the LMP93601. The serial interface is a generic 4-wire synchronous interface compatible with SPI type of interfaces used on many microcontrollers and DSP controllers. A typical serial interface access cycle is exactly 16 bits long, which includes an 8-bit command field (R/WB + 7-bit address) to provide a maximum of 128 direct access addresses, and an 8-bit data field.

LMP93601’s SCLK can be in either idle high or idle low state when CSB is de-asserted. The first incoming data on the SCLK rising edge, and all incoming data at SDI is captured on the SCLK rising edge. Outgoing data is sourced at SDO on the SCLK falling edge and the MCU can capture data from the LMP93601 on the SCLK rising edge.

8.3.15 Power Management Mode; Standby, Conversion and Shutdown

The device can be placed in Standby and Conversion mode via the SPI. In Conversion mode, the ADC and PGA are operating and converting data. In Standby mode the PGA and ADC are disabled and not converting data. In Standby mode the contents of the registers are unaffected, and there is a drastic power reduction. Only the internal reference, LDO, VCM driver and the digital are on.

The reaction time going from Standby mode to Conversion mode is approximately 100 μs.

The LMP93601 can be put in shutdown mode by taking the PWDNB pin low. In shutdown mode, all internal circuitry is disabled and no register settings are maintained. The power consumption is very low (< 0.1 uA). Releasing the PWDNB (taking it high) will “wake up” the device and it will return to the default Standby mode. Wake up time from shutdown can be up to 10 ms.

Table 5. Wake Up Time From Low Power Modes

| Mode | Registers | Power | Wake Up Time | Programmable via |
|----------|----------------|---------|---------------------------------------|------------------|
| Shutdown | Not maintained | ~0.1 μA | Less than 10 ms to go to Standby mode | PWDNB pin |

Table 5. Wake Up Time From Low Power Modes (continued)

| Mode | Registers | Power | Wake Up Time | Programmable via |
|------------|------------|--------------|---------------------------------------|------------------|
| Standby | Maintained | ~175 μ A | ~100 μ s to go to conversion mode | SPI |
| Conversion | Maintained | 1.1 mA | n/a | SPI |

8.3.16 Power-On Sequence and Reset (POR) Function

An internal power on reset is generated after both the internal LDO (to supply the internal digital) and IOVDD reach valid values. The internal LDO will reach stable values only after the AVDD has reached at least 2.7 V.

The device should be powered up with AVDD enabled and stabilized first, then the IOVDD. This allows the device to start in the default power up state and ensures that the internal power on reset is generated after both the internal LDO (to supply the internal digital) and IOVDD reach valid values. The internal LDO will reach stable values only after the AVDD has reached at least 2.7 V for 1 ms. Alternatively, AVDD and IOVDD can be connected together, but this can result in an erroneous brown-out condition being reported when the ramp time of the supplies is slower than 0.1 V/ms. For example, if the AVDD = IOVDD are linearly ramped from 0 to 3.3 V in longer than 330 μ s, the brown could possibly trigger and be logged in the status register and the first conversion result could read '7FFF'. To avoid this erroneous brown-out report, three alternative solutions are available:

- After the supplies are stable, reset the part (either with the RSTB pin or with a soft reset via SPI). After this reset, the part can be programmed and used as intended.
- Or, after the supplies are stable, program the part as desired, but before initiating the first conversion, read back the status register(s) of the enabled channel(s) to clear the erroneous brown-out status.
- Or, wait supplying the XCLK to the part until after the supplies are stable

8.3.17 Brown-Out Detection Function

A brown-out detection circuit monitors the AVDD. It triggers an alarm only when AVDD falls below ~2.55 V and stays below 2.55 V for more than 16 fxclock cycles. The brown-out detection has a hysteresis of ~65 mV. The alarm will result in "0x7FFF" data and the appropriate channel status register(s) can be read to decode the alarm. The brown-out error function can be masked via SPI with the "alarm mask" register.

8.3.18 Reset Function

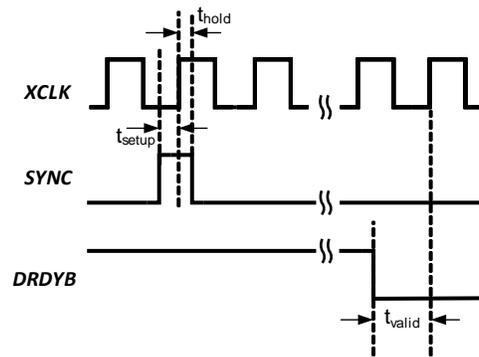
The device can be reset to the default (Standby) state via the SPI or taking the RSTB pin low. The reaction time from the reset (either via SPI or RSTB pin) to the device getting to Standby mode is on the order of 100 μ s. See [Table 6](#)

8.4 Device Functional Modes

8.4.1 Single-Shot Mode

In Single Shot mode each conversion is triggered by a Start Trigger from the microcontroller unit (MCU) to the LMP93601 by pulsing the SYNC pin or via a start SPI command (SYNC is recommended for exact timing control). After the LOCK bit is set, the external μ C should wait 3 XCLK cycles before it sends a start trigger. This is to allow the internal synchronizer enough time to synchronize the SPI write of the LOCK bit into the XCLK domain. This assumes the analog has already settled (otherwise, allow ~100 μ s to go from standby to conversion mode).

The SYNC has typical setup/hold time of 20 ns with respect to XCLK, as shown in [Figure 19](#).

Device Functional Modes (continued)

Figure 19. Single Shot Sync Setup/Hold Time

Device Functional Modes (continued)

See Figure 20 for details regarding the Single Shot Flow Chart.

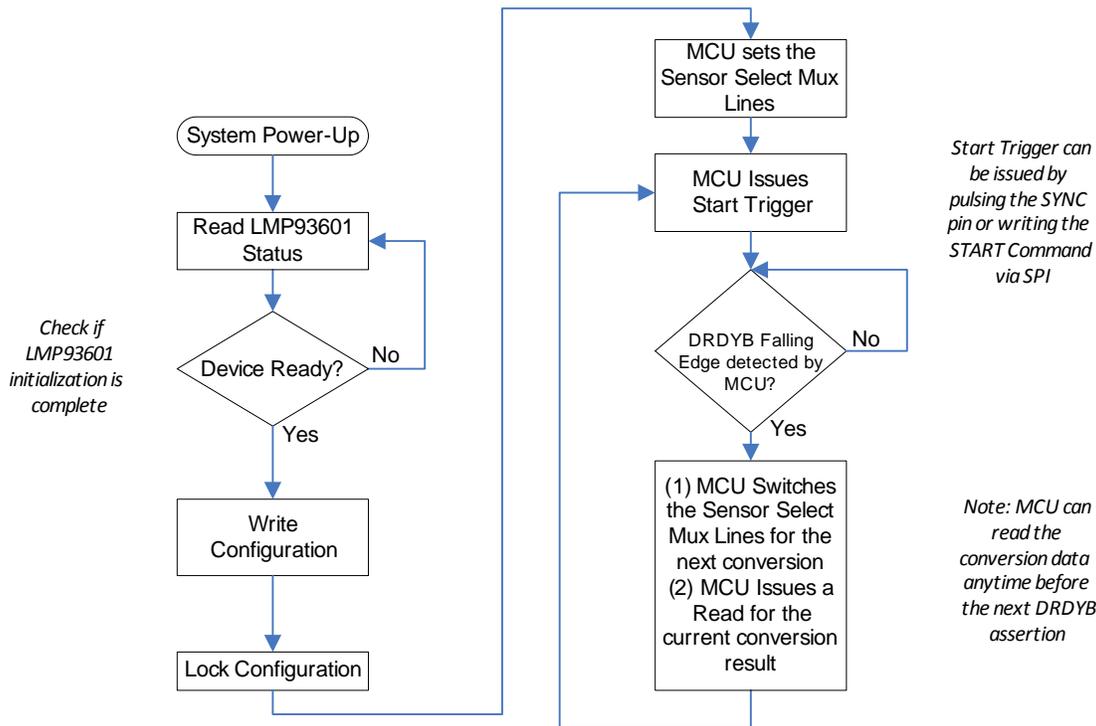


Figure 20. Single Shot Flow Chart

Device Functional Modes (continued)

8.4.2 Continuous Mode

In Continuous mode the LMP93601 only requires a single Start Trigger to start. The Start Trigger can start either by a SYNC or a Start command via the SPI (SYNC is recommended). After the LOCK bit is set, the external MCU should wait 3 XCLK cycles before it sends a start trigger. This allows the internal synchronizer enough time to synchronize the SPI write of the LOCK bit into the XCLK domain. This assumes the analog has already settled (else allow ~100 μ s to go from standby to conversion mode).

It will convert all enabled channels without requiring another Start Trigger. [Figure 21](#) shows the Continuous Mode Flow Chart.

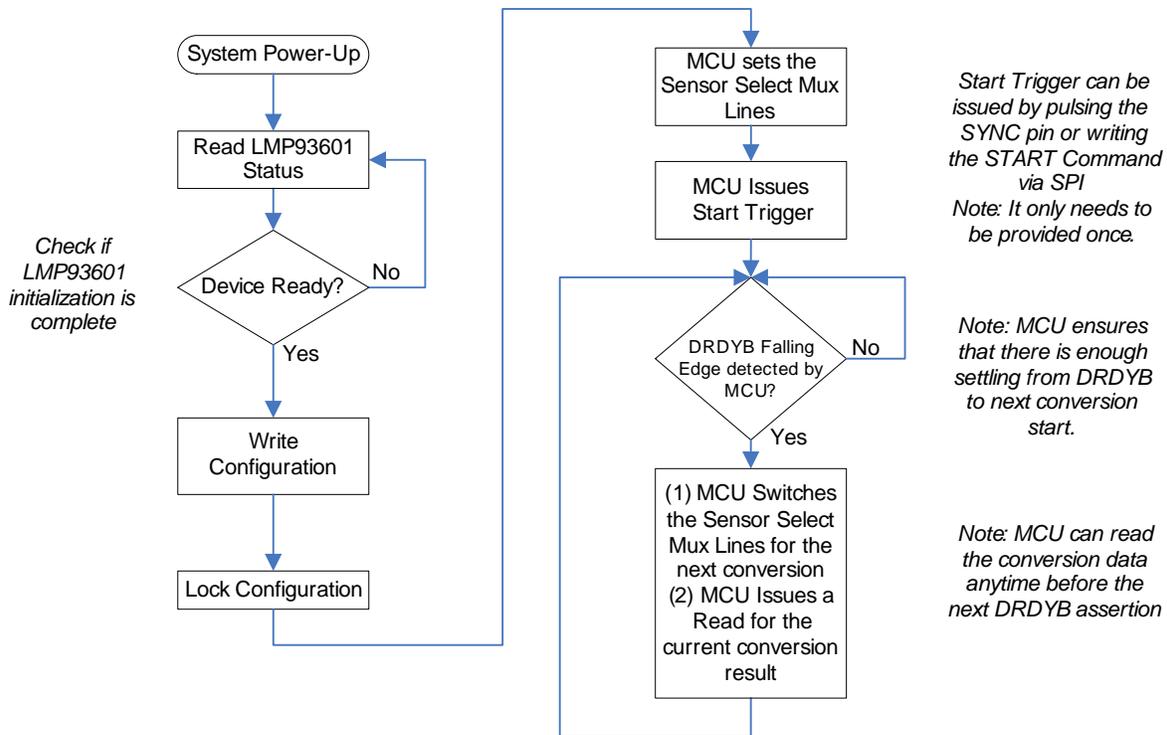


Figure 21. Continuous Mode Flow Chart

8.5 Programming

8.5.1 Window to Capture Data and Status

SPI Protocols can be asynchronous to XCLK. Data and status read can only happen between the consecutive DRDYB falling edges. For example, after DRDYB is asserted by the LMP93601, the MCU has to finish reading all data before DRDYB is asserted again.

For best performance in continuous acquisition mode, it is recommended to read the data within 70 µs after DRDYB is asserted in order to keep the SPI activity during conversion to a minimum.

NOTE

The de-assertion of DRDYB happens after a data read command is received.

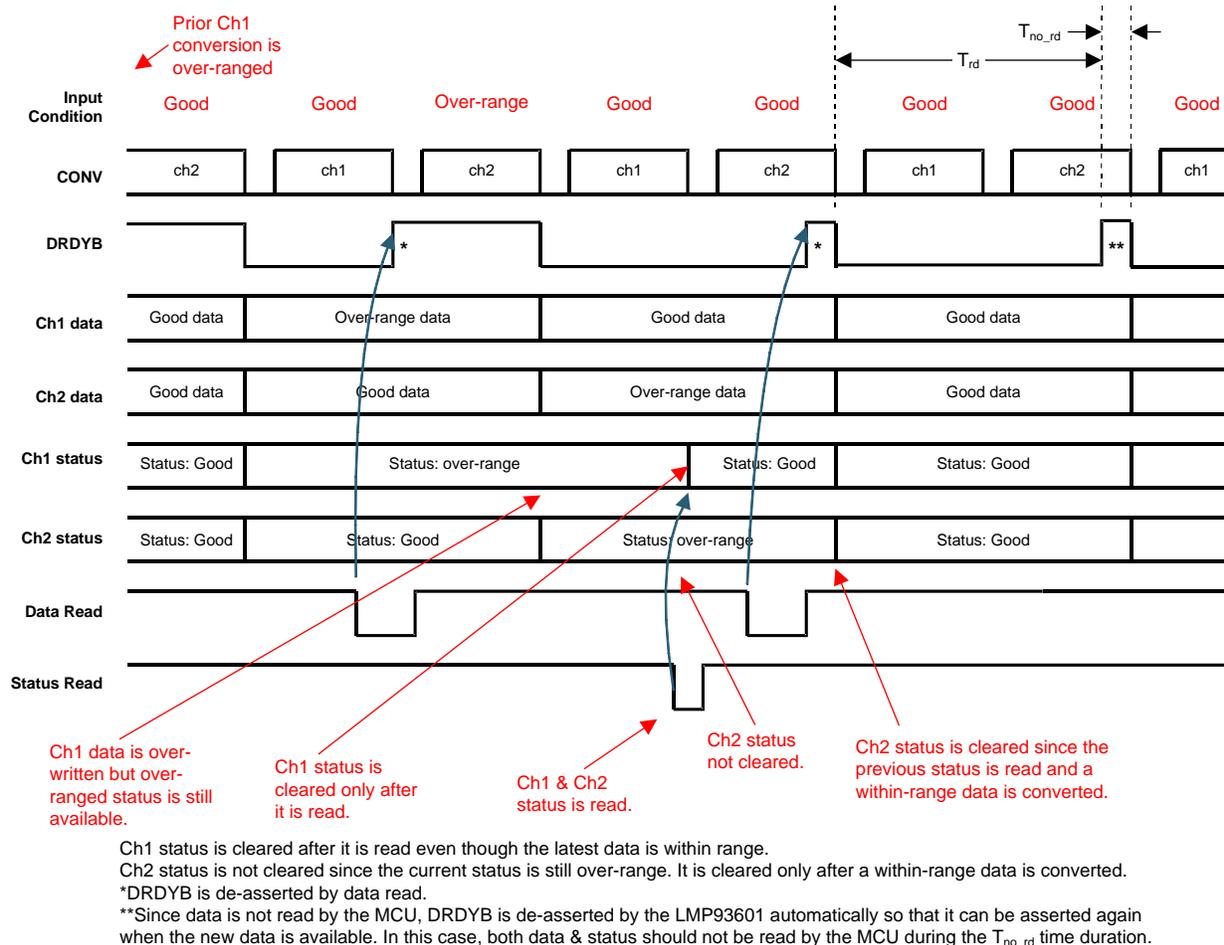


Figure 22. Channel Data Transfer Timing Diagram

Programming (continued)

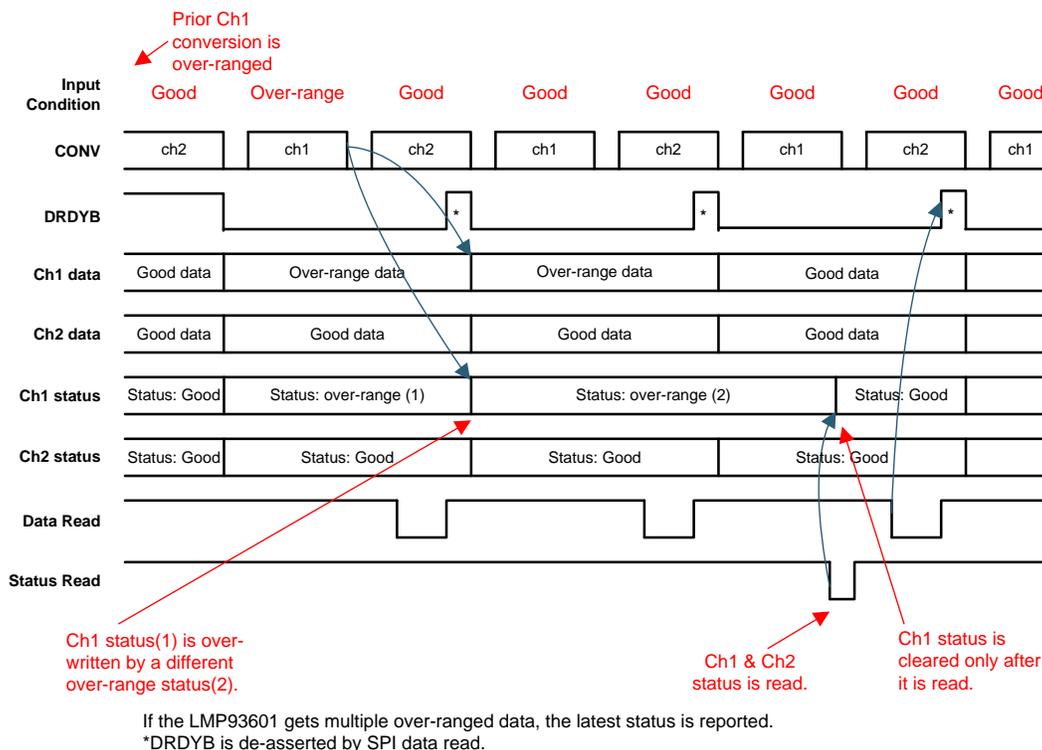


Figure 23. Channel Data Transfer Timing Diagram

8.5.2 Single Byte Access

WRITE: A single byte write access is a total of 16 SCLK periods during CSB assertion. Incoming data is captured on the rising edge of the SCLK. A command byte consists of an R/W bit and a 7-bit address field and R/W = 0 for write protocols.

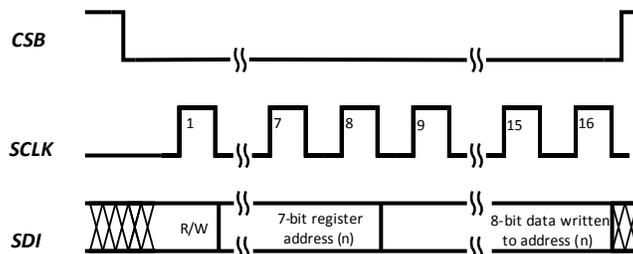


Figure 24. Single Byte Write Access

READ: Similar to a write, the LMP93601 captures incoming data on the SCLK rising edge. After the 8th rising edge, the LMP93601 output data is sourced on the SCLK falling edge and the MCU should capture it on the rising edge. R/W = 1 for read protocols.

Programming (continued)

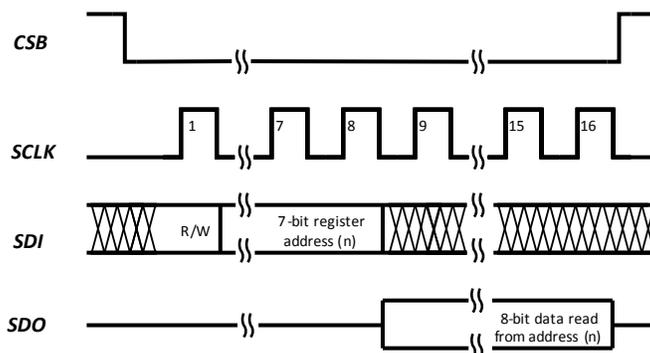


Figure 25. Single Byte Read Access

8.6 Register Maps

Table 6. LMP93601 Internal Registers

| ADDR [6:0] | Name | # of Bits | Type | Default | Description | Locked when conversion is enabled? |
|------------|---------|-----------|--------------------|---------|---|------------------------------------|
| 0x00 | Lock | 1 | R/W ⁽¹⁾ | 'h00 | [0] 0: configuration bits are writeable (default) 1: configuration bits are read-only (that is, locked) unless noted. [7:1] always 0 | n/a ⁽²⁾ |
| 0x01 | Config1 | 4 | R/W ⁽¹⁾ | 'h00 | [7] continuous/single shot: 0: Continuous – the part will convert all enabled channels sequentially in a round-robin manner. After all channels are converted, it will repeat the round-robin. (default) 1: Single-Shot - the part will convert all enabled channels once in a round-robin manner after receiving a start-trigger (SYNC pulse preferred). It will wait for the next trigger before converting all enabled channels again. [2:0] Channel enable Channel enable configuration for the 3 channels (Ch1-3): 3'b000: Only Ch1 is enabled(default) 3'b001: Only Ch2 is enabled 3'b010: Only Ch3 is enabled 3'b011: Only Ch1 & Ch2 enabled 3'b100: Ch1, 2, & 3 enabled 3'b101, 3'b110, 3'b111: Reserved [6:3]: always 0 | Y |

(1) R/W = Read or Write

(2) n/a = not applicable

Register Maps (continued)
Table 6. LMP93601 Internal Registers (continued)

| ADDR [6:0] | Name | # of Bits | Type | Default | Description | Locked when conversion is enabled? |
|------------|---------|-----------|--------------------|---------|--|------------------------------------|
| 0x02 | Config2 | 3 | R/W ⁽¹⁾ | 'h82 | [7] Reference Output Enables for VCM 0: Disable the corresponding VCM output 1: Enable the corresponding VCM output (default) VCM = AVDD/3 [1:0] SPS select Global setting for all enabled channels 2'b00: 265 sps 2'b01: 530 sps 2'b10: 1057 sps(default) 2'b11: 1326 sps [6:2] always 0 | Y |
| 0x03 | Config3 | 5 | R/W ⁽¹⁾ | 'h52 | PGA settings for differential channels. All channels will always have the same setting. [6:4] Digital 3'b000: 1 3'b001: 2 3'b010: 4 3'b011: 8 3'b100: 16 3'b101: 32(default) 3'b110-111: Reserved [1:0] Analog 2'b00: 16 2'b01: 32 2'b10: 64 (default) 2'b11: 128 [7], [3:2] always 0 [2] , Bypass PGA, bit [1:0] would be ignored. See for more details | Y |
| 0x04 | Config4 | 1 | R/W ⁽¹⁾ | 'h00 | [0] Power Mode 0: Standby (default) 1: Conversion Mode (user still has to write the lock bit and then provide a start-trigger before conversion starts) [7:1] always 0 | Y |

Register Maps (continued)
Table 6. LMP93601 Internal Registers (continued)

| ADDR [6:0] | Name | # of Bits | Type | Default | Description | Locked when conversion is enabled? |
|------------|------------|-----------|--------------------|--------------------|---|------------------------------------|
| 0x05 | Alarm mask | 3 | R/W ⁽¹⁾ | 'h00 | <p>[7] Brownout Mask</p> <p>0: when brown-out is detected, all enabled channels' conversion result will be 0x7FFF (default)</p> <p>1: when brown-out is detected, the conversion result is not affected.</p> <p>[6]: Digital Gain Over range Mask</p> <p>0: when digital gain over-range is detected for a channel, its conversion result will be 0x7FFF (default)</p> <p>1: when digital gain over-range is detected, conversion result is not affected.</p> <p>[0] PGA over-range Mask</p> <p>0: when any of the PGA over-range is detected for a channel, its conversion result will be 0x7FFF (default)</p> <p>1: when any of the PGA over-range is detected, conversion result is not affected</p> <p>[5:1] always 0</p> | Y |
| 0x06 | sdo_cfg | 1 | R/W ⁽¹⁾ | 'h00 | <p>[0] SDO always driven mode</p> <p>0: SDO only driven during the read back frames of a SPI read, all other time, SDO is in Hi-Z (Default)</p> <p>1: SDO always driven mode: SDO driven high by LMP93601 except during the read back frame of a SPI read</p> <p>[7:1] always 0</p> | N |
| 0x07 | Soft reset | 1 | R/W ⁽¹⁾ | 'h00 | <p>[0]: Soft reset</p> <p>0: normal (Default)</p> <p>1: Reset all registers hence part will be in default condition</p> <p>To reset via SPI, one should write first a 1 to this bit and then a 0.</p> <p>[7:1] always 0</p> | N |
| 0x0f | START | 1 | WO ⁽³⁾ | n/a ⁽²⁾ | <p>[7] Start</p> <p>This is a write-only location. If written, it will act as the trigger to start the conversion sequence.</p> <p>In continuous mode, the round robin is triggered by a write to this register. The round robin will be repeated so only 1 write is needed.</p> <p>In Single-Shot mode, the round robin is triggered by a write to this register and all enabled channels will be converted once. The chip will wait for the next write to the START register before starting the next round robin conversion.</p> <p>NOTE: For accurate timing control, SYNC pulse as a start-trigger is preferred since it is synchronous to the XCLK domain.</p> <p>[6:0] always 0</p> | Only writeable if LOCK is 1 |

(3) WO = Write Only

Register Maps (continued)
Table 6. LMP93601 Internal Registers (continued)

| ADDR [6:0] | Name | # of Bits | Type | Default | Description | Locked when conversion is enabled? |
|--|----------------|-----------|-------------------|--------------------|---|------------------------------------|
| NOTE The following status register addresses are mapped in ascending order for easy read-back. | | | | | | |
| 0x10 | general Status | 1 | RO ⁽⁴⁾ | 'h00 | [0]: when this bit is high, the LMP93601 is ready to be programmed. | n/a ⁽²⁾ |
| 0x11 | Status1 | 8 | RO ⁽⁴⁾ | n/a ⁽²⁾ | [7:0]: Status for CH1: [0] - Digital gain overrange [1] - PGA positive output low [2] - PGA negative output low [3] - PGA positive output high [4] - PGA negative output high [5] - PGA differential output high [6] - Sign of PGA out. This alone does not trigger 7FFF error code. [7] Brown out | n/a ⁽²⁾ |
| 0x12 | Status2 | 8 | RO ⁽⁴⁾ | n/a ⁽²⁾ | [7:0] Status for CH2: same bit map as CH1 status (above) | n/a ⁽²⁾ |
| 0x13 | Status3 | 8 | RO ⁽⁴⁾ | n/a ⁽²⁾ | [7:0] Status for CH3: same bit map as CH1 status (above) | n/a ⁽²⁾ |
| Channel Results: When over-range is detected, the corresponding channel result will read back 0x7FFF, unless it is masked. When brown-out is detected, the converted channel result will read back 0x7FFF, unless it is masked. | | | | | | |
| NOTE The following channel result register addresses are mapped in ascending order for easy read-back. | | | | | | |
| 0x20 | CH1 LSB | 8 | RO ⁽⁴⁾ | n/a ⁽²⁾ | CH1 Result[7:0] | n/a ⁽²⁾ |
| 0x21 | CH1 MSB | 8 | RO ⁽⁴⁾ | n/a ⁽²⁾ | CH1 Result[15:8] | n/a ⁽²⁾ |
| 0x22 | CH2 LSB | 8 | RO ⁽⁴⁾ | n/a ⁽²⁾ | CH2 Result[7:0] | n/a ⁽²⁾ |
| 0x23 | CH2 MSB | 8 | RO ⁽⁴⁾ | n/a ⁽²⁾ | CH2 Result[15:8] | n/a ⁽²⁾ |
| 0x24 | CH3 LSB | 8 | RO ⁽⁴⁾ | n/a ⁽²⁾ | CH3 Result[7:0] | n/a ⁽²⁾ |
| 0x25 | CH3 MSB | 8 | RO ⁽⁴⁾ | n/a ⁽²⁾ | CH3 Result[15:8] | n/a ⁽²⁾ |
| 0x7E | Chip ID | 8 | RO ⁽⁴⁾ | 8'h73 | LMP93601 chip ID | n/a ⁽²⁾ |
| 0x7F | Revision ID | 8 | RO ⁽⁴⁾ | 8'h00 | LMP93601 Revision ID | n/a ⁽²⁾ |

(4) RO = Read Only

8.7 Multi Byte Access (Auto Increment) Mode

This interface will support address auto-increment feature. An access cycle may be extended to multiple registers simply by keeping the CSB asserted beyond the stated 16 clocks of the standard 16-bit protocol. In this mode, CSB must be asserted during $8*(1+N)$ clock cycles of SCLK, where N is the number of bytes to write or read during the access cycle. The auto-incrementing address mode is useful to access a block of registers of incrementing addresses.

WRITE: Example: if 2 bytes of data are sent by the MCU to the LMP93601, both addresses (n) and (n+1) will be written at the 16th and 24th rising edges of SCLK respectively. Similarly, if another 8 bits of data is sent, they will be written in the next address location.

Multi Byte Access (Auto Increment) Mode (continued)

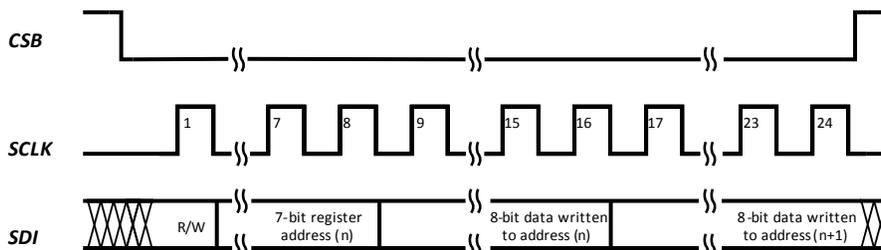


Figure 26. Example Multi Byte Write Access

READ: Example: if a read address is sent from the MCU to the LMP93601, the LMP93601 will first output the data at location (n). If another 8 SCLKs are sent, the data at location (n+1) will be output. Similarly, the LMP93601 will continue to send the data at the next address location until CSB is de-asserted.

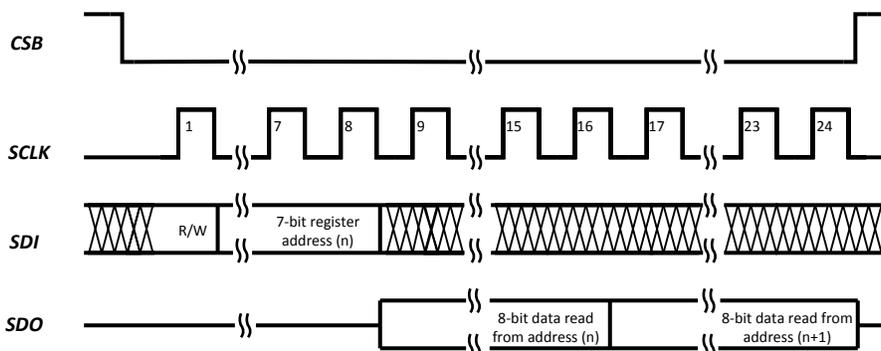


Figure 27. Example Multi Byte Read Access

NOTE

If a read (or write) is not $8 \cdot (1+N)$ clock cycles, the last byte will not be read or written. For example if 20 clocks were used, only the 1st data byte is being written, not the 2nd one.

8.8 Multi-Channel Data Read

CH1, CH2 and CH3 results can be read by a single SPI transaction in Little Endian Format:

- Byte Level: Ch1[7:0], Ch1[15:8], Ch2[7:0], Ch2[15:8], Ch3[7:0], Ch3[15:8].....
- Bit Level: Ch1[7], [6], [5], [4], [3], [2], [1], [0], [15], [14], [13], [12], [11], [10], [9], [8], Ch2[7].....

The overhead is a single byte of command which consists of a READ bit and a 7-bit address field.

NOTE

ADC rate is 1326 SPS (max). If all 3 channels are enabled, the conversion rate for each channel is $1326 \text{ SPS} / 3 = 426 \text{ SPS}$.

Multi-Channel Data Read (continued)

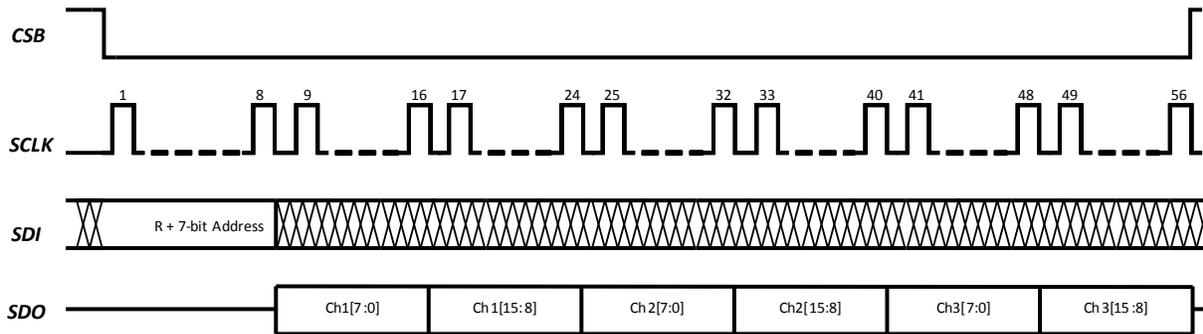


Figure 28. Example Multi Channel Read Access

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Micro-electro-mechanical systems (MEMS) thermopile sensor arrays are gaining popularity in building automation applications for efficient control of heating, ventilation, and air conditioning (HVAC) system in residential and commercial buildings. The sensors are installed in the building rooms for detecting the presence and the motion of the occupants in the rooms. Depending on the presence or absence of people in the room, the HVAC system is turned on or off respectively. In addition, the thermopile sensor are used for detecting flow of air in the in the duct-work system in the buildings.

A typical MEMS thermopile array sensor consists of a number of thermopile elements arranged in a matrix configuration. Each element of the array is accessed by selecting the corresponding XY address in the array using internal or external decoder circuits. An output frame consists of differential signals form X by Y elements. Each frame is transferred to the analog-front-end via OUTP (positive output) and OUTN (negative output) output pins of the sensor in serial format. The analog output signal of the MEMS thermopile sensor is in the micro volt range. It needs to be amplified significantly before made available to the input of an ADC for digitization.

9.2 Typical Applications

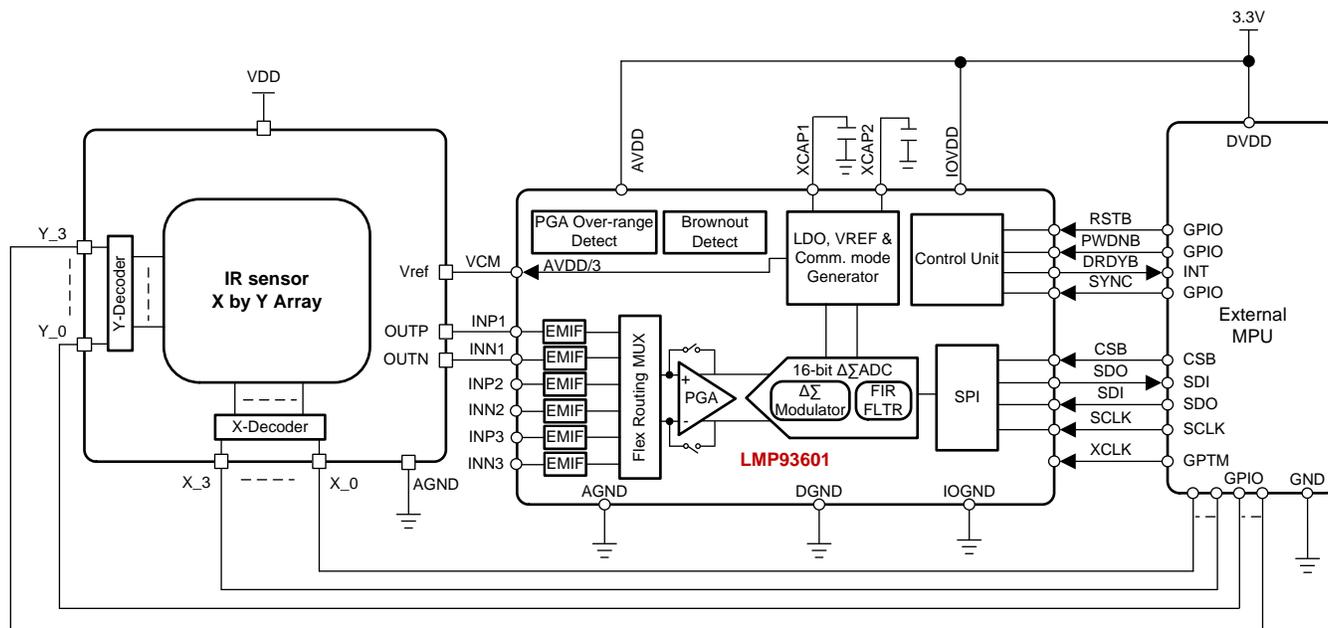


Figure 29. LMP93601 Thermopile Array Interface

9.2.1 Design Requirements

The application requires a microcontroller (MCU) such as Texas Instruments MSP430x, or TM4C129x series of MCUs connected via Synchronous Serial Interface (SPI) to the LMP93601 AFE. As shown in Figure 29, the X and Y decoder lines of the thermopile sensor (transducer) needs to be interfaced to the GPIO (General Purpose Input Output) pins of the MCU. The LMP93601 would require an external clock signal of 4 MHz (±3%).The timer subsystem of the MCU is well suited to generate the clock signal. A timer output pin shall be used to interface the output of the MCU timer to the XCLK pin of the LMP93601.

Typical Applications (continued)

The device provides a reference voltage output (VCM) source to center the output of the sensor around $AVDD/3$. If the sensor does not provide a reference input pin, the INPx, INNx inputs of the LMP93601 should be connected (pulled-up) to VCM output via 2.2 M Ω resistors.

The data converter of the LMP93601 is an incremental delta-sigma type ADC, the modulator is reset after every conversion. Therefore, after each thermopile element is sampled and the ADC modulator goes through a reset, there is no possibility of any trace of signal from the previously sampled element.

To sample each thermopile element in the sensor array, the X and Y decoder signals must be provided over the GPIO, then firmware should allow settling of the data on the decoder. The SYNC pin is provided to signal the beginning of conversion to LMP93601 ADC. A GPIO of the MCU needs to be interfaced to the SYNC input pin of the LMP93601 for this purpose.

9.2.2 Detailed Design Procedure

In thermopile array systems, settling time of the signal path plays an important role when higher frame transfer rates are desired. A frame is an array of X by Y thermopile elements. While the data from each pixel is being transferred out of the sensor in a sequence, the MUX output must settle to the proper voltage from the element in the array that is being accessed. The total analog signal path settling time is determined by combined sensor's settling time (t_{ssnsr}) and AFE's settling time (t_{safe}). The settling time is determined by the sum of capacitances of the following: pixel in the array, sensor's MUX, AFE's MUX, PCB, AFE's input stage, and sensor's resistance.

To achieve faster settling time, total capacitance in the signal path should be kept as low as possible. Therefore, the system designers should take the resistance of the sensor and the related capacitance into consideration to achieve optimal performance of the signal path. For example, the pixel-to-pixel settling time should be kept below 70 μ s to process five frame per second (1326 SPS) using a 16 x 16 array sensor. A simplified thermopile array sensor equivalent circuit is shown in Figure 30.

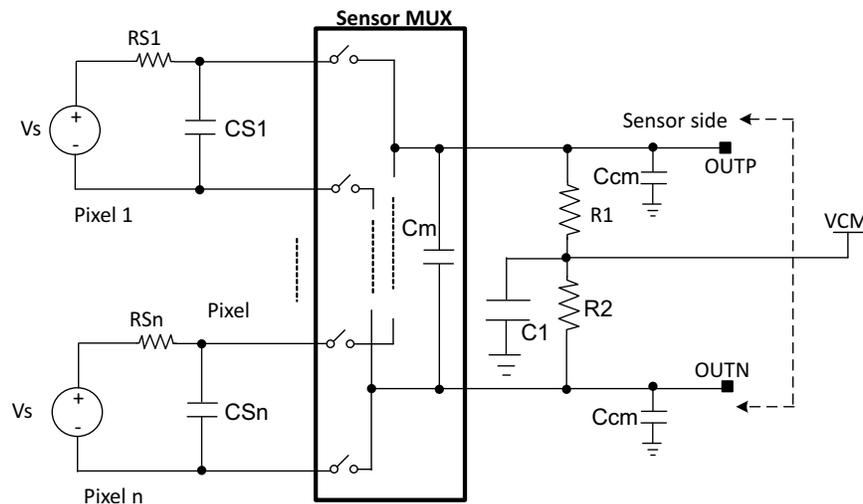


Figure 30. Simplified Thermopile Sensor Array

The value of biasing resistors; R1 and R2, should be much higher than the value of the sensor output resistance RSx (that is, $R1 = R2 > 10 * RSx$).

Typical Applications (continued)

The bias current of the sensor and the leakage current of the sensor's MUX should be considered as well. In Figure 31 R1 and R2 need to be matched closely to avoid introduction of differential offset error voltage in the signal path due to mismatched current flow through these resistors. Moreover, I_{OS} through R_{Sx} needs to be calibrated out over temperature. To simplify the circuit in Figure 31 the MUX inside the AFE is not shown.

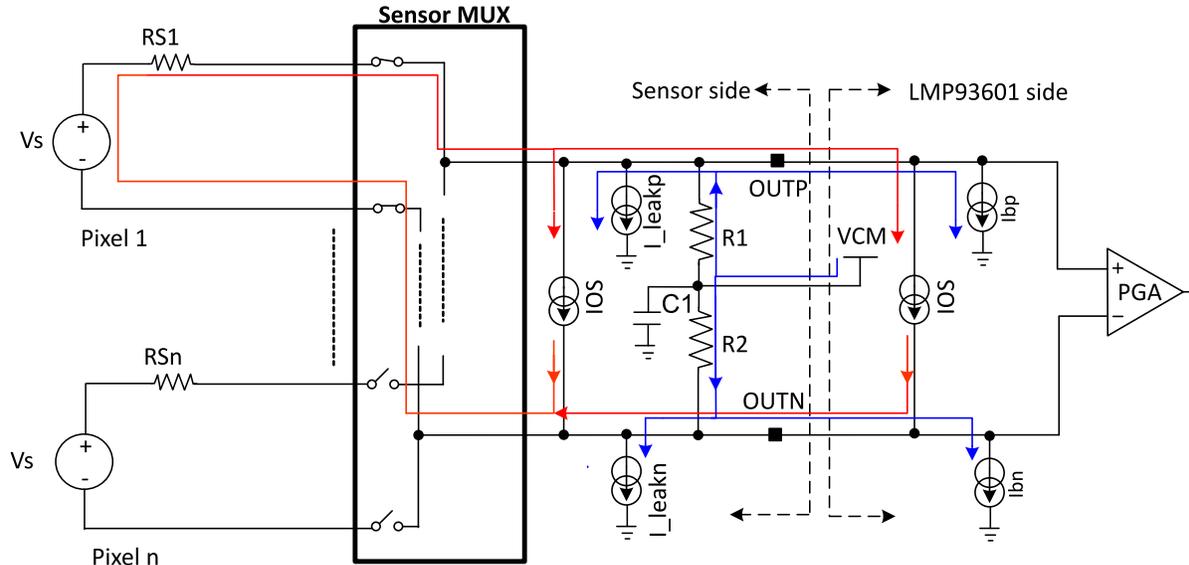


Figure 31.

10 Power Supply Recommendations

The LMP93601 requires two sources of power, AVDD and IOVDD. These pins can be supplied from the same supply rail as the MCU, from separate regulators or from a battery source. However, it is recommended that the MCU and the IOVDD share the same supply and the AVDD be supplied from a separate regulator. In any case, for proper operation, the supply range must remain within the 2.7 V to 5.5 V limits and IOVDD must always be lower than or equal to AVDD supply. It is highly recommended that during power up, the AVDD and IOVDD supplies ramp up in a manner to ensure the "IOVDD \leq AVDD" requirement is not violated.

11 Layout

11.1 Layout Guidelines

To achieve high noise performance of the LMP93601, particular attention must be paid to the layout of the input signals, inputs INPx and INNx. To avoid introduction of differential noise into the pins, the input traces must lay out symmetrically.

Proper power-supply decoupling is required on both AVDD and IOVDD. The Supply pins should be decoupled with at least a 0.1 μ F bypass capacitor each. The bypass capacitors should be placed as close to the power-supply pins as possible with a low impedance connection. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the bypass capacitor may offer superior bypass and noise immunity.

It is recommended that in the layout, analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] be separated from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. The best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

TI recommends placing 47 Ω resistors in series with all digital input and output pins (CS, SCLK, DIN, DOUT/DRDY, and DRDY). This resistance smooths sharp transitions, suppresses overshoot, and offers some overvoltage protection. Care must be taken to still meet all SPI timing requirements because the additional resistors interact with the bus capacitances present on the digital signal lines.

TI also strongly recommends that digital components, especially RF portions, be kept as far as practically possible from analog circuitry in a given system. Additionally, one should minimize the distance that digital control traces run through analog areas and avoid placing these traces near sensitive analog components. Digital return currents usually flow through a ground path that is as close as possible to the digital path. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature-sensing functions are much more significant than for ADC functions.

The internal ADC reference supply of the LMP93601 requires a 1 μ F high performance (low ESR & ESL) cap on the XCAP1. This cap must be placed in the immediate proximity of the pin. For best performance it is recommended that the DAP be connected to AGND. All three "GND" connections (AGND, DGND, and IOGND) must be connected to system ground and cannot be left floating.

11.2 Layout Example

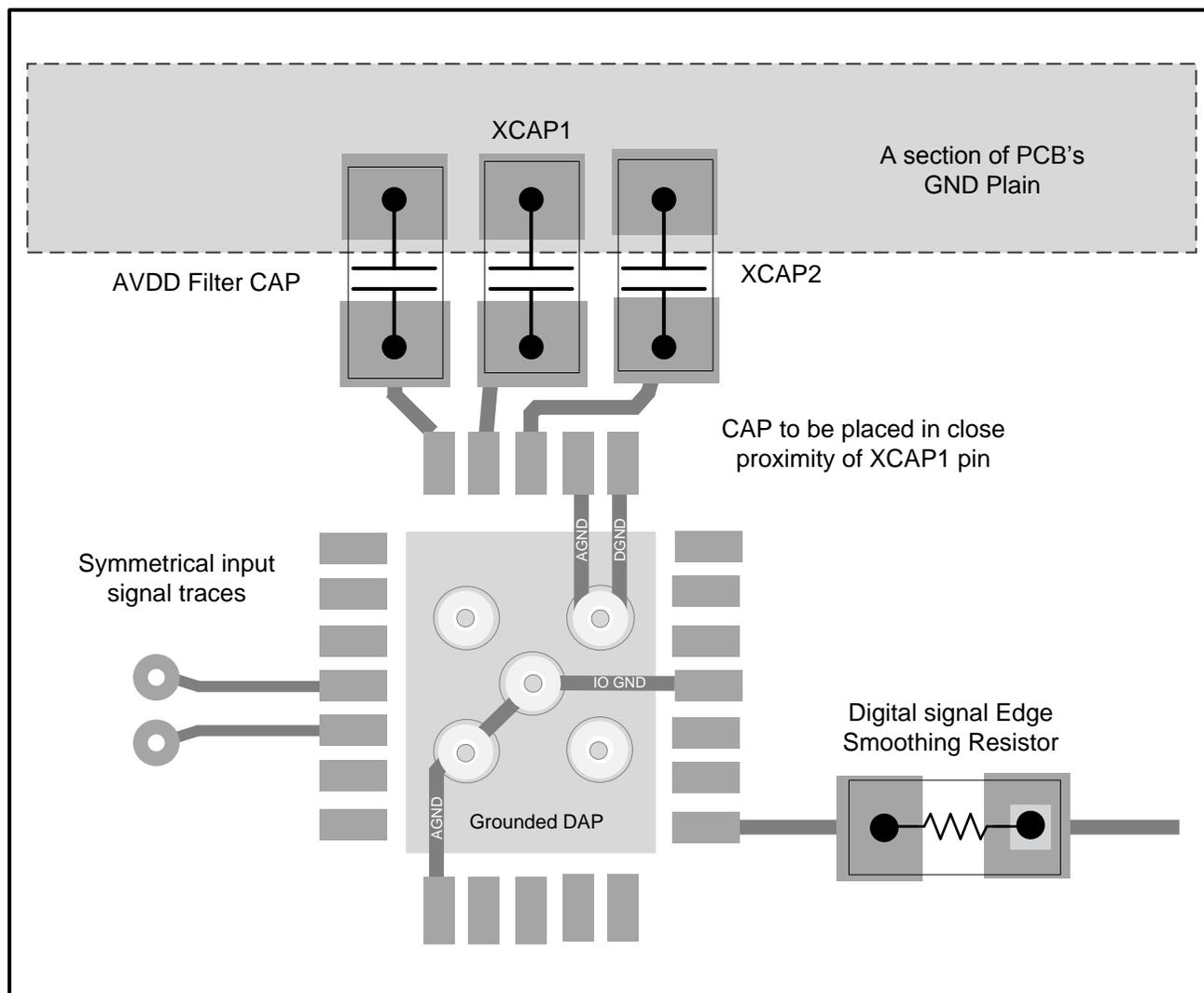


Figure 32. LMP93601 Layout Example

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designed devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| LMP93601NHZR | Active | Production | WQFN (NHZ) 24 | 4500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -25 to 85 | L93601 |
| LMP93601NHZR.A | Active | Production | WQFN (NHZ) 24 | 4500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -25 to 85 | L93601 |
| LMP93601NHZT | Obsolete | Production | WQFN (NHZ) 24 | - | - | Call TI | Call TI | -25 to 85 | L93601 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

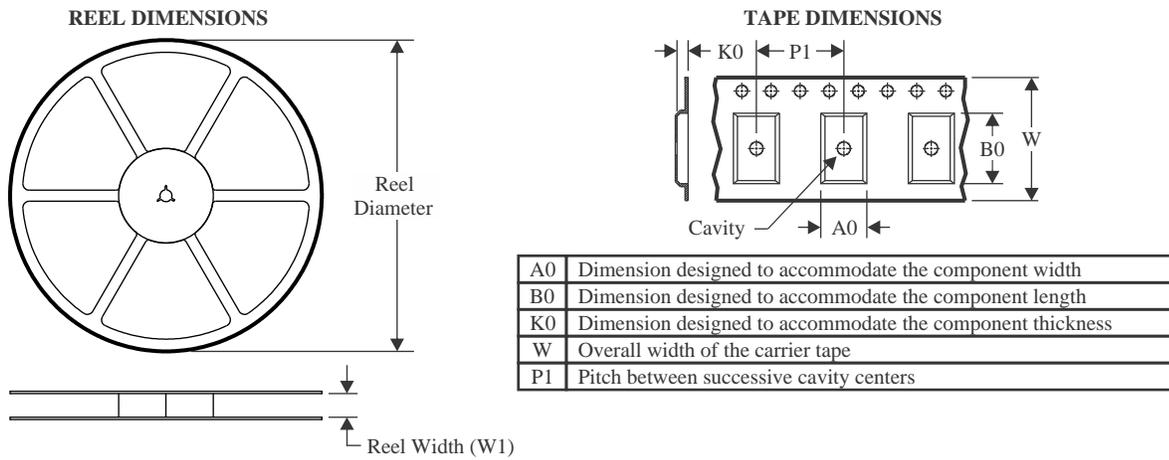
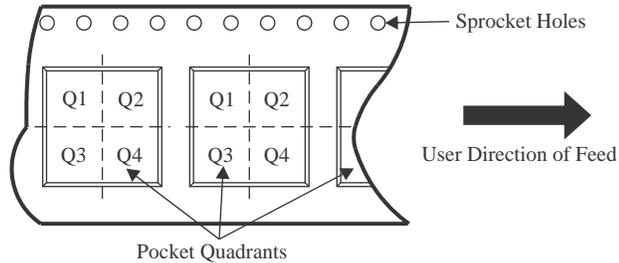
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMP93601NHZR | WQFN | NHZ | 24 | 4500 | 330.0 | 12.4 | 4.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |

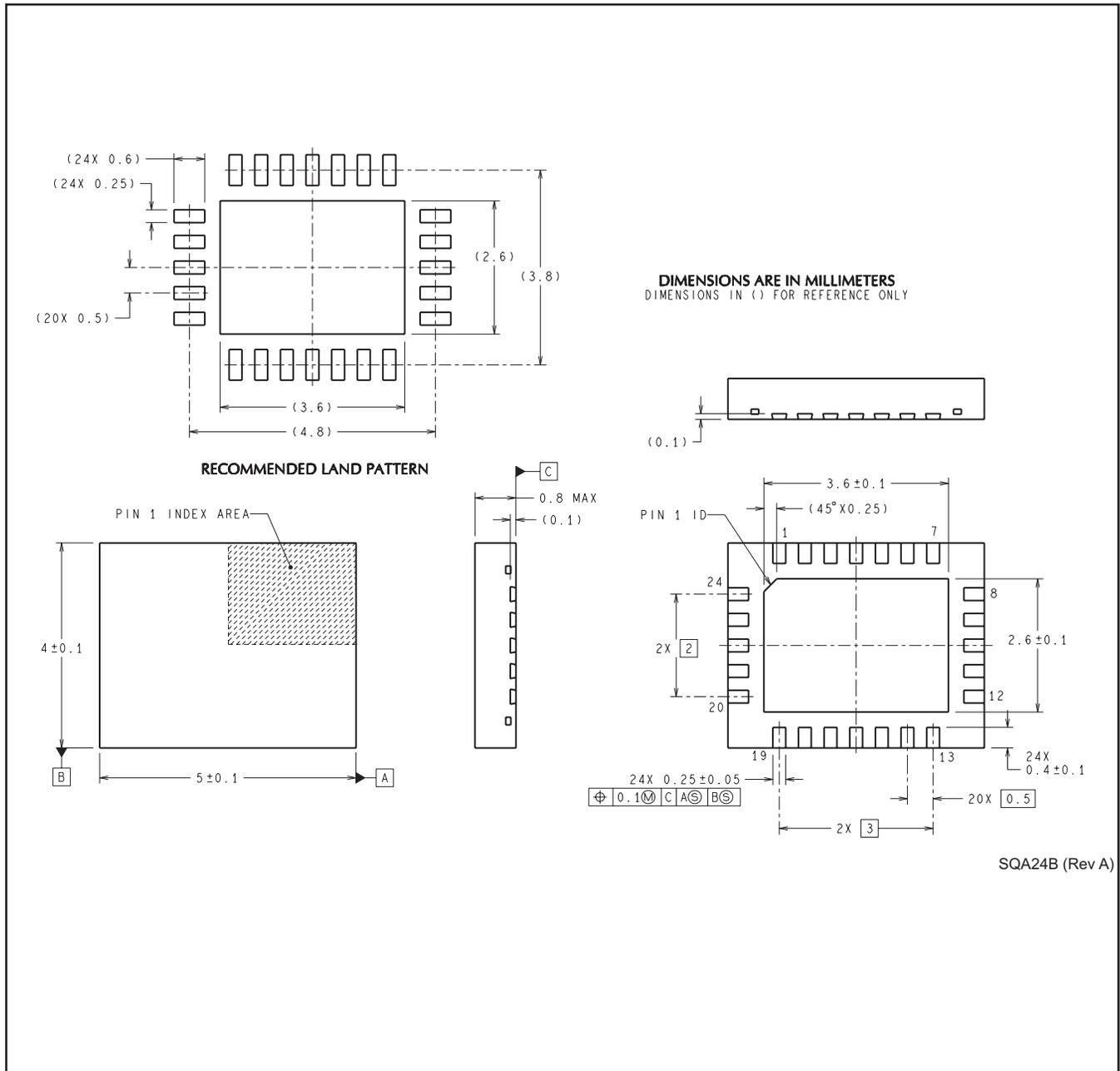
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMP93601NHZR | WQFN | NHZ | 24 | 4500 | 367.0 | 367.0 | 35.0 |

NHZ0024B



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