LMV3xx-N/-Q1 Single, Dual, and Quad General Purpose, Low-Voltage, Rail-to-Rail Output Operational Amplifiers

1 Features

- For $V^+ = 5$ V and $V^- = 0$ V, unless otherwise specified
- LMV321-N, LMV358-N, and LMV324-N are available in automotive AEC-Q100 grade 1 and grade 3 versions
- Ensured 2.7-V and 5-V performance
- No crossover distortion
- Industrial temperature range −40°C to +125°C
- Gain-bandwidth product 1 MHz
- Low supply current
- LMV321-N 130 µA
- LMV358-N 210 µA
- LMV324-N 410 µA
- Rail-to-rail output swing at 10 kΩ $V^+ - 10$ mV and $V^- + 65$ mV
- V_{CM} range −0.2 V to $V^+ - 0.8$ V

2 Applications

- Active filters
- General purpose low voltage applications
- General purpose portable devices

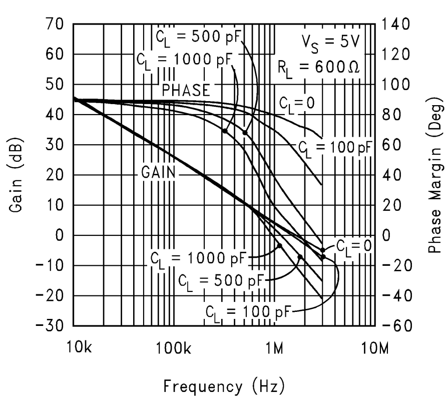
3 Description

The LMV358-N and LMV324-N are low-voltage (2.7 V to 5.5 V) versions of the dual and quad commodity op amps LM358 and LM324 (5 V to 30 V). The LMV321-N is the single channel version. The LMV321-N, LMV358-N, and LMV324-N are the most cost-effective solutions for applications where low-voltage operation, space efficiency, and low price are important. They offer specifications that meet or exceed the familiar LM358 and LM324. The LMV321-N, LMV358-N, and LMV324-N have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed to power ratio, achieving 1 MHz of bandwidth and 1-V/µs slew rate with low supply current.

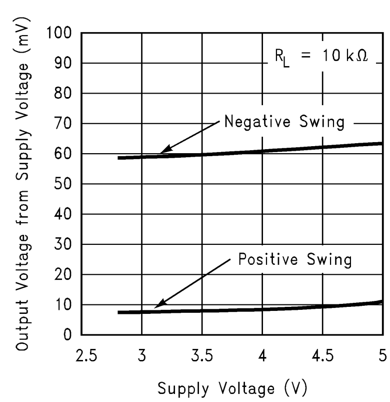
Device Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
LMV321-N	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
LMV321-N-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
LMV324-N	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm
LMV324-N-Q1	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm
LMV358-N	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
LMV358-N-Q1	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Gain and Phase vs Capacitive Load



Output Voltage Swing vs Supply Voltage

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (October 2014) to Revision K (August 2020) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document.......... 1
- Added application links to *Applications* section.......... 1
- Added Thermal Information table for commercial LMV3xx-N and information is updated.......... 6
- Added Thermal Information table for automotive LMV3xx-N-Q1.......... 6
- Changed Io, output short circuit current for LMV3xx-N in 5V DC Electrical Characteristics section.......... 7
- Added open-loop output impedance vs frequency figure for LMV3xx-N in *Typical Characteristics* section.......... 9
- Added output voltage vs output current figure for LMV3xx-N in *Typical Characteristics* section.......... 9

Changes from Revision I (February 2013) to Revision J (October 2014) — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.......... 1

Changes from Revision H (February 2013) to Revision I (February 2013) — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format.......... 33

5 Description (Continued)

The LMV321-N is available in the space saving 5-Pin SC70, which is approximately half the size of the 5-Pin SOT23. The small package saves space on PC boards and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

The chips are built with Texas Instruments's advanced submicron silicon-gate BiCMOS process. The LMV321-N/LMV358-N/LMV324-N have bipolar input and output stages for improved noise performance and higher output current drive.

6 Pin Configuration and Functions

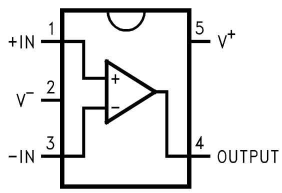


Figure 6-1. DBV and DCK Package
5-Pin SC70, SOT-23
Top View

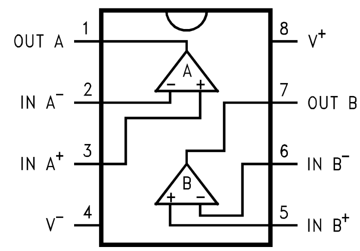


Figure 6-2. D and DGK Package
8-Pin SOIC, VSSOP
Top View

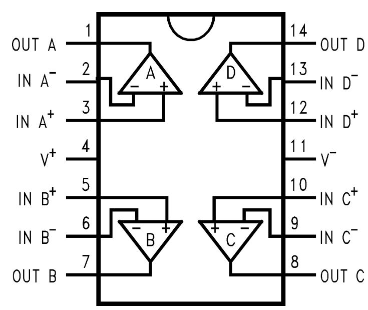


Figure 6-3. D and PW Package
14-Pin SOIC, TSSOP
Top View

Pin Functions

PIN				TYPE[(1)]	DESCRIPTION
NAME	LMV321-N, LMV321-N-Q1, LMV321-N-Q3 DVB, DCK	LMV358-N, LMV358-N-Q1, LMV358-N-Q3 D, DGK	LMV324-N, LMV324-N-Q1, LMV324-N-Q3 D, PW		
+IN	1	—	—	I	Noninverting input
IN A+	—	3	3	I	Noninverting input, channel A
IN B+	—	5	5	I	Noninverting input, channel B
IN C+	—	—	10	I	Noninverting input, channel C
IN D+	—	—	12	I	Noninverting input, channel D
–IN	3	—	—	I	Inverting input
IN A–	—	2	2	I	Inverting input, channel A
IN B–	—	6	6	I	Inverting input, channel B
IN C–	—	—	9	I	Inverting input, channel C
IN D–	—	—	13	I	Inverting input, channel D
OUTPUT	4	—	—	O	Output
OUT A	—	1	1	O	Output, channel A
OUT B	—	7	7	O	Output, channel B
OUT C	—	—	8	O	Output, channel C
OUT D	—	—	14	O	Output, channel D
V+	5	8	4	P	Positive (highest) power supply
V–	2	4	11	P	Negative (lowest) power supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power.

7 Specifications

7.1 Absolute Maximum Ratings

See [1] [9].

	MIN	MAX	UNIT
Differential Input Voltage	±Supply Voltage		V
Input Voltage	−0.3	+Supply Voltage	V
Supply Voltage (V^+–V^-)		5.5	V
Output Short Circuit to V^+	[2]		
Output Short Circuit to V^-	[3]		
Soldering Information: Infrared or Convection (30 sec)		260	°C
Junction Temperature[4]		150	°C
Storage temperature T_{stg}	−65	150	°C

7.2 ESD Ratings - Commercial

			VALUE	UNIT
LMV358-N, and LMV324-N in all packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Machine model	±100	
LMV321-N in all packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±900	V
		Machine model	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - Automotive

			VALUE	UNIT
LMV358-N-Q1, LMV324-N-Q1, LMV358-N-Q3 and LMV324-N-Q3 in all packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Machine model	±100	
LM321-N-Q1 and LM321-N-Q3 in all packages				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±900	V
		Machine model	±100	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.4 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage	2.7	5.5	V
Temperature Range [4]: LMV321-N, LMV358-N, LMV324-N	–40	125	°C
Temperature Range [4]: LMV321-N-Q1, LMV358-N-Q1, LMV324-N-Q1	–40	125	°C
Temperature Range [4]: LMV321-N-Q3, LMV358-N-Q3, LMV324-N-Q3	–40	85	°C

7.5 Thermal Information - Commercial

THERMAL METRIC[(1)]		LMV321-N		LMV324-N		LMV358-N		UNIT
		DBV	DCK	D	PW	D	DGK	
		5 PINS		14 PINS		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	265	478	145	155	207.9	235	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.6 Thermal Information - Automotive

THERMAL METRIC[(1)]		LMV321-N-Q1, LMV321-N-Q3	LMV324-N-Q1, LMV324-N-Q3		LMV358-N-Q1, LMV358-N-Q3		UNIT
		DBV	D	PW	D	DGK	
		5 PINS	14 PINS		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	265	145	155	190	235	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.7 2.7-V DC Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.0 V, V_O = V^+/2 and R_L > 1 MΩ.

		TEST CONDITIONS	MIN[(6)]	TYP[(5)]	MAX[(6)]	UNIT
V_{OS}	Input Offset Voltage			1.7	7	mV
TCV_{OS}	Input Offset Voltage Average Drift			5		μV/°C
I_B	Input Bias Current			11	250	nA
I_{OS}	Input Offset Current			5	50	nA
CMRR	Common Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 1.7 V	50	63		dB
PSRR	Power Supply Rejection Ratio	2.7 V ≤ V^+ ≤ 5 V V_O = 1V	50	60		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	0	−0.2		V
				1.9	1.7	V
V_O	Output Swing	R_L = 10 kΩ to 1.35 V	V^+ −100	V^+ −10		mV
				60	180	mV
I_S	Supply Current	Single		80	170	μA
		Dual Both amplifiers		140	340	μA
		Quad All four amplifiers		260	680	μA

7.8 2.7-V AC Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 1.0 V, V_O = V^+/2 and R_L > 1 MΩ.

		TEST CONDITIONS	MIN[(6)]	TYP[(5)]	MAX[(6)]	UNIT
GBWP	Gain-Bandwidth Product	C_L = 200 pF		1		MHz
Φ_m	Phase Margin			60		Deg
G_m	Gain Margin			10		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz		46		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz		0.17		$\frac{pA}{\sqrt{Hz}}$

7.9 5-V DC Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2.0 V, V_O = V^+/2 and R_L > 1 MΩ.

		TEST CONDITIONS	MIN(6)	TYP(5)	MAX(6)	UNIT
V_{OS}	Input Offset Voltage			1.7	7	mV
		Over Temperature			9	
TCV_{OS}	Input Offset Voltage Average Drift			5		μV/°C
I_B	Input Bias Current			15	250	nA
		Over Temperature			500	
I_{OS}	Input Offset Current			5	50	nA
		Over Temperature			150	
CMRR	Common Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 4 V	50	65		dB
PSRR	Power Supply Rejection Ratio	2.7 V ≤ V^+ ≤ 5 V V_O = 1V, V_{CM} = 1 V	50	60		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	0	−0.2		V
				4.2	4	V
A_V	Large Signal Voltage Gain (7)	R_L = 2 kΩ	15	100		V/mV
		R_L = 2 kΩ, Over Temperature	10			
V_O	Output Swing	R_L = 2 kΩ to 2.5 V	V^+ − 300	V^+ −40		mV
		R_L = 2 kΩ to 2.5 V, Over Temperature	V^+ − 400			
		R_L = 2 kΩ to 2.5 V		120	300	
		R_L = 2 kΩ to 2.5 V, Over Temperature			400	
		R_L = 10 kΩ to 2.5 V	V^+ − 100	V^+ − 10		
		R_L = 10 kΩ to 2.5 V, Over Temperature	V^+ − 200			
		R_L = 2 kΩ to 2.5 V		65	180	
		R_L = 2 kΩ to 2.5 V, 125°C			280	
I_O	Output Short Circuit Current	Sourcing, V_O = 0 V, LMV3xx-N	5	40		mA
		Sinking, V_O = 5 V, LMV3xx-N	10	40		
		Sourcing, V_O = 0 V	5	60		
		Sinking, V_O = 5 V	10	160		
I_S	Supply Current	Single		130	250	μA
		Single, Over Temperature			350	
		Dual (both amps)		210	440	
		Dual (both amps), Over Temperature			615	
		Quad (all four amps)		410	830	
		Quad (all four amps), Over Temperature			1160	

7.10 5-V AC Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 2.0 V, V_O = $V^+/2$ and R_L > 1 MΩ.

		TEST CONDITIONS	MIN(6)	TYP(5)	MAX(6)	UNIT
SR	Slew Rate	(8)		1		V/µs
GBWP	Gain-Bandwidth Product	C_L = 200 pF		1		MHz
Φ_m	Phase Margin			60		Deg
G_m	Gain Margin			10		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz		39		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz		0.21		$\frac{pA}{\sqrt{Hz}}$

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. *Section 7.4* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) Shorting output to V^+ will adversely affect reliability.
(3) Shorting output to V^- will adversely affect reliability.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC Board.
(5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(6) All limits are ensured by testing or statistical analysis.
(7) R_L is connected to V^-. The output voltage is 0.5 V ≤ V_O ≤ 4.5 V.
(8) Connected as voltage follower with 3-V step input. Number specified is the slower of the positive and negative slew rates.
(9) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.

7.11 Typical Characteristics

Unless otherwise specified, V_S = 5 V, single supply, T_A = 25°C.

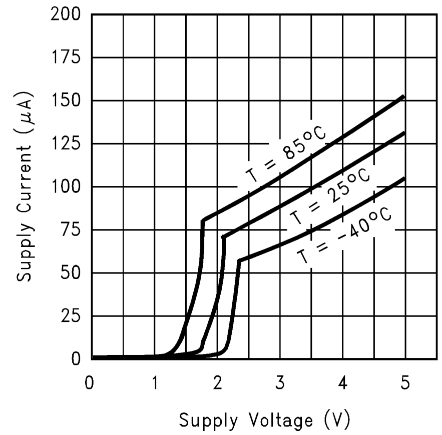


Figure 7-1. Supply Current vs Supply Voltage (LMV321-N)

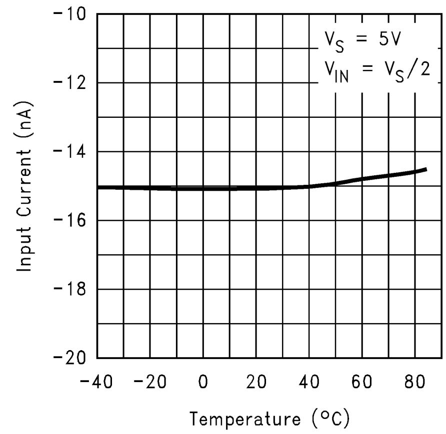


Figure 7-2. Input Current vs Temperature

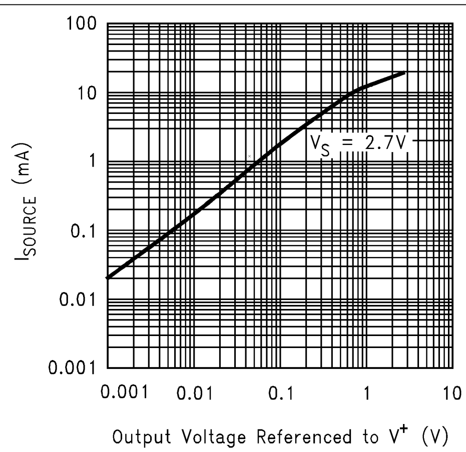


Figure 7-3. Sourcing Current vs Output Voltage

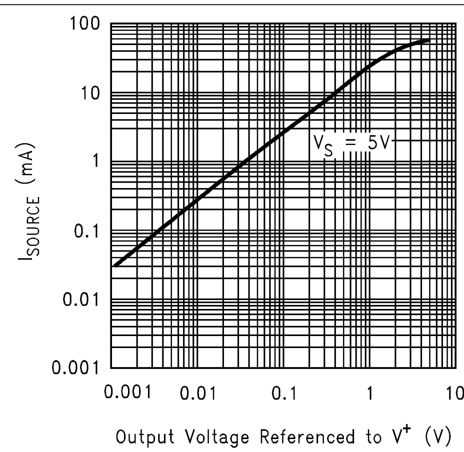


Figure 7-4. Sourcing Current vs Output Voltage

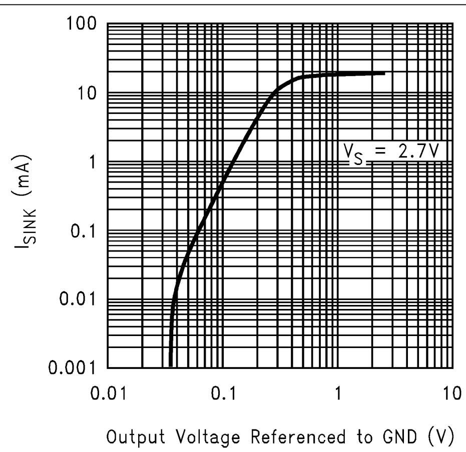


Figure 7-5. Sinking Current vs Output Voltage

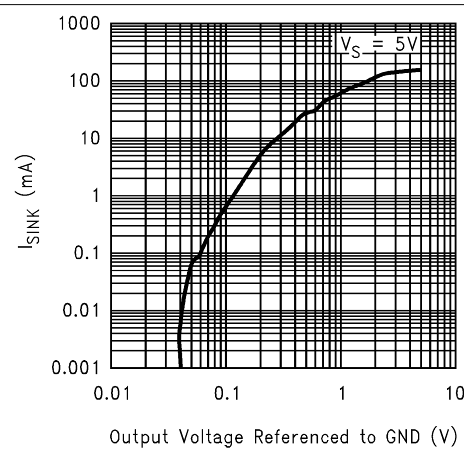


Figure 7-6. Sinking Current vs Output Voltage

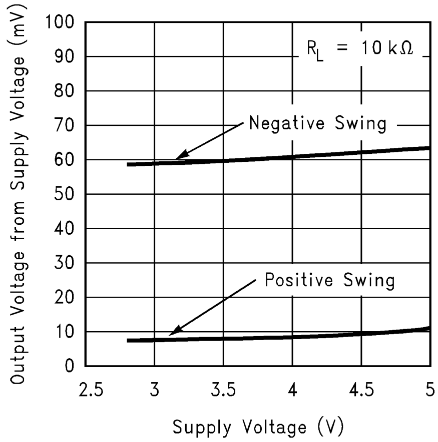


Figure 7-7. Output Voltage Swing vs Supply Voltage

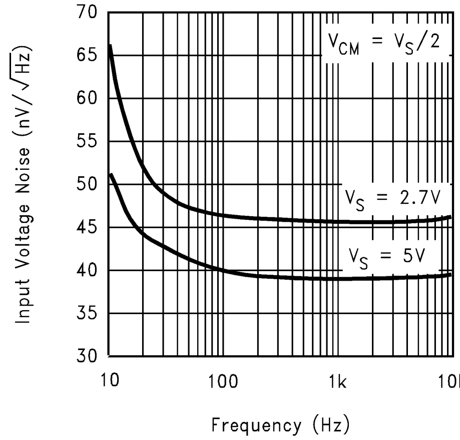


Figure 7-8. Input Voltage Noise vs Frequency

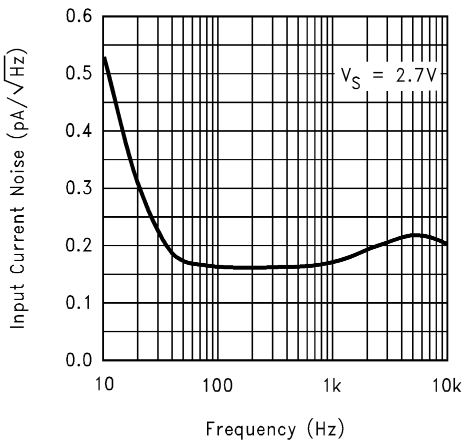


Figure 7-9. Input Current Noise vs Frequency

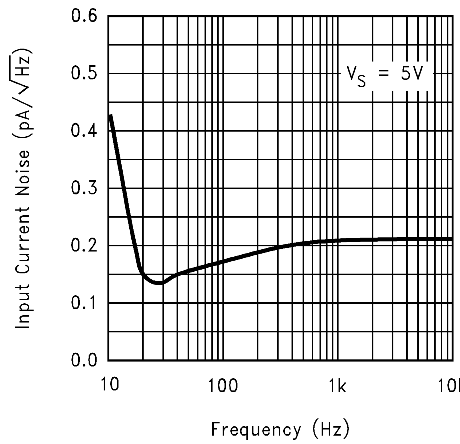


Figure 7-10. Input Current Noise vs Frequency

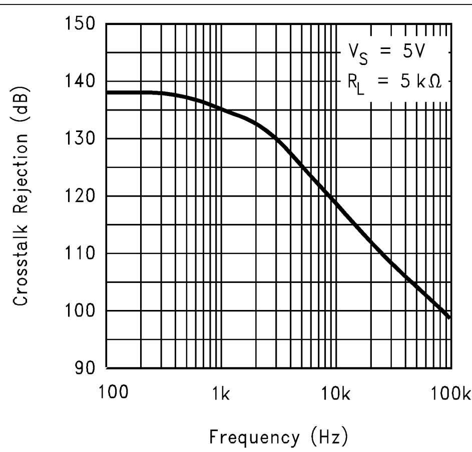


Figure 7-11. Crosstalk Rejection vs Frequency

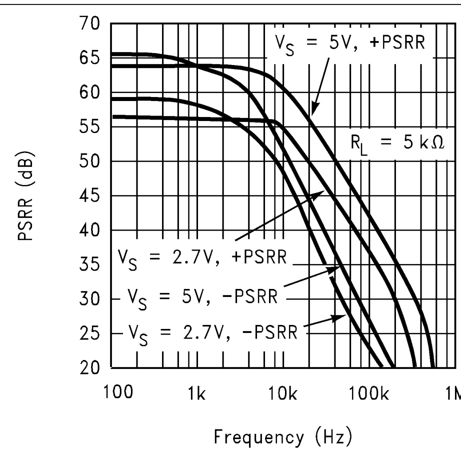


Figure 7-12. PSRR vs Frequency

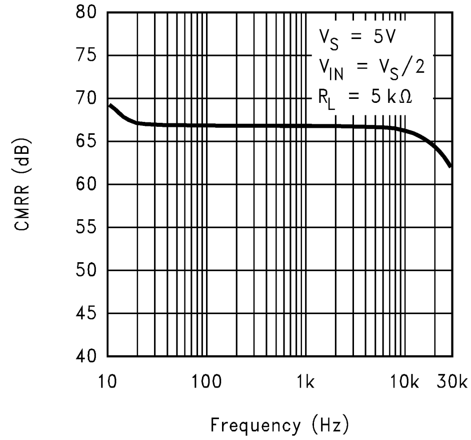


Figure 7-13. CMRR vs Frequency

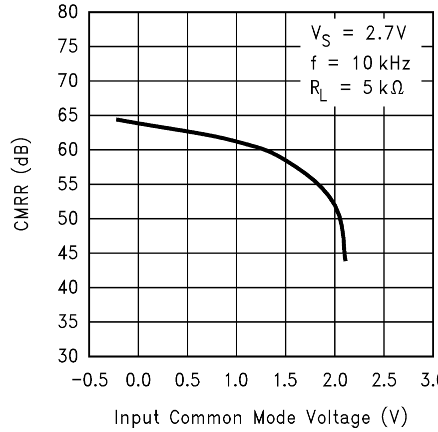


Figure 7-14. CMRR vs Input Common Mode Voltage

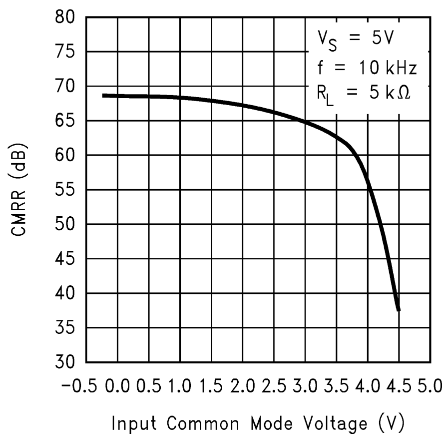


Figure 7-15. CMRR vs Input Common Mode Voltage

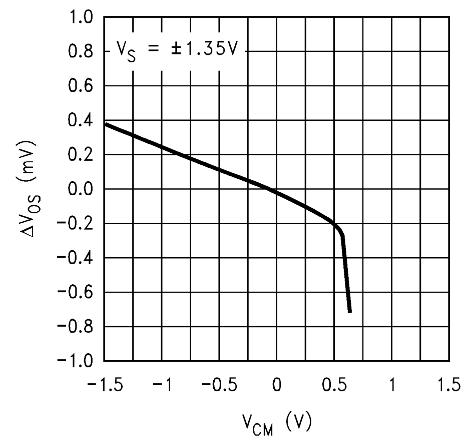


Figure 7-16. ΔV_{OS} vs CMR

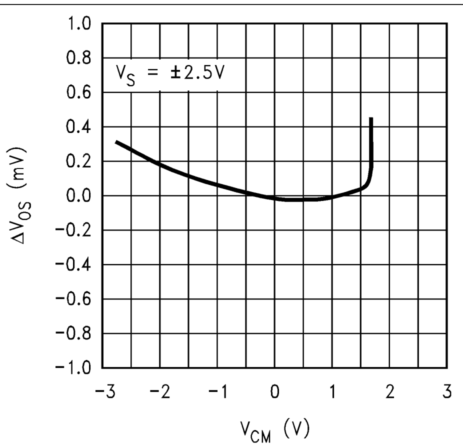


Figure 7-17. ΔV_{OS} vs CMR

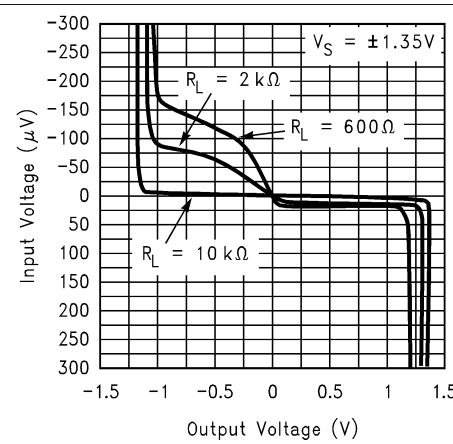


Figure 7-18. Input Voltage vs Output Voltage

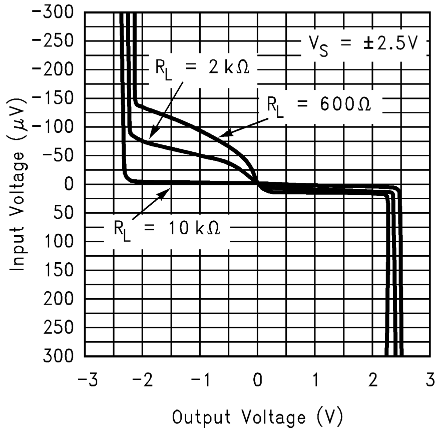


Figure 7-19. Input Voltage vs Output Voltage

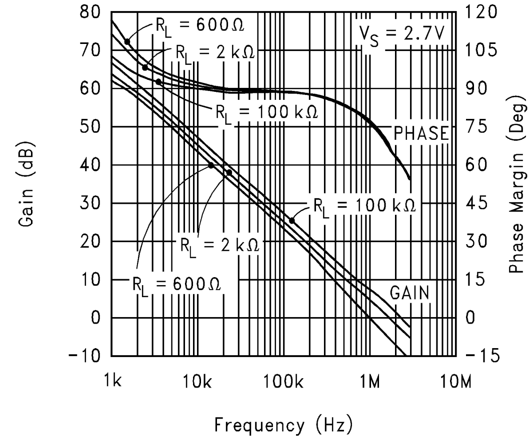


Figure 7-20. Open Loop Frequency Response

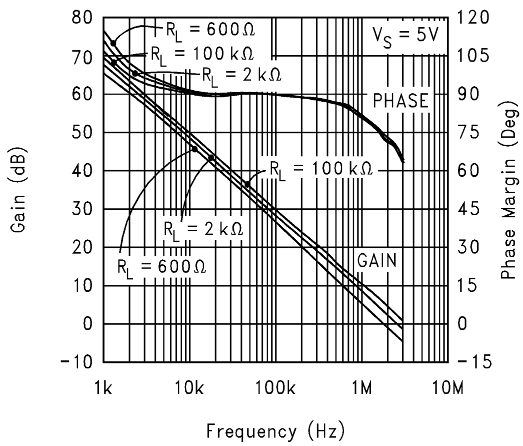


Figure 7-21. Open Loop Frequency Response

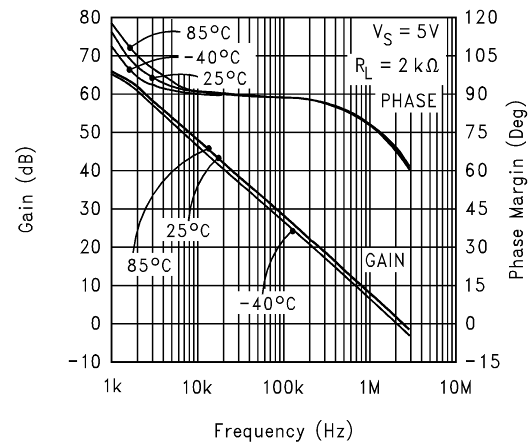


Figure 7-22. Open Loop Frequency Response vs Temperature

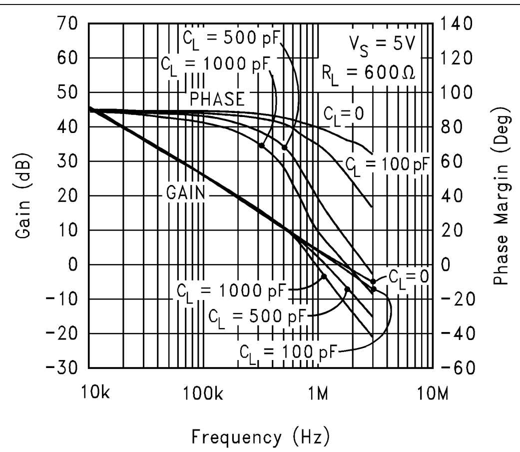


Figure 7-23. Gain and Phase vs Capacitive Load

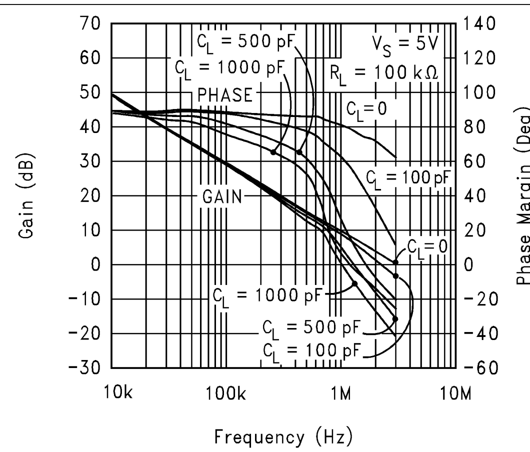


Figure 7-24. Gain and Phase vs Capacitive Load

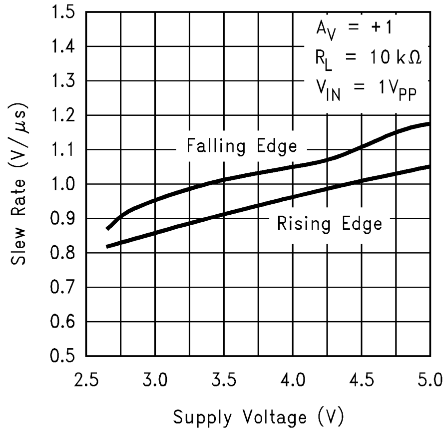


Figure 7-25. Slew Rate vs Supply Voltage

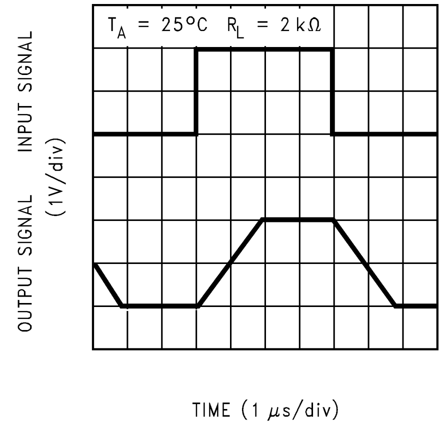


Figure 7-26. Non-Inverting Large Signal Pulse Response

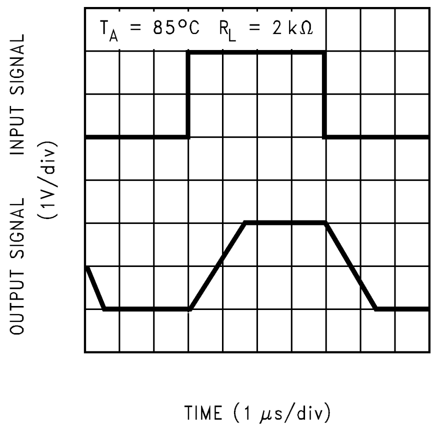


Figure 7-27. Non-Inverting Large Signal Pulse Response

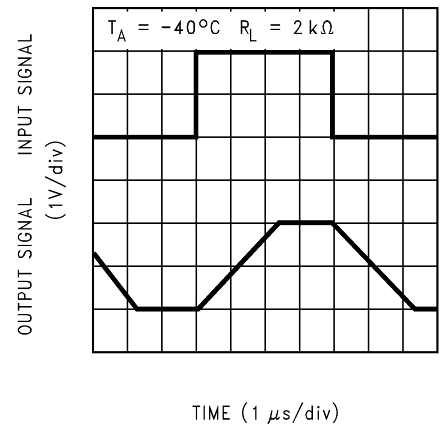


Figure 7-28. Non-Inverting Large Signal Pulse Response

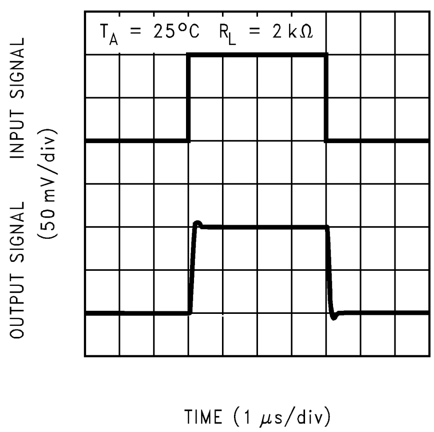


Figure 7-29. Non-Inverting Small Signal Pulse Response

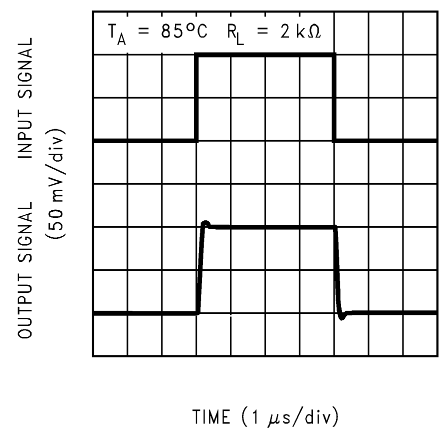


Figure 7-30. Non-Inverting Small Signal Pulse Response

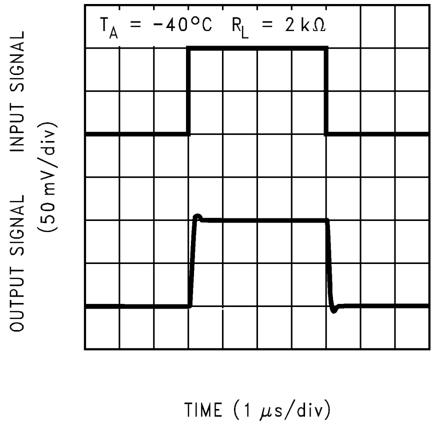


Figure 7-31. Non-Inverting Small Signal Pulse Response

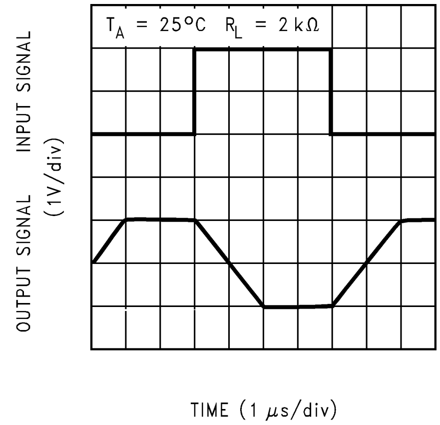


Figure 7-32. Inverting Large Signal Pulse Response

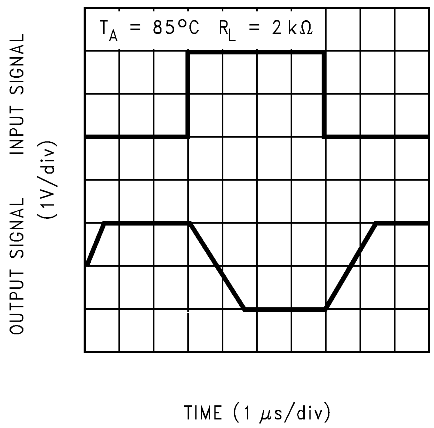


Figure 7-33. Inverting Large Signal Pulse Response

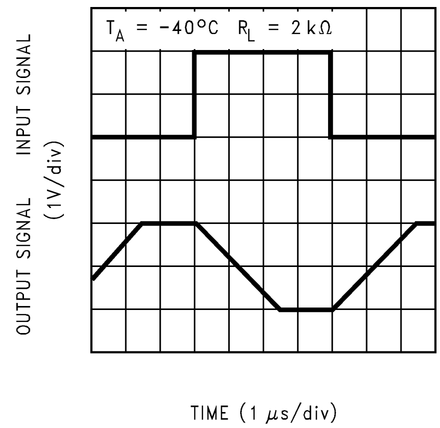


Figure 7-34. Inverting Large Signal Pulse Response

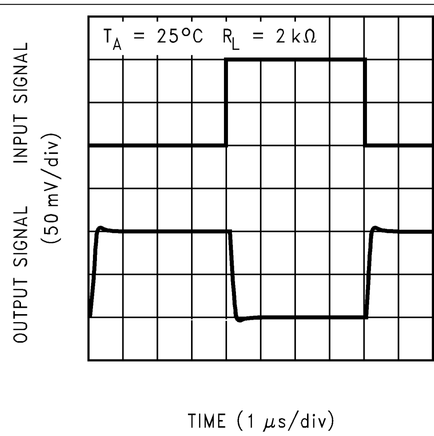


Figure 7-35. Inverting Small Signal Pulse Response

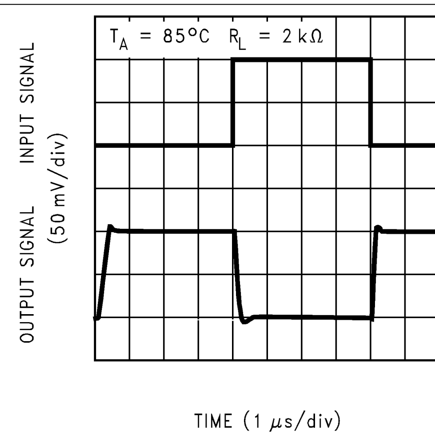


Figure 7-36. Inverting Small Signal Pulse Response

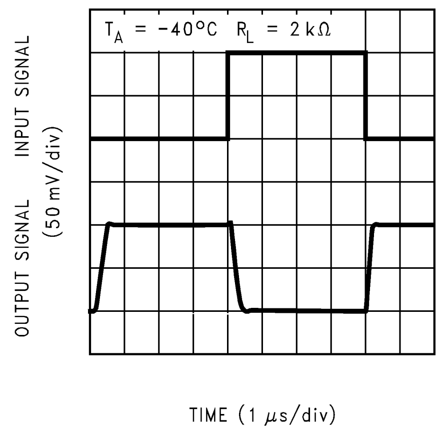


Figure 7-37. Inverting Small Signal Pulse Response

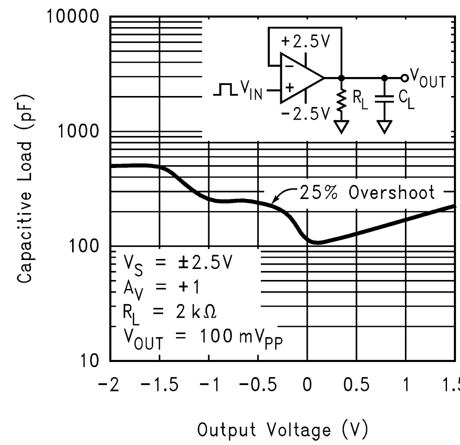


Figure 7-38. Stability vs Capacitive Load

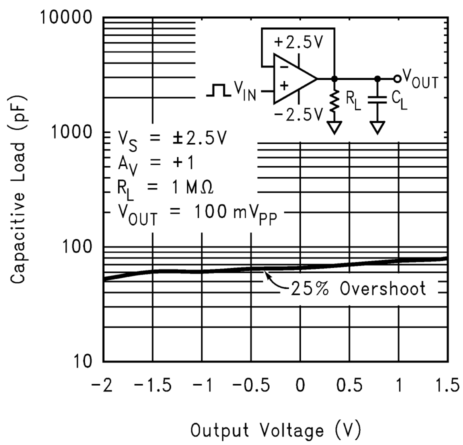


Figure 7-39. Stability vs Capacitive Load

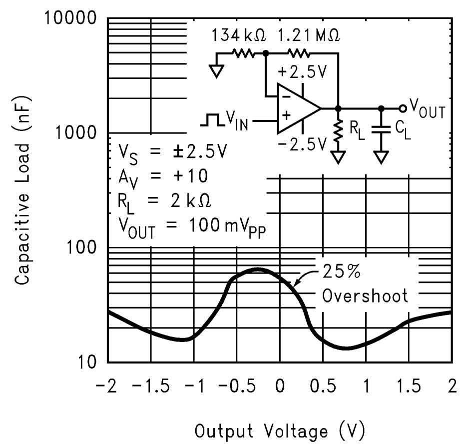


Figure 7-40. Stability vs Capacitive Load

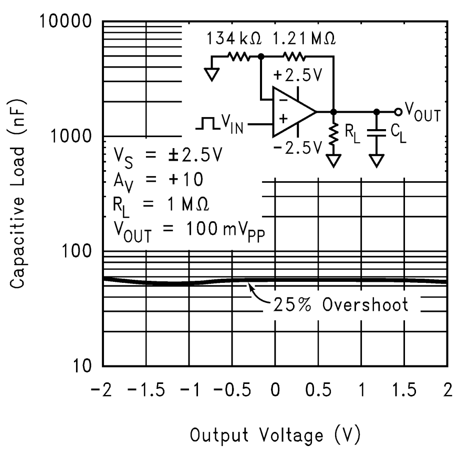


Figure 7-41. Stability vs Capacitive Load

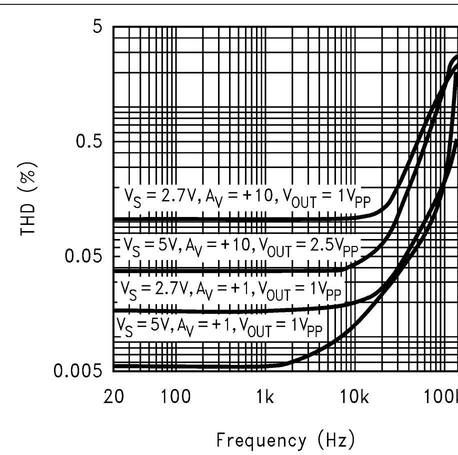


Figure 7-42. THD vs Frequency

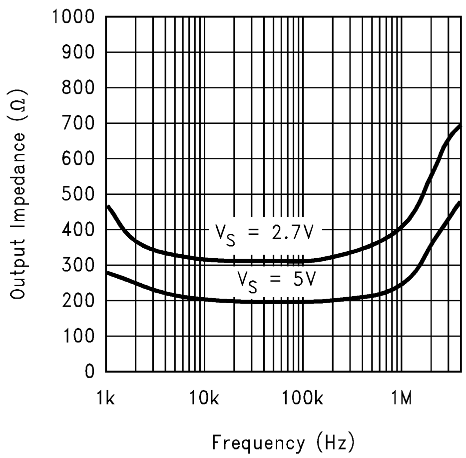


Figure 7-43. Open Loop Output Impedance vs Frequency

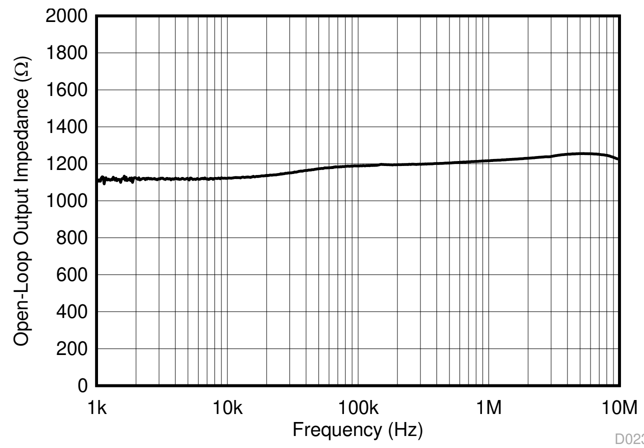


Figure 7-44. Open Loop Output Impedance vs Frequency (LM3xx-N)

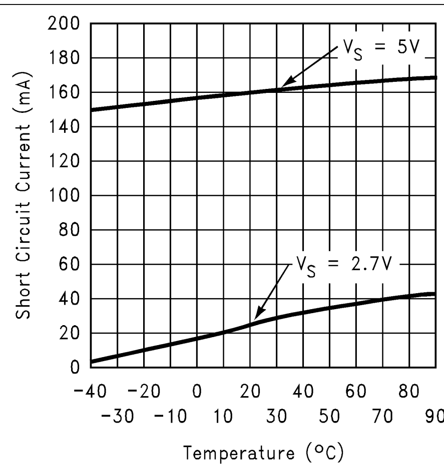


Figure 7-45. Short Circuit Current vs Temperature (Sinking)

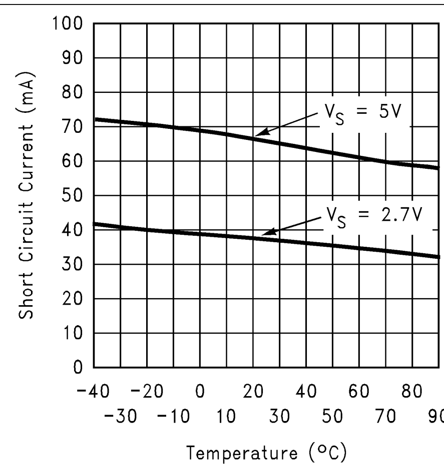


Figure 7-46. Short Circuit Current vs Temperature (Sourcing)

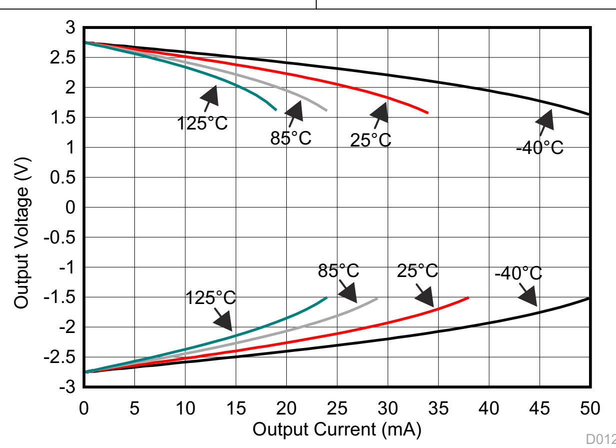


Figure 7-47. Output Voltage vs Output Current (LMV3xx-N)

8 Detailed Description

8.1 Overview

The LMV358-N/LMV324-N are low voltage (2.7 V to 5.5 V) versions of the dual and quad commodity op amps LM358/LM324 (5 V to 30 V). The LMV321-N is the single channel version. The LMV321-N/LMV358-N/LMV324-N are the most cost effective solutions for applications where low voltage operation, space efficiency, and low price are important. They offer specifications that meet or exceed the familiar LM358/LM324. The LMV321-N/LMV358-N/LMV324-N have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed to power ratio, achieving 1 MHz of bandwidth and 1-V/µs slew rate with low supply current.

8.1.1 Benefits of the LMV321-N/LMV358-N/LMV324-N

8.1.1.1 Size

The small footprints of the LMV321-N/LMV358-N/LMV324-N packages save space on printed circuit boards, and enable the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. The low profile of the LMV321-N/LMV358-N/LMV324-N make them possible to use in PCMCIA type III cards.

8.1.1.2 Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the LMV321-N/LMV358-N/LMV324-N can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

8.1.1.3 Simplified Board Layout

These products help you to avoid using long PC traces in your PC board layout. This means that no additional components, such as capacitors and resistors, are needed to filter out the unwanted signals due to the interference between the long PC traces.

8.1.1.4 Low Supply Current

These devices will help you to maximize battery life. They are ideal for battery powered systems.

8.1.1.5 Low Supply Voltage

Texas Instruments provides ensured performance at 2.7 V and 5 V. These specifications ensure operation throughout the battery lifetime.

8.1.1.6 Rail-to-Rail Output

Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

8.1.1.7 Input Includes Ground

Allows direct sensing near GND in single supply operation.

Protection should be provided to prevent the input voltages from going negative more than −0.3 V (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

8.1.1.8 Ease of Use and Crossover Distortion

The LMV321-N/LMV358-N/LMV324-N offer specifications similar to the familiar LM324-N. In addition, the new LMV321-N/LMV358-N/LMV324-N effectively eliminate the output crossover distortion. The scope photos in Figure 8-1 and Figure 8-2 compare the output swing of the LMV324-N and the LM324-N in a voltage follower configuration, with V_S = ± 2.5 V and R_L (= 2 kΩ) connected to GND. It is apparent that the crossover distortion has been eliminated in the new LMV324-N.

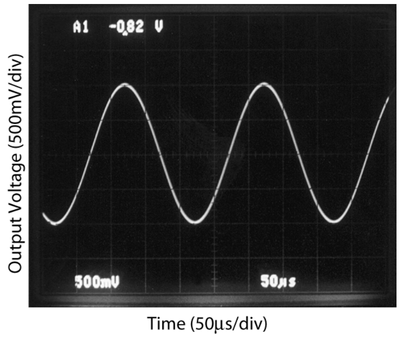


Figure 8-1. Output Swing of LMV324

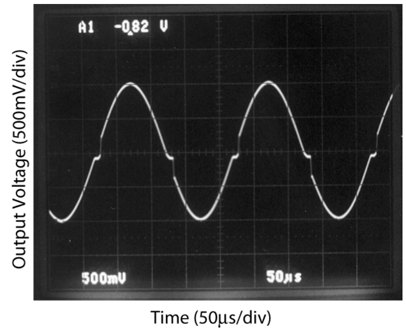
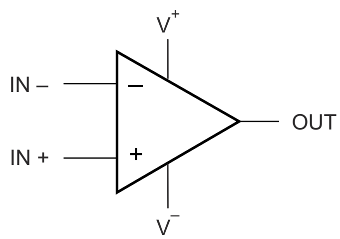


Figure 8-2. Output Swing of LM324

8.2 Functional Block Diagram



Each Amplifier

8.3 Feature Description

8.3.1 Capacitive Load Tolerance

The LMV321-N/LMV358-N/LMV324-N can directly drive 200 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, the circuit in Figure 8-3 can be used.

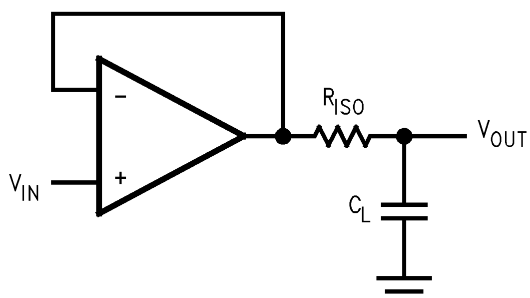


Figure 8-3. Indirectly Driving a Capacitive Load Using Resistive Isolation

In Figure 8-3, the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Figure 8-4 is an output waveform of Figure 8-3 using 620 Ω for R_{ISO} and 510 pF for C_L.

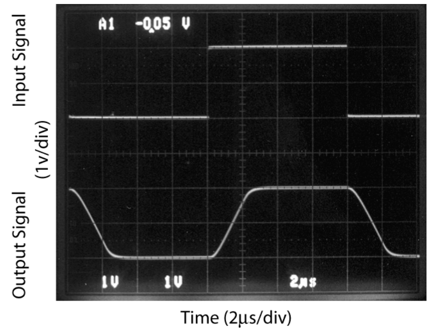


Figure 8-4. Pulse Response of the LMV324 Circuit in Figure 8-3

The circuit in Figure 8-5 is an improvement to the one in Figure 8-3 because it provides DC accuracy as well as AC stability. If there were a load resistor in Figure 8-3, the output would be voltage divided by R_{ISO} and the load resistor. Instead, in Figure 8-5, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L. Caution is needed in choosing the value of R_F due to the input bias current of the LMV321-N/LMV358-N/LMV324-N. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F. This in turn will slow down the pulse response.

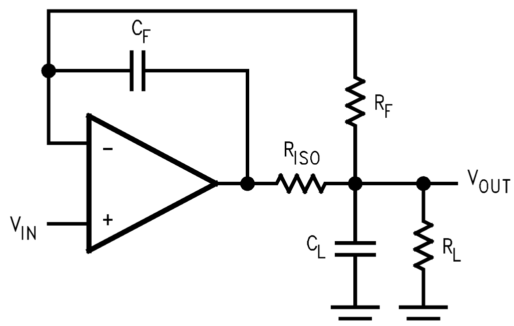


Figure 8-5. Indirectly Driving A Capacitive Load With DC Accuracy

8.3.2 Input Bias Current Cancellation

The LMV321-N/LMV358-N/LMV324-N family has a bipolar input stage. The typical input bias current of LMV321-N/LMV358-N/LMV324-N is 15 nA with 5V supply. Thus a 100 kΩ input resistor will cause 1.5 mV of error voltage. By balancing the resistor values at both inverting and non-inverting inputs, the error caused by the amplifier's input bias current will be reduced. The circuit in Figure 8-6 shows how to cancel the error caused by input bias current.

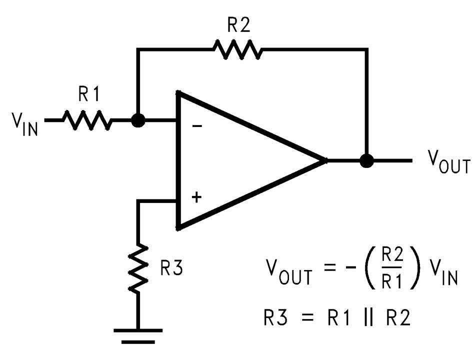


Figure 8-6. Cancelling the Error Caused by Input Bias Current

8.4 Device Functional Modes

The LMV321-N/LMV321-N-Q1/LMV358-N/LMV358-N-Q1/LMV324-N/LMV324-N-Q1 are powered on when the supply is connected. They can be operated as a single supply or a dual supply operational amplifier depending on the application.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMV32x-N family of amplifiers is specified for operation from 2.7 V to 5 V (±1.35 V to ±2.5 V). Many of the specifications apply from –40°C to 125°C. They provide ground-sensing inputs as well as rail-to-rail output swing. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

9.2 Typical Applications

9.2.1 Simple Low-Pass Active Filter

A simple active low-pass filter is shown in Figure 9-1.

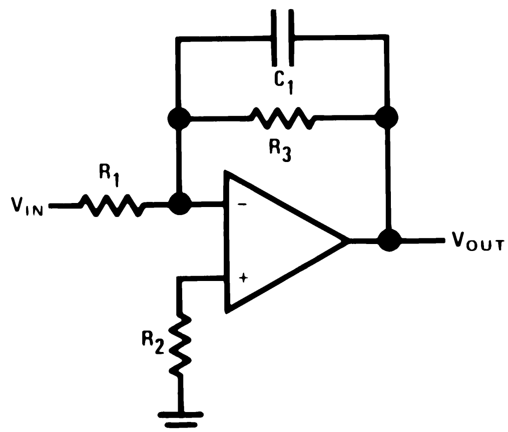


Figure 9-1. Simple Low-Pass Active Filter

9.2.1.1 Design Requirements

The simple single pole active lowpass filter shown in Figure 9-1 will pass low frequencies and attenuate frequencies above corner frequency (fc) at a roll-off rate of 20 dB/Decade.

9.2.1.2 Detailed Design Procedure

The values of R1, R2, R3, and C1 are selected using the formulas in Figure 9-2. The low-frequency gain (ω → 0) is defined by $-R_3/R_1$. This allows low-frequency gains other than unity to be obtained. The filter has a −20 dB/decade roll-off after its corner frequency fc. R_2 should be chosen equal to the parallel combination of R_1 and R_3 to minimize errors due to bias current. The frequency response of the filter is shown in Figure 9-3.

$$A_L = -\frac{R_3}{R_1}$$

$$f_c = \frac{1}{2\pi R_3 C_1}$$

$$R_2 = R_1 \,||\, R_3$$

Figure 9-2. Simple Low-Pass Active Filter Equations

9.2.1.3 Application Curves

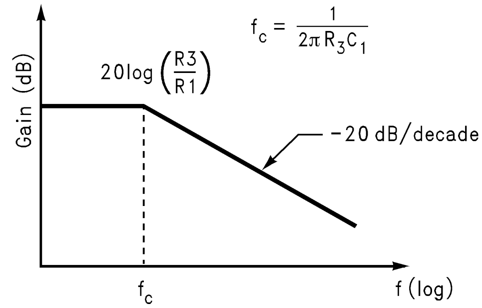


Figure 9-3. Frequency Response of Simple Low-Pass Active Filter

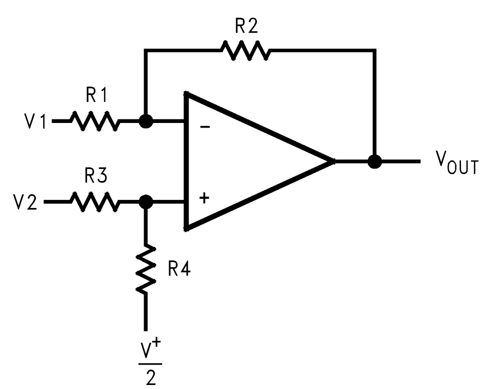
Note that the single-op-amp active filters are used in the applications that require low quality factor, Q (≤ 10), low frequency (≤ 5 kHz), and low gain (≤ 10), or a small value for the product of gain times Q (≤ 100). The op amp should have an open loop voltage gain at the highest frequency of interest at least 50 times larger than the gain of the filter at this frequency. In addition, the selected op amp should have a slew rate that meets the following requirement:

$$\text{Slew Rate} \geq 0.5 \times (\omega_H V_{OPP}) \times 10^{-6}\ \text{V/µsec} \tag{1}$$

where ω_H is the highest frequency of interest, and V_{OPP} is the output peak-to-peak voltage.

9.2.2 Difference Amplifier

The difference amplifier allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to two inputs. It is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.



$$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R4}{R1}V_2 - \frac{R2}{R1}V_1 + \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R3}{R1} \cdot \frac{V^+}{2}$$

for R1 = R3 and R2 = R4

$$V_{OUT} = \frac{R2}{R1}\left(V_2 - V_1\right) + \frac{V^+}{2}$$

Figure 9-4. Difference Amplifier

9.2.3 Instrumentation Circuits

The input impedance of the previous difference amplifier is set by the resistors R_1, R_2, R_3, and R_4. To eliminate the problems of low input impedance, one way is to use a voltage follower ahead of each input as shown in the following two instrumentation amplifiers.

9.2.3.1 Three-Op-Amp Instrumentation Amplifier

The quad LMV324 can be used to build a three-op-amp instrumentation amplifier as shown in Figure 9-5.

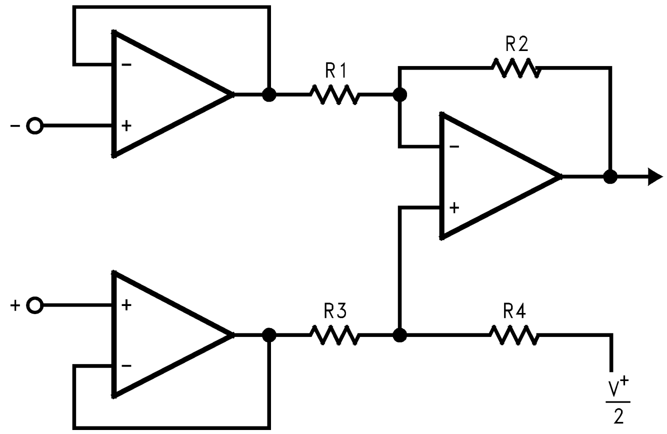
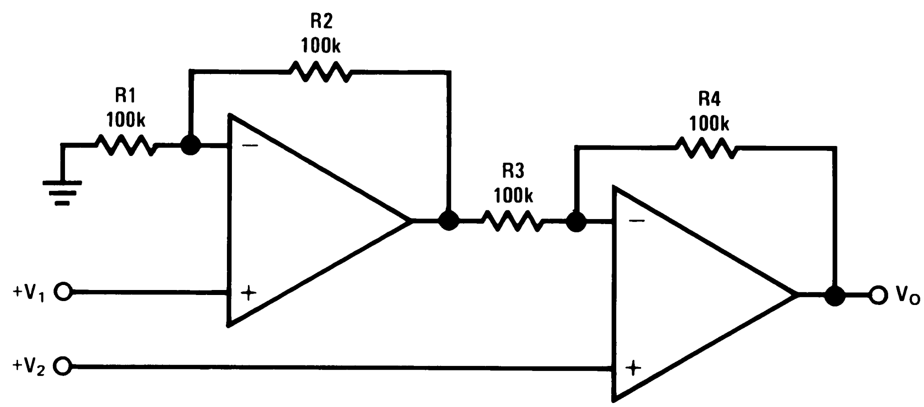


Figure 9-5. Three-Op-Amp Instrumentation Amplifier

The first stage of this instrumentation amplifier is a differential-input, differential-output amplifier, with two voltage followers. These two voltage followers assure that the input impedance is over 100 MΩ. The gain of this instrumentation amplifier is set by the ratio of R_2/R_1. R_3 should equal R_1, and R_4 should equal R_2. Matching of R_3 to R_1, and R_4 to R_2 affects the CMRR. For good CMRR over temperature, low drift resistors should be used. Making R_4 slightly smaller than R_2 and adding a trim pot equal to twice the difference between R_2 and R_4 will allow the CMRR to be adjusted for optimum performance.

9.2.3.2 Two-Op-Amp Instrumentation Amplifier

A two-op-amp instrumentation amplifier can also be used to make a high-input-impedance DC differential amplifier (Figure 9-6). As in the three-op-amp circuit, this instrumentation amplifier requires precise resistor matching for good CMRR. R_4 should equal R_1, and R_3 should equal R_2.



$$V_O = \left(1 + \frac{R4}{R3}\right)\left(V_2 - V_1\right), \text{ where } R1 = R4 \text{ and } R2 = R3$$

$$\text{As shown: } V_O = 2\left(V_2 - V_1\right)$$

Figure 9-6. Two-Op-Amp Instrumentation Amplifier

9.2.3.3 Single-Supply Inverting Amplifier

There may be cases where the input signal going into the amplifier is negative. Because the amplifier is operating in single supply voltage, a voltage divider using R_3 and R_4 is implemented to bias the amplifier so the input signal is within the input common-mode voltage range of the amplifier. The capacitor C_1 is placed between the inverting input and resistor R_1 to block the DC signal going into the AC signal source, V_{IN}. The values of R_1 and C_1 affect the cutoff frequency, $fc = 1 / 2\pi R_1 C_1$.

As a result, the output signal is centered around mid-supply (if the voltage divider provides $V^+ / 2$ at the non-inverting input). The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system.

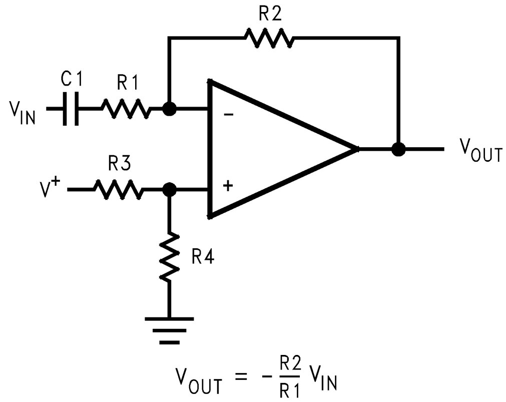


Figure 9-7. Single-Supply Inverting Amplifier

9.2.4 Sallen-Key 2nd-Order Active Low-Pass Filter

The Sallen-Key 2nd-order active low-pass filter is illustrated in Figure 9-8. The DC gain of the filter is expressed as:

$$A_{LP} = \frac{R_3}{R_4} + 1 \tag{2}$$

The transfer function is:

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{\frac{1}{C_1 C_2 R_1 R_2} A_{LP}}{S^2 + S\left(\frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} - \frac{A_{LP}}{C_2 R_2}\right) + \frac{1}{C_1 C_2 R_1 R_2}} \tag{3}$$

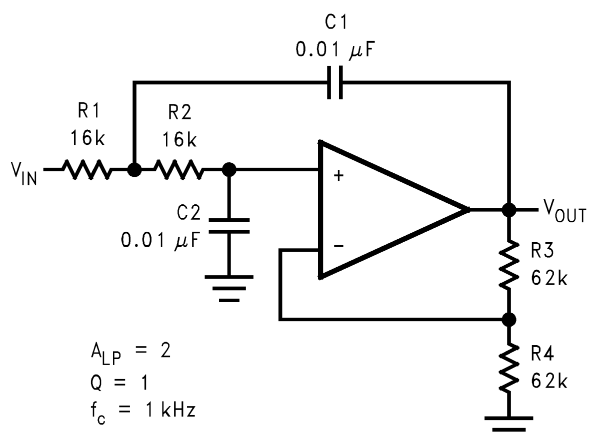


Figure 9-8. Sallen-Key 2nd-Order Active Low-Pass Filter

9.2.4.1 Detailed Design Procedure

The following paragraphs explain how to select values for R_1, R_2, R_3, R_4, C_1, and C_2 for given filter requirements, such as A_{LP}, Q, and f_c.

The standard form for a 2nd-order low pass filter is:

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{A_{LP}\,\omega_c^{\,2}}{S^2 + \left(\frac{\omega_c}{Q}\right)S + \omega_c^{\,2}} \tag{4}$$

where

Q: Pole Quality Factor

ω_C: Corner Frequency

A comparison between Equation 3 and Equation 4 yields:

$$\omega_c^{\,2} = \frac{1}{C_1\,C_2\,R_1\,R_2} \tag{5}$$

$$\frac{\omega_c}{Q} = \frac{1}{C_1\,R_1} + \frac{1}{C_1\,R_2} + \frac{1}{C_2\,R_2} - \frac{A_{LP}}{C_2\,R_2} \tag{6}$$

To reduce the required calculations in filter design, it is convenient to introduce normalization into the components and design parameters. To normalize, let $\omega_C = \omega_n$ = 1 rad/s, and $C_1 = C_2 = C_n$ = 1F, and substitute these values into Equation 5 and Equation 6. From Equation 5, we obtain:

$$R_1 = \frac{1}{R_2} \tag{7}$$

From Equation 6, we obtain:

$$R_2 = \frac{1 \pm \sqrt{1 - 4Q^2(2 - A_{LP})}}{2Q} \tag{8}$$

For minimum DC offset, $V^+ = V^-$, the resistor values at both inverting and non-inverting inputs should be equal, which means:

$$R_1 + R_2 = \frac{R_3\,R_4}{R_3 + R_4} \tag{9}$$

From Equation 2 and Equation 9, we obtain:

$$R_3 = (R_1 + R_2)A_{LP} \tag{10}$$

$$R_4 = \left(\frac{A_{LP}}{A_{LP} - 1}\right)(R_1 + R_2) \tag{11}$$

The values of C_1 and C_2 are normally close to or equal to:

$$C = \frac{10}{f_c}\,\mu F \tag{12}$$

As a design example:

Require: A_{LP} = 2, Q = 1, fc = 1 kHz

Start by selecting C_1 and C_2. Choose a standard value that is close to:

$$C = \frac{10}{f_c}\,\mu F \tag{13}$$

$$C_1 = C_2 = \frac{10}{1 \times 10^3}\,\mu F = 0.01\,\mu F \tag{14}$$

From Equation 7, Equation 8, Equation 10, and Equation 11,

$$R_1 = 1\,\Omega \tag{15}$$

$$R_2 = 1\,\Omega \tag{16}$$

$$R_3 = 4\,\Omega \tag{17}$$

$$R_4 = 4\,\Omega \tag{18}$$

The above resistor values are normalized values with ω_n = 1 rad/s and $C_1 = C_2 = C_n$ = 1F. To scale the normalized cutoff frequency and resistances to the real values, two scaling factors are introduced, frequency scaling factor (k_f) and impedance scaling factor (k_m).

$$k_f = \frac{\omega_c}{\omega_n} = \frac{2\pi \times 1 \times 10^3}{1} = 2\pi \times 10^3$$

$$k_m k_f = \frac{Cn}{C1}$$

$$k_m = 1.59 \times 10^4 \tag{19}$$

Scaled values:

$$R_2 = R_1 = 15.9\ k\Omega \tag{20}$$

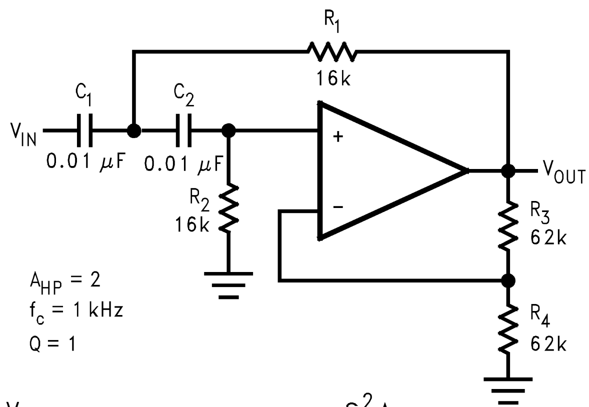
$$R_3 = R_4 = 63.6\ k\Omega \tag{21}$$

$$C_1 = C_2 = 0.01\ \mu F \tag{22}$$

An adjustment to the scaling may be made in order to have realistic values for resistors and capacitors. The actual value used for each component is shown in the circuit.

9.2.5 2nd-Order High Pass Filter

A 2nd-order high pass filter can be built by simply interchanging those frequency selective components (R_1, R_2, C_1, C_2) in the Sallen-Key 2nd-order active low pass filter. As shown in Figure 9-9, resistors become capacitors, and capacitors become resistors. The resulted high pass filter has the same corner frequency and the same maximum gain as the previous 2nd-order low pass filter if the same components are chosen.



$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{S^2 A_{HP}}{S^2 + S\left(\frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} + \frac{(1 - A_{HP})}{C_1 R_1}\right) + \frac{1}{C_1 C_2 R_1 R_2}}$$

Where $A_{HP} = 1 + \frac{R_3}{R_4}$

Figure 9-9. Sallen-Key 2nd-Order Active High-Pass Filter

9.2.6 State Variable Filter

A state variable filter requires three op amps. One convenient way to build state variable filters is with a quad op amp, such as the LMV324 (Figure 9-10).

This circuit can simultaneously represent a low-pass filter, high-pass filter, and bandpass filter at three different outputs. The equations for these functions are listed below. It is also called "Bi-Quad" active filter as it can produce a transfer function which is quadratic in both numerator and denominator.

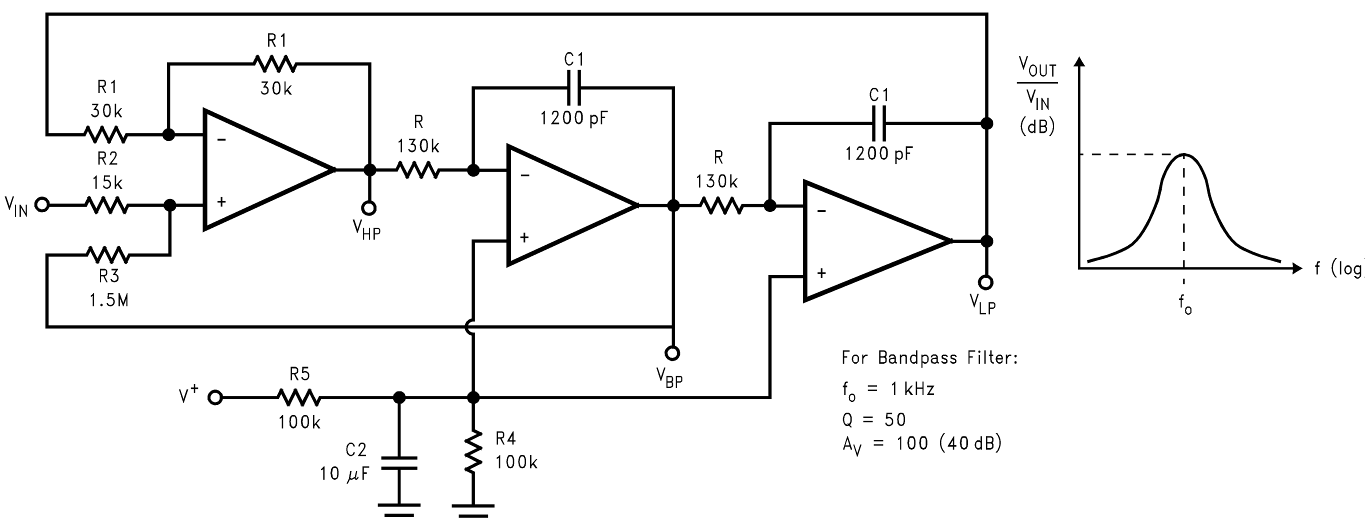


Figure 9-10. State Variable Active Filter

$$V_{LP} = \left(\frac{2R_3}{R_2 + R_3}\right) \frac{\frac{1}{R^2C^2}}{S^2 + \frac{1}{\left(\frac{R_2+R_3}{2R_2}\right)RC} S + \frac{1}{R^2C^2}} V_{IN}$$

$$V_{HP} = \left(\frac{2R_3}{R_2 + R_3}\right) \frac{S^2}{S^2 + \frac{1}{\left(\frac{R_2+R_3}{2R_2}\right)RC} S + \frac{1}{R^2C^2}} V_{IN}$$

$$V_{BP} = \left(\frac{2R_3}{R_2 + R_3}\right) \frac{\left(\frac{1}{RC}\right)S}{S^2 + \frac{1}{\left(\frac{R_2+R_3}{2R_2}\right)RC} S + \frac{1}{R^2C^2}} V_{IN} \quad (23)$$

where for all three filters,

$$Q = \frac{R_2 + R_3}{2R_2} \quad (24)$$

$$\omega_0 = \frac{1}{RC} \quad \text{(resonant frequency)} \quad (25)$$

9.2.6.1 Detailed Design Procedure

Assume the system design requires a bandpass filter with f_O = 1 kHz and Q = 50. What needs to be calculated are capacitor and resistor values.

First choose convenient values for C_1, R_1, and R_2:

$$C_1 = 1200\ \text{pF} \quad (26)$$

$$2R_2 = R_1 = 30\ \text{k}\Omega \quad (27)$$

Then from Equation 24,

$$\begin{aligned} R_3 &= R_2(2Q-1) \\ R_3 &= 15\ \text{k}\Omega \times (2 \times 50 - 1) \\ &= 1.5\ \text{M}\Omega \end{aligned} \quad (28)$$

From Equation 25,

$$\begin{aligned} R &= \frac{1}{\omega_0 C_1} \\ R &= \frac{1}{(2\pi \times 10^3)(1.2 \times 10^{-9})} \\ &= 132.7\ \text{k}\Omega \end{aligned} \quad (29)$$

From the above calculated values, the midband gain is $H_0 = R_3 / R_2 = 100$ (40 dB). The nearest 5% standard values have been added to Figure 9-10.

9.2.7 Pulse Generators and Oscillators

A pulse generator is shown in Figure 9-11. Two diodes have been used to separate the charge and discharge paths to capacitor C.

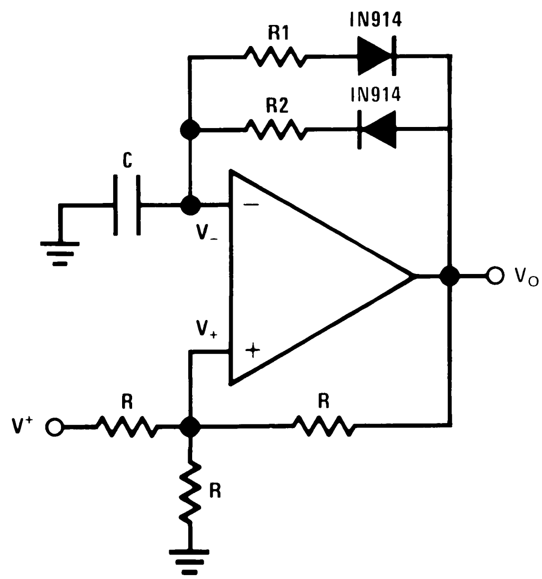
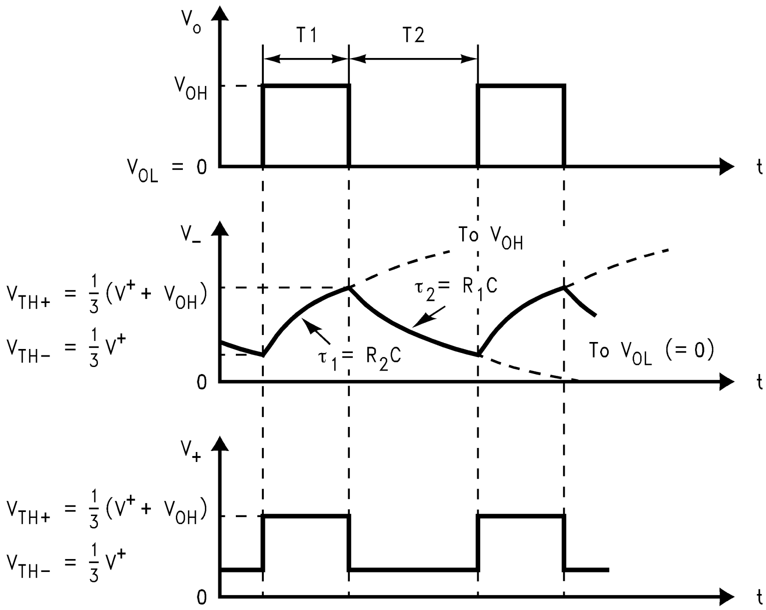


Figure 9-11. Pulse Generator

When the output voltage V_O is first at its high, V_{OH}, the capacitor C is charged toward V_{OH} through R_2. The voltage across C rises exponentially with a time constant $\tau = R_2C$, and this voltage is applied to the inverting input of the op amp. Meanwhile, the voltage at the non-inverting input is set at the positive threshold voltage (V_{TH+}) of the generator. The capacitor voltage continually increases until it reaches V_{TH+}, at which point the output of the generator will switch to its low, V_{OL} which 0 V is in this case. The voltage at the non-inverting input is switched to the negative threshold voltage (V_{TH-}) of the generator. The capacitor then starts to discharge toward V_{OL} exponentially through R_1, with a time constant $\tau = R_1C$. When the capacitor voltage reaches V_{TH-}, the output of the pulse generator switches to V_{OH}. The capacitor starts to charge, and the cycle repeats itself.



$$T_1 = R_2 C \ln \frac{3 V_{OH} - V_{OL} - V^+}{2 V_{OH} - V^+} \quad \text{and} \quad T_2 = R_1 C \ln \frac{3 V_{OL} - V_{OH} - V^+}{2 V_{OL} - V^+}$$

When $V_{OL} = 0V$

$$T_1 = R_2 C \ln \frac{3 V_{OH} - V^+}{2 V_{OH} - V^+} \quad \text{and} \quad T_2 = R_1 C \ln \left(1 + \frac{V_{OH}}{V^+}\right)$$

Figure 9-12. Waveforms of the Circuit in Figure 9-11

As shown in the waveforms in Figure 9-12, the pulse width (T_1) is set by R_2, C and V_{OH}, and the time between pulses (T_2) is set by R_1, C and V_{OL}. This pulse generator can be made to have different frequencies and pulse width by selecting different capacitor value and resistor values.

Figure 9-13 shows another pulse generator, with separate charge and discharge paths. The capacitor is charged through R_1 and is discharged through R_2.

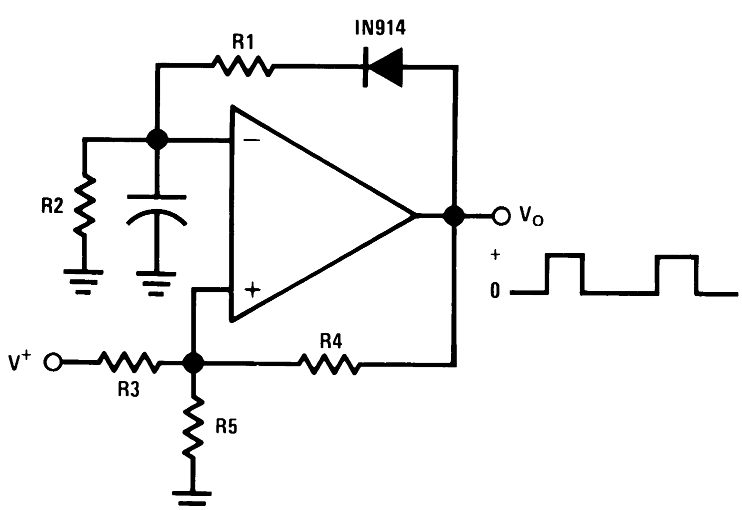


Figure 9-13. Pulse Generator

Figure 9-14 is a squarewave generator with the same path for charging and discharging the capacitor.

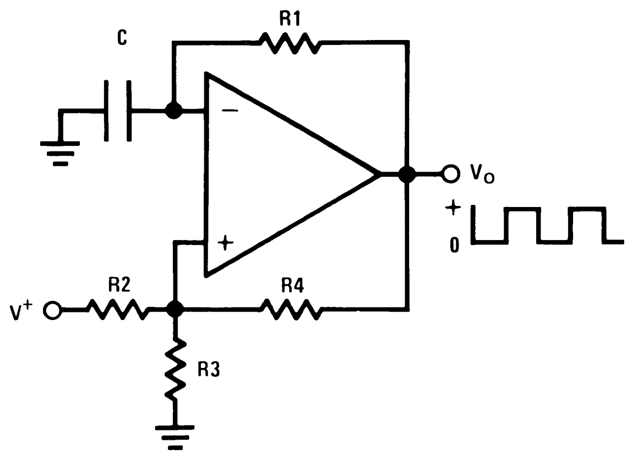


Figure 9-14. Squarewave Generator

9.2.8 Current Source and Sink

The LMV321-N/LMV358-N/LMV324-N can be used in feedback loops which regulate the current in external PNP transistors to provide current sources or in external NPN transistors to provide current sinks.

9.2.8.1 Fixed Current Source

A multiple fixed current source is shown in Figure 9-15. A voltage (V_{REF} = 2 V) is established across resistor R_3 by the voltage divider (R_3 and R_4). Negative feedback is used to cause the voltage drop across R_1 to be equal to V_{REF}. This controls the emitter current of transistor Q_1 and if we neglect the base current of Q_1 and Q_2, essentially this same current is available out of the collector of Q_1.

Large input resistors can be used to reduce current loss and a Darlington connection can be used to reduce errors due to the β of Q_1.

The resistor, R_2, can be used to scale the collector current of Q_2 either above or below the 1 mA reference value.

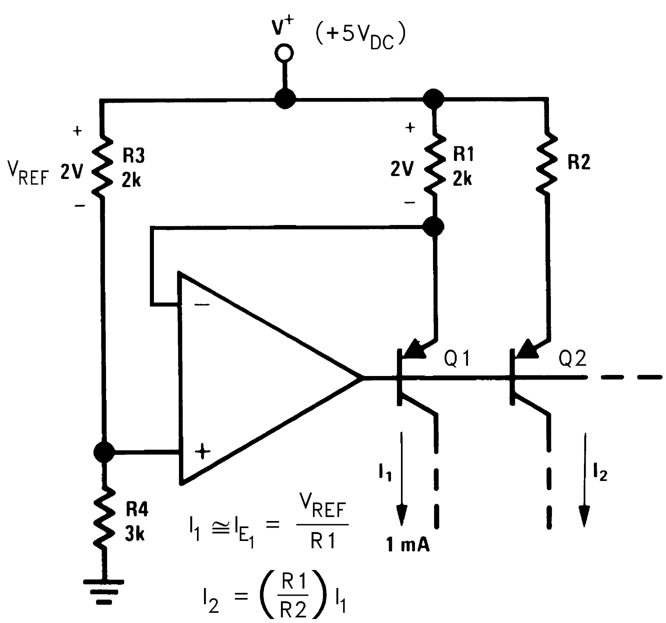


Figure 9-15. Fixed Current Source

9.2.8.2 High Compliance Current Sink

A current sink circuit is shown in Figure 9-16. The circuit requires only one resistor (R_E) and supplies an output current which is directly proportional to this resistor value.

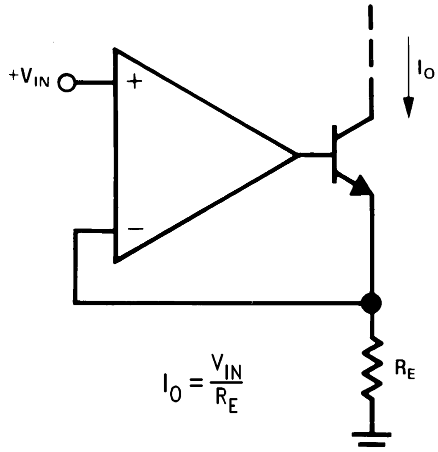


Figure 9-16. High Compliance Current Sink

9.2.9 Power Amplifier

A power amplifier is illustrated in Figure 9-17. This circuit can provide a higher output current because a transistor follower is added to the output of the op amp.

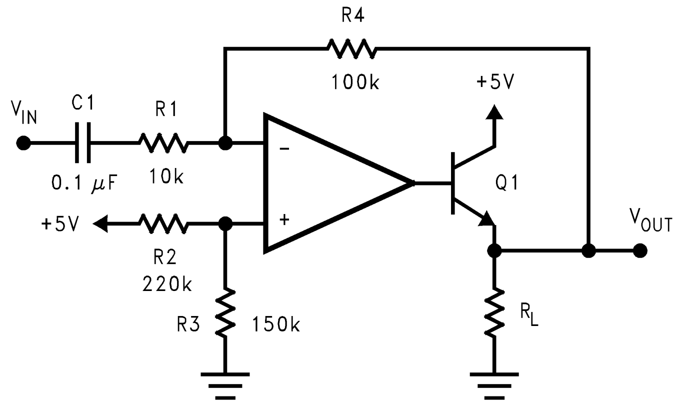


Figure 9-17. Power Amplifier

9.2.10 LED Driver

The LMV321-N/LMV358-N/LMV324-N can be used to drive an LED as shown in Figure 9-18.

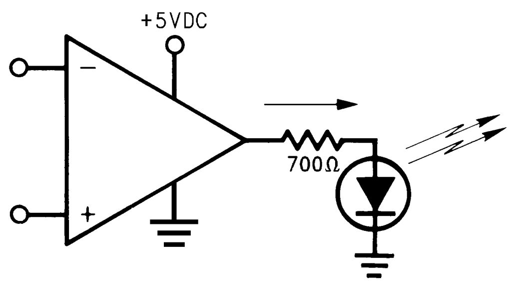


Figure 9-18. LED Driver

9.2.11 Comparator With Hysteresis

The LMV321-N/LMV358-N/LMV324-N can be used as a low power comparator. Figure 9-19 shows a comparator with hysteresis. The hysteresis is determined by the ratio of the two resistors.

$$V_{TH+} = V_{REF} / (1+R_1 / R_2) + V_{OH} / (1 + R_2 / R_1) \tag{30}$$

$$V_{TH-} = V_{REF} / (1 + R_1 / R_2) + V_{OL} / (1 + R_2 / R_1) \tag{31}$$

$$V_H = (V_{OH} - V_{OL}) / (1 + R_2 / R_1) \tag{32}$$

where

- V_{TH+}: Positive Threshold Voltage
- V_{TH-}: Negative Threshold Voltage
- V_{OH}: Output Voltage at High
- V_{OL}: Output Voltage at Low
- V_H: Hysteresis Voltage

Since LMV321-N/LMV358-N/LMV324-N have rail-to-rail output, the (V_{OH}–V_{OL}) is equal to V_S, which is the supply voltage.

$$V_H = V_S / (1 + R_2 / R_1) \tag{33}$$

The differential voltage at the input of the op amp should not exceed the specified absolute maximum ratings. For real comparators that are much faster, we recommend you use Texas Instruments' LMV331/LMV93/LMV339, which are single, dual and quad general purpose comparators for low voltage operation.

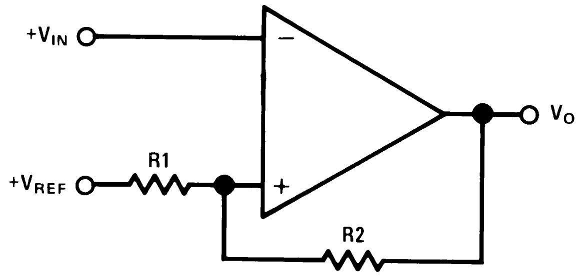


Figure 9-19. Comparator With Hysteresis

10 Power Supply Recommendations

The LMV3xx-N is specified for operation from 2.7 V to 5.5 V; many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in the *Layout Example* section.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

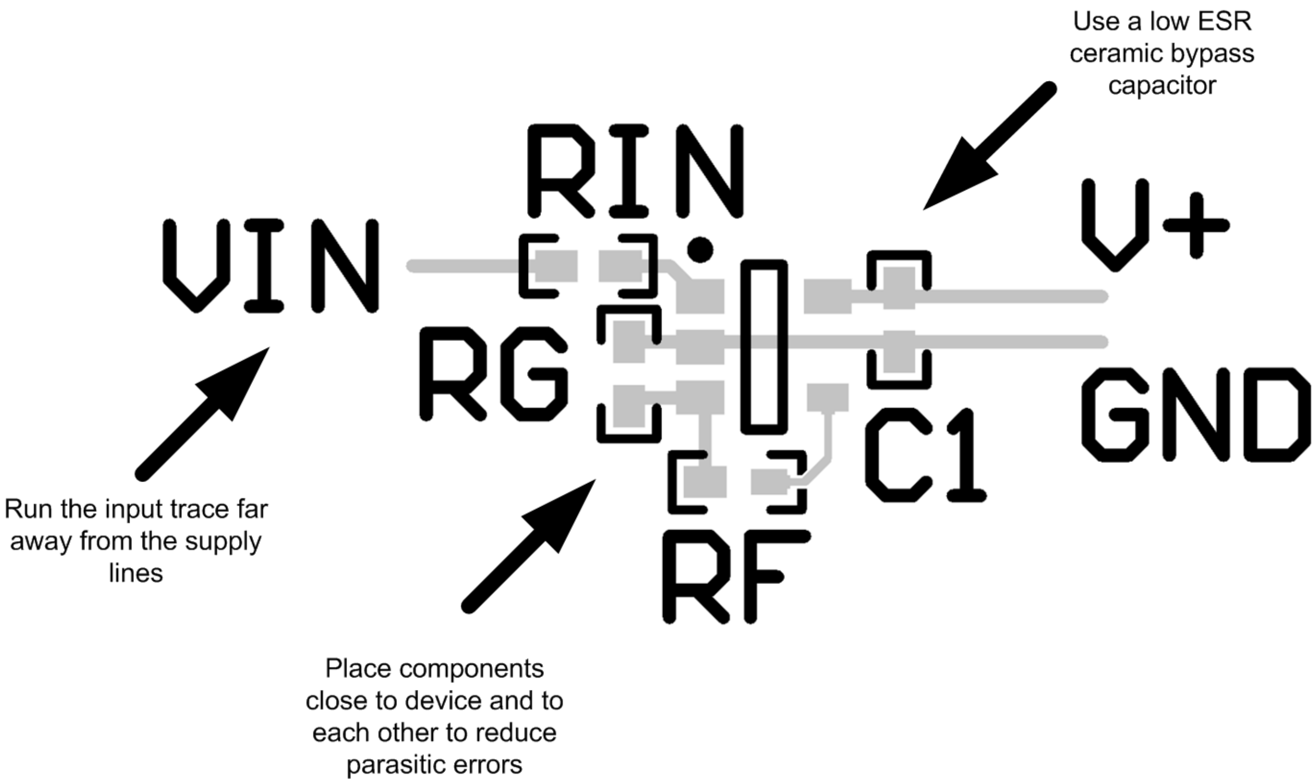


Figure 11-1. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV321-N	Click here	Click here	Click here	Click here	Click here
LMV321-N-Q1	Click here	Click here	Click here	Click here	Click here
LMV358-N	Click here	Click here	Click here	Click here	Click here
LMV358-N-Q1	Click here	Click here	Click here	Click here	Click here
LMV324-N	Click here	Click here	Click here	Click here	Click here
LMV324-N-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV321M5	LIFEBUY	SOT-23	DBV	5	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	A13	
LMV321M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A13	Samples
LMV321M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A13	Samples
LMV321M7/NOPB	ACTIVE	SC70	DCK	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A12	Samples
LMV321M7X	LIFEBUY	SC70	DCK	5	3000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 125	A12	
LMV321M7X/NOPB	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A12	Samples
LMV321Q1M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AYA	Samples
LMV321Q1M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AYA	Samples
LMV321Q3M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AZA	Samples
LMV321Q3M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AZA	Samples
LMV324M/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV324M	Samples
LMV324MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV324 MT	Samples
LMV324MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LMV324 MT	Samples
LMV324MX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV324M	Samples
LMV324Q1MA/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV324Q1 MA	Samples
LMV324Q1MAX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LMV324Q1 MA	Samples
LMV324Q1MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV324 Q1MT	Samples
LMV324Q1MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV324 Q1MT	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV324Q3MA/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LMV324Q3 MA	Samples
LMV324Q3MAX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LMV324Q3 MA	Samples
LMV324Q3MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV324 Q3MT	Samples
LMV324Q3MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV324 Q3MT	Samples
LMV358M	LIFEBUY	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 125	LMV 358M	
LMV358M/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV 358M	Samples
LMV358MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	V358	Samples
LMV358MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	V358	Samples
LMV358MX	LIFEBUY	SOIC	D	8	2500	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 125	LMV 358M	
LMV358MX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV 358M	Samples
LMV358Q1MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV35 8Q1MA	Samples
LMV358Q1MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMV35 8Q1MA	Samples
LMV358Q1MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AFAA	Samples
LMV358Q1MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AFAA	Samples
LMV358Q3MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV35 8Q3MA	Samples
LMV358Q3MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMV35 8Q3MA	Samples
LMV358Q3MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AHAA	Samples
LMV358Q3MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AHAA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV321-N, LMV321-N-Q1, LMV324-N, LMV324-N-Q1, LMV358-N, LMV358-N-Q1 :

- Catalog : LMV321-N, LMV324-N, LMV358-N

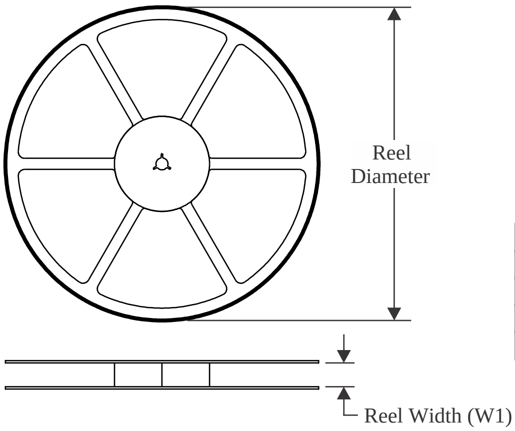
- Automotive : LMV321-N-Q1, LMV324-N-Q1, LMV358-N-Q1

NOTE: Qualified Version Definitions:

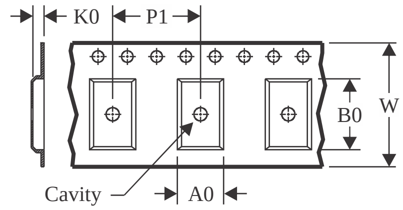
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

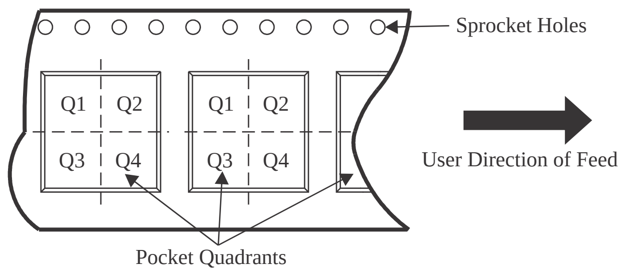


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

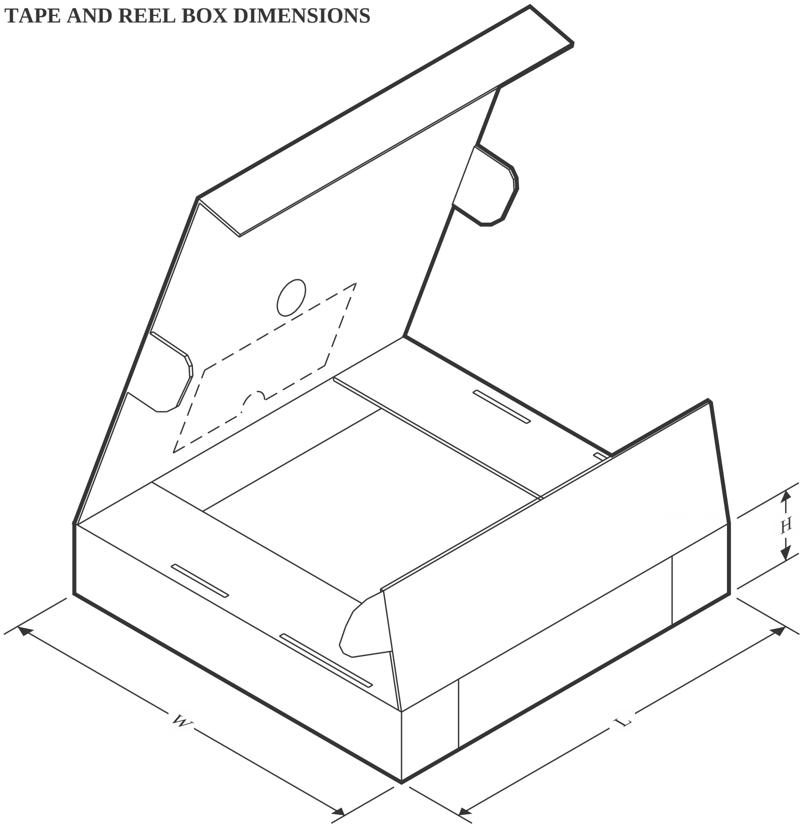


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV321M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV321M7X	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV321M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV321Q1M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321Q1M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321Q3M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321Q3M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV324MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV324Q1MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV324Q1MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV324Q3MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV324Q3MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV358MM/NOPB	VSSOP	DGK	8	1000	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV358MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV358MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV358Q1MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV358Q1MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358Q1MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358Q3MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV358Q3MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358Q3MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

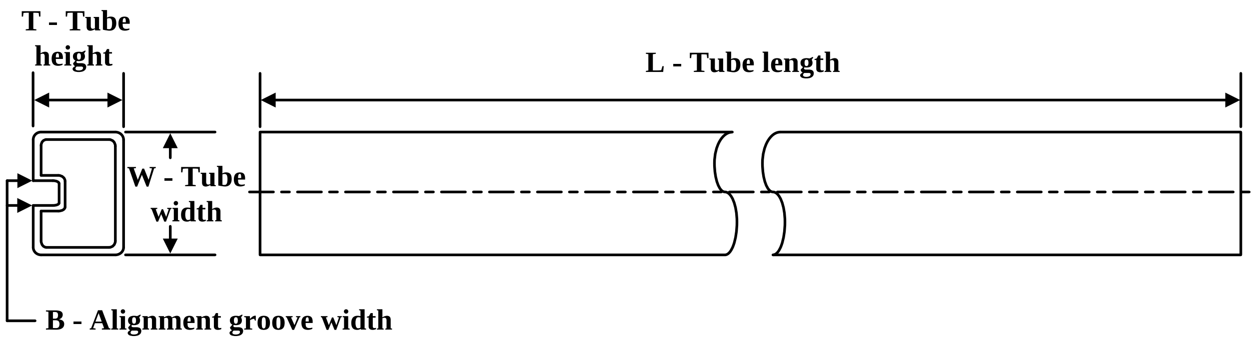


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV321M5	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV321M5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV321M5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV321M7/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0
LMV321M7X	SC70	DCK	5	3000	208.0	191.0	35.0
LMV321M7X/NOPB	SC70	DCK	5	3000	208.0	191.0	35.0
LMV321Q1M5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV321Q1M5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV321Q3M5/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV321Q3M5X/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV324MX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LMV324Q1MAX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LMV324Q1MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV324Q3MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV324Q3MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV358MM/NOPB	VSSOP	DGK	8	1000	366.0	364.0	50.0
LMV358MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV358MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV358MMX/NOPB	VSSOP	DGK	8	3500	366.0	364.0	50.0
LMV358MX	SOIC	D	8	2500	367.0	367.0	35.0
LMV358MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV358Q1MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV358Q1MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV358Q1MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV358Q3MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV358Q3MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV358Q3MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

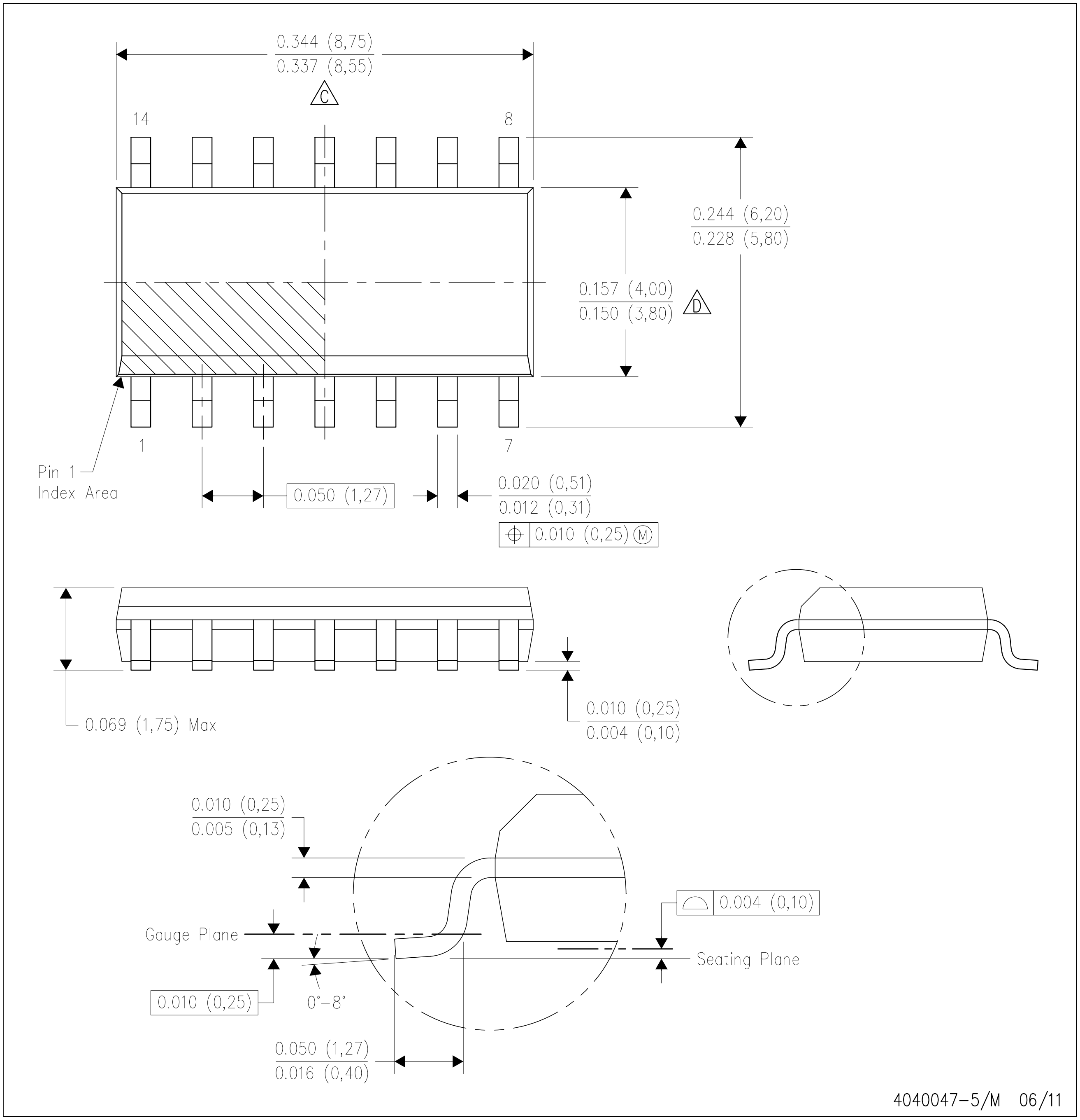
TUBE



*All dimensions are nominal

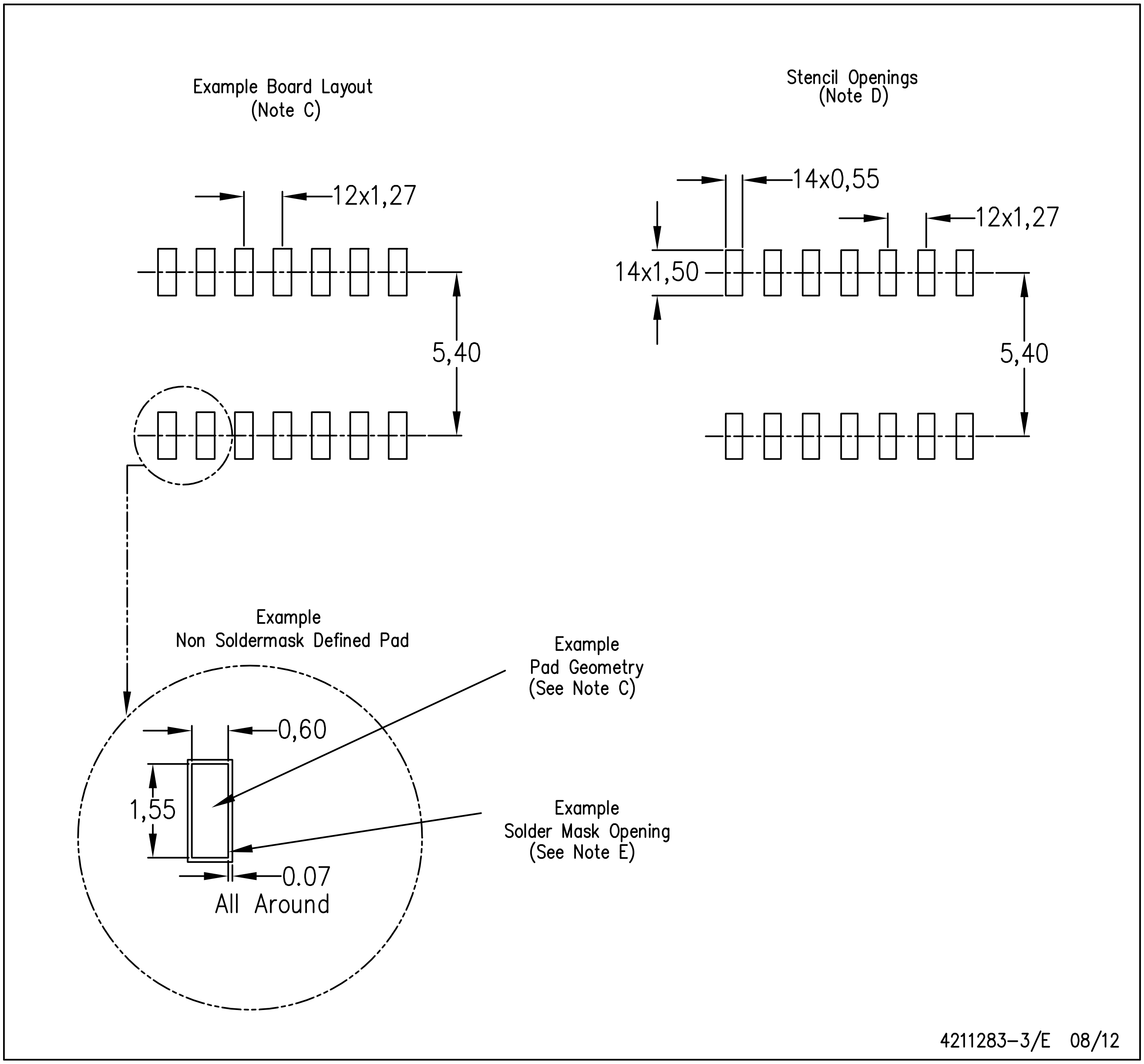
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV324M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMV324MT/NOPB	PW	TSSOP	14	94	530	10.2	3600	3.5
LMV324MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LMV324Q1MA/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMV324Q1MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LMV324Q3MA/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMV324Q3MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LMV358M	D	SOIC	8	95	495	8	4064	3.05
LMV358M	D	SOIC	8	95	495	8	4064	3.05
LMV358M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMV358Q1MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMV358Q3MA/NOPB	D	SOIC	8	95	495	8	4064	3.05

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



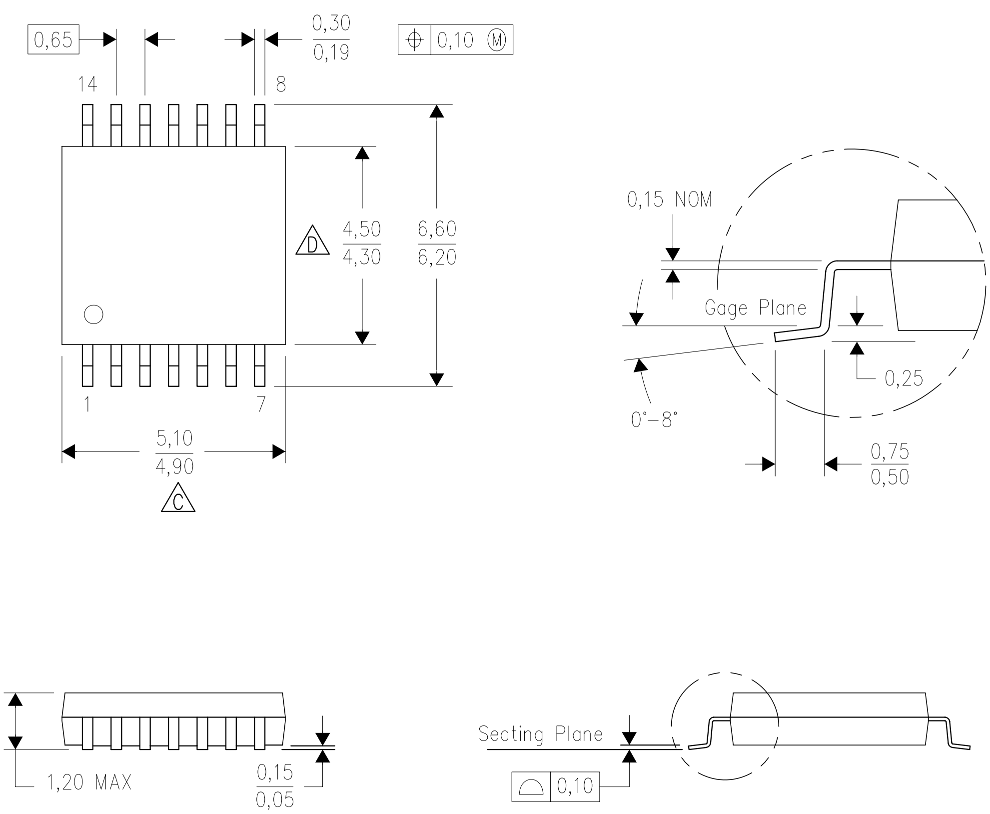
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE

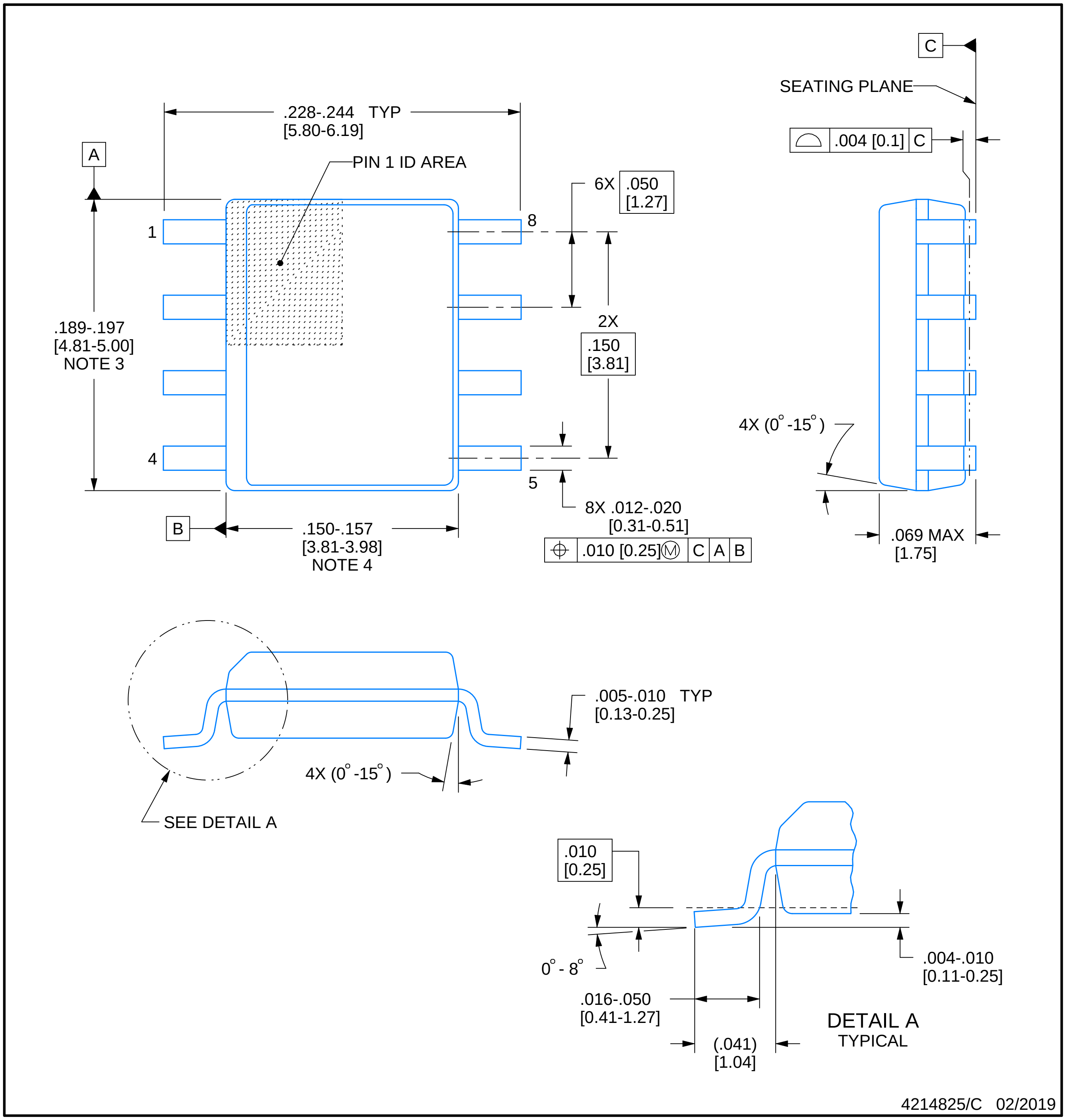


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE

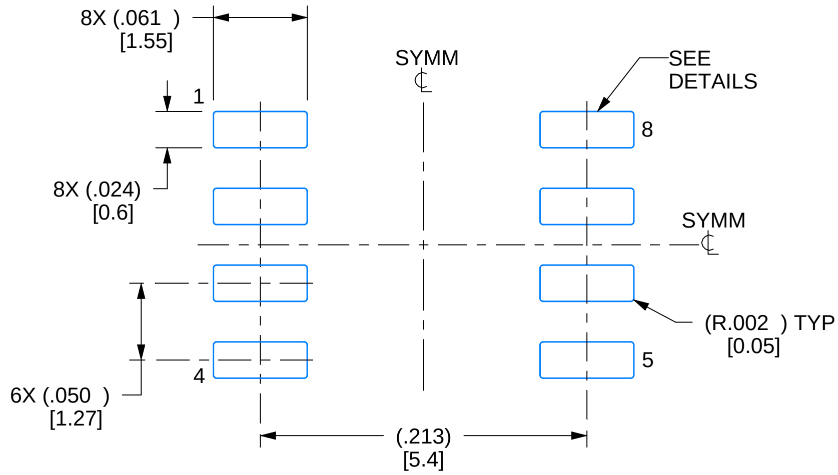


NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

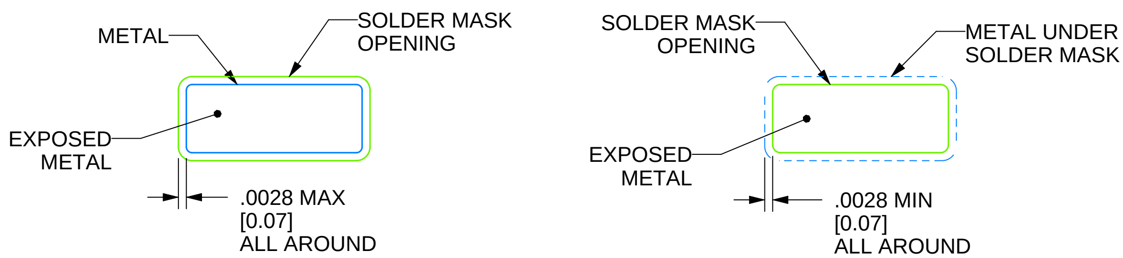


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

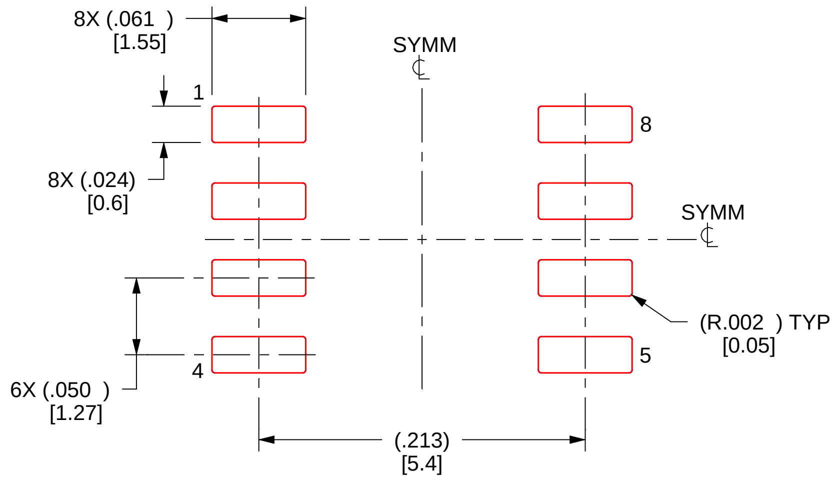
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

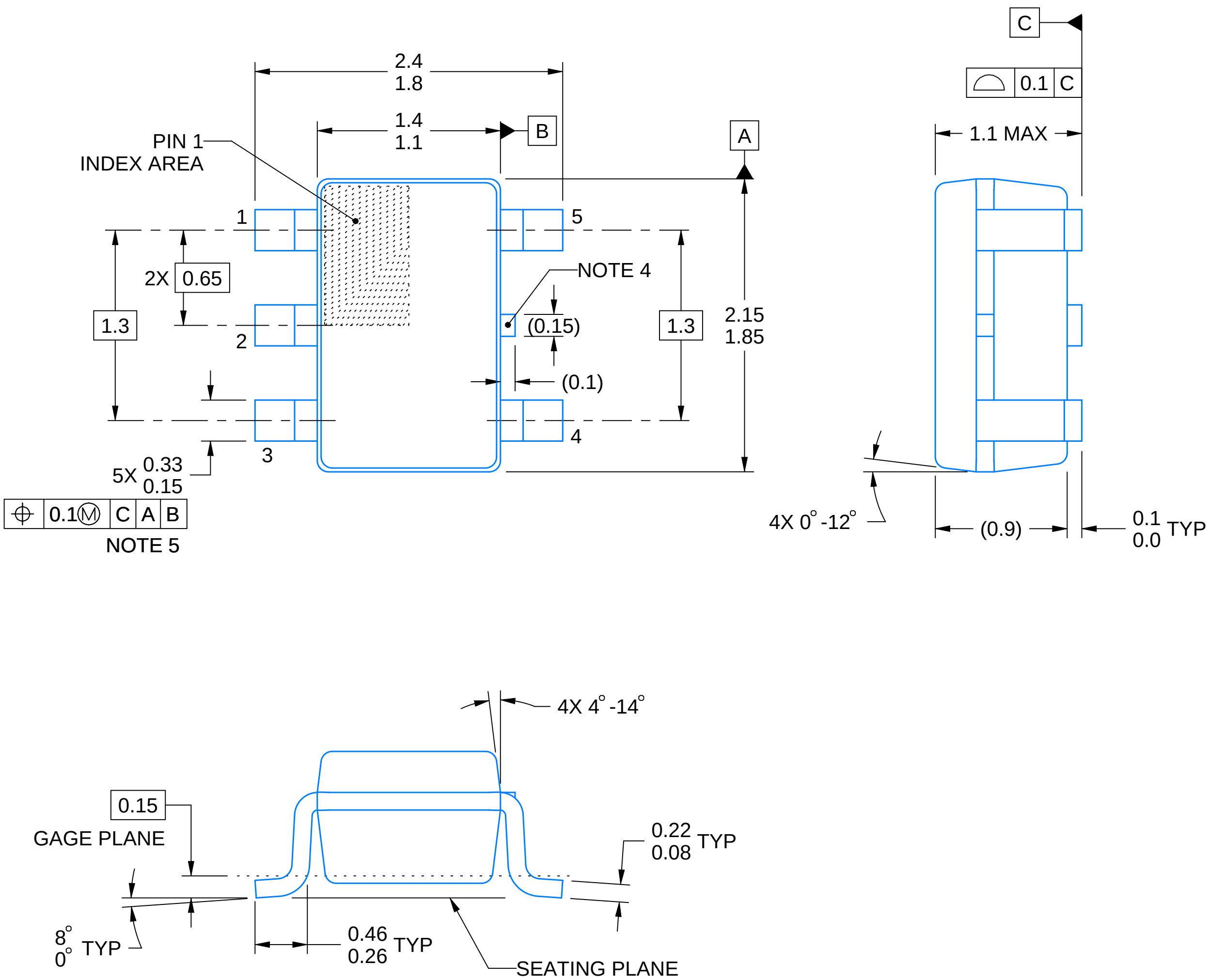


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

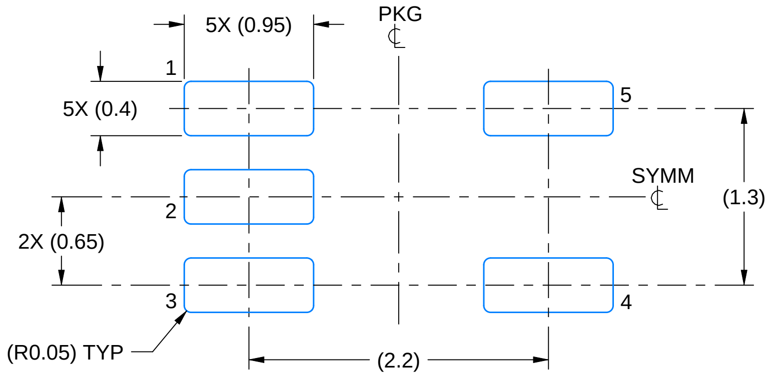
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



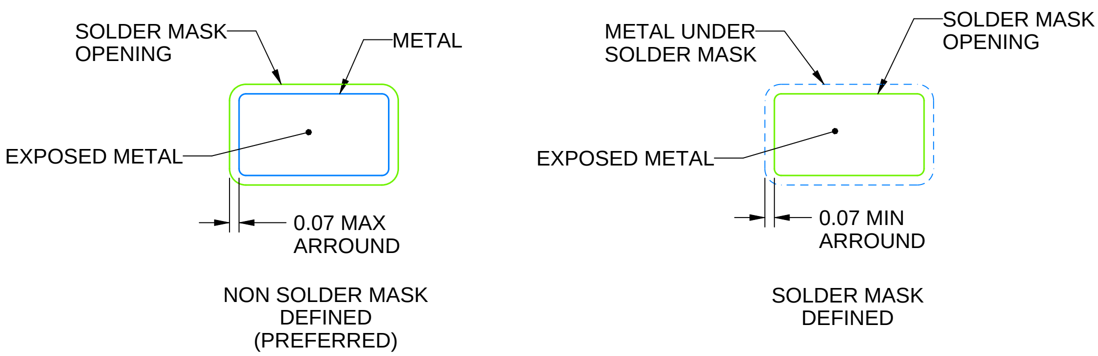
4214834/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

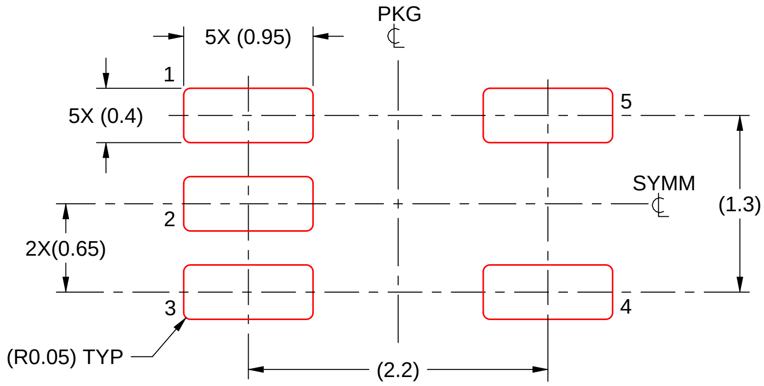


SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

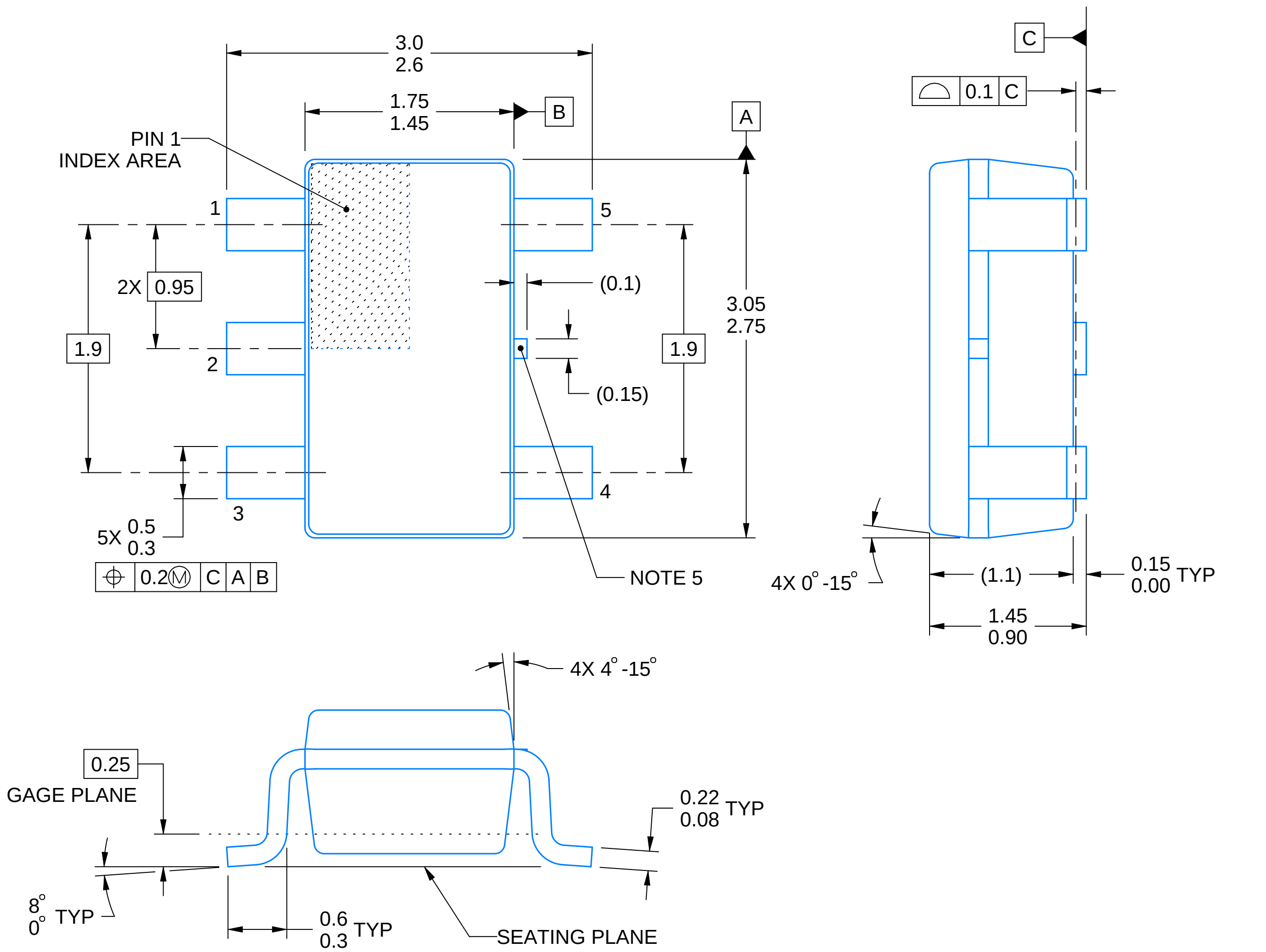


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/F 08/2024

NOTES: (continued)

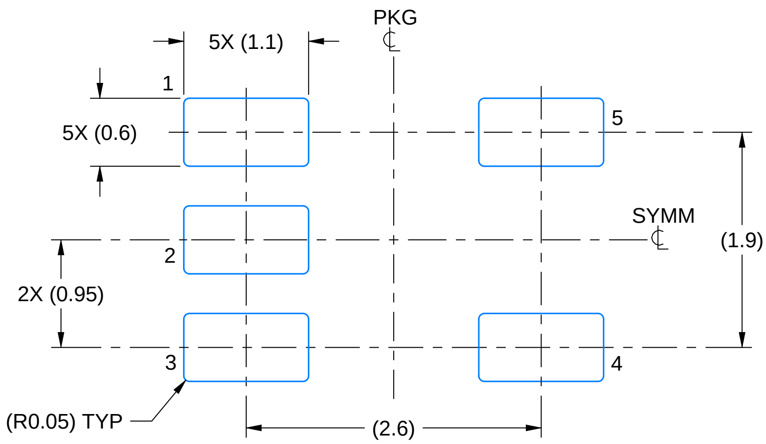
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.



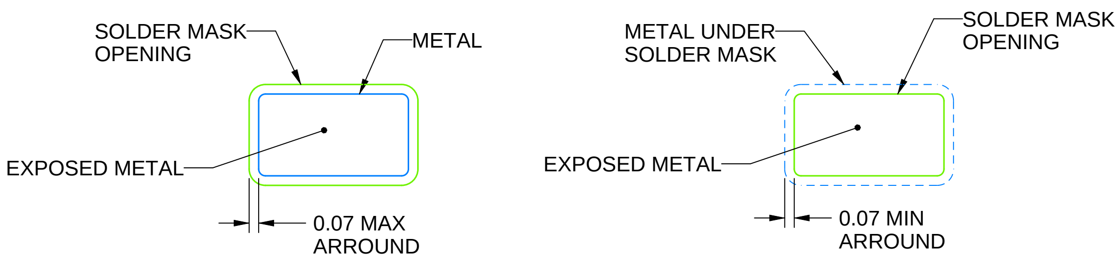
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

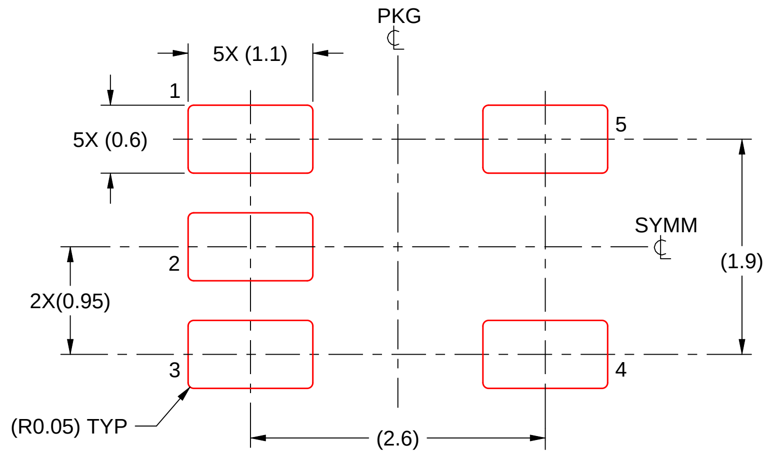
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

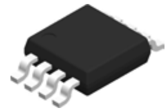


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

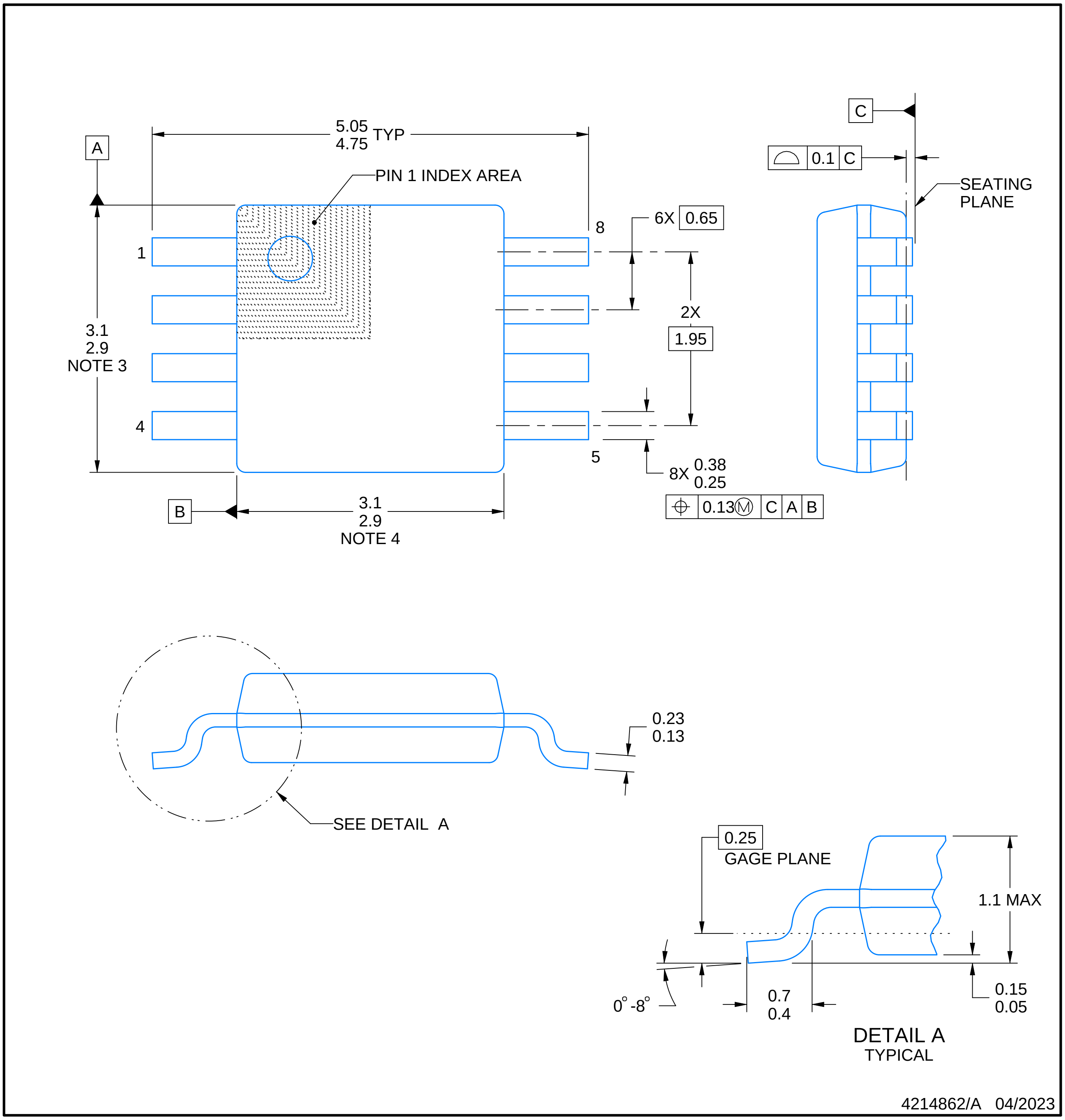
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

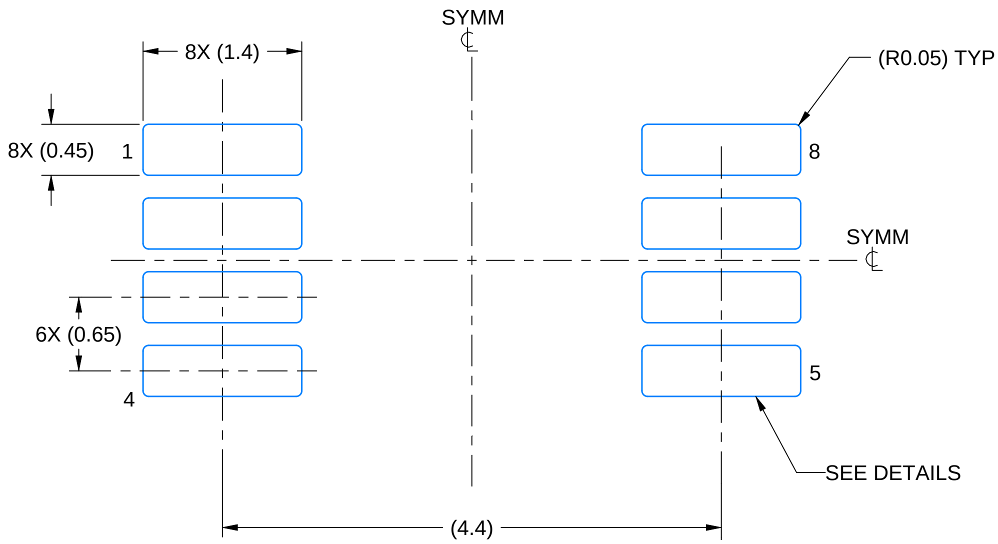
SMALL OUTLINE PACKAGE



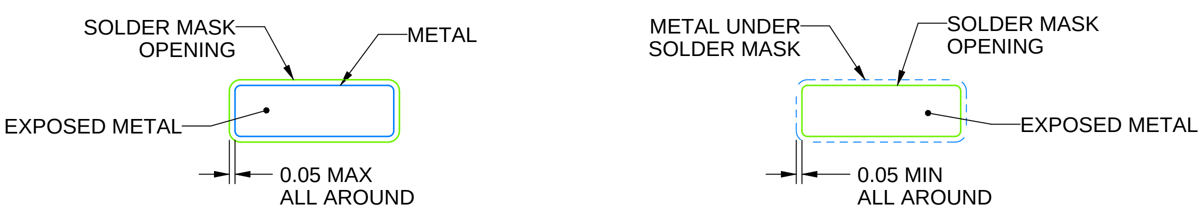
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

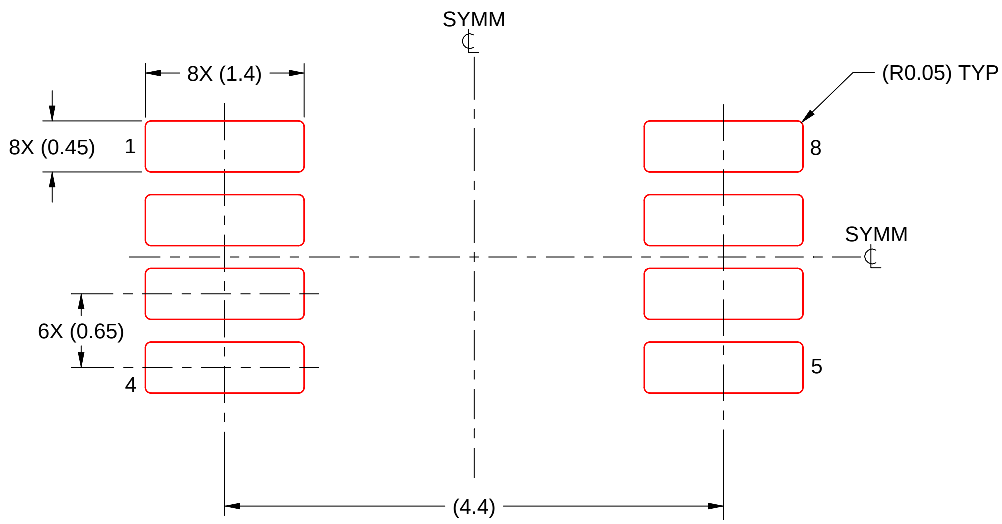
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.