LP324-N/LP2902-N Micropower Quad Operational Amplifier

Check for Samples: LP2902-N, LP324-N

FEATURES

- **Low Supply Current: 85µA (typ)**
- **Low Offset Voltage: 2mV (typ)**
- **Low Input Bias Current: 2nA (typ)**
- **Input Vommon Mode to GND**
- **Interfaces to CMOS Logic**
- **Wide Supply Range: 3V < V^+ < 32V**
- **Small Outline Package Available**
- **Pin-for-pin Compatible with LM324**

DESCRIPTION

The LP324-N series consists of four independent, high gain internally compensated micropower operational amplifiers. These amplifiers are specially suited for operation in battery systems while maintaining good input specifications, and extremely low supply current drain. In addition, the LP324-N has an input common mode range, and output source range which includes ground, making it ideal in single supply applications.

These amplifiers are ideal in applications which include portable instrumentation, battery backup equipment, and other circuits which require good DC performance and low supply current.

Connection Diagram

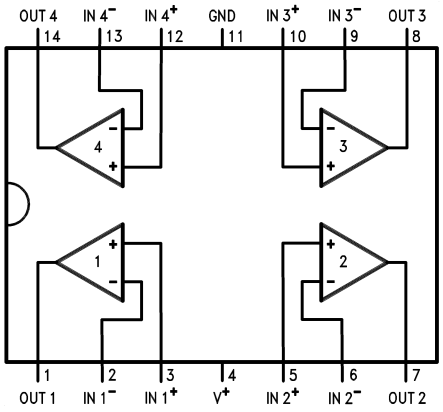


Figure 1. 14-Lead SOIC
See NFF0014A or D Package

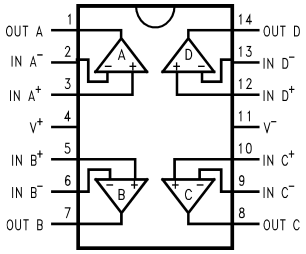
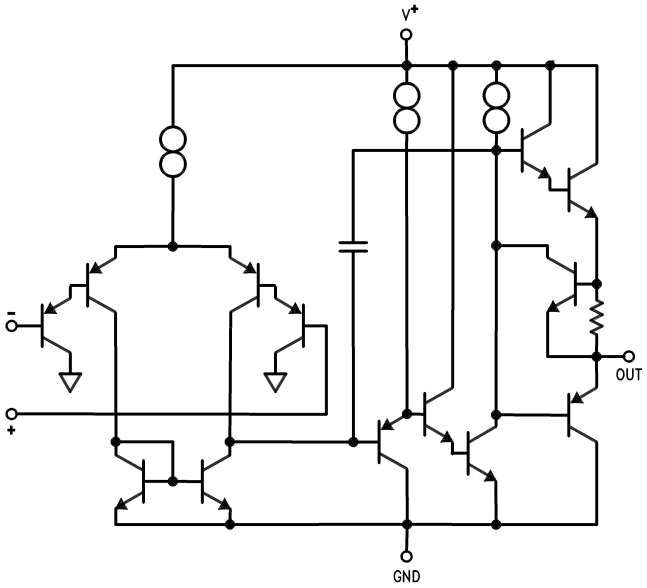


Figure 2. 14-Pin TSSOP
See PW Package

Simplified Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Supply Voltage	LP324-N	32V or ± 16V
	LP2902-N	26V or ± 13V
Differential Input Voltage	LP324-N	32V
	LP2902-N	26V
Input Voltage (3)	LP324-N	−0.3V to 32V
	LP2902-N	−0.3V to 26V
Output Short-Circuit to GND (One Amplifier) (4)		Continuous
$V^+ \le 15V$ and $T_A = 25°C$	ESD Susceptibility (5)	±500V

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The input voltage is not allowed to go more than −0.3V below V^- (GND) as this will turn on a parasitic transistor causing large currents to flow through the device.
(4) Short circuits from the output to GND can cause excessive heating and eventual destruction. The maximum sourcing output current is approximately 30 mA independent of the magnitude of V^+. At values of supply voltage in excess of 15 V_{DC}, continuous short-circuit to GND can exceed the power dissipation ratings (particularly at elevated temperatures) and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
(5) The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Operating Conditions

T_{JMAX}		150°C
θ_{JA} (1)	PW Package	154°C/W
	NFF014A Package	90°C/W
	D Package	140°C/W
Operating Temp. Range		See (2)
Storage Temp. Range		−65°C≤T_J≤ 150°C
Soldering Information	Wave Soldering(10sec)	260°C(lead temp.)
	Convection or Infrared(20sec)	235°C

(1) For operation at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{JA} and T_J max. $T_J = T_A + \theta_{JA}P_D$.
(2) The LP2902-N may be operated from −40°C ≤ T_A ≤ +85°C, and the LP324-N may be operated from 0°C ≤ T_A ≤ +70°C.

Electrical Characteristics (1)

Symbol	Parameter	Conditions	LP2902-N (2)			LP324-N			
			Typ	Tested Limit (3)	Design Limit (4)	Typ	Tested Limit (3)	Design Limit (4)	Units Limits
V_{OS}	Input Offset Voltage		2	4	**10**	2	4	**9**	mV (Max)
I_B	Input Bias Current		2	20	**40**	2	10	**20**	nA (Max)
I_{OS}	Input Offset Current		0.5	4	**8**	0.2	2	**4**	nA (Max)
A_{VOL}	Voltage Gain	R_L = 10k to GND V^+ = 30V	70	40	**30**	100	50	**40**	V/mV (Min)
CMRR	Common Mode Rej. Ratio	V^+ = 30V, 0V ≤ V_{CM} V_{CM} < V^+− 1.5	90	80	**75**	90	80	**75**	dB (Min)
PSRR	Power Supply Rej. Ratio	V^+ = 5V to 30V	90	80	**75**	90	80	**75**	dB (Min)
I_S	Supply Current	R_L = ∞	85	150	**250**	85	150	**250**	µA (Max)
V_O	Output Voltage Swing	I_L = 350µA to GND V_{CM} = 0V	3.6	3.4	**V^+−1.9V**	3.6	3.4	**V^+−1.9V**	V (Min)
		I_L = 350µA to V^+ V_{CM} = 0V	0.7	0.8	**1.0**	0.7	0.8	**1.0**	V (Max)
I_{OUT} Source	Output Source Current	V_O = 3V V_{IN} (diff) = 1V	10	7	**4**	10	7	**4**	mA (Min)
I_{OUT} Sink	Output Sink Current	V_O = 1.5V V_{IN} (diff) = 1V	5	4	**3**	5	4	**3**	mA (Min)
I_{OUT} Sink	Output Sink Current	V_O = 1.5V V_{CM} = 0V	4	2	**1**	4	2	**1**	mA (Min)
I_{SOURCE}	Output Short to GND	V_{IN} (diff) = 1V	20	25 **35**	**35**	20	25 **35**	**35**	mA (Max)
I_{SINK}	Output Short to V^+	V_{IN} (diff) = 1V	15	30	**45**	15	30	**45**	mA (Max)
V_{OS} Drift			10			10			µV/C°
I_{OS} Drift			10			10			pA/C°
GBW	Gain Bandwidth Product		100			100			KHz
SR	Slew Rate		50			50			V/mS

(1) **Boldface** numbers apply at temperature extremes. All other numbers apply only at $T_A = T_J$ = 25°C, V^+ = 5V, V_{cm} = V/2, and R_L =100k connected to GND unless otherwise specified.
(2) The LP2902-N operating supply range is 3V to 26V, and is not tested above 26V.
(3) Specified and 100% production tested.
(4) Specified (but not 100% production tested) over the operating supply voltage range (3.0V to 32V for the LP324-N, LP324-N, and 3.0V to 26V for the LP2902-N), and the common mode range (0V to V^+ −1.5V), unless otherwise specified. These limits are not used to calculate outgoing quality levels.

Typical Performance Curves

Input Voltage Range

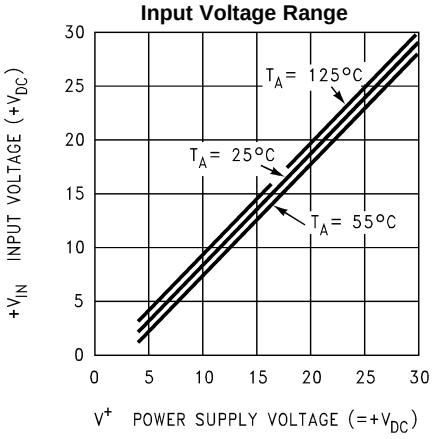


Figure 3.

Input Current

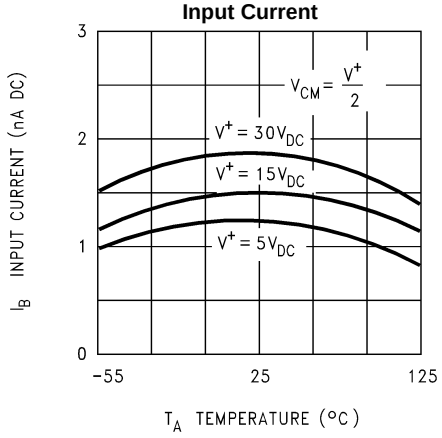


Figure 4.

Supply Current

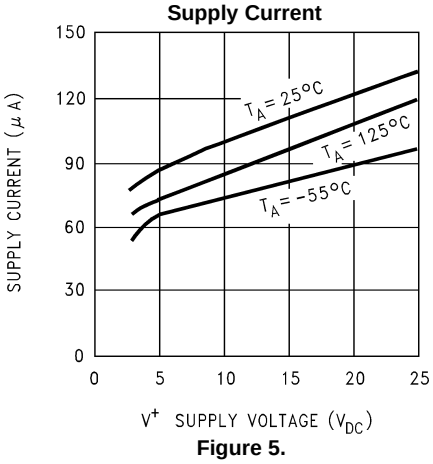


Figure 5.

Voltage Gain

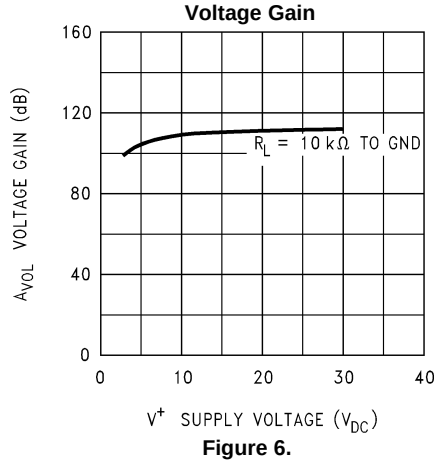


Figure 6.

Open Loop Frequency Response

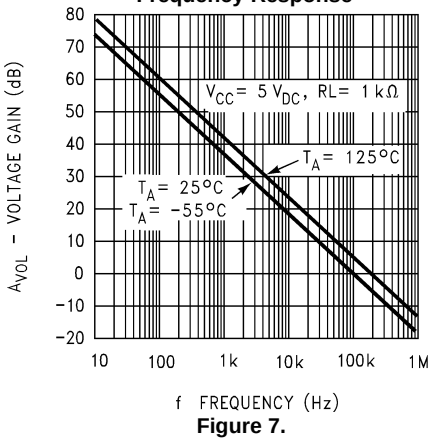


Figure 7.

Power Supply Rejection Ratio

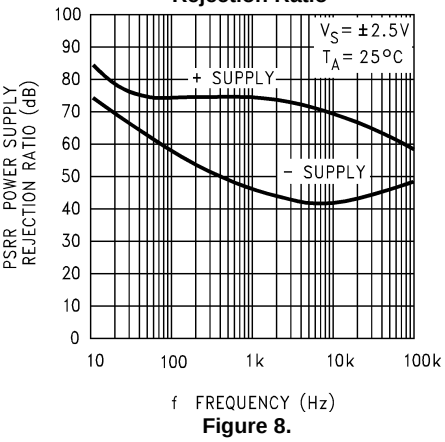


Figure 8.

Typical Performance Curves (continued)

Voltage Follower Pulse Response

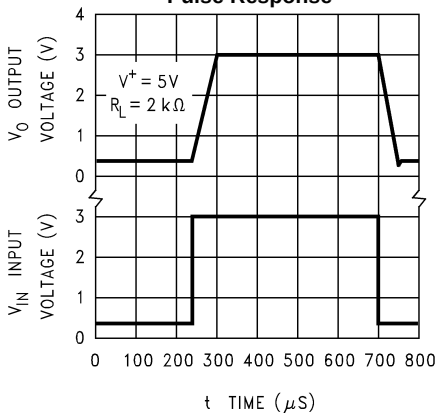


Figure 9.

Voltage Follower Pulse Response (Small Signal)

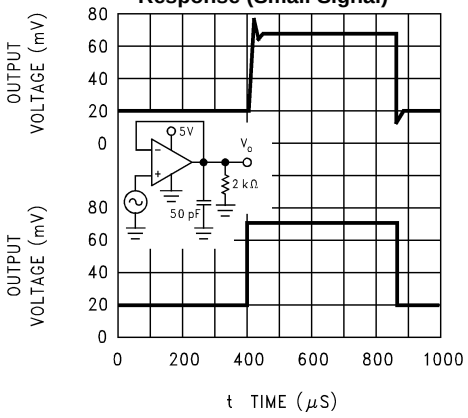


Figure 10.

Common Mode Rejection Ratio

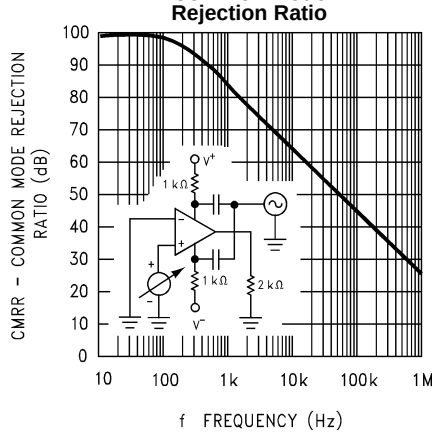


Figure 11.

Large Signal Frequency Response

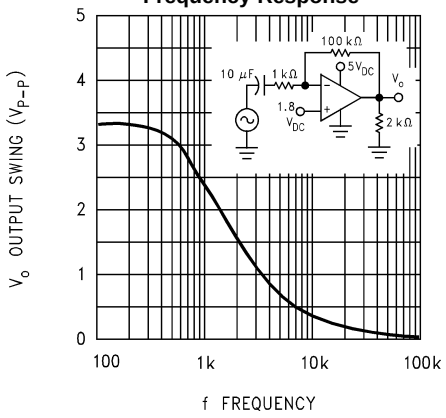


Figure 12.

Output Characteristics Current Sourcing

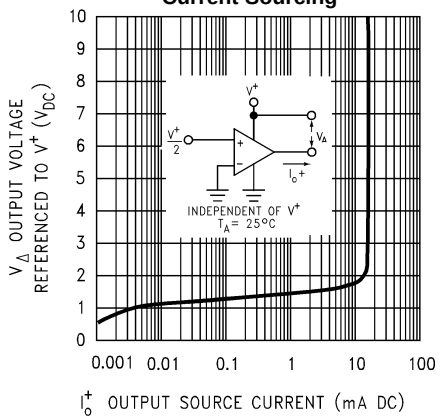


Figure 13.

Output Characteristics Current Sinking

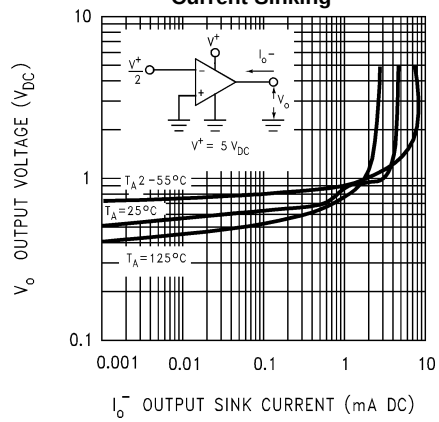


Figure 14.

Typical Performance Curves (continued)

Current Limiting

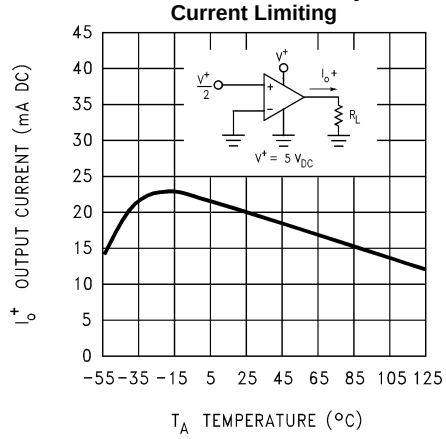


Figure 15.

APPLICATION HINTS

The LP324-N series is a micro-power pin-for-pin equivalent to the LM324 op amps. Power supply current, input bias current, and input offset current have all been reduced by a factor of 10 over the LM324. Like its predecessor, the LP324-N series op amps can operate on single supply, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or the unit is not inadvertently installed backwards in the test socket as an unlimited current surge through the resulting forward diode within the IC could destroy the unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

The amplifiers have a class B output stage which allows the amplifiers to both source and sink output currents. In applications where crossover distortion is undesirable, a resistor should be used from the output of the amplifier to ground. The resistor biases the output into class A operation.

The LP324-N has improved stability margin for driving capacitive loads. No special precautions are needed to drive loads in the 50 pF to 1000 pF range. It should be noted however that since the power supply current has been reduced by a factor of 10, so also has the slew rate and gain bandwidth product. This reduction can cause reduced performance in AC applications where the LM324 is being replaced by an LP324-N. Such situations usually occur when the LM324 has been operated near its power bandwidth.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. For example: If all four amplifiers were simultaneously shorted to ground on a 10V supply the junction temperature would rise by 110°C.

Exceeding the negative common-mode limit on either input will cause a reversal of phase to the output and force the amplifier to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a low state. In neither case does a latch occur since returning the input within the common mode range puts the input stage and thus the amplifier in a normal operating mode.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference to $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Figure 16. Driving CMOS

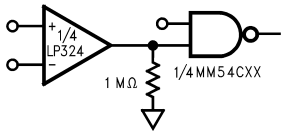


Figure 17. Comparator with Hysteresis

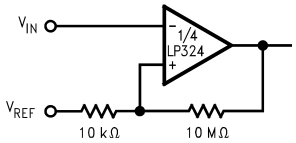


Figure 18. Non-Inverting Amplifier

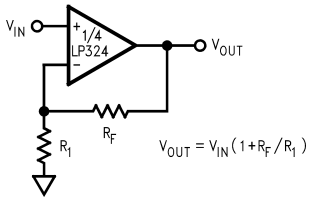


Figure 19. Adder/Subtractor

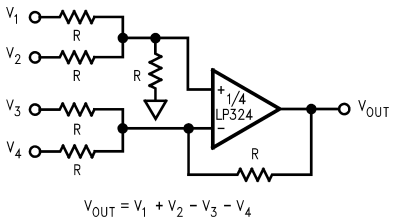


Figure 20. Unity Gain Buffer

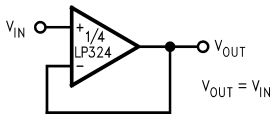


Figure 21. Positive Integrator

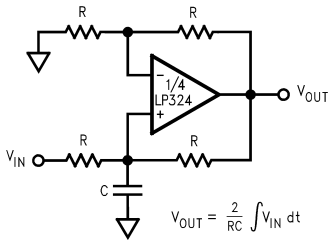


Figure 22. Differential Integrator

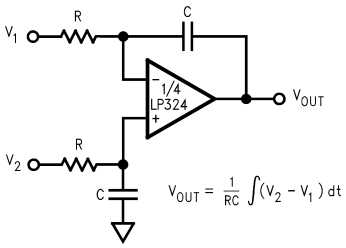


Figure 23. Howland Current Pump

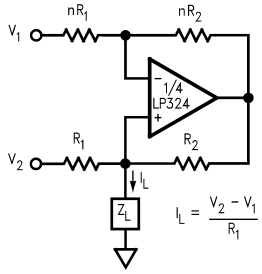


Figure 24. Bridge Current Amplifier

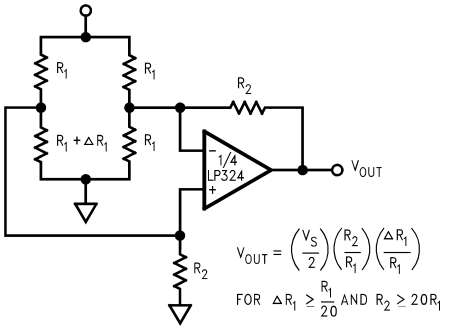


Figure 25. µ Power Current Source

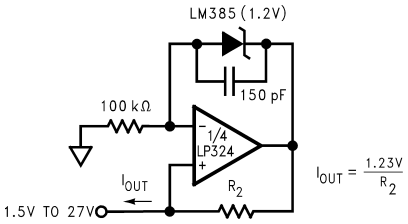


Figure 26. Lowpass Filter

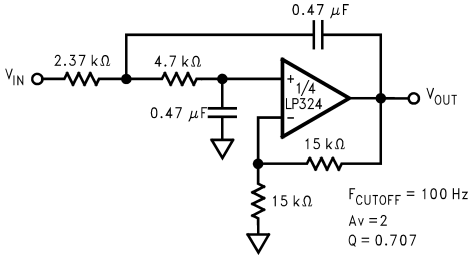


Figure 27. 1 kHz Bandpass Active Filter

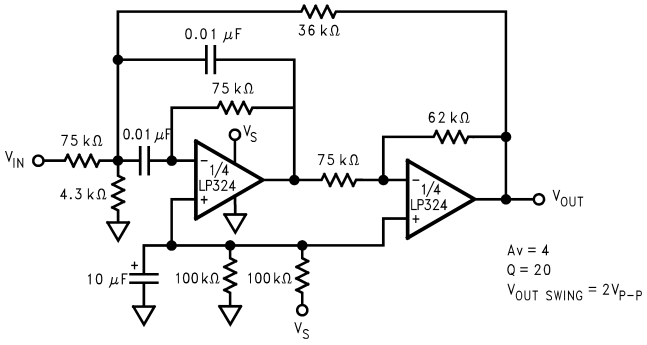


Figure 28. Band-Reject Filter

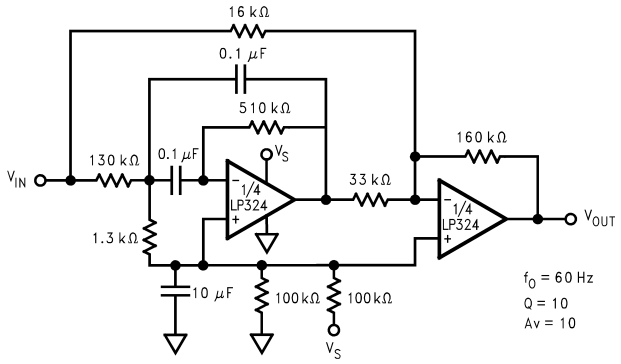


Figure 29. Pulse Generator

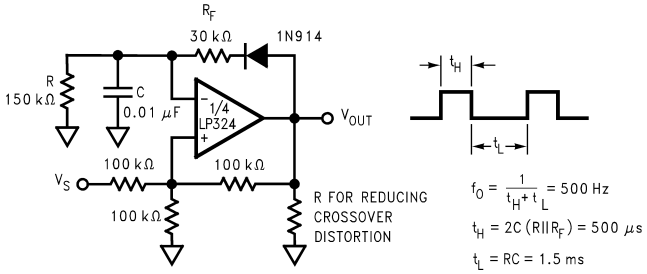
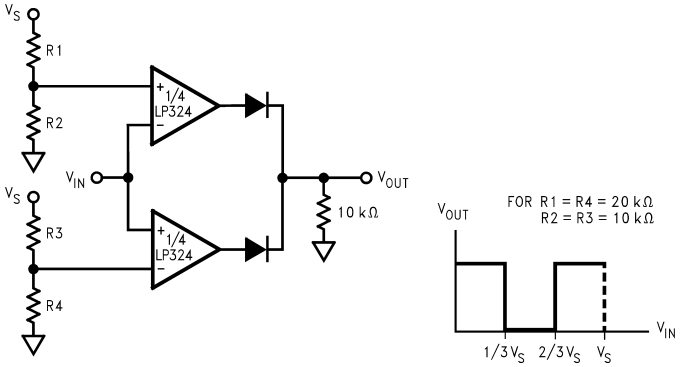


Figure 30. Window Comparator



REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2902M/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LP2902M	Samples
LP2902MX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LP2902M	Samples
LP2902N/NOPB	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LP2902N	Samples
LP324M/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LP324M	Samples
LP324MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LP324 MT	Samples
LP324MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LP324 MT	Samples
LP324MX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LP324M	Samples
LP324N/NOPB	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	Level-1-NA-UNLIM	0 to 70	LP324N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

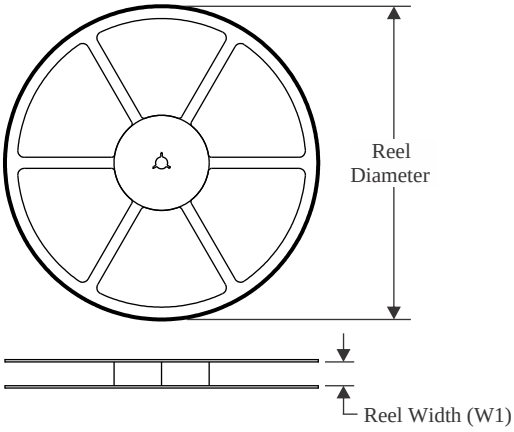
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

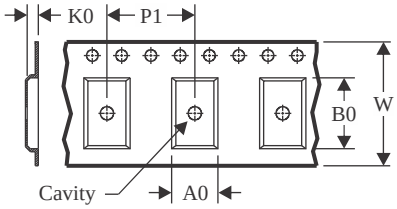
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

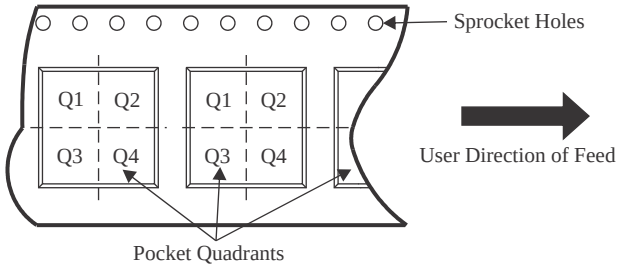


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

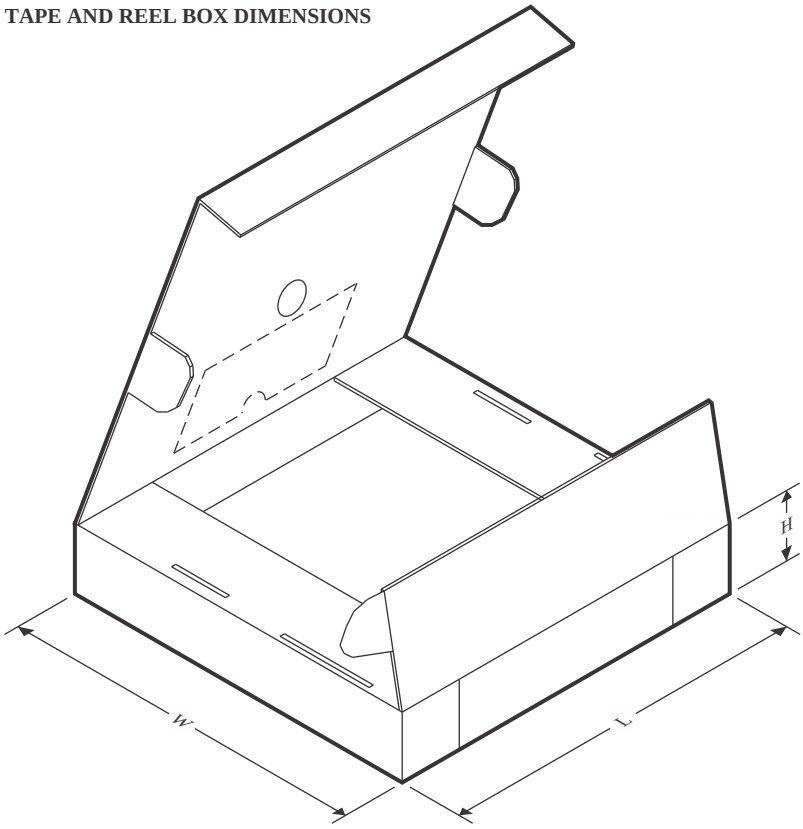
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2902MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LP324MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LP324MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

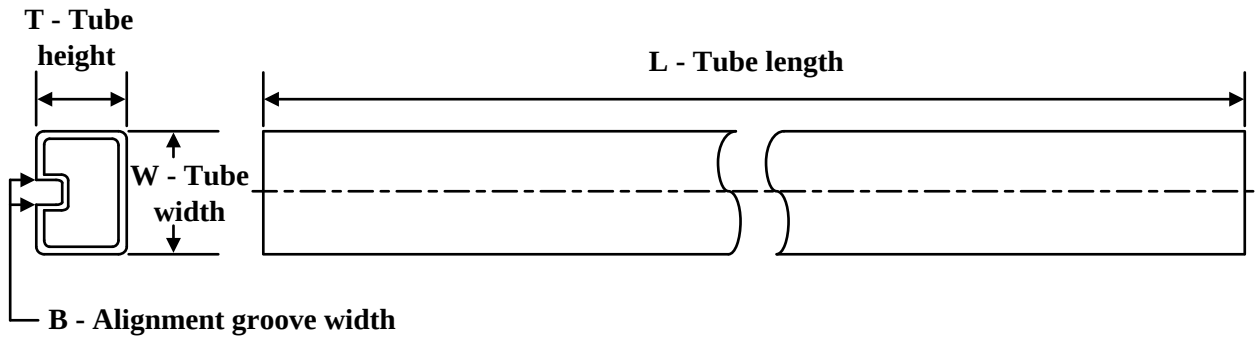
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

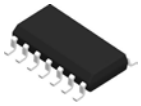
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2902MX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LP324MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LP324MX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP2902M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LP2902N/NOPB	N	PDIP	14	25	502	14	11938	4.32
LP324M/NOPB	D	SOIC	14	55	495	8	4064	3.05
LP324MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06
LP324N/NOPB	N	PDIP	14	25	502	14	11938	4.32

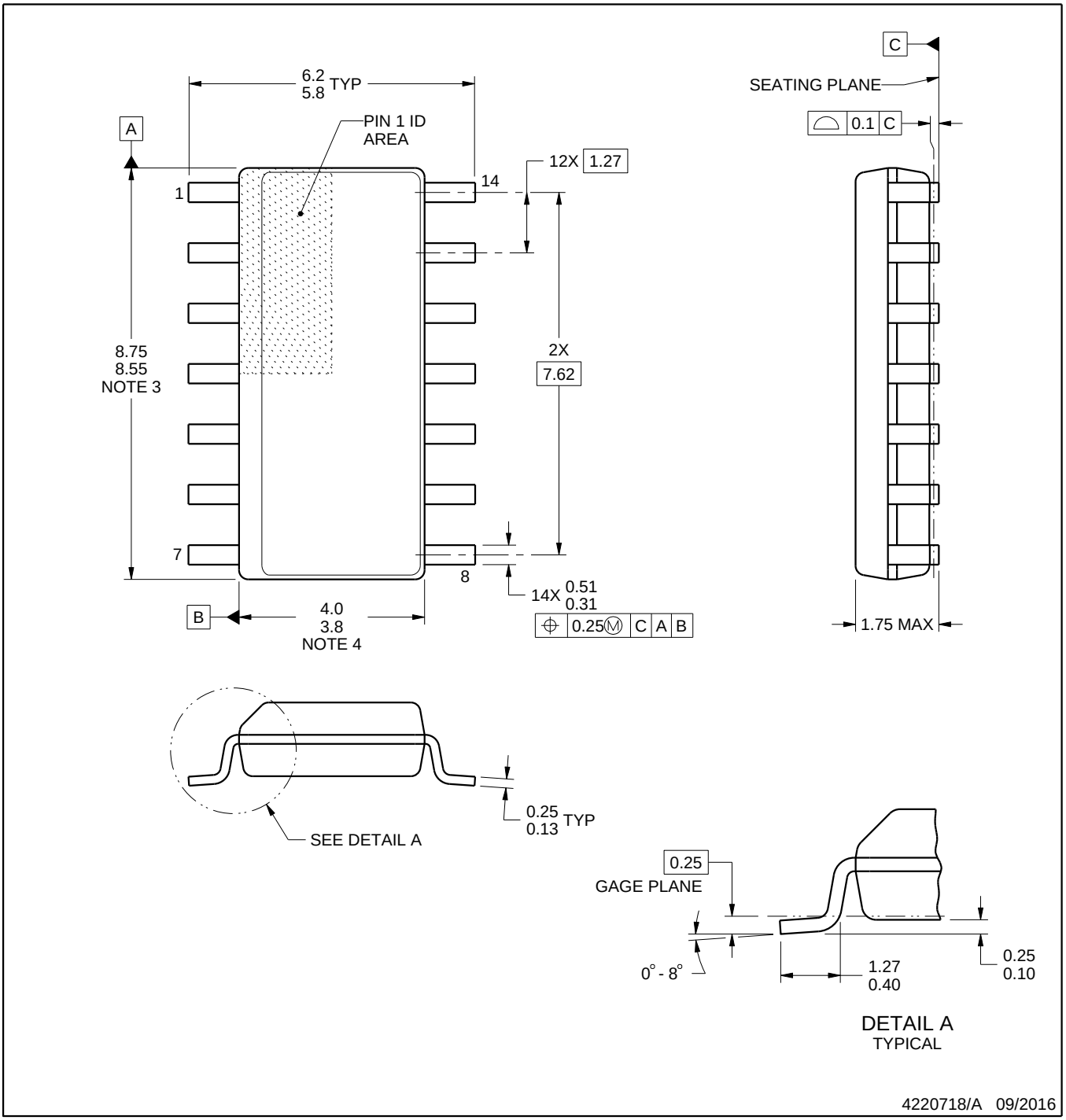


PACKAGE OUTLINE

D0014A

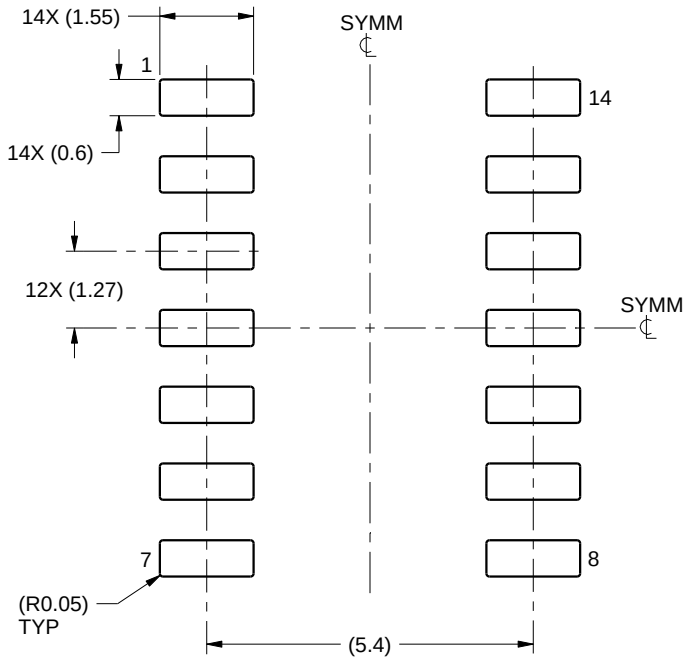
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

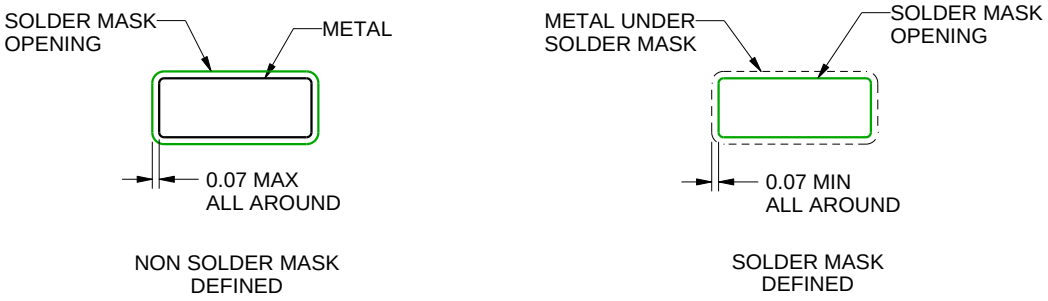


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

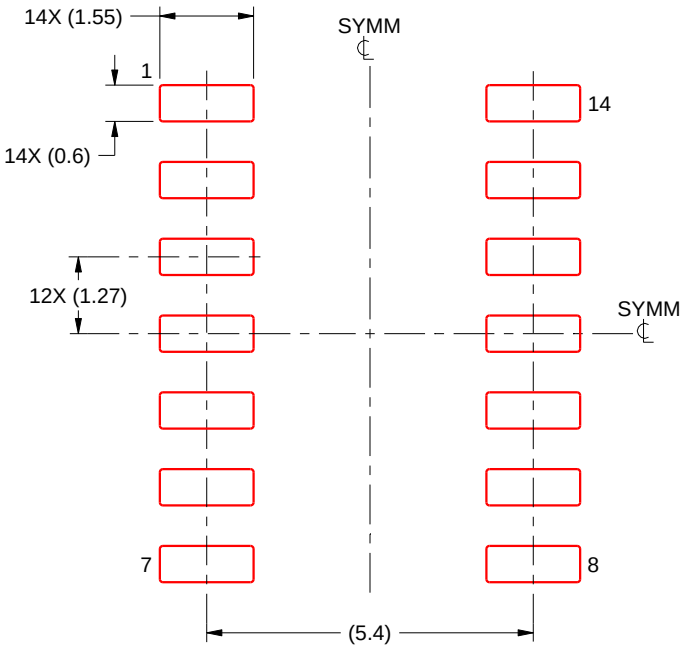
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

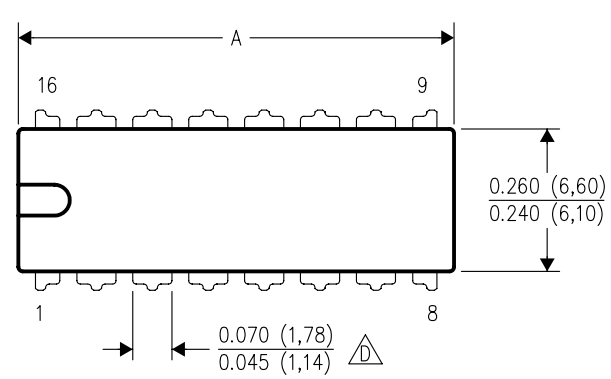
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

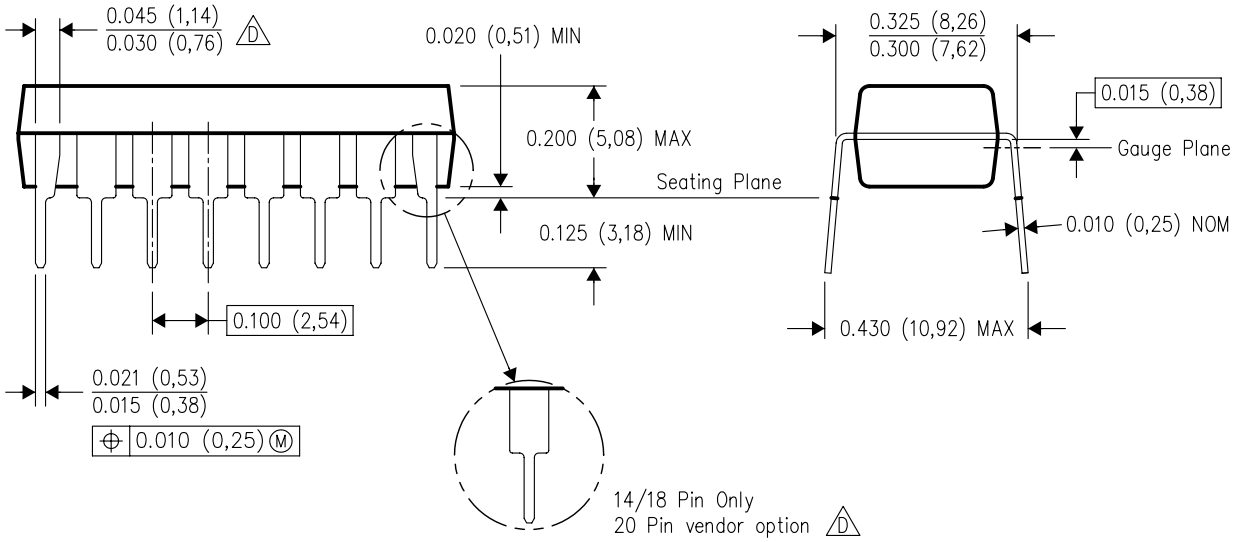
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

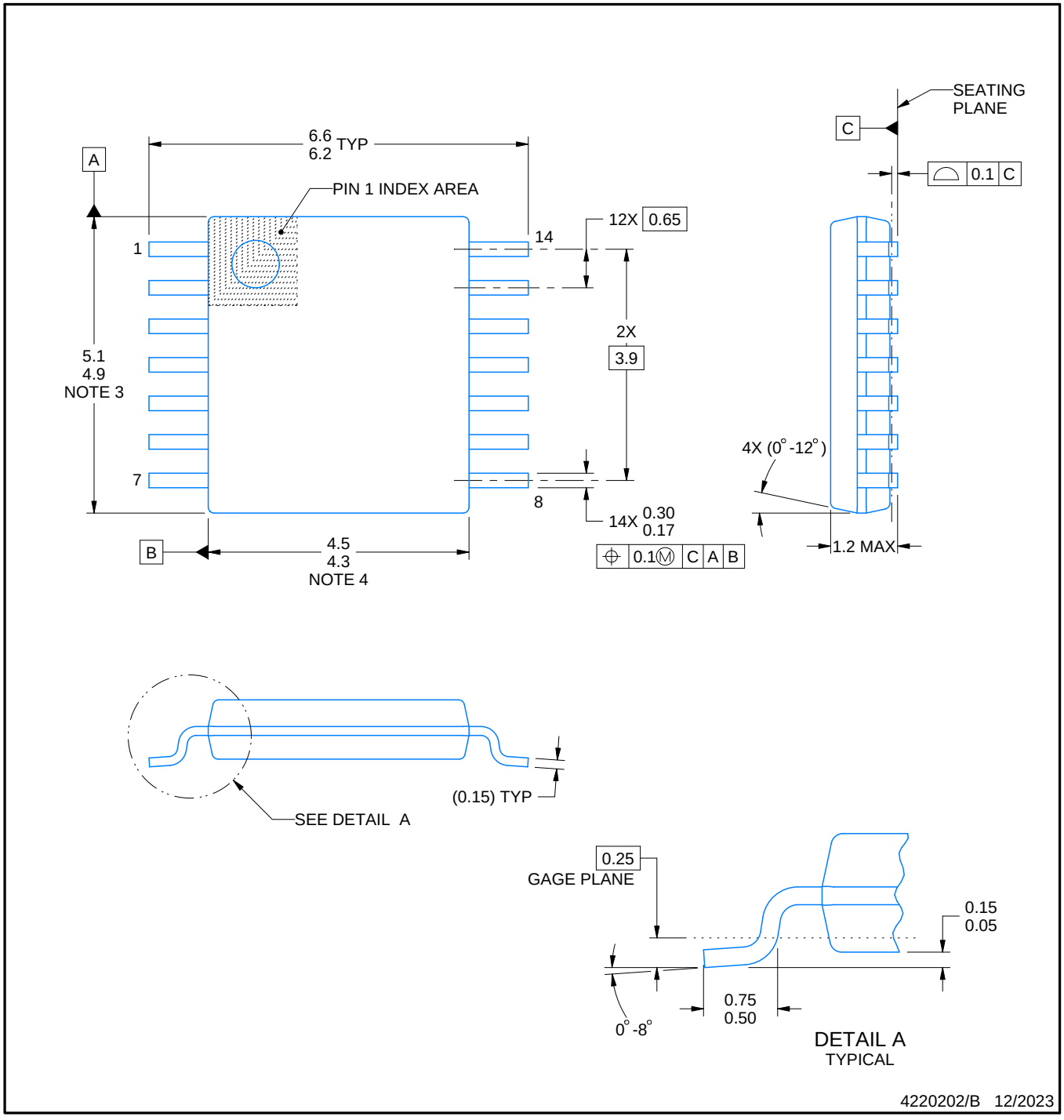
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

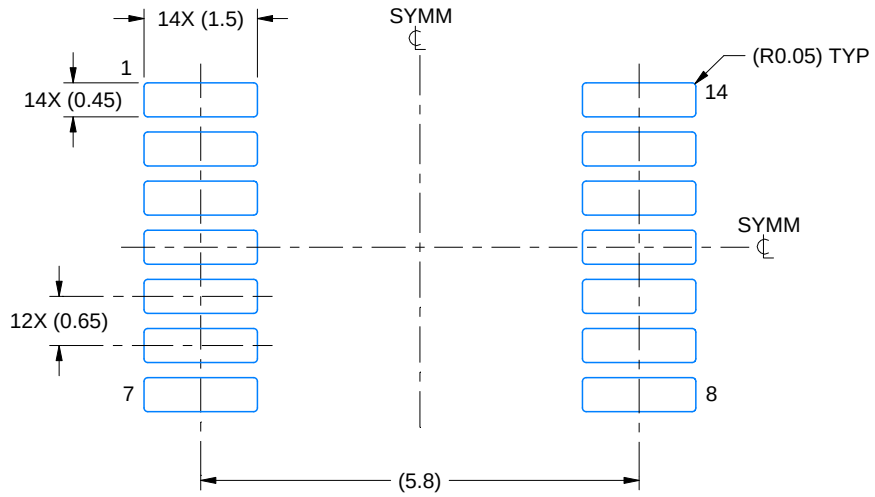
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

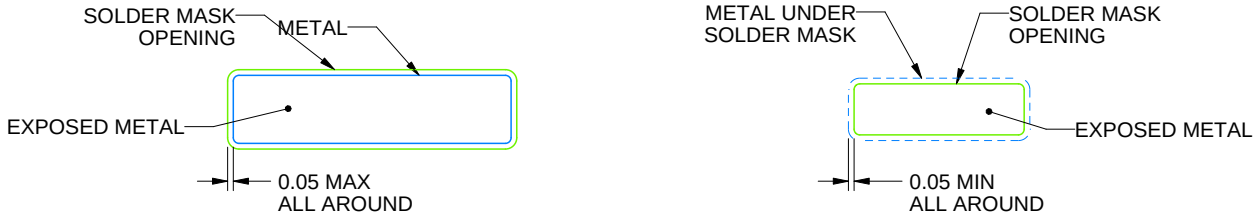


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

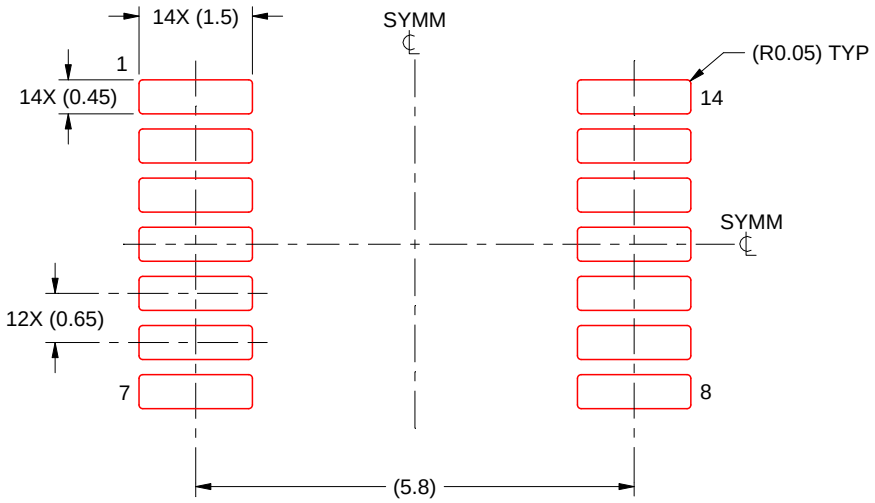


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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