LP8501 Multi-Purpose 9-Output LED Driver

Check for Samples: LP8501

FEATURES

- **Three Independent Program Execution Engines for User-defined Programs with Large SRAM Memory for Storing Lighting Programs**
- **9 Programmable Source (High Side) Driver Outputs with 25.5 mA Full-Scale Current, 8-bit Current Setting Resolution and 12-Bit PWM Control Resolution**
- **Flexible Grouping Possibility for All 9 Outputs Including GPO into Three Groups with Group PWM and Fade-In/ Fade-Out Controls**
- **Built-in LED Test**
- **Adaptive Charge Pump with 1x and 1.5x Gain Provides up to 95% LED Drive Efficiency, with Soft Start and Overcurrent/Short Circuit Protection**
- **Automatic Power Save Mode; I_{VDD} = 10 µA (typ.)**
- **Two Wire, I^2C-Compatible, Control Interface**
- **Small Application Circuit**
- **Pin-configured LED Powering for LEDs 1 to 6 and for LEDs 7 to 9**
- **Solution Area <18 mm^2**

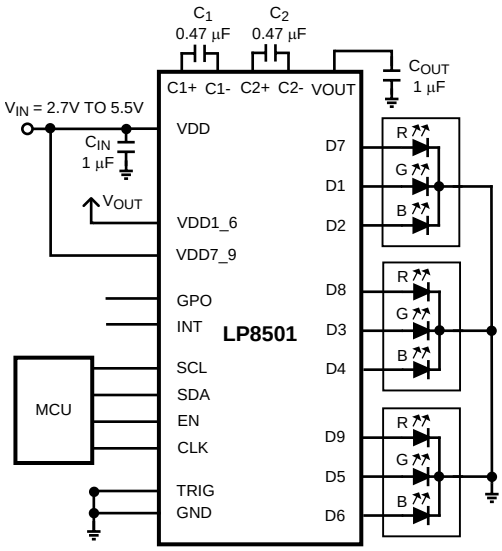
APPLICATIONS

- **Fun Lights and Indicator Lights**
- **LED Backlighting and Color Keypad Lighting**
- **Programmable Current Source**
- **Haptic Feedback Driver and GPIO Expander**

DESCRIPTION

The LP8501 is an LED driver with 9 outputs, designed to produce versatile lighting effects for mobile devices. The device is equipped with an internal program memory, which allows operation without processor control. Internal program memory is used by three independent program execution engines to produce user-defined lighting effects for the outputs.

A high-efficiency charge pump enables LED driving over full Li-Ion battery voltage range. The excellent efficiency over a wide operating range is achieved by autonomously selecting the best charge pump gain based on LED forward voltage requirements. The LP8501 is able to automatically enter power-save mode when LED outputs are not active, thus lowering idle current consumption down to 10 µA (typ.)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

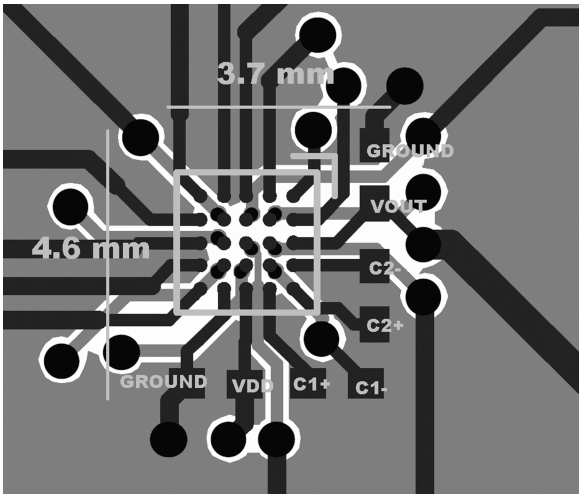
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2008–2013, Texas Instruments Incorporated

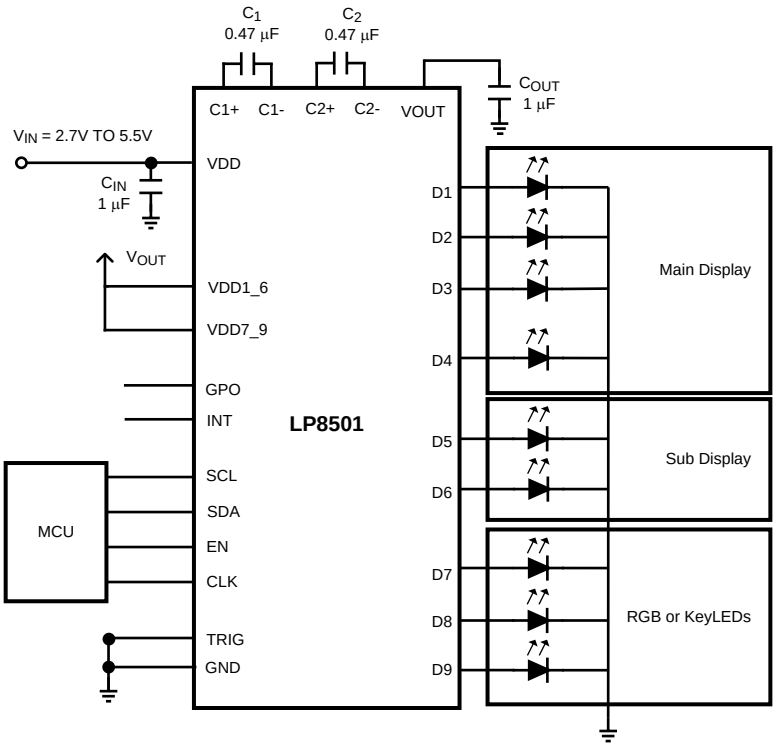
DESCRIPTION (CONTINUED)

The device has a flexible General Purpose Output (GPO) (which can be used, for example, as a digital control pin for other devices), an INT pin (interrupt function), which can be used to notify the processor, and a Trigger input interface, which allows program execution start without I^2C write.

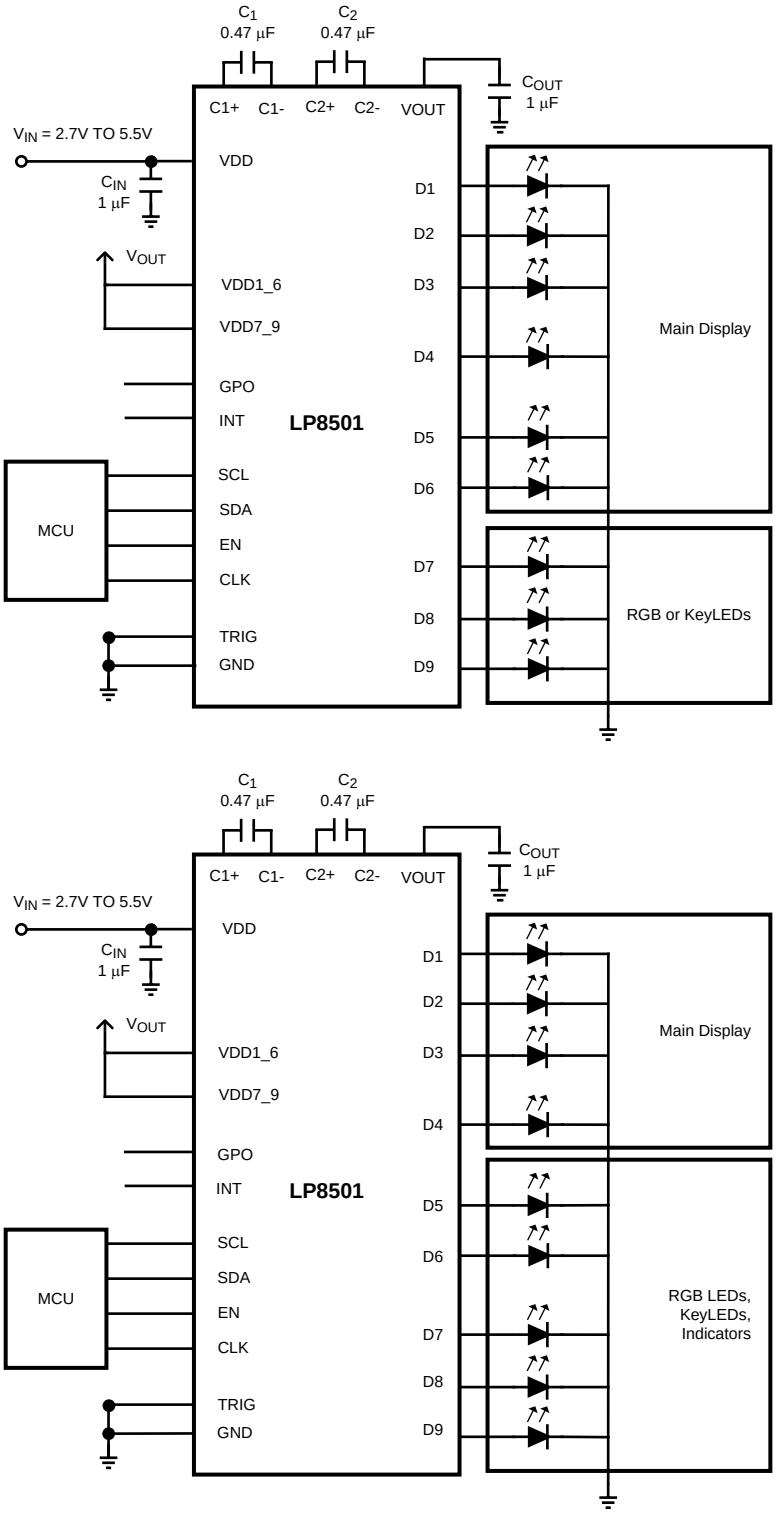
The device requires only four small and low-cost ceramic capacitors. The LP8501 is available in a tiny 25-bump 2.26 mm x 2.26 mm x 0.60 mm DSBGA package (0.4 mm pitch).

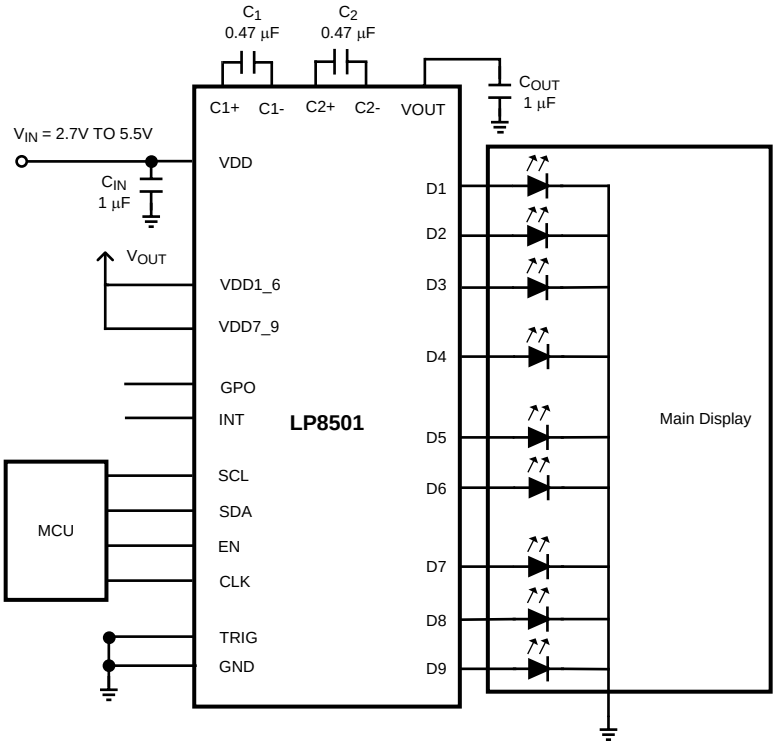


Typical Application Circuits



Copyright © 2008–2013, Texas Instruments Incorporated


C1
0.47 µF
C2
0.47 µF
COUT
1 µF
C1+
C1-
C2+
C2-
VOUT
VIN = 2.7V TO 5.5V
CIN
1 µF
VDD
VOUT
VDD1_6
VDD7_9
GPO
INT
LP8501
SCL
SDA
EN
CLK
TRIG
GND
MCU
D1
D2
D3
D4
D5
D6
D7
D8
D9
Main Display
RGB or KeyLEDs
C1
0.47 µF
C2
0.47 µF
COUT
1 µF
C1+
C1-
C2+
C2-
VOUT
VIN = 2.7V TO 5.5V
CIN
1 µF
VDD
VOUT
VDD1_6
VDD7_9
GPO
INT
LP8501
SCL
SDA
EN
CLK
TRIG
GND
MCU
D1
D2
D3
D4
D5
D6
D7
D8
D9
Main Display
RGB LEDs,
KeyLEDs,
Indicators



Connection Diagrams

Thin DSBGA 25-bump package, 2.26 x 2.26 x 0.60 mm body size, 0.4 mm pitch, Package Number YFQ0025

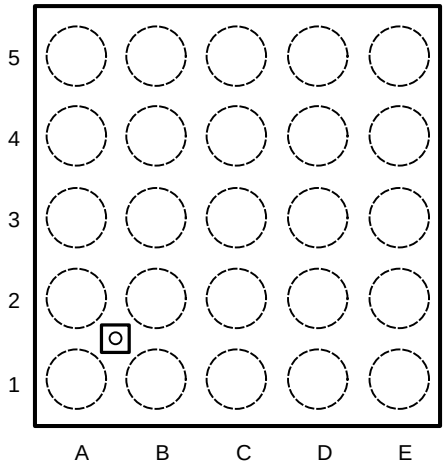


Figure 1. Top View

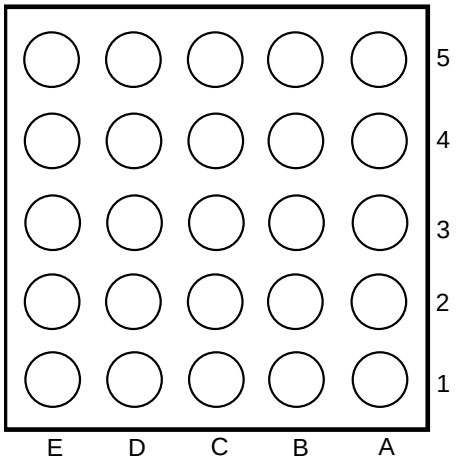


Figure 2. Bottom View

Copyright © 2008–2013, Texas Instruments Incorporated

PIN DESCRIPTIONS(1)

Pin	Name	Type	Description
A1	D1	A	Current source output 1
A2	D2	A	Current source output 2
A3	VOUT	A	Charge pump output
A4	C2-	A	Flying capacitor 2 negative terminal
A5	C2+	A	Flying capacitor 2 positive terminal
B1	D3	A	Current source output 3
B2	D4	A	Current source output 4
B3	VDD1_6	P	Power for D1 to D6 drivers
B4	C1-	A	Flying capacitor 1 negative terminal
B5	C1+	A	Flying capacitor 1 positive terminal
C1	D5	A	Current source output 5
C2	D6	A	Current source output 6
C3	VDD7_9	P	Power for D7 to D9 drivers
C4	EN	I	Enable
C5	VDD	P	Input power supply
D1	D7	A	Current source output 7.
D2	D8	A	Current source output 8.
D3	INT	OD/O	Interrupt for microcontroller unit. Leave unconnected if not used
D4	CLK	I	32 kHz clock input; connect to ground if not used.
D5	GND	G	Ground
E1	D9	A	Current source output 9.
E2	GPO	O	General purpose output. Leave unconnected if not used.
E3	TRIG	I/OD	Trigger; connect to ground if not used.
E4	SDA	I/OD	Serial interface data
E5	SCL	I	Serial interface clock

(1) A: Analog Pin, G: Ground Pin, P: Power Pin, I: Input Pin, I/O Input/Output Pin, O: Output Pin, OD: Open Drain Pin

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Copyright © 2008–2013, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

VDD		−0.3V to +6.0V
Voltage on D1 to D9, C1−, C1+, C2−, C2+, VOUT		−0.3V to + 6.0V
Voltage on Logic Pins (Input or Output Pins)		−0.3V to V_{DD} +0.3V with 6.0V max
Continuous Power Dissipation(4)		Internally Limited
Junction Temperature (T_{J-MAX})		125°C
Storage Temperature Range		−65°C to +150°C
Maximum Lead Temperature (Soldering)		See(5)
ESD Rating	Human Body Model: D1 to D9	4 kV(6)
	Human Body Model: All Other Pins	2.5 kV(6)
	Machine Model: All Pins	250V(7)

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) All voltages are with respect to the potential at the GND pins.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).
(5) For detailed soldering specifications and information, please refer to Texas Instruments Application Note AN1112 : DSBGA Wafer Level Chip Scale Package.
(6) Human Body Model, applicable standard JESD22-A114C
(7) Machine Model, applicable standard JESD22-A115-A

OPERATING RATINGS(1)(2)

V_{DD} Input Voltage Range	2.7V to 5.5V
Voltage on Logic Pins (Input or Output Pins)	0 to V_{DD}
Recommended Charge Pump Load Current	0 mA to 100 mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range(3)	−30°C to +85°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) All voltages are with respect to the potential at the GND pins.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

THERMAL PROPERTIES

Junction-to-Ambient Thermal Resistance (θ_{JA})(1), YFQ0025 Package(2)	Thermal Package	87°C/W

(1) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Copyright © 2008–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS[1][2][3]

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (−30°C < T_A < +85°C). Unless otherwise noted, specifications apply to the LP8501 Block Diagram with: V_{DD} = 3.6V, V_{EN} = 1.65V, C_{OUT} = 1 µF, C_{IN} = 1 µF, C_{1-2} = 0.47 µF.[4]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{VDD}	Standby supply current	VEN = 0V, CHIP_EN=0 (bit), external 32 kHz clock running or not running		0.2	**1**	µA
		CHIP_EN=0 (bit), external 32 kHz clock not running		0.7		µA
		CHIP_EN=0 (bit), external 32 kHz clock running		1.4		µA
	Normal Mode Supply Current	External 32 kHz clock running, charge pump and current source outputs disabled		0.6		mA
		Charge pump in 1x mode, no load, current source outputs disabled		0.8		mA
		Charge pump in 1.5x mode, no load, current source outputs disabled		1.8		mA
	Power Save Mode Supply Current	External 32 kHz clock running		11		µA
		Internal oscillator running		0.6		mA
f_{OSC}	Internal Oscillator Frequency Accuracy		−4 **−7**		+4 **+7**	%

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) All voltages are with respect to the potential at the GND pins.
(3) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(4) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

CHARGE PUMP ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{OUT}	Charge Pump Output Resistance	Gain = 1.5x Gain = 1x		3.5 1		Ω
f_{SW}	Switching Frequency			1.25		MHz
I_{GND}	Ground Current	Gain = 1.5x Gain = 1x		1.2 0.3		mA
t_{ON}	V_{OUT} Turn-On Time[1]	V_{DD} = 3.6V, I_{OUT} = 60 mA		100		µs

(1) Turn-on time is measured from the moment the charge pump is activated until the V_{OUT} crosses 90% of its target value.

LED DRIVER ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LEAKAGE}$	Leakage Current (outputs D1 to D9)			0.1	1	µA
I_{MAX}	Maximum Source Current	Outputs D1 to D9		25.5		mA
I_{OUT}	Output Current Accuracy[1]	Output current set to 17.5 mA	−4 **−5**		+4 **+5**	%
I_{MATCH}	Matching[1]	Output current set to 17.5 mA		1		%
f_{LED}	LED Switching Frequency			312		Hz
V_{SAT}	Saturation Voltage[2]	Output current set to 17.5 mA		60	100	mV

(1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current outputs on the part (D1 to D9), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN)/AVG. The largest number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts. Note that some manufacturers have different definitions in use.
(2) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at V_{OUT} – 1V.

Copyright © 2008–2013, Texas Instruments Incorporated

LED TEST ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Units
LSB	Least Significant Bit			30		mV
E_{ABS}	Total Unadjusted Error(1)	V_{IN_TEST} = 0V to V_{DD}		<±3	±4	LSB
t_{CONV}	Conversion Time			2.7		ms
V_{IN_TEST}	DC Voltage Range		0		5	V

(1) Total unadjusted error includes offset, full-scale and linearity errors.

LOGIC INTERFACE CHARACTERISTICS

V_{EN} = 1.65 to V_{DD} unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Logic input EN						
V_{IL}	Input Low Level				**0.5**	V
V_{IH}	Input High Level		**1.2**			V
I_I	Input Current		**–1.0**		**1.0**	µA
t_{DELAY}	Input Delay(1)			2		µs
Logic input SCL, SDA, TRIG, CLK						
V_{IL}	Input Low Level				**0.2xV_{EN}**	V
V_{IH}	Input High Level		**0.8xV_{EN}**			V
I_I	Input Current		**-1.0**		**1.0**	µA
Logic output SDA, TRIG, INT						
V_{OL}	Output Low Level	I_{OUT} = 3 mA (pullup current)		0.3	**0.5**	V
I_L	Output Leakage Current	V_{OUT} = 2.8V			**1.0**	µA
Logic output GPO						
V_{OL}	Output Low Level	I_{OUT} = 3 mA		0.3	**0.5**	V
V_{OH}	Output High Level	I_{OUT} = -2 mA	**V_{DD} −0.5**	V_{DD} −0.3		
I_L	Output Leakage Current	V_{OUT} = 2.8V			**1.0**	µA

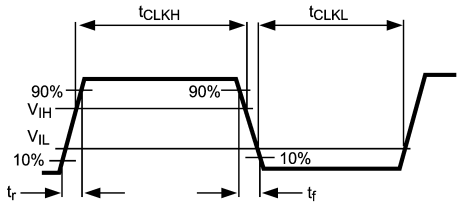
(1) The I^2C host should allow at least 500 µs before sending data to the LP8501 after the rising edge of the EN pin.

Copyright © 2008–2013, Texas Instruments Incorporated

RECOMMENDED EXTERNAL CLOCK SOURCE CONDITIONS (1) (2)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Logic input CLK						
f_{CLK}	Clock Frequency			32.7		kHz
t_{CLKH}	High Time		6			µs
t_{CLKL}	Low Time		6			µs
t_r	Clock Rise Time	10% to 90%			2	µs
t_f	Clock Fall Time	90% to 10 %			2	µs

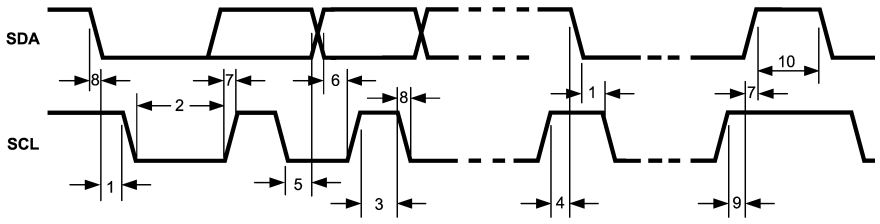
(1) Specified by design. V_{EN} = 1.65V to V_{DD}.
(2) The ideal external clock signal for the LP8501 is a 0V to V_{EN}, 25% to 75% duty-cycle square wave. At frequencies above 32.7 kHz, program execution will be faster and at frequencies below 32.7 kHz program execution will be slower.



SERIAL BUS TIMING PARAMETERS (SDA, SCL)(1)

Symbol	Parameter	Limit		Units
		Min	Max	
f_{SCL}	Clock Frequency		400	kHz
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time	50		ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	20+0.1 C_b	300	ns
8	Fall Time of SDA and SCL	15+0.1 C_b	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load Parameter for Each Bus Line Load of One Picofarad Corresponds to One Nanosecond	10	200	ns

(1) Specified by design. V_{EN} = 1.65V to V_{DD}.



TYPICAL PERFORMANCE CHARACTERISTICS

LED Current vs. Current Register Code

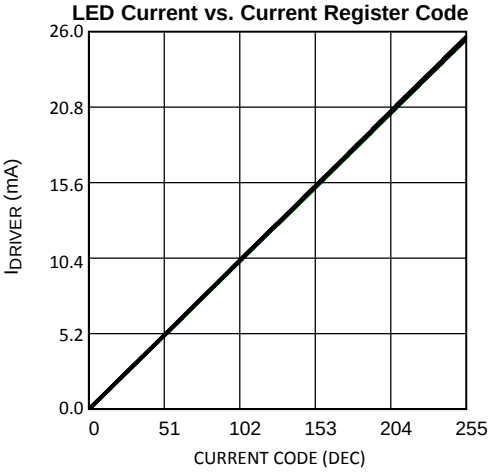


Figure 3.

LED Current vs. Supply Voltage

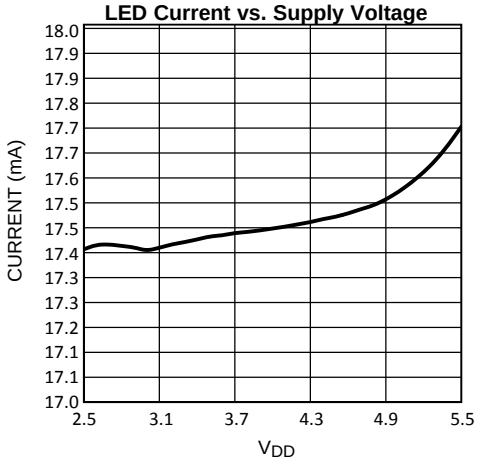


Figure 4.

LED Drive Efficiency vs. Input Voltage Automatic Gain Change

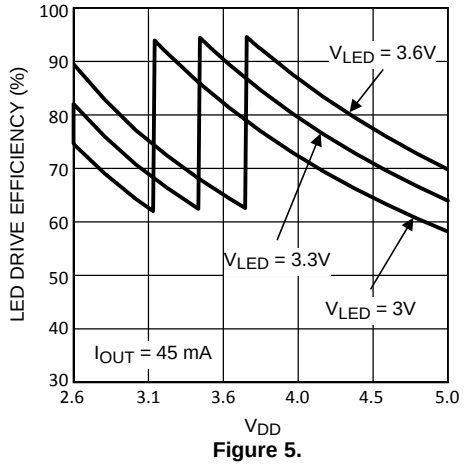


Figure 5.

Charge Pump Efficiency vs. Load Current 1.5x Mode

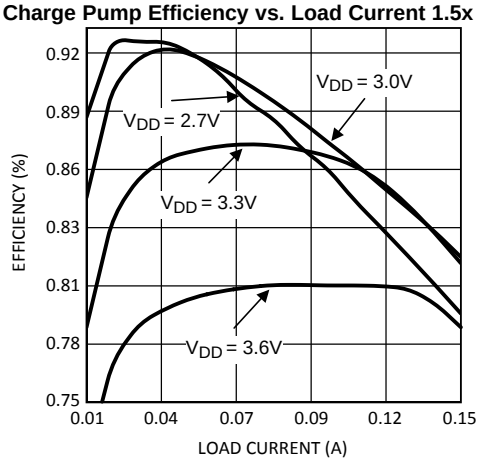


Figure 6.

Charge Pump Efficiency vs. Input Voltage 1.5x Mode

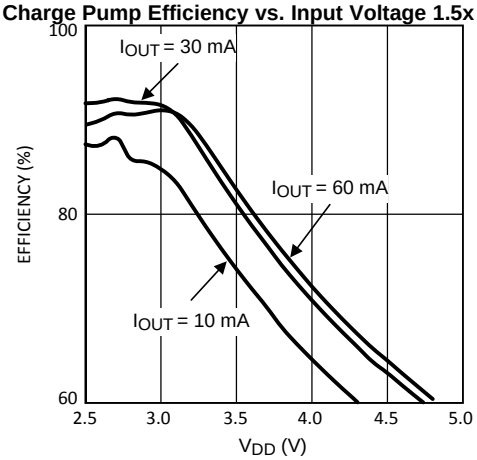


Figure 7.

Charge Pump Output Voltage 1.5x Mode vs. Load Current

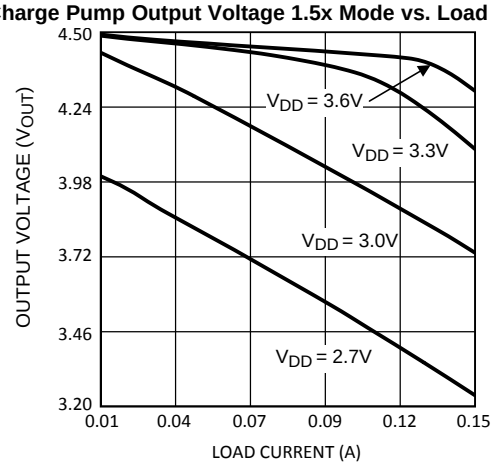


Figure 8.

Copyright © 2008–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Charge Pump Startup in 1x and 1.5x Modes

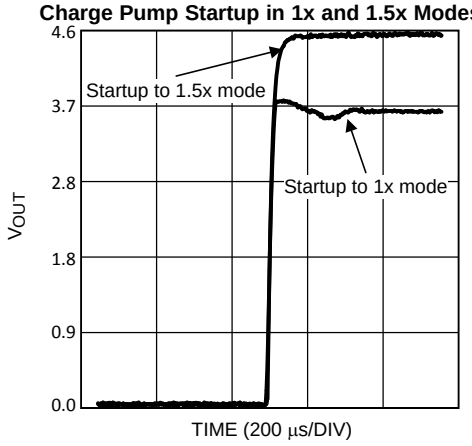


Figure 9.

Charge Pump Automatic Gain Change with Different Hysteresis

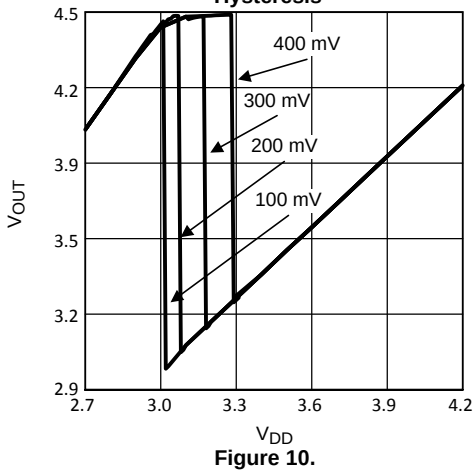


Figure 10.

Charge Pump Automatic Gain Change with Different LED Forward Voltages

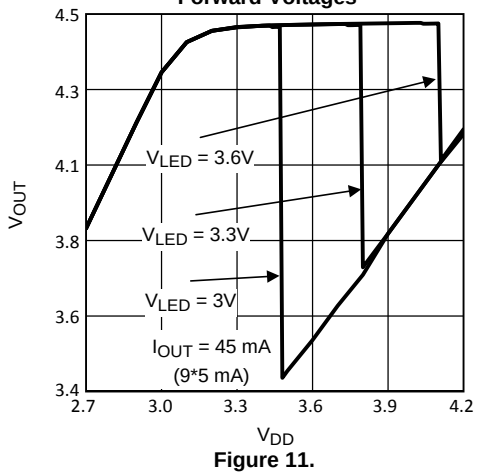


Figure 11.

Charge Pump Automatic Gain Change Hysteresis with 400 mV Setting

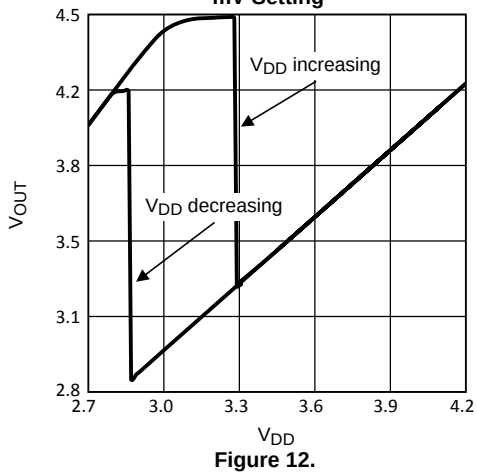


Figure 12.

Line Transient and Charge Pump Automatic Gain Change (1.5x to 1x) with 9 LED Outputs at 1mA 100% PWM

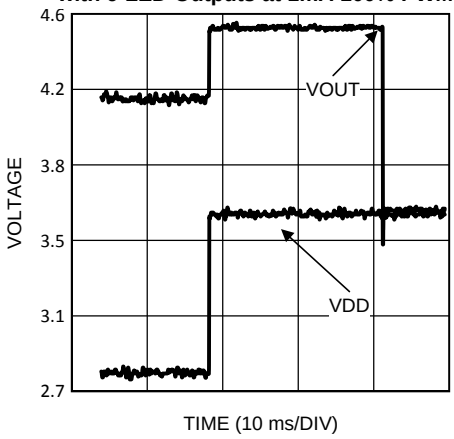


Figure 13.

Line Transient and Charge Pump Automatic Gain Change (1x to 1.5x) with 9 LED Outputs at 1mA 100% PWM

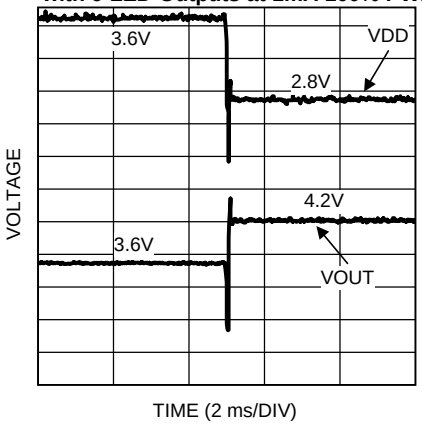


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Current Consumption with Different Charge Pump Modes (LED Outputs Off)

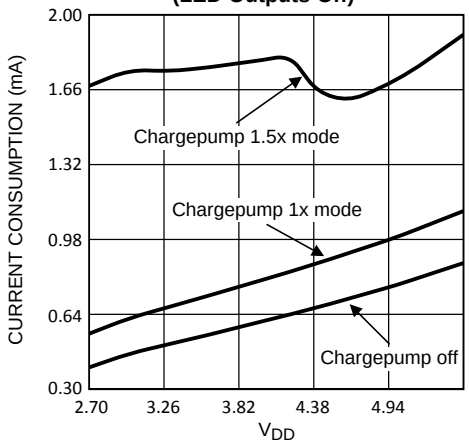


Figure 15.

Current Consumption in Power Save Mode with Different Clocks (Charge Pump in 1x Mode, LED Outputs Off)

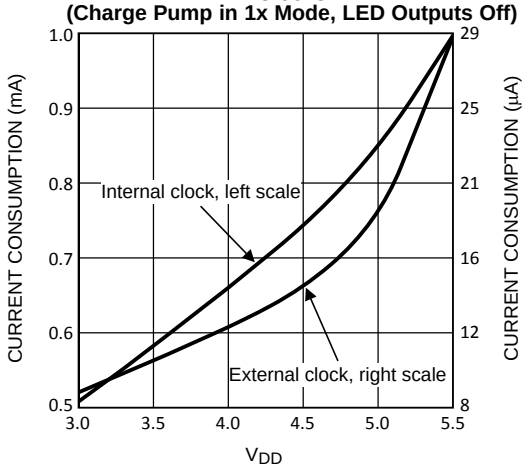


Figure 16.

Current Consumption with Different Temperatures (Charge Pump in 1x Mode, LED Outputs Off)

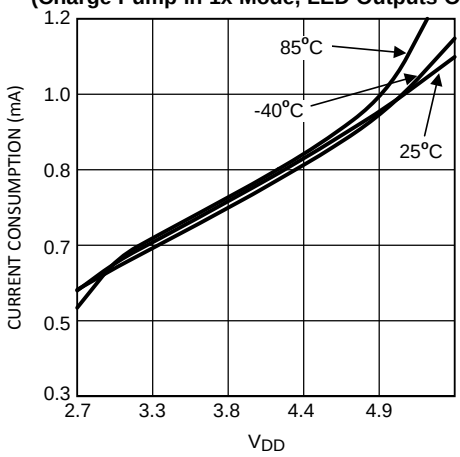


Figure 17.

Copyright © 2008–2013, Texas Instruments Incorporated

FUNCTIONAL OVERVIEW

The LP8501 is a fully integrated lighting management unit (LMU) designed for producing lighting effects for mobile devices. The LP8501 includes all necessary power management, high-side current sources, two-wire control interface and programmable execution engines. The overall maximum current for each driver is set by an 8-bit register.

The LP8501 controls LED luminance with a pulse width modulation (PWM) scheme with a resolution of 12 bits.

Programming

The LP8501 provides flexibility and programmability for dimming and sequencing control. Each LED can be controlled directly and independently through the serial bus. LED drivers can also be freely grouped together. The LED drivers may be grouped into a maximum of three groups. Each of the three groups' PWM can be controlled through the serial bus.

The LP8501 has three independent program execution engines, so it is possible to form three independently programmable LED banks. LED drivers can be grouped based on their function so that, for example, the first bank of drivers can be assigned to the keypad illumination, the second bank to the “fun lights” and the third group to the indicator LED(s). Each bank can contain 1 to 9 LED driver outputs. Instructions for program execution engines are stored in the program memory. The total amount of the program memory is 96 instructions, and the user can allocate the memory as required by the engines.

LED Error Detection

The LP8501 has built-in LED error detection. Error detection both detects open and short circuits, and provides an opportunity to measure the forward voltages of the LEDs. The test is activated by serial interface write, and the result can be read through the serial interface during the next cycle. This can be used for general purpose measurements such as checking the supply voltages and charge pump output voltage.

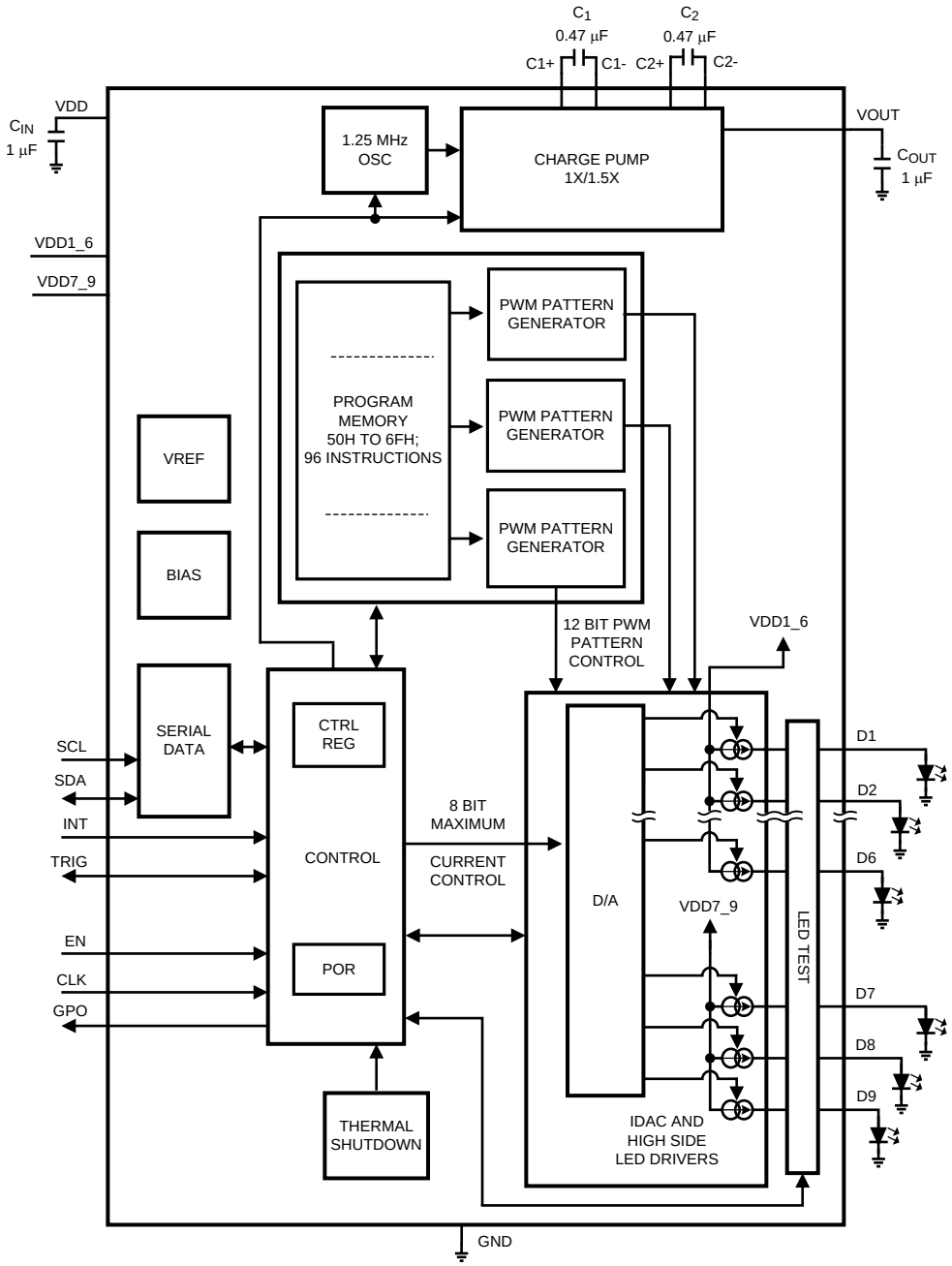
Energy Efficiency

When charge pump automatic mode selection is enabled, the LP8501 monitors the voltage over the drivers which are powered from the charge pump (V_{OUT}) so that the device can select the best charge pump gain and maintain good efficiency over the whole operating voltage range. In RGB LED applications the red LED element typically has a forward voltage of about 2V. For that reason, the outputs D7, D8 and D9 can be powered by V_{DD} since battery voltage is high enough to drive red LEDs over the whole operating range. This allows driving of three RGB LEDs with good efficiency because the red LEDs don't load the charge pump.

The LP8501 is able to automatically enter power-save mode, when LED outputs are not active, thus lowering idle current consumption down to 10 µA (typ.). Also, during the "down time" of the PWM cycle (constant current output status is low), additional power savings can be achieved under certain conditions.

Copyright © 2008–2013, Texas Instruments Incorporated

LP8501 Block Diagram



Copyright © 2008–2013, Texas Instruments Incorporated

Modes of Operation

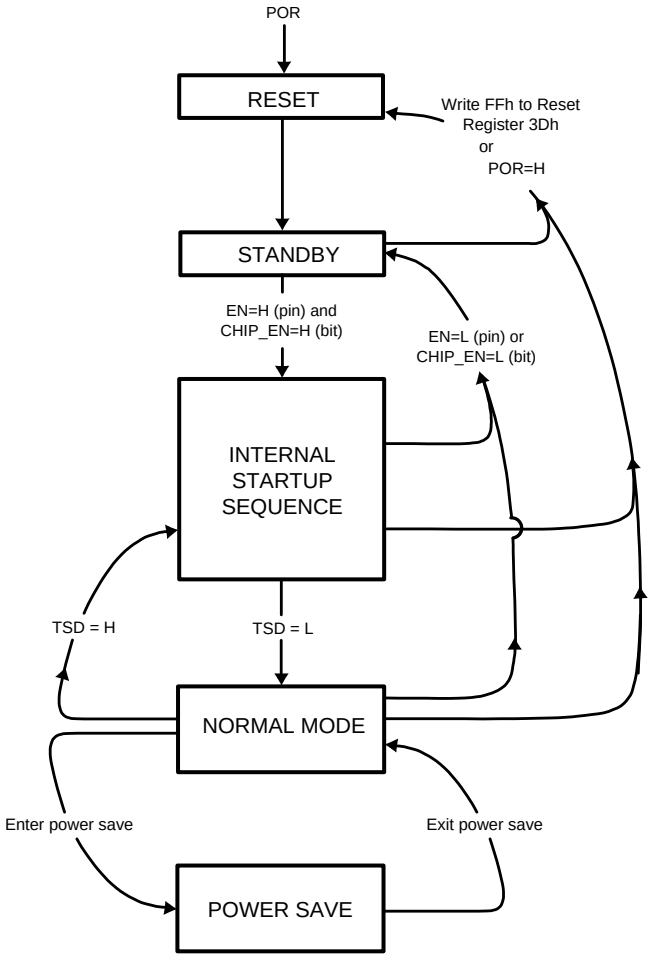
RESET In the RESET mode all the internal registers are reset to the default values. Reset is entered always if FFh is written to Reset Register (3Dh) or internal Power-On Reset (POR) is active. POR will activate during the chip startup or when the supply voltage V_{DD} fall below 1.5V (typ.). Once V_{DD} rises above 1.5V (typ.), POR will deactivate, and the chip will continue to the STANDBY mode. The CHIP_EN control bit is low after POR by default.

STANDBY: The STANDBY mode is entered if the register bit CHIP_EN or the EN pin is LOW, and Reset is not active. This is the low-power consumption mode, when all circuit functions are disabled. Registers can be written in this mode if the EN pin is raised to high state so that control bits will be effective right after the start up.

STARTUP: When CHIP_EN bit is written high and the EN pin is high, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (VREF, Bias, Oscillator etc.). Startup delay is 500 µs. If the chip temperature rises too high, the Thermal Shutdown (TSD) disables the chip operation, and chip waits in STARTUP mode until no thermal shutdown event is present.

NORMAL: During NORMAL mode the user controls the chip using the Control Registers.

POWER SAVE: In POWER SAVE mode analog blocks are disabled to minimize power consumption. See Power Saving for further information.



Charge Pump Operational Description

Overview

The LP8501 includes a pre-regulated switched-capacitor charge pump with a programmable voltage multiplications of 1 and 1.5x. The 1.5x mode combines the principles of a switched-capacitor charge pump and a linear regulator, generating a regulated 4.5V output from Li-Ion input voltage range. A two-phase non-overlapping clock generated internally controls the operation of the charge pump. During the charge phase, both flying capacitors (C1 and C2) are charged from input voltage. In the pump phase that follows, the flying capacitors are discharged to output. A traditional switched capacitor charge pump operating in this manner will use switches with very low on-resistance, ideally 0Ω, to generate an output voltage that is 1.5x the input voltage. The LP8501 regulates the output voltage by controlling the resistance of the input-connected pass-transistor switches in the charge pump.

Output Resistance

At lower input voltages, the charge pump output voltage may degrade due to effective output resistance (R_{OUT}) of the charge pump. The expected voltage drop can be calculated by using a simple model for the charge pump illustrated in Figure 18 below.

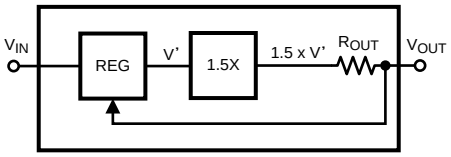


Figure 18. Charge Pump Output Resistance Model

The model shows a linear pre-regulation block (REG), a voltage multiplier (1.5x), and an output resistance (R_{OUT}). Output resistance models the output voltage drop that is inherent to switched capacitor converters. The output resistance is 3.5Ω (typ.), and it is a function of switching frequency, input voltage, flying capacitors' capacitance value, internal resistances of the switches and ESR of the flying capacitors. When the output voltage is in regulation, the regulator in the model controls the voltage V' to keep the output voltage equal to 4.5V (typ).

With increased output current, the voltage drop across R_{OUT} increases. To prevent a drop in output voltage, the voltage drop across the regulator is reduced, V' increases, and V_{OUT} remains at 4.5V. When the output current increases to the point that there is zero voltage drop across the regulator, V' equals the input voltage, and the output voltage is "on the edge" of regulation. Additional output current causes the output voltage to fall out of regulation, so that the operation is similar to a basic open-loop 1.5x charge pump. In this mode, output current results in output voltage drop proportional to the output resistance of the charge pump. The out-of-regulation output voltage can be approximated by: $V_{OUT} = 1.5 \times V_{IN} - I_{OUT} \times R_{OUT}$.

Controlling the Charge Pump

The c harge pump is controlled with two CP_MODE bits in CONFIG register (address 36h). When both of the bits are low, charge pump is disabled and output voltage is pulled down with an internal 300 kΩ (typ.) resistor. The charge pump can be forced to bypass mode, so that the battery voltage is connected directly to the current sources; in 1.5x mode output voltage is boosted to 4.5V. In automatic mode, charge pump operation mode is defined by current source outputs saturation as described in the next section.

LED Forward Voltage Monitoring

When the charge-pump automatic mode selection is enabled, voltages over LED drivers connected to charge pump are monitored. If the drivers do not have enough headroom, the charge pump gain is set to 1.5x. Driver saturation monitor does not have a fixed voltage limit, since saturation voltage is a function of temperature and current. Charge pump gain is set to 1x when battery voltage is high enough to supply all LEDs. Note that in order to get the automatic gain change work correctly, power config bits in register 05H must be set according to where the VDD1_6 and VDD7_9 are connected.

In automatic gain change mode, the charge pump is switched to bypass mode (1x) when LEDs are inactive for over 50 ms.

Copyright © 2008–2013, Texas Instruments Incorporated

Gain Change Hysteresis

Charge pump gain control utilizes digital filtering to prevent supply voltage disturbances (for example, the transient voltage on the power supply during the GSM burst) from triggering unnecessary gain changes. Hysteresis is provided to prevent periodic gain changes, which would occur due to LED driver and charge pump voltage drops in 1x mode. The hysteresis of the gain change can be configured by the user; default setting is factory programmable. Flexible configuration ensures that hysteresis can be minimized or set to desired level in each application.

LED Driver Operational Description

Overview

The LP8501 LED drivers are constant current sources. Output current can be programmed with an I^2C register up to 25.5 mA. The overall maximum current is set by 8-bit output current control registers with 100 µA step size. Each of the 9 LED drivers has a separate output current control register. See table below for current control.

CURRENT bits	Output Current
00000000	0.0 mA
00000001	0.1 mA
00000010	0.2 mA
...	...
10101111	17.5 mA default setting
....	....
11111110	25.4 mA
11111111	25.5 mA

The LED luminance pattern (dimming) is controlled with PWM (pulse width modulation) technique, which has internal resolution of 12 bits (8-bit control can be seen by user). PWM frequency is 312 Hz. See Figure 19.

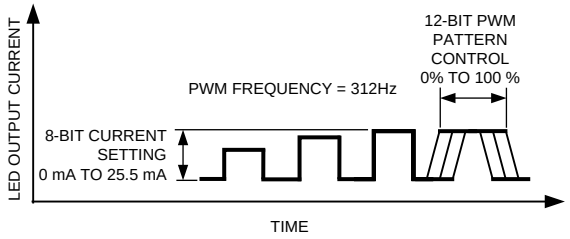


Figure 19. LED Pattern and Current Control Principle

For LED dimming a logarithmic or linear scale can be applied — see the figure below (Figure 20). Logarithmic or linear scheme can be set for both the program execution engine control and direct PWM control. By using a logarithmic PWM scale, the visual effect looks linear to the human eye.

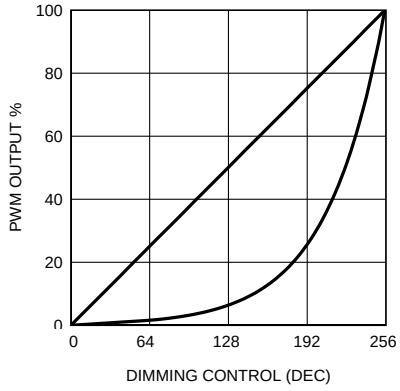


Figure 20. Logarithmic vs Linear Dimming

Copyright © 2008–2013, Texas Instruments Incorporated

Powering LEDs

The power for the LEDs is supplied via VDD1_6 (outputs D1 to D6) and VDD7_9 pins (outputs D7 and D9). Powering LEDs this way allows flexibility since the pins can be connected to the V_{DD} or to the V_{OUT} (or to another application power source, for example, an external DC/DC converter may be used), depending on the application.

In the case of LEDs which have forward voltages around 2 volts, LEDs can be powered directly from V_{DD}. If all the LEDs are powered from V_{DD} or an external power source and V_{OUT} is not used the charge pump can be left unconnected and charge pump capacitors can be left uninstalled. When the forward voltage of the LEDs is around 3.6V, V_{DD} may not be high enough. In this case the LEDs should be powered from the V_{OUT}.

Note that the power supply must be correctly defined in the LP8501 register settings (register 05h 'Power Config').

Controlling the PWM of High-Side LED Drivers

1. **Direct PWM Control**
   - All LP8501 LED drivers, D1 to D9, can be controlled independently through the two-wire serial I^2C compatible interface. For each high-side driver there is a PWM control register. Direct PWM control is active by default.
2. **Controlling by Program Execution Engines**
   - Engine control is used when the user wants to create programmed sequences. Th program execution engine has higher priority than direct control registers. Therefore, if the user has set a certain value to the PWM register, it will be automatically overridden when the program execution engine controls the driver. LED control and program execution engine operation is described later on in this document.
3. **Group Fader Control**
   - In addition to LED-by-LED PWM register control, the LP8501 is equipped with group fader control, which allows the user to fade in or fade out multiple LEDs by writing to only one register. This is a useful function to minimize serial bus traffic between the MCU and the LP8501. The LP8501 has three group fader registers, so it is possible to form three fader groups.
   - With the LP8501 it is also possible to set fade-in and fade-out times. These times control the time when ramping up or down the group PWM value. Time can be set with 4-bits according to the following table.

FADE IN/FADE OUT	Time (s)
0000	0.0
0001	0.05
0010	0.1
0011	0.2
0100	0.3
0101	0.4
0110	0.5
0111	0.6
1000	0.7
1001	0.8
1010	0.9
1011	1.0
1100	1.5
1101	2.0
1110	3.0
1111	4.0

Copyright © 2008–2013, Texas Instruments Incorporated

– When the LP8501 is shut down (through chip_en), the fading off can be achieved. When “fade-to-off” bit (in register 36h) is set to 1, the group fade times have effect, and the LEDs fade off according to the time set in the register.

Examples of Controlling LED Drivers

1. **Direct PWM Control Example —Start up the device:**
   – Supply, e.g., 3.6V to V_{DD}.
   – Supply, e.g., 1.8V to EN.
   – Write 40h (0100 0000b) to address 00h (enable LP8501).
   – Wait 500 µs (startup delay).

   Check LED powering
   – Suppose LED outputs from 1 to 6 are connected to V_{DD} and LED outputs 7 to 9 are connected to V_{OUT}.
   – Write 01h (0000 0001b) to address 05h (VDD1_6 powered from V_{DD} and VDD7_9 powered from V_{OUT}.

   Enable charge pump to AUTO mode and use internal clock
   – Write 19h (0001 1001b) to address 36h.

   Write PWM values:
   – Write 80h (1000 0000b) to address 16h (LED output 1 PWM duty cycle to 50%).
   – Write C0h (1100 0000b) to address 1Ah (LED output 5 PWM duty cycle to 75%).
   – Write FFh (1111 1111b) to address 1Eh (LED output 9 PWM duty cycle to 100%).

   LED outputs are turned on after PWM values are written. Changes to the PWM value registers are reflected immediately to the LED brightness. Default LED output current (17.5 mA) is used for LED outputs, if no other values are written.
2. **Controlling by Program Execution Engines Example —Start up device and configure device to SRAM write mode:**
   – Supply e.g. 3.6V to V_{DD}.
   – Supply e.g. 1.8V to EN.
   – Generate 32 kHz clock signal to CLK pin.
   – Write 40h (0100 0000b) to address 00h.
   – Wait 500 µs (startup delay).
   – Write 14h (0001 0100b) to address 01h (configure engines 1 and 2 to Load mode).

   Check LED powering
   – Suppose LED outputs from 1 to 6 are connected to V_{OUT} and LED outputs 7 to 9 are connected to V_{DD}.
   – Write 02h (0000 0010b) to address 05h (VDD1_6 powered from V_{OUT} and VDD7_9 powered from V_{DD}.

   Program load to SRAM
   – Write 00h (0000 0000b) to register 4Fh (select memory page 0).
   – Write 9Dh (1001 1101b) to register 50h (select LED output 1 for engine 1 MSB, instruction part).
   – Write 01h (0000 0001b) to register 51h (select LED output 1 for engine 1 LSB, output selection part).
   – Write 40h (0100 0000b) to register 52h (set PWM value to full FFh MSB, instruction part).
   – Write FFh (1111 1111b) to register 53h (set PWM value to full FFh LSB, PWM value part).
   – Write 7Eh (0111 1110b) to register 54h (wait for 0.48s (maximum) MSB, instruction part).
   – Write 00h (0000 0000b) to register 55h (wait for 0.48s LSB).
   – Write 40h (0100 0000b) to register 56h (set PWM value to zero MSB, instruction part).
   – Write 00h (0000 0000b) to register 57h (set PWM value to zero LSB, PWM value part).
   – Write 7Eh (0111 1110b) to register 58h (wait for 0.48s MSB, instruction part).
   – Write 00h (0000 0000b) to register 59h (wait for 0.48s LSB).
   – Write A2h (1010 0010b) to register 5Ah (branch instruction with loop count 4 MSB, instruction part).
   – Write 01h (0000 0001b) to register 5Bh (branch instruction with loop count 4 LSB sets program counter value to '1', i.e., program continues execution in this case from setting PWM value).
   – Write C0h (1100 0000b) to register 5Ch (end instruction MSB, instruction part).
   – Write 00h (0000 0000b) to register 5Dh (end instruction LSB).
   – Write 9Dh (1001 1101b) to register 5Eh (select LED output 3 for engine 2MSB, instruction part).

Copyright © 2008–2013, Texas Instruments Incorporated

- Write 03h (0000 0011b) to register 5Fh (select LED output 3for engine 2LSB, output selection part).
- Write 40h (0100 0000b) to register 60h (set PWM value to full FFh MSB, instruction part).
- Write FFh (1111 1111b) to register 61h (set PWM value to full FFh LSB, PWM value part).
- Write 7Eh (0111 1110b) to register 62h (wait for 0.48s (maximum) MSB, instruction part).
- Write 00h (0000 0000b) to register 63h (wait for 0.48s LSB).
- Write 40h (0100 0000b) to register 64h (set PWM value to zero MSB, instruction part).
- Write 00h (0000 0000b) to register 65h (set PWM value to zero LSB, PWM value part).
- Write 7Eh (0111 1110b) to register 66h (wait for 0.48s MSB, instruction part).
- Write 00h (0000 0000b) to register 67h (wait for 0.48s LSB).
- Write A2h (1010 0010b) to register 68h (branch instruction with loop count 4 MSB, instruction part).
- Write 01h (0000 0001b) to register 69h (branch instruction with loop count 4 LSB sets program counter value to '1', i.e., program continues execution in this case from setting PWM value).
- Write C0h (1100 0000b) to register 6Ah (end instruction MSB, instruction part).
- Write 00h (0000 0000b) to register 6Bh (end instruction LSB).

Set start address

- Write 00h (0000 0000b) to register 4Ch (set engine 1 start address to 0).
- Write 07h (0000 0111b) to register 4Dh (set engine 2 start address to 7, 7^{th} 16–bit write, 15^{th} I^2C write).
- Optional: Write 00h (0000 0000b) to register 37h (set program counter of engine 1 to 0).
- Optional: Write 00h (0000 0000b) to register 38h (set program counter of engine 2 to 0).

Enable powersave, set charge pump to auto mode and select external clock:

- Write 38h (0011 1000b) to register 36h.

Run program:

- Write 28h (0010 1000b) to register 01h (set engines 1 and 2 to Run mode).
- Write 68h (0110 1000b) to register 00h (set program execution from Hold to Run and keep device enabled).

LP8501 will now generate five 0.48 second long blinks to LED outputs 1 and 3.

3. **Group Fader ControlStart up the device:**
   - Supply, e.g., 3.6V to V_{DD}.
   - Supply, e.g., 1.8V to EN.
   - Write 40h (0100 0000b) to address 00h (enable the device).
   - Wait 500 µs (startup delay).

   Check LED powering

   - Suppose LED outputs from 1 to 9 are connected to V_{OUT}.
   - Write 03h (0000 0011b) to address 05h (VDD1_6 and VDD7_9 powered from V_{OUT}.

   Enable charge pump 1.5x mode and use internal clock:

   - Write 11h (0001 0001b) to register 36h.

   Select LED outputs 1, 3 and 7 to Fader Group 1:

   - Write 40h (0100 0000b) to address 06h (LED output 1 to group 1).
   - Write 40h (0100 0000b) to address 08h (LED output 3 to group 1).
   - Write 40h (0100 0000b) to address 0Ch (LED output 7 to group 1).

   Set group 1 fader times:

   - Write CFh (1100 1111b) to register 02h (group 1 Fade IN time to 1.5 s and Fade OUT time to 4s).

   Set group PWM value:

   - Write FFh (1111 1111b) to register 48h (group 1 PWM duty cycle to 100%, all three LED outputs fades on in 1.5s)

Copyright © 2008–2013, Texas Instruments Incorporated

LP8501 Engine Programming

The LP8501 has three independent programmable lighting engines. All the lighting engines have their own program memory block allocated by the user. Note that in order to access program memory the operation mode needs to be LOAD Program, at least for one of the three lighting engines. Also note that one should not change from RUN —mode directly to LOAD program. Correct sequence would be RUN (10) –> DISABLED (00) –> LOAD (01).

Program execution is clocked with 32 768Hz clock. This clock can be generated internally, or an external 32 kHz clock can be connected to CLK pin. Using external clock enables synchronization of LED timing to this clock rather than to the internal clock.

The engines have different priorities; thus when more than one engine is controlling the same LED output: the LED engine 1 has the highest priority, LED engine 2 second highest and LED engine 3 third highest.

Supported instruction set is listed in the tables below:

Table 1. LP8501 LED Driver Instructions

Inst.	Bit [15]	Bit [14]	Bit [13]	Bit [12]	Bit [11]	Bit [10]	Bit [9]	Bit [8]	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
Ramp	0	prescale	Step time					Sign	# of increments							
Set PWM	0	1	0	0	0	0	0	0	PWM value							
Wait	0	prescale	Time					0	0	0	0	0	0	0	0	0

Table 2. LP8501 LED Mapping Instructions

Inst.	Bit [15]	Bit [14]	Bit [13]	Bit [12]	Bit [11]	Bit [10]	Bit [9]	Bit [8]	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
mux_ld_start	1	0	0	1	1	1	0	0	0	SRAM address 0–95						
mux_ld_end	1	0	0	1	1	1	0	0	1	SRAM address 0–95						
mux_sel	1	0	0	1	1	1	0	1	0	LED select						
mux_clr	1	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0
mux_inc	1	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0
mux_dec	1	0	0	1	1	1	0	1	1	1	0	0	0	0	0	0
mux_set	1	0	0	1	1	1	1	1	1	SRAM address 0–95						

Table 3. LP8501 Branch Instructions

Inst.	Bit [15]	Bit [14]	Bit [13]	Bit [12]	Bit [11]	Bit [10]	Bit [9]	Bit [8]	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
Go to Start	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Branch	1	0	1	Loop count						Step number						
Int	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
End	1	1	0	Int	Reset	X	X	X	X	X	X	X	X	X	X	X
Trigger	1	1	1	Wait for a trigger						Send a trigger						X
				Ext. trig	X	X	ENGINE3	ENGINE2	ENGINE1	Ext. trig	X	X	ENGINE3	ENGINE2	ENGINE1	X

RAMP

This is the instruction useful for smoothly changing from one PWM value into another PWM value on the D1 to D9 outputs; in other words, generating ramps (with a negative or positive slope). The LP8501 allows programming of very fast and very slow ramps.

Ramp instruction generates a PWM ramp, using the effective PWM value as a starting value. At each ramp step the output is incremented/decremented by one unit, unless the step time span is 0 or number of increments is 0. Time span for one ramp step is defined with prescale (bit [14]) and step time (bits [13:9]). Prescale = 0 sets 0.49 ms cycle time and prescale = 1 sets 15.6 ms cycle time; so the minimum time span for one step is 0.49 ms (prescale * step time span = 0.49ms x 1) and the maximum time span is 15.6 ms x 31 = 484ms/step. Note: if all the step time bits [13:9] are set to zero, instruction is treated as Set PWM instruction.

The number of increment define how many steps will be taken during one ramp instruction; maximum increment value is 255d, which corresponds to incrementing from zero to the maximum value. If PWM reaches minimum/maximum value (0/255) during the ramp instruction, ramp instruction will be executed to the end regardless of saturation. This enables ramp instruction to be used as a combined ramp & wait instruction. Note: Ramp instruction is the wait instruction when the increment bits [7:0] are set to zero.

Setting bit LOG_EN high/low sets logarithmic (1) or linear ramp (0) (bit 5 in registers 06h — 0Eh and in register 15h for GPO). By using the logarithmic ramp setting the visual effect appears like a linear ramp, because the human eye behaves in a logarithmic way.

Name	Value (d)	Description
prescale	0	Divides master clock (32 768 Hz) by 16 = 2048 Hz → 0.488 ms cycle time
	1	Divides master clock (32 768 Hz) by 512 = 64 Hz → 15.625 ms cycle time
sign	0	Increase PWM output
	1	Decrease PWM output
step time	1 - 31	One ramp increment done in (step time) x (prescale). Note: 0 means Set PWM instruction
# of increments	0 - 255	The number of increment/decrement cycles Note: Value 0 takes the same time as increment by 1, but it is the wait instruction.

RAMP INSTRUCTION APPLICATION EXAMPLE

Let's say that the LED dimming is controlled according to the linear scale and effective PWM value at the moment t=0 is 140d (~55%,), as shown in Figure 21 below, and we want to reach a PWM value of 148d (~58%) at the moment t = 1.5s. The parameters for the RAMP instruction will be:

- Prescale = 1 → 15.625 ms cycle time
- Step time = 12 → step time span will be 12*15.625 ms = 187.5 ms
- Sign = 0 → increase PWM output
- # of increments = 8 → take 8 steps

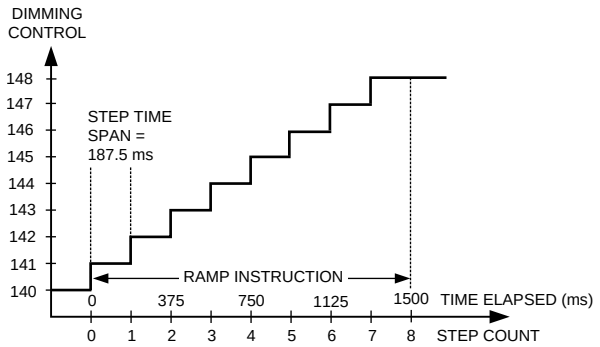


Figure 21. Example of Ramp Instruction

Copyright © 2008–2013, Texas Instruments Incorporated

SET_PWM

This instruction is used for setting the PWM value on the outputs D1 to D9 without any ramps. Set PWM output value from 0 to 255 with PWM value bits [7:0]. Instruction execution takes sixteen 32 kHz clock cycles (=488 µs).

Name	Value (d)	Description
PWM value	0 to 255	PWM output duty cycle 0 to 100%

WAIT

When a wait instruction is executed, the engine is set in a wait status, and the PWM values on the outputs are frozen.

Name	Value (d)	Description
prescale	0	Divide master clock (32 768 Hz) by 16 which means 0.488 ms cycle time
	1	Divide master clock (32 768 Hz) by 512 which means 15.625 ms cycle time
time	1 — 31	Total wait time will be = (time) x (prescale). Maximum 484 ms, minimum 0.488 ms

LED MAPPING INSTRUCTIONS

These commands define the engine-to-LED mapping. The mapping information is stored in a table, which is stored in the SRAM (program memory of the LP8501). Mapping information can be located anywhere in SRAM memory. LP8501 has three lighting engines (Engines) which can be mapped to 9 LED drivers or to one GPO pin. One engine can control one or multiple LED drivers. There are totally seven commands for the engine-to-LED driver control: **mux_ld_start, mux_ld_end, mux_sel, mux_clr, mux_inc, mux_dec, mux_set.** Note: the LED mapping instructions do not update PWM values to LED outputs. PWM values are updated after ramp or set_pwm instructions.

MUX_LD_START; MUX_LD_END

Mux_ld_start and mux_ld_ end define the mapping table location in the memory. With mux_ld_start instruction the mapped row can be activated at the same time by setting map = 1.

Name	Value (d)	Description
map	0	Mapped row inactive
	1	Set the mapped row active. MUX_LD_START only
SRAM address	0 - 95	Mapping table start/end address

MUX_SEL

With mux_sel instruction one, and only one, LED driver (or the GPO pin) can be connected to a lighting engine. Connecting multiple LEDs to one engine is done with the mapping table. After the mapping has been released from an LED, the PWM register value will still control the LED brightness. If the mapping is released from the GPO pin, serial bus control takes over the GPO state.

Name	Value (d)	Description
LED select	0 - 16	0 = no drivers selected 1 = LED1 selected 2 = LED2 selected ... 9 = LED9 selected 16 = GPO

MUX _CLR

Mux_clr clears engine-to-driver mapping. After the mapping has been released from an LED, the PWM register value will still control the LED brightness. If the mapping is released from the GPO pin, serial bus control takes over the GPO state.

Copyright © 2008–2013, Texas Instruments Incorporated

MUX_INC

A mux_inc instruction sets the next row active in the mapping table each time it is called. For example, if the 2nd row is active after a mux_inc instruction is called, the 3rd row will be active. If the mapping table end is reached, activation will roll to the mapping table start address next time when the mux_inc instruction is called. The engine will not push a new PWM value to the LED driver output before a SET_PWM or RAMP instruction is executed. If the mapping has been released from an LED, the value in the PWM register will still control the LED brightness. If the mapping is released from the GPO pin, serial bus control takes over the GPO state.

MUX_DEC

A mux_dec instruction sets the previous row active in the mapping table each time it is called. For example, if the 3rd row is active, after mux_dec instruction is called, the 2nd row will be active. If the mapping table start address is reached, activation will roll to the mapping table end address the next time the mux_dec instruction is called. The engine will not push a new PWM value to the LED driver output before a SET_PWM or RAMP instruction is executed. If the mapping has been released from an LED, the value in the PWM register will still control the LED brightness. If the mapping is released from the GPO pin, serial bus control takes over the GPO state.

MUX_SET

Mux_set sets the index pointer to point the mapping table row defined by bits [6:0] and sets the row active. The engine will not push a new PWM value to the LED driver output before a SET_PWM or RAMP instruction is executed. If the mapping has been released from an LED, the value in the PWM register will still control the LED brightness. If the mapping is released from the GPO pin, serial bus control takes over the GPO state.

Name	Value (d)	Description
SRAM address	0 to 95	Any SRAM address containing mapping data

GO-TO-START

A go-to-start command resets the Program Counter register (address 37h 38h or 39h) and continues executing the program from the I^2C register program start address defined in 4Ch-4Eh. Command takes sixteen 32 kHz clock cycles. Note that default value for all program memory registers is 00h, which is “Go-to-Start” command.

BRANCH

Branch instruction is mainly indented for repeating a portion of the program code several times. Step number parameter defines how many steps loop start point is relative to the engine Start Address. The loop count parameter defines how many times the instructions inside the loop are repeated. The LP8501 supports nested looping, i.e., loop inside loop. The number of nested loops is not limited. Instruction takes sixteen 32 kHz clock cycles.

Name	Value (d)	Description
loop count	0 to 63	The number of loops to be done. 0 means an infinite loop.
step number	0- to 95	How many steps loop start point is from engine Start Address.

INT

Sends interrupt to processor by pulling the INT pin down and setting the corresponding status bit high. Interrupt can be cleared by reading interrupt bits in STATUS/INTERRUPT register at address 3Ah. With this instruction program execution continues.

Copyright © 2008–2013, Texas Instruments Incorporated

END

Ends program execution and resets the PC. Instruction takes sixteen 32 kHz clock cycles. An end instruction can have two parameters, INT and RESET. These parameters are described in tables below. Execution engine bits (Register 00h bits [5:0]) are set to zero, i.e., hold mode.

Name	Value	Description
int	0	No interrupt will be sent. PWM registers values will remain intact. Program counter value is set to 0.
	1	Reset program counter value to 0 and send interrupt to processor by pulling the INT pin down and setting corresponding status bit high to notify that program has ended. PWM register values will remain intact. Interrupt can be cleared by reading interrupt bits in STATUS/INTERRUPT register at address 3Ah

Name	Value	Description
reset	0	Reset program counter value to 0 and hold. PWM register values remain intact.
	1	Reset program counter value to 0 and hold. PWM register values of the non-mapped drivers will remain. PWM register values of the mapped drivers will be set to '0000 0000'.

TRIGGER

Wait or send triggers can be used to synchronize operation between the program execution engines. A send trigger instruction takes sixteen 32 kHz clock cycles and a wait-for trigger takes at least sixteen 32 kHz clock cycles. The receiving engine stores the triggers which have been sent. Received triggers are cleared by wait for trigger instruction. Wait for trigger instruction is executed until all the defined triggers have been received (note: several triggers can be defined in the same instruction).

An external trigger input signal must stay low for at least two 32 kHz clock cycles to be executed. A trigger output signal is three 32 kHz clock cycles long. An external trigger signal is active low, i.e. when trigger is send/received the pin is pulled to GND. Sent external trigger is masked, i.e,. the device which has sent the trigger will not recognize it. If send and wait external triggers are used on the same instruction, the send external trigger is executed first, then the wait external trigger.

Name	Value (d)	Description
wait for a trigger	0 to 31	Wait for a trigger from the engine(s). Several triggers can be defined in the same instruction. Bit [7] engages engine 1, bit [8] engages engine 2, bit [9] engages engine 3 and bit [6] is for external trigger I/O. Bits [4] and [5] are not in use.
send a trigger	0 to 31	Send a trigger to the engine(s). Several triggers can be defined in the same instruction. Bit [1] engages engine 1, bit [2] engages engine 2, bit [3] engages engine 3 and bit [6] is for external trigger I/O. Bits [4] and [5] are not in use.

Power Saving

Automatic Power Save Mode

Automatic power save mode is enabled when the POWERSAVE_EN bit in register address 36h is '1'. Almost all analog blocks are powered down in power save if an external clock signal is used. Only the charge pump protection circuits remain active. However, if the internal clock has been selected, only the charge pump and LED drivers are disabled during the power save; the digital part of the LED controller needs to stay active. In both cases the charge pump enters the weak 1x mode. In this mode the charge pump utilizes a passive current limited keep-alive switch, which keeps the output voltage at the battery level. During the program execution LP8501 can enter power save if there is no PWM activity in any of the LED driver outputs. To prevent short power save sequences during program execution, LP8501 has an instruction look-ahead filter. During program execution engine 1, engine 2 and engine 3 instructions are constantly analyzed, and if there are time slots with no PWM activity on LED driver outputs for 50 ms, the device will enter power save. In power save mode program execution continues uninterruptedly. When an instruction that requires PWM activity is executed, a fast internal startup sequence will be started automatically.

Copyright © 2008–2013, Texas Instruments Incorporated

PWM Cycle Power Save Mode

PWM cycle power save mode is enabled when the PWM_POWERSAVE bit in register 36h is set to '1'. In PWM power save mode analog blocks are powered down during the down time of the PWM cycle. Blocks are powered down depending upon whether an external or an internal clock is used. While the Automatic Power-Save Mode saves energy when there is no PWM activity, the PWM Power-Save mode saves energy during PWM cycles. Like the Automatic Power-Save Mode, PWM Power-Save Mode works also during program execution.

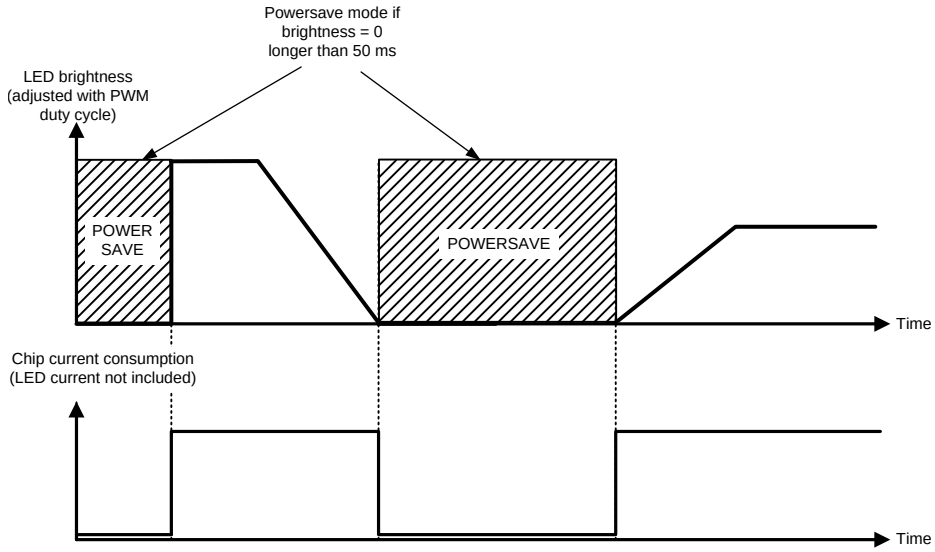


Figure 22. The Effect of Power-Save mode during a Lighting Sequence

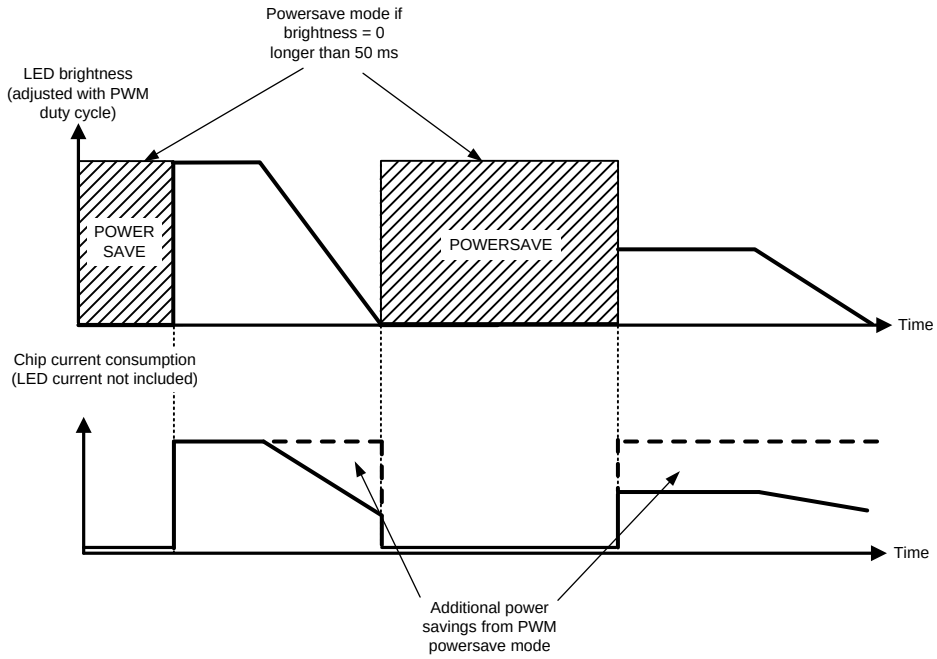


Figure 23. The effect of Powersave and PWM Powersave modes during a lighting sequence

Logic Interface Operational Description

The LP8501 features a flexible logic interface for connecting to processor and peripheral devices. Communication is done with and I^2C-compatible interface; different logic input/output pins makes it possible to, for example, trigger program execution or enable power saving for the device.

Copyright © 2008–2013, Texas Instruments Incorporated

IO LEVELS

I^2C interface, CLK and TRIG pin input levels are defined by the EN pin. Using the EN pin as voltage reference for logic inputs simplifies PWR routing and eliminates the need for a dedicated V_{IO} pin. In the following block diagram EN pin connections are illustrated.

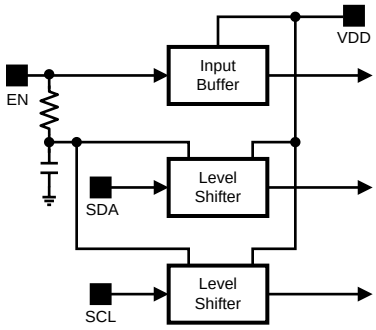


Figure 24. Using EN Pin As Digital IO Voltage Reference

GPO/INT Pins

The LP8501 has one General Purpose Output pin (GPO); the INT pin also can be configured as a GPO pin. The GPO pin level is defined by V_{DD} voltage. It also has its own PWM control register. GPO can be configured into fader groups, and it can be used in LED engine programming. When INT is configured as GPO, its level is defined by the V_{DD}. State of the pins can be controlled with GPO register (3Bh). GPO pins are digital CMOS outputs, and no pull-up/down resistors are needed.

When the INT pin GPO function is disabled, it operates as an open drain pin. The INT signal is active low, i.e., when interrupt signal is sent, the pin is pulled to GND. External pull-up resistor is needed for proper functionality.

Table 4. GPO register (3Bh)

Name	Bit	Description
INT_CONF	2	Enable INT pin GPO function 0 = INT pin functions as a INT pin 1 = INT pin functions as a GPO pin
GPO	1	0 = GPO pin state is low 1 = GPO pin state is high
GPO_INT	0	0 = INT pin state is low (INT_CONF=1) 1 = INT pin state is high (INT_CONF=0)

TRIG Pin

The TRIG pin can function as an external trigger input or output. The external trigger signal is active low if, when trigger is sent/received, the pin is pulled to GND. TRIG is an open drain pin, and an external pull-up resistor is needed for trigger line. The external trigger input signal must be at least two 32 kHz clock cycles long to be recognized. Trigger output signal is three 32 kHz clock cycles long. If TRIG pin is not used on application, it should be connected to GND to prevent floating of this pin and extra current consumption.

CLK Pin

The CLK pin is used for connecting an external 32 kHz clock to the LP8501. Using an external clock can improve automatic power-save mode efficiency because the internal clock can be switched off automatically when the device has entered powersave mode with an external clock present. The device can be used without the external clock. If an external clock is not used on the application, the CLK pin should be connected to GND to prevent floating of this pin and extra current consumption.

Copyright © 2008–2013, Texas Instruments Incorporated

I²C-Compatible Control Interface

The I²C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines should each have a pull-up resistor placed somewhere on the line and remain HIGH even when the bus is idle. Note: CLK pin is not used for serial bus data transfer.

Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW.

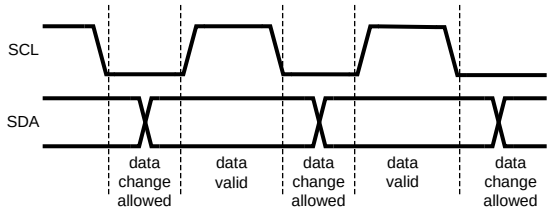


Figure 25. Data Validity Diagram

Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitions from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitions from LOW to HIGH while SCL is HIGH. The bus master always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LP8501 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LP8501 generates an acknowledge after each byte has been received.

There is one exception to the “acknowledge after every byte” rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

I²C-Compatible Chip Address

LP8501 serial bus address is 32h.

Copyright © 2008–2013, Texas Instruments Incorporated

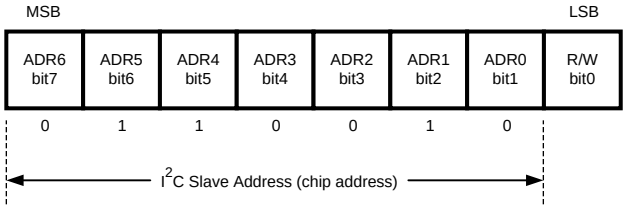


Figure 26. LP8501 Chip Address

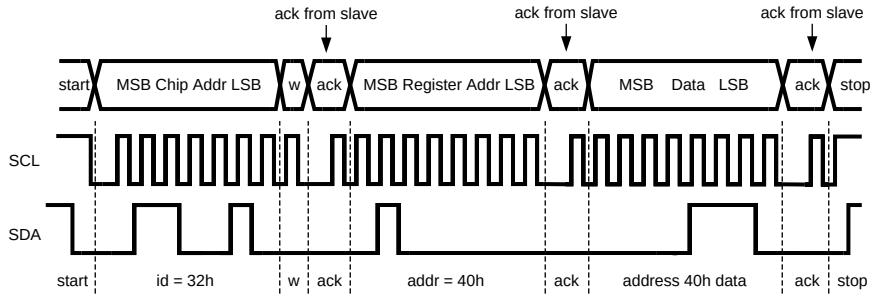
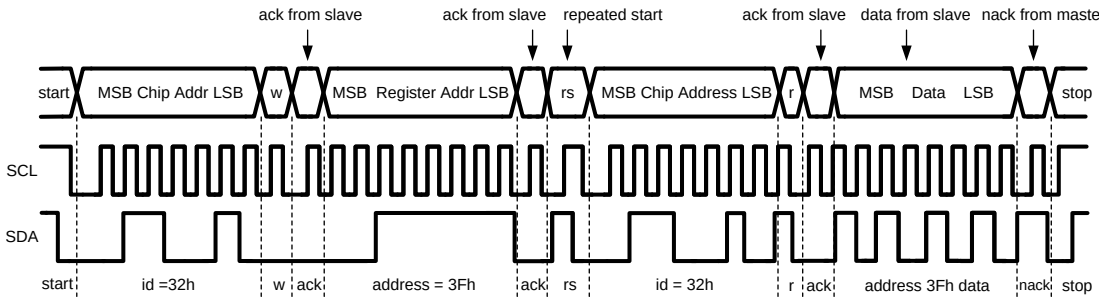


Figure 27. Write cycle (w = write; SDA = “0”) id = chip address = 32h for LP8501



When a READ function is to be accomplished, a WRITE function must precede the READ function, as show above.

Figure 28. Read cycle (r = read; SDA = "1"), id = chip address = 32h for LP8501

Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes, the slave’s control register address will be incremented by one after acknowledge signal. In order to reduce program load time LP8501 supports address auto increment. Register address is incremented after each 8 data bits. For example, the whole program memory page can be written in one serial bus write sequence. Note: serial bus address auto increment is not supported for register addresses from 16H to 1EH.
- Write cycle ends when the master creates stop condition.

Control Register Read Cycle

- Master device generates a start condition.

- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition

Auto Increment Feature

The auto increment feature allows writing several consecutive registers within one transmission. Every time an 8-bit word is sent to the LP8501, the internal address index counter will be incremented by one and the next register will be written. The table below shows writing sequence to two consecutive registers. The auto increment feature is enabled by writing the EN_AUTO_INCR bit high in the MISC register (address 36h). Note that the serial bus address auto increment is not supported for register addresses from 16h to 1Eh (PWM registers).

MASTER	START	CHIP ADDR = 32H	WRITE		REG ADDR		DATA		DATA		STOP
LP8501				ACK		ACK		ACK		ACK	

Copyright © 2008–2013, Texas Instruments Incorporated

LP8501 Registers

The LP8501 is controlled by a set of registers through the two-wire serial interface port. Some register bits are reserved for future use. The table below lists device registers, their addresses, and their abbreviations. A more detailed description is given in section.

Table 5. Control Register Map

Hex Address	Register Name	Bit(s)	Read/Write	Default Value After Reset	Bit Mnemonic and Description
00	ENABLE / ENGINE CNTRL1	[6]	R/W	x0xxxxxx	CHIP_EN 0 = LP8501 not enabled 1 = LP8501 enabled
		[5:4]	R/W	xx00xxxx	ENGINE1_EXEC Engine 1 program execution control
		[3:2]	R/W	xxxx00xx	ENGINE2_EXEC Engine 2 program execution control
		[1:0]	R/W	xxxxxx00	ENGINE3_EXEC Engine 3 program execution control
01	ENGINE CNTRL2	[5:4]	R/W	xx00xxxx	ENGINE1_MODE ENGINE 1 mode control
		[3:2]	R/W	xxxx00xx	ENGINE2_MODE ENGINE 2 mode control
		[1:0]	R/W	xxxxxx00	ENGINE3_MODE ENGINE 3 mode control
02	GROUP 1 FADING	[7:4]	R/W	0000xxxx	FADE_IN Fade-in time for group 1 fader
		[3:0]	R/W	xxxx0000	FADE_OUT Fade-in time for group 1 fader
03	GROUP 2 FADING	[7:4	R/W	0000xxxx	FADE_IN Fade-in time for group 2 fader
		[3:0]	R/W	xxxx0000	FADE_OUT Fade-in time for group 2 fader
04	GROUP 3 FADING	[7:4	R/W	0000xxxx	FADE_IN Fade-in time for group 3 fader
		[3:0]	R/W	xxxx0000	FADE_OUT Fade-in time for group 3 fader
05	POWER CONFIG	[1]	R/W	xxxxxx0x	CHP_CON_1_6 D1 to D6 power selection
		[0]	R/W	xxxxxxx0	CHP_CON_7_9 D7 to D9 power selection
06	D1 CONTROL	[7:6]	R/W	00xxxxxx	GROUP_SELECT Fader group selection for D1 output
		[5]	R/W	xx0xxxxx	LOG_EN Logarithmic dimming control for D1
07	D2 CONTROL	[7:6]	R/W	00xxxxxx	GROUP_SELECT Fader group selection for D2 output
		[5]	R/W	xx0xxxxx	Logarithmic dimming control for D2 output
08	D3 CONTROL	[7:6]	R/W	00xxxxxx	GROUP_SELECT Fader group selection for D3 output
		[5]	R/W	xx0xxxxx	LOG_EN Logarithmic dimming control for D3 output
09	D4 CONTROL	[7:6]	R/W	00xxxxxx	GROUP_SELECT Fader group selection for D4 output
		[5]	R/W	xx0xxxxx	LOG_EN Logarithmic dimming control for D4 output
0A	D5 CONTROL	[7:6]	R/W	00xxxxxx	GROUP_SELECT Fader group selection for D5 output
		[5]	R/W	xx0xxxxx	LOG_EN Logarithmic dimming control for D5 output

Copyright © 2008–2013, Texas Instruments Incorporated

Table 5. Control Register Map (continued)

Hex Address	Register Name	Bit(s)	Read/Write	Default Value After Reset	Bit Mnemonic and Description
0B	D6 CONTROL	[7:6]	R/W	00xxxxxx	GROUP_SELECT Fader group selection for D6 output
		[5]	R/W	xx0xxxxx	LOG_EN Logarithmic dimming control for D6 output
0C	D7 CONTROL	[7:6]	R/W	00xxxxxx	GROUP_SELECT Fader group selection for D7 output
		[5]	R/W	xx0xxxxx	LOG_EN Logarithmic dimming control for D7 output
0D	D8 CONTROL	[7:6]	R/W	00xxxxxx	GROUP_SELECT Fader group selection for D8 output
		[5]	R/W	xx0xxxxx	LOG_EN Logarithmic dimming control for D8 output
0E	D9 CONTROL	[7:6]	R/W	00xxxxxx	GROUP_SELECT Fader group selection for D9 output
		[5]	R/W	xx0xxxxx	LOG_EN Logarithmic dimming control for D9 output
0F TO 14	RESERVED	[7:0]			RESERVED FOR FUTURE USE
15	GPO CONTROL	[7:6]	R/W	00xxxxxx	GROUP_SELECT Fader group selection for GPO
		[5]	R/W	xx0xxxxx	LOG_EN Logarithmic dimming control for GPO
16	D1 PWM	[7:0]	R/W	00000000	PWM PWM duty cycle control for D1
17	D2 PWM	[7:0]	R/W	00000000	PWM PWM duty cycle control for D2
18	D3 PWM	[7:0]	R/W	00000000	PWM PWM duty cycle control for D3
19	D4 PWM	[7:0]	R/W	00000000	PWM PWM duty cycle control for D4
1A	D5 PWM	[7:0]	R/W	00000000	PWM PWM duty cycle control for D5
1B	D6 PWM	[7:0]	R/W	00000000	PWM PWM duty cycle control for D6
1C	D7 PWM	[7:0]	R/W	00000000	PWM PWM duty cycle control for D7
1D	D8 PWM	[7:0]	R/W	00000000	PWM PWM duty cycle control for D8
1E	D9 PWM	[7:0]	R/W	00000000	PWM PWM duty cycle control for D9
1F TO 24	RESERVED	[7:0]			RESERVED FOR FUTURE USE
25	GPO PWM	[7:0]	R/W	00000000	PWM PWM duty cycle control for GPO
26	D1 CURRENT CONTROL	[7:0]	R/W	10101111	CURRENT D1 output current control register. Default 17.5 mA (typ.)
27	D2 CURRENT CONTROL	[7:0]	R/W	10101111	CURRENT D2 output current control register. Default 17.5 mA (typ.)
28	D3 CURRENT CONTROL	[7:0]	R/W	10101111	CURRENT D3 output current control register. Default 17.5 mA (typ.)
29	D4 CURRENT CONTROL	[7:0]	R/W	10101111	CURRENT D4 output current control register. Default current is 17.5 mA (typ.)

Copyright © 2008–2013, Texas Instruments Incorporated

Table 5. Control Register Map (continued)

Hex Address	Register Name	Bit(s)	Read/Write	Default Value After Reset	Bit Mnemonic and Description
2A	D5 CURRENT CONTROL	[7:0]	R/W	10101111	CURRENT D5 output current control register. Default current is 17.5 mA (typ.)
2B	D6 CURRENT CONTROL	[7:0]	R/W	10101111	CURRENT D6 output current control register. Default current is 17.5 mA (typ.)
2C	D7 CURRENT CONTROL	[7:0]	R/W	10101111	CURRENT D7 output current control register. Default current is 17.5 mA (typ.)
2D	D8 CURRENT CONTROL	[7:0]	R/W	10101111	CURRENT D8 output current control register. Default current is 17.5 mA (typ.)
2E	D9 CURRENT CONTROL	[7:0]	R/W	10101111	CURRENT D9 output current control register. Default current is 17.5 mA (typ.)
2F TO 35	RESERVED FOR FUTURE USE	[7:0]			RESERVED FOR FUTURE USE
36	CONFIG	[7]	R/W	0xxxxx0x	PWM_POWERSAVE Enables PWM powersave option
		[6]	R/W	x1xxxx0x	EN_AUTO_INCR Serial bus address auto increment enable
		[5]	R/W	xx0xxx0x	POWERSAVE_EN Powersave mode enable
		[4:3]	R/W	xxx00x0x	CP_MODE Charge pump gain selection
		[2]	R/W	xxxxx00x	FADE_TO_OFF Automatic fade out enable
		[1]	R/W	xxxxxx0x	RESERVED **Note** that this bit should always be set to zero when writing register.
		[0]	R/W	xxxxxx00	INT_CLK_EN LED Clock source selection
37	ENGINE1 PC	[6:0]	R/W	x0000000	PC Program counter for engine 1
38	ENGINE2 PC	[6:0]	R/W	x0000000	PC Program counter for engine 2
39	ENGINE3 PC	[6:0]	R/W	x0000000	PC Program counter for engine 3
3A	STATUS/INTERRUPT	[7]	R	0xxxxxxx	LED_TEST_MEASUREMENT_DONE Indicates when the LED test measurement is done.
		[6]	R	x1xxxxxx	MASK_BUSY Mask bit for interrupt generated by START_UP BUSY or ENGINE_BUSY
		[5]	R	xx0xxxxx	START_UP BUSY This bit indicates that the start-up sequence is running
		[4]	R	xxx0xxxx	ENGINE_BUSY This bit indicates that a program execution engine is clearing internal registers
		[3]	R	xxxx0xxx	EXT_CLK_USED Indicates when external clock signal bit is set
		[2]	R	xxxxx0xx	ENG1_INT Interrupt bit for program execution engine 1
		[1]	R	xxxxxx0x	ENG2_INT Interrupt bit for program execution engine 2
		[0]	R	xxxxxxx0	ENG3_INT Interrupt bit for program execution engine 3

Copyright © 2008–2013, Texas Instruments Incorporated

Table 5. Control Register Map (continued)

Hex Address	Register Name	Bit(s)	Read/Write	Default Value After Reset	Bit Mnemonic and Description
3B	GPO	[2]	R/W	xxxxx0xx	INT_CONF INT pin can be configured to function as a GPO with this bit.
		[1]	R/W	xxxxxx0x	GPO GPO pin control
		[0]	R/W	xxxxxxx0	INT_GPO GPO pin control for INT pin (when INT_CONF is set to '1')
3D	RESET	[7:0]	R/W	00000000	RESET Writing 11111111 into this register resets the LP8501
41	LED TEST CONTROL	[7]	R/W	0xxxxxxx	EN_LED_TEST_ADC
		[6]	R/W	x0xxxxxx	EN_LED_TEST_INT
		[5]	R/W	xx0xxxxx	LED_TEST_CONTINUOUS_CONV Continuous LED test measurement selection
		[4:0]	R/W	xxx00000	LED_TEST_CTRL Control bits for LED test
42	LED TEST ADC	[7:0]	R	N/A	LED_TEST_ADC LED test result
48	GROUP FADER1	[7:0]	R/W	00000000	GROUP FADER
49	GROUP FADER2	[7:0]	R/W	00000000	GROUP FADER
4A	GROUP FADER3	[7:0]	R/W	00000000	GROUP FADER
4C	ENG1 PROG START ADDR	[6:0]	R/W	x0000000	ADDR
4D	ENG2 PROG START ADDR	[6:0]	R/W	x0001000	ADDR
4E	ENG3 PROG START ADDR	[6:0]	R/W	x0010000	ADDR
4F	PROG MEM PAGE SEL	[2:0]	R/W	xxxxx000	PAGE_SEL

Copyright © 2008–2013, Texas Instruments Incorporated

Table 5. Control Register Map (continued)

Hex Address	Register Name	Bit(s)	Read/Write	Default Value After Reset	Bit Mnemonic and Description
50	PROGRAM MEMORY 00h/10h/20h/30h/40h/50h	[15:8]	R/W	00000000	CMD Every Instruction is 16-bit wide. The LP8501 can store 96 instructions. Each instruction consists of 16 bits. Because one register has only 8 bits, one instruction requires two register addresses. In order to reduce program load time the LP8501 supports address auto-incrementation. Register address is incremented after each 8 data bits. Thus the whole program memory page can be written in one serial bus write sequence.
51		[7:0]	R/W	00000000	
52	PROGRAM MEMORY 01h/11h/21h/31h/41h/51h	[15:8]	R/W	00000000	
53		[7:0]	R/W	00000000	
54	PROGRAM MEMORY 02h/12h/22h/32h/42h/52h	[15:8]	R/W	00000000	
55		[7:0]	R/W	00000000	
56	PROGRAM MEMORY 03h/13h/23h/33h/43h/53h	[15:8]	R/W	00000000	
57		[7:0]	R/W	00000000	
58	PROGRAM MEMORY 04h/14h/24h/34h/44h/54h	[15:8]	R/W	00000000	
59		[7:0]	R/W	00000000	
5A	PROGRAM MEMORY 05h/15h/25h/35h/45h/55h	[15:8]	R/W	00000000	
5B		[7:0]	R/W	00000000	
5C	PROGRAM MEMORY 06h/16h/26h/36h/46h/56h	[15:8]	R/W	00000000	
5D		[7:0]	R/W	00000000	
5E	PROGRAM MEMORY 07H/17H/27H/37H/47H/57H	[15:8]	R/W	00000000	
5F		[7:0]	R/W	00000000	
60	PROGRAM MEMORY 08h/18h/28h/38h/48h/58h	[15:8]	R/W	00000000	
61		[7:0]	R/W	00000000	
62	PROGRAM MEMORY 09h/19h/29h/39h/49h/59h	[15:8]	R/W	00000000	
63		[7:0]	R/W	00000000	
64	PROGRAM MEMORY 0Ah/1Ah/2Ah/3Ah/4Ah/5Ah	[15:8]	R/W	00000000	
65		[7:0]	R/W	00000000	
66	PROGRAM MEMORY 0Bh/1Bh/2Bh/3Bh/4Bh/5Bh	[15:8]	R/W	00000000	
67		[7:0]	R/W	00000000	
68	PROGRAM MEMORY 0Ch/1Ch/2Ch/3Ch/4Ch/5Ch	[15:8]	R/W	00000000	
69		[7:0]	R/W	00000000	
6A	PROGRAM MEMORY 0Dh/1Dh/2Dh/3Dh/4Dh/5Dh	[15:8]	R/W	00000000	
6B		[7:0]	R/W	00000000	
6C	PROGRAM MEMORY 0Eh/1Eh/2Eh/3Eh/4Eh/5Eh	[15:8]	R/W	00000000	
6D		[7:0]	R/W	00000000	
6E	PROGRAM MEMORY 0FH/1FH/2FH/3FH/4FH/5FH	[15:8]	R/W	00000000	
6F		[7:0]	R/W	00000000	
76	GAIN CHANGE CONTROL	[7:6]	R/W	000xxxxx	THRESHOLD Threshold voltage (typ.) 00 — 400 mV 01 — 300 mV 10 — 200 mV 11 — 100 mV
		[5]	R/W	xx0xxxxx	RESERVED BIT When writing to register, write always '0'
		[4:3]	R/W	xx000xxx	TIMER 00 — 5 ms 01 — 10 ms 10 — 50 ms 11 — infinite
		[2]	R/W	xx0xx0xx	FORCE_1x Activates 1.5x to 1x timer

Copyright © 2008–2013, Texas Instruments Incorporated

LP8501 Control Register Details

00 ENABLE/ ENGINE CONTROL1

- **00 - Bit [6] CHIP_EN**
  - 1 = internal startup sequence powers up all the needed internal blocks and the device enters normal mode
  - 0 = standby mode is entered. Control registers can be written or read (writing into PWM and Channel1–3 PC registers and to register 00h ENGINE1–3_EXEC bits is not possible).
- **00 — Bits [5:4] ENGINE1_EXEC**
  - Engine 1 program execution control. Execution register bits define how the program is executed. Program start address can be programmed to Program Counter (PC) register 37h.
  - 00 = Hold: Hold causes the execution engine to finish the current instruction and then stop. Program counter (PC) can be read or written only in this mode.
  - 01 = Step: Execute the instruction at the location pointed by the PC, increment the PC by one and then reset ENG1_EXEC bits to 00 (i.e. enter *hold*).
  - 10 = Free Run: Start program execution from the instruction pointed by the PC.
  - 11 = Execute Once: Execute the instruction pointed by the current PC value and reset ENG1_EXEC to 00 (i.e. enter *hold*). The difference between *step* and *executeonce* is that *executeonce* does not increment the PC.
- **00 — Bits [3:2] ENGINE2_EXEC**
  - Engine 2 program execution control. Equivalent to above definition of control bits. Program start address can be programmed to Program Counter (PC) register 38h.
- **00 — Bits [1:0] ENGINE3_EXEC**
  - Engine 3 program execution control. Equivalent to engine 1 control bits. Program start address can be programmed to Program Counter (PC) register 39h.

01 ENGINE CONTROL2

- Operation modes are defined in this register.
  - **Disabled**: Engines can be configured to *disabled mode* separately.
  - **Load Program**: Writing to program memory is allowed only when the engine is in *load program* operation mode and engine busy bit (3Ah) is not set. Serial bus master should check the busy bit before writing to program memory. All the three engines are in hold while one or more engines are in *load program* mode. PWM values are frozen, also. Program execution continues when all the engines are out of *load program* mode. *Load program* mode resets the program counter of the respective engine. *Loadprogram* mode can be entered from the *disabledmode* only. Entering *loadprogram* mode from the *runprogram* mode is not allowed.
  - **Run Program**: *Run program* mode executes the instructions stored in the program memory. Execution register (ENG1_EXEC etc.) bits define how the program is executed (*hold*, *step*, *freerun* or *executeonce*). Program start address can be programmed to Program Counter (PC) register. The Program Counter is reset to zero when the PC's upper limit value is reached.
  - **Halt**: Instruction execution aborts immediately and engine operation halts.
- **01 — Bit [5:4] ENGINE1_MODE**
  - 00 = disabled
  - 01 = load program to SRAM, reset engine 1 PC
  - 10 = run program as defined by ENGINE1_EXEC bits
  - 11 = halt, halts program execution. Current command execution stopped
- **01 — Bits [3:2] ENGINE2_MODE**
  - 00 = disabled
  - 01 = load program to SRAM, reset engine 2 PC
  - 10 = run program as defined by ENGINE2_EXEC bits
  - 11 = halt, halts program execution. Current command execution stopped
- **01 — Bits [1:0] ENGINE3_MODE**
  - 00 = disabled
  - 01 = load program to SRAM, reset engine 3 PC

Copyright © 2008–2013, Texas Instruments Incorporated

  - 10 = run program as defined by ENGINE3_EXEC bits
  - 11 = halt, halts program execution. Current command execution stopped
- Note that changing mode from Run to Load is not allowed. Preferred sequence is 10 –> 00 –> 01.

02 GROUP 1 FADING

- This is the register used to assign fade-in and fade-out times for group 1. Time can be set with 4 bits.
- **02 — Bits [7:4] FADE_IN**
- **02 — Bits [3:0] FADE_OUT**

FADE_IN/FADE_OUT	Time, s
0000	0.0
0001	0.05
0010	0.1
0011	0.2
0100	0.3
0101	0.4
0110	0.5
0111	0.6
1000	0.7
1001	0.8
1010	0.9
1011	1.0
1100	1.5
1101	2.0
1110	3.0
1111	4.0

03 GROUP 2 FADING

- See GROUP 1 FADING

04 GROUP 3 FADING

- See GROUP 1 FADING

05 POWER CONFIG

- **05 — Bit [0] CHP_CON_7_9**
  - 1 = VDD7_9 should be connected to V_{OUT}
  - 0 = VDD7_9 should be connected to V_{DD}
- **05 — Bit [1] CHP_CON_1_6**
  - 1 = VDD1_6 should be connected to V_{OUT}
  - 0 = VDD1_6 should be connected to V_{DD}

06 D1 CONTROL

- This is the register used to assign the D1 output to the GROUP FADER group 1, 2, or 3, or none of them. This register selects between linear and logarithmic PWM brightness adjustment. By using logarithmic PWM scale the visual effect looks like linear. Logarithmic adjustment converts internally an 8-bit PWM value to a logarithmic 12-bit value.
- **06 — Bit [7:6] GROUP_SELECT**
  - 00 = No group fader set, clears group fader set for D1. Default setting.
  - 01 = Fader group 1 controls the D1 driver. The user can set the overall output of the group by the GROUP 1 FADER register at the address 48h and the fade-in/fade-out time by the GROUP 1 FADING register at the address 02h.
  - 10 = Fader group 2 controls the D1 driver. The user can set the overall output of the group by the GROUP 2 FADER register at the address 49h and the fade-in/fade-out time by the GROUP 2 FADING register at the address 03h.

Copyright © 2008–2013, Texas Instruments Incorporated

– 11 = Fader group 3 controls the D1 driver. The user can set the overall output of the group by the GROUP 3 FADER register at the address 4Ah and the fade-in/fade-out time by the GROUP 3 FADING register at the address 04h.

- **06 — Bit [5] LOG_EN**
  - 0 = linear adjustment.
  - 1 = logarithmic adjustment.
  - This bit is effective for both the program execution engine control and direct PWM control.

07 D2 CONTROL to 0E D9 CONTROL

- The control registers and control bits for D2 output to D9 output are similar to that given to D1.

15 GPO CONTROL

- The control register and control bits for GPO output are similar to that given to D1.

16 D1 PWM

- This is the PWM duty cycle control for D1 output. D1 PWM register is effective during direct control operation - direct PWM control is active after power up by default. Note: serial bus address auto increment is not supported for register addresses from 16 to 1E.
- **16 — Bits [7:0] PWM**
  - 16 - Bits [7:0] PWM These bits set the D1 output PWM as shown in Figure 29 below.

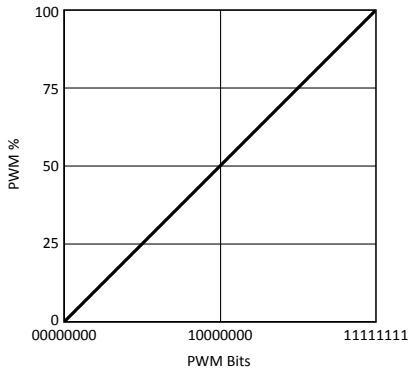


Figure 29.

17 D2 PWM to 1E D9 PWM

- PWM duty cycle control for outputs D2 to D9. The control registers and control bits for D2 output to D9 output are similar to that given to D1.

25 GPO PWM

- PWM duty cycle control for GPO. The control register and control bits for GPO are similar to that given to D1.

26 D1 OUTPUT CURRENT CONTROL

- D1 LED driver current control register. The resolution is 8-bits and step size is 100 µA. .

CURRENT bits	Output Current
00000000	0.0 mA
00000001	0.1 mA
00000010	0.2 mA
...	...
10101111	17.5 mA default setting
....	....
11111110	25.4 mA
11111111	25.5 mA

Copyright © 2008–2013, Texas Instruments Incorporated

27 D2 CURRENT CONTROL to 2E D9 CURRENT CONTROL

- The control registers and control bits for D2 output up to D9 output are similar to that given to D1 output.

36 CONFIG

- This register contains miscellaneous control bits.
- **36 — Bit [7] PWM_POWERSAVE**
  - 1 = PWM powersave ON
  - 0 = PWM powersave OFF
  - See the Power Saving section for further details.
- **36 — Bit [6] EN_AUTO_INCR**
  - The automatic increment feature of the serial bus address enables a quick memory write of successive registers within one transmission.
  - 1 = serial bus address automatic increment is enabled.
  - 0 = serial bus address automatic increment is disabled.
- **36 — Bit [5] POWERSAVE_EN**
  - 1 = power save mode is enabled.
  - 0 = power save mode is disabled. See the Power Saving section for further details.
- **36 — Bits [4:3] CP_MODE**
  - Charge pump operation mode
  - 00 = OFF
  - 01 = forced to bypass mode (1x)
  - 10 = forced to 1.5x mode; output voltage is boosted to 4.5V.
  - 11 = automatic mode selection
- **36 — Bit [2] FADE_TO_OFF**
  - Enables group fading when device is shut down through CHIP_EN.
  - 1 = Group fading ON.
  - 0 = Group fading OFF.
- **36 — Bit [1] RESERVED**
  - This bit is reserved and should be written to zero.
- **36 — Bits [0] Clock selection bit**
  - Program execution is clocked with internal 32 kHz clock or with external clock. Clocking is controlled with bits [1:0] n the following way:
  - 0 = external clock source (CLK pin)
  - 1 = internal clock
  - External clock can be used if a clock signal is present on CLK-pin. External clock frequency must be 32 kHz for correct operation. If a higher or a lower frequency is used, it will affect on the program engine operation speed.
  - If external clock is not used in the application, CLK pin should be connected to GND to avoid oscillation on this pin and extra current consumption.

37 ENGINE1 PC

- **37 — Bits [6:0] PC**
  - Program counter starting value for program execution engine 1; A value from 0000000 to 1100000. The maximum value depends on program memory allocation between the three program execution engines.

38 ENGINE2 PC

- **38 — Bits [6:0] PC**
  - Program counter starting value for program execution engine 2; A value from 0000000 to 1100000.

39 ENGINE3 PC

- **39 — Bits [6:0] PC**
  - Program counter starting value for program execution engine 3; A value from 0000000 to 1100000.

3A STATUS/INTERRUPT

Copyright © 2008–2013, Texas Instruments Incorporated

- **3A — Bit [7] LED_TEST_MEASUREMENT_DONE**
  - This bit indicates when the LED test is done, and the result is written to the LED TEST ADC register. Typically the conversion takes 2.7 milliseconds to complete.
  - 1 = LED test done
  - 0 = LED test not done
  - This bit is a read-only bit, and it is cleared (to “0”) automatically after a read operation.
- **3A — Bit [6] MASK_BUSY**
  - Mask bit for interrupts generated by STARTUP_BUSY or ENGINE_BUSY.
  - 1 = Interrupt events will be masked i.e. no external interrupt will be generated from STARTUP_BUSY or ENGINE_BUSY event (default).
  - 0 = External interrupt will be generated when STARTUP_BUSY or ENGINE_BUSY condition is no longer true. Reading the register 3Ah clears the status bits [5:4] and releases INT pin to high state.
- **3A — Bit [5] STARTUP_BUSY**
  - A status bit which indicates that the device is running the internal start-up sequence. See Modes of Operation for details.
  - 1 = internal start-up sequence running. Note: STARTUP_BUSY = 1 always when CHIP_EN bit is '0'
  - 0 = internal start-up sequence completed
- **3A — Bit[4] ENGINE_BUSY**
  - A status bit which indicates that a program execution engine is clearing internal registers. Serial bus master should not write or read program memory or registers 00h, 01h, 37h to 39h or 4Ch to 4Eh, when this bit is set to '1'.
  - 1 = at least one of the engines is clearing internal registers
  - 0 = engine ready
- **3A — Bit [3] EXT_CLK_USED**
  - 1 = external clock bit is set
  - 0 = external clock bit is not set
  - This bit is high when external clock signal on CLK pin is set from register. Does not detect automatically the external clock, only the bit selection from register 36h.
- **3A — Bits [2:0] ENG1_INT, ENG2_INT, ENG3_INT**
  - 1 = interrupt set
  - 0 = interrupt not set/clear
  - Interrupt bits for program execution engine 1, 2 and 3, respectively. These bits are set by END instruction. Reading the interrupt bit clears the interrupt.

3B GPO

- LP8501 has one General Purpose Output pin (GPO). Status of the pin can be controlled with this register. Also, INT pin can be configured to function as a GPO by setting the bit INT_CONF. When INT is configured to function as a GPO, output level is defined by the V_{DD} voltage.
- **3B — Bit [2] INT_CONF**
  - 1 = INT pin is set to function as an interrupt pin (default).
  - 0 = INT pin is configured to function as a GPO.
- **3B — Bit [1] GPO**
  - 0 =GPO pin state is low.
  - 1 = GPO pin state is high.
  - GPO pins are digital CMOS outputs, and no pull-up/down resistors are needed.
- **3B — Bit [0] GPO_INT**
  - 0 = INT pin state is low (if INT_CONF = 1).
  - 1 = INT pin state is high (if INT_CONF = 1).
  - When INT pin’s GPO function is disabled, it operates as an open drain pin. INT signal is active low, i.e. when interrupt signal is send, the pin is pulled to GND. External pull-up resistor is needed for proper functionality.

3D RESET

Copyright © 2008–2013, Texas Instruments Incorporated

- **3D — Bits [7:0] RESET**
  - Writing 11111111 into this register resets the LP8501. Internal registers are reset to the default values. Reading RESET register returns 00000000.

41 LED TEST CONTROL

- LED test control register
- **41 — Bit [7] EN_LEDTEST_ADC**
  - Writing this bit high (1) starts single LED test conversation. LED test measurement cycle is 2.7 milliseconds.
- **41 — Bit [6] EN_LEDTEST_INT**
  - 1 = interrupt signal will be send to the INT pin when the LED test is accomplished.
  - 0 = no interrupt signal will be send to the INT pin when the LED test is accomplished.
  - Interrupt can be cleared by reading STATUS/INTERRUPT register 3Ah.
- **41 — Bit [5] CONTINUOUS_CONV**
  - 1 = Continuous LED test measurement. Not active in powersave mode.
  - 0 = Continuous conversion is disabled.
- **41 — Bits [4:0] LED__TEST_CTRL**
  - These bits are used for choosing the LED driver output to be measured. V_{DD}, INT-pin and charge-pump output voltage can also be measured.

LED_TEST_CTRL bits	Measurement
00000	D1
00001	D2
00010	D3
00011	D4
00100	D5
00101	D6
00110	D7
000111	D8
01000	D9
01001 to 01110	Reserved
01111	V_{OUT}
10000	V_{DD}
10001	INT-pin voltage
10010	VDD1_6
10011	VDD7_9
10010 to 11111	N/A

42 LED TEST ADC

- **42 — Bits [7:0} LED_TEST_ADC**
  - This is used to store the LED test result. Read-only register. LED test ADC least significant bit corresponds to 30 mV. The measured voltage V (typ.) is calculated as follows: V = (RESULT(DEC) x 0.03 -1.478 V. For example, if the result is 10100110 = 166(DEC), the measured voltage is 3.50V (typ.). See Figure 30 below.

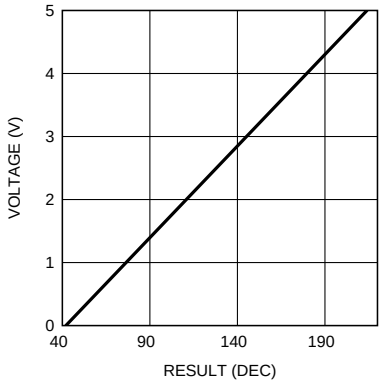


Figure 30.

48 GROUP FADER1

- **48 — Bits [7:0] GROUP_FADER**
  - An 8-bit register to control all the LED-drivers mapped to GROUP FADER1. Group fader allows the user to control dimming of multiple LEDs with a single serial bus write. This is a faster method to control the dimming of multiple LEDs compared to the dimming done with the PWM registers (address 16h to 1Eh), which would need multiple writes.

49 GROUP FADER2

- **49 — Bits [7:0] GROUP_FADER**
  - See GROUP FADER1 description.

4A GROUP FADER3

- **4A — Bits [7:0]GROUP_FADER**
  - See GROUP FADER1 description.

4C ENGINE1 PROG START ADDR

- Program memory allocation for program execution engines is defined with PROG START ADDR registers.
- **4C — Bits [6:0] — ADDR**
  - Engine 1 program start address.

4D ENG2 PROG START ADDR

- **4D — Bits [6:0] — ADDR**
  - Engine 2 program start address.

4E ENG3 PROG START ADDR

- **4E — Bits [6:0] — ADDR**
  - Engine 3 program start address.

4F PROG MEM PAGE SELECT

- **4F — Bits [2:0] — PAGE_SEL**
  - These bits select the program memory page. The program memory is divided into six pages of 16 instructions; thus the total amount of the program memory is 96 instructions.

76 — GAIN CHANGE CONTROL

Note that these controls have effect only in automatic mode.

- **76 — Bits [7:6] — THRESHOLD**
  - Threshold voltage (typ.) pre-setting. Bits set the threshold voltage at which the charge pump gain changes from 1.5x to 1x. The threshold voltage is defined as the voltage difference between highest voltage output (D1 to D6) and input voltage V_{DD} : $V_{THRESHOLD}$ = V_{DD} — MAX (voltage on D1 to D6).
  - If $V_{THRESHOLD}$ is larger than the set value (100 mV to 400 mV), the charge pump is in 1x mode.
  - 00 = 400 mV

Copyright © 2008–2013, Texas Instruments Incorporated

- 01 = 300 mV
- 10 = 200 mV
- 11 = 100 mV
- Note: Values above are typical and should not be used as product specification.
- Note: Writing to THRESHOLD [7:6] bits by the user overrides factory settings. Factory settings are not user accessible.
- **76 — Bit [5] — RESERVED**
  - This bit is reserved for future use. When writing to register 76h, this bit should be written '0'.
- **76 — Bits [4:3] — TIMER**
  - Automatic mode change from 1.5x to 1x is attempted at the interval specified with these bits. After the specified interval time mode change to 1x is allowed if there is enough voltage over the LED drivers to ensure proper operation. If FORCE_1x is set to '1' after the specified interval time 1x mode is always tested.
  - 00 = 5 ms
  - 01 = 10 ms
  - 10 = 50 ms
  - 11 = infinite. The charge pump switches gain from 1x mode to 1.5x mode only. The gain reset back to 1x is enabled under certain conditions, for example in the powersave mode.
- **76 — Bit [2] — FORCE_1x**
  - Activates forced mode change. In forced mode charge pump mode change from 1.5x to 1x is attempted at the interval specified with the TIMER bits.
  - 1 = forced mode changes enabled
  - 0 = forced mode changes disabled

Copyright © 2008–2013, Texas Instruments Incorporated

APPLICATIONS INFORMATION

Recommended External Components

The LP8501 requires 4 external capacitors for proper operation. Surface-mount multi-layer ceramic capacitors are recommended. Tantalum and aluminium capacitors are not recommended because of their high ESR. For the flying capacitors (C1 and C2) multi-layer ceramic capacitors should always be used. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR <20 mΩ typ.). Ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LP8501. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over −55°C to 125°C; X5R: ±15% over −55°C to 85°C). Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LP8501. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, −20%) and vary significantly over temperature (Y5V: +22%, -82% over −30°C to +85°C range; Z5U: +22%, −56% over +10°C to +85°C range). Under some conditions, a nominal 1 µF Y5V or Z5U capacitor could have a capacitance of only 0.1µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LP8501.

For proper operation it is necessary to have at least 0.24 µF of effective capacitance for each of the flying capacitors under all operating conditions. The output capacitor C_{OUT} directly affects the magnitude of the output ripple voltage. In general, the higher the value of C_{OUT}, the lower the output ripples magnitude. For proper operation it is necessary to have at least 0.50 µF of effective capacitance for C_{IN} and C_{OUT} under all operating conditions. The voltage rating of all four capacitors should be 6.3V; 10V is recommended.

The table below lists recommended external components from some leading ceramic capacitor manufacturers. It is strongly recommended that the LP8501 circuit be thoroughly evaluated early in the design-in process with the mass-production capacitors of choice. This will help ensure that any variability in capacitance does not negatively impact circuit performance.

Model	Type	Vendor	Voltage Rating	Package Size
1 µF for COUT and CIN				
C1005X5R1A105K	Ceramic X5R	TDK	10V	0402
LMK105BJ105KV-F	Ceramic X5R	Taiyo Yuden	10V	0402
ECJ0EB1A105M	Ceramic X5R	Panasonic	10V	0402
ECJUVBPA105M	Ceramic X5R, array of two	Panasonic	10V	0504
470 nF for C1 and C2				
C1005X5R1A474K	Ceramic X5R	TDK	10V	0402
LMK105BJ474KV-F	Ceramic X5R	Taiyo Yuden	10V	0402
ECJ0EB0J474K	Ceramic X5R	Panasonic	6.3V	0402
LEDs		User defined.		

Copyright © 2008–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision C (May 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format; publish full data sheet to replace product brief	44

Copyright © 2008–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8501TME/NOPB	ACTIVE	DSBGA	YFQ	25	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 85	8501	Samples
LP8501TMX/NOPB	ACTIVE	DSBGA	YFQ	25	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 85	8501	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

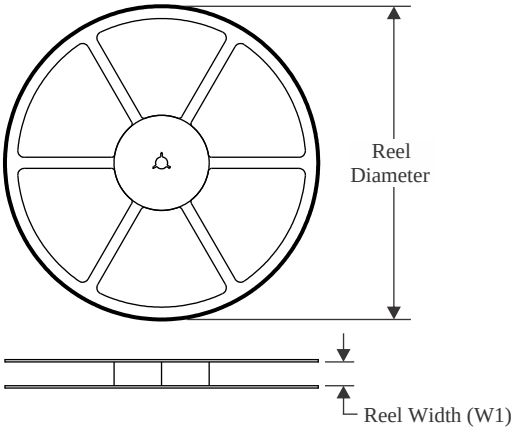
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

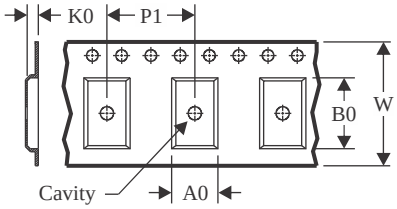
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

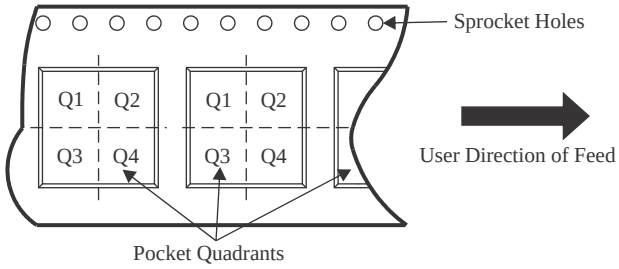


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

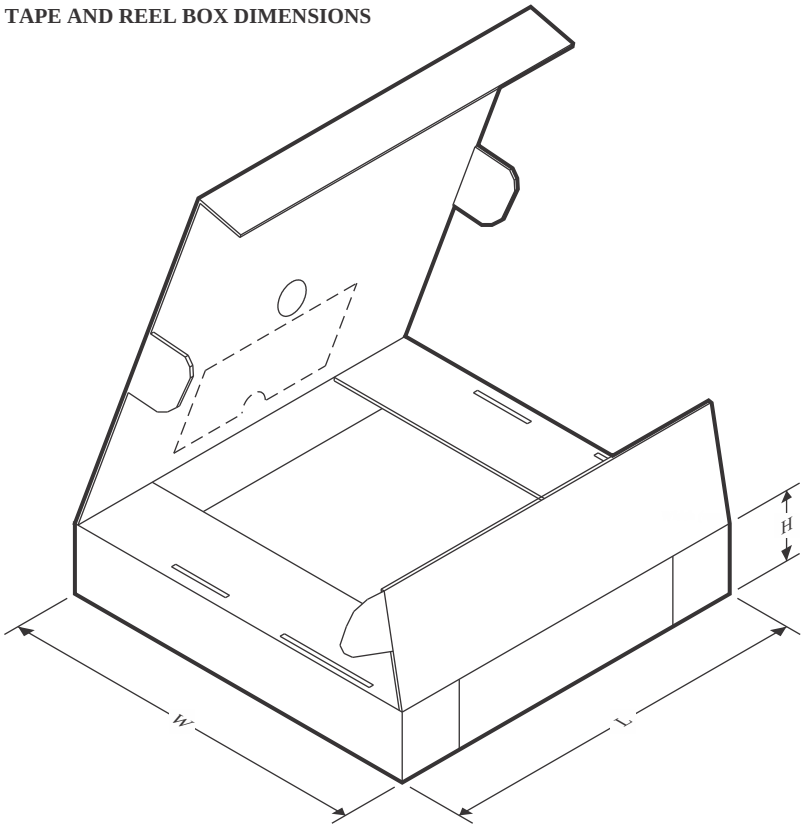
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8501TME/NOPB	DSBGA	YFQ	25	250	178.0	8.4	2.43	2.48	0.75	4.0	8.0	Q1
LP8501TMX/NOPB	DSBGA	YFQ	25	3000	178.0	8.4	2.43	2.48	0.75	4.0	8.0	Q1

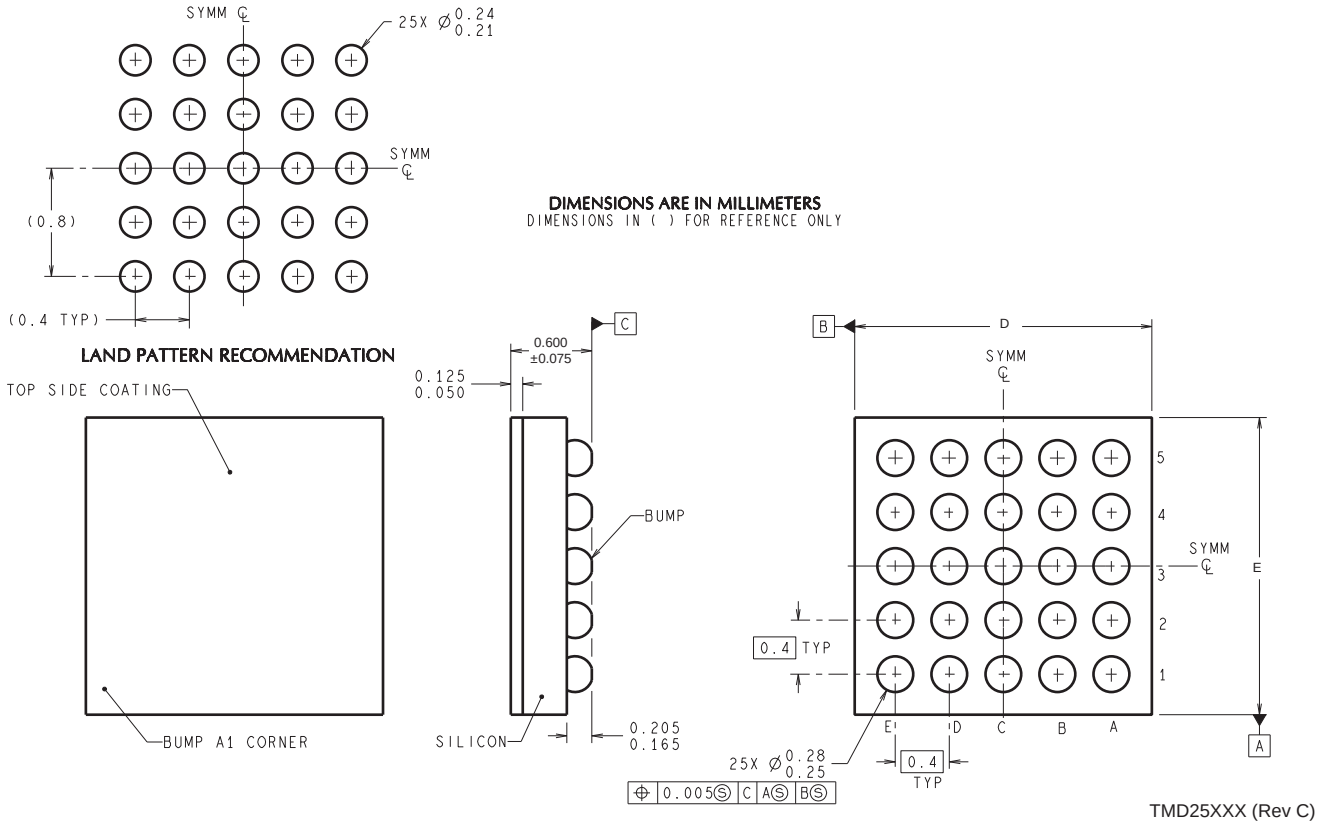
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8501TME/NOPB	DSBGA	YFQ	25	250	208.0	191.0	35.0
LP8501TMX/NOPB	DSBGA	YFQ	25	3000	208.0	191.0	35.0

YFQ0025



D: Max = 2.29 mm, Min = 2.23 mm

E: Max = 2.29 mm, Min = 2.23 mm

4215084/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated