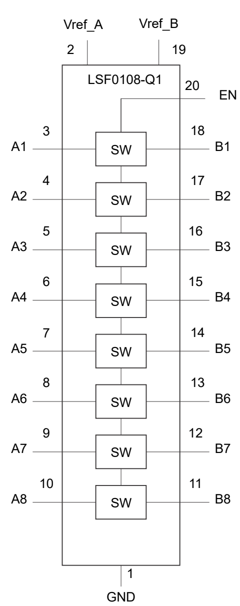
LSF0108-Q1 Automotive 8-Channel Multi-Voltage Level Translator

1 Features

- AEC-Q100 qualified with the following results:
  - Device HBM ESD classification level 2000-V
  - Device CDM ESD classification level 1000-V
- Available in wettable flank VQFN (RKS) package
- Provides bidirectional voltage translation with no direction pin
- Supports up to 100 MHz up translation and greater than 100 MHz down translation at ≤ 30-pF capacitive load and up to 40 MHz up or down translation at 50-pF capacitive load
- Supports hot insertion
- Allow bidirectional voltage level translation between
  - 0.65 V ↔ 1.8 V, 2.5 V, 3.3 V, 5 V (RKS package only)
  - 0.95 V ↔ 1.8 V, 2.5 V, 3.3 V, 5 V
  - 1.2 V ↔ 1.8 V, 2.5 V, 3.3 V, 5 V
  - 1.8 V ↔ 2.5 V, 3.3 V, 5 V
  - 2.5 V ↔ 3.3 V, 5 V
  - 3.3 V ↔ 5 V
- Low standby current
- 5-V tolerance I/O port to support TTL
- Low r_{on} provides less signal distortion
- High-impedance I/O pins for EN = low
- Flow-through pin-out for easy PCB trace routing
- Latch-up performance exceeds 100 mA per JESD 17
- –40°C to +125°C operating temperature range



Functional Block Diagram

2 Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I^2C, and other interfaces in telecom infrastructure
- Infotainment and cluster
- Body electronics and lighting
- Hybrid, electric, and powertrain systems
- Passive safety
- ADAS

3 Description

- Supports up to 100 MHz up translation and greater than 100 MHz down translation at ≦ 30 pF capacitive load and up to 40 MHz up and down translation at 50 pF capacitive load:
  - Allows the LSF family to support more consumer or telecom interfaces (MDIO or SDIO)
- Bidirectional voltage translation without DIR pin:
  - Minimizes system effort to develop voltage translation for bidirectional interface (PMBus, I^2C, or SMbus)
- 5 V tolerance on IO port and 125°C support:
  - With 5 V tolerance and 125°C support, the LSF family is flexible and compliant with TTL levels in industrial and telecom applications
- Channel specific translation:
  - The LSF family is able to set up different voltage translation levels on each channel

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LSF0108-Q1	PW (TSSOP, 20)	6.5 mm × 6.4 mm
	RKS (VQFN, 20)	4.5 mm × 2.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (June 2023) to Revision H (July 2023)	Page
• Updated *Features* section to clarify 0.65 V capability is only for RKS package	1
• Added the *Electrical Characteristics - PW Package* table	7
• Updated *Feature Description* section	12
• Added separate table for PW package in the *Enable, Disable, and Reference Voltage Guidelines* section	16

Changes from Revision F (April 2023) to Revision G (June 2023)	Page
• Added 0.65 V capability under *Features* section and throughout data sheet where voltage range is mentioned	1
• Updated the *Package Information* table to include package size	1
• Changed *pull up resistor* to *bias resistor* on description row for EN pin in *Pin Functions* table	4
• Updated the Recommended Operating Conditions table to reflect max of 5.5V	5
• Updated Thermal Information table	5
• Updated On-state resistance with 0.65V specs	6
• Changed all Switching Characteristic Table Test Conditions	8
• Updated the *Application Operating Condition* table	16

Changes from Revision E (November 2022) to Revision F (April 2023)	Page
• Changed the status of the *RKS* package from: *preview* to: *active*	1

Changes from Revision D (April 2021) to Revision E (November 2022)	Page
• Added the *Auto Bidirectional Voltage Translation*, *Output Enable*, *Wettable Flanks*, *Up and Down Translation*, *Bias Circuitry*, *Mixed-Mode Voltage Translation*, *Single Supply Translation*, and *Voltage Translation for Vref_B < Vref_A + 0.8 V* sections	1
• Added the *RKS package* to the data sheet	4
• Updated the *Overview* section	11
• Updated the *Device Functional Modes* section	13
• Updated the *Application Information* section	15
• Updated the *Enable, Disable, and Reference Voltage Guidelines* section	16
• Updated the *Pull-Up Resistor Sizing* section	17

5 Pin Configuration and Functions

All packages are on the same relative scale

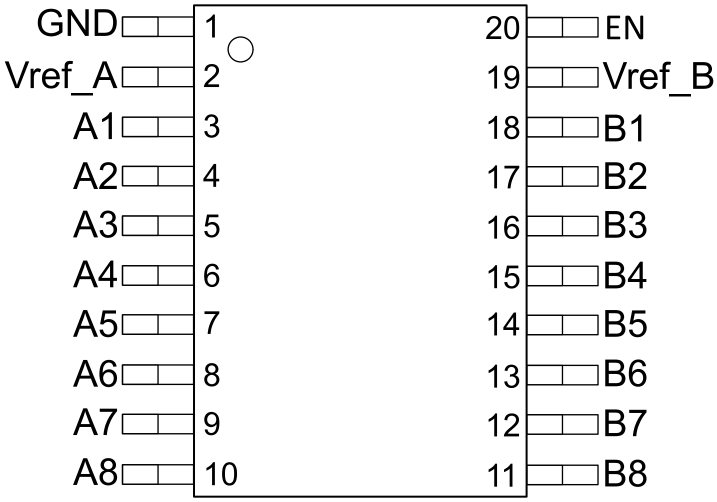


Figure 5-1. PW Package, 20-Pin TSSOP (Transparent Top View)

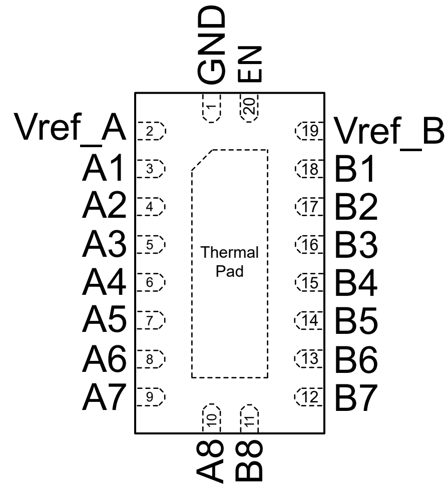


Figure 5-2. RKS Package, 20-Pin VQFN (Transparent Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A1	3	I/O	Data port
A2	4	I/O	Data port
A3	5	I/O	Data port
A4	6	I/O	Data port
A5	7	I/O	Data port
A6	8	I/O	Data port
A7	9	I/O	Data port
A8	10	I/O	Data port
B1	18	I/O	Data port
B2	17	I/O	Data port
B3	16	I/O	Data port
B4	15	I/O	Data port
B5	14	I/O	Data port
B6	13	I/O	Data port
B7	12	I/O	Data port
B8	11	I/O	Data port
EN	20	I	Switch enable input; connect to V_{ref_B} and pull-up through a bias resistor (200 kΩ).
GND	1	—	Ground
Vref_A	2	—	Reference supply voltage A. For more information, see *Application and Implementation* section.
Vref_B	19	—	Reference supply voltage B. For more information, see *Application and Implementation* section.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_I	Input voltage range [(2)]	–0.5	7	V
$V_{I/O}$	Input-output voltage range [(2)]	–0.5	7	V
	Continuous channel current		128	mA
I_{IK}	Input Clamp Current (V_I < 0)		–50	mA
$T_{J(Max)}$	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and input-output negative voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	±1000	V

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{I/O}$	Input-output voltage	A1, A2 - An, B2 - Bn	0	5.5	V
$V_{ref\_A/B/EN}$ [(1)]	Reference Voltage		0	5.5	V
EN-Switch[(2)]	Switch mode enable voltage (Switch mode enable voltage)		1.5	5.5	V
I_{PASS}	Pass switch current			64	mA
T_A	Ambient temperature		–40	125	°C

(1) **RKS package:** To support translation, V_{REF1} supports 0.65 V to V_{REF2} - 0.6 V. V_{REF2} must be between V_{REF1} + 0.6 V to 5.5 V. See Typical Application for more information. **PW package:** To support translation, V_{REF1} supports 0.85 V to V_{REF2} - 0.6 V. V_{REF2} must be between V_{REF1} + 0.6 V to 5.5 V. See Typical Application for more information.
(2) To support switching, V_{REF1} and V_{REF2} Do not need to be connected. EN pin should use a voltage not less than 1.5V when the switch mode is to be enabled. Enabled voltage on this pin should be equal to 1.5V or I/O supply voltage, whichever is higher.

6.4 Thermal Information (Q1)

THERMAL METRIC[(1)]		LSF0108-Q1		UNIT
		PW (TSSOP)	WRKS (VQFN)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.8	74.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	76.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.8	46.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.4	13.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	46.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics - RKS Package

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP [1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA	V_{EN} = 0 V		-1.2		0	V
I_{IH}	Input leakage current	V_I = 5 V, V_O = 0V	V_{EN} = 0 V		.001	0.5	3	µA
I_{CC}	Supply current	V_{ref_B} = V_{EN} = 5.5 V, V_{ref_A} = 4.5 V, I_O = 0, V_I = V_{CC} or GND			.002	.05	1.5	µA
$C_{I(EN)}$	Input capacitance	V_I = 3 V or 0 V				40		pF
$C_{IO(off)}$	Off capacitance	V_O = 3 V or 0 V	V_{EN} = 0 V			4	6	pF
$C_{IO(on)}$	On capacitance	V_O = 3 V or 0 V	V_{EN} = 3 V			10.5	12.5	pF
R_{ON} [2]	On-state resistance	V_I = 0 V, V_{ref_B} = 5 V[5]	I_O = 64 mA	V_{ref_A} = 1 V		5		Ω
				V_{ref_A} = 1.8 V		4		
				V_{ref_A} = 2.5 V		3		
				V_{ref_A} = 3.3 V		3		
			I_O = 20 mA	V_{ref_A} = 0.65 V		15		
			I_O = 32 mA	V_{ref_A} = 1 V		5		
				V_{ref_A} = 1.8 V		4		
				V_{ref_A} = 2.5 V		3		
				V_{ref_A} = 3.3 V		3		
		V_I = 1.8 V, V_{ref_B} = 5 V[5]	I_O = 15 mA	V_{ref_A} = 3.3 V		4		
		V_I = 1 V, V_{ref_B} = 3.3 V[5]	I_O = 10 mA	V_{ref_A} = 1.8 V		7		
		V_I = 0 V, V_{ref_B} = 3.3 V[5]	I_O = 10 mA	V_{ref_A} = 0.65 V		15		
				V_{ref_A} = 1 V		5		
		V_I = 0 V, V_{ref_B} = 1.8 V[5]	I_O = 10 mA	V_{ref_A} = 0.65 V		15		
				V_{ref_A} = 1 V		6		

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. Minimum ON-state resistance is determined by the lowest voltage of the two (A or B) pins.
(3) Measured in application connected current source configuration only. See Section 7

6.6 Electrical Characteristics - PW Package

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYPSection 6.6	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA	V_{EN} = 0 V		-1.2		0	V
I_{IH}	Input leakage current	V_I = 5 V, V_O = 0V	V_{EN} = 0 V				5	µA
I_{CC}	Supply current	V_{ref_B} = V_{EN} = 5.5 V, V_{ref_A} = 4.5 V, I_O = 0, V_I = V_{CC} or GND				6		µA
$C_{I(EN)}$	Input capacitance	V_I = 3 V or 0 V				40		pF
$C_{IO(off)}$	Off capacitance	V_O = 3 V or 0 V	V_{EN} = 0 V			4	6	pF
$C_{IO(on)}$	On capacitance	V_O = 3 V or 0 V	V_{EN} = 3 V			10.5	12.5	pF
R_{ON} [1]	On-state resistance	V_I = 0 V, V_{ref_B} = 5 V[5]	I_O = 64 mA	V_{ref_A} = 1 V		10		Ω
				V_{ref_A} = 1.8 V		9		
				V_{ref_A} = 3.3 V		8		
			I_O = 32 mA	V_{ref_A} = 1.8 V		10		
				V_{ref_A} = 2.5 V		15		
		V_I = 1.8 V, V_{ref_B} = 5 V[5]	I_O = 15 mA	V_{ref_A} = 3.3 V		9		
		V_I = 1 V, V_{ref_B} = 3.3 V[5]	I_O = 10 mA	V_{ref_A} = 1.8 V		18		
		V_I = 0 V, V_{ref_B} = 3.3 V[5]	I_O = 10 mA	V_{ref_A} = 1 V		20		
		V_I = 0 V, V_{ref_B} = 1.8 V[5]	I_O = 10 mA	V_{ref_A} = 1 V		30		

(1) Measured by the voltage drop between the A and B pins at the indicated current through the switch. Minimum ON-state resistance is determined by the lowest voltage of the two (A or B) pins.
(2) Measured in application connected current source configuration only. See Section 7

6.7 Switching Characteristics (Translating Down)

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PLH}	Low-to-high propagation delay	V_{CCB} = 3.3 V, $V_{CCB} = V_{IH} = V_{ref\_A}$ + 1, V_{IL} = 0, $V_M = 0.5V_{ref\_A}$ (2)	C_L = 15 pF		0.75		ns
			C_L = 30 pF		1.4		
			C_L = 50 pF		1.9		
T_{PHL}	High to low propagation delay		C_L = 15 pF		0.85		ns
			C_L = 30 pF		1.5		
			C_L = 50 pF		2		
T_{PLH}	Low-to-high propagation delay	V_{CCB} = 2.5 V, $V_{CCB} = V_{IH} = V_{ref\_A}$ + 1, V_{IL} = 0, $V_M = 0.5V_{ref\_A}$ (2)	C_L = 15 pF		0.8		ns
			C_L = 30 pF		1.45		
			C_L = 50 pF		2		
T_{PHL}	High to low propagation delay		C_L = 15 pF		0.9		ns
			C_L = 30 pF		1.55		
			C_L = 50 pF		2.1		

(1) Guaranteed by simulation, not tested in production
(2) Translating Down: the high-voltage side driving toward the low-voltage side

6.8 Switching Characteristics (Translating Up)

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PLH}	Low-to-high propagation delay	V_{CCB} = 3.3 V, $V_{CCB} = V_T = V_{ref\_A}$ + 1, $V_{ref\_A} = V_{IH}$, V_{IL} = 0, $V_M = 0.5V_{ref\_A}$ and R_L = 300 Ω(2)	C_L = 15 pF		0.9		ns
			C_L = 30 pF		1.55		
			C_L = 50 pF		2.1		
T_{PHL}	High to low propagation delay		C_L = 15 pF		1		ns
			C_L = 30 pF		1.65		
			C_L = 50 pF		2.2		
T_{PLH}	Low-to-high propagation delay	V_{CCB} = 2.5 V, $V_{CCB} = V_T = V_{ref\ A}$ + 1, $V_{ref\_A} = V_{IH}$, V_{IL} = 0, $V_M = 0.5V_{ref\_A}$ and R_L = 300 Ω(2)	C_L = 15 pF		0.8		ns
			C_L = 30 pF		1.35		
			C_L = 50 pF		1.8		
T_{PHL}	High to low propagation delay		C_L = 15 pF		0.9		ns
			C_L = 30 pF		1.45		
			C_L = 50 pF		1.9		

(1) Guaranteed by simulation, not tested in production
(2) Translating up: the low-voltage side driving toward the high-voltage side

6.9 Typical Characteristics

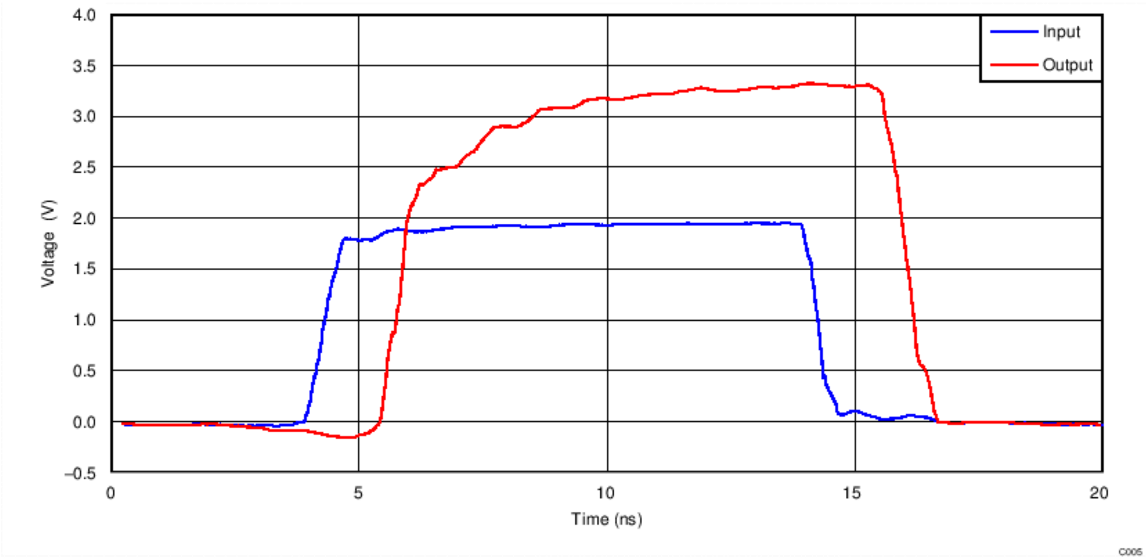
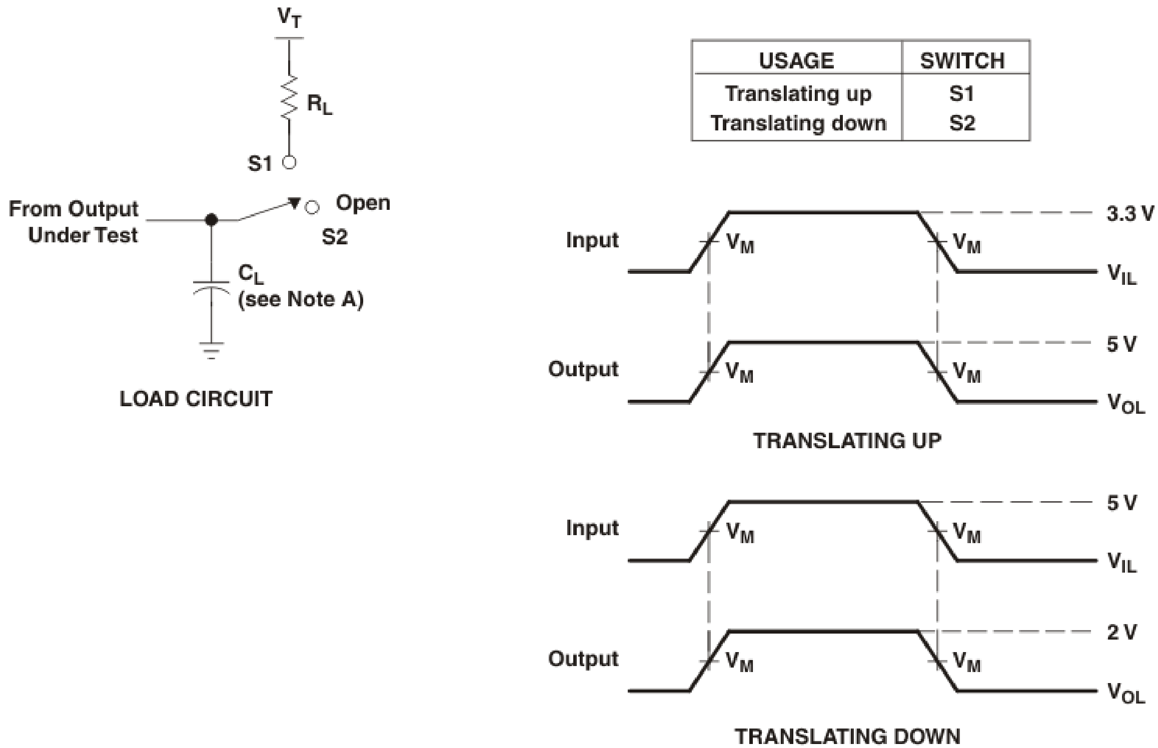


Figure 6-1. Signal Integrity (1.8 to 3.3 V Translation Up at 50 MHz)

7 Parameter Measurement Information



USAGE	SWITCH
Translating up	S1
Translating down	S2

NOTES:
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

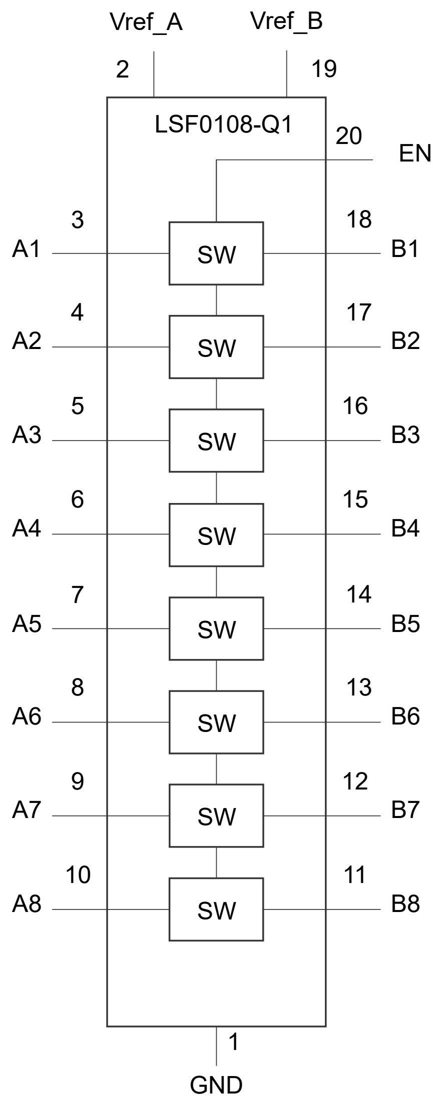
Figure 7-1. Load Circuit for Outputs

8 Detailed Description

8.1 Overview

The LSF0108-Q1 can be used in level-translation applications for interfacing devices or systems operating at different supply voltages. The LSF0108-Q1 is excellent for use in applications where an open-drain driver is connected to the data I/Os. LSF0108-Q1 can achieve 100 MHz with appropriate pull-up resistors and layout. The LSF0108-Q1 may also be used in applications where a push-pull driver is connected to the data I/Os. For an overview of device setup and operation, see *The Logic Minute* training series on *Understanding the LSF Family of Bidirectional, Multi-Voltage Level Translators*.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Auto Bidirectional Voltage Translation

All devices in the LSF family are auto bidirectional voltage level translators. The LSF0108 (RKS package) has 0.65 V to 5.5 V on the V_{ref_A} supply and from 1.8V to 5.5 V on the V_{ref_B} supply. The LSF0108 (PW package) has 0.9 V to 5.5 V on the V_{ref_A} supply and from 1.8V to 5.5 V on the V_{ref_B} supply. This allows bidirectional voltage translation without the need for a direction pin in open-drain or push-pull applications. The LSF family supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 30-pF capacitance and 250-Ω pullup resistor. Both the output driver of the controller and the peripheral device output can be push-pull or open-drain (pull-up resistors may be required). During operation of the device, the B-side is often referred to as the high side while the A-side is referred to as the low side.

8.3.2 Output Enable

To enable the I/O pins, the EN input should be tied directly to V_{ref_B} during operation and both pins must be pulled up to the HIGH side (V_{CCB}) through a bias resistor (typically 200 kΩ). To be in the high impedance state during power-up, power-down, or during operation, the EN pin must be LOW. The EN pin should always be tied directly to the V_{ref_B} pin and is recommended to be disabled by an open-drain driver without a pullup resistor. This allows V_{ref_B} to regulate the EN input and bias the channels for proper translation. A filter capacitor on V_{ref_B} is recommended for a stable supply at the device.

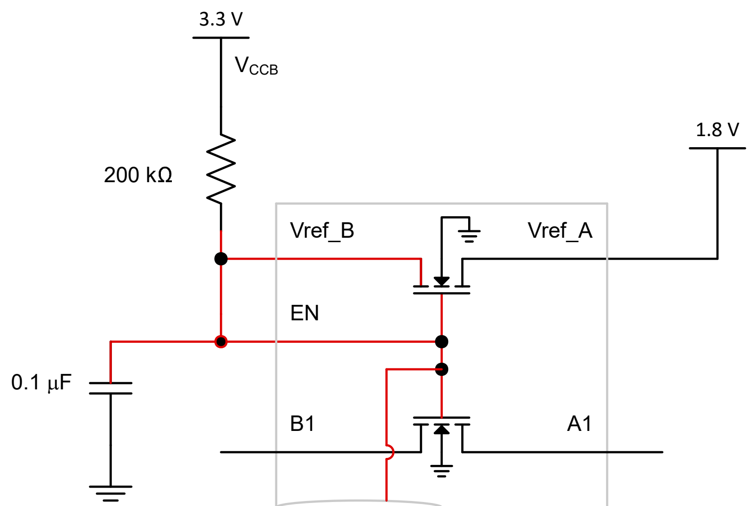


Figure 8-1. EN Pin Tied to V_{ref_B} Directly and to V_{CCB} Through a Pull-Up Resistor

The supply voltage of open drain I/O devices can be completely different from the supplies used for the LSF and has no impact on the operation. For additional details on how to use the enable pin, see the *Using the Enable Pin with the LSF Family video.*

Table 8-1. EN Pin Function Table

INPUT EN(1) PIN	Data Port State
Tied directly to V_{ref_B}	An = Bn
L	Hi-Z

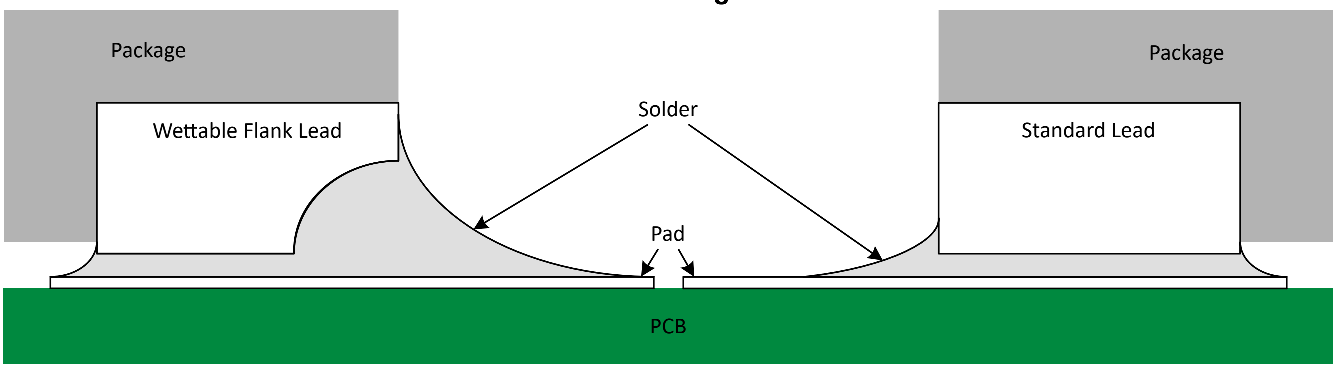
(1) EN is controlled by V_{ref_B} logic levels.

8.3.3 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

Wettable flanks help improve side wetting after soldering which makes QFN packages easier to inspect with automatic optical inspection (AOI). A wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet as shown in the figure. Please see the mechanical drawing for additional details.

Figure 8-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering



8.4 Device Functional Modes

For each channel (n), when either the An or Bn port is LOW, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled LOW. The low R_{ON} of the switch allows connections to be made with minimal propagation delay and signal distortion.

Table 8-1 provides a summary of device operation. For additional details on the functional operation of the LSF family of devices, see the *Down Translation with the LSF Family* and *Up Translation with the LSF Family* videos.

Table 8-2. Device Functionality

Signal Direction[1]	Input State	Switch State	Functionality
B to A (Down Translation)	B = LOW	ON (Low Impedance)	A-side voltage is pulled low through the switch to the B-side voltage
	B = HIGH	OFF (High Impedance)	A-side voltage is clamped at V_{ref_A} [2]
A to B (Up Translation)	A = LOW	ON (Low Impedance)	B-side voltage is pulled low through the switch to the A-side voltage
	A = HIGH	OFF (High Impedance)	B-side voltage is clamped at V_{ref_A} and then pulled up to the V_{PU} supply voltage

(1) The downstream channel should not be actively driven through a low impedance driver, or else bus contention may occur.
(2) The A-side can have a pullup to V_{ref_A} for additional current drive capability or may also be pulled above V_{ref_A} with a pullup resistor. Specifications in the *Recommended Operating Conditions* section should always be followed.

8.4.1 Up and Down Translation

Up Translation: When the signal is driven from A to B and the An port is HIGH, the switch will be OFF and the Bn port will then be driven to a voltage higher than V_{ref_A} by the pullup resistor that is connected to the pull-up supply voltage. This functionality allows seamless translation between the higher and lower voltages selected by the user, without the need for directional control. Pull-up resistors are always required on the high side, and pull-ups are only required on the low side if the output of the low side device is open drain or its input has a leakage greater than 1 µA.

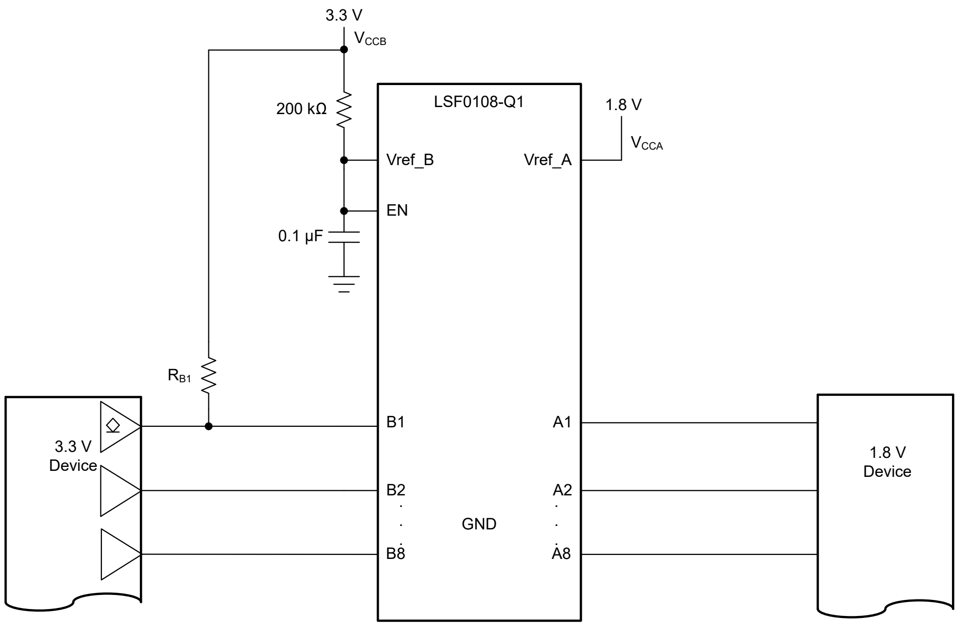


Figure 8-3. Up Translation Example Schematic with Push-Pull and Open Drain Configuration

Up translation with the LSF requires attention to two important factors: maximum data rate and sink current. Maximum data rate is directly related to the rising edge of the output signal. Sink current depends on supply values and the chosen pull-up resistor values. Equation 1 shows the maximum data rate formula, and Equation 2 presents the maximum sink current formula, both of which are estimations. A low RC value is needed to reach high speeds, which also require strong drivers. For estimated data rate and sink current calculations based on circuit component, see the *Up Translation with the LSF Family* video.

$$\frac{1}{3 \times 2R_{B1}C_{B1}} = \frac{1}{6R_{B1}C_{B1}}\left(\frac{bits}{second}\right) \quad (1)$$

$$I_{OL} \cong \frac{V_{CCA}}{R_{A1}} + \frac{V_{CCB}}{R_{B1}}\left(A\right) \quad (2)$$

Down Translation: When the signal is being driven HIGH from the Bn port to An port, the switch will be OFF, clamping the voltage on the An port to the voltage set by V_{ref_A}. A pull-up resistor can be added on either side of the device. There are special circumstances that allow the removal of one or both of the pull-up resistors. If the signal is always going to be down translated from a push-pull transmitter, then the resistor on the B-side can be removed. If the leakage current into the receiver on the A-side is less than 1 µA, then the resistor on the A-side can also be removed. This arrangement, with no external pull-up resistors, can be used when down translating from a push-pull output to a low-leakage input. For an open drain transmitter, the pull-up resistor on the B-side is necessary because an open drain output cannot drive high by itself. Table 9-2 lists a summary of device operation. For additional details on the functional operation of the LSF family of devices, see the *Up Translation with the LSF Family* and *Down Translation with the LSF Family* videos.

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LSF0108-Q1 device can perform voltage translation for open-drain or push-pull interface. Table 9-1 provides some consumer or telecom interfaces as reference to the different channel numbers that are supported by the LSF0108-Q1.

Table 9-1. Voltage Translator for Consumer or Telecom Interface

Part Name	Channel Number	Interface
LSF0108-Q1	8	GPIO, MDIO, SDIO, SVID, UART, SMBus, PMBus, I^2C, and SPI

Some important reminders regarding the LSF family of devices are as follows:

- LSF devices are switch-based, not buffer-based (see the TXB family for buffer-based devices)
- Specific data rates cannot be calculated by using 1/Tpd
- V_{CCB}/V_{CCA} are not the same as V_{ref_B} or V_{ref_A}: V_{CCB} refers to the B-side supply voltage supplied to the LSF device, while V_{ref_B} refers to the voltage at the V_{ref_B} pin (pin 7 of Figure 9-1) on the other side of the 200 kΩ resistor

9.2 Typical Application

9.2.1 I^2C PMBus, SMBus, GPIO

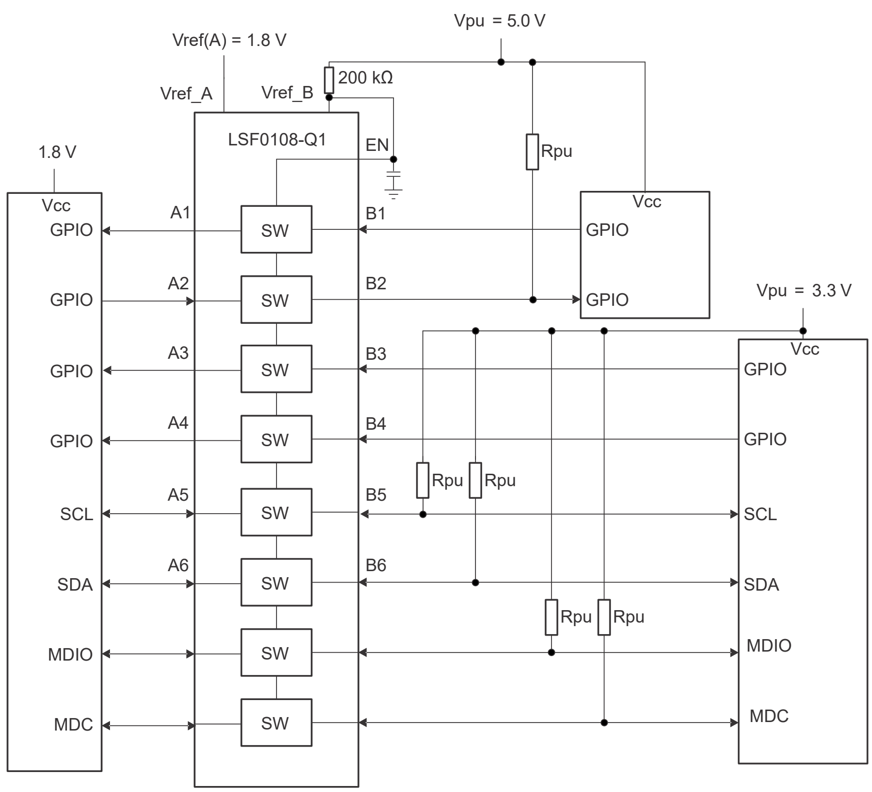


Figure 9-1. Bidirectional Translation to Multiple Voltage Levels

9.2.1.1 Design Requirements

9.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

As shown in Figure 9-1, V_{ref_B} is connected through a 200-kΩ resistor to the V_{PU} power supply at 5 V and V_{ref_A} is connected to a 1.8 V power supply. The A1 and A2 channels have a maximum output voltage equal to V_{ref_A} , and the B1 and B2 channels have a maximum output voltage equal to V_{PU} .

The LSF0108-Q1 has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state. The power consumption is very low because LSF0108-Q1 is a switch-type voltage translator. It is recommended to always enable LSF0108-Q1 for bidirectional application (I^2C, SMBus, PMBus, or MDIO).

Table 9-2. Application Operating Condition - RKS Package

PARAMETER		MIN	TYP	MAX	UNIT
V_{ref_A} (1)	reference voltage (A)	0.65		5.5	V
V_{ref_B}	reference voltage (B)	V_{ref_A} + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	V_{ref_A} + 0.8		5.5	V
V_{pu}	pull-up supply voltage	0		V_{ref_B}	V

Table 9-3. Application Operating Condition - PW Package

PARAMETER		MIN	TYP	MAX	UNIT
V_{ref_A} (1)	reference voltage (A)	0.9		5.5	V
V_{ref_B}	reference voltage (B)	V_{ref_A} + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	V_{ref_A} + 0.8		5.5	V
V_{pu}	pull-up supply voltage	0		V_{ref_B}	V

(1) V_{ref_A} have to be the lowest voltage level across all of inputs and outputs.

Note

The 200 kΩ, bias resistor is required to allow V_{ref_B} to regulate the EN input.

A filter capacitor on V_{ref_B} is recommended. Also V_{ref_B} and $V_{I(EN)}$ are recommended to be at 1.0 V higher than V_{ref_A} for best signal integrity.

9.2.1.1.2 Bias Circuitry

For proper operation, V_{CCA} must always be at least 0.8 V less than V_{CCB} ($V_{CCA} + 0.8 \leqq V_{CCB}$). The 200 kΩ bias resistor is required to allow V_{ref_B} to regulate the EN input and properly bias the device for translation. A 0.1 µF capacitor is recommended for providing a path from V_{ref_B} to ground for high frequency noise. V_{ref_B} and $V_{I(EN)}$ are recommended to be 1.0 V higher than V_{ref_A} for best signal integrity.

Attempting to drive the EN pin directly with a push-pull output device is a very common design error with the LSF0108-Q1 series of devices. It is also very important to note that current does flow into the A-side voltage supply during normal operation. Not all voltage sources can sink current, so be sure that applicable designs can handle this current. For more design details, see the *Understanding the Bias Circuit for the LSF Family* video.

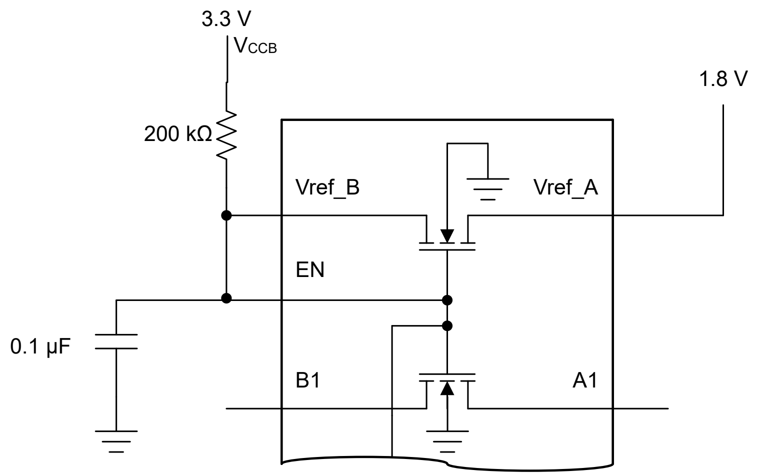


Figure 9-2. Bias Circuitry Inside the LSF010x Device

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{ref_B} and both pins pulled to HIGH side V_{CCB} through a bias resistor (typically 200 kΩ). This allows V_{ref_B} to regulate the EN input. A filter capacitor on V_{ref_B} is recommended. The controller output driver can be push-pull or open-drain (pull-up resistors may be required) and the peripheral device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to V_{PU}).

Note

If either output is push-pull, then data must be unidirectional or the outputs must be tri-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, then no direction control is needed.

Figure 9-1 shows how the reference supply voltage V_{ref_A} is connected to the processor core power supply at 1.8 V and V_{ref_B} is connected through a 200 kΩ resistor to a 5 V power supply. The output of A3 and B4 has a maximum output voltage equal to V_{ref_A}, and the bidirectional interface (Ch5/6, MDIO, MDC) has a maximum output voltage equal to V_{pu}.

9.2.1.2.2 Pull-Up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. Doing this causes a voltage drop of 260 mV to 350 mV to have a valid LOW signal on the downstream channel. If the current through the pass transistor is higher than 15 mA, the voltage drop is also higher in the ON state. To set the current through each pass transistor at 15 mA, calculate the pull-up resistor value using the following equation:

$$Rpu = \frac{(\mathrm{Vpu} - 0.35\ \mathrm{V})}{0.015\ A} \tag{3}$$

Table 9-4 provides resistor values, reference voltages, and currents at 8 mA, 5 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used so that the voltage drop across the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF family device at 0.175 V, although the 15 mA applies only to current flowing through the LSF family device. The device driving the low state at 0.175 V must sink current from one or more of the pull-up resistors and maintain V_{OL}. A decrease in resistance will increase current, and thus result in increased V_{OL}.

Table 9-4. Pull-Up Resistor Values

V_{PU} (1) (2)	8 mA		5 mA		3 mA	
	NOMINAL (Ω)	+10%(3) (Ω)	NOMINAL (Ω)	+10%(3) (Ω)	NOMINAL (Ω)	+10%(3) (Ω)
5 V	581	639	930	1023	1550	1705
3.3 V	369	406	590	649	983	1082
2.5 V	269	296	430	473	717	788
1.8 V	181	199	290	319	483	532
1.5 V	144	158	230	253	383	422
1.2 V	106	117	170	187	283	312

(1) Calculated for V_{OL} = 0.35 V
(2) Assumes output driver V_{OL} = 0.175 V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

9.2.1.2.3 LSF0108-Q1 Bandwidth

The maximum frequency of the LSF0108-Q1 is dependent on the application. The device can operate at speeds of >100 MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application. The LSF0108-Q1 behaves like a standard switch where the bandwidth of the device is dictated by the on resistance and on capacitance of the device.

Figure 9-3 shows a bandwidth measurement of the LSF0108-Q1 using a two-port network analyzer.

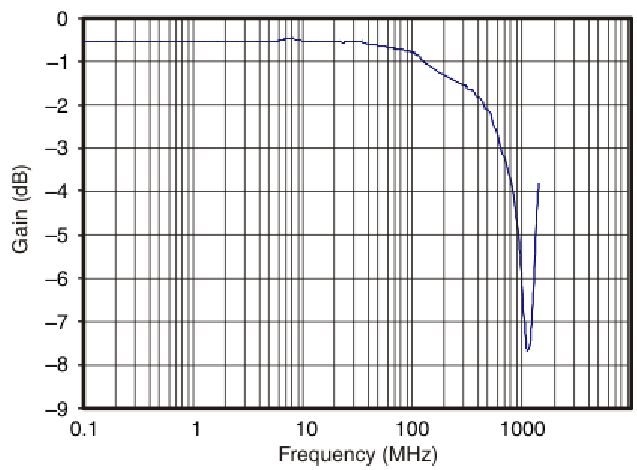


Figure 9-3. 3-dB Bandwidth

The 3-dB point of the LSF0108-Q1 is ≅ 600 MHz; however, this measurement is an analog type of measurement. For digital applications the signal should not degrade up to the fifth harmonic of the digital signal. The frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In the case of the LSF0108-Q1, a digital clock frequency of greater than 100 MHz can be achieved.

The LSF0108-Q1 does not provide any drive capability. Therefore higher frequency applications will require higher drive strength from the host side. No pull-up resistor is needed on the host side (3.3 V) if the LSF0108-Q1 is being driven by standard CMOS totem pole output driver. Ideally, it is best to minimize the trace length from the LSF0108-Q1 on the sink side (1.8 V) to minimize signal degradation.

All fast edges have an infinite spectrum of frequency components; however, there is an inflection (or knee) in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

To calculate the maximum practical frequency component, or the knee frequency (f_{knee}), use Equation 4 and Equation 5:

$$f_{knee} = \frac{0.5}{RT\,(10 - 80\%)} \tag{4}$$

$$f_{knee} = \frac{0.4}{RT\,(20 - 80\%)} \tag{5}$$

For signals with rise time characteristics based on 10% to 90% thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise time characteristics based on 20% to 80% thresholds, which is very common in many of today's device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the LSF0108-Q1 close to the I^2C output of the processor.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pull-up resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected.

9.2.1.3 Application Curves

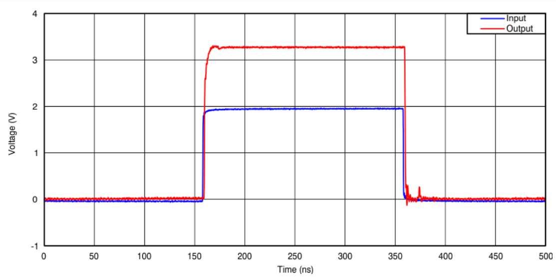


Figure 9-4. Captured Waveform From Above I^2C Set-Up (1.8 V to 3.3 V at 2.5 MHz)

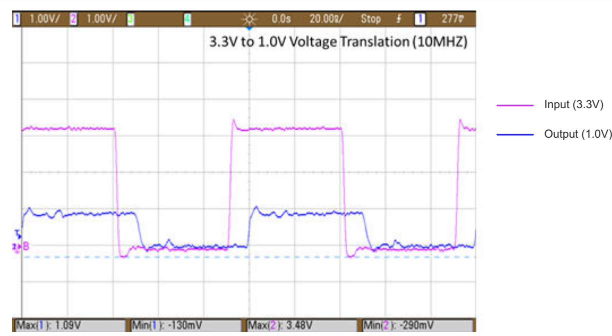


Figure 9-5. Captured Waveform From Above MDIO Setup

9.2.2 Mixed-Mode Voltage Translation

The supply voltage (V_{PU}) for each channel can be individually set with a pull-up resistor. Figure 9-6 shows an example of this mixed-mode multi-voltage translation. For additional details on multi-voltage translation, see the *Multi-voltage Translation with the LSF Family* video.

With the V_{ref_B} pulled up to 5 V and V_{ref_A} connected to 1.8 V, all channels will be clamped to 1.8 V at which point a pullup can be used to define the high level voltage for a given channel.

- **Push-Pull Down Translation (5 V to 1.8 V):** Channel 1 is an example of this setup. When B1 is 5 V, A1 is clamped to 1.8 V, and when B1 is LOW, A1 is driven LOW through the switch.
- **Push-Pull Up Translation (1.8 V to 5 V)**: Channel 2 is an example of this setup. When A2 is 1.8 V, the switch is high impedance and the B2 channel is pulled up to 5 V. When A2 is LOW, B2 is driven LOW through the switch.
- **Push-Pull Down Translation (3.3 V to 1.8 V):** Channels 3 and 4 are examples of this setup. When either B3 or B4 are driven to 3.3 V, A3 or A4 are clamped to 1.8 V, and when either B3 or B4 are LOW, A3 or A4 are driven LOW through the switch.
- **Open-Drain Bidirectional Translation (3.3 V ↔ 1.8 V):** Channels 5 through 8 are examples of this setup. These channels are for bidirectional operation for I^2C and MDIO to translate between 1.8 V and 3.3 V with open-drain drivers.

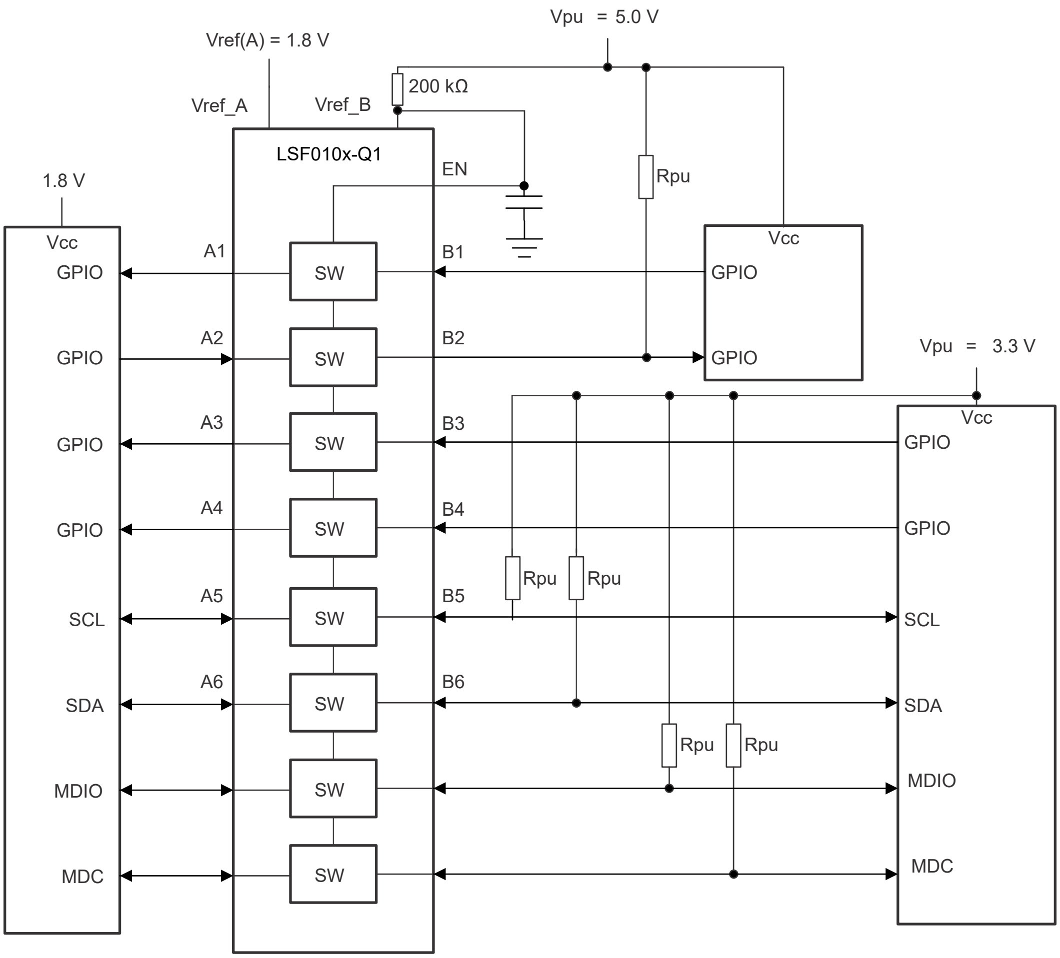


Figure 9-6. Multi-Voltage Translation with the LSF010x-Q1

9.2.2.1 Single Supply Translation

Sometimes, an external device will have an unknown voltage that could be above or below the desired translation voltage, preventing a normal connection of the LSF. Resistors are added on the A side in place of the second supply in this case – this is an example of when LSF single supply operation is utilized, shown in Figure 9-5. In the following figure, a single 3.3 V supply is used to translate between a 3.3 V device and a device that can change between 1.8 V and 5.0 V. R1 and R2 are added in place of the second supply. Note that due to some current coming out of the V_{ref_A} pin, this cannot be treated as a simple voltage divider.

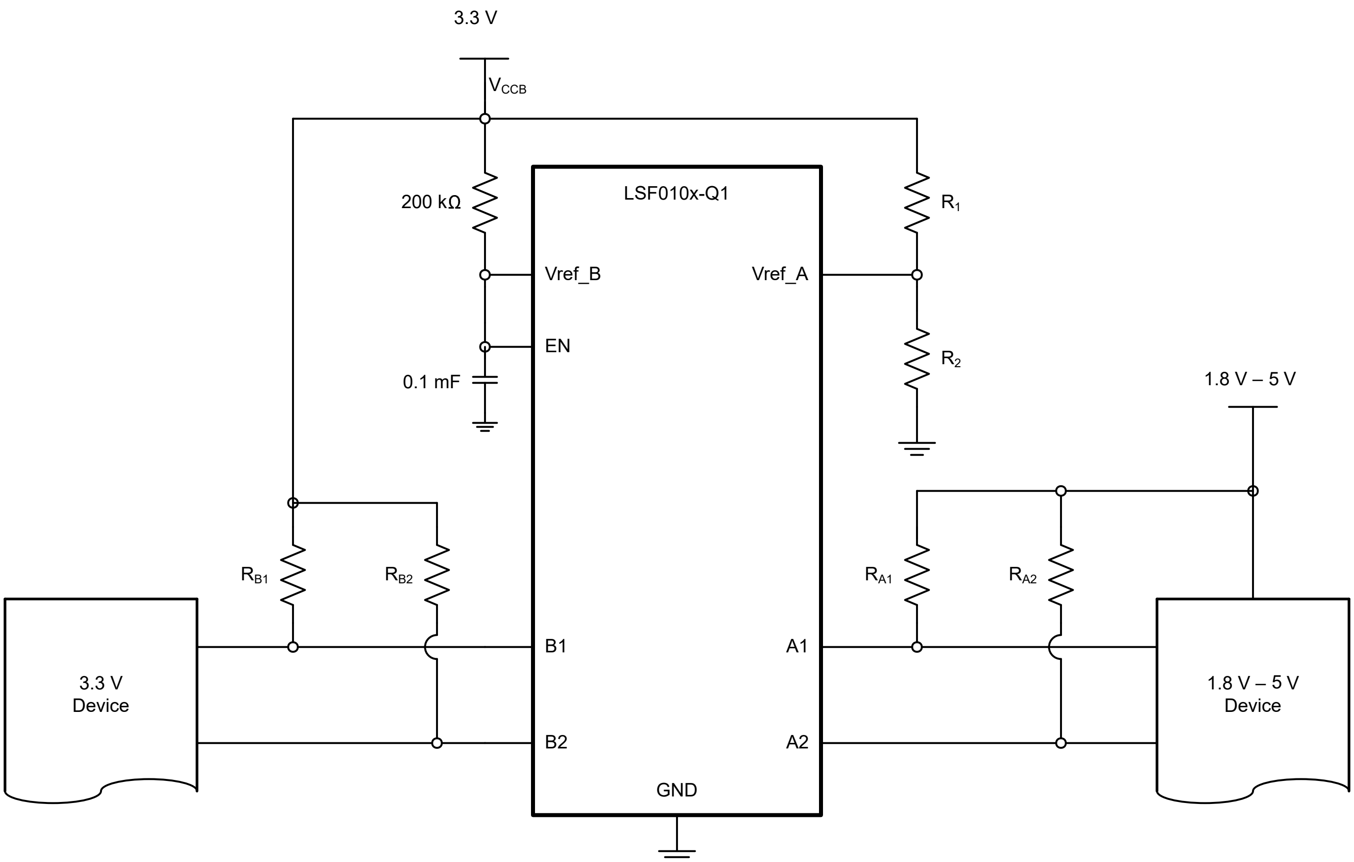


Figure 9-7. Single Supply Translation with 3.3 V Supply

The steps to select the resistor values for R1 and R2 are as follows:

1. Select a value for R1. Typically, 1 MΩ is used to reduce current consumption.
2. Plug in values for your system into the following equation. Note that V_{ref_A} is the lowest voltage in the system. V_{CCB} is the primary supply and R1 is the selected value from step 1.

$$R_2 = \frac{200\left(10^3\right) \times R_1 \times V_{REFA}}{\left(200\left(10^3\right) + R_1\right)\left(V_{CCB} - V_{REFA}\right) - 0.85 \times R_1} \tag{6}$$

The single supply used must be at least 0.8 V larger than the lowest desired translation voltage. The voltage at V_{ref_A} must be selected as the lowest voltage to be used in the system. The LSF evaluation module (LSF-EVM) contains unpopulated pads to place R1 and R2 for single supply operation testing. For an example single supply translation schematic and details, see the *Single Supply Translation with the LSF Family* video.

9.2.2.2 Voltage Translation for $V_{ref\_B} < V_{ref\_A} + 0.8$ V

As described in the *Enable, Disable, and Reference Voltage Guidelines* section, it is generally recommended that $V_{ref\_B} > V_{ref\_A} + 0.8$ V; however, the device can still operate in the condition where $V_{ref\_B} < V_{ref\_A} + 0.8$ V as long as additional considerations are made for the design.

Typical Operation ($V_{ref\_B} > V_{ref\_A} + 0.8$ V): in this scenario, pullup resistors are not required on the A-side for proper down-translation as is shown for channels 1 and 2 of Figure 9-6. The typical operating mode of the device is designed so that when down translating from B to A, the A-side I/O ports will clamp at V_{ref_A} to provide proper voltage translation. For further explanation of device operation, see the *Down Translation with the LSF Family* video.

Requirements for $V_{ref\_B} < V_{ref\_A} + 0.8$ V Operation: in this scenario, there is not a large enough voltage difference between V_{ref_A} and V_{ref_B} to ensure that the A side I/O ports will be clamped at V_{ref_A}, but rather at a voltage approximately equal to V_{ref_B} – 0.8 V. For example, if V_{ref_B} = 1.8 V and V_{ref_A} = 1.2 V, the A-side I/Os will clamp to a voltage around 1.0 V. Therefore, to operate in such a condition, the following additional design considerations must be met:

- V_{ref_B} must be greater than V_{Ref_A} during operation ($V_{ref\_B} > V_{ref\_A}$)
- Pullup resistors should be populated on A-side I/O ports so that the line will be fully pulled up to the desired voltage.

Figure 9-8 shows an example of this setup, where 1.2 V ↔ 1.8 V translation is achieved with the LSF0108-Q1. This type of setup also applies for other voltage nodes such as 1.8 V ↔ 2.5 V, 1.05 V ↔ 1.5 V, and others as long as the *Recommended Operating Conditions* table is followed.

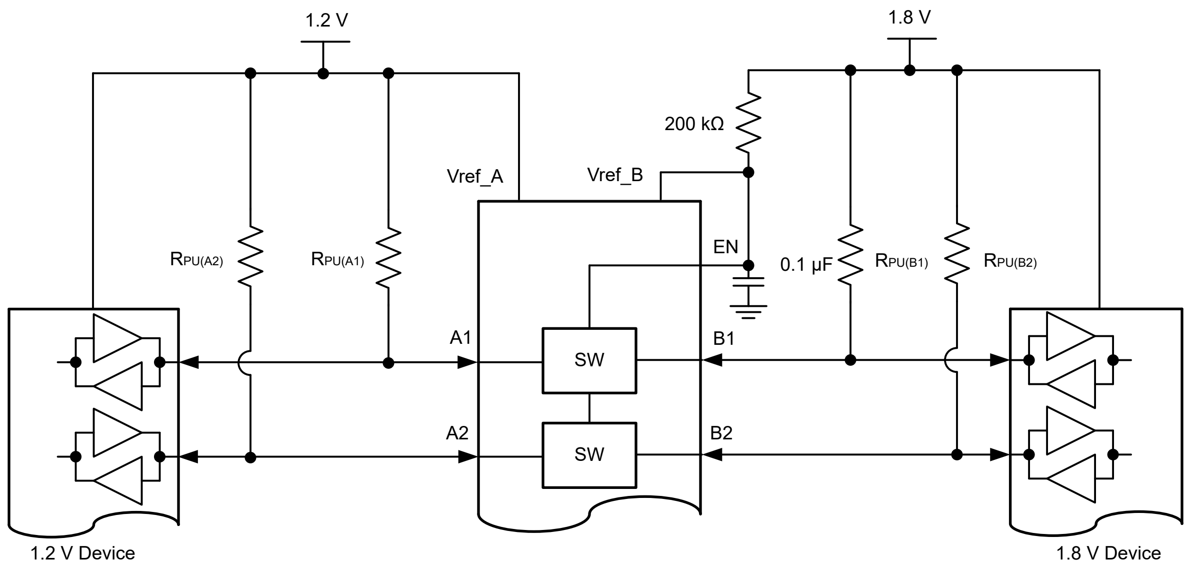


Figure 9-8. 1.2 V to 1.8 V Level Translation with LSF010x-Q1

9.3 Power Supply Recommendations

There are no power sequence requirements for the LSF0108-Q1. For enable and reference voltage guidelines, refer to *Section 9.2.1.1.1*.

9.4 Layout

9.4.1 Layout Guidelines

Because the LSF0108-Q1 is a switch-type level translator, the signal integrity is highly related with a pull-up resistor and PCB capacitance condition.

- Short signal trace as possible to reduce capacitance and minimize stub from pull-up resistor.
- Place LSF close to high voltage side.
- Select the appropriate pull-up resistor that applies to translation levels and driving capability of transmitter.

9.4.2 Layout Example

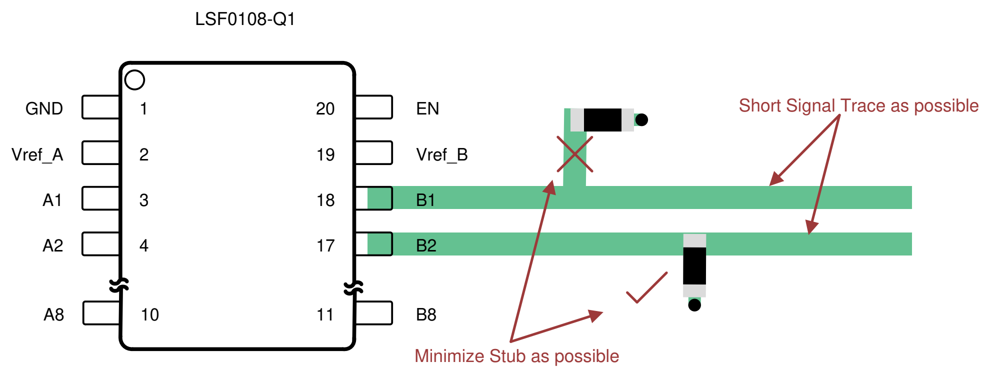


Figure 9-9. Short Trace Layout

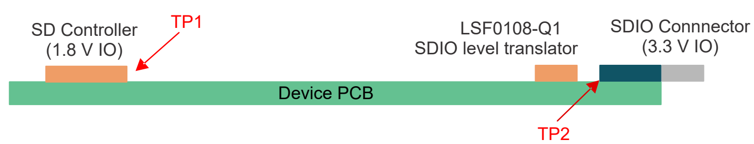


Figure 9-10. Device Placement

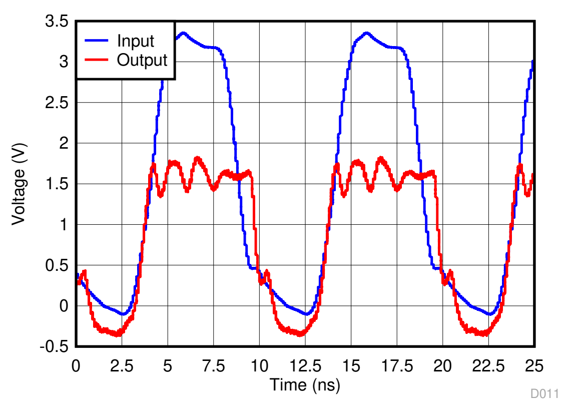


Figure 9-11. Waveform From TP1 (Pull-Up Resistor: 160-Ω and 50-pF Capacitance 3.3 V to 1.8 V at 100 MHz)

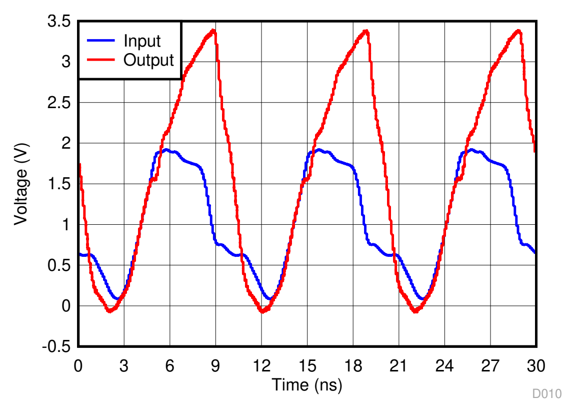


Figure 9-12. Waveform From TP2 (Pull-Up Resistor: 160-Ω and 50-pF Capacitance 1.8 V to 3.3 V at 100 MHz)

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LSF0108QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LSF0108Q	Samples
LSF0108QWRKSRQ1	ACTIVE	VQFN	RKS	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LSF0108	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

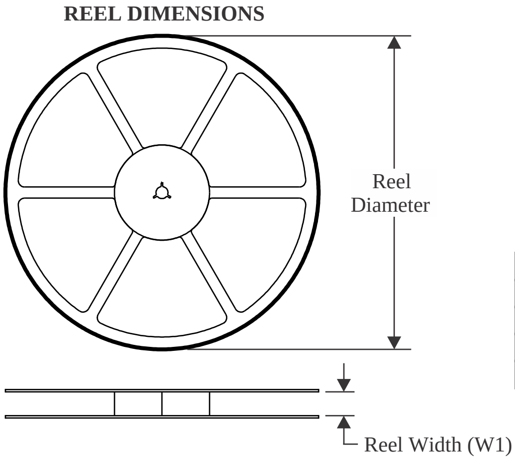
OTHER QUALIFIED VERSIONS OF LSF0108-Q1 :

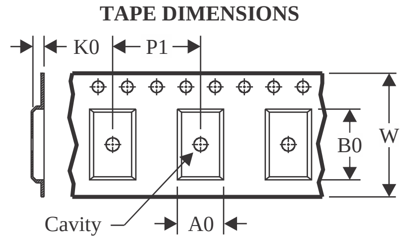
- Catalog : LSF0108

NOTE: Qualified Version Definitions:

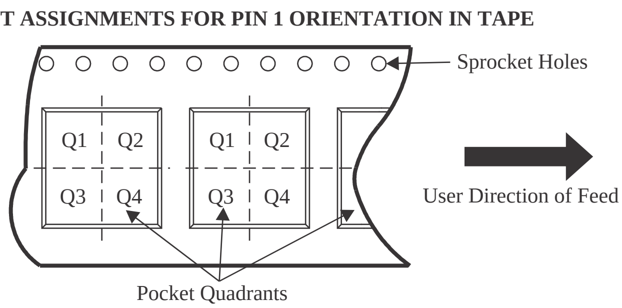
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





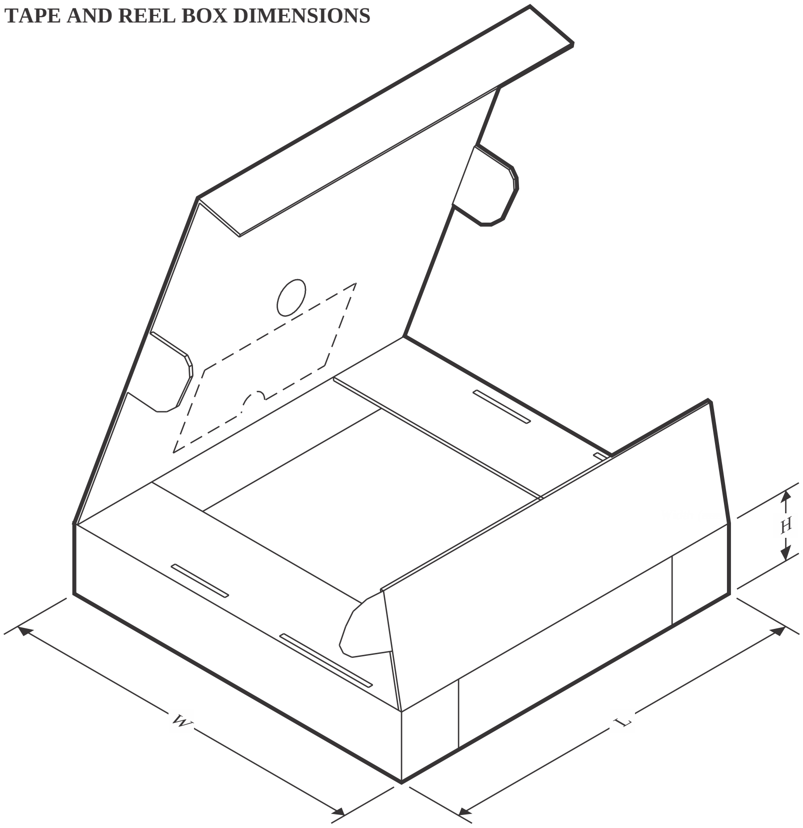
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LSF0108QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LSF0108QWRKSRQ1	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LSF0108QPWRQ1	TSSOP	PW	20	2000	364.0	364.0	27.0
LSF0108QWRKSRQ1	VQFN	RKS	20	3000	210.0	185.0	35.0

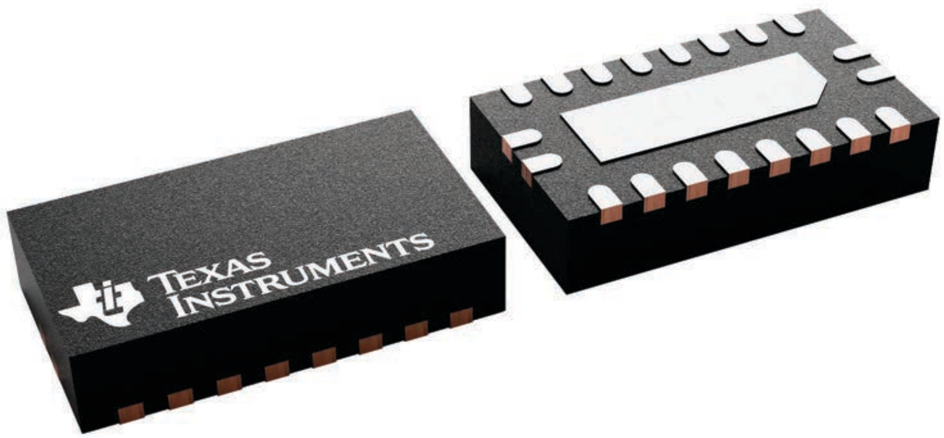
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

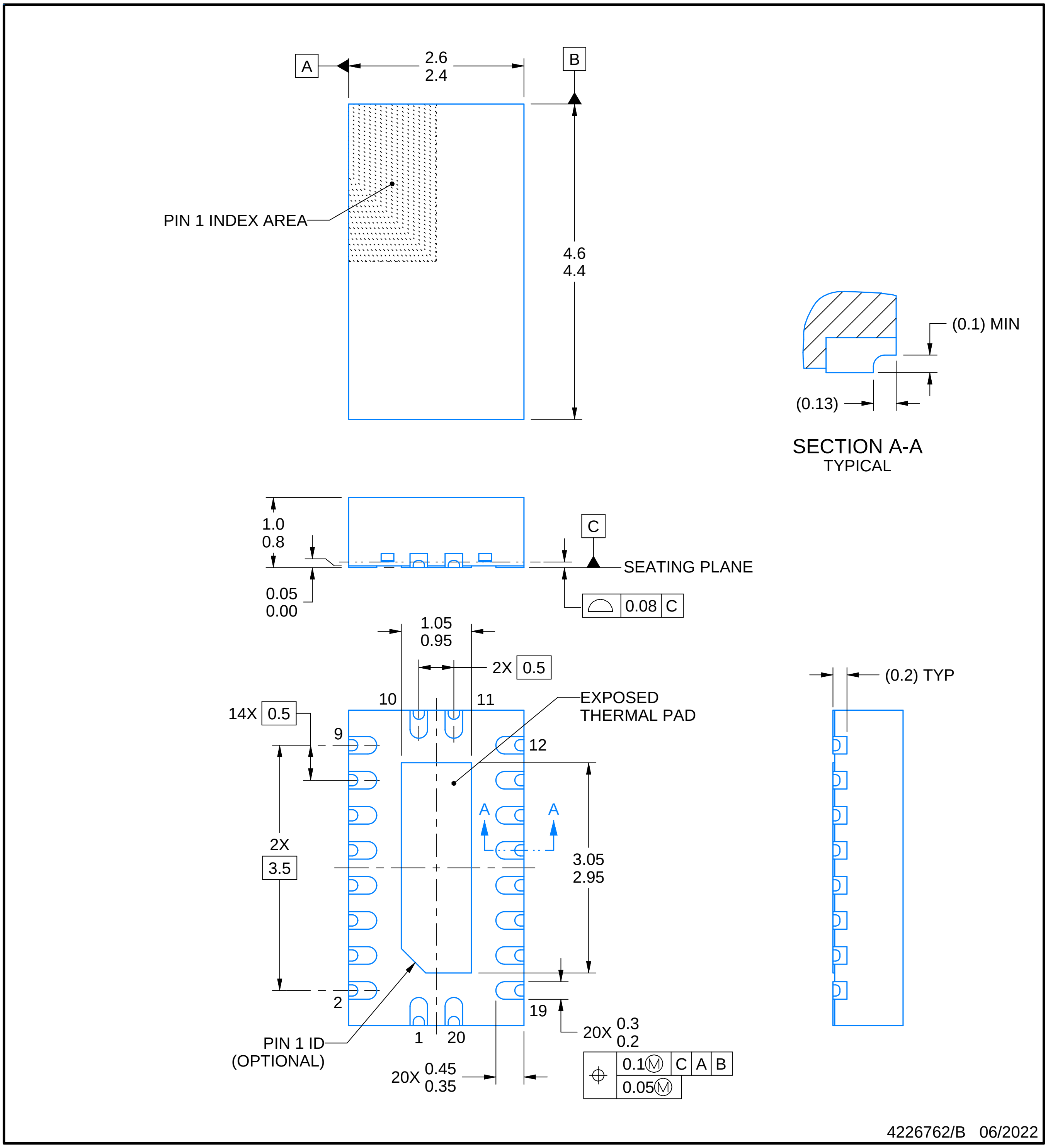
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



RKS0020B

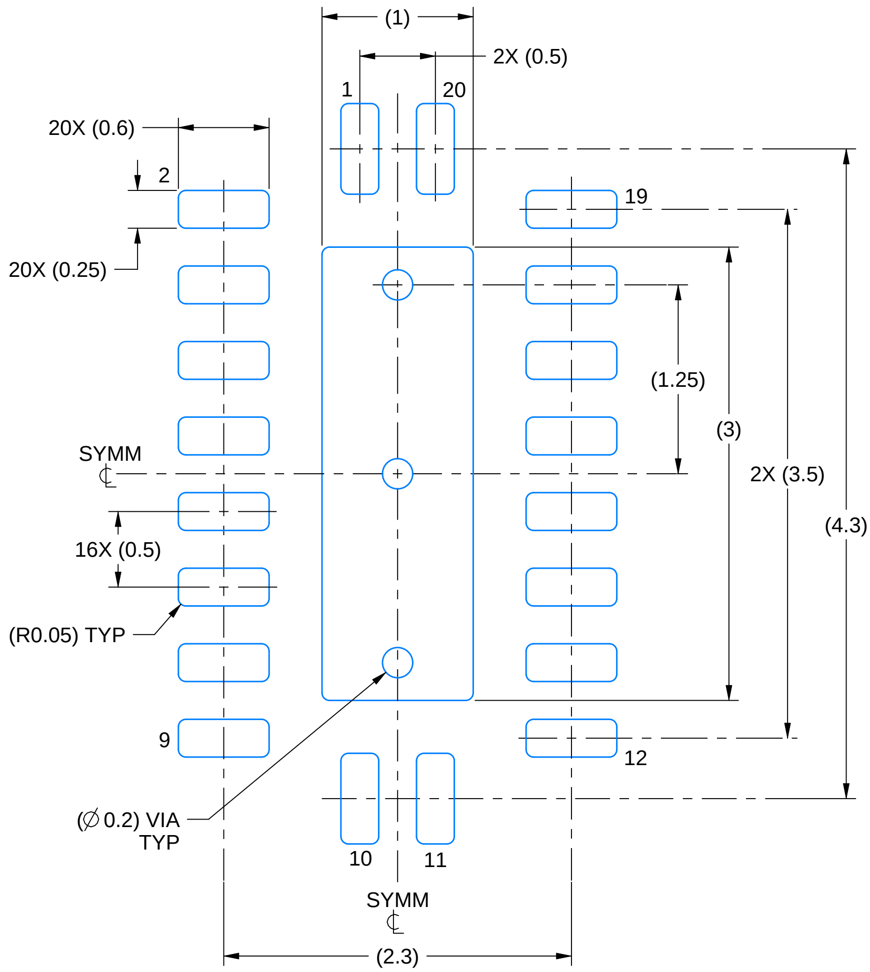
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

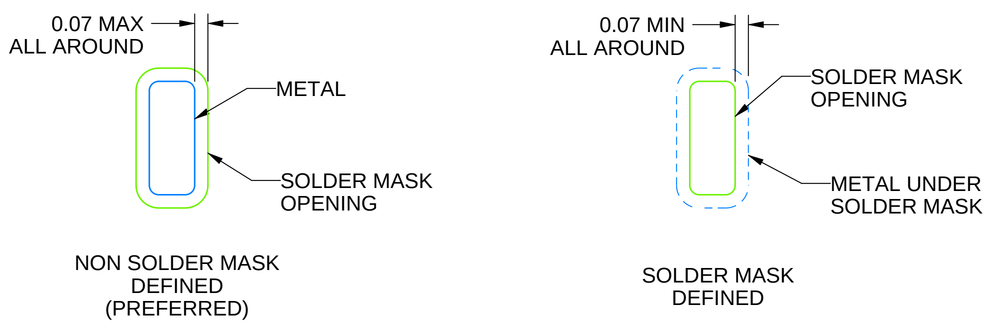


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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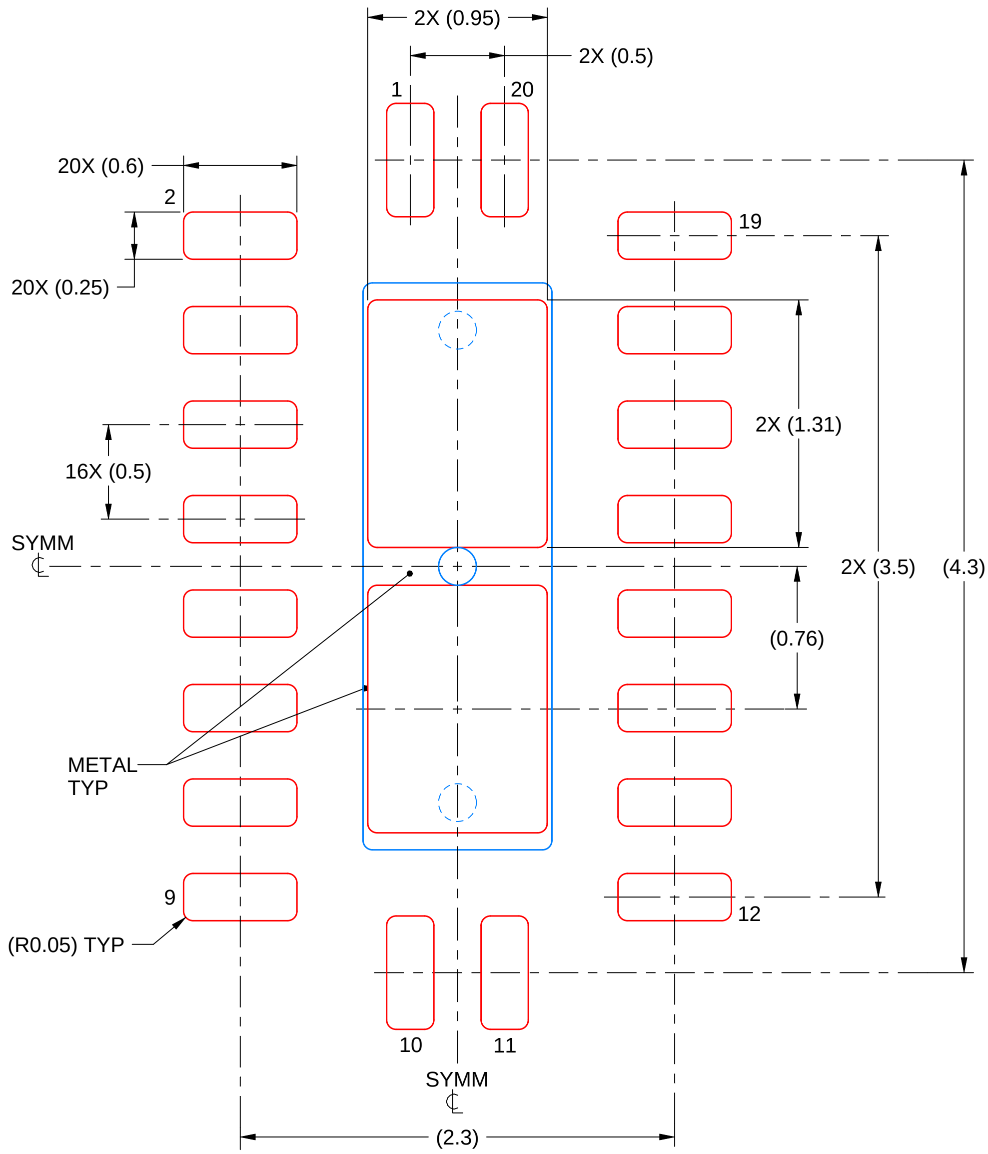
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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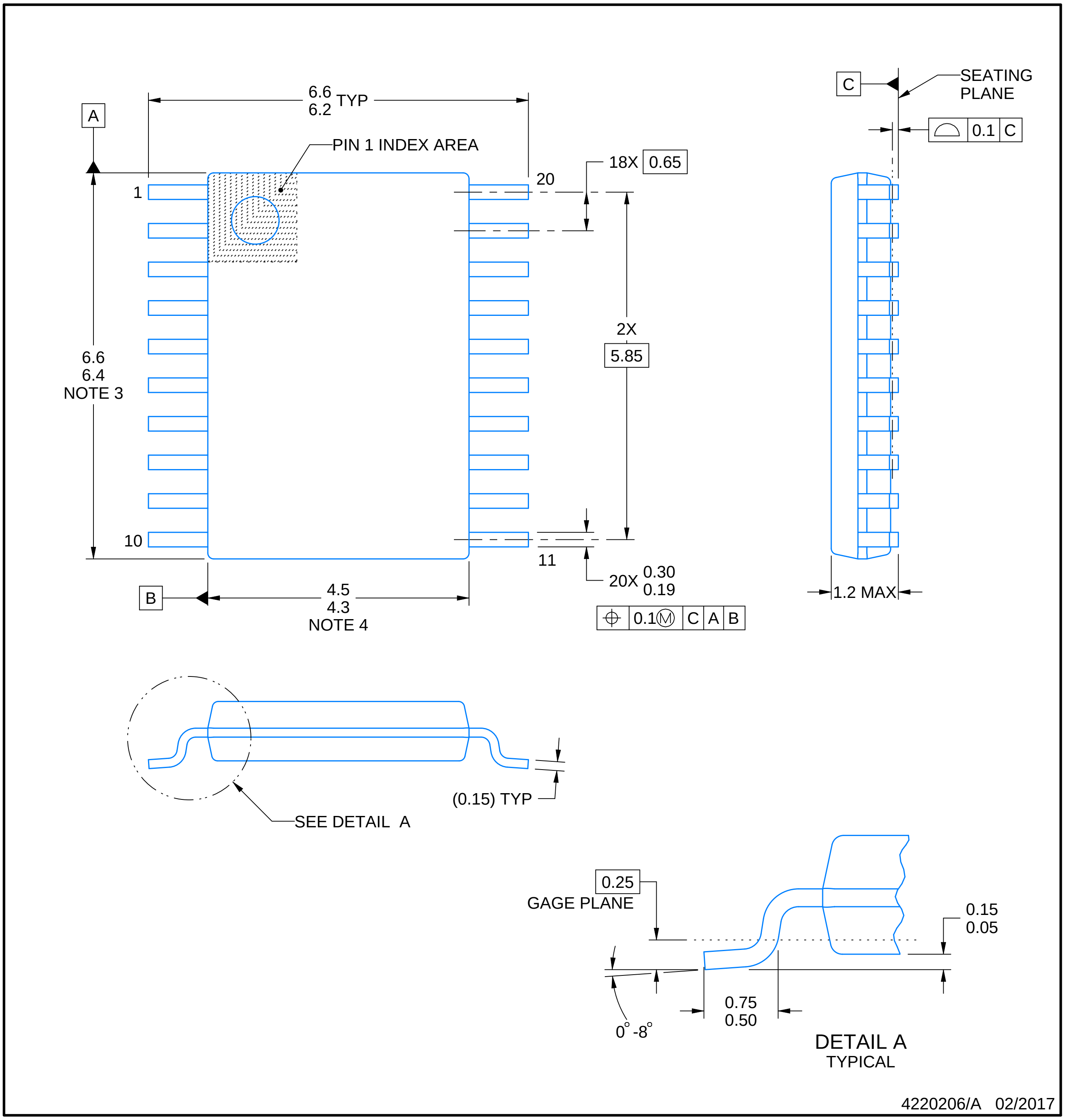
NOTES: (continued)

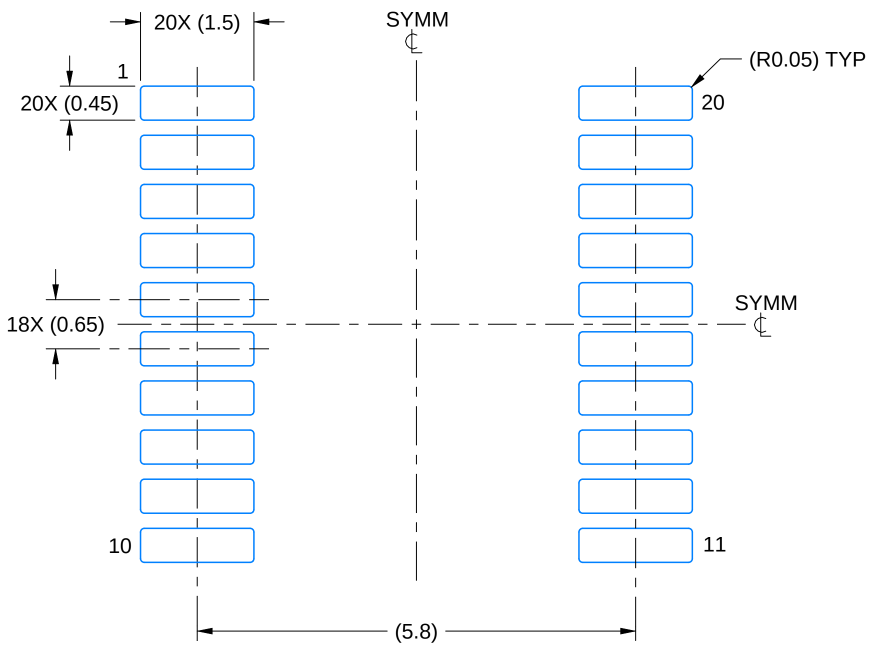
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



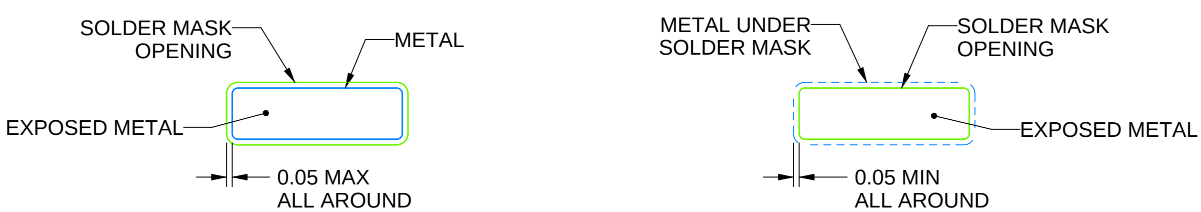
4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

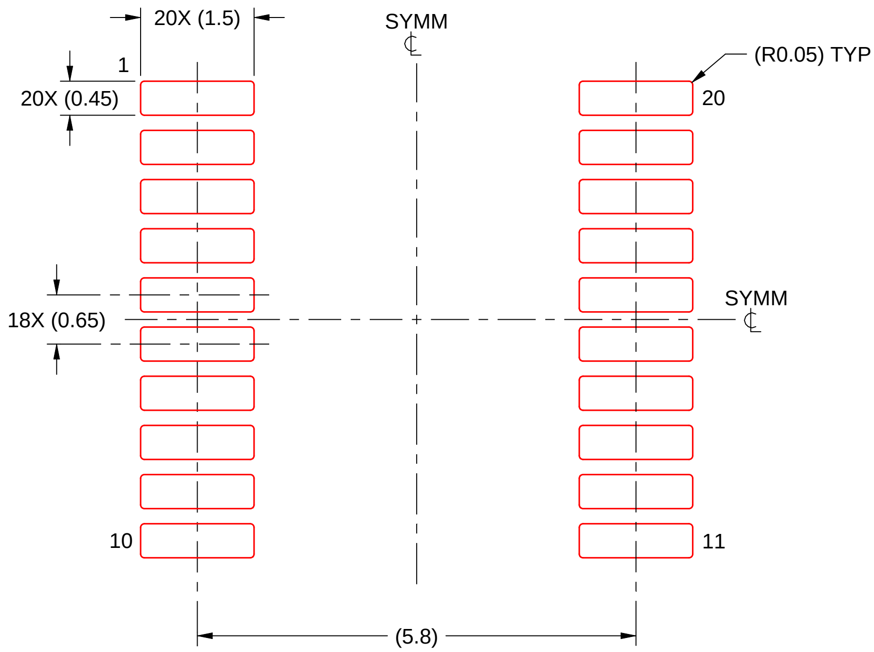
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



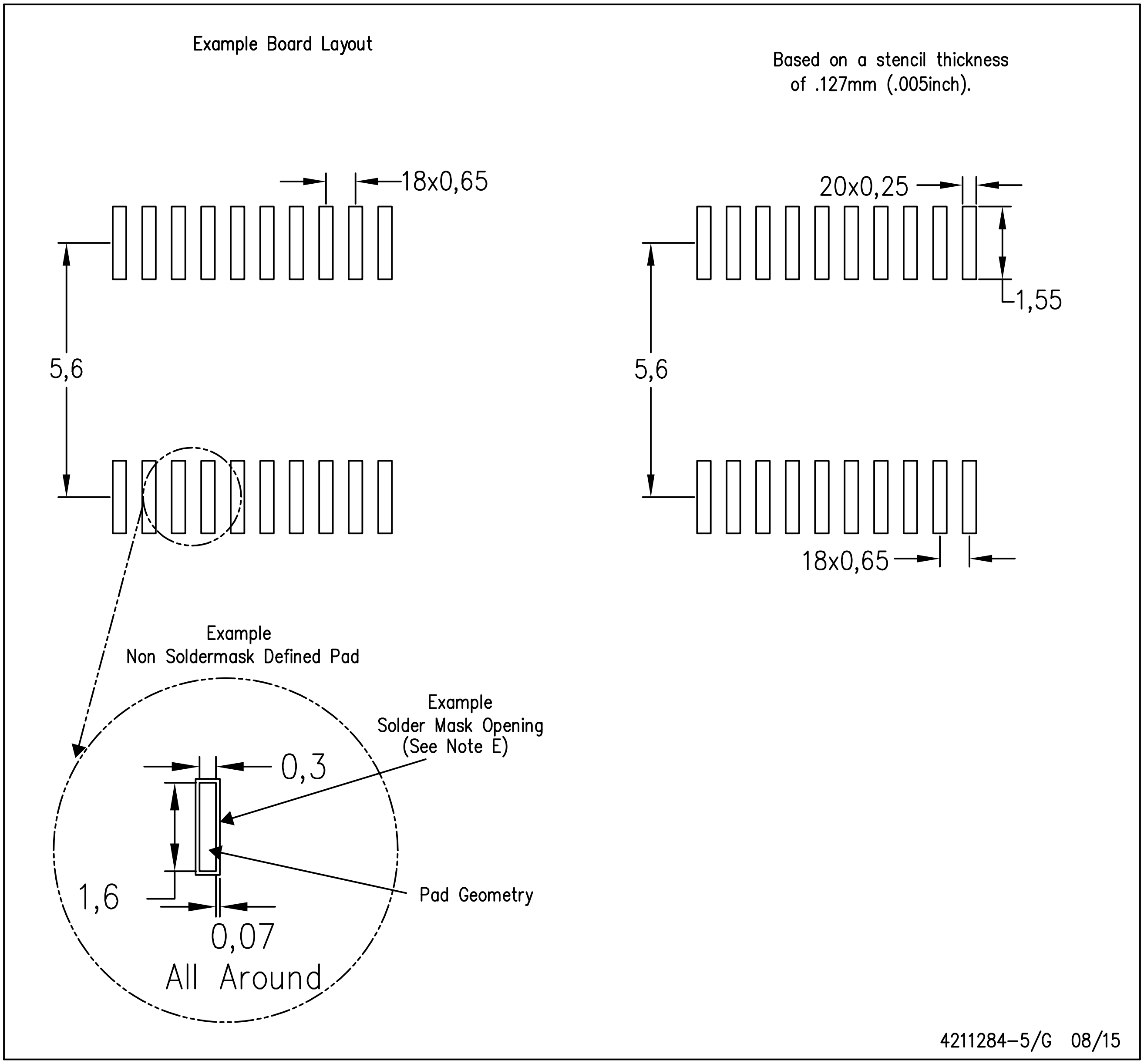
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

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