

# MAX211 5V Multichannel RS-232 Line Driver and Receiver with $\pm 15\text{kV}$ ESD Protection

## 1 Features

- RS-232 bus-pin ESD protection exceeds  $\pm 15\text{kV}$  using human-body model (HBM)
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU v.28 standards
- Operates at 5V  $V_{CC}$  supply
- Four drivers and five receivers
- Operates up to 120kbit/s
- Low supply current in shutdown mode: 5 $\mu\text{A}$  typical
- External capacitors: 4  $\times$  0.1 $\mu\text{F}$
- Latch-up performance exceeds 100mA per JESD 78, class II

## 2 Applications

- [Battery-powered systems](#)
- [PDAs](#)
- [Notebooks](#)
- [Laptops](#)
- [Palmtop PCs](#)
- [Hand-held equipment](#)

## 3 Description

The MAX211 device consists of four line drivers, five line receivers, and a dual charge-pump circuit with  $\pm 15\text{kV}$  ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5V supply. The devices operate at data signaling rates up to 120kbit/s and a maximum of 30V/ $\mu\text{s}$  driver output slew rate.

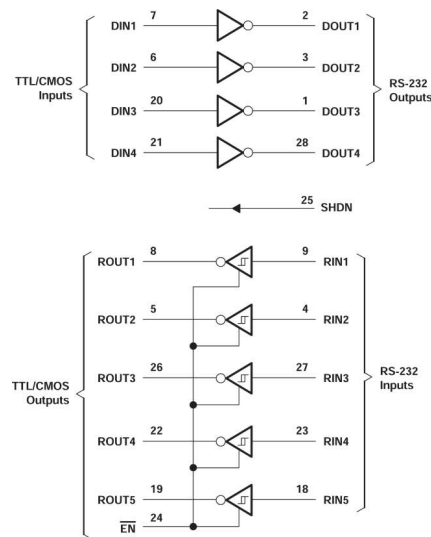
The MAX211 has both shutdown (SHDN) and enable control ( $\overline{\text{EN}}$ ). In shutdown mode, the charge pumps are turned off,  $V_+$  is pulled down to  $V_{CC}$ ,  $V_-$  is pulled to GND, and the transmitter outputs are disabled. This reduces supply current typically to 1 $\mu\text{A}$ .  $\overline{\text{EN}}$  is used to put the receiver outputs into the high-impedance state to allow wired-OR connection of two RS-232 ports. It has no effect on the RS-232 drivers or the charge pumps.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
MAX211	DB (SSOP, 28)	10.2mm $\times$ 7.8mm
	DW (SOIC, 28)	17.9mm $\times$ 10.3mm

(1) For more information, see [Section 11](#).

(2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



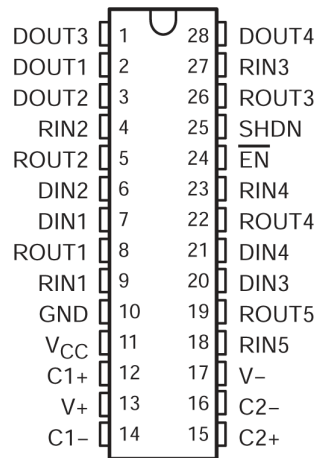
Logic Diagram (Positive Logic)



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## 4 Pin Configuration and Functions



**Figure 4-1. DB or DW Package (Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	DB or DW		
DOUT3	1	O	RS232 line data output (to remote RS232 system)
DOUT1	2	O	RS232 line data output (to remote RS232 system)
DOUT2	3	O	RS232 line data output (to remote RS232 system)
RIN2	4	I	RS232 line data input (from remote RS232 system)
ROUT2	5	O	Logic data output (to UART)
DIN2	6	I	Logic data input (from UART)
DIN1	7	I	Logic data input (from UART)
ROUT1	8	O	Logic data output (to UART)
RIN1	9	I	RS232 line data input (from remote RS232 system)
GND	10	-	Ground
V <sub>CC</sub>	11	--	Supply Voltage, Connect to external 3V to 5.5V power supply
C1+	12	--	Positive lead of C1 capacitor
V+	13	O	Positive charge pump output for storage capacitor only
C1-	14	--	Negative lead of C1 capacitor
C2+	15	--	Positive lead of C2 capacitor
C2-	16	--	Negative lead of C2 capacitor
V-	17	O	Negative charge pump output for storage capacitor only
RIN5	18	I	RS232 line data input (from remote RS232 system)
ROUT5	19	O	Logic data output (to UART)
DIN3	20	I	Logic data input (from UART)
DIN4	21	I	Logic data input (from UART)
ROUT4	22	O	Logic data output (to UART)
RIN4	23	I	RS232 line data input (from remote RS232 system)
$\overline{\text{EN}}$	24	--	Active low enable
SHDN	25	--	Active high shutdown
ROUT3	26	O	Logic data output (to UART)
RIN3	27	I	RS232 line data input (from remote RS232 system)
DOUT4	28	O	RS232 line data output (to remote RS232 system)
Thermal Pad	-	--	Exposed thermal pad. Can be connected to GND or left floating.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$ <sup>(2)</sup>	Supply voltage range		-0.3	6	V
$V+$ <sup>(2)</sup>	Positive charge pump voltage range		$V_{CC} - 0.3$	14	V
$V-$ <sup>(2)</sup>	Negative charge pump voltage range		0.3	-14	V
$V_I$	Input voltage range	Drivers	-0.3	$V+ + 0.3$	V
		Receivers (DW package)		$\pm 30$	V
		Receivers (DB package)		$\pm 25$	V
$V_O$	Output voltage range	Drivers	$V- - 0.3V$	$V+ + 0.3$	V
		Receivers	-0.3	$V_{CC} + 0.3$	V
	Short-circuit duration	DOUT	Continuous		
$T_J$	Operating virtual junction temperature			150	°C
$T_{stg}$	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

### 5.2 ESD Protection

PIN	TEST CONDITIONS	TYP	UNIT
$D_{OUT}$ , $R_{IN}$	Human-Body Model	$\pm 15$	kV

### 5.3 Recommended Operating Conditions

(see<sup>(1)</sup> and Figure 6-4)

			MIN	NOM	MAX	UNIT
Supply voltage			1.5	5	5.5	V
$V_{IH}$	Driver high-level input voltage	DIN	2			V
	Control high-level input voltage	$\overline{EN}$ , SHDN	2.4			V
$V_{IL}$	Driver and control low-level input voltage	DIN, $\overline{EN}$ , SHDN			0.8	V
$V_I$	Driver and control input voltage	DIN, $\overline{EN}$ , SHDN	0		5.5	V
		DW Package	-30		30	V
	Receiver input voltage	DB Package	-25		25	V
$T_A$	Operating free-air temperature	MAX211C	0		70	°C
		MAX211I	-40		85	°C

- (1) Test conditions are C1–C4 = 0.1 $\mu$ F at  $V_{CC} = 5V \pm 0.5V$ .

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DB	DW	UNIT
		28-PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.1	46	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.2	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.0	37.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	4.6	7.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	36.5	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see <sup>(2)</sup>)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$I_{CC}$	Supply current	No load,	See <a href="#">Figure 8-1</a>		14	20	mA
	Shutdown supply current (DB package)	$T_A = 25^\circ\text{C}$	See <a href="#">Figure 6-1</a>		5	10	$\mu\text{A}$
	Shutdown supply current (DW package)	$T_A = 25^\circ\text{C}$	See <a href="#">Figure 6-1</a>		1	20	$\mu\text{A}$

- (1) All typical values are at  $V_{CC} = 5\text{V}$ , and  $T_A = 25^\circ\text{C}$ .  
(2) Test conditions are  $C1-C4 = 0.1\mu\text{F}$  at  $V_{CC} = 5\text{V} \pm 0.5\text{V}$ .

## 5.6 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see <sup>(3)</sup> and [Figure 6-4](#))

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	DOUT at $R_L = 3\text{k}\Omega$ to GND		5	9		V
$V_{OL}$	Low-level output voltage	DOUT at $R_L = 3\text{k}\Omega$ to GND		-5	-9		V
$I_{IH}$	Driver high-level input current	$DIN = V_{CC}$			15	200	$\mu\text{A}$
	Control high-level input current	$\overline{EN}, \text{SHDN} = V_{CC}$			3	10	
$I_{IL}$	Driver low-level input current	$DIN = 0\text{V}$			-15	-200	$\mu\text{A}$
	Control low-level input current	$\overline{EN}, \text{SHDN} = 0\text{V}$			-3	-10	
$I_{OS}$ <sup>(2)</sup>	Short-circuit output current	$V_{CC} = 5.5\text{V}$ ,	$V_O = 0\text{V}$		$\pm 10$	$\pm 60$	mA
$r_o$	Output resistance	$V_{CC}, V_+, \text{ and } V_- = 0\text{V}$ ,	$V_O = \pm 2\text{V}$	300			$\Omega$

- (1) All typical values are at  $V_{CC} = 5\text{V}$ , and  $T_A = 25^\circ\text{C}$ .  
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.  
(3) Test conditions are  $C1-C4 = 0.1\mu\text{F}$  at  $V_{CC} = 5\text{V} \pm 0.5\text{V}$ .

## 5.7 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see <sup>(3)</sup>)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
	Maximum data rate	$C_L = 50\text{pF}$ to $1000\text{pF}$ , One DOUT switching,	$R_L = 3\text{k}\Omega$ to $7\text{k}\Omega$ , See <a href="#">Figure 6-2</a>	120			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output	$C_L = 2500\text{pF}$ , All drivers loaded,	$R_L = 3\text{k}\Omega$ , See <a href="#">Figure 6-2</a>		2		$\mu\text{s}$
$t_{PHL(D)}$	Propagation delay time, high- to low-level output	$C_L = 2500\text{pF}$ , All drivers loaded,	$R_L = 3\text{k}\Omega$ , See <a href="#">Figure 6-2</a>		2		$\mu\text{s}$
$t_{sk(p)}$	Pulse skew <sup>(2)</sup>	$C_L = 150\text{pF}$ to $2500\text{pF}$ ,	$R_L = 3\text{k}\Omega$ to $7\text{k}\Omega$ , See <a href="#">Figure 6-3</a>		300		ns

## 5.7 Switching Characteristics, Driver (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see <sup>(3)</sup>)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
SR(tr)	Slew rate, transition region (see <a href="#">Figure 6-2</a> )	$C_L = 50\text{pF}$ to $1000\text{pF}$ , $V_{CC} = 5\text{V}$ , $R_L = 3\text{k}\Omega$ to $7\text{k}\Omega$ ,	3	6	30	V/ $\mu\text{s}$

- (1) All typical values are at  $V_{CC} = 5\text{V}$ , and  $T_A = 25^\circ\text{C}$ .
- (2) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.
- (3) Test conditions are C1–C4 = 0.1 $\mu\text{F}$  at  $V_{CC} = 5\text{V} \pm 0.5\text{V}$ .

## 5.8 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see <sup>(2)</sup> and [Figure 8-1](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -1\text{mA}$	3.5	$V_{CC} - 0$	4 V	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 1.6\text{mA}$			0.4	V
$V_{IT+}$	Positive-going input threshold voltage	$V_{CC} = 5\text{V}$ , $T_A = 25^\circ\text{C}$		1.7	2.4	V
$V_{IT-}$	Negative-going input threshold voltage	$V_{CC} = 5\text{V}$ , $T_A = 25^\circ\text{C}$	0.8	1.2		V
$V_{hys}$	Input hysteresis ( $V_{IT+} - V_{IT-}$ )		0.2	0.5	1	V
$r_i$	Input resistance	$V_{CC} = 5\text{V}$ , $T_A = 25^\circ\text{C}$	3	5	7	k $\Omega$
	Output leakage current	$\overline{EN} = V_{CC}$ , $0 \leq RO_{UT} \leq V_{CC}$		$\pm 0.05$	$\pm 10$	$\mu\text{A}$

- (1) All typical values are at  $V_{CC} = 5\text{V}$ , and  $T_A = 25^\circ\text{C}$ .
- (2) Test conditions are C1–C4 = 0.1 $\mu\text{F}$  at  $V_{CC} = 5\text{V} \pm 0.5\text{V}$ .

## 5.9 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see <sup>(3)</sup>)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	$C_L = 150\text{pF}$ , See <a href="#">Figure 6-4</a>		0.5	10	$\mu\text{s}$
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	$C_L = 150\text{pF}$ , See <a href="#">Figure 6-4</a>		0.5	10	$\mu\text{s}$
$t_{en}$	Output enable time	$C_L = 150\text{pF}$ , See <a href="#">Figure 6-5</a> $R_L = 1\text{k}\Omega$ ,		600		ns
$t_{dis}$	Output disable time	$C_L = 150\text{pF}$ , See <a href="#">Figure 6-5</a> $R_L = 1\text{k}\Omega$ ,		200		ns
$t_{sk(p)}$	Pulse skew <sup>(2)</sup>	See <a href="#">Figure 6-3</a>		300		ns

- (1) All typical values are at  $V_{CC} = 5\text{V}$ , and  $T_A = 25^\circ\text{C}$ .
- (2) Pulse skew is defined as  $|t_{PLH} - t_{PHL}|$  of each channel of the same device.
- (3) Test conditions are C1–C4 = 0.1 $\mu\text{F}$ , at  $V_{CC} = 5\text{V} \pm 0.5\text{V}$ .

## 6 Parameter Measurement Information

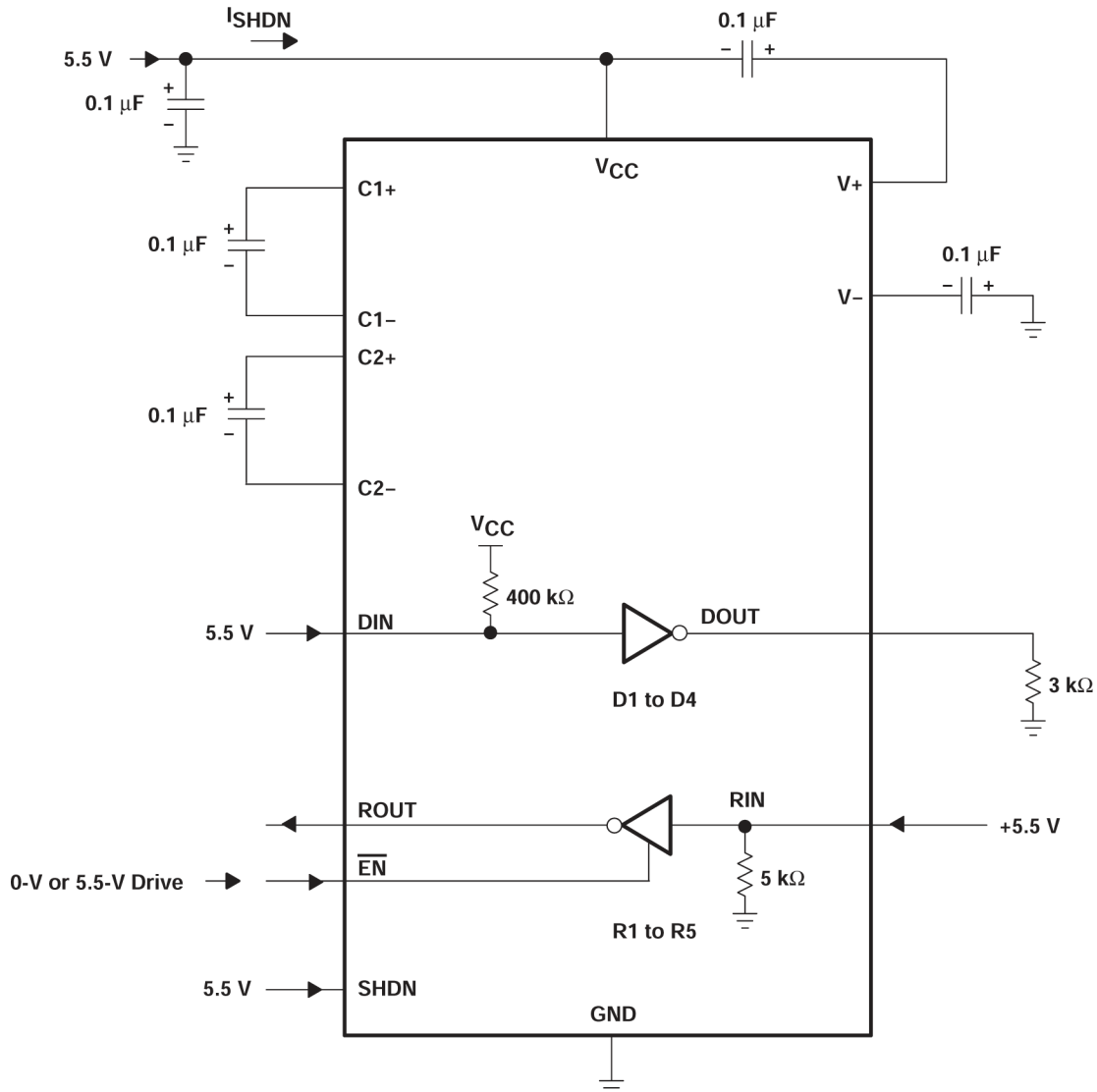
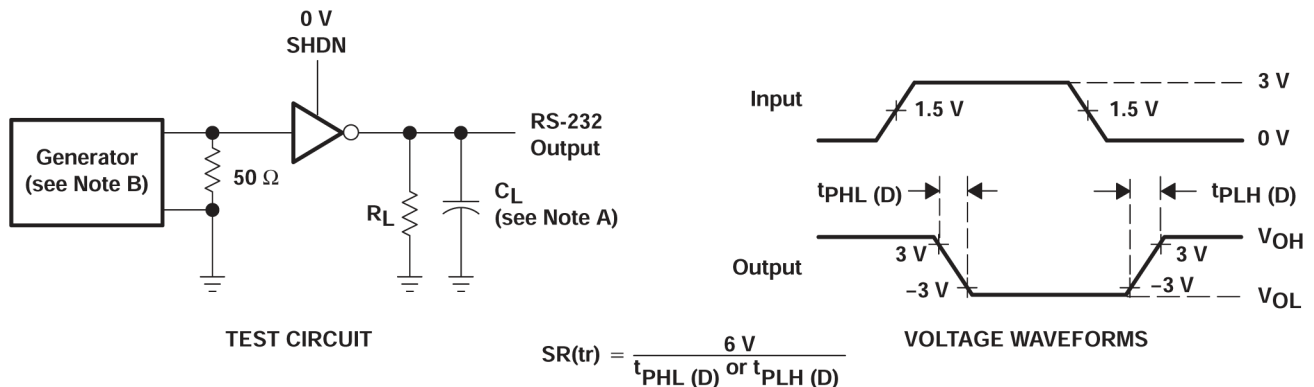


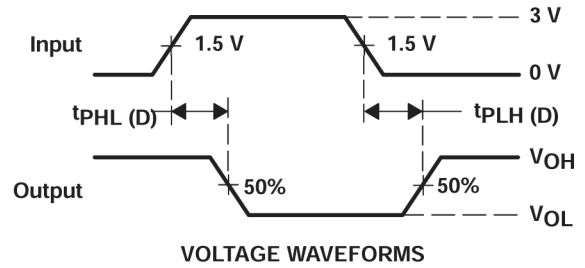
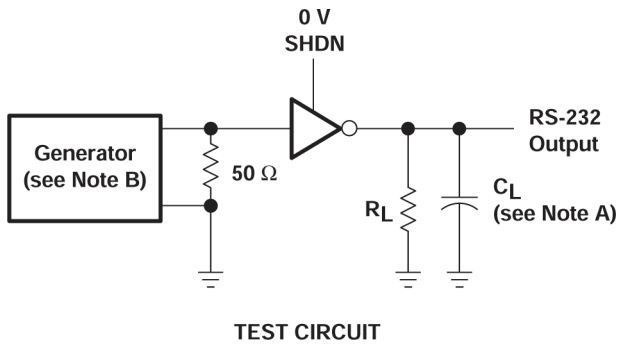
Figure 6-1. Shutdown Current Test Circuit



A.  $C_L$  includes probe and jig capacitance.

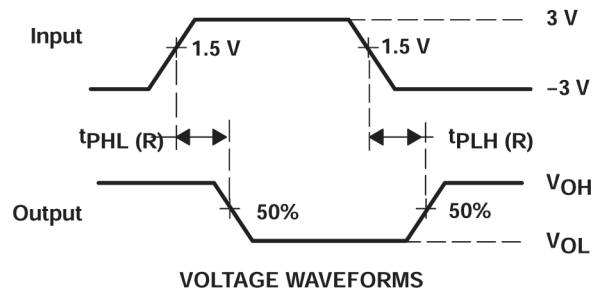
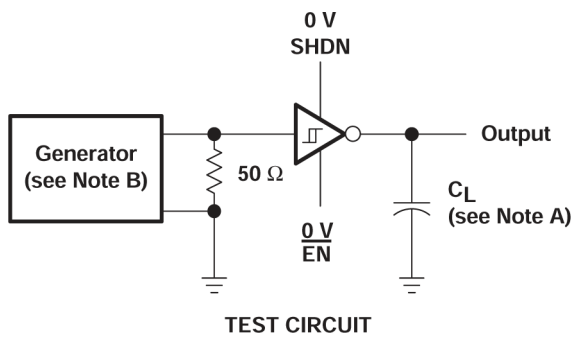
B. The pulse generator has the following characteristics: PRR = 120kbit/s,  $Z_O = 50\Omega$ , 50% duty cycle,  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ .

Figure 6-2. Driver Slew Rate and Propagation Delay Times



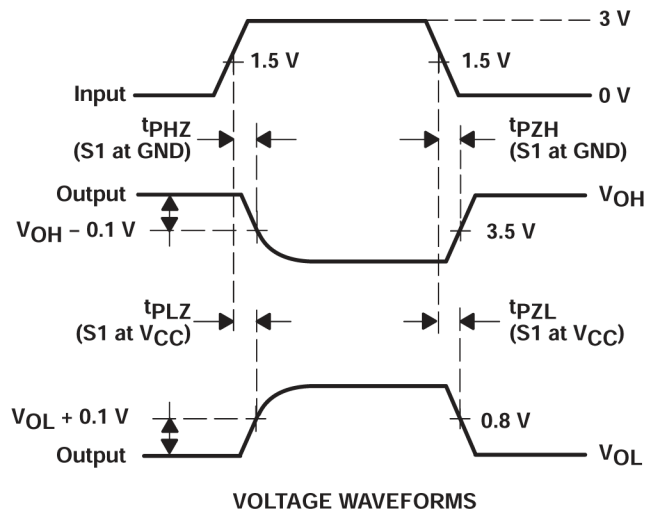
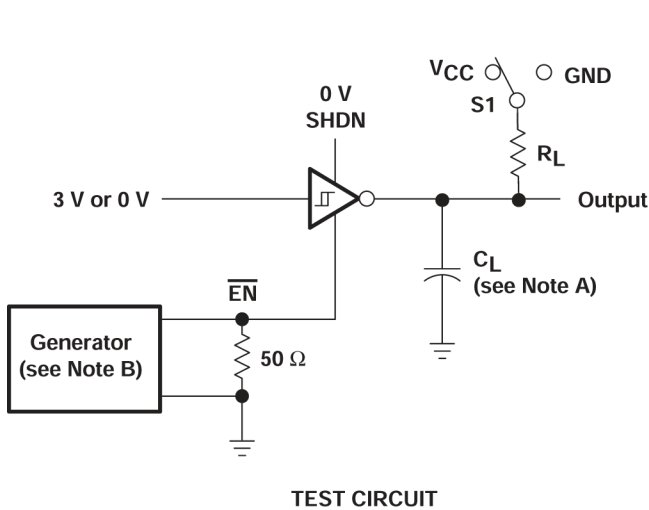
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 120kbit/s,  $Z_O = 50\Omega$ , 50% duty cycle,  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ .

**Figure 6-3. Driver Pulse Skew**



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50\Omega$ , 50% duty cycle,  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ .

**Figure 6-4. Receiver Propagation Delay Times**



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50\Omega$ , 50% duty cycle,  $t_r \leq 10\text{ns}$ ,  $t_f \leq 10\text{ns}$ .
- C.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- D.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

**Figure 6-5. Receiver Enable and Disable Times**



## 7 Device Functional Modes

**Table 7-1. Function Table**

INPUTS <sup>(1)</sup>		DRIVER	RECEIVER	DEVICE STATUS
SHDN	$\overline{\text{EN}}$			
L	L	All active	All active	Normal operation
L	H	All active	Z	Normal operation
H	X	Z	Z	Shutdown

(1) X = don't care, Z = high impedance

**Table 7-2. Function Table Each Driver**

INPUTS <sup>(1)</sup>		OUTPUT DOUT	DRIVER STATUS
DIN	SHDN		
L	L	H	Normal operation
H	L	L	
X	H	Z	Powered off

(1) X = don't care, Z = high impedance

**Table 7-3. Function Table Each Receiver**

INPUTS <sup>(1)</sup>		OUTPUT ROUT	RECEIVER STATUS
RIN	EN		
L	L	H	Normal operation
H	L	L	
X	H	Z	Powered off

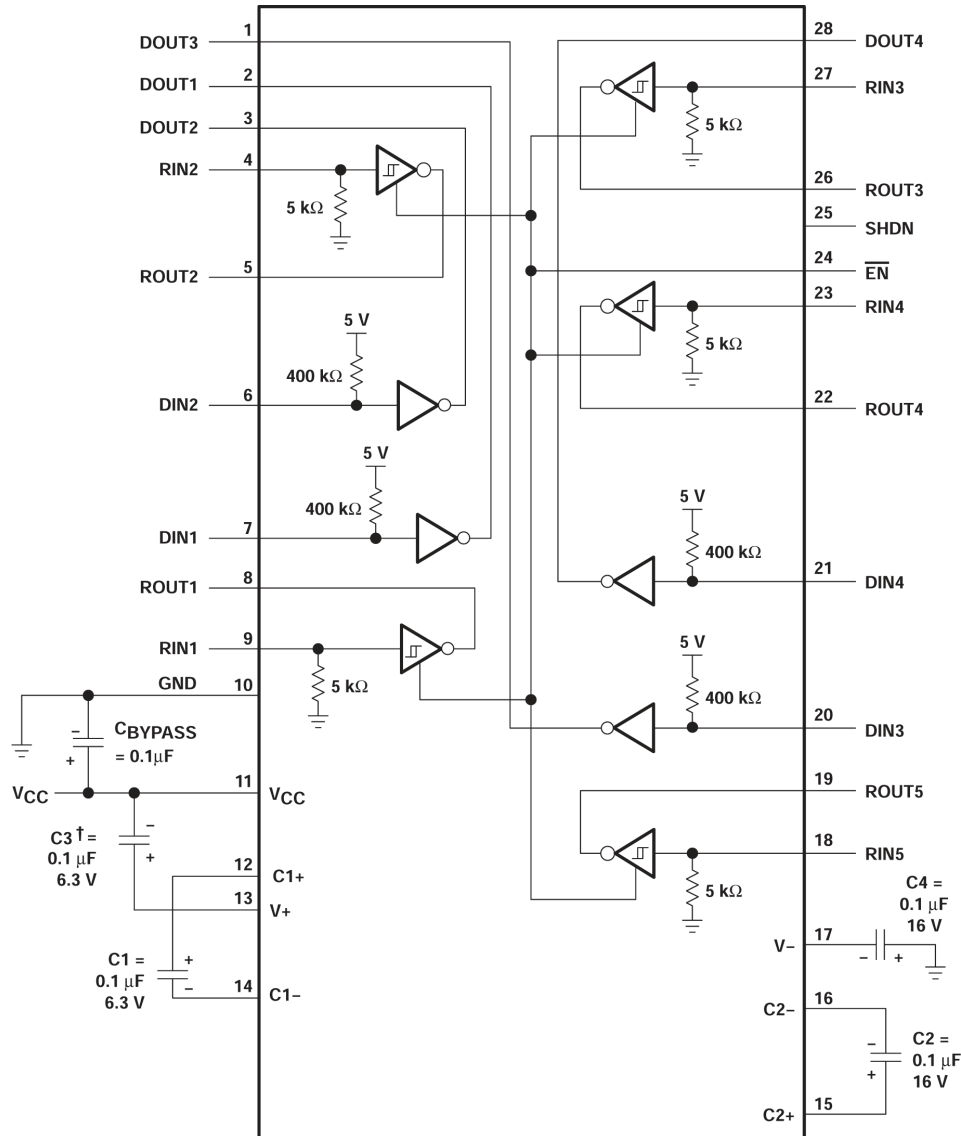
(1) X = don't care, Z = high impedance

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information



### Note

C3 can be connected to  $V_{CC}$  or GND.

- A. Resistor values shown are nominal.
- B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, connect the capacitors as shown.

**Figure 8-1. Typical Operating Circuit and Capacitor Values**

### 8.1.1 Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX211 requires 0.1 $\mu$ F capacitors, although capacitors up to 10 $\mu$ F can be used without harm. Ceramic dielectrics are suggested for the 0.1 $\mu$ F capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (2 $\times$ ) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10 $\mu$ F) to reduce the output impedance at V+ and V–.

Bypass V<sub>CC</sub> to ground with at least 0.1 $\mu$ F. In applications sensitive to power-supply noise generated by the charge pumps, decouple V<sub>CC</sub> to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

### 8.1.2 Electrostatic Discharge (ESD) Protection

Texas Instruments MAX211 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of  $\pm 15$ kV when powered down.

### 8.1.3 ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

### 8.1.4 Human-Body Model

The Human-Body Model (HBM) of ESD testing is shown in Figure 8-2. Figure 8-3 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100pF capacitor charged to the ESD voltage of concern and subsequently discharged into the DUT through a 1.5k $\Omega$  resistor.

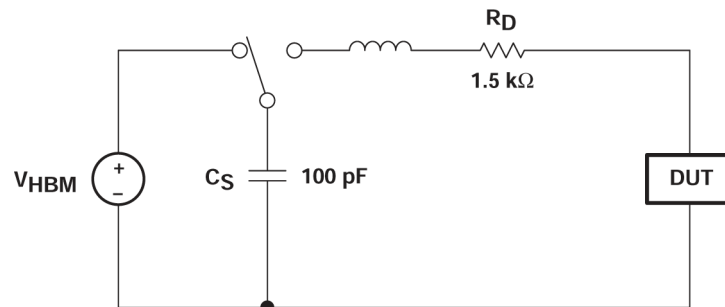


Figure 8-2. HBM ESD Test Circuit

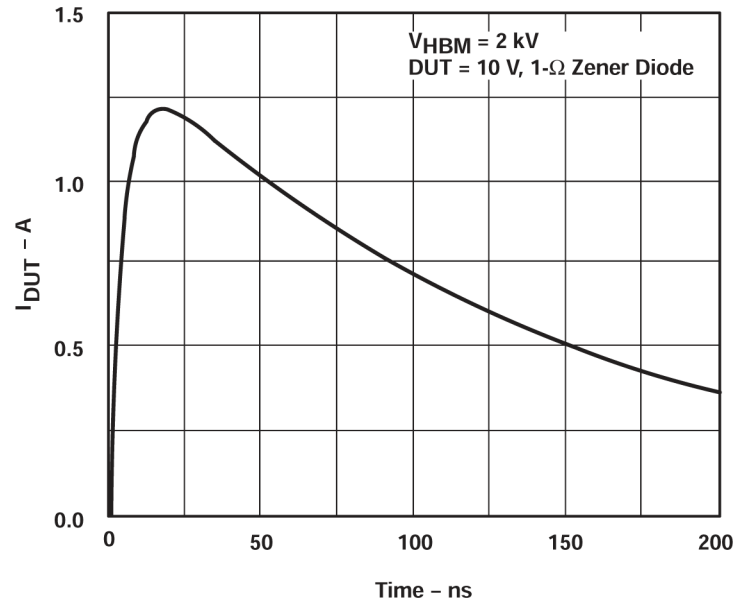


Figure 8-3. Typical HBM Current Waveform

### 8.1.5 Machine Model

The Machine Model (MM) ESD test applies to all pins, using a 200pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
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### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision E (January 2004) to Revision F (July 2024)</b>	<b>Page</b>
• Changed the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed the Input voltage range for Receivers from $\pm 30V$ to $\pm 25V$ for the DB package in the <i>Absolute Maximum Ratings</i> and the <i>Recommended Operating Conditions</i> .....	4
• Changed the Shutdown supply current for DB package TYP value from $1\mu A$ to $5\mu A$ <i>Electrical Characteristics</i> . .....	5

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX211CDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX211C	<a href="#">Samples</a>
MAX211IDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX211I	<a href="#">Samples</a>
MAX211IDBRG4	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX211I	<a href="#">Samples</a>
MAX211IDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX211I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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