SLAS619R – AUGUST 2010 – REVISED SEPTEMBER 2018

MSP430F51x2, MSP430F51x1 Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Low Supply-Voltage Range: 3.6 V Down to 1.8 V
- Ultra-Low Power Consumption
  - Active Mode (AM): 180 µA/MHz
  - Standby Mode (LPM3 WDT Mode, 3 V): 1.1 µA
  - Off Mode (LPM4 RAM Retention, 3 V): 0.9 µA
  - Shutdown Mode (LPM4.5, 3 V): 0.25 µA
- Wake up From Standby Mode in Less Than 5 µs
- 16-Bit RISC Architecture, Extended Memory, 40-ns Instruction Cycle Time
- Flexible Power-Management System
  - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
  - FLL Control Loop for Frequency Stabilization
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - Low-Frequency Trimmed Internal Reference Source (REFO)
  - 32-kHz Crystals (XT1)
  - High-Frequency Crystals up to 25 MHz (XT1)
- Hardware Multiplier Supports 32-Bit Operations
- 3-Channel DMA
- Up to Twelve 5-V-Tolerant Digital Push/Pull I/Os With up to 20-mA Drive Strength(1)
- 16-Bit Timer TD0 With Three Capture/Compare Registers and Support of High-Resolution Mode
- 16-Bit Timer TD1 With Three Capture/Compare Registers and Support of High-Resolution Mode
- 16-Bit Timer TA0 With Three Capture/Compare Registers
- Universal Serial Communication Interfaces (USCIs) (1)
  - USCI_A0 Supports:
    - Enhanced UART Supports Automatic Baud-Rate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI_B0 Supports:
    - I^2C
    - Synchronous SPI
- 10-Bit 200-ksps Analog-to-Digital Converter (ADC)
  - Internal Reference
  - Sample-and-Hold
  - Autoscan Feature
  - Up to 8 External Channels and 2 Internal Channels, Including Temperature Sensor(1)
- Up to 16-Channel On-Chip Comparator Including an Ultra-Low-Power Mode(1)
- Serial Onboard Programming, No External Programming Voltage Needed
- Device Comparison Summarizes the Available Family Members
- Available in 40-Pin QFN (RSB), 38-Pin TSSOP (DA), and 40-Pin Die-Sized BGA (YFF) Packages

(1) Full functionality in the 40-pin QFN package options. For the available features of other packages, see Signal Descriptions.

1.2 Applications

- Analog and Digital Sensor Systems
- LED Lighting
- Digital Power Supplies
- Motor Controls
- Remote Controls
- Thermostats

1.3 Description

The TI MSP family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the devices to wake up from low-power modes to active mode in less than 5 µs.

The MSP430F51x2 microcontrollers include two 16-bit high-resolution timers, two USCIs (USCI_A0 and USCI_B0), a 32-bit hardware multiplier, a high-performance 10-bit ADC, an on-chip comparator, a 3-channel DMA, 5-V tolerant I/Os, and up to 29 I/O pins.

The MSP430F51x1 microcontrollers include two 16-bit high-resolution timers, two USCIs (USCI_A0 and USCI_B0), a 32-bit hardware multiplier, an on-chip comparator, a 3-channel DMA, 5-V tolerant I/Os, and up to 29 I/O pins.

Typical applications for these devices include analog and digital sensor systems, LED lighting, digital power supplies, motor controls, remote controls, thermostats, digital timers, and hand-held meters.

For complete module descriptions, see the *MSP430F5xx and MSP430F6xx Family User's Guide*.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (2)
MSP430F5172IYFF	DSBGA (40)	See Section 8
MSP430F5172IRSB	WQFN (40)	5 mm × 5 mm
MSP430F5172IDA	TSSOP (38)	12.5 mm × 6.2 mm

(1) For the most current part, package, and ordering information, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) The dimensions shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 8.

1.4 Functional Block Diagrams

Figure 1-1 shows the functional block diagram for the MSP430F51x2 devices.

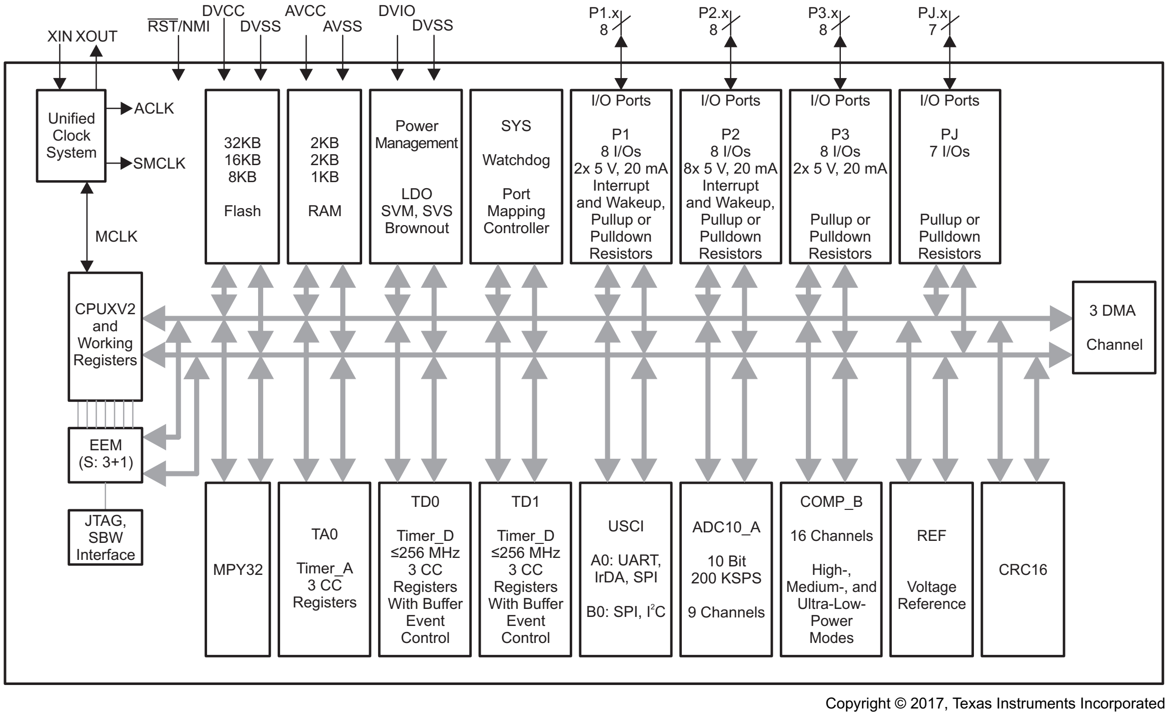

Figure 1-1. Functional Block Diagram, MSP430F51x2

Figure 1-2 shows the functional block diagram for the MSP430F51x1 devices.

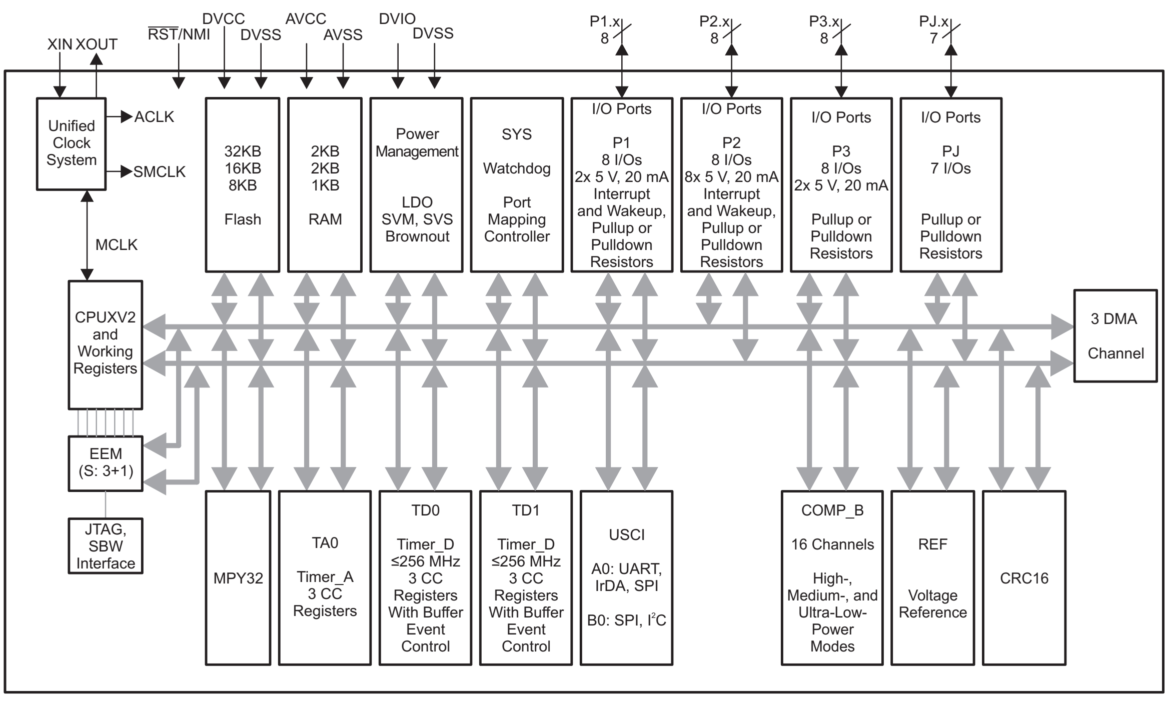

Figure 1-2. Functional Block Diagram, MSP430F51x1

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2 Revision History

Changes from July 20, 2018 to September 20, 2018 — **Page**

- Added typical conditions statements at the beginning of Section 5, *Specifications* 14
- Updated Section 7.4, *Documentation Support* 101

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison(1)(2)

<table>
<tr><th rowspan="2">DEVICE</th><th rowspan="2">FLASH (KB)</th><th rowspan="2">SRAM (KB)</th><th rowspan="2">Timer_A(3)</th><th rowspan="2">Timer_D(4)</th><th colspan="2">USCI</th><th rowspan="2">ADC10_A (Ch)</th><th rowspan="2">Comp_B (Ch)</th><th rowspan="2">I/Os</th><th rowspan="2">PACKAGE</th></tr>
<tr><th>CHANNEL A: UART, IrDA, SPI</th><th>CHANNEL B: SPI, I2C</th></tr>
<tr><td rowspan="3">MSP430F5172</td><td rowspan="3">32</td><td rowspan="3">2</td><td rowspan="3">3</td><td rowspan="3">3, 3</td><td rowspan="3">1</td><td rowspan="3">1</td><td rowspan="2">9 ext, 2 int</td><td rowspan="2">16</td><td rowspan="2">31</td><td>40 QFN</td></tr>
<tr><td>40 DSBGA</td></tr>
<tr><td>8 ext, 2 int</td><td>15</td><td>29</td><td>38 TSSOP</td></tr>
<tr><td rowspan="3">MSP430F5152</td><td rowspan="3">16</td><td rowspan="3">2</td><td rowspan="3">3</td><td rowspan="3">3, 3</td><td rowspan="3">1</td><td rowspan="3">1</td><td rowspan="2">9 ext, 2 int</td><td rowspan="2">16</td><td rowspan="2">31</td><td>40 QFN</td></tr>
<tr><td>40 DSBGA</td></tr>
<tr><td>8 ext, 2 int</td><td>15</td><td>29</td><td>38 TSSOP</td></tr>
<tr><td rowspan="3">MSP430F5132</td><td rowspan="3">8</td><td rowspan="3">1</td><td rowspan="3">3</td><td rowspan="3">3, 3</td><td rowspan="3">1</td><td rowspan="3">1</td><td rowspan="2">9 ext, 2 int</td><td rowspan="2">16</td><td rowspan="2">31</td><td>40 QFN</td></tr>
<tr><td>40 DSBGA</td></tr>
<tr><td>8 ext, 2 int</td><td>15</td><td>29</td><td>38 TSSOP</td></tr>
<tr><td rowspan="3">MSP430F5171</td><td rowspan="3">32</td><td rowspan="3">2</td><td rowspan="3">3</td><td rowspan="3">3, 3</td><td rowspan="3">1</td><td rowspan="3">1</td><td rowspan="3">–</td><td rowspan="2">16</td><td rowspan="2">31</td><td>40 QFN</td></tr>
<tr><td>40 DSBGA</td></tr>
<tr><td>15</td><td>29</td><td>38 TSSOP</td></tr>
<tr><td rowspan="3">MSP430F5151</td><td rowspan="3">16</td><td rowspan="3">2</td><td rowspan="3">3</td><td rowspan="3">3, 3</td><td rowspan="3">1</td><td rowspan="3">1</td><td rowspan="3">–</td><td rowspan="2">16</td><td rowspan="2">31</td><td>40 QFN</td></tr>
<tr><td>40 DSBGA</td></tr>
<tr><td>15</td><td>29</td><td>38 TSSOP</td></tr>
<tr><td rowspan="3">MSP430F5131</td><td rowspan="3">8</td><td rowspan="3">1</td><td rowspan="3">3</td><td rowspan="3">3, 3</td><td rowspan="3">1</td><td rowspan="3">1</td><td rowspan="3">–</td><td rowspan="2">16</td><td rowspan="2">31</td><td>40 QFN</td></tr>
<tr><td>40 DSBGA</td></tr>
<tr><td>15</td><td>29</td><td>38 TSSOP</td></tr>
</table>

(1) For the most current package and ordering information, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_D with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_D, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power sensing and measurement microcontrollers One platform. One ecosystem. Endless possibilities.

Products for MSP430 ultra-low-power microcontrollers MCUs for metrology, monitoring, system control, and communications

Companion Products for MSP430F5172 Review products that are frequently purchased or used in conjunction with this product.

Reference Designs for MSP430F5172 TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout for the 40-pin RSB package.

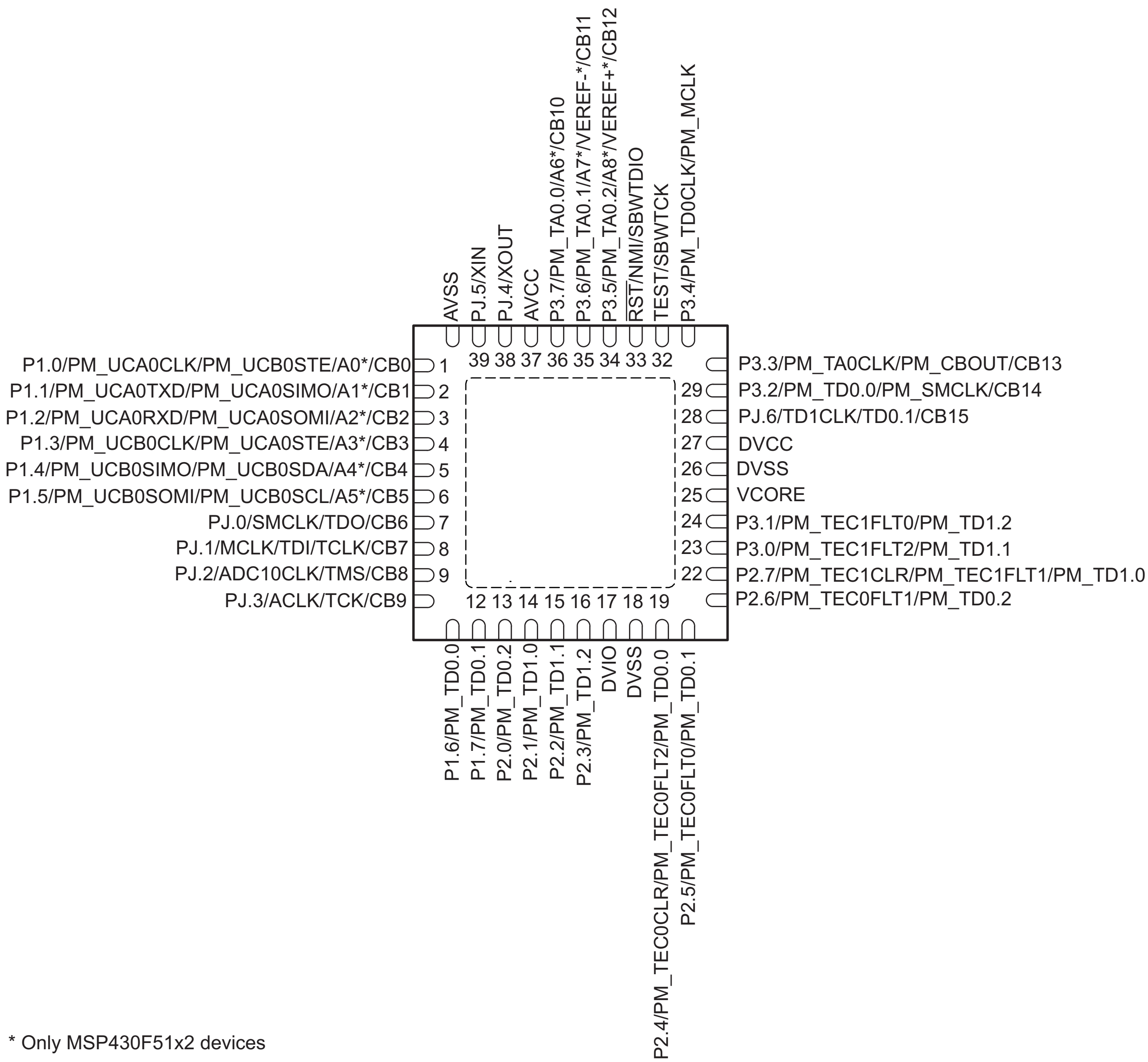


Figure 4-1. 40-Pin RSB Package (Top View)

Figure 4-2 shows the pinout for the 38-pin DA package.

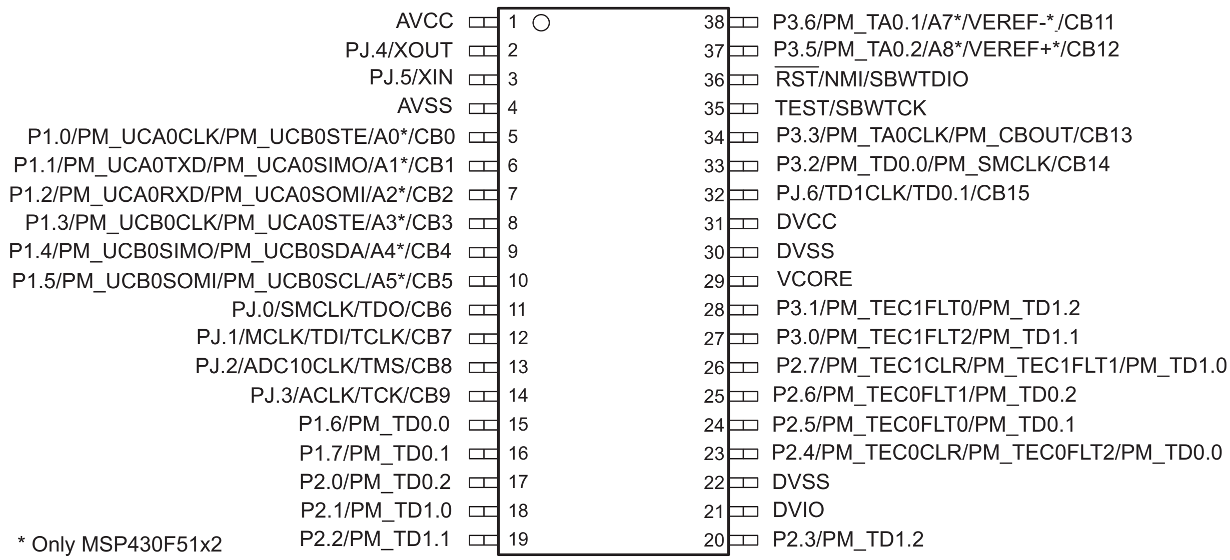


Figure 4-2. 38-Pin DA Package (Top View)

Figure 4-3 shows the pinout for the 40-pin YFF package. For the package dimensions, see the *Mechanical Data* in Section 8.

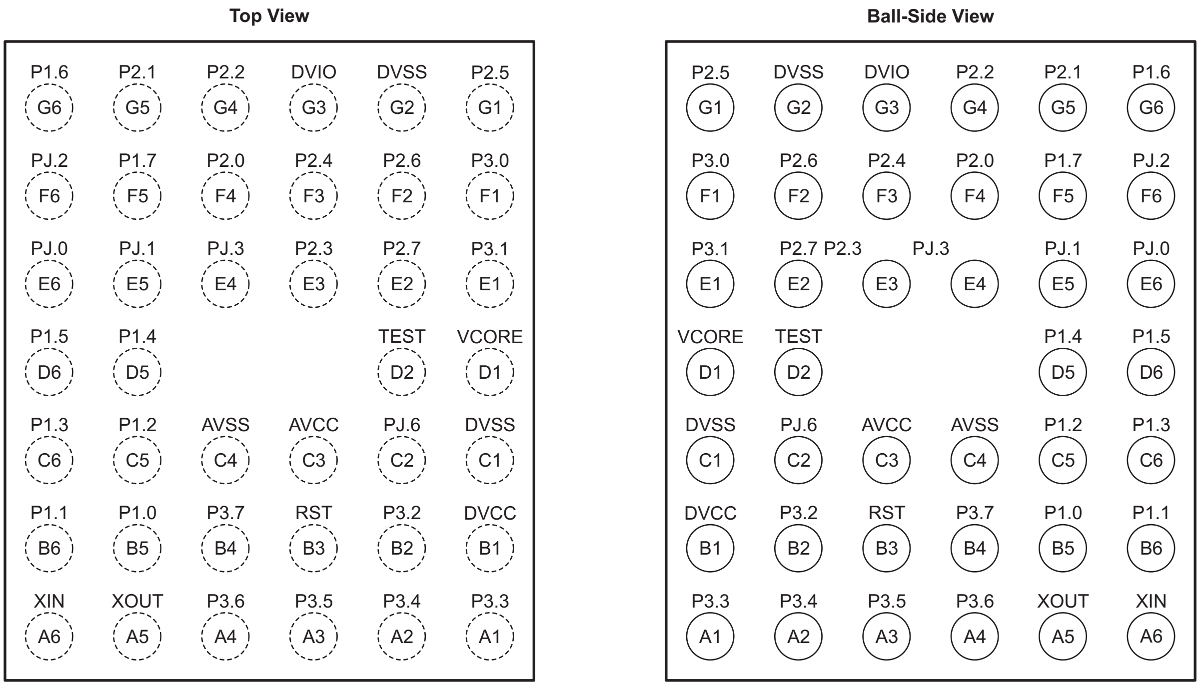


Figure 4-3. 40-Pin YFF Package (Top View and Bottom View)

4.2 Signal Descriptions

Table 4-1 describes the signals for all device and package variants.

Table 4-1. Signal Descriptions

TERMINAL				I/O (1)	DESCRIPTION
NAME	NO. (2)				
	RSB	DA	YFF		
P1.0/ PM_UCA0CLK/ PM_UCB0STE/ A0 (3)/ CB0	1	5	B5	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (4) Default mapping: Clock signal input – USCI_A0 SPI slave mode; Clock signal output – USCI_A0 SPI master mode Default mapping: Slave transmit enable – USCI_B0 SPI mode Analog input A0 – 10-bit ADC (3) Comparator_B Input 0
P1.1/ PM_UCA0TXD/ PM_UCA0SIMO/ A1 (3)/ CB1	2	6	B6	I/O	General-purpose digital I/O Default mapping: Transmit data – USCI_A0 UART mode Default mapping: Slave in, master out – USCI_A0 SPI mode Analog input A1 – 10-bit ADC (3) Comparator_B Input 1
P1.2/ PM_UCA0RXD/ PM_UCA0SOMI/ A2 (3)/ CB2	3	7	C5	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A0 UART mode Default mapping: Slave out, master in – USCI_A0 SPI mode Analog input A2 – 10-bit ADC (3) Comparator_B Input 2
P1.3/ PM_UCB0CLK/ PM_UCA0STE/ A3 (3)/ CB3	4	8	C6	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Clock signal input – USCI_B0 SPI slave mode; Clock signal output – USCI_B0 SPI master mode Default mapping: Slave transmit enable – USCI_A0 SPI mode Analog input A3 – 10-bit ADC (3) Comparator_B Input 3
P1.4/ PM_UCB0SIMO/ PM_UCB0SDA/ A4 (3)/ CB4	5	9	D5	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave in, master out – USCI_B0 SPI mode Default mapping: I^2C data – USCI_B0 I^2C mode Analog input A4 – 10-bit ADC (3) Comparator_B Input 4
P1.5/ PM_UCB0SOMI/ PM_UCB0SCL/ A5 (3)/ CB5	6	10	D6	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave out, master in – USCI_B0 SPI mode Default mapping: I^2C clock – USCI_B0 I^2C mode Analog input A5 – 10-bit ADC (3) Comparator_B Input 5
PJ.0/ SMCLK/ TDO/ CB6	7	11	E6	I/O	General-purpose digital I/O SMCLK clock output Test data output port Comparator_B Input 6
PJ.1/ MCLK/ TDI/TCLK/ CB7	8	12	E5	I/O	General-purpose digital I/O MCLK clock output Test data input or test clock input Comparator_B Input 7
PJ.2/ ADC10CLK/ TMS/ CB8	9	13	F6	I/O	General-purpose digital I/O ADC10_A clock output Test mode select Comparator_B Input 8
PJ.3/ ACLK/ TCK/ CB9	10	14	E4	I/O	General-purpose digital I/O ACLK output port Test clock Comparator_B Input 9
P1.6/ PM_TD0.0	11	15	G6	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD0 CCR0 compare output/capture input

(1) I = input, O = output
(2) N/A = not available on this package offering
(3) The ADC10_A module is available on MSP430F51x2 devices. The secondary pin functions Ax (ADC10_A channel x) available only in MSP430F51x2 devices.
(4) For details on the Port Mapping Controller, see Section 6.9.2.

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O (1)	DESCRIPTION
NAME	NO. (2)				
	RSB	DA	YFF		
P1.7/ PM_TD0.1	12	16	F5	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD0 CCR1 compare output/capture input
P2.0/ PM_TD0.2	13	17	F4	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD0 CCR2 compare output/capture input
P2.1/ PM_TD1.0	14	18	G5	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD1 CCR0 compare output/capture input
P2.2/ PM_TD1.1	15	19	G4	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD1 CCR1 compare output/capture input
P2.3/ PM_TD1.2	16	20	E3	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD1 CCR2 compare output/capture input
DVIO	17	21	G3		5-V tolerant digital I/O power supply
DVSS	18	22	G2		Digital ground supply
P2.4/ PM_TEC0CLR/ PM_TEC0FLT2/ PM_TD0.0	19	23	F3	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD0 external clear input Default mapping: TD0 fault input channel 2 (controlled by module input enable) Default mapping: TD0 CCR0 compare output
P2.5/ PM_TEC0FLT0/ PM_TD0.1	20	24	G1	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD0 fault input channel 0 Default mapping: TD0 CCR1 compare output
P2.6/ PM_TEC0FLT1/ PM_TD0.2	21	25	F2	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD0 fault input channel 1 Default mapping: TD0 CCR2 compare output
P2.7/ PM_TEC1CLR/ PM_TEC1FLT1/ PM_TD1.0	22	26	E2	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD1 external clear Default mapping: TD1 fault input channel 1 (controlled by module input enable) Default mapping: TD1 CCR0 compare output
P3.0/ PM_TEC1FLT2/ PM_TD1.1	23	27	F1	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD1 fault input channel 2 Default mapping: TD1 CCR1 compare output
P3.1/ PM_TEC1FLT0/ PM_TD1.2	24	28	E1	I/O, DV_{IO}	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD1 fault input channel 0 Default mapping: TD1 CCR2 compare output
VCORE	25	29	D1		Regulated core power supply
DVSS	26	30	C1		Digital ground supply
DVCC	27	31	B1		Digital power supply
PJ.6/ TD1CLK/ TD0.1/ CB15	28	32	C2	I/O	General-purpose digital I/O TD1 clock input TD0 CCR1 compare output Comparator_B Input 15
P3.2/ PM_TD0.0/ PM_SMCLK/ CB14	29	33	B2	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD0 CCR0 capture input Default mapping: SMCLK output Comparator_B Input 14
P3.3/ PM_TA0CLK/ PM_CBOUT/ CB13	30	34	A1	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TA0 clock input Default mapping: Comparator_B output Comparator_B Input 13
P3.4/ PM_TD0CLK/ PM_MCLK	31	–	A2	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TD0 clock input Default mapping: MCLK output
TEST/ SBWTCK	32	35	D2		Test mode pin – select digital I/O on JTAG pins Spy-Bi-Wire input clock
$\overline{RST}$/ NMI/ SBWTDIO	33	36	B3		Reset input active low (5) Nonmaskable interrupt input Spy-Bi-Wire data input/output

(5) When this pin is configured as reset, the internal pullup resistor is enabled by default.

Table 4-1. Signal Descriptions (continued)

TERMINAL				I/O (1)	DESCRIPTION
NAME	NO. (2) RSB	DA	YFF		
P3.5/ PM_TA0.2/ A8 (3) VEREF+/ CB12	34	37	A3	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TA0 CCR2 compare output/capture input Analog input A8 – 10-bit ADC (3) Positive terminal for the ADC reference voltage for an external applied reference voltage Comparator_B Input 12
P3.6/ PM_TA0.1/ A7 (3)/ VEREF-/ CB11	35	38	A4	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TA0 CCR1 compare output/capture input Analog input A7 – 10-bit ADC (3) Negative terminal for the ADC reference voltage for an external applied reference voltage Comparator_B Input 11
P3.7/ PM_TA0.0/ A6 (3)/ CB10	36	–	B4	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: TA0 CCR0 compare output/capture input Analog input A6 – 10-bit ADC (3) Comparator_B Input 10
AVCC	37	1	C3		Analog power supply
PJ.4/ XOUT	38	2	A5	I/O	General-purpose digital I/O Output terminal of crystal oscillator
PJ.5/ XIN	39	3	A6	I/O	General-purpose digital I/O Input terminal for crystal oscillator
AVSS	40	4	C4		Analog ground supply
QFN pad	–	NA	NA		Recommended to connect to DVSS externally

5 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage V_{CC} applied at DVCC to DVSS	–0.3	4.1 V	V
Voltage V_{IO} applied at VIO to DVSS	–0.3	6.1 V	V
Voltage applied to any pin (excluding VCORE)(2)	–0.3	V_{CC} + 0.3	V
Diode current at any device pin		±2	mA
Maximum operating junction temperature, T_J		95	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. V_{CORE} is for internal device usage only. No external DC loading or voltage should be applied.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

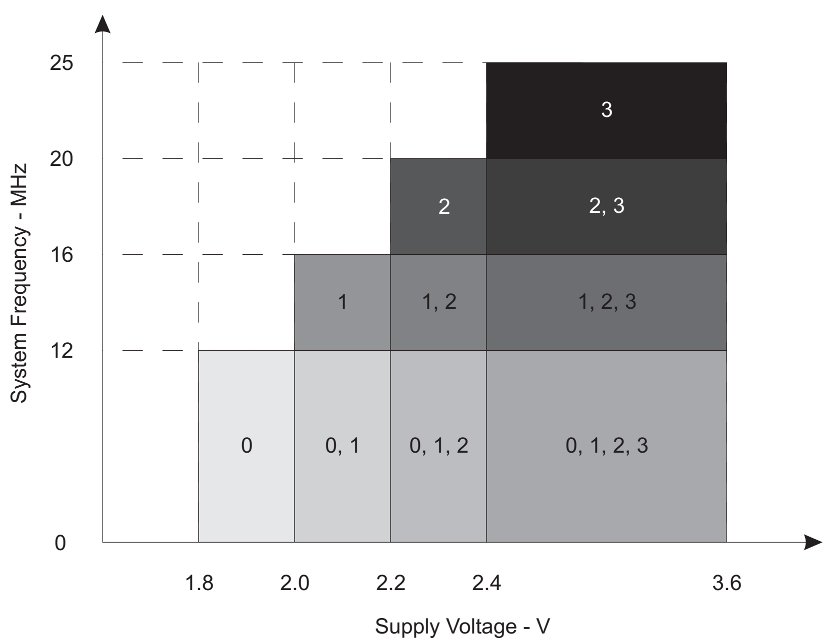
			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming $V_{(AVCC)}$ = $V_{(DVCC)}$ = V_{CC}(1)(2)	PMMCOREVx = 0	1.8		3.6	V
		PMMCOREVx = 0, 1	2.0		3.6	
		PMMCOREVx = 0, 1, 2	2.2		3.6	
		PMMCOREVx = 0, 1, 2, 3	2.4		3.6	
V_{IO}	Supply voltage of pins P1.6, P1.7, P2.0 to P2.7, P3.0, and P3.1 supplied by VIO(3)(4)		1.8		5.5	V
V_{SS}	Supply voltage $V_{(AVSS)}$ = $V^{(DVSS)}$ = V_{SS}			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
$C_{(VCORE)}$	Recommended capacitor at VCORE(5)			470		nF
$C_{(DVCC)}$/ $C_{(VCORE)}$	Capacitor ratio of DVCC to VCORE		10			

(1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between $V_{(AVCC)}$ and $V_{(DVCC)}$ can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the Section 5.28 threshold parameters for the exact values and further details.
(3) If DVIO is not supplied by the same source as DVCC, TI recommends powering AVCC and DVCC before powering DVIO. At DVCC and AVCC voltages higher than 1.8 V, the maximum difference of 0.3 V between DVIO and (DVCC and AVCC) can be exceeded. DVIO must be higher than or equal to DVCC.
Increased cross current can flow into DVCC if DVIO is less than (DVCC – 0.3 V), with a maximum current flowing when DVIO is equal to DVCC/2. To avoid high currents into DVCC, DVIO must be higher than or equal to DVCC, DVIO must not float, and DVIO must be turned off quickly. TI recommends pulling the DVIO pins to low before disabling DVIO.
(4) For best cross-current prevention, voltage applied to DVIO should not be lower than DVCC. However, if DVIO is switched off during operation, due to application requirements, DVIO should be pulled to ground to prevent a floating voltage.
(5) A capacitor tolerance of ±20% or better is required.

Recommended Operating Conditions *(continued)*

			MIN	NOM	MAX	UNIT
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(6) (7) (see Figure 5-1)	PMMCOREVx = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V (default condition)	0		12	MHz
		PMMCOREVx = 1, 2.0 V ≤ V_{CC} ≤ 3.6 V	0		16	
		PMMCOREVx = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	0		20	
		PMMCOREVx = 3, 2.4 V ≤ V_{CC} ≤ 3.6 V	0		25	
P_{INT}	Internal power dissipation		$V_{CC} \times I_{(DVCC)}$			W
P_{IO}	I/O power dissipation of the I/O pins powered by DVCC		$(V_{CC} - V_{IOH}) \times I_{IOH} + V_{IOL} \times I_{IOL}$			W
P_{IO5}	I/O power dissipation of the I/O pins powered by VIO		$(V_{IO} - V_{IOH5}) \times I_{IOH5} + V_{IOL5} \times I_{IOL5}$			W
P_{MAX}	Maximum allowed power dissipation, $P_{MAX} > P_{IO} + P_{IO5} + P_{INT}$		$(T_J - T_A) / R\theta_{JA}$			W

(6) The MSP430™ CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
(7) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

Figure 5-1. Frequency vs Supply Voltage

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREVx	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) 1 MHz TYP	1 MHz MAX	8 MHz TYP	8 MHz MAX	12 MHz TYP	12 MHz MAX	20 MHz TYP	20 MHz MAX	25 MHz TYP	25 MHz MAX	UNIT
$I_{AM,\ Flash}$	Flash	3 V	0	0.24	0.27	1.48	1.60							mA
			1	0.26		1.66		2.48	2.7					
			2	0.28		1.83		2.72		4.50	4.8			
			3	0.28		1.83		2.66		4.40		5.60	6.15	
$I_{AM,\ RAM}$	RAM	3 V	0	0.17	0.2	0.89	0.97							mA
			1	0.18		1.00		1.49	1.62					
			2	0.20		1.14		1.68		2.75	3.0			
			3	0.20		1.20		1.78		2.92		3.64	4.0	

5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		V_{CC}	PMMCOREVx	–40°C TYP	–40°C MAX	25°C TYP	25°C MAX	60°C TYP	60°C MAX	85°C TYP	85°C MAX	UNIT
$I_{LPM0,\ 1MHz}$	Low-power mode 0	2.2 V	0	82	90	85	90	87	95	85	100	µA
		3 V	3	88	100	85	100	90	104	88	104	
I_{LPM2}	Low-power mode 2	2.2 V	0	10	12.5	10	12	10	12.5	12.5	13	µA
		3 V	3	9	11.5	11	13	11	15	12	14	
$I_{LPM3,\ XT1LF}$	Low-power mode 3, crystal mode	2.2 V	0	1.7	–	1.8	2.0	2.5	–	3.5	6.0	µA
		3 V		2.0	–	2.0	2.2	3.0	–	3.7	6.0	
		2.2 V	1	1.8	–	1.9	–	2.5	–	4.0	–	
		3 V		2.1	–	2.2	–	2.5	–	4.0	–	
		2.2 V	2	1.8	–	2.0	–	2.5	–	4.2	–	
		3 V		2.0	–	2.2	–	2.8	–	4.2	–	
		2.2 V	3	1.9	–	2.0	2.5	2.9	–	4.8	6.5	
		3 V		2.1	–	2.2	2.5	3.0	–	5.2	7.0	
$I_{LPM3,\ VLO}$	Low-power mode 3, VLO mode	2.2 V	0	1.0	–	1.0	1.25	1.6	–	3.5	4.5	µA
		3 V		1.1	–	1.2	1.4	1.5	–	3.6	5.0	
		2.2 V	1	1.0	–	1.1	–	1.8	–	3.0	–	
		3 V		1.3	–	1.1	–	2.0	–	3.2	–	
		2.2 V	2	1.1	–	1.1	–	1.8	–	3.1	–	
		3 V		1.1	–	1.2	–	2.0	–	3.2	–	
		2.2 V	3	1.1	–	1.1	1.4	1.9	–	3.5	5.0	
		3 V		1.1	–	1.2	1.5	2.1	–	4.0	5.2	
I_{LPM4}	Low-power mode 4	3 V	0	0.8	–	0.9	1.3	1.4	–	3.5	4.7	µA
			1	0.8	–	1.0	–	1.4	–	3.5	–	
			2	0.8	–	1.0	–	1.5	–	3.6	–	
			3	0.9	–	1.0	1.3	1.6	–	3.6	5.0	
$I_{LPM4.5}$	Low-power mode 4.5	2.2 V	x	0.06	–	0.20	0.26	0.33	–	0.60	0.9	µA
		3 V	x	0.07	–	0.25	0.29	0.37	–	0.77	0.9	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. DVIO = DVCC = AVCC.
(2) The currents are characterized with a Micro Crystal MS1V-T1K SMD crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.

5.6 Thermal Resistance Characteristics

THERMAL METRIC				VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air	Low-K board (JESD51-3)	QFN (RSB)	87	°C/W
			TSSOP (DA)	109	
		High-K board (JESD51-7)	QFN (RSB)	35	
			TSSOP (DA)	69	
θ_{JC}	Junction-to-case thermal resistance		QFN (RSB)	36	°C/W
			TSSOP (DA)	19	

5.7 Schmitt-Trigger Inputs – General-Purpose I/O (P1.0 to P1.5, P3.2 to P3.7, and PJ.0 to PJ.6)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		1.8 V	0.3		0.8	V
			3 V	0.4		1.0	
R_{Pull}	Pullup or pulldown resistor[1]	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

(1) Also applies to $\overline{RST}$ pin when pullup or pulldown resistor is enabled.

5.8 Schmitt-Trigger Inputs – General-Purpose I/O (P1.6 and P1.7, P2.0 to P2.7, and P3.0 and P3.1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{IO}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.20		2.00	
			5 V	2.10		2.50	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		0.90	V
			3 V	0.75		1.30	
			5 V	1.10		1.60	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		1.8 V	0.27		0.45	V
			3 V	0.45		0.65	
			5 V	0.9		1.2	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

5.9 Inputs – Ports P1 and P2[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC} or V_{IO}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing[2]	Port P1.0 to P1.5, external trigger pulse duration to set interrupt flag	1.8 V to 3.6 V	20		ns
		Port P1.6 and P1.7 and P2.0 to P2.7, external trigger pulse duration to set interrupt flag	1.8 V to 5 V	25		

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

5.10 Leakage Current – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	Port P1.0 to P1.5, P3.0 to P3.7, PJ.0 to PJ.6	See (1) (2)	1.8 V to 3.6 V		±1	±50	nA
		Port P1.6 and P1.7, P2.0 to P2.7		1.8 V to 5 V		±1	±50	

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

5.11 Outputs – Ports P1, P3, PJ (Full Drive Strength, P1.0 to P1.5, P3.2 to P3.7, PJ.0 to PJ.6)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA (1)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –10 mA (2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –5 mA (1)	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –15 mA (2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA (1)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 10 mA (2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 5 mA (1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 15 mA (2)		V_{SS}	V_{SS} + 0.60	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

5.12 Outputs – Ports P1 to P3 (Full Drive Strength, P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{IO}	MIN	MAX	UNIT
V_{OH5}	High-level output voltage	$I_{(OH5max)}$ = –3 mA (1)	1.8 V	V_{IO} – 0.25	V_{IO}	V
		$I_{(OH5max)}$ = –10 mA (2)		V_{IO} – 0.60	V_{IO}	
		$I_{(OH5max)}$ = –5 mA (1)	3 V	V_{IO} – 0.25	V_{IO}	
		$I_{(OH5max)}$ = –15 mA (2)		V_{IO} – 0.60	V_{IO}	
		$I_{(OH5max)}$ = –7 mA (1)	5 V	V_{IO} – 0.25	V_{IO}	
		$I_{(OH5max)}$ = –20 mA (2)		V_{IO} – 0.60	V_{IO}	
V_{OL5}	Low-level output voltage	$I_{(OL5max)}$ = 3 mA (1)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OL5max)}$ = 10 mA (2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OL5max)}$ = 5 mA (1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OL5max)}$ = 15 mA (2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OL5max)}$ = 7 mA (1)	5 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OL5max)}$ = 20 mA (2)		V_{SS}	V_{SS} + 0.60	

(1) The maximum total current, $I_{(OH5max)}$ and $I_{(OL5max)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OH5max)}$ and $I_{(OL5max)}$, for all outputs combined should not exceed ±200 mA to hold the maximum voltage drop specified.

5.13 Outputs – Ports P1, P3, PJ (Reduced Drive Strength, P1.0 to P1.5, P3.2 to P3.7, PJ.0 to PJ.6)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA(2)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA(3)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA(2)	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA(3)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA(2)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA(3)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA(2)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA(3)		V_{SS}	V_{SS} + 0.60	

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

5.14 Outputs – Ports P1 to P3 (Reduced Drive Strength, P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{IO}	MIN	MAX	UNIT
V_{OH5}	High-level output voltage	$I_{(OH5max)}$ = –1 mA(2)	1.8 V	V_{IO} – 0.25	V_{IO}	V
		$I_{(OH5max)}$ = –3 mA(3)		V_{IO} – 0.60	V_{IO}	
		$I_{(OH5max)}$ = –2 mA(2)	3 V	V_{IO} – 0.25	V_{IO}	
		$I_{(OH5max)}$ = –6 mA(3)		V_{IO} – 0.60	V_{IO}	
		$I_{(OH5max)}$ = –4 mA(2)	5.0 V	V_{IO} – 0.25	V_{IO}	
		$I_{(OH5max)}$ = –12 mA(3)		V_{IO} – 0.60	V_{IO}	
V_{OL5}	Low-level output voltage	$I_{(OL5max)}$ = 1 mA(2)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OL5max)}$ = 3 mA(3)		V_{SS}	V_{SS} + 0.60	
		$I_{(OL5max)}$ = 2 mA(2)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OL5max)}$ = 6 mA(3)		V_{SS}	V_{SS} + 0.60	
		$I_{(OH5max)}$ = 4 mA(2)	5.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OL5max)}$ = 12 mA(3)		V_{SS}	V_{SS} + 0.60	

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OH5max)}$ and $I_{(OL5max)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OH5max)}$ and $I_{(OL5max)}$, for all outputs combined, should not exceed ±200 mA to hold the maximum voltage drop specified.

5.15 Output Frequency – Ports P1.0 to P1.5, P3.2 to P3.7, PJ.0 to PJ.6

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	PJ.0/SMCLK C_L = 20 pF, R_L = 1 kΩ(1) (2)	V_{CC} = 1.8 V, PMMCOREVx = 0	16		MHz
			V_{CC} = 3 V, PMMCOREVx = 3	25		
f_{Port_CLK}	Clock output frequency	PJ.3/ACLK PJ.0/SMCLK PJ.1/MCLK C_L = 20 pF(2)	V_{CC} = 1.8 V, PMMCOREVx = 0	16		MHz
			V_{CC} = 3 V, PMMCOREVx = 3	25		

(1) A resistive divider with 2 × 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.16 Output Frequency – Ports P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.6 port mapper SMCLK from P3.4, C_L = 20 pF, R_L = 1 kΩ(1) (2)	V_{CC} = 1.8 V, V_{IO} = 1.8 V, PMMCOREVx = 0	16		MHz
			V_{CC} = 3 V, V_{IO} = 3 V, PMMCOREVx = 3	25		
			V_{CC} = 3 V, V_{IO} = 5 V, PMMCOREVx = 3	25		
f_{Port_CLK}	Clock output frequency	P1.6 port mapper SMCLK from P3.4, C_L = 20 pF(2)	V_{CC} = 1.8 V, V_{IO} = 1.8 V, PMMCOREVx = 0	16		MHz
			V_{CC} = 3 V, V_{IO} = 3 V, PMMCOREVx = 3	25		
			V_{CC} = 3 V, V_{IO} = 5 V, PMMCOREVx = 3	25		

(1) A resistive divider with 2 × 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.17 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0), Ports P1.0 to P1.5, P3.2 to P3.7, PJ.0 to PJ.6

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

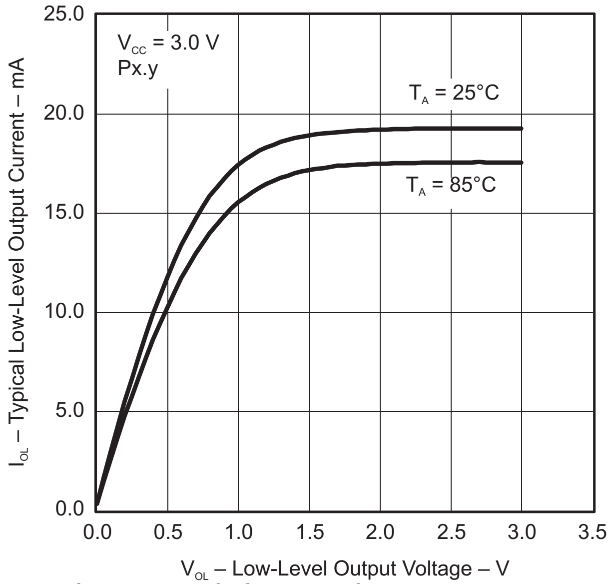


Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage

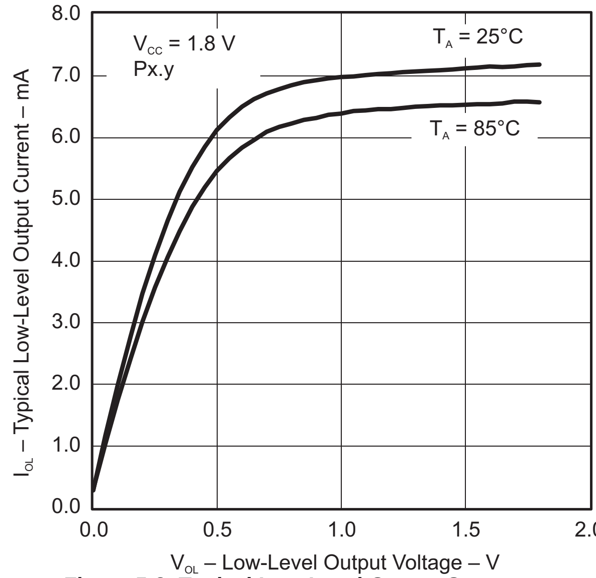


Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

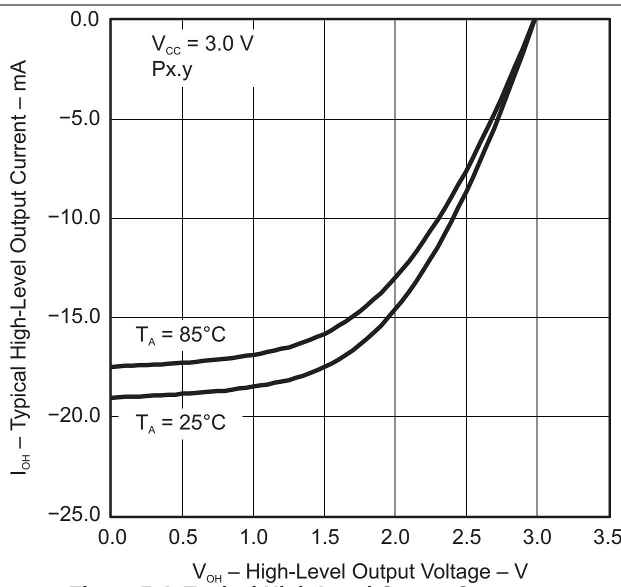


Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage

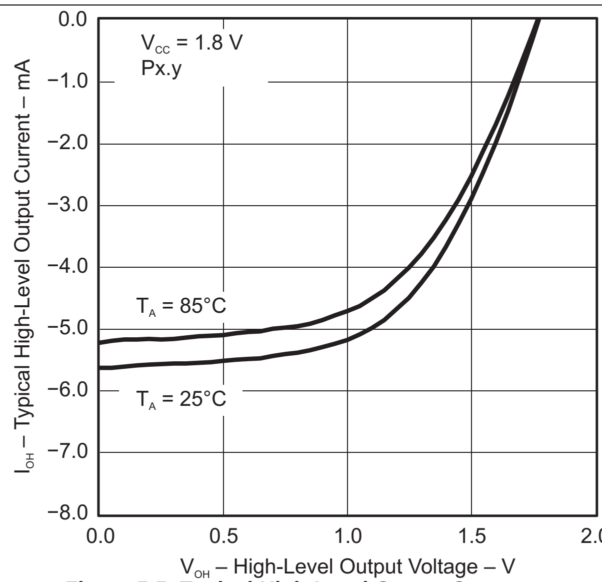


Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

5.18 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1), Ports P1.0 to P1.5, P3.2 to P3.7, PJ.0 to PJ.6

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

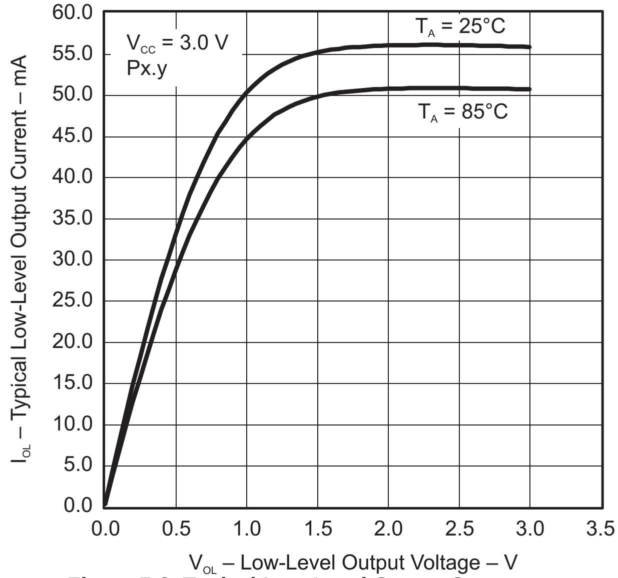


Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage

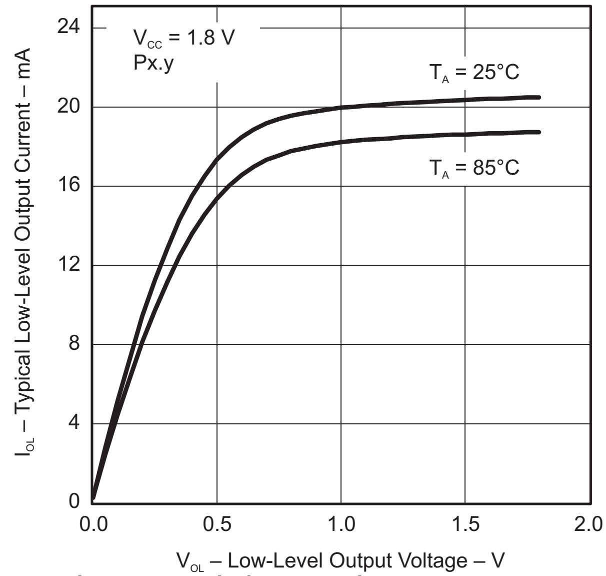


Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage

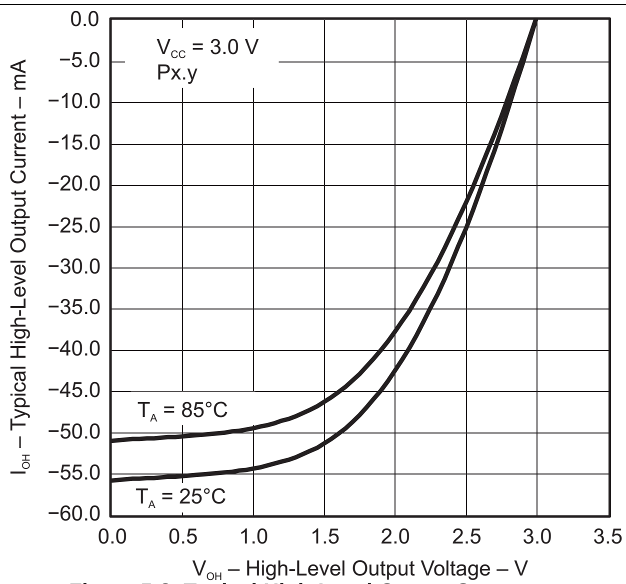


Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage

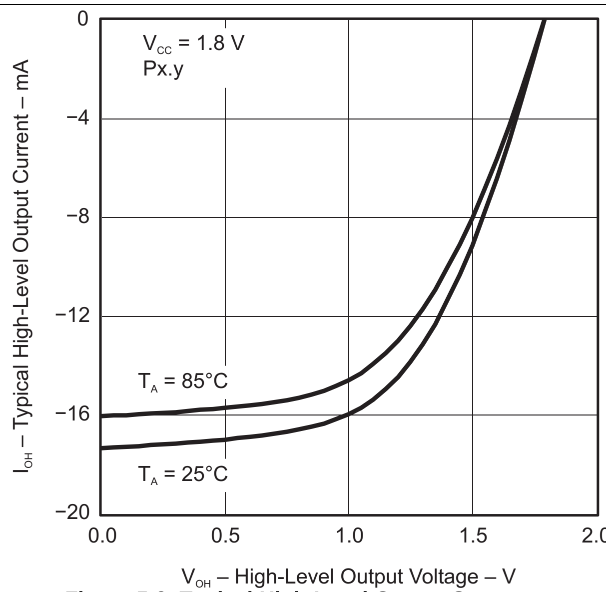


Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage

5.19 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0), Ports P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

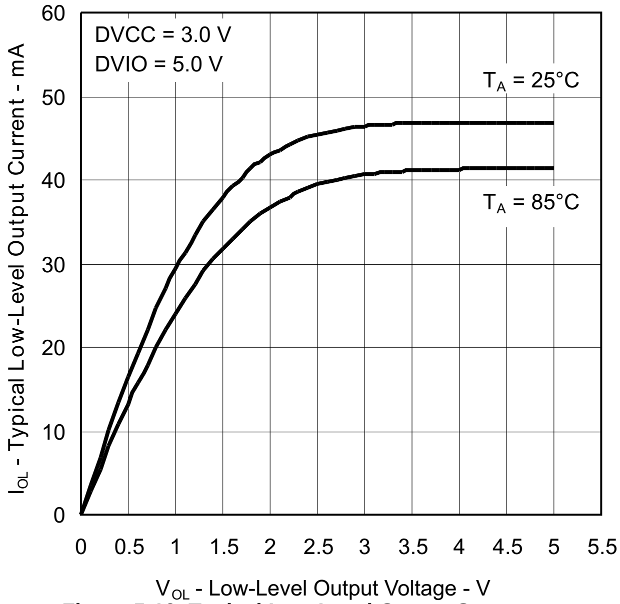


Figure 5-10. Typical Low-Level Output Current vs Low-Level Output Voltage

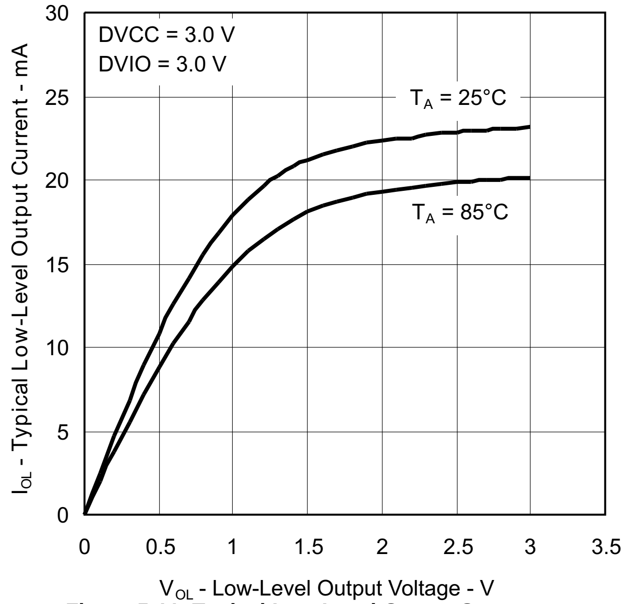


Figure 5-11. Typical Low-Level Output Current vs Low-Level Output Voltage

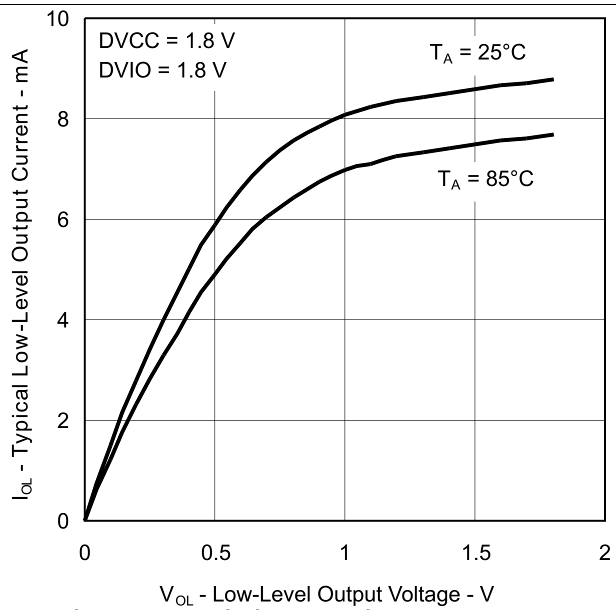


Figure 5-12. Typical Low-Level Output Current vs Low-Level Output Voltage

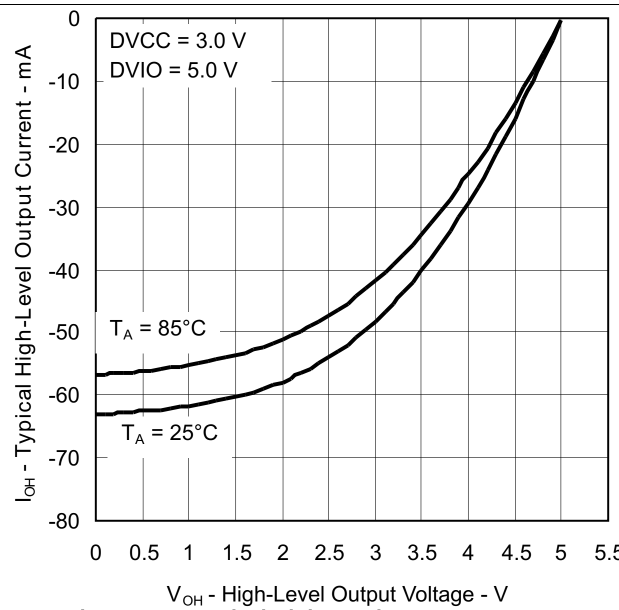


Figure 5-13. Typical High-Level Output Current vs High-Level Output Voltage

Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0), Ports P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1 *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

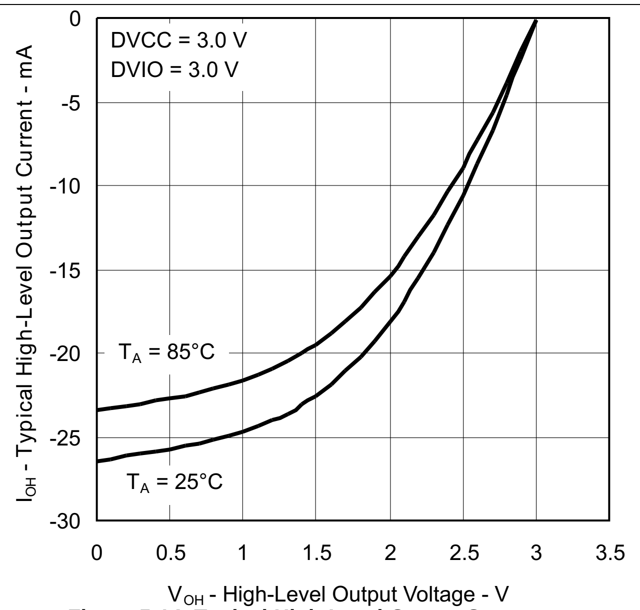


Figure 5-14. Typical High-Level Output Current vs High-Level Output Voltage

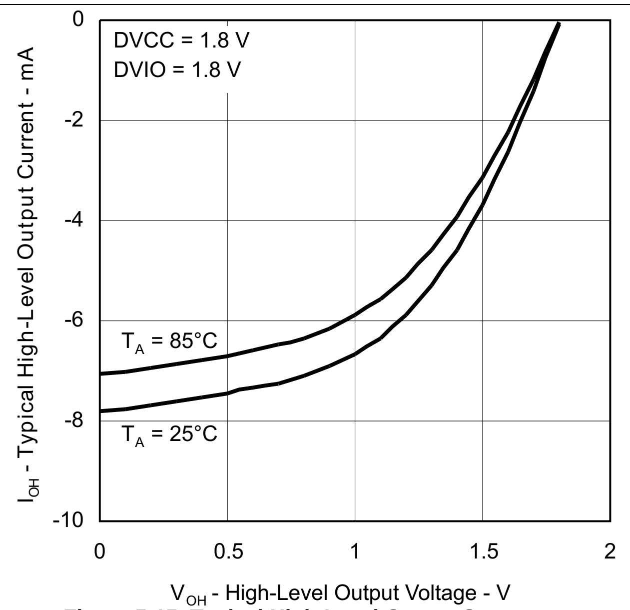


Figure 5-15. Typical High-Level Output Current vs High-Level Output Voltage

5.20 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1), Ports P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

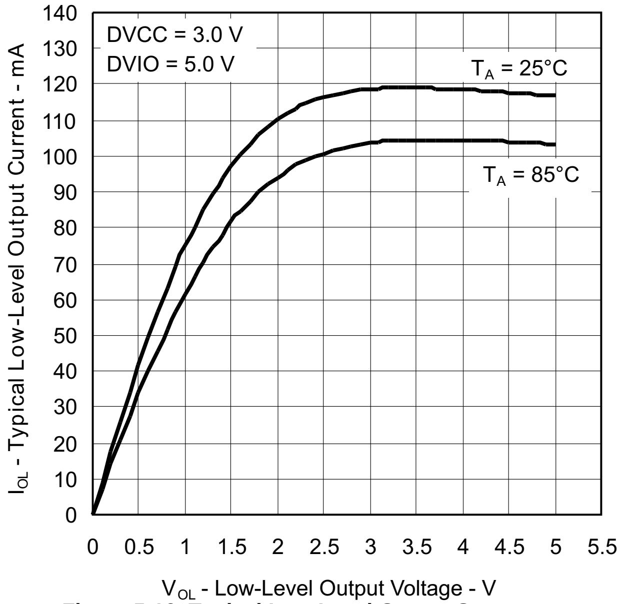


Figure 5-16. Typical Low-Level Output Current vs Low-Level Output Voltage

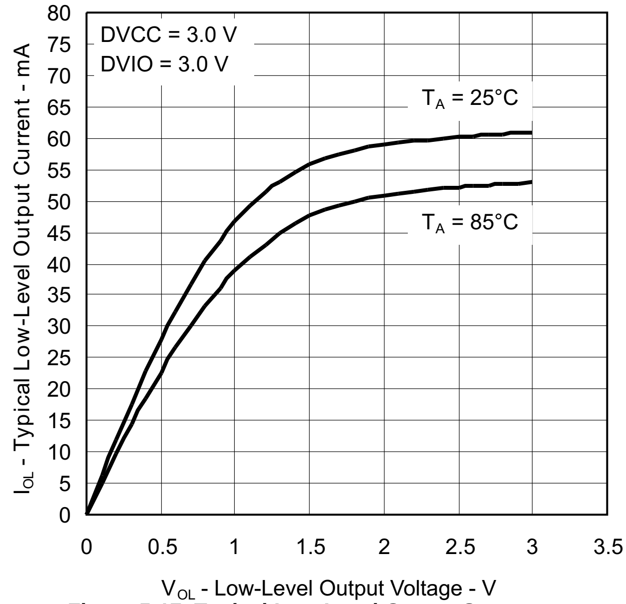


Figure 5-17. Typical Low-Level Output Current vs Low-Level Output Voltage

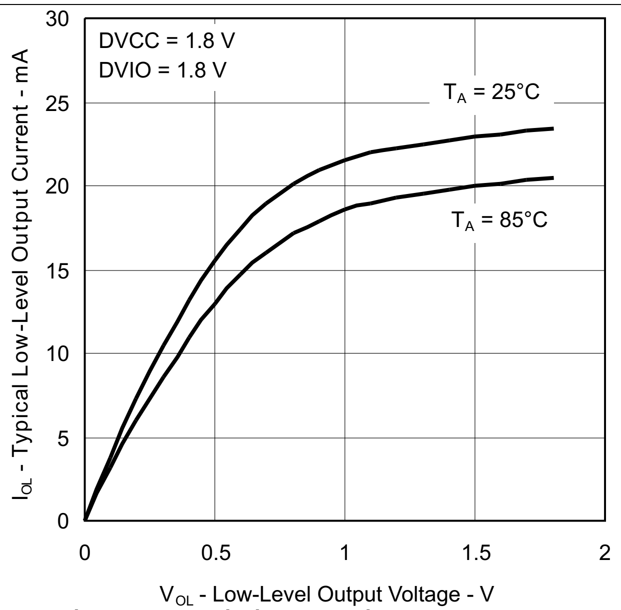


Figure 5-18. Typical Low-Level Output Current vs Low-Level Output Voltage

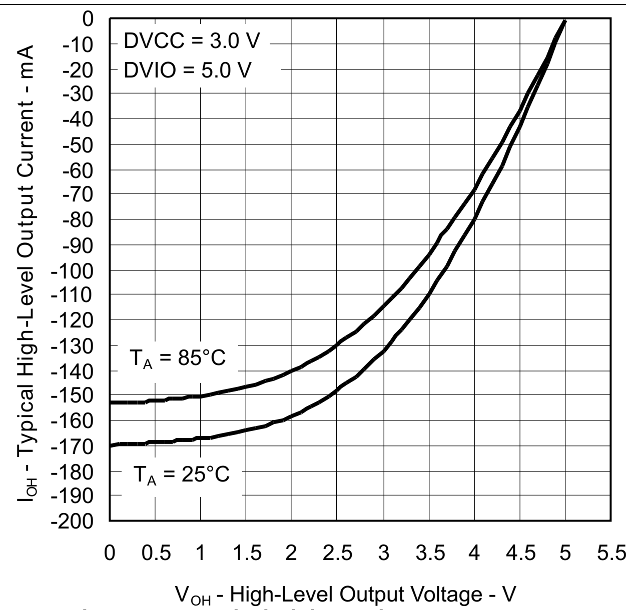


Figure 5-19. Typical High-Level Output Current vs High-Level Output Voltage

Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1), Ports P1.6 and P1.7, P2.0 to P2.7, P3.0 and P3.1 *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

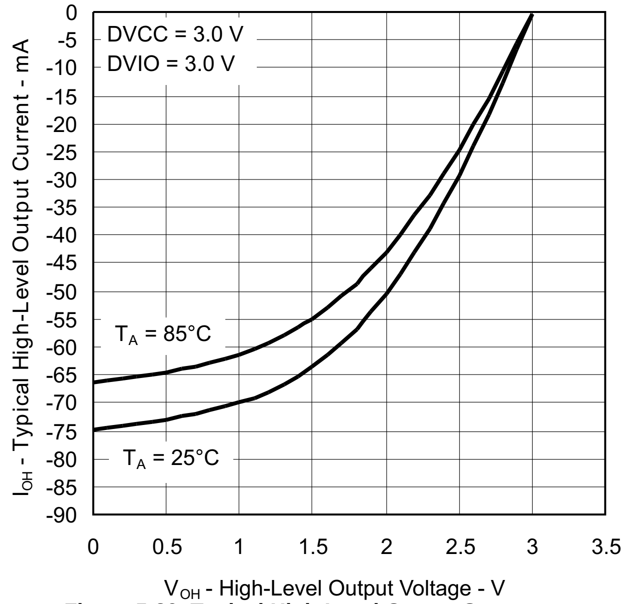


Figure 5-20. Typical High-Level Output Current vs High-Level Output Voltage

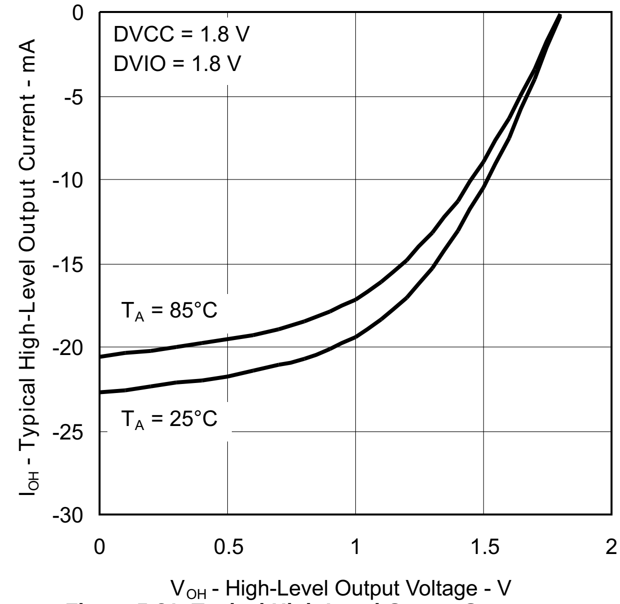


Figure 5-21. Typical High-Level Output Current vs High-Level Output Voltage

5.21 Crystal Oscillator, XT1, Low-Frequency Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC.LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C	3 V		0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			0.290		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, LF mode	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30%		70%	
$f_{Fault,LF}$	Oscillator fault frequency, LF mode	XTS = 0		10		10000	Hz
$t_{START,LF}$	Start-up time, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 12 pF	3 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 12 pF			500		

5.22 Crystal Oscillator, XT1, High-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC,HF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, HF mode	f_{OSC} = 4 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C	3 V		200		µA
		f_{OSC} = 12 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C			260		
		f_{OSC} = 20 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			325		
		f_{OSC} = 32 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			450		
$f_{XT1,HF0}$	XT1 oscillator crystal frequency, HF mode 0	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0(2)		4		8	MHz
$f_{XT1,HF1}$	XT1 oscillator crystal frequency, HF mode 1	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 1(2)		8		16	MHz
$f_{XT1,HF2}$	XT1 oscillator crystal frequency, HF mode 2	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2(2)		16		24	MHz
$f_{XT1,HF3}$	XT1 oscillator crystal frequency, HF mode 3	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 3(2)		24		32	MHz
$f_{XT1,HF,SW}$	XT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, XT1BYPASS = 1(3) (2)		0.7		32	MHz
OA_{HF}	Oscillation allowance for HF crystals(4)	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,HF}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,HF}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2, $f_{XT1,HF}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 3, $f_{XT1,HF}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Start-up time, HF mode	f_{OSC} = 6 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3 V		0.5		ms
		f_{OSC} = 20 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(5) (6)	XTS = 1			1		pF

(1) To improve EMI on the XT1 oscillator the following guidelines should be observed.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) Maximum frequency of operation of the entire device cannot be exceeded.
(3) When XT1BYPASS is set, the VLO, REFO, XT1 circuits are automatically powered down.
(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

Crystal Oscillator, XT1, High-Frequency Mode(1) *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
	Duty cycle, HF mode	XTS = 1, Measured at ACLK, $f_{XT1,HF2}$ = 20 MHz		40%	50%	60%	
$f_{Fault,HF}$	Oscillator fault frequency, HF mode(7)	XTS = 1(8)		30		300	kHz

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

5.23 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(85°C – (–40°C)). The coefficient is negative.
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V). The coefficient is positive.

5.24 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	1.8 V to 3.6 V		3		µA
f_{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5%	
		T_A = 25°C	3 V			±1.5%	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	
t_{START}	REFO start-up time	40%/60% duty cycle	1.8 V to 3.6 V		25		µs

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.25 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-22)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0)(1)	DCORSELx = 0, DCOx = 0, MODx = 0	0.07		0.20	MHz
$f_{DCO(0,31)}$	DCO frequency (0, 31)(1)	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
$f_{DCO(1,0)}$	DCO frequency (1, 0)(1)	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.38	MHz
$f_{DCO(1,31)}$	DCO frequency (1, 31)(1)	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
$f_{DCO(2,0)}$	DCO frequency (2, 0)(1)	DCORSELx = 2, DCOx = 0, MODx = 0	0.32		0.75	MHz
$f_{DCO(2,31)}$	DCO frequency (2, 31)(1)	DCORSELx = 2, DCOx = 31, MODx = 0	3.17		7.38	MHz
$f_{DCO(3,0)}$	DCO frequency (3, 0)(1)	DCORSELx = 3, DCOx = 0, MODx = 0	0.64		1.51	MHz
$f_{DCO(3,31)}$	DCO frequency (3, 31)(1)	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
$f_{DCO(4,0)}$	DCO frequency (4, 0)(1)	DCORSELx = 4, DCOx = 0, MODx = 0	1.3		3.2	MHz
$f_{DCO(4,31)}$	DCO frequency (4, 31)(1)	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
$f_{DCO(5,0)}$	DCO frequency (5, 0)(1)	DCORSELx = 5, DCOx = 0, MODx = 0	2.5		6.0	MHz
$f_{DCO(5,31)}$	DCO frequency (5, 31)(1)	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
$f_{DCO(6,0)}$	DCO frequency (6, 0)(1)	DCORSELx = 6, DCOx = 0, MODx = 0	4.6		10.7	MHz
$f_{DCO(6,31)}$	DCO frequency (6, 31)(1)	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
$f_{DCO(7,0)}$	DCO frequency (7, 0)(1)	DCORSELx = 7, DCOx = 0, MODx = 0	8.5		19.6	MHz
$f_{DCO(7,31)}$	DCO frequency (7, 31)(1)	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
$S_{DCORSEL}$	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.4	ratio
S_{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.02		1.12	ratio
	Duty cycle	Measured at SMCLK	40%	50%	60%	
df_{DCO}/dT	DCO frequency temperature drift	f_{DCO} = 1 MHz, V_{CORE} = 1.2 V, 2.0 V		0.1		%/°C
df_{DCO}/dV_{CORE}	DCO frequency voltage drift	f_{DCO} = 1 MHz		1.9		%/V

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO}, should be set to reside within the range of $f_{DCO(n, 0),MAX} \le f_{DCO} \le f_{DCO(n, 31),MIN}$, where $f_{DCO(n, 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

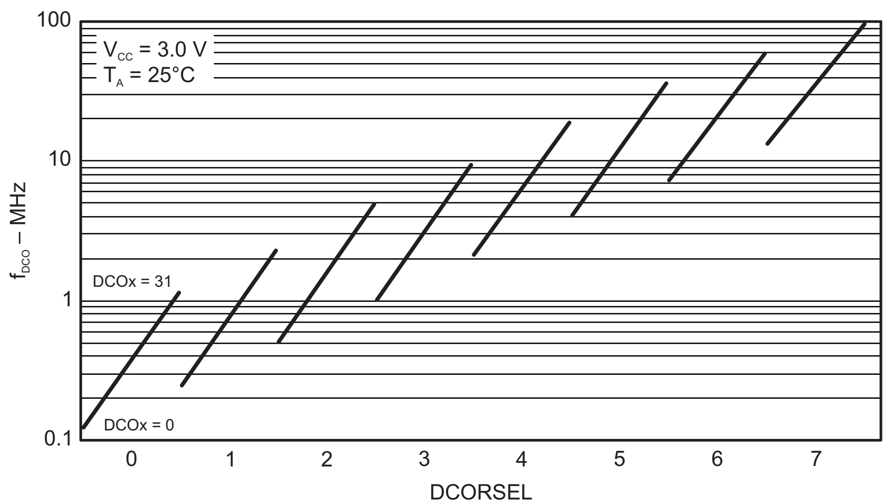


Figure 5-22. Typical DCO Frequency

5.26 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DVCC\_BOR\_IT-)}$	BOR_H on voltage, DV_{CC} falling level	dDV_{CC}/d_t < 3 V/s			1.45	V
$V_{(DVCC\_BOR\_IT+)}$	BOR_H off voltage, DV_{CC} rising level	dDV_{CC}/d_t < 3 V/s	0.80	1.30	1.50	V
$V_{(DVCC\_BOR\_hys)}$	BOR_H hysteresis		40		275	mV
$V_{(VCORE\_BOR\_IT-)}$	BOR_L on voltage, V_{CORE} falling level	DV_{CC} = 1.8 V to 3.6 V	0.69		0.87	V
$V_{(VCORE\_BOR\_IT+)}$	BOR_L off voltage, V_{CORE} rising level	DV_{CC} = 1.8 V to 3.6 V	0.83		1.05	V
$V_{(VCORE\_BOR\_hys)}$	BOR_L hysteresis		60		200	mV
td_{BOR}	BOR_L reset release time				2000	µs
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset		2			µs

5.27 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CORE3}(AM)	Core voltage, active mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 25 mA		1.90		V
V_{CORE2}(AM)	Core voltage, active mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 21 mA		1.80		V
V_{CORE1}(AM)	Core voltage, active mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 17 mA		1.60		V
V_{CORE0}(AM)	Core voltage, active mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 13 mA		1.40		V
V_{CORE3}(LPM)	Core voltage, active mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 30 µA		1.94		V
V_{CORE2}(LPM)	Core voltage, low-current mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA		1.84		V
V_{CORE1}(LPM)	Core voltage, low-current mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA		1.64		V
V_{CORE0}(LPM)	Core voltage, low-current mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA		1.44		V

5.28 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		2		µA
$V_{(SVSH\_IT-)}$	SVS_H on voltage level	SVSHE = 1, SVSHRVL = 0	1.59	1.64	1.69	V
		SVSHE = 1, SVSHRVL = 1	1.79	1.84	1.91	
		SVSHE = 1, SVSHRVL = 2	1.98	2.04	2.11	
		SVSHE = 1, SVSHRVL = 3	2.10	2.16	2.23	
$V_{(SVSH\_IT+)}$	SVS_H off voltage level	SVSHE = 1, SVSMHRRL = 0	1.62	1.74	1.81	V
		SVSHE = 1, SVSMHRRL = 1	1.88	1.94	2.01	
		SVSHE = 1, SVSMHRRL = 2	2.07	2.14	2.21	
		SVSHE = 1, SVSMHRRL = 3	2.20	2.26	2.33	
		SVSHE = 1, SVSMHRRL = 4	2.32	2.40	2.48	
		SVSHE = 1, SVSMHRRL = 5	2.56	2.70	2.84	
		SVSHE = 1, SVSMHRRL = 6	2.85	3.00	3.15	
		SVSHE = 1, SVSMHRRL = 7	2.85	3.00	3.15	
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		2.5		µs
		SVSHE = 1, dV_{DVCC}/dt = ±1 mV/µs, SVSHFP = 0		25		
$t_{(SVSH)}$	SVS_H on or off delay time	SVSHE = 0 → 1, SVSHFP = 1		12.5		µs
		SVSHE = 0 → 1, SVSHFP = 0		100		
dV_{DVCC}/dt	DV_{CC} rise time		0		1000	V/s

5.29 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM_H current consumption	SVMHE = 0, DV_{CC} = 3.6 V		0		nA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 0		200		nA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		2.0		µA
$V_{(SVMH)}$	SVM_H on or off voltage level	SVMHE = 1, SVSMHRRL = 0	1.65	1.74	1.86	V
		SVMHE = 1, SVSMHRRL = 1	1.85	1.94	2.02	
		SVMHE = 1, SVSMHRRL = 2	2.02	2.14	2.22	
		SVMHE = 1, SVSMHRRL = 3	2.18	2.26	2.35	
		SVMHE = 1, SVSMHRRL = 4	2.32	2.40	2.48	
		SVMHE = 1, SVSMHRRL = 5	2.56	2.70	2.84	
		SVMHE = 1, SVSMHRRL = 6	2.85	3.00	3.15	
		SVMHE = 1, SVSMHRRL = 7	2.85	3.00	3.15	
		SVMHE = 1, SVMHOVPE = 1		3.75		
$t_{pd(SVMH)}$	SVM_H propagation delay	SVMHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		2.5		µs
		SVMHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		20		µs
$t_{(SVMH)}$	SVM_H on or off delay time	SVMHE = 0 → 1, SVSHFP = 1		12.5		µs
		SVMHE = 0 → 1, SVSHFP = 0		100		µs

5.30 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS_L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		2.0		µA
$t_{(SVSL)}$	SVS_L on or off delay time	SVSLE = 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		6		µs
		SVSLE = 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		50		µs
$t_{pd(SVSL)}$	SVS_L propagation delay	SVMHE = 0 → 1, SVSLFP = 1		12.5		µs
		SVMHE = 0 → 1, SVSLFP = 0		100		µs

5.31 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM_L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 0		200		nA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 1		2.0		µA
$t_{pd(SVML)}$	SVM_L propagation delay	SVMLE = 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		2.5		µs
		SVMLE = 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		30		µs
$t_{(SVML)}$	SVM_L on or off delay time	SVMLE = 0 → 1, SVSLFP = 1		12.5		µs
		SVMLE = 0 → 1, SVSLFP = 0		100		µs

5.32 Wake-up Times From Low-Power Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{FAST-WAKE-UP}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode(1)	PMMCOREVx = SVSMLRRLx = n (where n = 0, 1, 2, or 3), SVSLFP = 1	$f_{MCLK} \geq 4$ MHz		3	6.5	µs
			1 MHz < f_{MCLK} < 4 MHz		4	8.0	
$t_{SLOW-WAKE-UP}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode(2)(3)	PMMCOREVx = SVSMLRRLx = n (where n = 0, 1, 2, or 3), SVSLFP = 0			150	165	µs
$t_{WAKE-UP\ LPM5}$	Wake-up time from LPM4.5 to active mode(4)				2	3	ms
$t_{WAKE-UP-RESET}$	Wake-up time from RST or BOR event to active mode(4)				2	3	ms

(1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{WAKE-UP-FAST}$ is possible with SVS_L and SVM_L in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide*.
(2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{WAKE-UP-SLOW}$ is set with SVS_L and SVM_L in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide*.
(3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.
(4) This value represents the time from the wake-up event to the reset vector execution.

5.33 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	1.8 V, 3 V		25	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture.	1.8 V, 3 V	20		ns

5.34 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
$f_{max,BITCLK}$	Maximum BITCLK clock frequency (equals baud rate in MBaud)(1)			1			MHz
t_τ	UART receive deglitch time		2.2 V	50	150	200	ns
			3 V	50	150	200	

(1) The DCO wake-up time must be considered in LPM3 and LPM4. The wake-up time must be considered in LPMx.5.

5.35 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see Figure 5-23 and Figure 5-24)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK or ACLK, Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time	PMMCOREV = 0	1.8 V	55		ns
			3 V	38		
		PMMCOREV = 3	2.4 V	30		
			3 V	25		
$t_{HD,MI}$	SOMI input data hold time	PMMCOREV = 0	1.8 V	0		ns
			3 V	0		
		PMMCOREV = 3	2.4 V	0		
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 0	1.8 V		20	ns
			3 V		18	
		UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 3	2.4 V		16	
			3 V		15	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	–10		ns
			3 V	–8		
		C_L = 20 pF, PMMCOREV = 3	2.4 V	–10		
			3 V	–8		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-23 and Figure 5-24.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-23 and Figure 5-24.

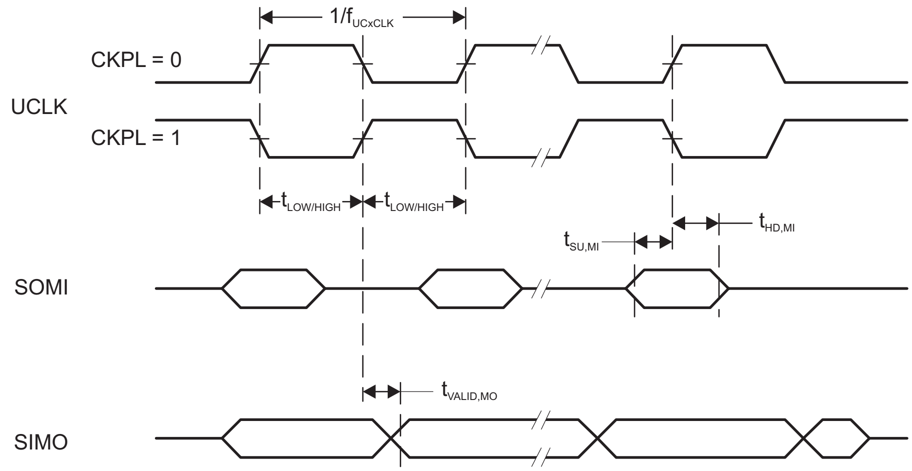


Figure 5-23. SPI Master Mode, CKPH = 0

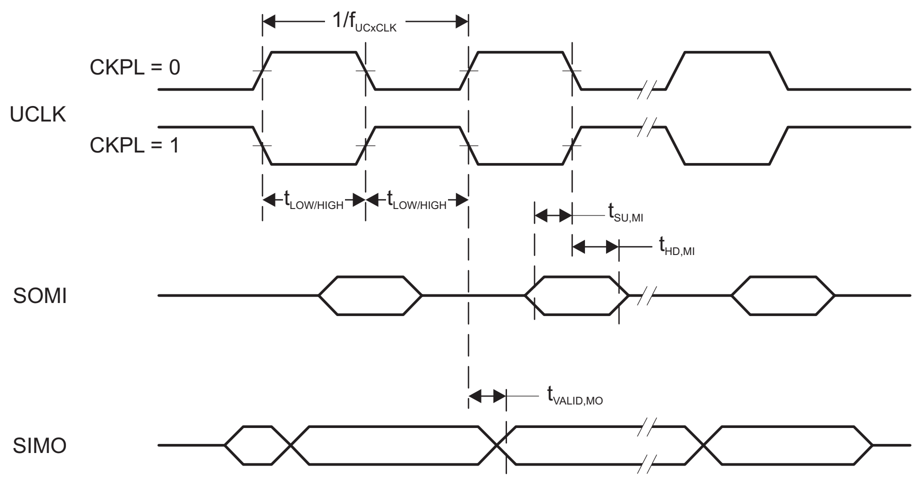


Figure 5-24. SPI Master Mode, CKPH = 1

5.36 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see Figure 5-25 and Figure 5-26)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock	PMMCOREV = 0	1.8 V	11		ns
			3 V	8		
		PMMCOREV = 3	2.4 V	7		
			3 V	6		
$t_{STE,LAG}$	STE lag time, Last clock to STE high	PMMCOREV = 0	1.8 V	3		ns
			3 V	3		
		PMMCOREV = 3	2.4 V	3		
			3 V	3		
$t_{STE,ACC}$	STE access time, STE low to SOMI data out	PMMCOREV = 0	1.8 V		66	ns
			3 V		50	
		PMMCOREV = 3	2.4 V		36	
			3 V		30	
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance	PMMCOREV = 0	1.8 V		30	ns
			3 V		23	
		PMMCOREV = 3	2.4 V		16	
			3 V		13	
$t_{SU,SI}$	SIMO input data setup time	PMMCOREV = 0	1.8 V	5		ns
			3 V	5		
		PMMCOREV = 3	2.4 V	2		
			3 V	2		
$t_{HD,SI}$	SIMO input data hold time	PMMCOREV = 0	1.8 V	5		ns
			3 V	5		
		PMMCOREV = 3	2.4 V	5		
			3 V	5		
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 0	1.8 V		76	ns
			3 V		60	
		UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 3	2.4 V		44	
			3 V		40	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	18		ns
			3 V	12		
		C_L = 20 pF, PMMCOREV = 3	2.4 V	10		
			3 V	8		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-25 and Figure 5-26.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-25 and Figure 5-26.

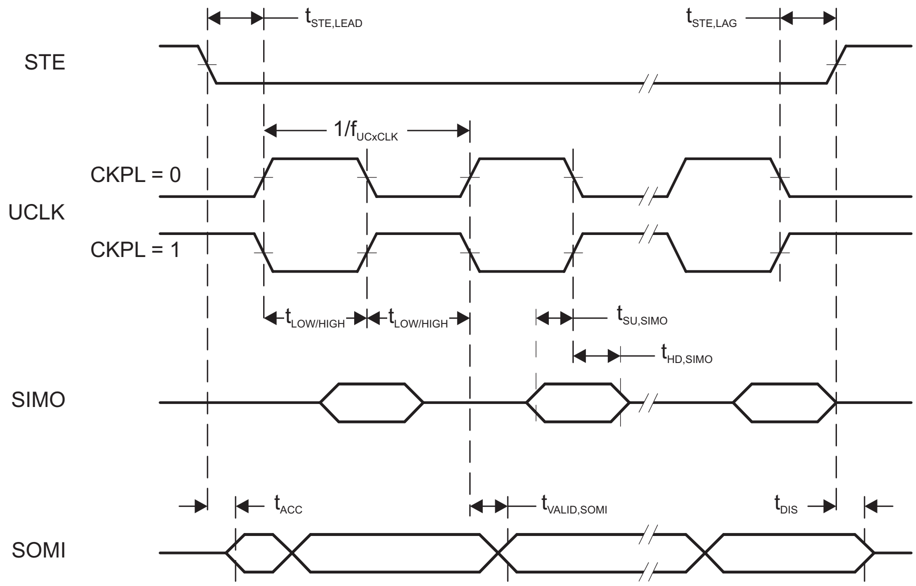


Figure 5-25. SPI Slave Mode, CKPH = 0

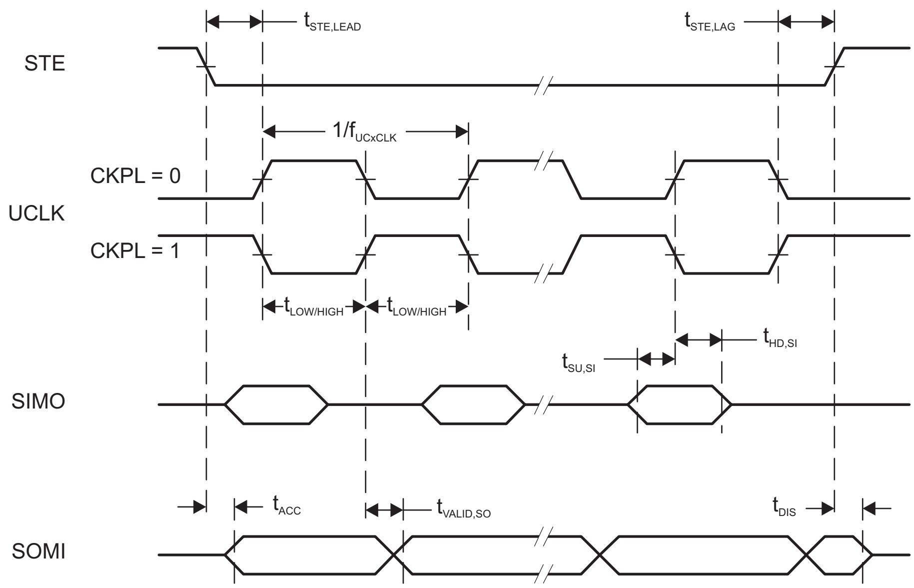


Figure 5-26. SPI Slave Mode, CKPH = 1

5.37 USCI (I^{2}C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-27)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0	400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0		µs
		f_{SCL} > 100 kHz		0.6		
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.7		µs
		f_{SCL} > 100 kHz		0.6		
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0		ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250		ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0		µs
		f_{SCL} > 100 kHz		0.6		
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	50	600	ns
			3 V	50	600	

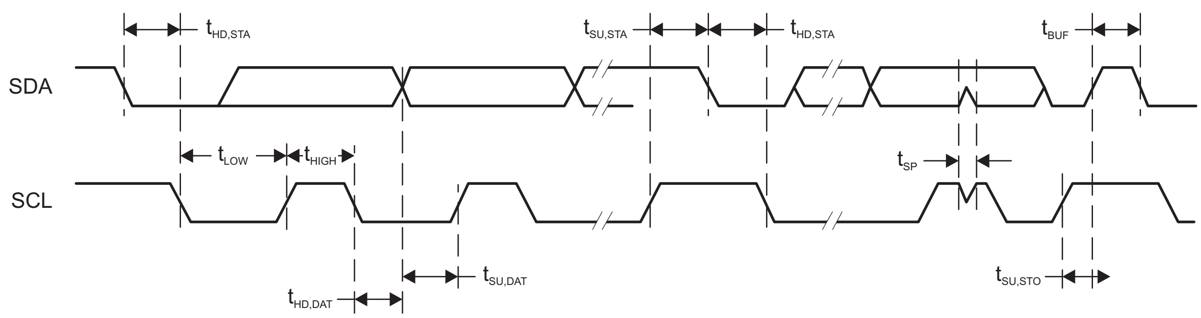


Figure 5-27. I^{2}C Mode Timing

5.38 10-Bit ADC, Power Supply and Input Range Conditions (MSP430F51x2 Devices Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		1.8		3.6	V
$V_{(Ax)}$	Analog input voltage range[2]	All ADC10_A pins: P1.0 to P1.5 and P3.6 and P3.7 terminals		0		AV_{CC}	V
I_{ADC10_A}	Operating supply current into AVCC terminal, REF module and reference buffer off	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00	2.2 V		60	90	µA
			3 V		75	100	
	Operating supply current into AVCC terminal, REF module on, reference buffer on	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01	3 V		113	130	
	Operating supply current into AVCC terminal, REF module off, reference buffer on	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VEREF = 2.5 V	3 V		105	125	
	Operating supply current into AVCC terminal, REF module off, reference buffer off	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VEREF = 2.5 V	3 V		70	95	
C_I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad	2.2 V		3.5		pF
R_I	Input MUX ON resistance	$AV_{CC} > 2.0$ V, $0\text{ V} \le V_{Ax} \le AV_{CC}$				36	kΩ
		$1.8\text{V} < AV_{CC} < 2.0$ V, $0\text{ V} \le V_{Ax} \le AV_{CC}$				96	

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. The external reference voltage requires decoupling capacitors.
Two decoupling capacitors, 10 µF and 100 nF, should be connected to VEREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x5xx and MSP430x6xx Family User's Guide*.

5.39 10-Bit ADC, Timing Parameters (MSP430F51x2 Devices Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$		For specified performance of ADC10_A linearity parameters	2.2 V, 3 V	0.45	5	5.5	MHz
$f_{ADC10OSC}$	Internal ADC10_A oscillator[1]	ADC10DIV = 0, $f_{ADC10CLK} = f_{ADC10OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, $f_{ADC10OSC}$ = 4 MHz to 5 MHz	2.2 V, 3 V	2.4		3.0	µs
		External $f_{ADC10CLK}$ from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0			12 × 1 / $f_{ADC10CLK}$		
$t_{ADC10ON}$	Turnon settling time of the ADC	See [2]				100	ns
t_{Sample}	Sampling time	R_S = 1000 Ω, R_I = 96 kΩ, C_I = 3.5 pF[3]	1.8 V	3			µs
		R_S = 1000 Ω, R_I = 36 kΩ, C_I = 3.5 pF[3]	3 V	1			

(1) The ADC10OSC is sourced directly from MODOSC inside the UCS.
(2) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(3) Approximately eight Tau (τ) are required for an error of less than ±0.5 LSB

5.40 10-Bit ADC, Linearity Parameters (MSP430F51x2 Devices Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ (VEREF+ – VEREF-) ≤ 1.6 V, C_{VEREF+} = 20 pF			±1.0	LSB
		1.6 V < (VEREF+ – VEREF-) ≤ V_{AVCC}, C_{VEREF+} = 20 pF			±1.0	
E_D	Differential linearity error	1.4 V ≤ (VEREF+ – VEREF-), C_{VEREF+} = 20 pF			±1.0	LSB
E_O	Offset error	1.4 V ≤ (VEREF+ – VEREF-), C_{VEREF+} = 20 pF, Internal impedance of source R_S < 100 Ω			±1.0	LSB
E_G	Gain error, external reference	1.4 V ≤ (VEREF+ – VEREF-), C_{VEREF+} = 20 pF			±1.0	LSB
	Gain error, external reference, buffered				±5	
	Gain error, internal reference	See (1)			±1.5%	VREF
E_T	Total unadjusted error, internal reference	See (1)			±1.5%	VREF

(1) Dominated by the absolute voltage of the integrated reference voltage.

5.41 REF, External Reference (MSP430F51x2 Devices Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
VEREF+	Positive external reference voltage input	VEREF+ > VEREF- (2)		1.4		AV_{CC}	V
VEREF-	Negative external reference voltage input	VEREF+ > VEREF- (3)		0		1.2	V
VEREF+ – VEREF-	Differential external reference voltage input	VEREF+ > VEREF- (4)		1.4		AV_{CC}	V
$I_{(VEREF+)}$, $I_{(VEREF-)}$	Static input current	1.4 V ≤ VEREF+ ≤ V(AVCC), VEREF- = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTx = 0x0001, Conversion rate 200 ksps	2.2 V, 3 V		±8.5	±26	µA
		1.4 V ≤ VEREF+ ≤ V(AVCC), VEREF- = 0 V, $f_{ADC10CLK}$ = 5 MHZ, ADC10SHTX = 0x1000, Conversion rate 20 ksps	2.2 V, 3 V			±1	
$C_{(VEREF+/-)}$	Capacitance at VEREF+ and VEREF- terminals	See (5)		10			µF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VEREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x5xx and MSP430x6xx Family User's Guide*.

5.42 REF, Built-In Reference (MSP430F51x2 Devices Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
VREF+	Positive built-in reference voltage	REFVSEL = {2} for 2.5 V, REFON = 1		3 V		2.51	±1.5%	V
		REFVSEL = {1} for 2.0 V, REFON = 1		3 V		1.99	±1.5%	
		REFVSEL = {0} for 1.5 V, REFON = 1		2.2 V, 3 V		1.5	±1.5%	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.5 V			1.8			V
		REFVSEL = {1} for 2.0 V			2.3			
		REFVSEL = {2} for 2.5 V			2.8			
I_{REF+}	Operating supply current into AVCC terminal(2)	$f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V		3 V		15.5	19	µA
		$f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2.0 V		3 V		18	24	
		$f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V		3 V		21	30	
TC_{REF+}	Temperature coefficient of built-in reference(3)	REFVSEL = {0, 1, 2}, REFON = 1				30	50	ppm/°C
I_{SENSOR}	Operating supply current into AVCC terminal(4)	REFON = 1, INCH = 0Ah, ADC10ON = 1, T_A = 30°C		2.2 V		150	180	µA
				3 V		150	190	
V_{SENSOR}	See (5)	REFON = 1, INCH = 0Ah, ADC10ON = 1, T_A = 30°C		2.2 V		765		mV
				3 V		765		
V_{MID}	AV_{CC} divider at channel 11	ADC10ON = 1, INCH = 0Bh, V_{MID} ≈ 0.5 × V_{AVCC}		2.2 V	1.06	1.1	1.14	V
				3 V	1.46	1.5	1.54	
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected(6)	ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB			30			µs
$t_{VMID(sample)}$	Sample time required if channel 11 is selected(7)	ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB			1			µs
PSRR_DC	Power supply rejection ratio (DC)	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), T_A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1				120	300	µV/V
PSRR_AC	Power supply rejection ratio (AC)	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), T_A = 25°C, f = 1 kHz, ΔVpp = 100 mV, REFVSEL = {0, 1, 2}, REFON = 1				6.4		mV/V
t_{SETTLE}	Settling time of reference voltage(8)	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), REFVSEL = {0, 1, 2}, REFON = 0 → 1	T_A = –40°C to 85°C			23	125	µs
			T_A = 25°C			23	50	
			T_A = 85°C			16	25	

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
(2) The internal reference current is supplied through the AVCC terminal. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
(3) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C)).
(4) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
(5) The temperature sensor offset can be as much as ±20°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(6) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(7) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.
(8) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB.

5.43 Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			1.8		3.6	V
I_{AVCC_COMP}	Comparator operating supply current into AVCC, Excludes reference resistor ladder	CBPWRMD = 00, CBON = 1, CBRSx = 00	1.8 V			38	µA
			2.2 V		31	38	
			3 V		32	39	
		CBPWRMD = 01, CBON = 1, CBRSx = 00	2.2 V, 3 V		10	17	
		CBPWRMD = 10, CBON = 1, CBRSx = 00	2.2 V, 3 V		0.2	0.85	
V_{REF}	Reference voltage level	CBREFLx = 01, CBREFACC = 0	≥1.8 V	1.42	1.44	1.46	V
		CBREFLx = 10, CBREFACC = 0	≥2.2 V	1.89	1.92	1.95	
		CBREFLx = 11, CBREFACC = 0	≥3.0 V	2.35	2.39	2.43	
I_{AVCC_REF}	Quiescent current of resistor ladder into AVCC, Including REF module current	CBREFACC = 1, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0	2.2 V, 3 V		10	17	µA
		CBREFACC = 0, CBREFLx = 01, CBRSx = 10, REFON = 0, CBON = 0	2.2 V, 3 V		33	40	
V_{IC}	Common mode input range			0		V_{CC} – 1	V
V_{OFFSET}	Input offset voltage	CBPWRMD = 00				±20	mV
		CBPWRMD = 01, 10				±10	
C_{IN}	Input capacitance				5		pF
R_{SIN}	Series input resistance	On (switch closed)			3	4	kΩ
		Off (switch opened)		50			MΩ
t_{PD}	Propagation delay, response time	CBPWRMD = 00, CBF = 0				450	ns
		CBPWRMD = 01, CBF = 0				600	
		CBPWRMD = 10, CBF = 0				50	µs
$t_{PD,filter}$	Propagation delay with filter active	CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 00		0.35	0.6	1.5	µs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01		0.6	1.0	1.8	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10		1.0	1.8	3.4	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11		1.8	3.4	6.5	
t_{EN_CMP}	Comparator enable time	CBON = 0 → 1, CBPWRMD = 00 or 01			1	2	µs
		CBON = 0 → 1, CBPWRMD = 10				100	
t_{EN_REF}	Resistor reference enable time	CBON = 0 to CBON = 1			1.0	1.5	µs
TC_{CB_REF}	Temperature coefficient reference of V_{CB_REF}					50	ppm/°C
V_{CB_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n + 0.5) / 32	VIN × (n + 1) / 32	VIN × (n + 1.5) / 32	V

5.44 Timer_D, Power Supply and Reference Clock

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
DV_{CC}	Digital supply voltage	$V_{(DVSS)}$ = 0 V		1.8		3.6	V
$f_{REF,DCO}$	Timer_D input reference clock frequency	PMMCOREVx = 0	1.8 V ≤ V_{CC} ≤ 3.6 V	8		12.0	MHz
		PMMCOREVx = 1	2.0 V ≤ V_{CC} ≤ 3.6 V	8		16.0	
		PMMCOREVx = 2	2.2 V ≤ V_{CC} ≤ 3.6 V	8		20.0	
		PMMCOREVx = 3	2.4 V ≤ V_{CC} ≤ 3.6 V	8		25.5	
$I_{(64MHz)}$	$I_{(DVCC)}$ at 64-MHz Timer_D clock, clock generator only	$f_{reference}$ = 8 MHz, MCx = 0, TDHREGEN = 1, TDHMx = 0, TDHCLKCR = 0			253	320	µA
$I_{(128MHz)}$	$I_{(DVCC)}$ at 128-MHz Timer_D clock, clock generator only	$f_{reference}$ = 16 MHz, MCx = 0, TDHREGEN = 1, TDHMx = 0, TDHCLKCR = 0			285	360	µA
$I_{(200MHz)}$	$I_{(DVCC)}$ at 200-MHz Timer_D clock, clock generator only	$f_{reference}$ = 25 MHz, MCx = 0, TDHREGEN = 1, TDHMx = 0, TDHCLKCR = 1			280	345	µA
$I_{(256MHz)}$	$I_{(DVCC)}$ at 256-MHz Timer_D clock, clock generator only	$f_{reference}$ = 16 MHz, MCx = 0, TDHREGEN = 1, TDHMx = 1, TDHCLKCR = 1			265	330	µA
$I_{(0,16,64)}$	$I_{(DVCC)}$	TDHCLKRx = 0, TDHCLKSRx = 16, TDHCLKTRIM = 64	2.2 V		244		µA
			3.0 V		295	325	
$I_{(1,16,64)}$	$I_{(DVCC)}$	TDHCLKRx = 1, TDHCLKSRx = 16, TDHCLKTRIM = 64	2.2 V		282		µA
			3.0 V		300	400	
$I_{(2,16,64)}$	$I_{(DVCC)}$	TDHCLKRx = 2, TDHCLKSRx = 16, TDHCLKTRIM = 64	2.2 V		358		µA
			3.0 V		414	470	

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.

5.45 Timer_D, Local Clock Generator Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{HRCG(0,0,64)}$	HRCG frequency (0, 0, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 0, TDHCLKTRIM = 64	39	56	73	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 0, TDHCLKTRIM = 64	78	112	146	
$f_{HRCG(0,7,64)}$	HRCG frequency (0, 7, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 7, TDHCLKTRIM = 64	46	66	86	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 7, TDHCLKTRIM = 64	92	132	172	
$f_{HRCG(0,15,64)}$	HRCG frequency (0, 15, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 15, TDHCLKTRIM = 64	55	78	101	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 15, TDHCLKTRIM = 64	110	156	202	
$f_{HRCG(0,23,64)}$	HRCG frequency (0, 23, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 23, TDHCLKTRIM = 64	61	87	113	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 23, TDHCLKTRIM = 64	122	174	226	
$f_{HRCG(0,31,0)}$	HRCG frequency (0, 31, 0)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 0	36	56	73	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 0	72	112	146	
$f_{HRCG(0,31,64)}$	HRCG frequency (0, 31, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 64	68	98	128	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 64	136	196	256	
$f_{HRCG(0,31,127)}$	HRCG frequency (0, 31, 127)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 127	97	138	180	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 0, TDHCLKSRx = 31, TDHCLKTRIM = 127	196	176	360	
$f_{HRCG(1,0,64)}$	HRCG frequency (1, 0, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 0, TDHCLKTRIM = 64	71	101	131	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 0, TDHCLKTRIM = 64	142	202	262	
$f_{HRCG(1,7,64)}$	HRCG frequency (1, 7, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 7, TDHCLKTRIM = 64	84	120	156	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 7, TDHCLKTRIM = 64	168	240	312	
$f_{HRCG(1,15,64)}$	HRCG frequency (1, 15, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 15, TDHCLKTRIM = 64	97	139	182	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 15, TDHCLKTRIM = 64	196	278	364	
$f_{HRCG(1,23,64)}$	HRCG frequency (1, 23, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 23, TDHCLKTRIM = 64	108	154	200	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 23, TDHCLKTRIM = 64	216	308	400	
$f_{HRCG(1,31,0)}$	HRCG frequency (1, 31, 0)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 0	68	97	126	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 0	136	194	252	
$f_{HRCG(1,31,64)}$	HRCG frequency (1, 31, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 64	123	175	227	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 64	246	350	454	

Timer_D, Local Clock Generator Frequency *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{HRCG(1,31,127)}$	HRCG frequency (1, 31, 127)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 127	169	241	313	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 0, TDHCLKRx = 1, TDHCLKSRx = 31, TDHCLKTRIM = 127	338	482	616	
$f_{HRCG(2,0,64)}$	HRCG frequency (2, 0, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 0, TDHCLKTRIM = 64	126	180	234	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 1, TDHCLKSRx = 0, TDHCLKTRIM = 64	252	360	468	
$f_{HRCG(2,7,64)}$	HRCG frequency (2, 7, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 7, TDHCLKTRIM = 64	138	208	270	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 7, TDHCLKTRIM = 6	276	416	540	
$f_{HRCG(2,15,64)}$	HRCG frequency (2, 15, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 15, TDHCLKTRIM = 64	168	240	312	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 15, TDHCLKTRIM = 64	336	480	624	
$f_{HRCG(2,23,64)}$	HRCG frequency (2, 23, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 23, TDHCLKTRIM = 64	189	270	351	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 23, TDHCLKTRIM = 64	378	540	702	
$f_{HRCG(2,31,0)}$	HRCG frequency (2, 31, 0)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 31, TDHCLKTRIM = 0	119	170	221	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 31, TDHCLKTRIM = 0	238	340	442	
$f_{HRCG(2,31,64)}$	HRCG frequency (2, 31, 64)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, DHCLKSRx = 31, TDHCLKTRIM = 64	212	303	394	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, DHCLKSRx = 31, TDHCLKTRIM = 64	424	606	788	
$f_{HRCG(2,31,127)}$	HRCG frequency (2, 31, 127)	TDHREGEN = 0, TDHMx = 0, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 31, TDHCLKTRIM = 127	290	413	537	MHz
		TDHREGEN = 0, TDHMx = 1, TDHCLKCR = 1, TDHCLKRx = 2, TDHCLKSRx = 31, TDHCLKTRIM = 127	580	826	1074	
$S_{HRCG,0,SR}$	TDHCLKSRx step size in range 0	$S_{HRCGSR} = f_{HRCGSR(HRCGSR+1)} - f_{HRCG(HRCGSR)}$	120	185	225	kHz
$S_{HRCG,1,SR}$	TDHCLKSRx step size in range 1	$S_{HRCGSR} = f_{HRCGSR(HRCGSR+1)} - f_{HRCG(HRCGSR)}$	220	325	395	kHz
$S_{HRCG,2,SR}$	TDHCLKSRx step size in range 2	$S_{HRCGSR} = f_{HRCGSR(HRCGSR+1)} - f_{HRCG(HRCGSR)}$	400	555	700	kHz
$S_{HRCG,0,TRIM}$	0 > = TDHCLKTRIMx < 16, step size in range 0	$S_{HRCGSR} = f_{HRCGSR(HRCGTRIM+1)} - f_{HRCG(HRCGTRIM)}$, TDHCLKSRx = X, Y, Z	55	85	120	kHz
	15 < TDHCLKTRIMx < 49, step size in range 1		40	85	130	
	48 < TDHCLKTRIMx < 64, step size in range 2		40	85	120	
$S_{HRCG,1,TRIM}$	0 > = TDHCLKTRIMx < 16, step size in range 0	$S_{HRCGSR} = f_{HRCGSR(HRCGTRIM+1)} - f_{HRCG(HRCGTRIM)}$, TDHCLKSRx = X, Y, Z	90	160	230	kHz
	15 < TDHCLKTRIMx < 49, step size in range 1		80	160	230	
	48 < TDHCLKTRIMx < 64, step size in range 2		80	160	230	

Timer_D, Local Clock Generator Frequency *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$S_{HRCG,2,TRIM}$	0 > = TDHCLKTRIMx < 16, step size in range 0	$S_{HRCGSR} = f_{HRCGSR(HRCGTRIM+1)} – f_{HRCG(HRCGTRIM)}$, TDHCLKSRx = X, Y, Z	150	230	360	kHz
	15 < TDHCLKTRIMx < 49, step size in range 1		130	230	350	
	48 < TDHCLKTRIMx < 32, step size in range 2		100	230	340	
df_{HRCG}/dT	HRCG frequency temperature drift	f_{HRCG} = 8 MHz, TDHREGEN = 0			±0.17	%/°C
		f_{HRCG} = 16 MHz, TDHREGEN = 0			±0.16	
		f_{HRCG} = 25 MHz, TDHREGEN = 0			±0.16	
		f_{HRCG} = 8, 16, or 25 MHz, TDHREGEN = 1		0		
df_{HRCG}/dV_{DVCC}	HRCG frequency voltage drift	f_{HRCG} = 8, 16, or 25 MHz, TDHREGEN = 0	0		5	%/V
		f_{HRCG} = 8, 16, or 25 MHz, TDHREGEN = 1		0		
t_{SETTLE}	Settling time	TDHEN = 0 → 1, TDHFW = 0	3	5	9	µs
	Settling time, fast wake-up	TDHEN = 0 → 1, TDHFW = 1			1.5	

5.46 Timer_D, Trimmed Clock Frequencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency tolerance during trimming		–0.5%		+0.5%	
$f_{TRIM(64MHz)}$	TDHMx = 0, TDHREGEN = 0, TDHCLKCR = 0, TDHxCTL1 = TDHxCTL1_64	T_A = 25°C, V_{CC} = 1.8 V	63	64	65	MHz
$f_{TRIM(128MHz)}$	TDHMx = 0, TDHREGEN = 0, TDHCLKCR = 1, TDHxCTL1 = TDHxCTL1_128	T_A = 25°C, V_{CC} = 2.0 V	126	128	130	MHz
$f_{TRIM(200MHz)}$	TDHMx = 0, TDHREGEN = 0, TDHCLKCR = 1, TDHxCTL1 = TDHxCTL1_200	T_A = 25°C, V_{CC} = 2.4 V	197	200	203	MHz
$f_{TRIM(256MHz)}$	TDHMx = 1, TDHREGEN = 0, TDHCLKCR = 1, TDHxCTL1 = TDHxCTL1_256	T_A = 25°C, V_{CC} = 2.2 V	250	256	262	MHz

5.47 Timer_D, Frequency Multiplication Mode

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	External frequency tolerance			0%		
$E_{(TDHREGEN = 1,64)}$	$f_{reference}$ = 8 MHz, TDHMx = 0, TDHREGEN = 1, TDHCLKCR = 0, TDHCLKRx = 0	T_A = 25°C, V_{CC} = 1.8 V	–1%		+1%	
$E_{(TDHREGEN = 1,128)}$	$f_{reference}$ = 16 MHz, TDHMx = 0, TDHREGEN = 1, TDHCLKCR = 1, TDHCLKRx = 0	T_A = 25°C, V_{CC} = 2.0 V	–1%		+1%	
$E_{(TDHREGEN = 1,200)}$	$f_{reference}$ = 25 MHz, TDHMx = 0, TDHREGEN = 1, TDHCLKCR = 1, TDHCLKRx = 0	T_A = 25°C, V_{CC} = 2.4 V	–1%		+1%	
$E_{(TDHREGEN = 1,256)}$	$f_{reference}$ = 16 MHz, TDHMx = 1, TDHREGEN = 1, TDHCLKCR = 1, TDHCLKRx = 0	T_A = 25°C, V_{CC} =2.2 V	–1%		+1%	

5.48 Timer_D, Input Capture and Output Compare Timing

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{TD,cap}$	Timer_D input capture timing, minimum pulse duration to trigger input capture event	f_{MAX} = 262 MHz		4		ns
$t_{TD0,cap,matching}$	Timer0_D input capture timing, matching between input capture channels P1.6 to P1.7 and P2.0	f_{MAX} = 262 MHz		1	2	LSB
	Timer0_D input capture timing, matching between input capture channels. P2.4 to P2.5 and P2.6	f_{MAX} = 262 MHz		3	4	
$t_{TD1,cap,matching}$	Timer1_D input capture timing, matching between input capture channels P2.1 to P2.2 and P2.3	f_{MAX} = 262 MHz		2	3	LSB
	Timer1_D input capture timing, matching between input capture channels. P2.7 to P3.0 and P3.1	f_{MAX} = 262 MHz		2	4	
$t_{TD01,cap,matching}$	Timer0_D and Timer1_D input capture timing, matching between input capture channels. Timer0_D is the high-resolution clock generator source.	f_{MAX} = 262 MHz		4	8	LSB
$t_{TD0,comp,matching}$	Timer0_D output compare timing, matching between output capture compare channels for pins P1.6, P1.7, and P2.0	Rising edges, f_{MAX} = 262 MHz			4	ns
		Falling edges, f_{MAX} = 262 MHz			4	
		Rising and falling edges, f_{MAX} = 262 MHz			8	
$t_{TD1,comp,matching}$	Timer1_D output compare timing, matching between output capture compare channels for pins P2.1, P2.2, and P2.3	Rising edges, f_{MAX} = 262 MHz			4	ns
		Falling edges, f_{MAX} = 262 MHz			4	
		Rising and falling edges, f_{MAX} = 262 MHz			8	
$t_{TD01,comp,matching}$	Timer0_D and Timer1_D output compare timing, matching between output compare channels. Timer0_D is the high-resolution clock generator source	All edges, f_{MAX} = 262 MHz			8	LSB

5.49 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_J	MIN	TYP	MAX	UNIT
$DV_{CC(PGM/ERASE)}$	Program and erase supply voltage		1.8		3.6	V
I_{PGM}	Supply current from DVCC during program			3	5	mA
I_{ERASE}	Supply current from DVCC during erase			2	6.5	mA
I_{MERASE}, I_{BANK}	Supply current from DVCC during mass erase or bank erase			2	6.5	mA
t_{CPT}	Cumulative program time (1)				16	ms
	Program and erase endurance		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	25°C	100			years
t_{Word}	Word or byte program time (2)		64		85	µs
$t_{Block, 0}$	Block program time for first byte or word (2)		49		65	µs
$t_{Block, 1–(N–1)}$	Block program time for each additional byte or word, except for last byte or word (2)		37		49	µs
$t_{Block, N}$	Block program time for last byte or word (2)		55		73	µs
$t_{Mass Erase}$	Mass erase time (2)		23		32	ms
$t_{Seg Erase}$	Segment erase time (2)		23		32	ms
$f_{MCLK,MGR}$	MCLK frequency in marginal read mode (FCLK4.MGR0 = 1 or FCTL4.MGR1 = 1)		0		1	MHz

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.
(2) These values are hardwired into the state machine of the flash controller.

5.50 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2.2 V, 3 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency, 4-wire JTAG (2)	2.2 V	0		5	MHz
		3 V	0		10	
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the minimum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see Figure 6-1).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

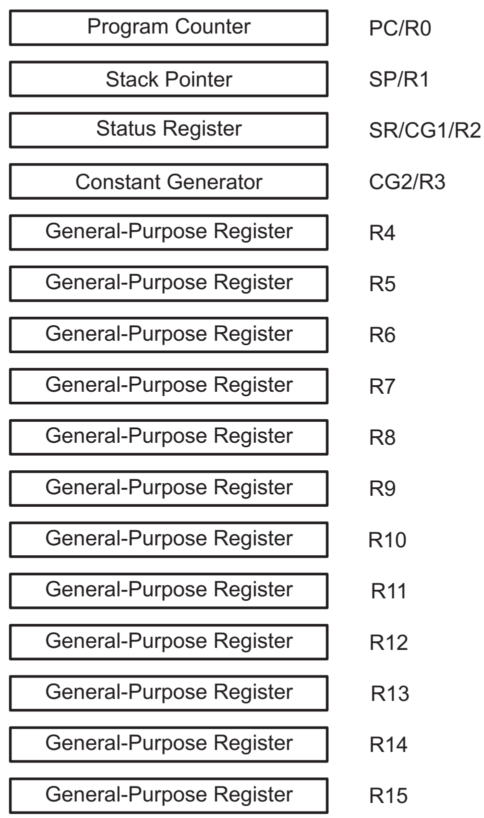


Figure 6-1. Integrated CPU Registers

6.2 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 6-1 lists examples of the three types of instruction formats; Table 6-2 lists the address modes.

Table 6-1. Instruction Word Formats

FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 6-2. Address Mode Descriptions

ADDRESS MODE	S(1)	D(1)	SYNTAX	EXAMPLE	OPERATION
Register	+	+	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	+	+	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	+	+	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	+	+	MOV & MEM, & TCDAT		M(MEM) → M(TCDAT)
Indirect	+		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	+		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	+		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source, D = destination

6.3 Operating Modes

The MSP430 has one active mode and six software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wake-up input from $\overline{\text{RST}}$/NMI, P1, and P2

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see Table 6-3). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-3. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up External reset Watchdog time-out, key violation Flash memory key violation	WDTIFG, KEYV (SYSRSTIV)[1] [2]	Reset	0FFFEh	63, highest
System NMI PMM Vacant memory access JTAG mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)[1]	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator fault Flash memory access violation	NMIIFG, OFIFG, ACCVIFG (SYSUNIV)[1] [2]	(Non)maskable	0FFFAh	61
Comp_B	CBIIFG, CBIFG (CBIV)[1] [3]	Maskable	0FFF8h	60
TEC0	TEC0FLTIFG, TEC0EXCLRIFG, TEC0AXCLRIFG[1] [3]	Maskable	0FFF6h	59
TD0	TD0CCR0 CCIFG0 [3]	Maskable	0FFF4h	58
TD0	TD0CCR1 CCIFG1, ... TD0CCR2 CCIFG2, TD0IFG, TD0HFLIFG, TD0HFHIFG, TD0HLKIFG, TD0HUNLKIFG (TD0IV)[1] [3]	Maskable	0FFF2h	57
Watchdog Timer_A interval timer mode	WDTIFG	Maskable	0FFF0h	56
USCI_A0 receive or transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV)[1] [3]	Maskable	0FFEEh	55
USCI_B0 receive or transmit	UCB0RXIFG, UCB0TXIFG, I^{2}C Status Interrupt Flags (UCB0IV)[1] [3]	Maskable	0FFECh	54
ADC10_A (MSP430F51x2 only)	ADC10IFG0, ADC10INIFG, ADC10LOIFG, ADC10HIIFG, ADC10TOVIFG, ADC10OVIFG (ADC10IV)[1] [3]	Maskable	0FFEAh	53
TA0	TA0CCR0 CCIFG0[3]	Maskable	0FFE8h	52
TA0	TA0CCR1 CCIFG1 ... TA0CCR2 CCIFG2, TA0IFG (TA0IV)[1] [3]	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)[1] [3]	Maskable	0FFE4h	50
TEC1	TEC1FLTIFG, TEC1EXCLRIFG, TEC1AXCLRIFG[1] [3]	Maskable	0FFE2	49
TD1	TD1CCR0 CCIFG0[3]	Maskable	0FFE0h	48
TD1	TD1CCR1 CCIFG1 ... TD1CCR2 CCIFG2, TD1IFG, TD1HFLIFG, TD1HFHIFG, TD1HLKIFG, TD1HUNLKIFG (TD1IV)[1] [3]	Maskable	0FFDEh	47
I/O port P1	P1IFG.0 to P1IFG.7 (P1IV)[1] [3]	Maskable	0FFDCh	46
I/O port P2	P2IFG.0 to P2IFG.7 (P2IV)[1] [3]	Maskable	0FFDAh	45
Reserved	Reserved[4]		0FFD8h	44
			⋮	⋮
			0FF80h	0, lowest

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.
(Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.
(3) Interrupt flags are in the module.
(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

6.5 Memory Organization

Table 6-4 summarizes the memory map of all devices.

Table 6-4. Memory Organization

		MSP430F5132, MSP430F5131	MSP430F5152, MSP430F5151	MSP430F5172, MSP430F5171
Memory Main: interrupt vector Main: code memory	Size Flash Flash	8KB 00FFFFh–00FF80h 00FFFFh–00E000h	16KB 00FFFFh–00FF80h 00FFFFh–00C000h	32KB 00FFFFh–00FF80h 00FFFFh–008000h
RAM	Size	1KB	2KB	2KB
	Sector 0	001FFFh–001C00h	0023FFh–001C00h	0023FFh–001C00h
Information memory (Flash)	Size	512 Byte	512 Byte	512 Byte
	Info A	128B 0019FFh–001980h	128B 0019FFh–001980h	128B 0019FFh–001980h
	Info B	128B 00197Fh–001900h	128B 00197Fh–001900h	128B 00197Fh–001900h
	Info C	128B 0018FFh–001880h	128B 0018FFh–001880h	128B 0018FFh–001880h
	Info D	128B 00187Fh–001800h	128B 00187Fh–001800h	128B 00187Fh–001800h
Bootloader (BSL) memory	Size	2K	2KB	2KB
	BSL 3	512B 0017FFh–001600h	512B 0017FFh–001600h	512B 0017FFh–001600h
	BSL 2	512B 0015FFh–001400h	512B 0015FFh–001400h	512B 0015FFh–001400h
	BSL 1	512B 0013FFh–001200h	512B 0013FFh–001200h	512B 0013FFh–001200h
	BSL 0	512B 0011FFh–001000h	512B 0011FFh–001000h	512B 0011FFh–001000h
Peripherals	Size Flash	4KB 000FFFh–000000h	4KB 000FFFh–000000h	4KB 000FFFh–000000h

6.6 Bootloader (BSL)

The BSL lets users program the flash memory or RAM using a UART serial interface. Access to the device memory by the BSL is protected by user-defined password. A bootloader security key is provided to disable the BSL completely or to disable the erasure of the flash if an invalid password is supplied. For complete description of the features of the BSL and its implementation, see *MSP430 Programming With the Bootloader (BSL)*. Table 6-5 lists the pins required for BSL access.

Table 6-5. BSL Functions

BSL FUNCTION	DESCRIPTION		
	40-PIN QFN RSB PACKAGE	38-PIN TSSOP DA PACKAGE	40-PIN DSBGA YFF PACKAGE
$\overline{RST}$/NMI/SBWTDIO	Entry sequence signal	Entry sequence signal	Entry sequence signal
TEST/SBWTCK	Entry sequence signal	Entry sequence signal	Entry sequence signal
Data transmit	P3.7 - 36	P3.5 - 37	P3.7 - B4
Data receive	P3.6 - 35	P3.6 - 38	P3.6 - A4
VCC	Power supply	Power supply	Power supply
VSS	Ground supply	Ground supply	Ground supply

6.7 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

6.8 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data is lost. Features of the RAM include:

- RAM has n sectors. The size of a sector can be found in Section 6.5.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. The peripherals can be manged using all instructions. For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide*.

6.9.1 Digital I/O

Up to three 8-bit I/O ports are implemented. Port PJ contains seven individual I/O pins, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- All 8 bits of ports P1 and P2 support edge-selectable interrupt input.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise. P1 and P2 can also be accessed word-wise (PA).
- The input and output voltage levels of the pins supplied by DV_{IO} (see Table 4-1) are defined by the voltage supplied by DV_{IO} (up to 5 V).

6.9.2 Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to Port P1, Port P2, and Port P3 (see Table 6-6).

Table 6-6. Port Mapping Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_UCA0CLK	USCI_A0 clock input/output (direction controlled by USCI)	
	PM_UCB0STE	USCI_B0 SPI slave transmit enable (direction controlled by USCI)	
2	PM_UCA0TXD	USCI_A0 UART TXD (Direction controlled by USCI – output)	
	PM_UCA0SIMO	USCI_A0 SPI slave in master out (direction controlled by USCI)	
3	PM_UCB0SOMI	USCI_B0 SPI slave out master in (direction controlled by USCI)	
	PM_UCB0SCL	USCI_B0 I^2C clock (open drain and direction controlled by USCI)	
4	PM_UCA0RXD	USCI_A0 UART RXD (Direction controlled by USCI – input)	
	PM_UCA0SOMI	USCI_A0 SPI slave out master in (direction controlled by USCI)	
5	PM_UCB0SIMO	USCI_B0 SPI slave in master out (direction controlled by USCI)	
	PM_UCB0SDA	USCI_B0 I^2C data (open drain and direction controlled by USCI)	
6	PM_UCB0CLK	USCI_B0 clock input/output (direction controlled by USCI)	
	PM_UCA0STE	USCI_A0 SPI slave transmit enable (direction controlled by USCI)	
7	PM_TD0.0	TD0 input capture channel 0	TD0 output compare channel 0
8	PM_TD0.1	TD0 input capture channel 1	TD0 output compare channel 1
9	PM_TD0.2	TD0 input capture channel 2	TD0 output compare channel 2
10	PM_TD1.0	TD1 input capture channel 0	TD1 output compare channel 0
11	PM_TD1.1	TD1 input capture channel 1	TD1 output compare channel 1
12	PM_TD1.2	TD1 input capture channel 2	TD1 output compare channel 2
13	PM_CLR1TD0.0	TD0 external clear input	TD0 output compare channel 0
	PM_FLT1_2TD0.0	TD0 fault input channel 2	
14	PM_FLT1_0TD0.1	TD0 fault input channel 0	TD0 output compare channel 1
15	PM_FLT1_1TD0.2	TD0 fault input channel 1	TD0 output compare channel 2
16	PM_CLR2TD1.0	TD1 external clear input (controlled by module input enable)	TD1 output compare channel 0
	PM_FLT2_1TD1.0	TD1 fault input channel 1 (controlled by module input enable)	
17	PM_FLT2_2TD1.1	TD1 fault input channel 2	TD1 output compare channel 1
18	PM_FLT2_0TD1.2	TD1 fault input channel 0	TD1 output compare channel 2
19	PM_TD0.0SMCLK	TD0 input capture channel 0	SMCLK output
20	PM_TA0CLKCBOUT	TA0 input clock	Comparator_B output
21	PM_TD0CLKMCLK	TD0 input clock	MCLK output
22	PM_TA0_0	TA0 input capture channel 0	TA0 output compare channel 0
23	PM_TA0_1	TA0 input capture channel 1	TA0 output compare channel 1
24	PM_TA0_2	TA0 input capture channel 2	TA0 output compare channel 2
25	PM_DMAE0SMCLK	DMAE0 input	SMCLK output
26	PM_DMAE1MCLK	DMAE1 input	MCLK output
27	PM_DMAE2SVM	DMAE2 input	SVM output
28	PM_TD0OUTH	TD0 3-state input	ADC10CLK
29	PM_TD1OUTH	TD1 3-state input	ACLK
30	Reserved	None	DVSS
31 (0FFh)(1)	PM_ANALOG	Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide, and the upper bits are ignored, which results in a read out value of 31.

Table 6-7 lists the default assignments for all pins that support port mapping.

Table 6-7. Default Mapping

PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P1.0/PM_UCA0CLK/ PM_UCB0STE/A0/CB0	PM_UCA0CLK PM_UCB0STE	USCI_A0 clock input/output (direction controlled by USCI)	USCI_B0 SPI slave transmit enable (direction controlled by USCI)
P1.1/PM_UCA0TXD/ PM_UCA0SIMO/A1/CB1	PM_UCA0TXD PM_UCA0SIMO	USCI_A0 UART TXD (Direction controlled by USCI – output)	USCI_A0 SPI slave in master out (direction controlled by USCI)
P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A2/CB2	PM_UCA0RXD PM_UCA0SOMI	USCI_A0 UART RXD (Direction controlled by USCI – input)	USCI_A0 SPI slave out master in (direction controlled by USCI)
P1.3/PM_UCB0CLK/ PM_UCA0STE/A3/CB3	PM_UCB0CLK PM_UCA0STE	USCI_B0 clock input/output (direction controlled by USCI)	USCI_A0 SPI slave transmit enable (direction controlled by USCI)
P1.4/PM_UCB0SIMO/ PM_UCB0SDA/A4/CB4	PM_UCB0SIMO PM_UCB0SDA	USCI_B0 SPI slave in master out (direction controlled by USCI)	USCI_B0 I^2C data (open drain and direction controlled by USCI)
P1.5/PM_UCB0SOMI/ PM_UCB0SCL/A5/CB5	PM_UCB0SOMI PM_UCB0SCL	USCI_B0 SPI slave out master in (direction controlled by USCI)	USCI_B0 I^2C clock (open drain and direction controlled by USCI)
P1.6/PM_TD0.0	PM_TD0.0	TD0 input capture channel 0	TD0 output compare channel 0
P1.7/PM_TD0.1	PM_TD0.1	TD0 input capture channel 1	TD0 output compare channel 1
P2.0/PM_TD0.2	PM_TD0.2	TD0 input capture channel 2	TD0 output compare channel 2
P2.1/PM_TD1.0	PM_TD1.0	TD1 input capture channel 0	TD1 output compare channel 0
P2.2/PM_TD1.1	PM_TD1.1	TD1 input capture channel 1	TD1 output compare channel 1
P2.3/PM_TD1.2	PM_TD1.2	TD1 input capture channel 2	TD1 output compare channel 2
P2.4/PM_TEC0CLR/ PM_TEC0FLT2/PM_TD0.0	PM_CLR1TD0.0 PM_FLT1_2TD0.0	TD0 external clear input (controlled by module input enable) TD0 fault input channel 2 (controlled by module input enable)	TD0 output compare channel 0
P2.5/PM_TEC0FLT0/PM_TD0.1	PM_FLT1_0TD0.1	TD0 fault input channel 0	TD0 output compare channel 1
P2.6/PM_TEC0FLT1/PM_TD0.2	PM_FLT1_1TD0.2	TD0 fault input channel 1	TD0 output compare channel 2
P2.7/PM_TEC1CLR/ PM_TEC1FLT1/PM_TD1.0	PM_CLR2TD1.0 PM_FLT2_1TD1.0	TD1 external clear input (controlled by module input enable) TD1 fault input channel 1 (controlled by module input enable)	TD1 output compare channel 0
P3.0/PM_TEC1FLT2/ PM_TD1.1	PM_FLT2_2TD1.1	TD1 fault input channel 2	TD1 output compare channel 1
P3.1/PM_TEC1FLT0/ PM_TD1.2	PM_FLT2_0TD1.2	TD1 fault input channel 0	TD1 output compare channel 2
P3.2/PM_TD0.0/ PM_SMCLK/CB14	PM_TD0.0SMCLK	TD0 input capture channel 0	SMCLK output
P3.3/PM_TA0CLK/ PM_CBOUT/CB13	PM_TA0CLKCBOUT	TA0 input clock	Comparator_B output
P3.4/PM_TD0CLK/ PM_MCLK	PM_TD0CLKMCLK	TD0 input clock	MCLK output
P3.5/PM_TA0.2/ VEREF+/CB12	PM_TA3_2	TA0 input capture channel 0	TA0 output compare channel 0
P3.6/PM_TA0.1/A7 VEREF-/CB11	PM_TA3_1	TA0 input capture channel 1	TA0 output compare channel 1
P3.7/PM_TA0.0/ A6/CB10	PM_TA3_0	TA0 input capture channel 2	TA0 output compare channel 2

6.9.3 Oscillator and System Clock

The clock system (Unified Clock System [UCS]) module includes support for a 32-kHz watch crystal oscillator and high-frequency crystal oscillator, an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), and an integrated internal digitally controlled oscillator (DCO). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turnon clock source and stabilizes in less than 5 µs. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal or high-frequency crystal (XT1), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

6.9.4 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, and brownout protection. The brownout circuit provides the proper internal reset signal to the device during power on and power off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

6.9.5 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

6.9.6 Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.9.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors) (see Table 6-8). It also includes a data exchange mechanism using JTAG that is called a JTAG mailbox and that can be used in the application.

Table 6-8. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	INTERRUPT EVENT	WORD ADDRESS	OFFSET	PRIORITY
SYSRSTIV, System Reset	No interrupt pending	019Eh	00h	
	Brownout (BOR)		02h	Highest
	RST/NMI (POR)		04h	
	PMMSWBOR (BOR)		06h	
	LPM5 wake-up (BOR)		08h	
	Security violation (BOR)		0Ah	
	SVSL (POR)		0Ch	
	SVSH (POR)		0Eh	
	SVML_OVP (POR)		10h	
	SVMH_OVP (POR)		12h	
	PMMSWPOR (POR)		14h	
	WDT time-out (PUC)		16h	
	WDT key violation (PUC)		18h	
	KEYV flash key violation (PUC)		1Ah	
	Reserved		1Ch	
	Peripheral area fetch (PUC)		1Eh	
	PMM key violation (PUC)		20h	
	Reserved		22h to 3Eh	Lowest
SYSSNIV, System NMI	No interrupt pending	019Ch	00h	
	SVMLIFG		02h	Highest
	SVMHIFG		04h	
	DLYLIFG		06h	
	DLYHIFG		08h	
	VMAIFG		0Ah	
	JMBINIFG		0Ch	
	JMBOUTIFG		0Eh	
	VLRLIFG		10h	
	VLRHIFG		12h	
	Reserved		14h to 1Eh	Lowest
SYSUNIV, User NMI	No interrupt pending	019Ah	00h	
	NMIIFG		02h	Highest
	OFIFG		04h	
	ACCVIFG		06h	
	Reserved		08h to 1Eh	Lowest

6.9.8 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to wake to move data to or from a peripheral. Table 6-9 lists the triggers that can be assigned to start a DMA transfer.

Table 6-9. DMA Trigger Assignments(1)

TRIGGER	CHANNEL		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TD0CCR0 CCIFG	TD0CCR0 CCIFG	TD0CCR0 CCIFG
4	TD0CCR2 CCIFG	TD0CCR2 CCIFG	TD0CCR2 CCIFG
5	TD1CCR0 CCIFG	TD1CCR0 CCIFG	TD1CCR0 CCIFG
6	TD1CCR2 CCIFG	TD1CCR2 CCIFG	TD1CCR2 CCIFG
7	Reserved	Reserved	Reserved
8	Reserved	Reserved	Reserved
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	Reserved	Reserved	Reserved
21	Reserved	Reserved	Reserved
22	Reserved	Reserved	Reserved
23	Reserved	Reserved	Reserved
24	ADC10IFG0	ADC10IFG0	ADC10IFG0
25	Reserved	Reserved	Reserved
26	Reserved	Reserved	Reserved
27	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.

6.9.9 Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two modules, A and B.

The USCI_Ax module provides support for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The USCI_Bx module provides support for SPI (3- or 4-pin) or I^2C.

6.9.10 TA0

TA0 is a 16-bit timer/counter with three capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-10). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-10. TA0 Signal Connections

INPUT PIN NUMBER			DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER		
RSB (40-PIN QFN)	DA (38-PIN TSSOP)	YFF (40-PIN DSBGA)						RSB (40-PIN QFN)	DA (38-PIN TSSOP)	YFF (40-PIN DSBGA)
P3.3 - 30	P3.3 - 34	P3.3 - G6	TA0CLK	TACLK	Timer	NA	NA	–	–	–
ACLK (internal)	ACLK	ACLK	ACLK	ACLK				–	–	–
SMCLK (internal)	SMCLK	SMCLK	SMCLK	SMCLK				–	–	–
P3.3 - 30	P3.3 - 34	P3.3 - G6	TA0CLK	$\overline{\text{TACLK}}$				–	–	–
P3.7 - 36	–	P3.7 - G4	TA0.0	CCI0A	CCR0	TA0	TA0.0	P3.7 - 36	–	P3.7 - G4
–	–	–	CBOUT	CCI0B				–	–	–
–	–	–	V_{SS}	GND				–	–	–
–	–	–	V_{CC}	V_{CC}				–	–	–
P3.6 - 35	–	P3.6 - G3	TA0.1	CCI1A	CCR1	TA1	TA0.1	P3.6 - 35	P3.6 - 38	P3.6 - G3
–	–	–	ACLK	CCI1B				ADC10_A[1] (internal) ADC10SHS x = 001b	ADC10_A[1] (internal) ADC10SHS x = 001b	ADC10_A[1] (internal) ADC10SHS x = 001b
–	–	–	V_{SS}	GND				–	–	–
–	–	–	V_{CC}	V_{CC}				–	–	–
P3.5 - 34	P3.5 - 37	P3.5 - F3	TA0.2	CCI2A	CCR2	TA2	TA0.2	P3.5 - 34	P3.5 - 37	P3.5 - F3
–	–	–	V_{SS}	CCI2B				–	–	–
–	–	–	V_{SS}	GND				–	–	–
–	–	–	V_{CC}	V_{CC}				–	–	–

(1) The ADC10_A trigger is available on MSP430F51x2 devices.

6.9.11 TD0

TD0 is a 16-bit timer/counter with three capture/compare registers supporting up to 256-MHz (4-ns) resolution. TD0 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-11). TD0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. External fault inputs as well as a external timer counter clear is supported along with interrupt flags from the TEC0 module.

Table 6-11. TD0 Signal Connections

INPUT PIN NUMBER			DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER		
RSB (40-PIN QFN)	DA (38-PIN TSSOP)	YFF (40-PIN DSBGA)						RSB (40-PIN QFN)	DA (38-PIN TSSOP)	YFF (40-PIN DSBGA)
P3.4 - 31	–	P3.4 - G5	TD0CLK	TDCLK	Timer	NA	NA	–	–	–
ACLK (internal)	ACLK (internal)	ACLK (internal)	ACLK	ACLK				–	–	–
SMCLK (internal)	SMCLK (internal)	SMCLK (internal)	SMCLK	SMCLK				–	–	–
P3.4 - 31	–	P3.4 - G5	TD0CLK	$\overline{\text{TDCLK}}$				–	–	–
–	–	–	–	CLK0				–	–	–
P2.4 - 19	P2.4 - 23	P2.4 - B4	TEC0CLR	TECXCLR				–	–	–
P1.6 - 11 (1)	P1.6 - 15 (1)	P1.6 - A1 (1)	TD0.0	CCI0A	CCR0	TD0	TD0	P1.6 - 11 (1)	P1.6 - 15 (1)	P1.6 - A1 (1)
P3.2 - 29	P3.2 - 33	P3.2 - F5	TD0.0	CCI0B				P2.4 - 19	P2.4 - 23	P2.4 - B4
–	–	–	V_{SS}	GND				ADC10_A (internal) ADC10SHS x = 010b (2)	ADC10_A (internal) ADC10SHS x = 010b (2)	ADC10_A (internal) ADC10SHS x = 010b (2)
–	–	–	V_{CC}	V_{CC}				–	–	–
P2.5 - 20	P2.5 - 24	P2.5 - A6	TEC0FLT0	TECXFLT0				–	–	
P1.7 - 12 (1)	P1.7 - 16 (1)	P1.7 - B2 (1)	TD0.1	CCI1A	CCR1	TD1	TD1	P1.7 - 12 (1)	P1.7 - 16 (1)	P1.7 - B2 (1)
CBOUT (internal)	CBOUT (internal)	CBOUT (internal)	TD0.1	CCI1B				PJ.6 - 28	PJ.6 - 32	PJ.6 - E5
–	–	–	V_{SS}	GND				P2.5 - 20	P2.5 - 24	P2.5 - A6
–	–	–	V_{CC}	V_{CC}				ADC10_A (internal) ADC10SHS x = 011b (2)	ADC10_A (internal) ADC10SHS x = 011b (2)	ADC10_A (internal) ADC10SHS x = 011b (2)
P2.6 - 21	P2.6 - 20	P2.6 - B5	TEC0FLT1	TECXFLT1				–	–	
P2.0 - 13 (1)	P2.0 - 17 (1)	P2.0 - B3 (1)	TD0.2	CCI2A	CCR2	TD2	TD2	P2.0 - 13 (1)	P2.0 - 17 (1)	P2.0 - B3 (1)
ACLK (internal)	ACLK (internal)	ACLK (internal)	TD0.2	CCI2B				P2.6 - 21	P2.6 - 25	P2.6 - B5
–	–	–	V_{SS}	GND				–	–	–
–	–	–	V_{CC}	V_{CC}				–	–	–
P2.4 - 19	P2.4 - 23	P2.4 - B4	TEC0FLT2	TECXFLT2				–	–	–

(1) Pins P1.6 for TD0.0, P1.7 for TD0.1, and P2.0 for TD0.2 are optimized for matching.
(2) The ADC10_A trigger is available on MSP430F51x2 devices.

6.9.12 TD1

TD1 is a 16-bit timer/counter with three capture/compare registers supporting up to 256-MHz (4-ns) resolution. TD1 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-12). TD1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. External fault inputs as well as a external timer counter clear is supported along with interrupt flags from the TEC0 module.

Table 6-12. TD1 Signal Connections

INPUT PIN NUMBER			DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER		
RSB (40-PIN QFN)	DA (38-PIN TSSOP)	YFF (40-PIN DSBGA)						RSB (40-PIN QFN)	DA (38-PIN TSSOP)	YFF (40-PIN DSBGA)
PJ.6 - 28	PJ.6 - 32	PJ.6 - E5	TD1CLK	TDCLK	Timer	NA	NA	–	–	–
ACLK (internal)	ACLK (internal)	ACLK (internal)	ACLK	ACLK				–	–	–
SMCLK(internal)	SMCLK	SMCLK	SMCLK	SMCLK				–	–	–
PJ.6 - 28	PJ.6 - 32	PJ.6 - E5	TD1CLK	$\overline{TDCLK}$				–	–	–
–	–	–	from TD0 (internal)	CLK0						
P2.7 - 22	P2.7 - 26	P2.7 - C5	TEC1CLR	TECxCLR				–	–	–
P2.1 - 14 (1)	P2.1 - 18 (1)	P2.1 - A2	TD1.0	CCI0A	CCR0	TD0	TD0	P2.1 - 14 (1)	P2.1 - 18 (1)	P2.1 - A2 (1)
–	–	–	TD1.0	CCI0B				P2.7 - 22	P2.7 - 26	P2.7 - C5
–	–	–	V_{SS}	GND				–	–	–
–	–	–	V_{CC}	V_{CC}				–	–	–
P3.1 - 24	P3.1 - 28	P3.1 - C6	TEC1FLT0	TECXFLT0				–	–	–
P2.2 - 15 (1)	P2.2 - 19 (1)	P2.2 - A3	TD1.1	CCI1A	CCR1	TD1	TD1	P2.2 - 15 (1)	P2.2 - 19 (1)	P2.2 - A3 (1)
CBOUT (internal)	CBOUT (internal)	CBOUT (internal)	TD1.1	CCI1B				P3.0 - 23	P3.0 - 27	P3.0 - B6
–	–	–	V_{SS}	GND				–	–	–
–	–	–	V_{CC}	V_{CC}				–	–	–
P2.7 - 22	P2.7 - 26	P2.7 - C5	TEC1FLT1	TECXFLT1				–	–	–
P2.3 - 16 (1)	P2.3 - 20 (1)	P2.3 - C4	TD1.2	CCI2A	CCR2	TD2	TD2	P2.3 - 16 (1)	P2.3 - 20 (1)	P2.3 - C4 (1)
ACLK (internal)	ACLK (internal)	ACLK (internal)	TD1.2	CCI2B				P3.1 - 24	P3.1 - 28	P3.1 - C6
–	–	–	V_{SS}	GND				–	–	–
–	–	–	V_{CC}	V_{CC}				–	–	–
P3.0 - 23	P3.0 - 27	P3.0 - B6	TEC1FLT2	TECXFLT2				–	–	–

(1) Pins P2.1 for TD1.0, P2.2 for TD1.1, and P2.3 for TD1.2 are optimized for matching.

6.9.13 Comparator_B

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.9.14 ADC10_A (MSP430F51x2 Only)

The ADC10_A module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

6.9.15 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.9.16 Reference (REF) Module Voltage Reference

The REF is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

6.9.17 Embedded Emulation Module (EEM) (S Version)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.9.18 Peripheral File Map

Table 6-13 lists the base address and offset range for the registers of all peripherals.

Table 6-13. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 6-14)	0100h	000h–01Fh
PMM (see Table 6-15)	0120h	000h–010h
Flash Control (see Table 6-16)	0140h	000h–00Fh
CRC16 (see Table 6-17)	0150h	000h–007h
RAM Control (see Table 6-18)	0158h	000h–001h
Watchdog (see Table 6-19)	015Ch	000h–001h
UCS (see Table 6-20)	0160h	000h–01Fh
SYS (see Table 6-21)	0180h	000h–01Fh
Shared Reference (see Table 6-22)	01B0h	000h–001h
Port Mapping Control (see Table 6-23)	01C0h	000h–007h
Port Mapping Port P1 (see Table 6-24)	01C8h	000h–007h
Port Mapping Port P2 (see Table 6-25)	01D0h	000h–007h
Port Mapping Port P3 (see Table 6-26)	01D8h	000h–007h
Port P1, P2 (see Table 6-27)	0200h	000h–01Fh
Port P3 (see Table 6-28)	0220h	000h–01Fh
Port PJ (see Table 6-29)	0320h	000h–01Fh
TA0 (see Table 6-30)	03C0h	000h–03Fh
32-Bit Hardware Multiplier (see Table 6-31)	04C0h	000h–02Fh
DMA General Control (see Table 6-32)	0500h	000h–00Fh
DMA Channel 0 (see Table 6-33)	0500h	010h–00Ah
DMA Channel 1 (see Table 6-34)	0500h	020h–00Ah
DMA Channel 2 (see Table 6-35)	0500h	030h–00Ah
USCI_A0 (see Table 6-36)	05C0h	000h–01Fh
USCI_B0 (see Table 6-36)	05E0h	000h–01Fh
ADC10_A (see Table 6-38) (MSP430F51x2 only)	0740h	000h–01Fh
Comparator_B (see Table 6-39)	08C0h	000h–00Fh
TD0 (see Table 6-40)	0B00h	000h–03Fh
TEC0 (see Table 6-42)	0C00h	000h–007h
TD1 (see Table 6-41)	0B40h	000h–03Fh
TEC1 (see Table 6-43)	0C20h	000h–007h

Table 6-14. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 6-15. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high-side control	SVSMHCTL	04h
SVS low-side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

Table 6-16. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 6-17. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC result	CRC16INIRES	04h

Table 6-18. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 6-19. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 6-20. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

Table 6-21. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 6-22. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

Table 6-23. Port Mapping Control (Base Address: 01C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping password	PMAPPWD	00h
Port mapping control	PMAPCTL	02h

Table 6-24. Port Mapping for Port P1 (Base Address: 01C8h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1.0 mapping	P1MAP0	00h
Port P1.1 mapping	P1MAP1	01h
Port P1.2 mapping	P1MAP2	02h
Port P1.3 mapping	P1MAP3	03h
Port P1.4 mapping	P1MAP4	04h
Port P1.5 mapping	P1MAP5	05h
Port P1.6 mapping	P1MAP6	06h
Port P1.7 mapping	P1MAP7	07h

Table 6-25. Port Mapping for Port P2 (Base Address: 01D0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P2.0 mapping	P2MAP0	00h
Port P2.1 mapping	P2MAP2	01h
Port P2.2 mapping	P2MAP2	02h
Port P2.3 mapping	P2MAP3	03h
Port P2.4 mapping	P2MAP4	04h
Port P2.5 mapping	P2MAP5	05h
Port P2.6 mapping	P2MAP6	06h
Port P2.7 mapping	P2MAP7	07h

Table 6-26. Port Mapping for Port P3 (Base Address: 01D8h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3.0 mapping	P3MAP0	00h
Port P3.1 mapping	P3MAP1	01h
Port P3.2 mapping	P3MAP2	02h
Port P3.3 mapping	P3MAP3	03h
Port P3.4 mapping	P3MAP4	04h
Port P3.5 mapping	P3MAP5	05h
Port P3.6 mapping	P3MAP6	06h
Port P3.7 mapping	P3MAP7	07h

Table 6-27. Port Registers Port P1, P2 (Base Addresses: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 resistor enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 resistor enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 6-28. Port Registers P3 (Base Addresses: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 resistor enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah

Table 6-29. Port Registers PJ (Base Addresses: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ resistor enable	PJREN	06h
Port PJ drive strength	PJDS	08h
Port PJ selection	PJSEL	0Ah

Table 6-30. TA0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
TA0 counter	TA0R	10h
Capture/compare 0	TA0CCR0	12h
Capture/compare 1	TA0CCR1	14h
Capture/compare 2	TA0CCR2	16h
TA0 expansion 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 6-31. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control 0	MPY32CTL0	2Ch

Table 6-32. DMA General Control (Base Address: 0500h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

Table 6-33. DMA Channel 0 (Base Address: 0510h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah

Table 6-34. DMA Channel 1 (Base Address: 0520h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah

Table 6-35. DMA Channel 2 (Base Address: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah

Table 6-36. USCI0_A Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 0	UCA0CTL0	01h
USCI control 1	UCA0CTL1	00h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 6-37. USCI0_B Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 0	UCB0CTL0	00h
USCI synchronous control 1	UCB0CTL1	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

Table 6-38. ADC10_A Registers (MSP430F51x2 Devices Only) (Base Address: 0740h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC10_A control 0	ADC10CTL0	00h
ADC10_A control 1	ADC10CTL1	02h
ADC10_A control 2	ADC10CTL2	04h
ADC10_A window comparator low threshold	ADC10LO	06h
ADC10_A window comparator high threshold	ADC10HI	08h
ADC10_A memory control register 0	ADC10MCTL0	0Ah
ADC10_A conversion memory register	ADC10MEM0	12h
ADC10_A interrupt enable	ADC10IE	1Ah
ADC10_A interrupt flags	ADC10IGH	1Ch
ADC10_A interrupt vector word	ADC10IV	1Eh

Table 6-39. Comparator_B Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comparator_B control 0	CBCTL0	00h
Comparator_B control 1	CBCTL1	02h
Comparator_B control 2	CBCTL2	04h
Comparator_B control 3	CBCTL3	06h
Comparator_B interrupt	CBINT	0Ch
Comparator_B interrupt vector word	CBIV	0Eh

Table 6-40. TD0 Registers (Base Address: 0B00h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TD0 control 0	TD0CTL0	00h
TD0 control 1	TD0CTL1	02h
TD0 control 2	TD0CTL2	04h
TD0 counter	TD0R	06h
Capture/compare control 0	TD0CCTL0	08h
Capture/compare 0	TD0CCR0	0Ah
Capture/compare latch 0	TD0CL0	0Ch
Capture/compare control 1	TD0CCTL1	0Eh
Capture/compare 1	TD0CCR1	10h
Capture/compare latch 1	TD0CL1	12h
Capture/compare control 2	TD0CCTL2	14h
Capture/compare 2	TD0CCR2	16h
Capture/compare latch 2	TD0CL2	18h
TD0 high-resolution control 0	TD0HCTL0	38h
TD0 high-resolution control 1	TD0HCTL1	3Ah
TD0 high-resolution interrupt	TD0HINT	3Ch
TD0 interrupt vector	TD0IV	3Eh

Table 6-41. TD1 Registers (Base Address: 0B40h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TD1 control 0	TD1CTL0	00h
TD1 control 1	TD1CTL1	02h
TD1 control 2	TD1CTL2	04h
TD1 counter	TD1R	06h
Capture/compare control 0	TD1CCTL0	08h
Capture/compare 0	TD1CCR0	0Ah
Capture/compare latch 0	TD1CL0	0Ch
Capture/compare control 1	TD1CCTL1	0Eh
Capture/compare 1	TD1CCR1	10h
Capture/compare latch 1	TD1CL1	12h
Capture/compare control 2	TD1CCTL2	14h
Capture/compare 2	TD1CCR2	16h
Capture/compare latch 2	TD1CL2	18h
TD1 high-resolution control 0	TD1HCTL0	38h
TD1 high-resolution control 1	TD1HCTL1	3Ah
TD1 high-resolution interrupt	TD1HINT	3Ch
TD1 interrupt vector	TD1IV	3Eh

Table 6-42. TEC0 Registers (Base Address: 0C00h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Timer event control 0 external control 0	TEC0CTL0	00h
Timer event control 0 external control	TEC0CTL1	02h
Timer event control 0 external control	TEC0CTL2	04h
Timer event control 0 status	TEC0STA	06h
Timer event control 0 external interrupt	TEC0XINT	08h
Timer event control 0 external interrupt vector	TEC0IV	0Ah

Table 6-43. TEC1 Registers (Base Address: 0C20h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Timer event control 1 external control 0	TEC1CTL0	00h
Timer event control 1 external control	TEC1CTL1	02h
Timer event control 1 external control	TEC1CTL2	04h
Timer event control 1 status	TEC1STA	06h
Timer event control 1 external interrupt	TEC1XINT	08h
Timer event control 1 external interrupt vector	TEC1IV	0Ah

6.10 Input/Output Diagrams

6.10.1 Port P1 (P1.0 to P1.5) Input/Output With Schmitt Trigger

Figure 6-2 shows the port diagram. Table 6-44 summarizes the selection of the pin function.

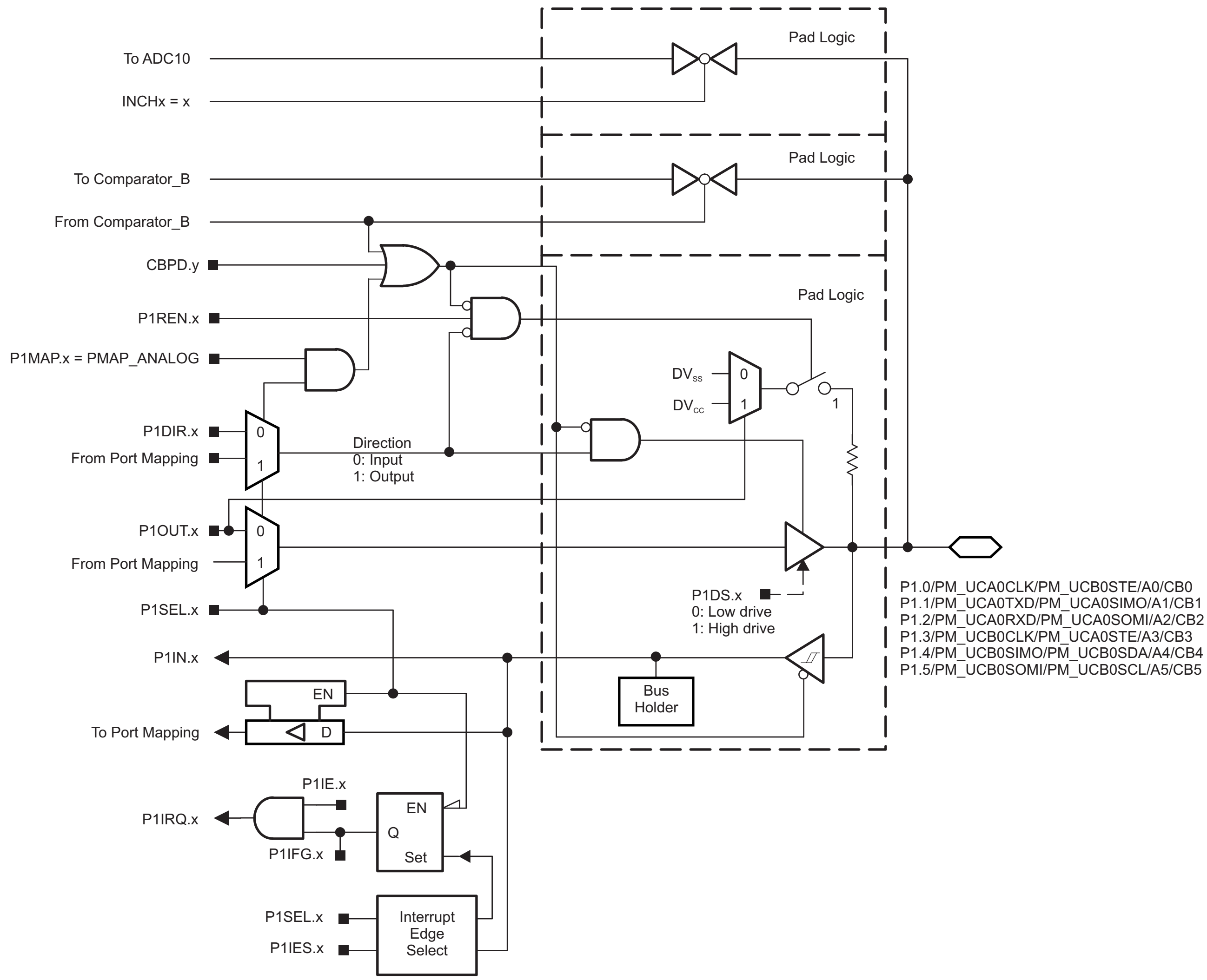


Figure 6-2. Port P1 (P1.0 to P1.5) Diagram

Table 6-44. Port P1 (P1.0 to P1.5) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P1DIR.x	P1SEL.x	P1MAP.x	CBPD.y
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	X	0
PM_UCA0CLK/ PM_UCB0STE/		UCA0CLK/UCB0STE(2) (3)	0	1	default	0
A0/		A0(4)	X	1	31 INCHx = 0	X
CB0		CB0	X	X	X	1 (y = 0)
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0	X	0
PM_UCA0TXD/ PM_UCA0SIMO/		PM_UCA0TXD/PM_UCA0SIMO(2)	0	1	default	0
A1/		A1(4)	X	1	31 INCHx = 1	X
CB1		CB1	X	X	X	1 (y = 1)
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	X	0
PM_UCA0RXD/ PM_UCA0SOMI/		PM_UCA0RXD/PM_UCA0SOMI(2)	0	1	default	0
A2/		A2(4)	X	1	31 INCHx = 2	X
CB2		CB2	X	X	X	1 (y = 2)
P1.3/	3	P1.x (I/O)	I: 0; O: 1	0	X	0
PM_UCB0CLK/ PM_UCA0STE/		UCB0CLK/UCA0STE(2)	0	1	default	0
A3/		A3(4)	X	1	31 INCHx = 3	X
CB3		CB3	X	X	X	1 (y = 3)
P1.4/	4	P1.x (I/O)	I: 0; O: 1	0	X	0
PM_UCB0SIMO/ PM_UCB0SDA/		PM_UCB0SIMO/PM_UCB0SDA(2) (5)	0	1	default	0
A4/		A4(4)	X	1	31 INCHx = 4	X
CB4		CB4	X	X	X	1 (y = 4)
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	X	0
PM_UCB0SOMI/ PM_UCB0SCL/		PM_UCB0SOMI/PM_UCB0SCL(2) (5)	0	1	default	0
A5/		A5(4)	X	1	31 INCHx = 5	X
CB5		CB5	X	X	X	1 (y = 5)

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) MSP430F51x2 device only
(5) If the I^2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

6.10.2 Port P1 (P1.6 to P1.7) Input/Output With Schmitt Trigger

Figure 6-3 shows the port diagram. Table 6-45 summarizes the selection of the pin function.

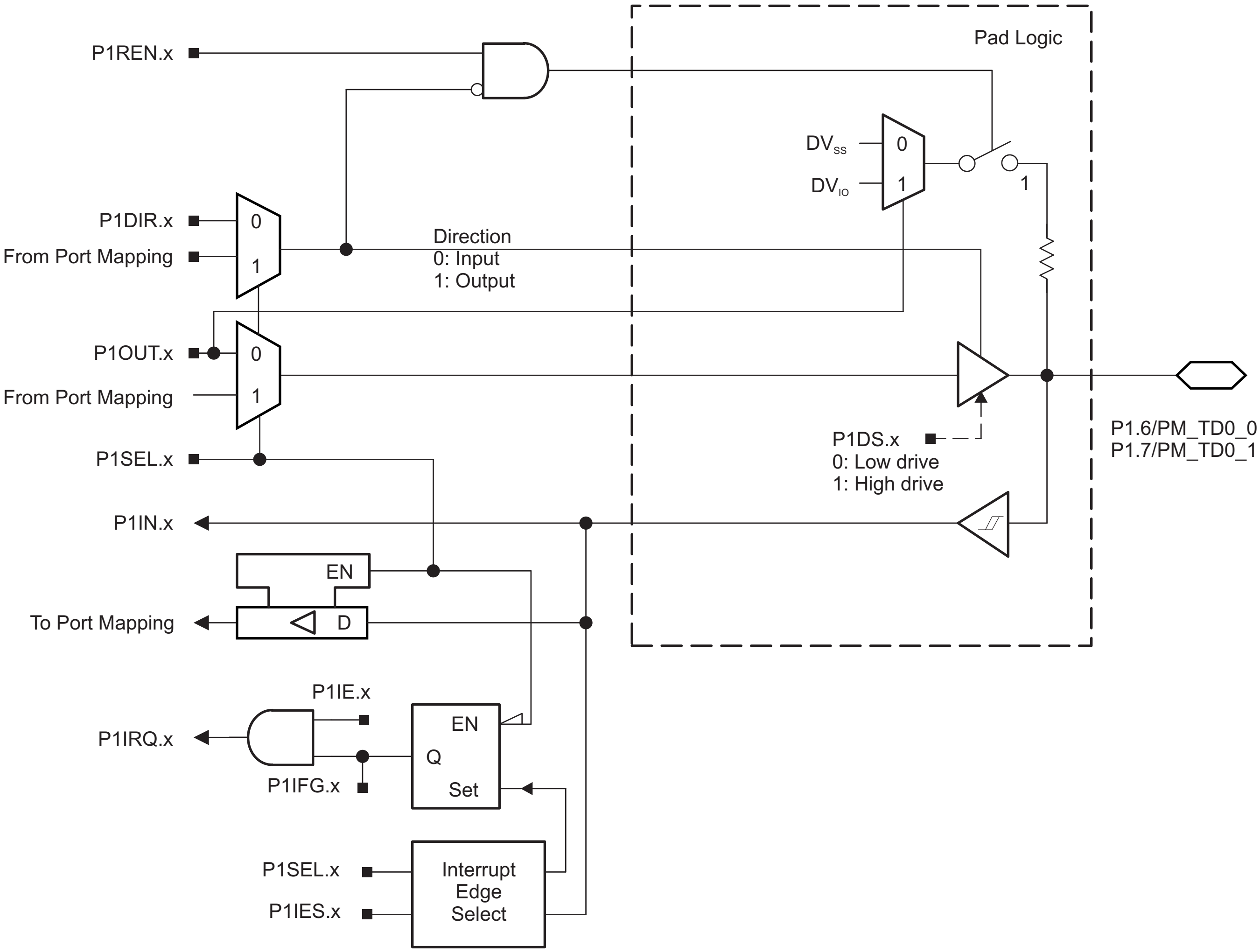


Figure 6-3. Port P1 (P1.6 and P1.7) Diagram

Table 6-45. Port P1 (P1.6 and P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[(1)]		
			P1DIR.x	P1SEL.x	P1MAP.x
P1.6/		P1.x (I/O)	I: 0; O: 1	0	X
PM_TD0.0	6	TD0.CCI0A	0	1	default
		TD0.TA0	1	1	default
P1.7/		P1.x (I/O)	I: 0; O: 1	0	X
PM_TD0.1	7	TD0.CCI1A	0	1	default
		TD0.TA1	1	1	default

(1) X = Don't care

6.10.3 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

Figure 6-4 shows the port diagram. Table 6-46 summarizes the selection of the pin function.

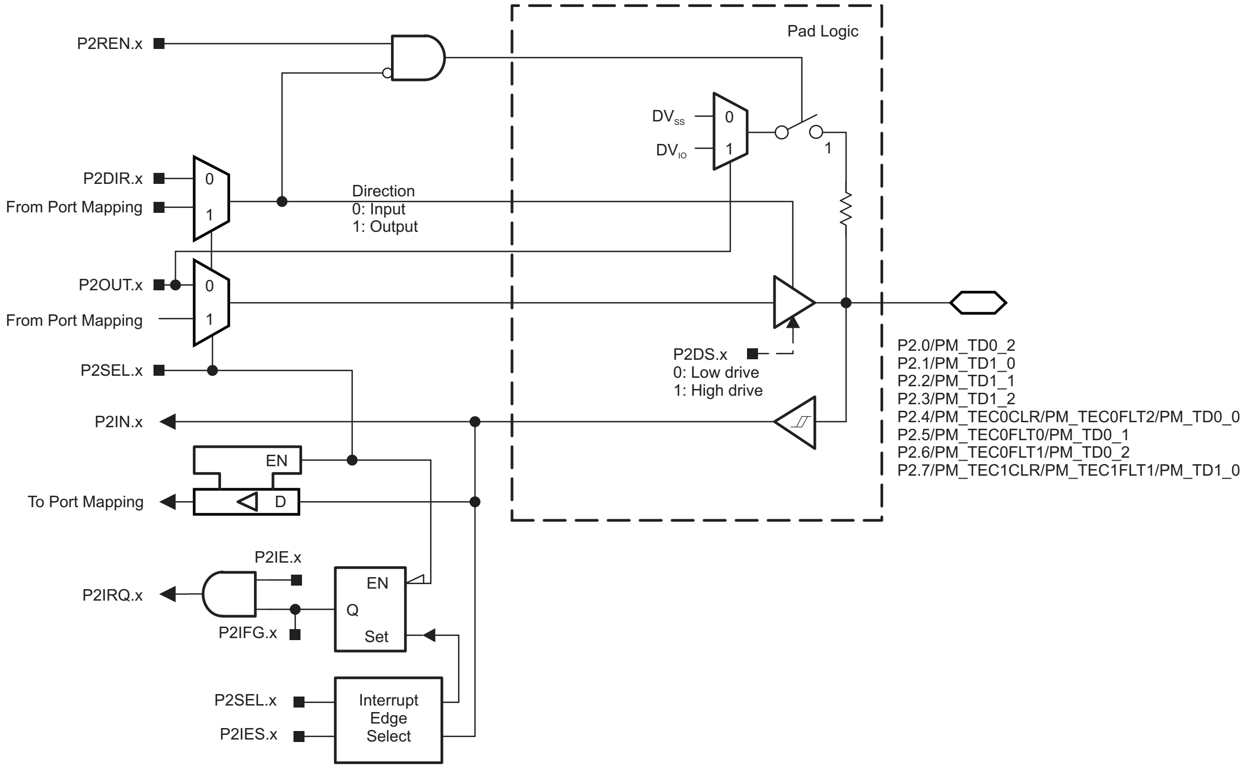


Figure 6-4. Port P2 (P2.0 to P2.7) Diagram

Table 6-46. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P2DIR.x	P2SEL.x	P2MAP.x
P2.0/		P2.x (I/O)	I: 0; O: 1	0	X
PM_TD0.2	0	TD0.CCI2A	0	1	default
		TD0.TA2	1	1	default
P2.1/		P2.x (I/O)	I: 0; O: 1	0	X
PM_TD1.0	1	TD1.CCI0A	0	1	default
		TD1.TA0	1	1	default
P2.2/		P2.x (I/O)	I: 0; O: 1	0	X
PM_TD1.1	2	TD1.CCI1A	0	1	default
		TD1.TA1	1	1	default
P2.3/		P2.x (I/O)	I: 0; O: 1	0	0
PM_TD1.2	3	TD1.CCI2A	0	1	default
		TD1.TA2	1	1	default
P2.4/		P2.x (I/O)	I: 0; O: 1	0	X
PM_TEC0CLR/	4	TD0.TECEXTCLR, controlled by enable signals in the TEC0 module	0	1	default
PM_TEC0FLT2/		TD0.TECXFLT2, controlled by enable signals in the TEC0 module	0	1	default
PM_TD0.0		TD0.TA0	1	1	default
P2.5/		P2.x (I/O)	I: 0; O: 1	0	x
PM_TEC0FLT0/	5	TD0.TECXFLT0, controlled by enable signals in the TEC0 module	0	1	default
PM_TD0.1		TD0.TA1	1	1	default
P2.6/		P2.x (I/O)	I: 0; O: 1	0	X
PM_TEC0FLT1/	6	TD0.TECXFLT1, controlled by enable signals in the TEC0 module	0	1	default
PM_TD0.2		TD0.TA2	1	1	default
P2.7/		P2.x (I/O)	I: 0; O: 1	0	X
PM_TEC1CLR/	7	TD1.TECEXTCLR, controlled by enable signals in the TEC1 module	0	1	default
PM_TEC1FLT1/		TD1.TECXFLT1, controlled by enable signals in the TEC1 module	0	1	default
PM_TD1.0		TD1.TA0	1	1	default

6.10.4 Port P3 (P3.0 and P3.1) Input/Output With Schmitt Trigger

Figure 6-5 shows the port diagram. Table 6-47 summarizes the selection of the pin function.

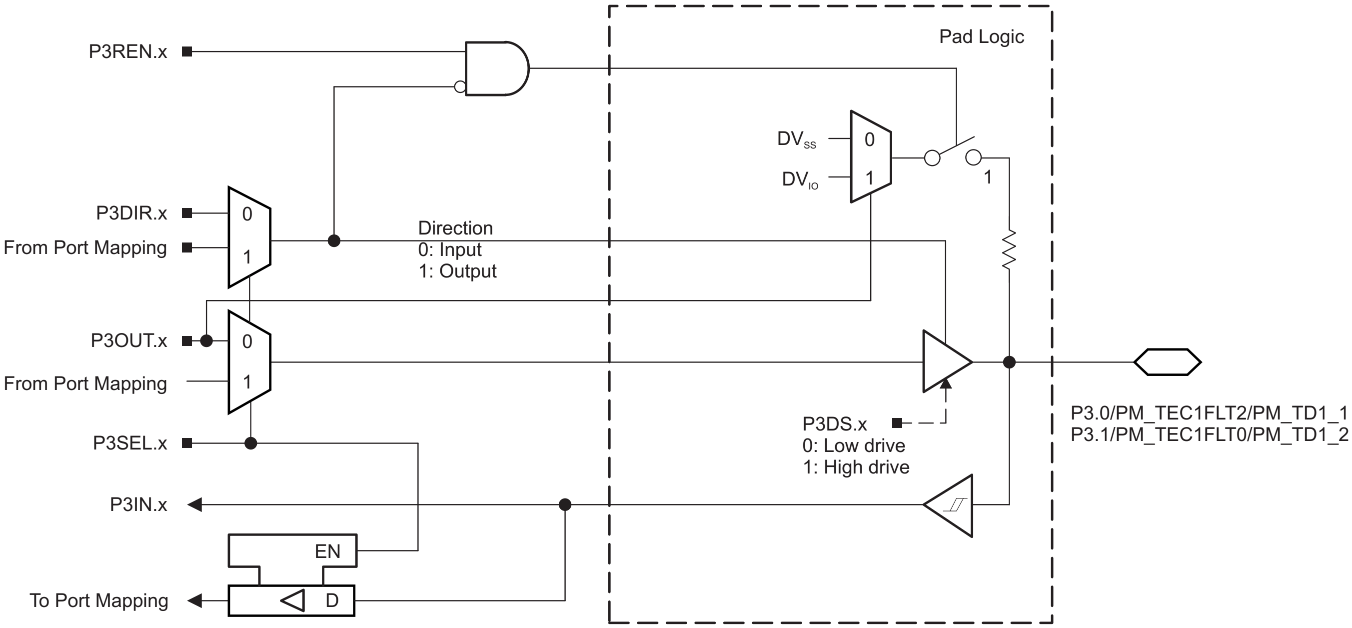


Figure 6-5. Port P3 (P3.0 and P3.1) Diagram

Table 6-47. Port P3 (P3.0 and P3.1) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P3DIR.x	P3SEL.x	P3MAP.x
P3.0/	0	P3.x (I/O)	I: 0; O: 1	0	X
PM_TEC1FLT2/		TD1.TECXFLT2, controlled by enable signals in the TEC1 module	0	1	default
PM_TD1.1		TD1.TA1	1	1	default
P3.1/	1	P3.x (I/O)	I: 0; O: 1	0	X
PM_TEC1FLT0/		TD1.TECXFLT0, controlled by enable signals in the TEC1 module	0	1	default
PM_TD1.2		TD1.TA2	1	1	default

6.10.5 Port P3 (P3.2 and P3.3) Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-48 summarizes the selection of the pin function.

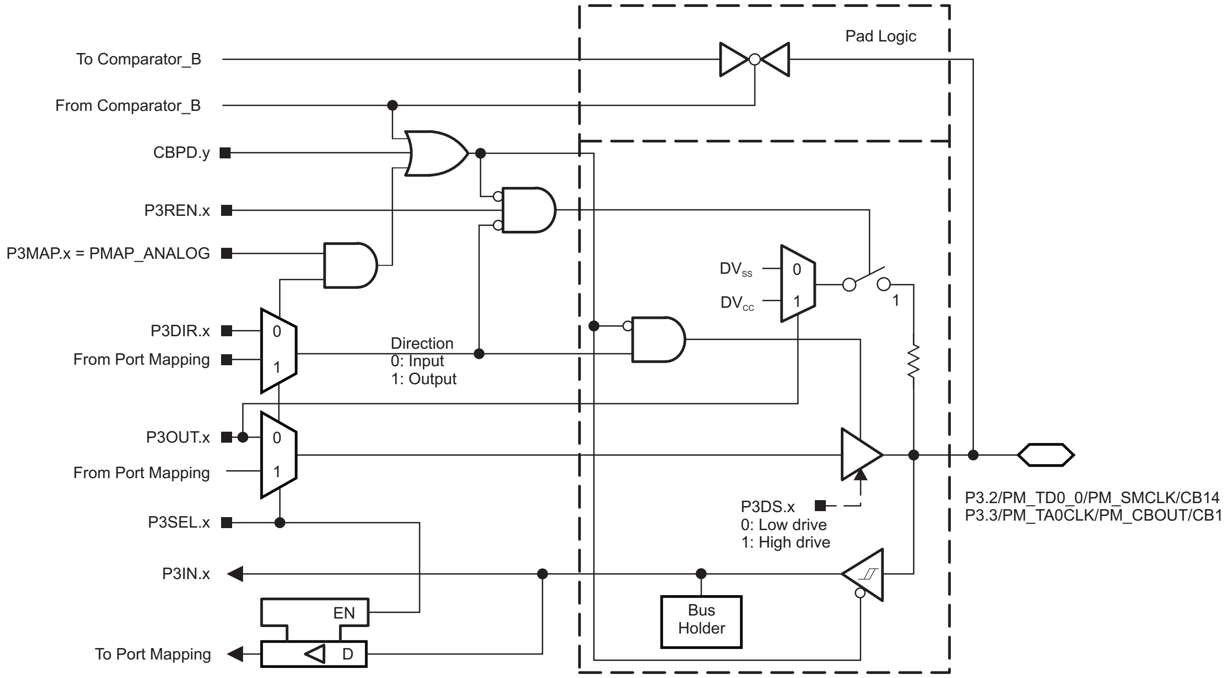


Figure 6-6. Port P3 (P3.2 and P3.3) Diagram

Table 6-48. Port P3 (P3.2 and P3.3) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P3DIR.x	P3SEL.x	P3MAP.x	CBPD.y
P3.2/	2	P3.x (I/O)	I: 0; O: 1	0	X	0
PM_TD0.0/		TD0.CCI0A	0	1	default	0
PM_SMCLK/		SMCLK output	1	1	default	0
CB14		CB14	X	X	X	1 (y = 14)
P3.3/	3	P3.x (I/O)	I: 0; O: 1	0	X	0
PM_TA0CLK/		TA0.TA0CLK	0	1	default	0
PM_CBOUT/		CBOUT	1	1	default	0
CB13		CB13	X	X	X	1 (y = 13)

(1) X = Don't care

6.10.6 Port P3 (P3.4) Input/Output With Schmitt Trigger

Figure 6-7 shows the port diagram. Table 6-49 summarizes the selection of the pin function.

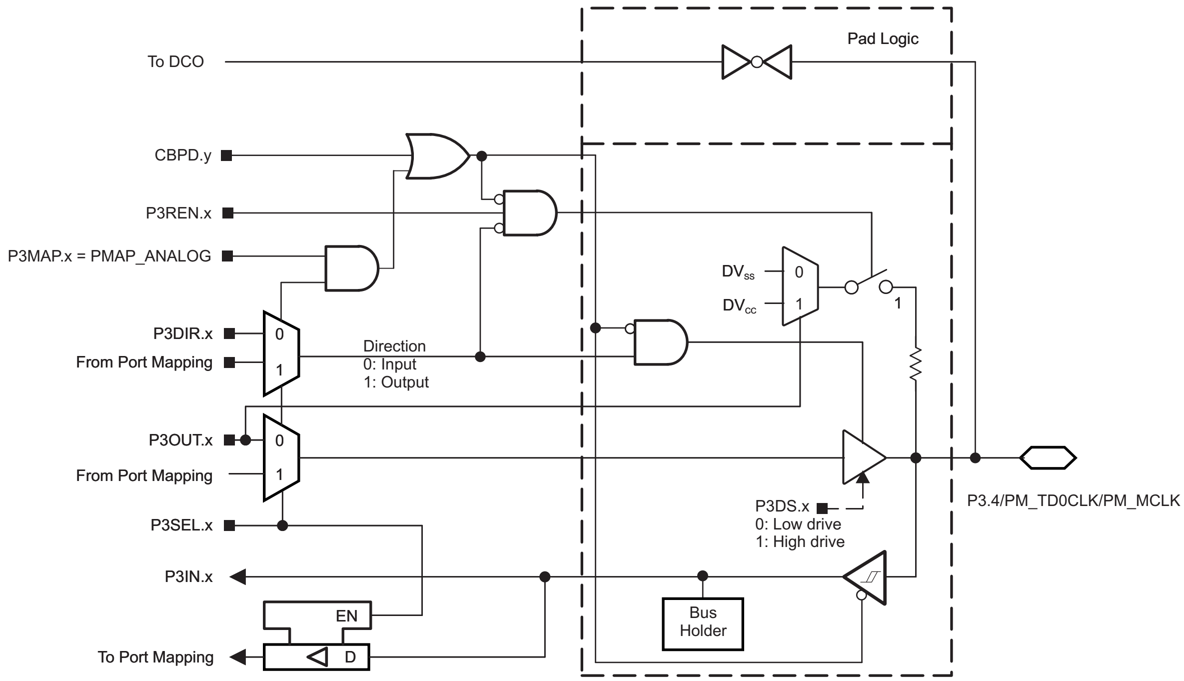


Figure 6-7. Port P3 (P3.4) Diagram

Table 6-49. Port P3 (P3.4) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P3DIR.x	P3SEL.x	P3MAP.x	
P3.4/	4	P3.x (I/O)	I: 0; O: 1	0	X	0
PM_TD0CLK/		TD0 clock input	0	1	default	0
PM_MCLK		MCLK output	1	1	default	0

(1) X = Don't care

6.10.7 Port P3 (P3.5) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-50 summarizes the selection of the pin function.

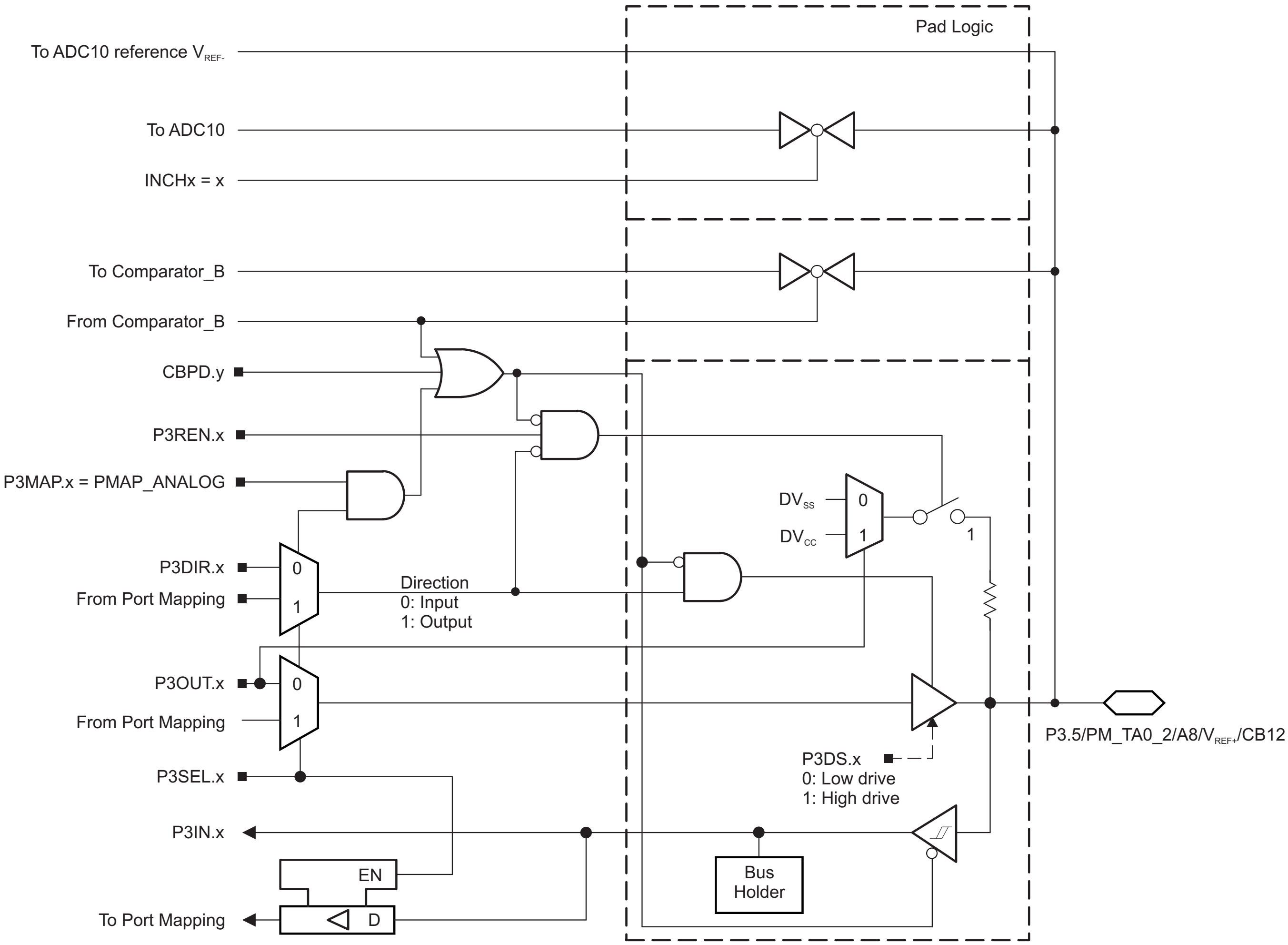


Figure 6-8. Port P3 (P3.5) Diagram

Table 6-50. Port P3 (P3.5) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P3DIR.x	P3SEL.x	P3MAP.x	CBPD.y
P3.5/	5	P3.x (I/O)	I: 0; O: 1	0	X	0
PM_TA0.2/		TA0.CCI2A	0	1	default	0
		TA0.TA2	1	1	default	0
VEREF+/		VEREF+(2)	X	1	31	X
A8/		A8(2)	X	1	INCHx=8	X
CB12		CB12	X	X	X	1 (y = 12)

(1) X = Don't care
(2) MSP430F51x2 devices only.

6.10.8 Port P3 (P3.6) Input/Output With Schmitt Trigger

Figure 6-9 shows the port diagram. Table 6-51 summarizes the selection of the pin function.

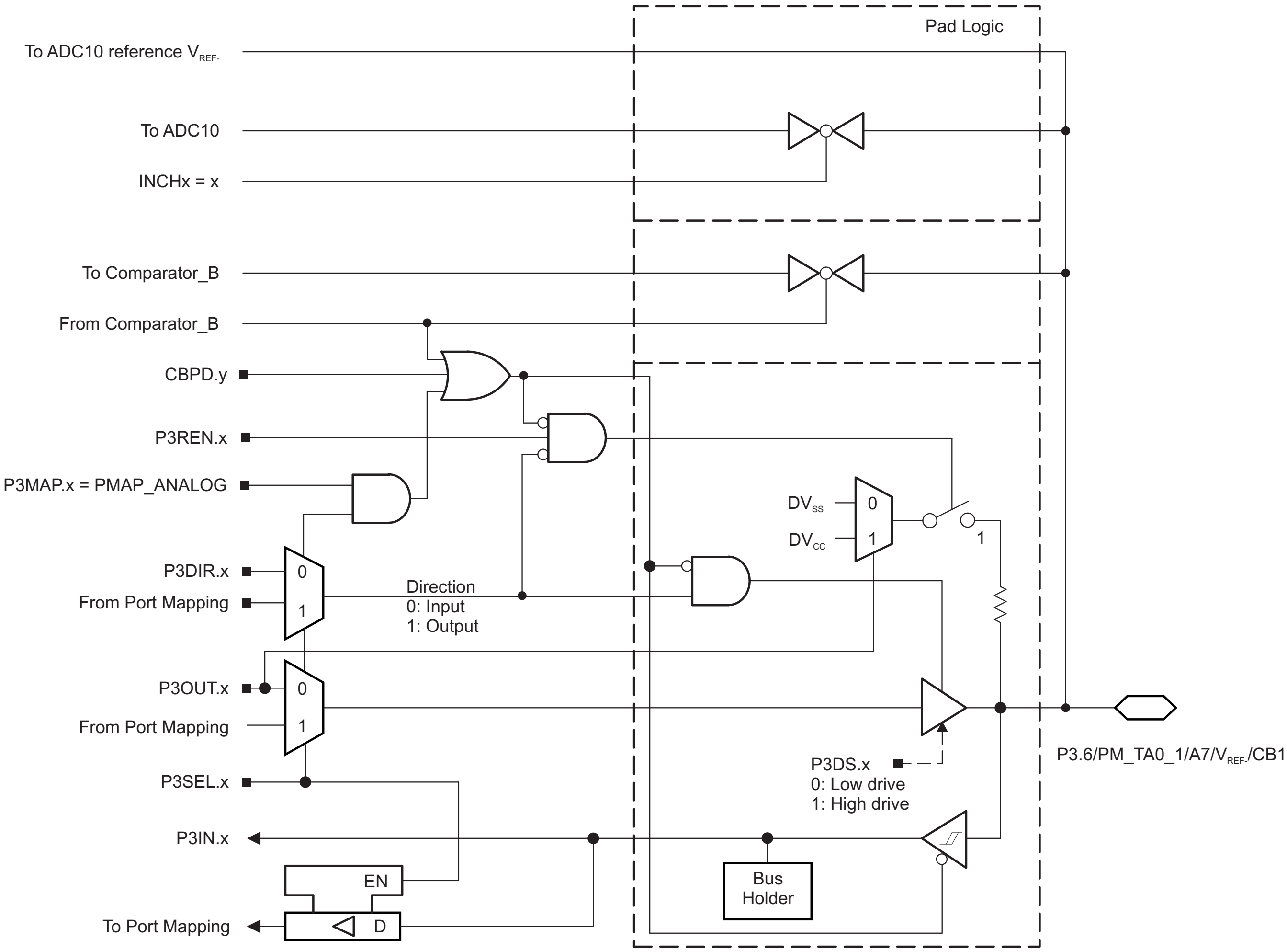


Figure 6-9. Port P3 (P3.6) Diagram

Table 6-51. Port P3 (P3.6) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P3DIR.x	P3SEL.x	P3MAP.x	CBPD.y
P3.6/	6	P3.x (I/O) (2)	I: 0; O: 1	0	X	0
PM_TA0.1/		TA0.CCR0	0	1	default	0
		TA0.TA1	1	1	default	0
VEREF-/		VEREF- (3)	X	1	31	X
A7/		A7 (3)	X	1	31 INCHx = 7	X
CB11		CB11	X	X	0	1 (y = 11)

(1) X = Don't care
(2) Default condition.
(3) MSP430F51x2 devices only.

6.10.9 Port P3 (P3.7) Input/Output With Schmitt Trigger

Figure 6-10 shows the port diagram. Table 6-52 summarizes the selection of the pin function.

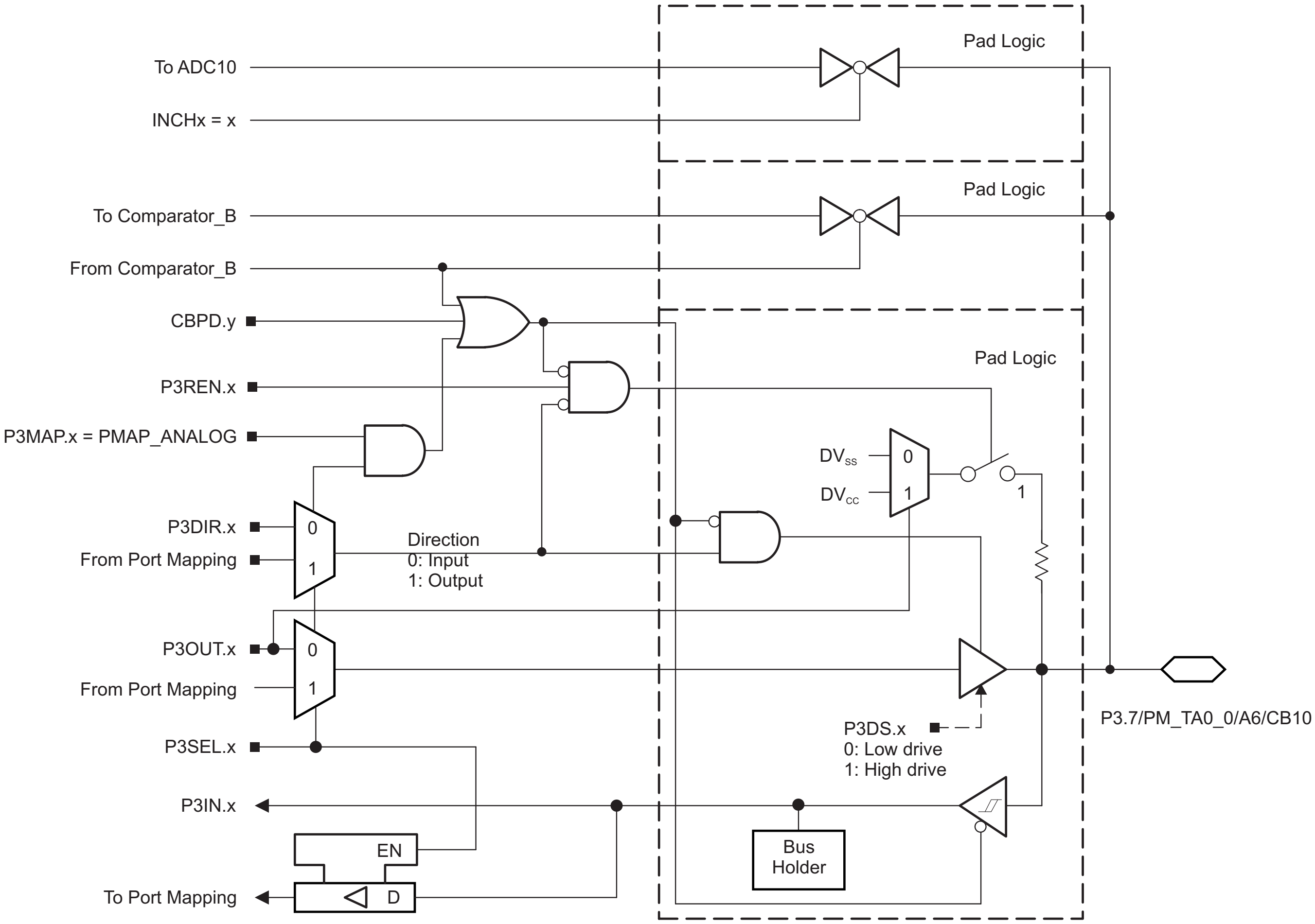


Figure 6-10. Port P3 (P3.7) Diagram

Table 6-52. Port P3 (P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			P3DIR.x	P3SEL.2	P3MAP.x	CBPD.y
P3.7/	7	P3.x (I/O) (1)	I: 0; O: 1	0	X	0
PM_TA0.0/		TA0.CCR0	0	1	default	0
		TA0.TA0	1	1	default	0
A6/		A6 (2)	X	1	31 INCHx = 6	X
CB10		CB10	X	X	0	1 (y = 10)

(1) X = Don't care
(2) MSP430F51x2 devices only.

6.10.10 Port J (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 6-11 shows the port diagram. Table 6-53 summarizes the selection of the pin function.

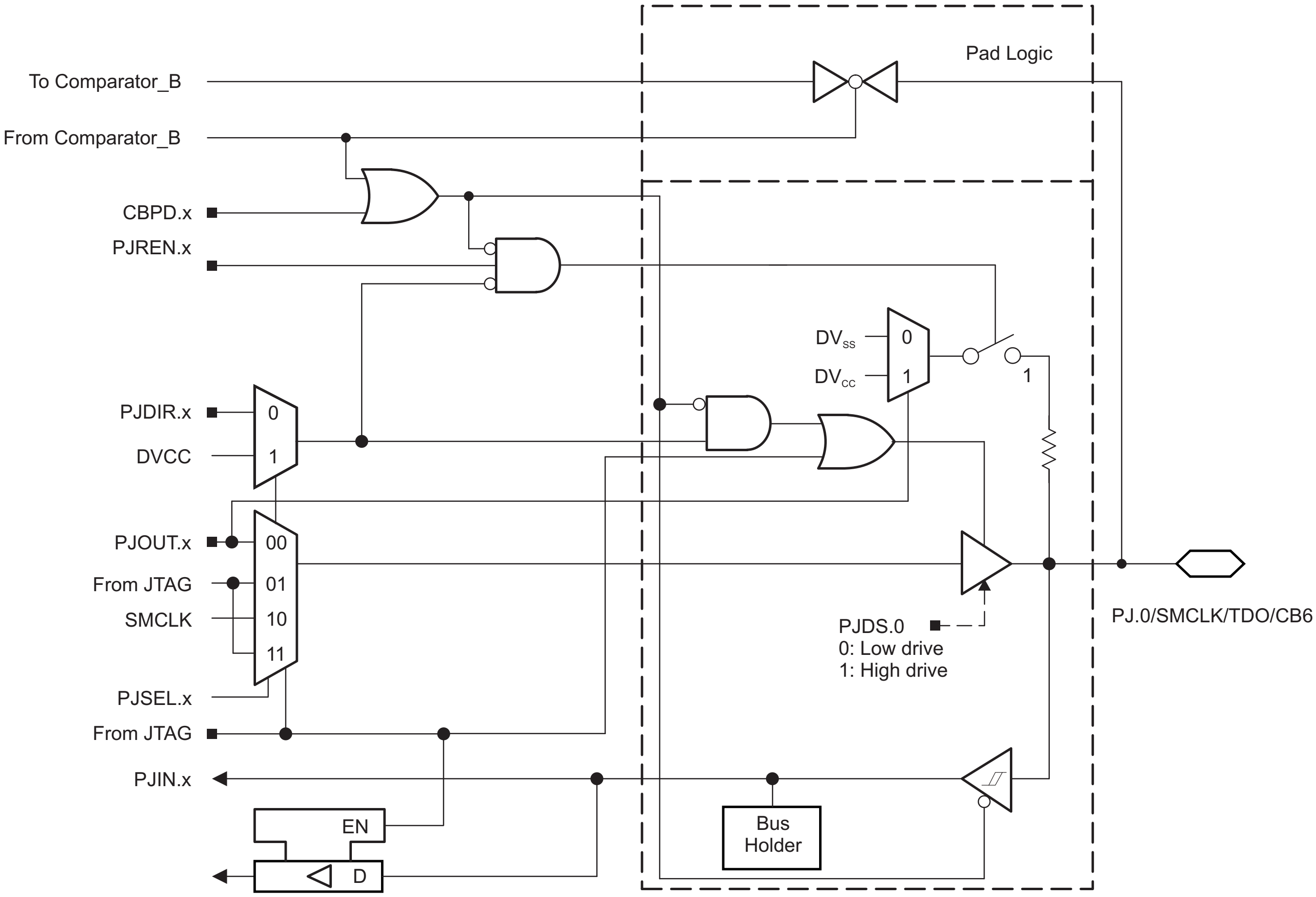


Figure 6-11. Port PJ (PJ.0) Diagram

6.10.11 Port J (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 6-12 shows the port diagram. Table 6-53 summarizes the selection of the pin function.

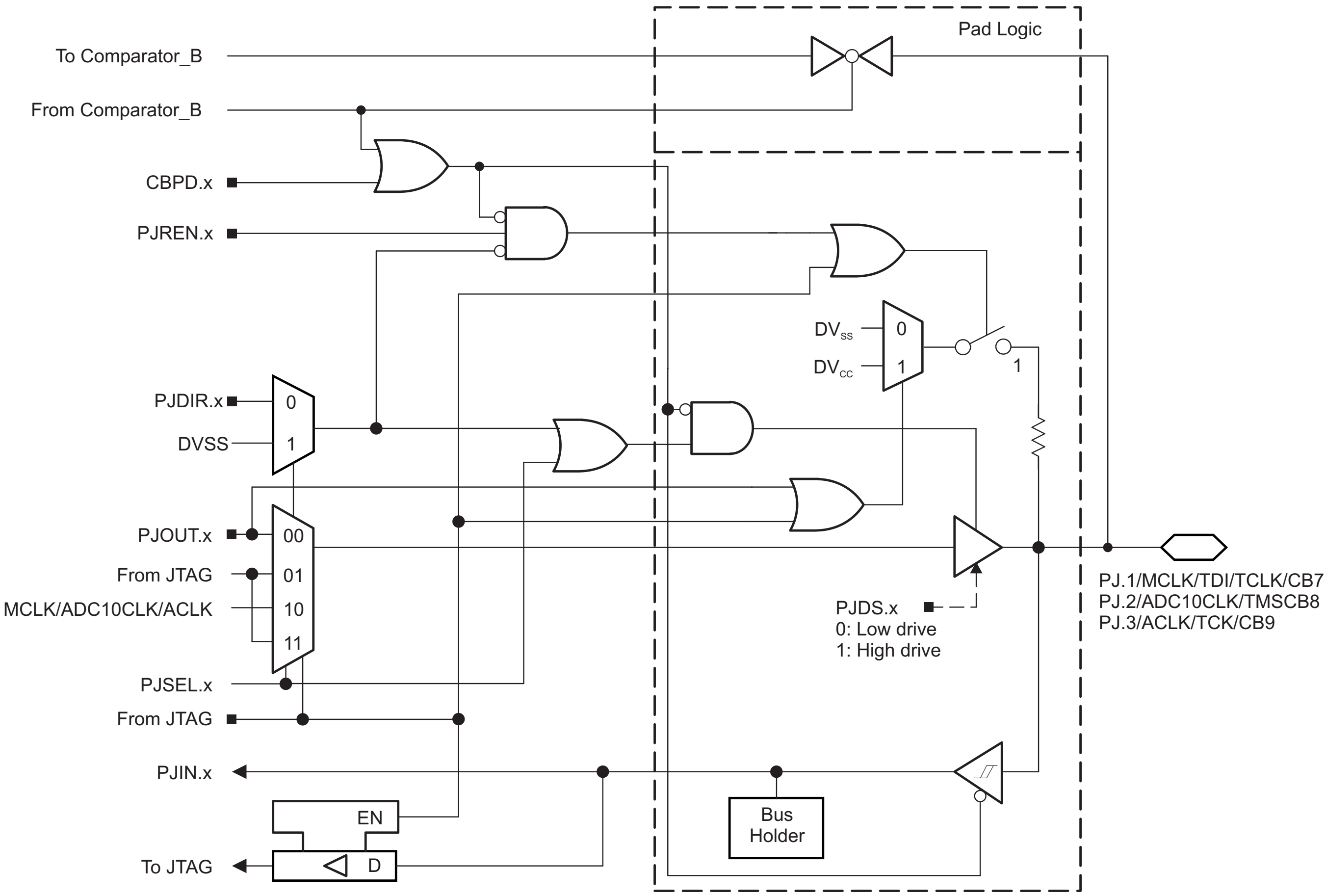


Figure 6-12. Port PJ (PJ.1 to PJ.3) Diagram

Table 6-53. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]			
			PJDIR.x	PJSEL.x	JTAG MODE	CBPD.y
PJ.0/	0	PJ.x (I/O)[2]	I: 0; O: 1	0	0	0
SMCLK/		SMCLK	1	1	0	0
TDO/		TDO[3]	X	X	1	X
CB6		CB6	X	X	0	1 (y = 6)
PJ.1/	1	PJ.x (I/O)[2]	I: 0; O: 1	0	0	0
MCLK/		MCLK	1	1	0	0
TDI/TCLK/		TDI/TCLK[3] [4]	X	X	1	X
CB7		CB7	0	X	0	1 (y = 7)
PJ.2/	2	PJ.x (I/O)[2]	I: 0; O: 1	0	0	0
ADC10CLK/		ADC10CLK (See [5])	1	1	0	0
TMS/		TMS[3] [4]	X	X	1	X
CB8		CB8	X	X	0	1 (y = 8)
PJ.3/	3	PJ.x (I/O)[2]	I: 0; O: 1	0	0	0
ACLK/		ACLK	1	1	0	0
TCK/		TCK[3] [4]	X	X	1	X
CB9		CB9	X	X	0	1 (y = 9)

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.
(5) MSP430F51x2 device only.

6.10.12 Port J (PJ.4) Input/Output With Schmitt Trigger

Figure 6-13 shows the port diagram. Table 6-54 summarizes the selection of the pin function.

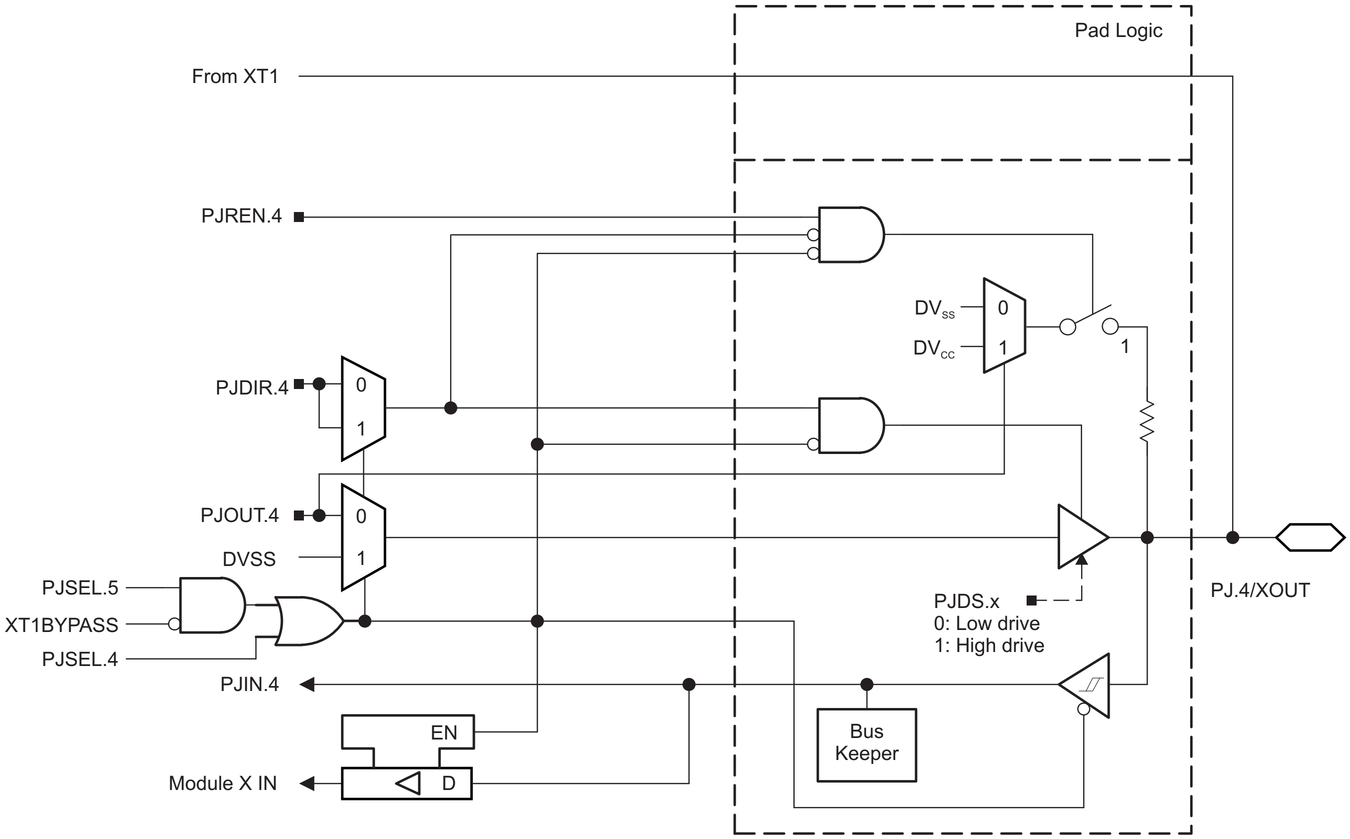


Figure 6-13. Port PJ (PJ.4) Diagram

6.10.13 Port J (PJ.5) Input/Output With Schmitt Trigger

Figure 6-14 shows the port diagram. Table 6-54 summarizes the selection of the pin function.

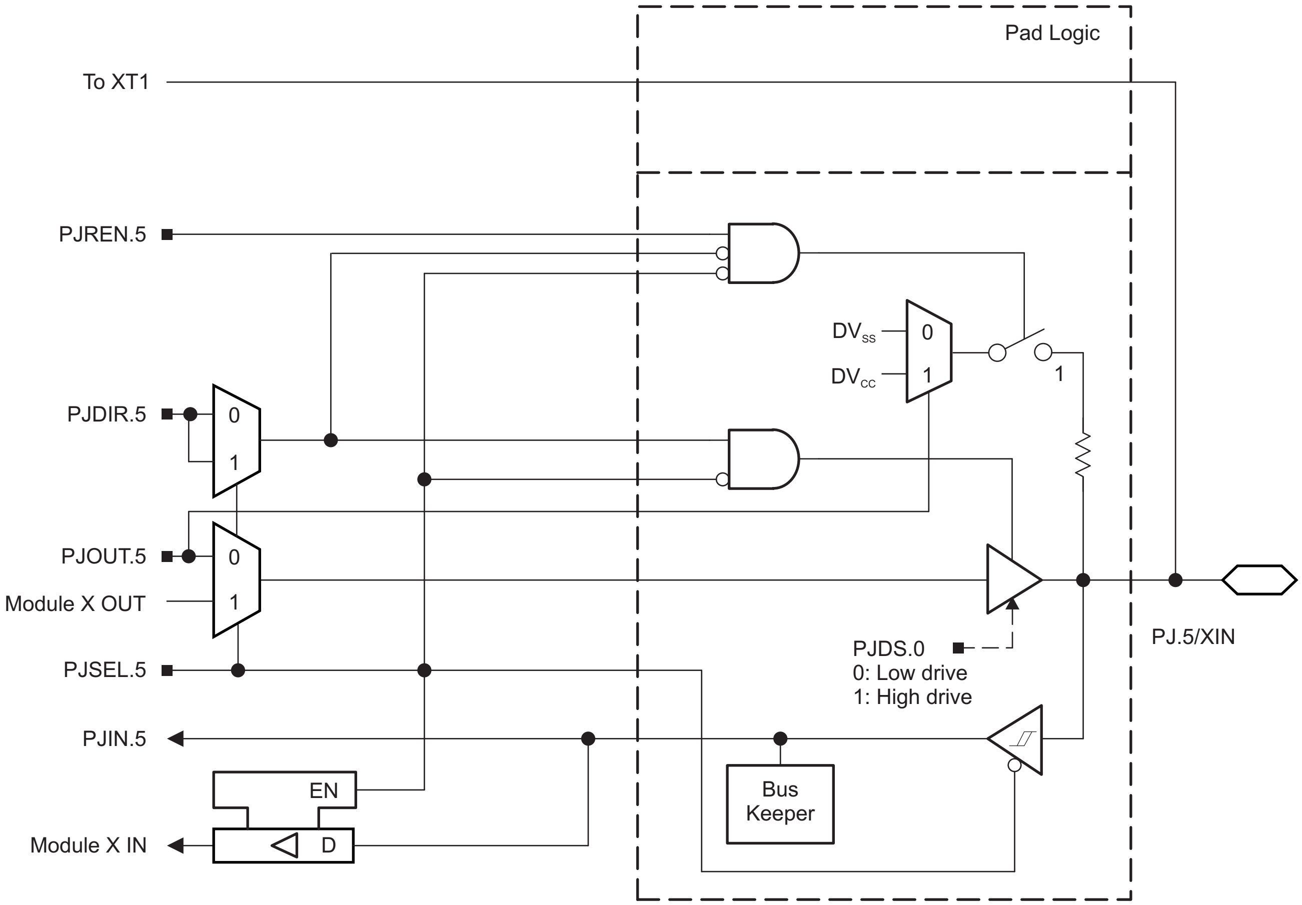


Figure 6-14. Port PJ (PJ.5) Diagram

Table 6-54. Port PJ (PJ.4 and PJ.5) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)			
			PJDIR.x	PJSEL.4	PJSEL.5	XT1BYPASS
PJ.4/	4	PJ.4 (I/O)	I: 0; O: 1	0	0	X
					1	1
XOUT		XOUT crystal mode (2)	X	X	1	0
PJ.5/	5	PJ.5 (I/O) (2)	I: 0; O: 1	X	0	x
XIN		XIN crystal mode (3)	X	X	1	0
		XIN bypass mode (3)	X	X	1	1

(1) X = Don't care
(2) Setting PJSEL.5 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, PJ.4 can be used as general-purpose I/O.
(3) Setting PJSEL.5 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, PJ.5 is configured for crystal mode or bypass mode.

6.10.14 Port J (PJ.6) Input/Output With Schmitt Trigger

Figure 6-15 shows the port diagram. Table 6-55 summarizes the selection of the pin function.

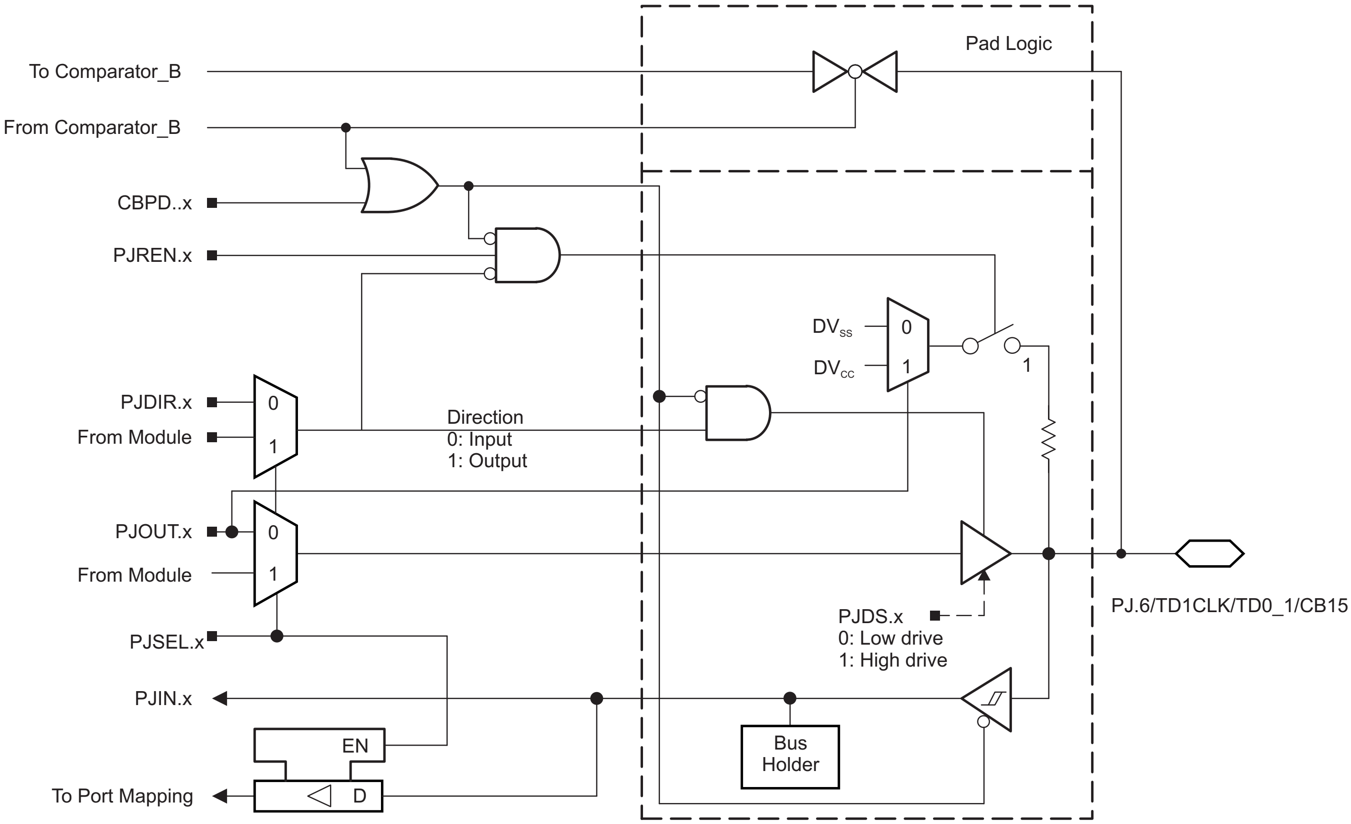


Figure 6-15. Port PJ (PJ.6) Diagram

Table 6-55. Port PJ (PJ.6) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			PJDIR.x	PJSEL.x	CBPD.y
PJ.6/	6	PJ.x (I/O)	I: 0; O: 1	0	0
TD1CLK/		TD1 clock input	0	1	0
TD0.1/		TD0.TA1	1	1	0
CB15		CB15	X	X	1 (y = 15)

(1) X = Don't care

6.11 Device Descriptors

Table 6-56 and Table 6-57 list the complete contents of the device descriptor tag-length-value (TLV) structure for the MSP430F51x2 and MSP430F51x1 devices, respectively.

Table 6-56. MSP430F51x2 Device Descriptor Table(1)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE					
				F5172		F5152		F5132	
				RSB, YFF	DA	RSB	DA	RSB	DA
Info Block	Info length	0x1A00	1	0x06	0x06	0x06	0x06	0x06	0x06
	CRC length	0x1A01	1	0x06	0x06	0x06	0x06	0x06	0x06
	CRC value	0x1A02	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Device ID	0x1A04	1	0x30	0x30	0x2C	0x2C	0x28	0x28
	Device ID	0x1A05	1	0x80	0x80	0x80	0x80	0x80	0x80
	Hardware revision	0x1A06	1	0x30	030	0x30	0x30	0x30	0x30
	Firmware revision	0x1A07	1	0x10	0x10	0x10	0x10	0x10	0x10
Die Record	Die record tag	0x1A08	1	0x08	08	0x08	08	0x08	08
	Die record length	0x1A09	1	0x0A	0A	0x0A	0A	0x0A	0A
	Lot/wafer ID	0x1A0A	4	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Die X position	0x1A0Eh	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Die Y position	0x1A10	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Test results	0x1A12	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
ADC10 Calibration	ADC10 calibration tag	0x1A14	1	0x13	0x13	0x13	0x13	0x13	0x13
	ADC10 calibration length	0x1A15	1	0x10	0x10	0x10	0x10	0x10	0x10
	ADC gain factor	0x1A16	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC offset	0x1A18	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V reference Temperature sensor 30°C	0x1A1A	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V reference Temperature sensor 85°C	0x1A1C	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V reference Temperature sensor 30°C	0x1A1Eh	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V reference Temperature sensor 85°C	0x1A20	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V reference Temperature sensor 30°C	0x1A22	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V reference Temperature sensor 85°C	0x1A24	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
REF User Calibration	REF tag	0x1A26	1	0x12	0x12	0x12	0x12	0x12	0x12
	REF length	0x1A27	1	0x06	0x06	0x06	0x06	0x06	0x06
	REF 1.5-V reference	0x1A28	2	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	REF 2.0-V reference	0x1A2A	2	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	REF 2.5-V reference	0x1A2C	2	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
Timer_D0 Calibration	Timer_D tag	0x1A2E	1	0x15	0x15	0x15	0x15	0x15	0x15
	Timer_D length	0x1A2F	1	0x08	0x08	0x08	0x08	0x08	0x08
	Timer_D 64-MHz frequency	0x1A30	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 128-MHz frequency	0x1A32	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 200-MHz frequency	0x1A34	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 256-MHz frequency	0x1A36	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
Timer_D1 Calibration	Timer_D tag	0x1A38	1	0x15	0x15	0x15	0x15	0x15	0x15
	Timer_D length	0x1A39	1	0x08	0x08	0x08	0x08	0x08	0x08
	Timer_D 64-MHz frequency	0x1A3A	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 128-MHz frequency	0x1A3C	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 200-MHz frequency	0x1A3E	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 256-MHz frequency	0x1A40	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit

(1) NA = Not applicable

Table 6-56. MSP430F51x2 Device Descriptor Table(1) (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE					
				F5172		F5152		F5132	
				RSB, YFF	DA	RSB	DA	RSB	DA
Peripheral Descriptor	Peripheral descriptor tag	0x1A42	1	0x02	0x02	0x02	0x02	0x02	0x02
	Peripheral descriptor length	0x1A43	1	0x53	0x53	0x53	0x53	0x53	0x53
	BSL memory	0x1A44	2	0x8A08	0x8A08	0x8A08	0x8A08	0x8A08	0x8A08
	Information memory	0x1A46	2	0x860C	0x860C	0x860C	0x860C	0x860C	0x860C
	RAM	0x1A48	2	0x2A0E	0x2A0E	0x2A0E	0x2A0E	0x280E	0x280E
	Main memory	0x1A4A	2	0x9240	0x9240	0x9060	0x9060	0x8E70	0x8E70
	Delimiter	0x1A4C	1	0x00	0x00	0x00	0x00	0x00	0x00
	Peripheral count	0x1A4D	1	0x1C	0x1C	0x1B	0x1B	0x1B	0x1B
	MSP430CPUXV2	0x1A4E	2	0x2300	0x2300	0x2300	0x2300	0x2300	0x2300
	SBW	0x1A50	2	0x0F00	0x0F00	0x0F00	0x0F00	0x0F00	0x0F00
	EEM-S	0x1A52	2	0x0300	0x0300	0x0300	0x0300	0x0300	0x0300
	TI BSL	0x1A54	2	0xFC00	0xFC00	0xFC00	0xFC00	0xFC00	0xFC00
	SFR	0x1A56	2	0x4110	0x4110	0x4110	0x4110	0x4110	0x4110
	PMM	0x1A58	2	0x3002	0x3002	0x3002	0x3002	0x3002	0x3002
	FCTL	0x1A5A	2	0x3802	0x3802	0x3802	0x3802	0x3802	0x3802
	CRC16	0x1A5C	2	0x3C01	0x3C01	0x3C01	0x3C01	0x3C01	0x3C01
	CRC16_RB	0x1A5E	2	0x3D00	0x3D00	0x3D00	0x3D00	0x3D00	0x3D00
	RAMCTL	0x1A60	2	0x4400	0x4400	0x4400	0x4400	0x4400	0x4400
	WDT_A	0x1A62	2	0x4000	0x4000	0x4000	0x4000	0x4000	0x4000
	UCS	0x1A64	2	0x4801	0x4801	0x4801	0x4801	0x4801	0x4801
	SYS	0x1A66	2	0x4202	0x4202	0x4202	0x4202	0x4202	0x4202
	Shared REF	0x1A68	2	0xA003	0xA003	0xA003	0xA003	0xA003	0xA003
	Port Mapping	0x1A6A	2	0x1001	0x1001	0x1001	0x1001	0x1001	0x1001
	Port 1/2	0x1A6C	2	0x5104	0x5104	0x5104	0x5104	0x5104	0x5104
	Port 3/4	0x1A6E	2	0x5202	0x5202	0x5202	0x5202	0x5202	0x5202
	Port J	0x1A70	2	0x5F10	0x5F10	0x5F10	0x5F10	0x5F10	0x5F10
	TA0	0x1A72	2	0x610A	0x610A	0x610A	0x610A	0x610A	0x610A
	MPY32	0x1A74	2	0x8510	0x8510	0x8510	0x8510	0x8510	0x8510
	DMA with 3 channels	0x1A76	2	0x4704	0x4704	0x4704	0x4704	0x4704	0x4704
	USCI_A0/B0	0x1A78	2	0x900C	0x900C	0x900C	0x900C	0x900C	0x900C
	ADC10_A	0x1A7A	2	0xD318	0xD318	0xD318	0xD318	0xD318	0xD318
	COMP_B	0x1A7C	2	0xA818	0xA818	0x1A919	0xA818	0x1A919	0xA818
	TIMER_D0	0x1A7E	2	0xD624	0xD624	0xD624	0xD624	0xD624	0xD624
	TIMER_D1	0x1A80	2	0x6D04	0x6D04	0x6D04	0x6D04	0x6D04	0x6D04
	TEC_0	0x1A82	2	0x700C	0x700C	0x700C	0x700C	0x700C	0x700C
	TEC_1	0x1A84	2	0x7002	0x7002	0x7002	0x7002	0x7002	0x7002

Table 6-56. MSP430F51x2 Device Descriptor Table(1) (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE					
				F5172		F5152		F5132	
				RSB, YFF	DA	RSB	DA	RSB	DA
Interrupts	COMP_B	0x1A86	1	0xA8	0xA8	0xA8	0xA8	0xA8	0xA8
	TEC_0	0x1A87	1	0x6D	0x6D	0x6D	0x6D	0x6D	0x6D
	TIMER_D0	0x1A88	1	0x62	0x62	0x62	0x62	0x62	0x62
	TIMER_D0	0x1A89	1	0x63	0x63	0x63	0x63	0x63	0x63
	WDTIFG	0x1A8A	1	0x40	0x40	0x40	0x40	0x40	0x40
	USCI_A0	0x1A8B	1	0x90	0x90	0x90	0x90	0x90	0x90
	USCI_B0	0x1A8C	1	0x91	0x91	0x91	0x91	0x91	0x91
	ADC10_A	0x1A8D	1	0xD0	0xD0	0xD0	0xD0	0xD0	0xD0
	TA0.CCIFG0	0x1A8E	1	0x60	0x60	0x60	0x60	0x60	0x60
	TA0.CCIFG1..4	0x1A8F	1	0x61	0x61	0x61	0x61	0x61	0x61
	DMA	0x1A90	1	0x46	0x46	0x46	0x46	0x46	0x46
	TEC_1	0x1A91	1	0x6E	0x6E	0x6E	0x6E	0x6E	0x6E
	TIMER_D1	0x1A92	1	0x64	0x64	0x64	0x64	0x64	0x64
	TIMER_D1	0x1A93	1	0x65	0x65	0x65	0x65	0x65	0x65
	Port P1	0x1A94	1	0x50	0x50	0x50	0x50	0x50	0x50
	Port P2	0x1A95	1	0x51	0x51	0x51	0x51	0x51	0x51
	Delimiter	0x1A96	1	0x00	0x00	0x00	0x00	0x00	0x00
Empty	Unused memory	0x1A97 - 0x1AB9		0xFF	0xFF	0xFF	0xFF	0xFF	0xFF

Table 6-57. MSP430F51x1 Device Descriptor Table(1)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE					
				F5171		F5151		F5131	
				RSB	DA	RSB	DA	RSB	DA
Info Block	Info length	0x1A00	1	0x06	0x06	0x06	0x06	0x06	0x06
	CRC length	0x1A01	1	0x06	0x06	0x06	0x06	0x06	0x06
	CRC value	0x1A02	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Device ID	0x1A04	1	0x2E	0x2E	0x2A	0x2A	0x26	0x26
	Device ID	0x1A05	1	0x80	0x80	0x80	0x80	0x80	0x80
	Hardware revision	0x1A06	1	0x30	0x30	0x30	0x30	0x30	0x30
	Firmware revision	0x1A07	1	0x10	0x10	0x10	0x10	0x10	0x10
Die Record	Die record tag	0x1A08	1	0x08	08	0x08	08	0x08	08
	Die record length	0x1A09	1	0x0A	0A	0x0A	0A	0x0A	0A
	Lot/wafer ID	0x1A0A	4	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Die X position	0x1A0Eh	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Die Y position	0x1A10	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Test results	0x1A12	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit

(1) NA = Not applicable

Table 6-57. MSP430F51x1 Device Descriptor Table[(1)] (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE					
				F5171		F5151		F5131	
				RSB	DA	RSB	DA	RSB	DA
ADC10 Calibration	ADC10 calibration tag	0x1A14	1	0x05	0x05	0x05	0x05	0x05	0x05
	ADC10 calibration length	0x1A15	1	0x10	0x10	0x10	0x10	0x10	0x10
	ADC gain factor	0x1A16	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC offset	0x1A18	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V reference Temperature sensor 30°C	0x1A1A	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V reference Temperature sensor 85°C	0x1A1C	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V reference Temperature sensor 30°C	0x1A1Eh	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V reference Temperature sensor 85°C	0x1A20	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V reference Temperature sensor 30°C	0x1A22	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V reference Temperature sensor 85°C	0x1A24	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
REF User Calibration	REF tag	0x1A26	1	0x12	0x12	0x12	0x12	0x12	0x12
	REF length	0x1A27	1	0x06	0x06	0x06	0x06	0x06	0x06
	REF 1.5-V reference	0x1A28	2	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	REF 2.0-V reference	0x1A2A	2	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
	REF 2.5-V reference	0x1A2C	2	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF
Timer_D0 Calibration	Timer_D tag	0x1A2E	1	0x15	0x15	0x15	0x15	0x15	0x15
	Timer_D length	0x1A2F	1	0x08	0x08	0x08	0x08	0x08	0x08
	Timer_D 64-MHz frequency	0x1A30	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 128-MHz frequency	0x1A32	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 200-MHz frequency	0x1A34	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 256-MHz frequency	0x1A36	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
Timer_D1 Calibration	Timer_D tag	0x1A38	1	0x15	0x15	0x15	0x15	0x15	0x15
	Timer_D length	0x1A39	1	0x08	0x08	0x08	0x08	0x08	0x08
	Timer_D 64-MHz frequency	0x1A3A	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 128-MHz frequency	0x1A3C	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 200-MHz frequency	0x1A3E	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Timer_D 256-MHz frequency	0x1A40	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit

Table 6-57. MSP430F51x1 Device Descriptor Table[(1)] (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE					
				F5171		F5151		F5131	
				RSB	DA	RSB	DA	RSB	DA
Peripheral Descriptor	Peripheral descriptor tag	0x1A42	1	0x02	0x02	0x02	0x02	0x02	0x02
	Peripheral descriptor length	0x1A43	1	0x51	0x51	0x51	0x51	0x51	0x51
	BSL memory	0x1A44	2	0x8A08	0x8A08	0x8A08	0x8A08	0x8A08	0x8A08
	Information memory	0x1A46	2	0x860C	0x860C	0x860C	0x860C	0x860C	0x860C
	RAM	0x1A48	2	0x2A0E	0x2A0E	0x2A0E	0x2A0E	0x280E	0x280E
	Main memory	0x1A4A	2	0x9240	0x9240	0x9060	0x9060	0x8E70	0x8E70
	Delimiter	0x1A4C	1	0x00	0x00	0x00	0x00	0x00	0x00
	Peripheral count	0x1A4D	1	0x1B	0x1B	0x1B	0x1B	0x1B	0x1B
	MSP430CPUXV2	0x1A4E	2	0x2300	0x2300	0x2300	0x2300	0x2300	0x2300
	SBW	0x1A50	2	0x0F00	0x0F00	0x0F00	0x0F00	0x0F00	0x0F00
	EEM-S	0x1A52	2	0x0300	0x0300	0x0300	0x0300	0x0300	0x0300
	TI BSL	0x1A54	2	0xFC00	0xFC00	0xFC00	0xFC00	0xFC00	0xFC00
	SFR	0x1A56	2	0x4110	0x4110	0x4110	0x4110	0x4110	0x4110
	PMM	0x1A58	2	0x3002	0x3002	0x3002	0x3002	0x3002	0x3002
	FCTL	0x1A5A	2	0x3802	0x3802	0x3802	0x3802	0x3802	0x3802
	CRC16	0x1A5C	2	0x3C01	0x3C01	0x3C01	0x3C01	0x3C01	0x3C01
	CRC16_RB	0x1A5E	2	0x3D00	0x3D00	0x3D00	0x3D00	0x3D00	0x3D00
	RAMCTL	0x1A60	2	0x4400	0x4400	0x4400	0x4400	0x4400	0x4400
	WDT_A	0x1A62	2	0x4000	0x4000	0x4000	0x4000	0x4000	0x4000
	UCS	0x1A64	2	0x4801	0x4801	0x4801	0x4801	0x4801	0x4801
	SYS	0x1A66	2	0x4202	0x4202	0x4202	0x4202	0x4202	0x4202
	Shared REF	0x1A68	2	0xA003	0xA003	0xA003	0xA003	0xA003	0xA003
	Port Mapping	0x1A6A	2	0x1001	0x1001	0x1001	0x1001	0x1001	0x1001
	Port 1/2	0x1A6C	2	0x5104	0x5104	0x5104	0x5104	0x5104	0x5104
	Port 3/4	0x1A6E	2	0x5202	0x5202	0x5202	0x5202	0x5202	0x5202
	Port J	0x1A70	2	0x5F10	0x5F10	0x5F10	0x5F10	0x5F10	0x5F10
	TA0	0x1A72	2	0x610A	0x610A	0x610A	0x610A	0x610A	0x610A
	MPY32	0x1A74	2	0x8510	0x8510	0x8510	0x8510	0x8510	0x8510
	DMA with 3 channels	0x1A76	2	0x4704	0x4704	0x4704	0x4704	0x4704	0x4704
	USCI_A0/B0	0x1A78	2	0x900C	0x900C	0x900C	0x900C	0x900C	0x900C
	COMP_B	0x1A7A	2	0xA830	0xA830	0xA830	0xA830	0xA830	0xA830
	TIMER_D0	0x1A7C	2	0xD624	0xD624	0xD624	0xD624	0xD624	0xD624
	TIMER_D1	0x1A7E	2	0x6D04	0x6D04	0x6D04	0x6D04	0x6D04	0x6D04
	TEC_0	0x1A80	2	0x700C	0x700C	0x700C	0x700C	0x700C	0x700C
	TEC_1	0x1A82	2	0x7002	0x7002	0x7002	0x7002	0x7002	0x7002

Table 6-57. MSP430F51x1 Device Descriptor Table[(1)] (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE					
				F5171		F5151		F5131	
				RSB	DA	RSB	DA	RSB	DA
Interrupts	COMP_B	0x1A83	1	0xA8	0xA8	0xA8	0xA8	0xA8	0xA8
	TEC_0	0x1A84	1	0x6D	0x6D	0x6D	0x6D	0x6D	0x6D
	TIMER_D0	0x1A85	1	0x62	0x62	0x62	0x62	0x62	0x62
	TIMER_D0	0x1A86	1	0x63	0x63	0x63	0x63	0x63	0x63
	WDTIFG	0x1A87	1	0x40	0x40	0x40	0x40	0x40	0x40
	USCI_A0	0x1A88	1	0x90	0x90	0x90	0x90	0x90	0x90
	USCI_B0	0x1A89	1	0x91	0x91	0x91	0x91	0x91	0x91
	ADC10_A	0x1A8A	1	0xD0	0xD0	0xD0	0xD0	0xD0	0xD0
	TA0.CCIFG0	0x1A8B	1	0x60	0x60	0x60	0x60	0x60	0x60
	TA0.CCIFG1..4	0x1A8C	1	0x61	0x61	0x61	0x61	0x61	0x61
	DMA	0x1A8D	1	0x46	0x46	0x46	0x46	0x46	0x46
	TEC_1	0x1A8E	1	0x6E	0x6E	0x6E	0x6E	0x6E	0x6E
	TIMER_D1	0x1A8F	1	0x64	0x64	0x64	0x64	0x64	0x64
	TIMER_D1	0x1A90	1	0x65	0x65	0x65	0x65	0x65	0x65
	Port P1	0x1A91	1	0x50	0x50	0x50	0x50	0x50	0x50
	Port P2	0x1A92	1	0x51	0x51	0x51	0x51	0x51	0x51
	Delimiter	0x1A93	1	0x00	0x00	0x00	0x00	0x00	0x00
Empty	Unused Memory	0x1A94–0x1AB9		0xFF	0xFF	0xFF	0xFF	0xFF	0xFF

7 Device and Documentation Support

7.1 Getting Started and Next Steps

For more information on the MSP430 family of devices and the tools and libraries that are available to help with your development, visit the MSP430 ultra-low-power sensing & measurement MCUs overview.

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

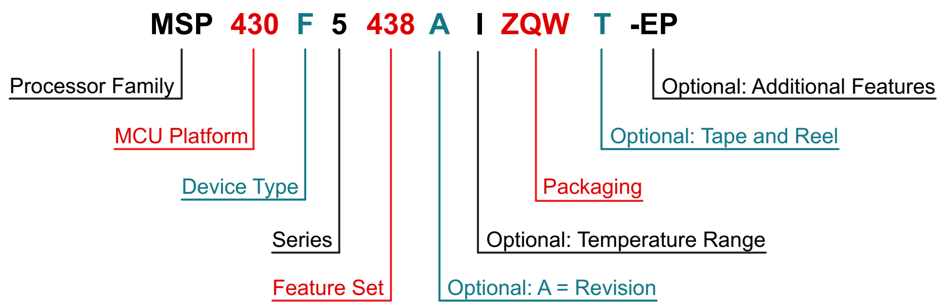
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 7-1 provides a legend for reading the complete device name.



Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	**Specialized Application** AFE = Analog Front End BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD 0 = Low-Voltage Series
Feature Set	Various levels of integration within a series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced Product (–40°C to 105°C) -HT = Extreme Temperature Parts (–55°C to 150°C) -Q1 = Automotive Q100 Qualified	

Figure 7-1. Device Nomenclature

7.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at MSP430 Ultra-Low-Power MCUs – Tools & software.

Table 7-1 lists the debug features of these MCUs. See the *Code Composer Studio IDE for MSP430 User's Guide* for details on the available features.

Table 7-1. Hardware Debug Features

MSP430 ARCHITECTURE	4-WIRE JTAG	2-WIRE JTAG	BREAK-POINTS (N)	RANGE BREAK-POINTS	CLOCK CONTROL	STATE SEQUENCER	TRACE BUFFER	LPMx.5 DEBUGGING SUPPORT
MSP430Xv2	Yes	Yes	3	Yes	Yes	No	No	No

Design Kits and Evaluation Modules

MSP430 40-Pin Package Board and USB Programmer The MSP-FET430U40 is a bundle featuring a standalone 40-pin ZIF socket target board which is used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol and the MSP-FET Flash Emulation Tool.

MSP430 40-Pin Target Development Board for MSP430F5x MCUs The MSP-TS430RSB40 is a stand-alone 40-pin ZIF socket target board that is used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol.

Software

MSP430Ware™ Software MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of Code Composer Studio™ IDE or as a stand-alone package.

MSP430F51x2, MSP430F51x1 Code Examples C Code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

MSP Driver Library Driver Library's abstracted API keeps you above the bits and bytes of the MSP430 hardware by providing easy-to-use function calls. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

MSP EnergyTrace™ Technology EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption.

ULP (Ultra-Low Power) Advisor ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully utilize the unique ultra-low power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to squeeze every last nano amp out of your application. At build time, ULP Advisor will provide notifications and remarks to highlight areas of your code that can be further optimized for lower power.

IEC60730 Software Package The IEC60730 MSP430 software package was developed to be useful in assisting customers in complying with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC60730 MSP430 software package can be embedded in customer applications running on MSP430s to help simplify the customer's certification efforts of functional safety-compliant consumer devices to IEC 60730-1:2010 Class B.

Fixed Point Math Library for MSP The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

Floating Point Math Library for MSP430 Continuing to innovate in the low power and low cost microcontroller space, TI brings you MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating point math library of scalar functions brings you up to 26x better performance. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio and IAR IDEs. Read the user’s guide for an in depth look at the math library and relevant benchmarks.

Development Tools

Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers Code Composer Studio is an integrated development environment (IDE) that supports all MSP microcontroller devices. Code Composer Studio comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar utilities and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers. When using CCS with an MSP MCU, a unique and powerful set of plugins and embedded software utilities are made available to fully leverage the MSP microcontroller.

Command-Line Programmer MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) files directly to the MSP microcontroller without an IDE.

MSP MCU Programmer and Debugger The MSP-FET is a powerful emulation development tool – often called a debug probe – which allows users to quickly begin application development on MSP low-power microcontrollers (MCU). Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging. The MSP-FET provides a debug communication pathway between a host computer and the target MSP. Furthermore, the MSP-FET also provides a Backchannel UART connection between the computer's USB interface and the MSP UART. This affords the MSP programmer a convenient method for communicating serially between the MSP and a terminal running on the computer. It also supports loading programs (often called firmware) to the MSP target using the BSL (bootloader) through the UART and I^2C communication protocols.

MSP-GANG Production Programmer The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 Flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that allow the user to fully customize the process. The MSP Gang Programmer is provided with an expansion board, called the Gang Splitter, that implements the interconnections between the MSP Gang Programmer and multiple target devices. Eight cables are provided that connect the expansion board to eight target devices (through JTAG or Spy-Bi-Wire connectors). The programming can be done with a PC or as a stand-alone device. A PC-side graphical user interface is also available and is DLL-based.

7.4 Documentation Support

The following documents describe the MSP430F51x2 and MSP430F51x1 devices. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for links to the product folder, see Section 7.5). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

MSP430F5172 Device Erratasheet Describes the known exceptions to the functional specifications for all silicon revisions of the device.

MSP430F5152 Device Erratasheet Describes the known exceptions to the functional specifications for all silicon revisions of the device.

MSP430F5132 Device Erratasheet Describes the known exceptions to the functional specifications for all silicon revisions of the device.

MSP430F5171 Device Erratasheet Describes the known exceptions to the functional specifications for all silicon revisions of the device.

MSP430F5151 Device Erratasheet Describes the known exceptions to the functional specifications for all silicon revisions of the device.

MSP430F5131 Device Erratasheet Describes the known exceptions to the functional specifications for all silicon revisions of the device.

User's Guides

MSP430F5xx and MSP430F6xx Family User's Guide Detailed information on the modules and peripherals available in this device family.

MSP430 Flash Device Bootloader (BSL) User's Guide The MSP430 bootloader (BSL) lets users communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

MSP430 Programming With the JTAG Interface This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

MSP430 Hardware Tools User's Guide This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

Application Reports

MSP430 32-kHz Crystal Oscillators Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

MSP430 System-Level ESD Considerations System-Level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three different ESD topics to help board designers and OEMs understand and design robust system-level designs: (1) Component-level ESD testing and system-level ESD testing, their differences and why component-level ESD rating does not ensure system-level robustness. (2) General design guidelines for system-level ESD protection at different levels including enclosures, cables, PCB layout, and on-board ESD protection devices. (3) Introduction to System Efficient ESD Design (SEED), a co-design methodology of on-board and on-chip ESD protection to achieve system-level ESD robustness, with example simulations and test results. A few real-world system-level ESD protection design examples and their results are also discussed.

7.5 Related Links

Table 7-2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
MSP430F5172	Click here	Click here	Click here	Click here	Click here
MSP430F5152	Click here	Click here	Click here	Click here	Click here
MSP430F5132	Click here	Click here	Click here	Click here	Click here
MSP430F5171	Click here	Click here	Click here	Click here	Click here
MSP430F5151	Click here	Click here	Click here	Click here	Click here
MSP430F5131	Click here	Click here	Click here	Click here	Click here

7.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community
TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki
Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.7 Trademarks

MSP430, MSP430Ware, Code Composer Studio, EnergyTrace, ULP Advisor, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

7.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F5131IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F5131	Samples
MSP430F5131IDAR	ACTIVE	TSSOP	DA	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F5131	Samples
MSP430F5131IRSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5131	Samples
MSP430F5131IRSBT	ACTIVE	WQFN	RSB	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5131	Samples
MSP430F5131IYFFR	ACTIVE	DSBGA	YFF	40	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5131	Samples
MSP430F5131IYFFT	ACTIVE	DSBGA	YFF	40	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5131	Samples
MSP430F5132IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F5132	Samples
MSP430F5132IDAR	ACTIVE	TSSOP	DA	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F5132	Samples
MSP430F5132IRSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5132	Samples
MSP430F5132IRSBT	ACTIVE	WQFN	RSB	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5132	Samples
MSP430F5132IYFFR	ACTIVE	DSBGA	YFF	40	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5132	Samples
MSP430F5132IYFFT	ACTIVE	DSBGA	YFF	40	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5132	Samples
MSP430F5151IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F5151	Samples
MSP430F5151IRSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5151	Samples
MSP430F5151IRSBT	ACTIVE	WQFN	RSB	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5151	Samples
MSP430F5151IYFFR	ACTIVE	DSBGA	YFF	40	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5151	Samples
MSP430F5151IYFFT	ACTIVE	DSBGA	YFF	40	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5151	Samples
MSP430F5152IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F5152	Samples
MSP430F5152IDAR	ACTIVE	TSSOP	DA	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F5152	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F5152IRSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5152	Samples
MSP430F5152IRSBT	ACTIVE	WQFN	RSB	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5152	Samples
MSP430F5152IYFFR	ACTIVE	DSBGA	YFF	40	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5152	Samples
MSP430F5152IYFFT	ACTIVE	DSBGA	YFF	40	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5152	Samples
MSP430F5171IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F5171	Samples
MSP430F5171IDAR	ACTIVE	TSSOP	DA	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F5171	Samples
MSP430F5171IRSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5171	Samples
MSP430F5171IRSBT	ACTIVE	WQFN	RSB	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5171	Samples
MSP430F5171IYFFR	ACTIVE	DSBGA	YFF	40	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5171	Samples
MSP430F5171IYFFT	ACTIVE	DSBGA	YFF	40	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5171	Samples
MSP430F5172IDA	ACTIVE	TSSOP	DA	38	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F5172	Samples
MSP430F5172IDAR	ACTIVE	TSSOP	DA	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430F5172	Samples
MSP430F5172IRSBR	ACTIVE	WQFN	RSB	40	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5172	Samples
MSP430F5172IRSBT	ACTIVE	WQFN	RSB	40	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	M430 F5172	Samples
MSP430F5172IYFFR	ACTIVE	DSBGA	YFF	40	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5172	Samples
MSP430F5172IYFFT	ACTIVE	DSBGA	YFF	40	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5172	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

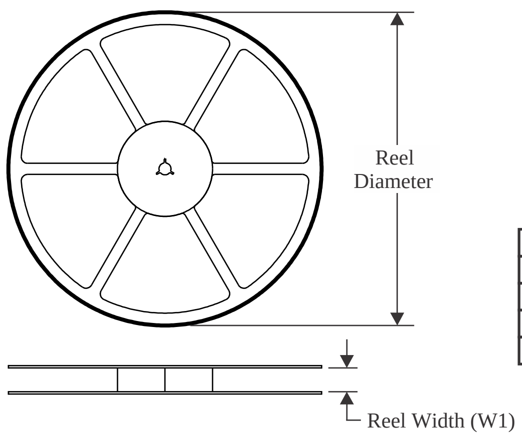
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

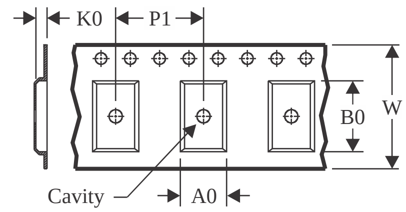
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

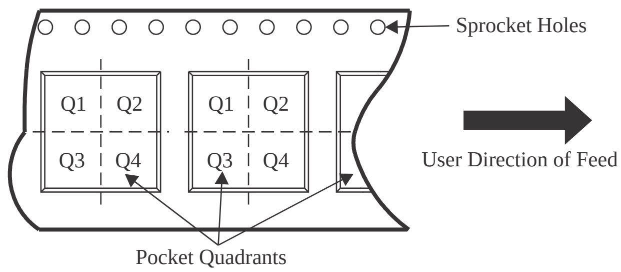


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

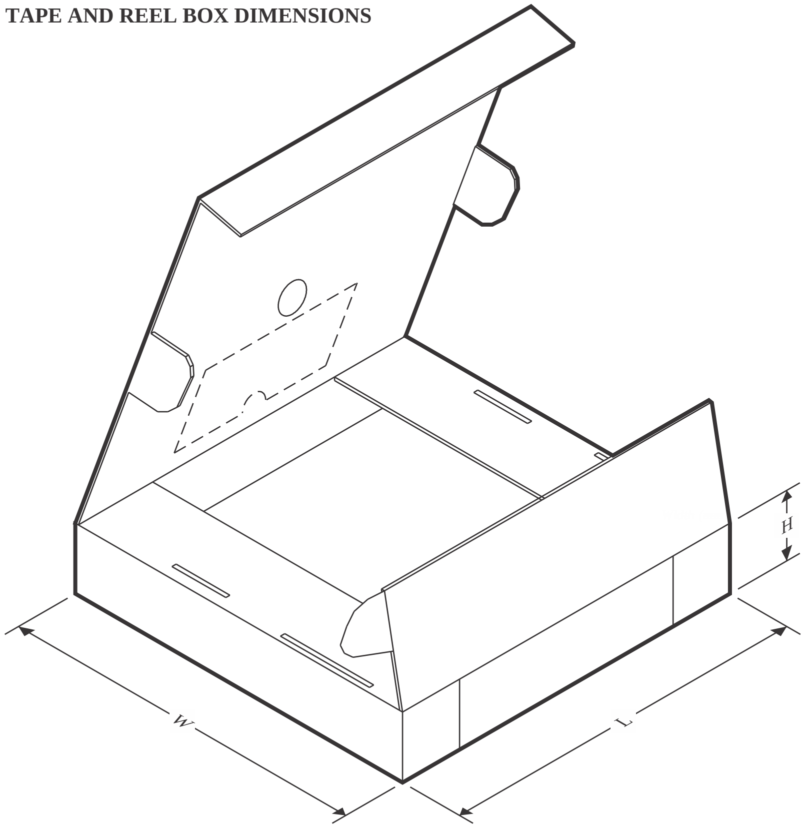


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5131IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430F5131IRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430F5131IRSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430F5131IYFFR	DSBGA	YFF	40	3000	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1
MSP430F5131IYFFT	DSBGA	YFF	40	250	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1
MSP430F5132IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430F5132IRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430F5132IRSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430F5132IYFFR	DSBGA	YFF	40	3000	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1
MSP430F5132IYFFT	DSBGA	YFF	40	250	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1
MSP430F5151IRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430F5151IRSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430F5151IYFFR	DSBGA	YFF	40	3000	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1
MSP430F5151IYFFT	DSBGA	YFF	40	250	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1
MSP430F5152IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430F5152IRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5152IRSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430F5152IYFFR	DSBGA	YFF	40	3000	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1
MSP430F5152IYFFT	DSBGA	YFF	40	250	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1
MSP430F5171IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430F5171IRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430F5171IRSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430F5171IYFFR	DSBGA	YFF	40	3000	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1
MSP430F5171IYFFT	DSBGA	YFF	40	250	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1
MSP430F5172IDAR	TSSOP	DA	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
MSP430F5172IRSBR	WQFN	RSB	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430F5172IRSBT	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430F5172IYFFR	DSBGA	YFF	40	3000	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1
MSP430F5172IYFFT	DSBGA	YFF	40	250	180.0	8.4	2.86	3.16	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

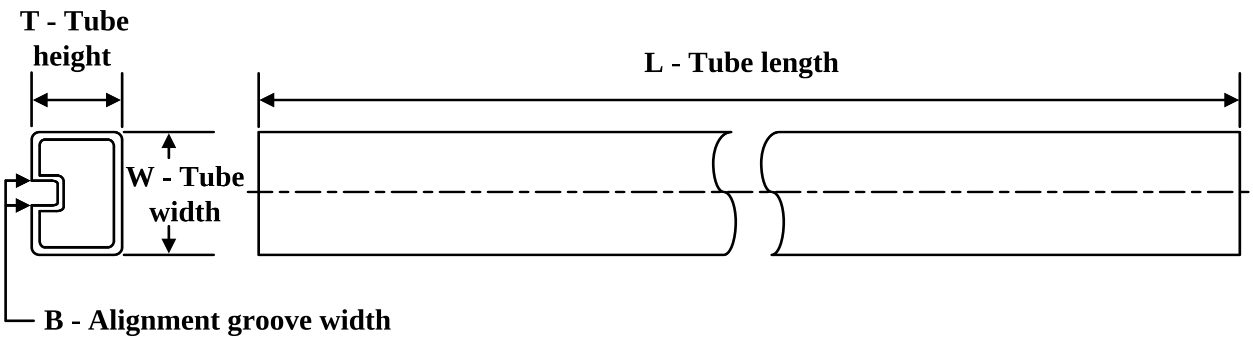


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5131IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430F5131IRSBR	WQFN	RSB	40	3000	367.0	367.0	35.0
MSP430F5131IRSBT	WQFN	RSB	40	250	210.0	185.0	35.0
MSP430F5131IYFFR	DSBGA	YFF	40	3000	182.0	182.0	20.0
MSP430F5131IYFFT	DSBGA	YFF	40	250	182.0	182.0	20.0
MSP430F5132IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430F5132IRSBR	WQFN	RSB	40	3000	367.0	367.0	35.0
MSP430F5132IRSBT	WQFN	RSB	40	250	210.0	185.0	35.0
MSP430F5132IYFFR	DSBGA	YFF	40	3000	182.0	182.0	20.0
MSP430F5132IYFFT	DSBGA	YFF	40	250	182.0	182.0	20.0
MSP430F5151IRSBR	WQFN	RSB	40	3000	367.0	367.0	35.0
MSP430F5151IRSBT	WQFN	RSB	40	250	210.0	185.0	35.0
MSP430F5151IYFFR	DSBGA	YFF	40	3000	182.0	182.0	20.0
MSP430F5151IYFFT	DSBGA	YFF	40	250	182.0	182.0	20.0
MSP430F5152IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430F5152IRSBR	WQFN	RSB	40	3000	367.0	367.0	35.0
MSP430F5152IRSBT	WQFN	RSB	40	250	210.0	185.0	35.0
MSP430F5152IYFFR	DSBGA	YFF	40	3000	182.0	182.0	20.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5152IYFFT	DSBGA	YFF	40	250	182.0	182.0	20.0
MSP430F5171IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430F5171IRSBR	WQFN	RSB	40	3000	367.0	367.0	35.0
MSP430F5171IRSBT	WQFN	RSB	40	250	210.0	185.0	35.0
MSP430F5171IYFFR	DSBGA	YFF	40	3000	182.0	182.0	20.0
MSP430F5171IYFFT	DSBGA	YFF	40	250	182.0	182.0	20.0
MSP430F5172IDAR	TSSOP	DA	38	2000	350.0	350.0	43.0
MSP430F5172IRSBR	WQFN	RSB	40	3000	367.0	367.0	35.0
MSP430F5172IRSBT	WQFN	RSB	40	250	210.0	185.0	35.0
MSP430F5172IYFFR	DSBGA	YFF	40	3000	182.0	182.0	20.0
MSP430F5172IYFFT	DSBGA	YFF	40	250	182.0	182.0	20.0

TUBE

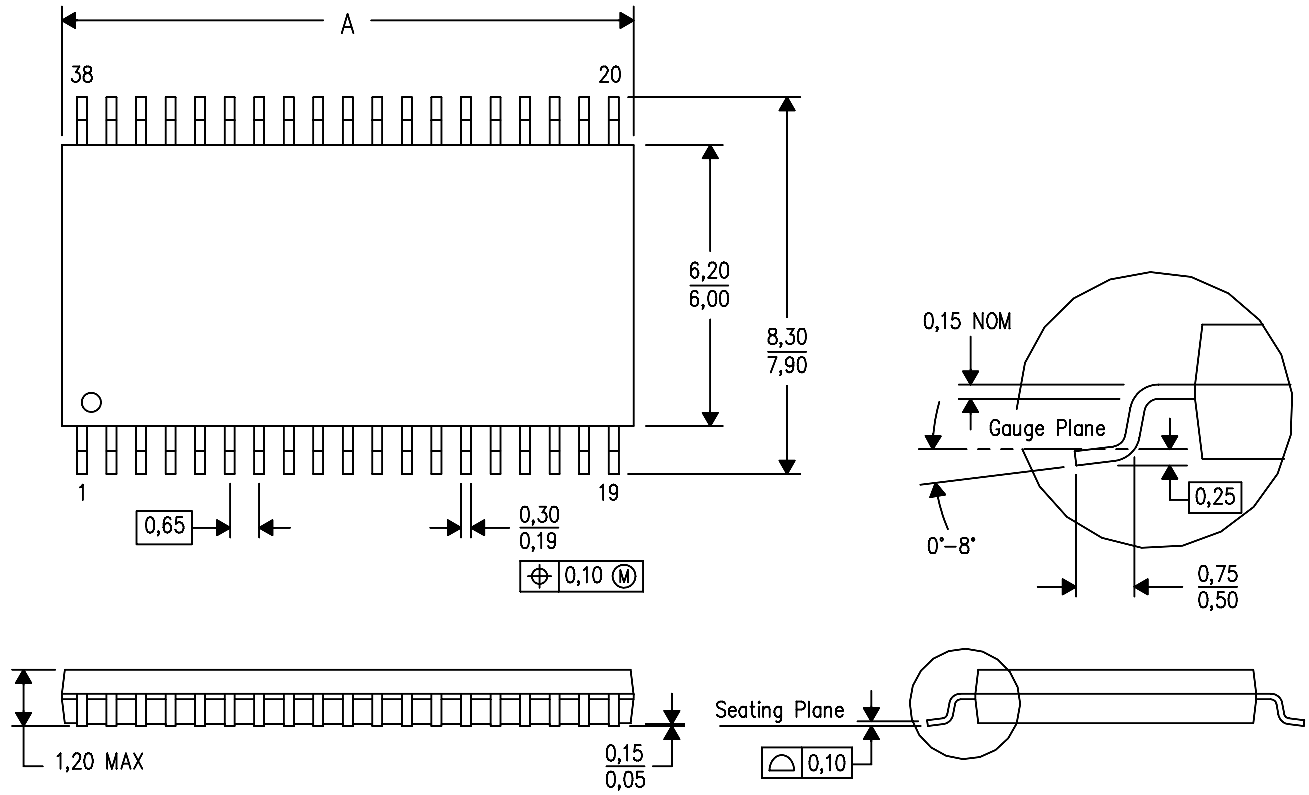


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430F5131IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430F5132IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430F5151IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430F5152IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430F5171IDA	DA	TSSOP	38	40	530	11.89	3600	4.9
MSP430F5172IDA	DA	TSSOP	38	40	530	11.89	3600	4.9

DA (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

38 PIN SHOWN

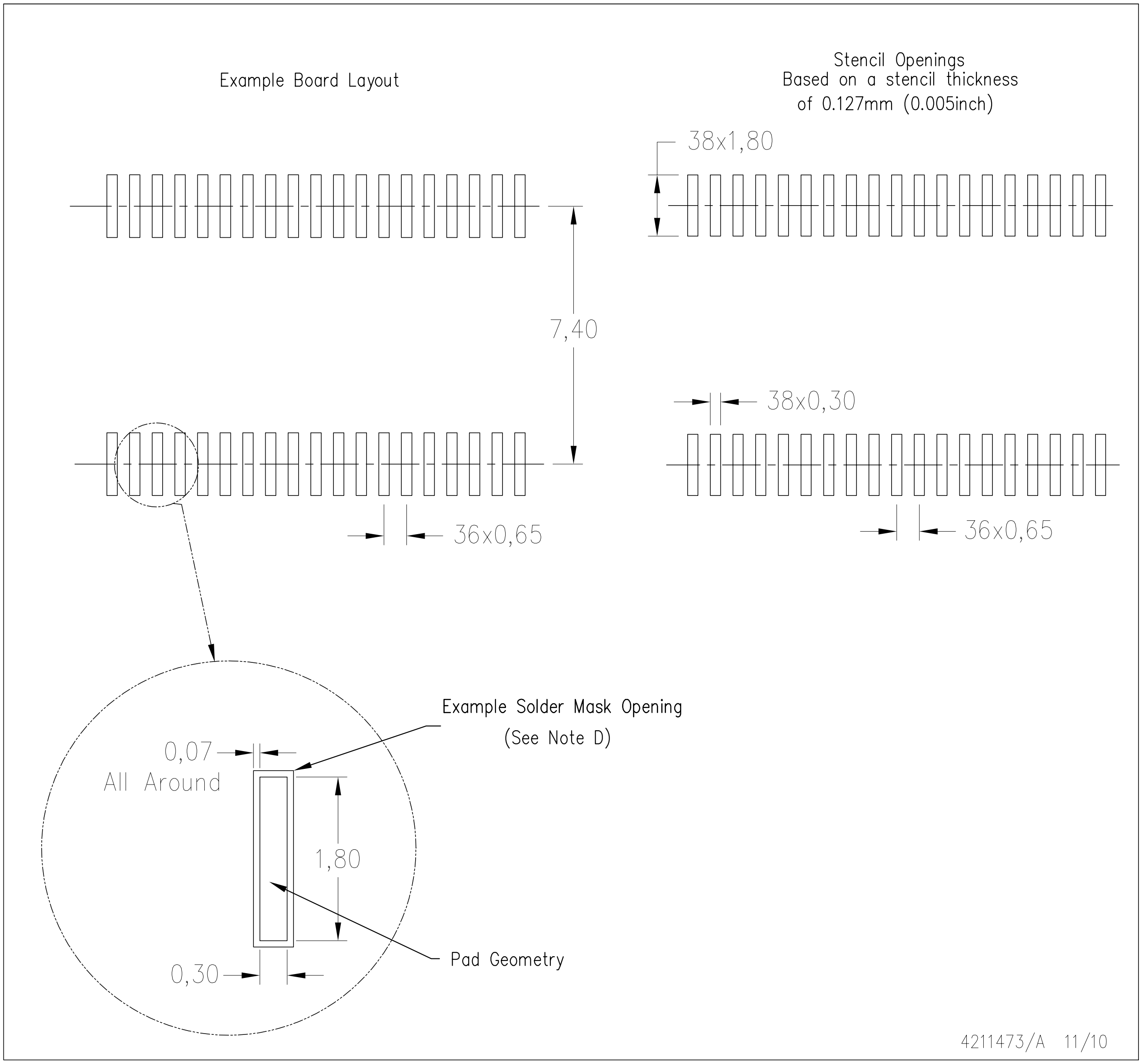


PINS ** / DIM	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
(D) MO–153 Variation	DB–1	DC	DD–1

4040066/F 01/2009

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
(D) Falls within JEDEC MO–153, except 30 pin body length.

DA (R–PDSO–G38) PLASTIC SMALL OUTLINE

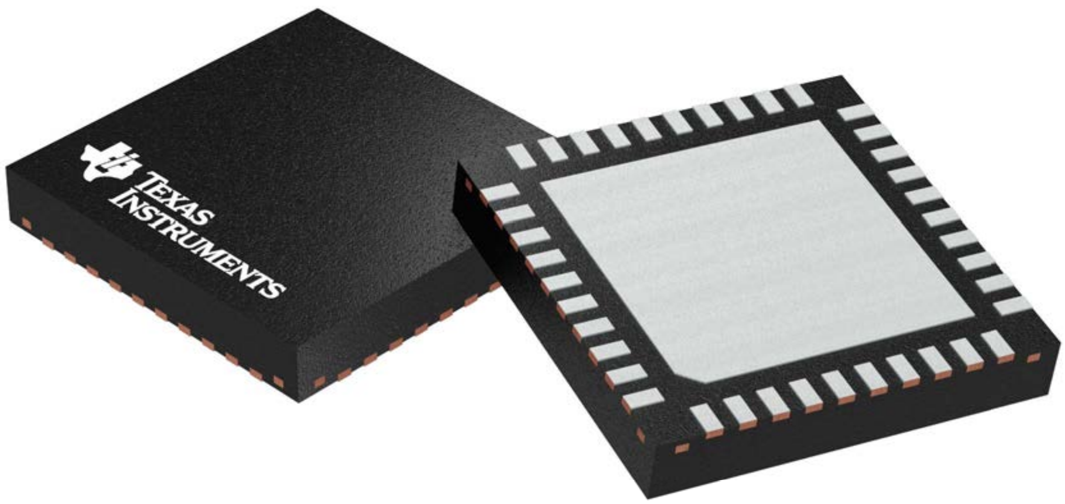


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Contact the board fabrication site for recommended soldermask tolerances.

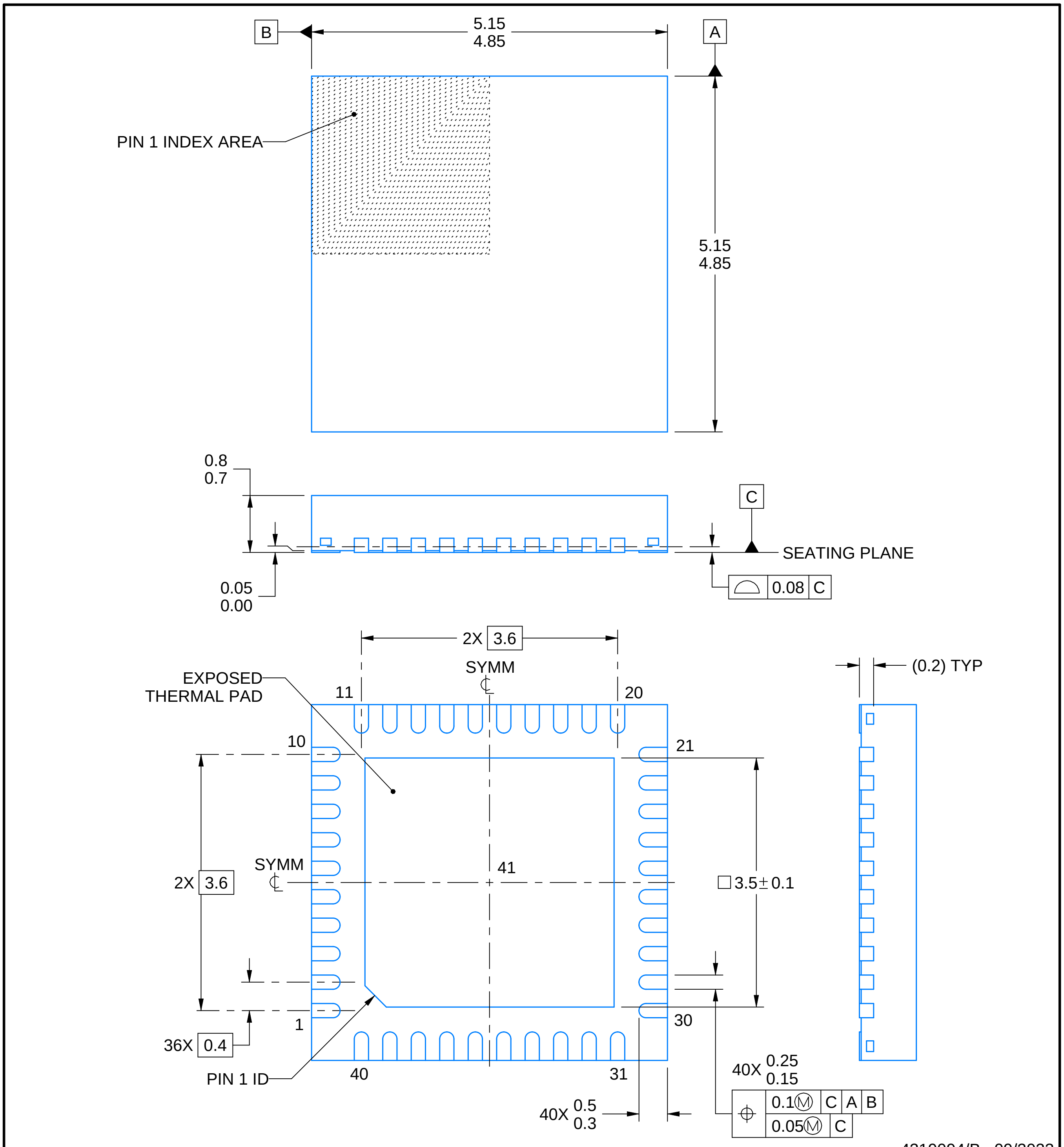
RSB 40 WQFN - 0.8 mm max height

5 x 5 mm, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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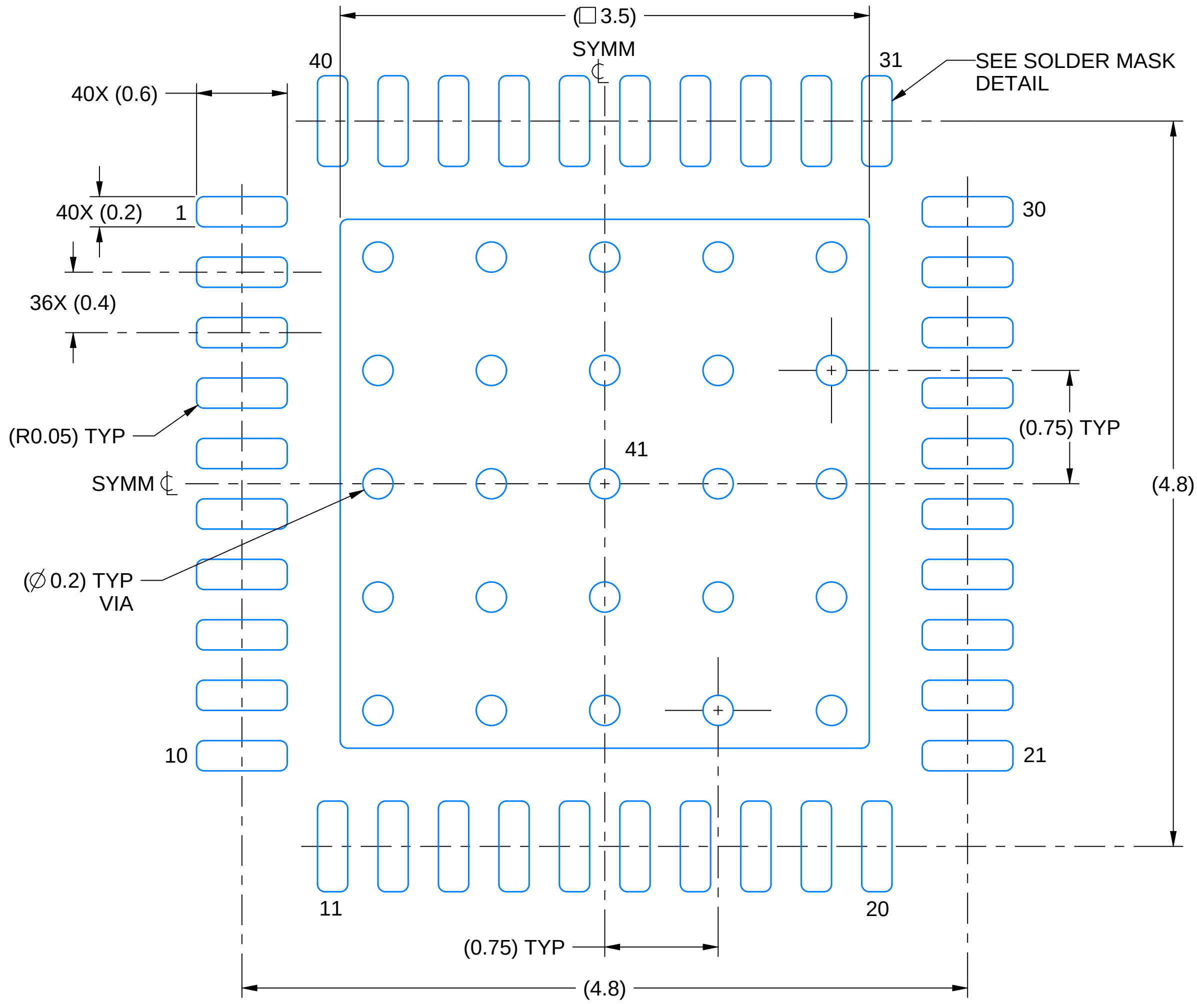
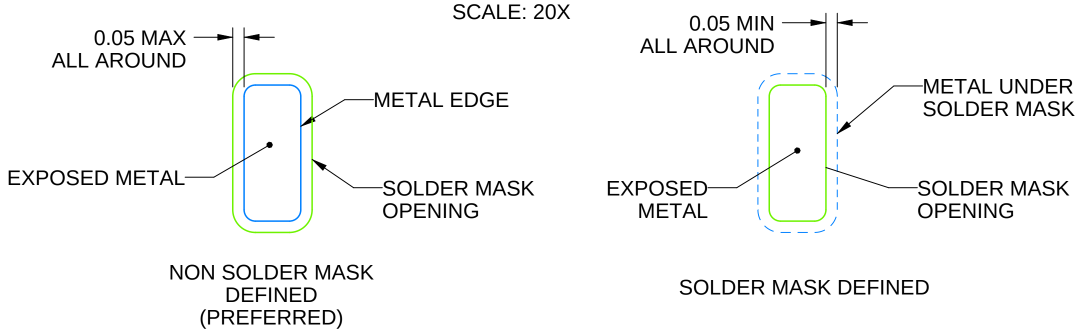
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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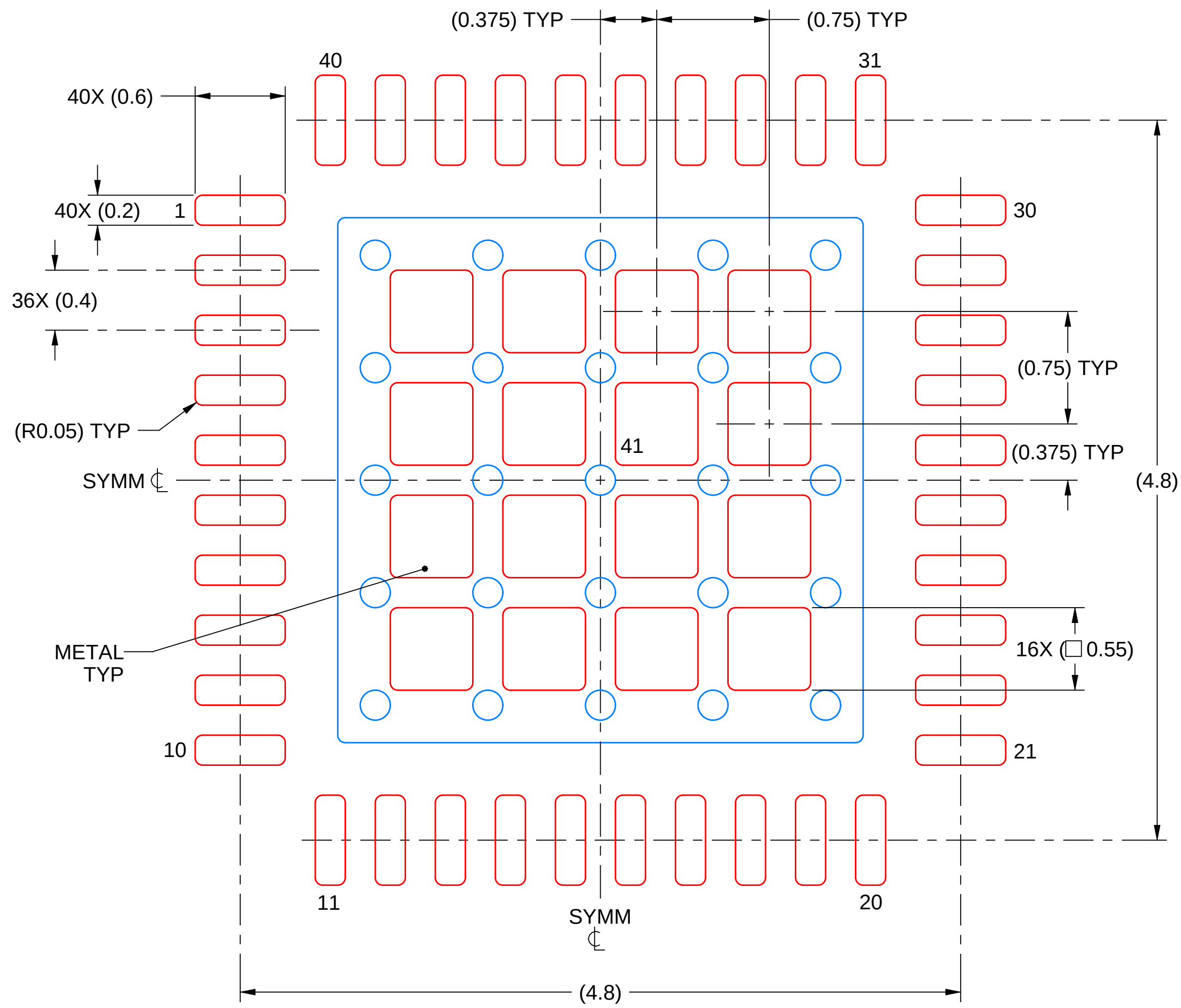
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 41
40% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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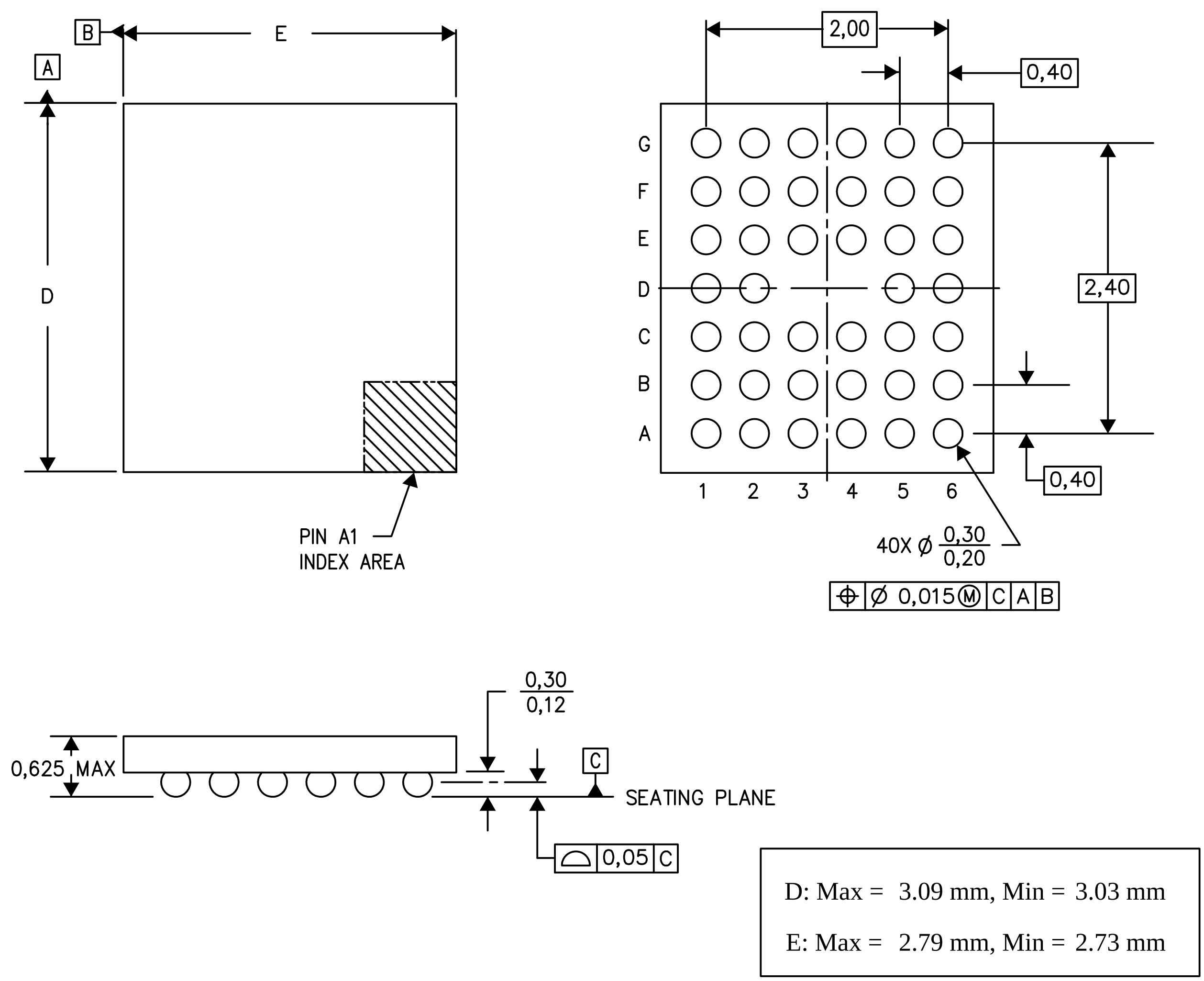
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YFF (R–XBGA–N40) DIE–SIZE BALL GRID ARRAY



4207625–35/A0 12/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265